UCD9244-EP Digital PWM System Controller with 4-Bit, 6-Bit, or 8-Bit VID Support

1 Features

- Fully Configurable Four-Output Non-Isolated DC/DC PWM Controller with support for TMS320C6670™ and TMS320C6678™ DSP VID interface
- Supports Switching Frequencies Up to 2MHz With 250 ps Duty-Cycle Resolution
- Up To 1mV Closed Loop Resolution
- Hardware-Accelerated, 3-Pole/3-Zero Compensator with Non-Linear Gain for Improved Transient Performance
- Supports Multiple Soft-Start and Soft-Stop Configurations Including Prebias Start-up
- Supports Voltage Margining and Sequencing
- Sync In Terminal Aligns DPWM Clocks Between Multiple UCD92xx Devices
- 12-Bit Digital Monitoring of Power Supply Parameters Including:
  - Input Current and Voltage
  - Output Current and Voltage
  - Temperature at Each Power Stage
  - Auxiliary ADC Inputs
- Multiple Levels of Over-current Fault Protection:
  - External Current Fault Inputs
  - Analog Comparators Monitor Current Sense Voltage
  - Current Continually Digitally Monitored
- Over and Under-voltage Fault Protection
- Over-temperature Fault Protection
- Enhanced Nonvolatile Memory With Error Correction Code (ECC)
- Device Operates From a Single Supply With an Internal Regulator Controller That Allows Operation Over a Wide Supply Voltage Range
- Supported by Fusion Digital Power™ Designer, a Full Featured PC Based Design Tool to Simulate, Configure, and Monitor Power Supply Performance.
- Supports Defense, Aerospace, and Medical Applications
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military (–55°C to 125°C) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

2 Applications

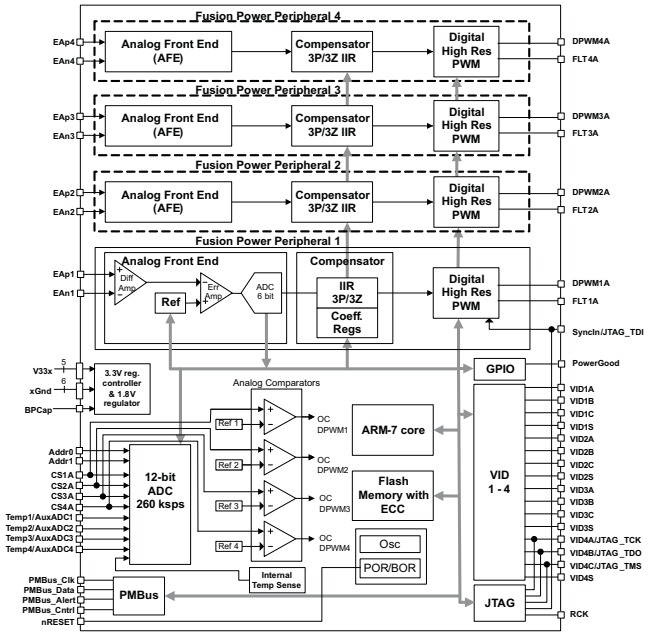
- Networking Equipment
- Telecommunications Equipment
- FPGA, DSP, and Memory Power

3 Description

The UCD9244 is a four-rail synchronous buck digital PWM controller designed for non-isolated DC/DC power applications. This device integrates dedicated circuitry for DC/DC loop management with support for up to four VID interfaces. Additionally, the UCD9244 has flash memory and a serial interface to support configurability, monitoring and management.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
UCD9244MRGCTEP	QFN (64)	9mm × 9mm



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4 Revision History

Changes from Original (January 2014) to Revision A **Page**

- Changed format to meet latest standards, added Detailed Description and Power Supply sections ... 1
- Added footnote to $t_{retention}$ parameter ... 9

5 Description (Continued)

Several Voltage Identification (VID) modes are supported, including a 4-bit parallel interface, a 6-bit interface and an 8-bit serial interface.

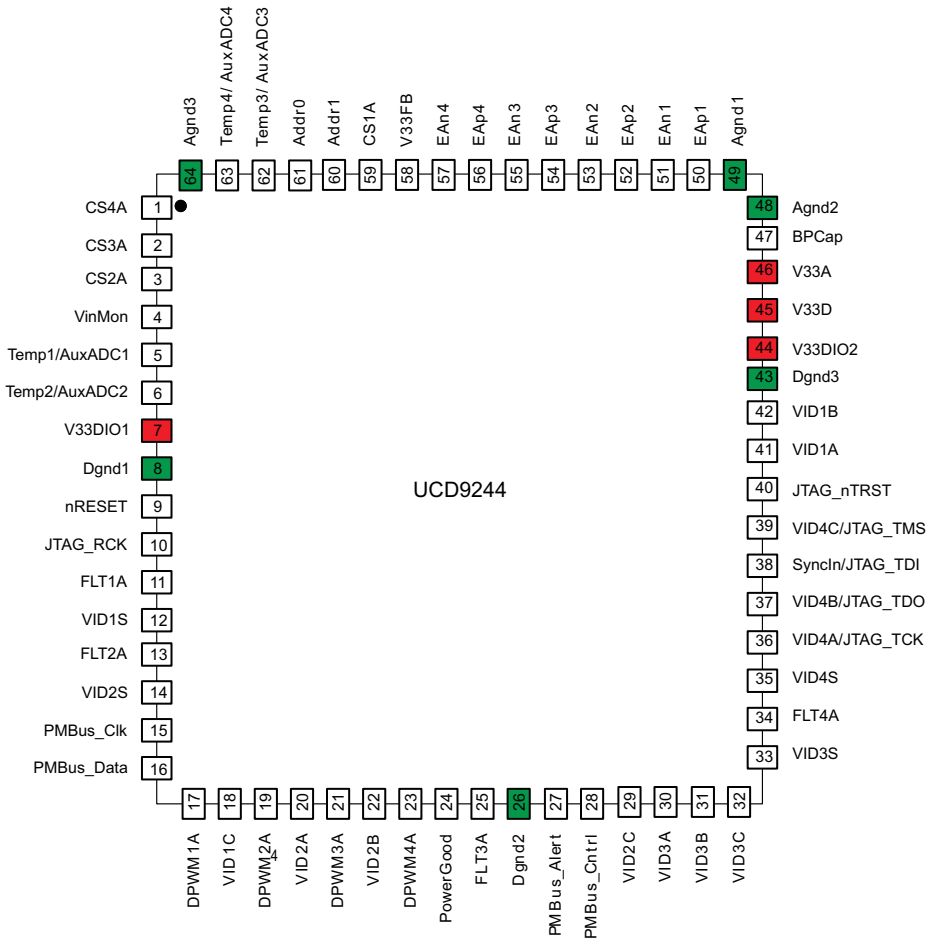
The UCD9244 was designed to provide a wide variety of desirable features for non-isolated DC/DC converter applications while minimizing the total system component count by reducing external circuits. The solution integrates multi-loop management with sequencing, margining and tracking to optimize for total system efficiency. Additionally, loop compensation and calibration are supported without the need to add external components.

To facilitate configuring the device, the Texas Instruments Fusion Digital Power™ Designer is provided. This PC based Graphical User Interface offers an intuitive interface to the device. This tool allows the design engineer to configure the system operating parameters for the application, store the configuration to on-chip non-volatile memory and observe both frequency domain and time domain simulations for each of the power stage outputs.

TI has also developed multiple complementary power stage solutions – from discrete drivers in the UCD7k family to fully tested power train modules in the PTD family. These solutions have been developed to complement the UCD92xx family of system power controllers.

6 Terminal Configuration and Functions

RGC Package
QFN-64
(Top View)



(1) In case of conflict between and the table shall take precedence

(2) Preliminary versions of this data sheet prior to June 14, 2010 had a different definition for terminals 17, 18, and 21. Board designs made with that earlier pinout should be updated.

Terminal Functions

TERMINAL NUMBER	TERMINAL LABEL	TERMINAL DESCRIPTION
1	CS4A	Power stage 4A current sense input and input to analog comparator 4
2	CS3A	Power stage 3A current sense input and input to analog comparator 3
3	CS2A	Power stage 2A current sense input and input to analog comparator 2
4	VinMon	Input Voltage monitor
5	Temp1/AuxADC1	Temperature sense input for Rail 1, or Auxiliary ADC input 1
6	Temp2/AuxADC2	Temperature sense input for Rail 2, or Auxiliary ADC input 2
7	V33DIO1	Digital Input / Output 3.3V supply
8	Dgnd1	Digital ground
9	nRESET	Active low device reset input. Pull up to 3.3V with a 10kΩ resistor
10	JTAG_RCK	JTAG Return Clock
11	FLT1A	Fault indicator for stage 1A
12	VID1S	VID Select terminal for Rail 1
13	FLT2A	Fault indicator for stage 2A
14	VID2S	VID Select terminal for Rail 2
15	PMBus_Clk	PMBus Clock. Pull up to 3.3V with a 2kΩ resistor
16	PMBus_Data	PMBus Data. Pull up to 3.3V with a 2kΩ resistor
17	DPWM1A	Digital Pulse Width Modulator output 1A
18	VID1C	VID input terminal for Rail 1 - most significant bit
19	DPWM2A	Digital Pulse Width Modulator output 2A
20	VID2A	VID input terminal for Rail 2 - least significant bit
21	DPWM3A	Digital Pulse Width Modulator output 3A
22	VID2B	VID input terminal for Rail 2
23	DPWM4A	Digital Pulse Width Modulator output 4A
24	Power_Good	Power Good Indication
25	FLT3A	Fault indicator for stage 3A
26	Dgnd2	Digital Ground
27	PMBus_Alert	PMBus Alert. Pull up to 3.3V with a 2kΩ resistor
28	PMBus_Cntrl	PMBus Control. Pull up to 3.3V with a 2kΩ resistor
29	VID2C	VID input terminal for Rail 2 - most significant bit
30	VID3A	VID input terminal for Rail 3 - least significant bit
31	VID3B	VID input terminal for Rail 3
32	VID3C	VID input terminal for Rail 3 - most significant bit
33	VID3S	VID Select terminal for Rail 3
34	FLT4A	Fault indicator for stage 4A
35	VID4S	VID Select terminal for Rail 4
36	VID4A/JTAG_TCK	Mux'ed terminal - VID input terminal for Rail 4 (LSB), JTAG Test Clock
37	VID4B/JTAG_TDO	Mux'ed terminal - VID input terminal for Rail 4, JTAG Test Data Output
38	SyncIn/JTAG_TDI	Mux'ed terminal - SyncIn, JTAG Test Data In. Tie to V33D with 10kΩ resistor
39	VID4C/JTAG_TMS	Mux'ed terminal - VID input for rail 4 (MSB); JTAG Test mode select. Tie to V33D with a 10kΩ resistor
40	JTAG_nTRST	JTAG Test Reset - Tie to ground with a 10kohm resistor
41	VID1A	VID input terminal for Rail 1 - least significant bit
42	VID1B	VID input terminal for Rail 1
43	Dgnd3	Digital Ground
44	V33DIO2	Digital Input / Output 3.3V supply
45	V33D	Digital core 3.3V supply
46	V33A	Analog 3.3V supply

Terminal Functions (continued)

TERMINAL NUMBER	TERMINAL LABEL	TERMINAL DESCRIPTION
47	BPCap	1.8V Bypass Capacitor -- tie 0.1µF cap to analog ground
48	Agnd2	Analog ground
49	Agnd1	Analog ground
50	EAp1	Error analog, differential voltage, Positive channel 1 input
51	EAn1	Error analog, differential voltage, Negative channel 1 input
52	EAp2	Error analog, differential voltage, Positive channel 2 input
53	EAn2	Error analog, differential voltage, Negative channel 2 input
54	EAp3	Error analog, differential voltage, Positive channel 3 input
55	EAn3	Error analog, differential voltage, Negative channel 3 input
56	EAp4	Error analog, differential voltage, Positive channel 4 input
57	EAn4	Error analog, differential voltage, Negative channel 4 input
58	V33FB	Connection to the base of 3.3V linear regulator transistor (no connect if unused)
59	CS1A	Power stage 1A current sense input and input to analog comparator 1
60	Addr1	PMBus Address sense. Channel 1.
61	Addr0	PMBus Address sense. Channel 0.
62	Temp3/AuxADC3	Temperature sense input for Rail 3, or Auxiliary ADC input 3
63	Temp4/AuxADC4	Temperature sense input for Rail 4, or Auxiliary ADC input 4
64	Agnd3	Analog ground
	PowerPad	It is recommended that this pad be connected to analog ground

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Voltage applied at V_{33D} to DGND	–0.3 to 3.8	V
Voltage applied at V_{33A} to AGND	–0.3 to 3.8	V
Voltage applied to any terminal(2)	–0.3 to 3.8	V
Maximum junction temperature (T_J)	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to GND.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	-55	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V	Supply voltage during operation, V_{33D}, V_{33DIO}, V_{33A}	3	3.3	3.6	V
T_J	Operating junction temperature range	–55		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCD9244-EP QFN 64 TERMINAL	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	24.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	10	
θ_{JB}	Junction-to-board thermal resistance(4)	4.2	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	4.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current	V_{33A} = 3.3 V		8	15	mA
I_{V33DIO}		V_{33DIO} = 3.3 V		42	55	mA
I_{V33}		Total V_{33} supply current, V_{33A} = V_{33DIO} = 3.3 V		54	80	mA
I_{V33DIO}		V_{33D} = 3.3 V storing configuration parameters in flash memory		52	65	mA
INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS						
V_{33}	3.3-V linear regulator	Emitter of NPN transistor	3.25	3.3	3.6	V
V_{33FB}	3.3-V linear regulator feedback			4	4.6	V
I_{V33FB}	Series pass base drive	V_{IN} = 12 V	0.2	0.4	8	mA
Beta	Series NPN pass device		40			
EXTERNALLY SUPPLIED 3.3 V POWER						
V_{33D}, V_{33DIO1}, V_{33DIO2}	Digital 3.3-V power	T_J = 25°C	3.0		3.6	V
V33A	Analog 3.3-V power	T_J = 25°C	3.0		3.6	V
ERROR AMPLIFIER INPUTS EAPn, EANn						
V_{CM}	Common mode voltage each terminal		0		1.8	V
V_{ERROR}	Internal error Voltage range	AFE_GAIN field of CLA_GAINS = 1X(1)	–256		248	mV
EAP-EAN	Error voltage digital resolution	AFE_GAIN field of CLA_Gains = 8X		1		mV
R_{EA}	Input Impedance	Ground reference, T_J = 25°C		1.5		MΩ
I_{OFFSET}	Input offset current	1-kΩ source impedance,T_J = 25°C	–5		5	µA
Vref 10-bit DAC						
V_{ref}	Reference Voltage Setpoint		0		1.7	V
V_{refres}	Reference Voltage Resolution			1.56		mV
ANALOG INPUTS CS1A, CS2A, CS3A, CS4A,VinMon, Temp1, Temp2, Temp3, Temp4, Addr0, Addr1						
V_{ADC_RANGE}	Measurement range for voltage monitoring	Inputs: VinMon, Temp1, Temp2, Temp3, Temp4, CS1A, CS2A, CS3A, CS4A	0		2.6	V
Voffset	input offset voltage		–27		27	mV
V_{OC_THRS}	Over-current comparator threshold voltage range(2)	Inputs: CS1A, CS2A, CS3A, CS4A	0.032		2	V
V_{OC_RES}	Over-current comparator threshold voltage range	Inputs: CS, 1A, CS2A, CS3A, CS4A		31.25		mV
$Temp_{internal}$	Int. temperature sense accuracy	Over range from 0°C to 100°C	–15		15	°C
INL	ADC integral nonlinearity	T_J = -40°C to 125°C	–2.5		2.5	mV
I_{lkg}	Input leakage current	3V applied to terminal			100	nA
R_{IN}	Input impedance	Ground reference		8		MΩ
C_{IN}	Current Sense Input capacitance			10		pF

(1) See the UCD92xx PMBus Command Reference for the description of the AFE_GAIN field of CLA_GAINS command.
(2) Can be disabled by setting to '0'

7.6 Electrical Characteristics (Continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA(1), V_{33DIO} = 3 V			Dgnd +0.3	V
V_{OH}	High-level output voltage	I_{OH} = -6 mA(2), V_{33DIO} = 3 V	V_{33DIO} –0.6V			V
V_{IH}	High-level input voltage	V_{33DIO} = 3V	2.1		3.6	V
V_{IL}	Low-level input voltage	V_{33DIO} = 3.5 V			1.4	V
SYSTEM PERFORMANCE						
V_{RESET}	Voltage where device comes out of reset	V_{33D} terminal	2.3		2.4	V
t_{RESET}	Pulse width needed for reset	nRESET terminal	2			µs
V_{RefAcc}	Setpoint Reference Accuracy	Vref commanded to be 1V, at 25°C AFEgain = 4, 1V input to EAP/N measured at output of the EADC(3)	–10		10	mV
	Setpoint Reference Accuracy over temperature	–55°C to 125°C	–40		40	mV
$V_{DiffOffset}$	Differential offset between gain settings	AFEgain = 4 compared to AFEgain = 1, 2, or 8	–4		4	mV
t_{Delay}	Digital Compensator Delay		240		240 + 1 switching cycle	ns
F_{SW}	Switching Frequency		15.260		2000	kHz
	Accuracy		–5%		5%	
Duty	Max and Min Duty Cycle		0%		100%	
V_{33}Slew	Minimum V_{33} slew rate	V33 slew rate between 2.3V and 2.9V, T_J = -40°C to 125°C	0.25			V/ms
$t_{retention}$	Retention of configuration parameters(4)	T_J = 25 °C	100			Years
Write_Cycles	Number of nonvolatile erase/write cycles	T_J = 25 °C	20			K cycles
$Rate_{VID}$	Max VID message rate	All rails configured to accept VID messages(5)			1	msg/msec
		All rails configured to accept 6-bit VID messages(5)			4	
		All rails configured to accept 8-bit VID messages(6)			4	

(1) The maximum I_{OL}, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(2) The maximum I_{OH}, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.
(3) With default device calibration. PMBus calibration can be used to improve the regulation tolerance.
(4) The data retention specification is based on accelerated stress testing at 170°C for 420 hours and using an Arrhenius model with activation energy of 0.6 eV.
(5) VID message rate on each interface. Measured over a 1.0 msec interval.
(6) VID message rate on PMBus interface.

7.7 ADC Monitoring Intervals And Response Times

The ADC operates in a continuous conversion sequence that measures each rail's output voltage and output current, plus six other variables (input voltage, internal temperature, and four external temperature sensors). The length of the sequence is determined by the number of output rails (NumRails) configured for use. The time to complete the monitoring sampling sequence is give by the formula: $t_{ADC\_SEQ} = t_{ADC} \times (2 \times NumRAILS + 6)$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ADC}	ADC single-sample time			3.84		µs
t_{ADC_SEQ}	ADC sequencer interval	Min = 2 × 1 Rail + 6 = 8 samples Max = 2 × 4 Rails + 6 = 14 samples	30.72		53.76	µs

The most recent ADC conversion results are periodically converted into the proper measurement units (volts, amperes, degrees), and each measurement is compared to its corresponding fault and warning limits. The monitoring operates asynchronously to the ADC, at intervals shown in the table below.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Vout}	Output voltage monitoring interval			200		µs
t_{Iout}	Output current monitoring interval			200×NRails		µs
t_{Vin}	Input voltage monitoring interval			1		ms
t_{TEMP}	Temperature monitoring interval			100		ms
t_{AUXADC}	Auxiliary ADC monitoring interval			100		ms

Because the ADC sequencer and the monitoring comparisons are asynchronous to each other, the response time to a fault condition depends on where the event occurs within the monitoring interval and within the ADC sequence interval. Once a fault condition is detected, some additional time is required to determine the correct action based on the FAULT_RESPONSE code, and then to perform the appropriate response. The following table lists the worse-case fault response times.

PARAMETER		TEST CONDITIONS	TYP	MAX no VID	MAX /w VID(1)	UNIT
t_{OVF}, t_{UVF}	Over-/under-voltage fault response time during normal operation	Normal regulation, no PMBus activity, 4 stages enabled		250	800	µs
t_{OVF}, t_{UVF}	Over-/under-voltage fault response time, during data logging	During data logging to nonvolatile memory(2)		800	1000	µs
t_{OVF}, t_{UVF}	Over-/under-voltage fault response time, when tracking or sequencing enable	During tracking and soft-start ramp.		400		µs
t_{OCF}, t_{UCF}	Over-/under-current fault response time during normal operation	Normal regulation, no PMBus activity, 4 stages enabled 75% to 125% current step(3)		100 + (600 × NRails)	5000	µs
t_{OCF}, t_{UCF}	Over-/under-current fault response time, during data logging	During data logging to nonvolatile memory 75% to 125% current step		600 + (600 × NRails)	5000	µs
t_{OTF}	Over-temperature fault response time	Temperature rise of 10°C/sec, at OT threshold	1.60			sec
$t_{3\text{-}State}$	Time to tristate the PWM output after a shutdown is initiated	DRIVER_CONFIG = 0x01	5.5			µs

(1) Controller receiving VID commands at a rate of 4000 msg/sec.
(2) During a STORE_DEFAULT_ALL command, which stores the entire configuration to nonvolatile memory, the fault detection latency can be up to 10 ms.
(3) Because the current measurement is averaged with a smoothing filter, the response time to an over-current condition depends on a combination of the time constant (τ) from Table 6, the recent measurement history, and how much the measured value exceeds the over-current limit.

7.8 Hardware Fault Detection Latency

The controller contains hardware fault detection circuits that are independent of the ADC monitoring sequencer.

PARAMETER		TEST CONDITIONS	MAX TIME	UNIT
t_{FAULT}	Time to disable DPWM output base on active FAULT terminal signal	High level on FAULT terminal	18	µs
t_{CLF}	Time to disable the DPWM A output based on internal analog comparator	Step change in CS voltage from 0V to 2.5V	4	Switch Cycles

7.9 PMBus/SMBus/I²C

The timing characteristics and timing diagram for the communications interface that supports I2C, SMBus and PMBus are shown below.

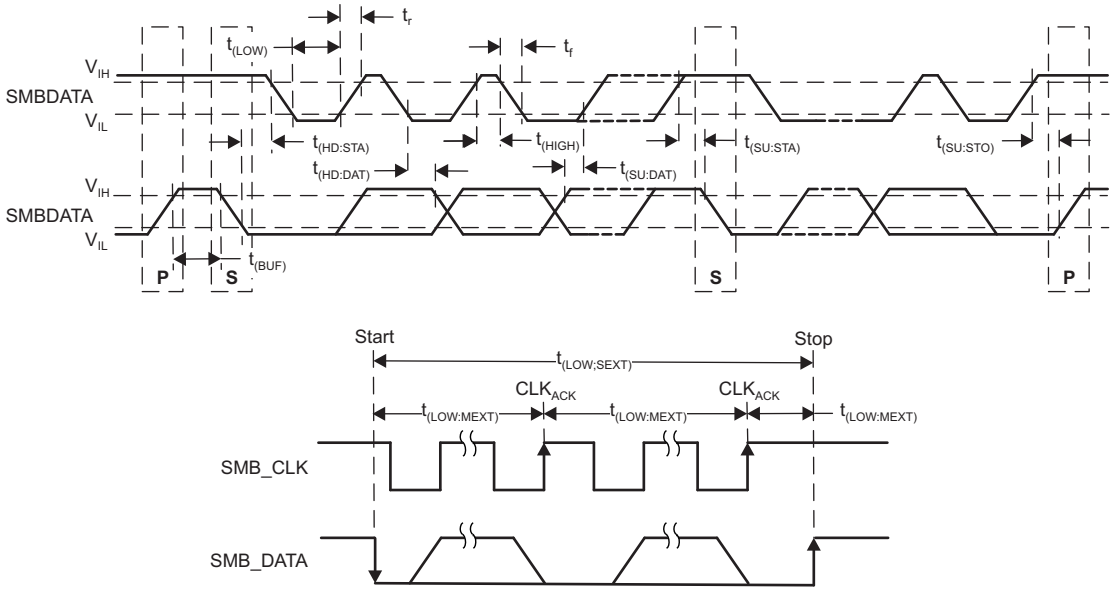


Figure 1. I²C/SMBus/PMBus Timing In Extended Mode Diagram

7.10 I²C/SMBus/PMBus Timing Requirements

T_J = –55°C to 125°C, 3V < V_{33} < 3.6V, typical values at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus/PMBus operating frequency	Slave mode; SMBC 50% duty cycle	10		1000	kHz
f_{I2C}	I C operating frequency	Slave mode; SCL 50% duty cycle	10		1000	kHz
$t_{(BUF)}$	Bus free time between start and stop		5			µs
$t_{(HD:STA)}$	Hold time after (repeated) start		0.3			µs
$t_{(SU:STA)}$	Repeated start setup time		0.3			µs
$t_{(SU:STO)}$	Stop setup time		0.3			µs
$t_{(HD:DAT)}$	Data hold time	Receive mode	0			ns
$t_{(SU:DAT)}$	Data setup time		55			ns
$t_{(TIMEOUT)}$	Error signal/detect	See (1)			35	ms
$t_{(LOW)}$	Clock low period		0.55			µs
$t_{(HIGH)}$	Clock high period	See (2)	0.3		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
t_{FALL}	Clock/data fall time	Rise time t_{RISE} = V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15), T_J = -40°C to 125°C			1000	ns
t_{RISE}	Clock/data rise time	Fall time t_{FALL} = 0.9 V_{33} to (V_{ILMAX} – 0.15), T_J = -40°C to 125°C			1000	ns

(1) The UCD9244 times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving UCD9244 that is in progress.
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

7.11 Typical Characteristics

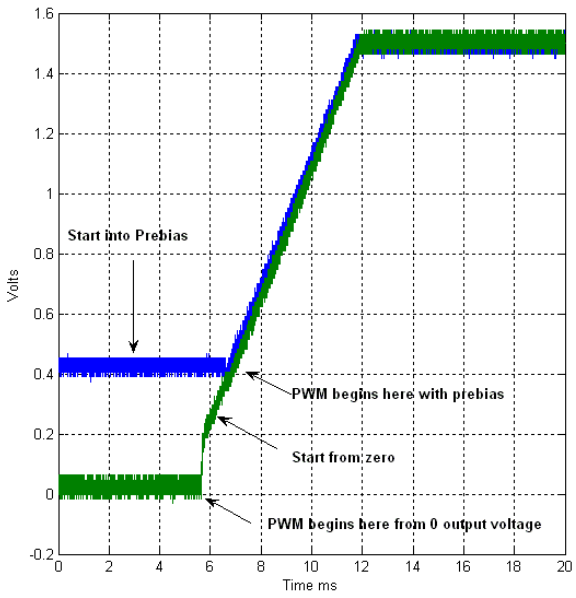


Figure 2. Soft-Start Ramp

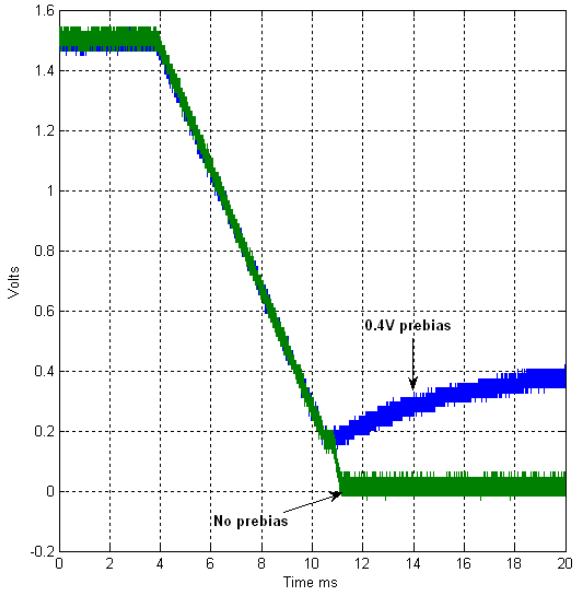


Figure 3. Soft-Stop Ramp

8 Detailed Description

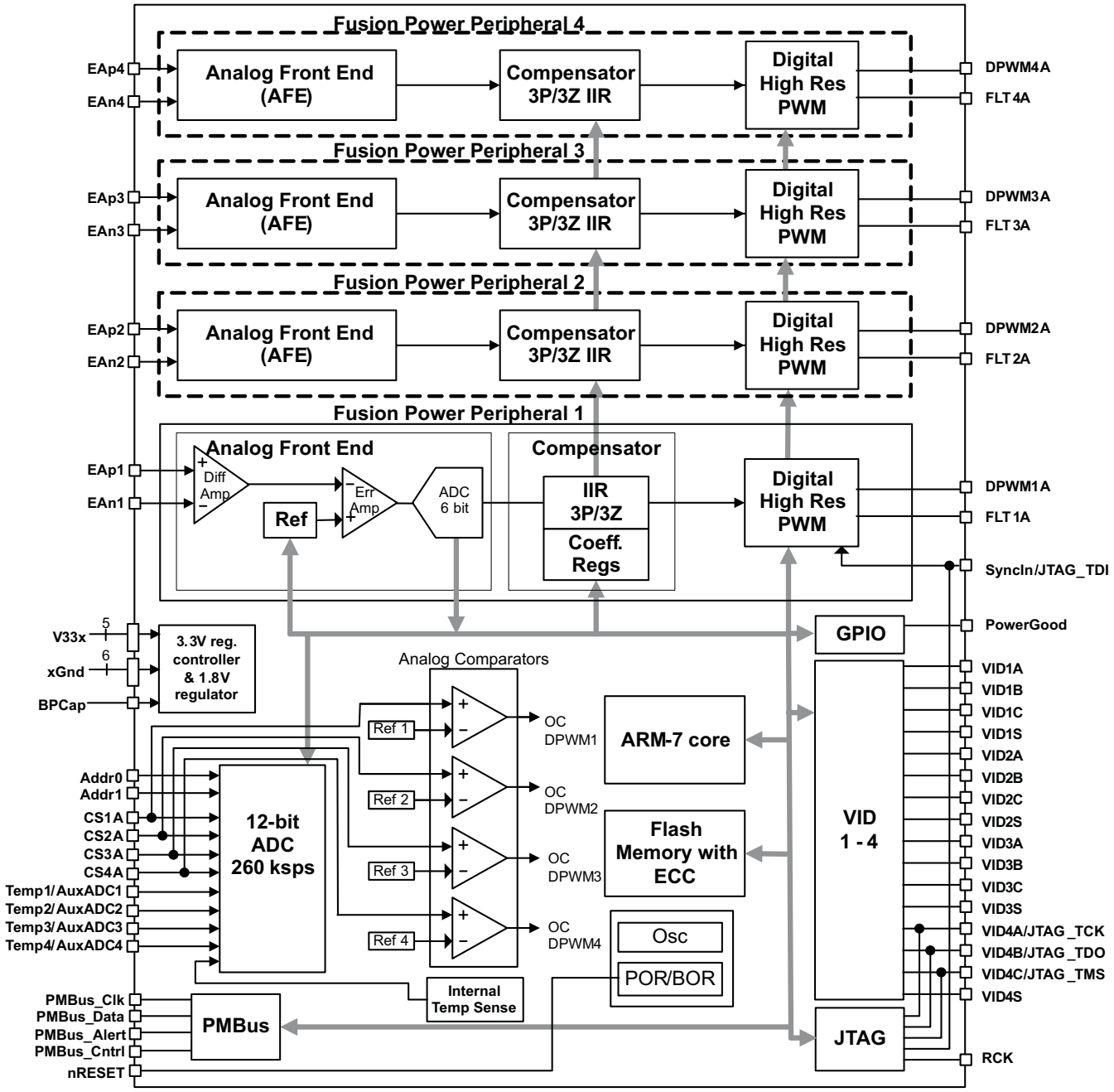
8.1 Overview

The UCD9244 contains four Fusion Power Peripherals (FPP). Each FPP consists of:

- A differential input error voltage amplifier.
- A 10-bit DAC used to set the output regulation reference voltage.
- A fast ADC with programmable input gain to digitally measure the error voltage.
- A dedicated 3-pole/3-zero digital filter to compensate the error voltage
- A digital PWM (DPWM) engine that generates the PWM pulse width based on the compensator output.

Each controller is configurable through the PMBus serial interface.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PMBus Interface

The PMBus is a serial interface specifically designed to support power management. It is based on the SMBus interface that is built on the I^2C physical specification. The UCD9244 supports revision 1.2 of the PMBus standard. Wherever possible, standard PMBus commands are used to support the function of the device. For unique features of the UCD9244, MFR_SPECIFIC commands are defined to configure or activate those features. These commands are defined in the *UCD92xx PMBUS Command Reference*.

The UCD9244 is PMBus compliant, in accordance with the "Compliance" section of the PMBus specification. The firmware is also compliant with the SMBus 2.0 specification, including support for the SMBus ALERT function. The hardware can support 100 kHz, 400 kHz, or 1 MHz PMBus operation.

8.3.2 Resistor Programmed PMBus Address Decode

The PMBus Address is selected using resistors attached to the ADDR0 and ADDR1 terminals. At power-up, the device applies a bias current to each address detect terminal. The measured voltage on each terminal determines the PMBus address as defined in Table 1. For example, a 133kΩ resistor on ADDR1 and a 75kΩ on ADDR0 will select PMBus address = 100. Resistors are chosen from the standard EIA-E96 series, and should have accuracy of 1% or better.

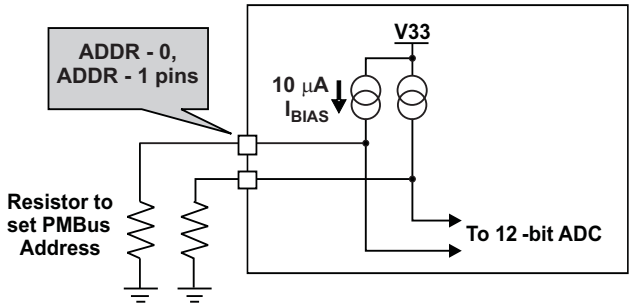


Figure 4. PMBus Address Detection Method

A short or open on either address terminal causes the PMBus address to default to address 126. To avoid potential conflicts between multiple devices, it is best to avoid using address 126.

Some addresses should be avoided; see Table 1 for details.

Feature Description (continued)

Table 1. PMBus Address Bins(1)

		ADDR0													
		(short) < 36.5k	42.2k	48.7k	56.2k	64.9k	75k	86.6k	100k	115k	133k	154k	178k	205k	(open) > 237k
ADDR1	< 36.5k (short)	126	126	126	126	126	126	126	126	126	126	126	126	126	126
	42.2k	126	126(2)	1	2	3	4	5	6	7	8	9	10	11(3)	126
	48.7k	126	126(2)	13	14	15	16	17	18	19	20	21	22	33	126
	56.2k	126	24	25	26	27	28	29	30	31	32	33	34	35	126
	64.9k	126	36	37	38	39	40	41	42	43	44	45	46	47	126
	75k	126	48	49	50	51	52	53	54	55	56	57	58	59	126
	86.6k	126	60	61	62	63	64	65	66	67	68	69	70	71	126
	100k	126	72	73	74	75	76	77	78	79	80	81	82	83	126
	115k	126	84	85	86	87	88	89	90	91	92	93	94	95	126
	133k	126	96	97	98	99	100	101	102	103	104	105	106	107	126
	154k	126	108	109	110	111	112	113	114	115	116	117	118	119	126
	178k	126	120	121	122	123	124	125	126	126(2)	126	126	126	126	126
	205k	126	126	126	126	126	126	126	126	126	126	126	126	126	126
	> 237k (open)	126	126	126	126	126	126	126	126	126	126	126	126	126	126

(1) Shaded addresses are not recommended as they will cause conflict when multiple devices are used.
(2) Reserved. Do not use.
(3) Conflicts with ROM. Do not use.

8.3.3 VID Interface

The UCD9244 supports VID (Voltage Identification) inputs from up to four external VID enabled devices. The VID codes may be 4-, 6-, or 8-bit values; the format is selected using the VID_CONFIG PMBus command. In 4- and 6-bit mode, each host uses four VID input signals (VID_A, VID_B, VID_C, and VID_S) to send VID codes to the UCD9244. In 8-bit mode, the PMBus input is used to receive VID commands from the VID devices' I^2C interfaces.

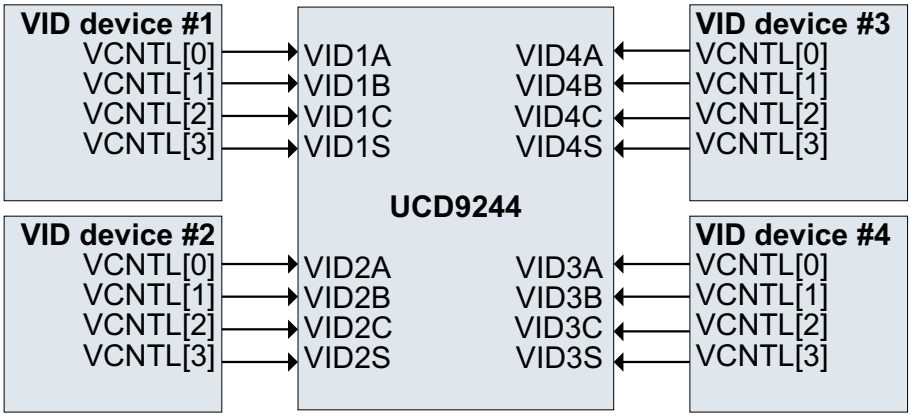


Figure 5. One UCD9244 Controlled By Four DSPS/ASICS Devices Using 4-Bit Or 6-Bit VID Format

Regardless of which VID mode is used, the commanded output voltage reference is set according to this formula:

$$Vref\_cmd = (VID\_CODE \times VID\_Slope) + VID\_Offset \quad (1)$$

where

$$VID\_Slope = (VID\_Vout\_High - VID\_Vout\_Low) / ((2\text{^}VID\_Format) - 1) \quad (2)$$

and

$$VID\_Offset = VID\_Vout\_Low \quad (3)$$

The VID_Vout_High, VID_Vout_Low, and VID_Format values are set using the VID_CONFIG PMBus command. The same command is used to set the initial VID code that will be used at power-up. In addition, the VID_CONFIG command also sets the initial voltage that the device ramps to at the end of the soft start; and defines a lockout interval over which the VID is ignored during the soft start.

VID Lockout Interval: Because the VID signals may be originating from a device that is being powered by the UCD9244, the voltage levels on the VID signal may not be valid logic levels until the supply voltage at the powered device has stabilized. For this reason a configurable lockout interval is applied each time the regulated output voltage is turned on. The lockout interval timer starts when the output voltage reaches the top of the soft-start ramp. Positive values range from 1 to 32767 ms, with 1 ms resolution. A value of 0 will enable the VID inputs immediately at the top of the start ramp. Negative values disable the lockout, allowing the VID inputs to remain active all the time regardless of the output voltage state. The default value is 0.

8.3.4 Jtag Interface

The JTAG interface can provide an alternate interface for programming the device. Four of the JTAG terminals on the UD9244 (TMS, TDI, TDO, and TCK) are shared with other functions (VID4A, VID4B, VID4C, and Syncln). JTAG is disabled by default. There are three conditions under which the JTAG interface is enabled:

1. When the ROM_MODE PMBus command is issued.
2. On power-up if the Data Flash is blank. This allows JTAG to be used for writing the configuration parameters to a programmed device with no PMBus interaction.
3. When an invalid address is detected at power-up. By opening or shorting one of the address terminals to ground, an invalid address can be generated that enables JTAG.

When the JTAG port is enabled the shared terminals are not available for use as Syncln or VID terminals.

If JTAG is to be used, an external mechanism such as jumpers or a mux must be used to prevent conflict between JTAG and the Syncln or VID terminals.

8.3.5 Bias Supply Generator (Shunt Regulator Controller)

The I/O and analog circuits in the UCD9244 require 3.3V to operate. This can be provided using a stand-alone external 3.3V supply, or it can be generated from the main input supply using an internal shunt regulator and an external transistor. Regardless of which method is used to generate the 3.3V supply, bypass capacitors of 0.1 µF and 4.7 µF should be connected from V33A and V33D to ground near the device. An additional bypass capacitor from 0.1 to 1 µF must be connected from the BPCap terminal to ground for the internal 1.8V supply to the device's logic circuits.

Figure 6 shows a typical application using the external transistor. The base of the transistor is driven by a resistor R1 to Vin and a transconductance amplifier whose output is on the V33FB terminal. The NPN emitter becomes the 3.3V supply for the chip.

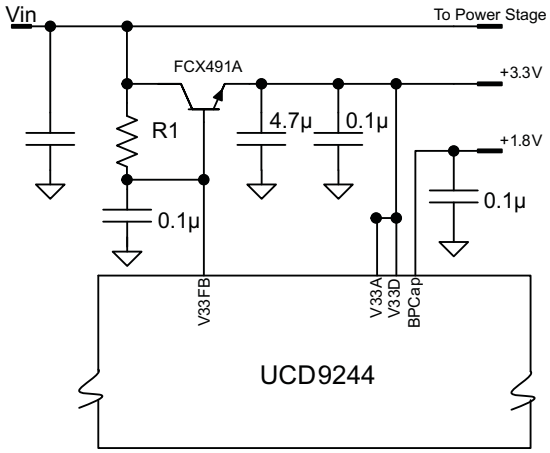


Figure 6. 3.3V Shunt Regulator Controller I/O

In order to generate the correct voltage on the base of the external pass transistor, the internal transconductance amplifier sinks current into the V33FB terminal and a voltage is produced across R1. This resistor value should be chosen so that ISINK is in the range from 0.2 to 0.4mA. R1 is defined as

$$R_1 = \frac{V_{in} - 3.3 - V_{be}}{\frac{I_E}{(\beta + 1)} + I_{SINK}} \quad (4)$$

Where I_{SINK} is the current into the V33FB terminal; V_{in} is the power supply input voltage, typically 12V; I_E is the current draw of the device and any pull up resistors tied to the 3.3V supply; and β is the beta of the pass transistor. For I_{SINK} = 0.3 mA, V_{in}=12V, β=99, V_{be} = 0.7V and I_E=50mA, this formula selects R1 = 10kΩ. Weaker transistors or larger current loads will require less resistance to maintain the desired I_{SINK} current. For example, lowering β to 40 would require R1 = 5.23 kΩ; likewise, an input voltage of 5V requires a value of 1.24 kΩ for R1.

8.3.6 Power-On Reset

The UCD9244 has an integrated power-on reset (POR) circuit that monitors the supply voltage. At power-up, the POR circuit detects the V33D rise. When V33D is greater than V_{RESET}, the device initiates an internal startup sequence. At the end of the startup sequence, the device begins normal operation, as defined by the downloaded device PMBus configuration.

8.3.7 External Reset

The device can be forced into the reset state by an external circuit connected to the nRESET terminal. A logic low voltage on this terminal holds the device in reset. To avoid an erroneous trigger caused by noise, a 10kΩ pull up resistor to 3.3V is recommended.

8.3.8 ON_OFF_CONFIG

The ON_OFF_CONFIG command is used to select the method of turning rails on and off. It can be configured so that the rail:

- stays off,
- turns on automatically,
- responds to the PMBus_Cntrl terminal,
- responds to OPERATION command, or
- responds to logical-AND of the PMBus_Cntrl terminal and the OPERATION command.

The ON_OFF_CONFIG command also sets the active polarity of the PMBus_Cntrl terminal.

8.3.9 Output Voltage Adjustment

The output voltage may be set to maintain a steady voltage or it may be controlled dynamically by the VID interface, depending on the VID_CONFIG setting. When not being commanded by the VID interface, the nominal output voltage is programmed by a combination of PMBus settings: VOUT_COMMAND, VOUT_CAL_OFFSET, VOUT_SCALE_LOOP, and VOUT_MAX. Their relationship is shown in Figure 7. These PMBus parameters need to be set such that the resulting Vref DAC value does not exceed the maximum value of V_{ref}.

Output voltage margining is configured by the VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW commands. The OPERATION command selects between the nominal output voltage and either of the margin voltages. The OPERATION command also includes an option to suppress certain voltage faults and warnings while operating at the margin settings.

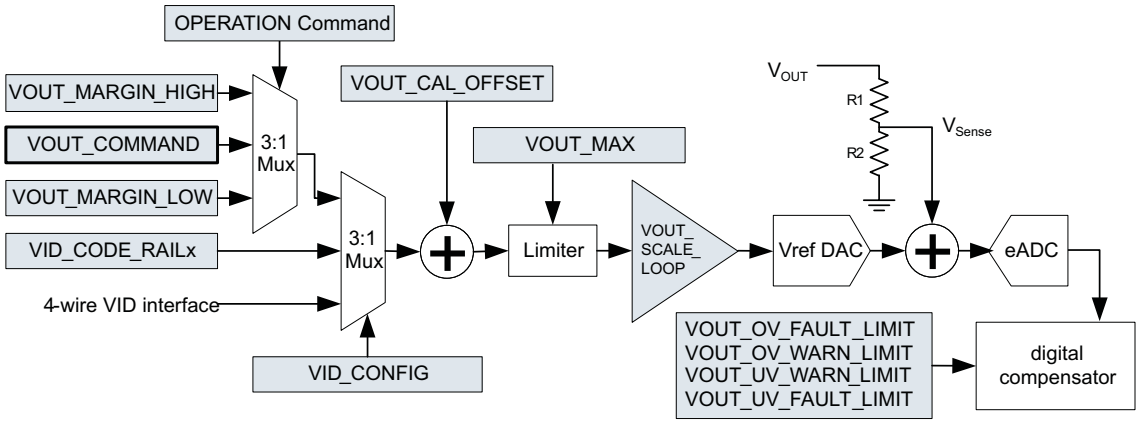


Figure 7. PMBus Voltage Adjustment Mechanisms

For a complete description of the commands supported by the UCD9244 see the UCD92xx PMBUS Command Reference (SLUU337). Each of these commands can also be issued from the Texas Instruments Fusion Digital Power™ Designer program. This Graphical User Interface (GUI) PC program issues the appropriate commands to configure the UCD9244 device.

8.3.10 Calibration

To optimize the operation of the UCD9244, PMBus commands are supplied to enable fine calibration of output voltage, output current, and temperature measurements. The supported commands and related calibration formulas may be found in the UCD92xx PMBUS Command Reference (SLUU337).

8.3.11 Analog Front End (AFE)

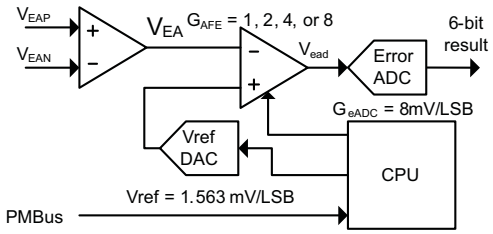


Figure 8. Analog Front End Block Diagram

The UCD9244 senses the power supply output voltage differentially through the EAP and EAN terminals. The error amplifier utilizes a switched capacitor topology that provides a wide common mode range for the output voltage sense signals. The fully differential nature of the error amplifier also ensures low offset performance.

The output voltage is sampled at a programmable time (set by the EADC_SAMPLE_TRIGGER PMBus command). When the differential input voltage is sampled, the voltage is captured in internal capacitors and then transferred to the error amplifier where the value is subtracted from the set-point reference which is generated by the 10-bit Vref DAC as shown in Figure 8. The resulting error voltage is then amplified by a programmable gain circuit before the error voltage is converted to a digital value by the error ADC (EADC). This programmable gain is configured through the PMBus and affects the dynamic range and resolution of the sensed error voltage as shown in Table 2. The internal reference gains and offsets are factory-trimmed at the 4x gain setting, so it is recommended that this setting be used whenever possible.

Table 2. Analog Front End Resolution

AFE_GAIN for PMBus Command	AFE Gain	EFFECTIVE ADC RESOLUTION (mV)	DIGITAL ERROR VOLTAGE DYNAMIC RANGE (mV)
0	1x	8	–256 to 248
1	2x	4	–128 to 124
2 (Recommended)	4x	2	–64 to 62
3	8x	1	–32 to 31

The AFE variable gain is one of the compensation coefficients that are stored when the device is configured by issuing the CLA_GAINS PMBus command. Compensator coefficients are arranged in several banks: one bank for start/stop ramp or tracking, one bank for normal regulation mode and one bank for light load mode. This allows the user to trade-off resolution and dynamic range for each operational mode.

The EADC, which samples the error voltage, has high accuracy, high resolution, and a fast conversion time. However, its range is limited as shown in Table 2. If the output voltage is different from the reference by more than this, the EADC reports a saturated value at –32 LSBs or 31 LSBs. The UCD9244 overcomes this limitation by adjusting the Vref DAC up or down in order to bring the error voltage out of saturation. In this way, the effective range of the ADC is extended. When the EADC saturates, the Vref DAC is slewed at a rate of 0.156 V/ms, referred to the EA differential inputs.

The differential feedback error voltage is defined as $V_{EA} = V_{EAP} – V_{EAN}$. An attenuator network using resistors R1 and R2 (Figure 9) should be used to ensure that V_{EA} does not exceed the maximum value of Vref when operating at the commanded voltage level. The commanded voltage level is determined by the PMBus settings described in the *Output Voltage Adjustment* section.

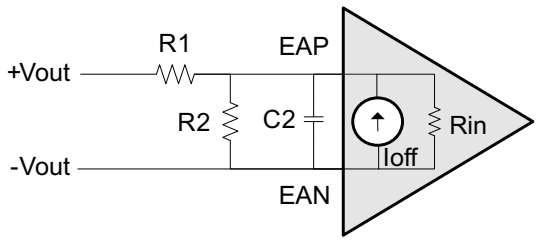


Figure 9. Input Offset Equivalent Circuit

8.3.12 Voltage Sense Filtering

Conditioning should be provided on the EAP and EAN signals. Figure 9 shows a divider network between the output voltage and the voltage sense input to the controller. The resistor divider is used to bring the output voltage within the dynamic range of the controller. When no attenuation is needed, R2 can be left open and the signal conditioned by the low-pass filter formed by R1 and C2.

As with any power supply system, maximize the accuracy of the output voltage by sensing the voltage directly across an output capacitor as close to the load as possible. Route the positive and negative differential sense signals as a balanced pair of traces or as a twisted pair cable back to the controller. Put the divider network close to the controller. This ensures that there is low impedance driving the differential voltage sense signal from the voltage rail output back to the controller. The resistance of the divider network is a trade-off between power loss and minimizing interference susceptibility. A parallel resistance (R_p) of 1kΩ to 4kΩ is a good compromise. Once RP is chosen, R1 and R2 can be determined from the following formulas.

$$R_1 = \frac{R_P}{K}$$

$$R_2 = \frac{R_P}{1-K}$$

$$\text{where } K = \frac{V_{EA}}{V_{OUT}} \cong \text{VOUT\_SCALE\_LOOP} \tag{5}$$

It is recommended that a capacitor be placed across the lower resistor of the divider network. This acts as an additional pole in the compensation and as an anti-alias filter for the EADC. To be effective as an anti-alias filter, the corner frequency should be 35% to 40% of the switching frequency. Then the capacitor is calculated as:

$$C2 = \frac{1}{2\pi \times 0.35 \times F_{SW} \times R_P} \tag{6}$$

To obtain the best possible accuracy, the input resistance and offset current on the device should be considered when calculating the gain of a voltage divider between the output voltage and the EA sense inputs of the UCD9244. The input resistance and input offset current are specified in the parametric tables in this datasheet. $V_{EA} = V_{EAP} - V_{EAN}$ in the equation below.

$$V_{EA} = \frac{R_2}{R_1 + R_2 + \left(\frac{R_1 R_2}{R_{EA}}\right)} V_{OUT} + \frac{R_1 R_2}{R_1 + R_2 + \left(\frac{R_1 R_2}{R_{EA}}\right)} I_{OFFSET} \tag{7}$$

The effect of the offset current can be reduced by making the resistance of the divider network low.

8.3.13 DPWM Engine

The output of the compensator feeds the high resolution DPWM engine. The DPWM engine produces the pulse width modulated gate drive output from the device. In operation, the compensator calculates the necessary duty cycle as a digital number representing a percentage from 0 to 100%. The duty cycle value is multiplied by the configured period to generate a comparator threshold value. This threshold is compared against the high speed switching period counter to generate the desired DPWM pulse width. This is shown in Figure 10.

Each DPWM engine can be synchronized to another DPWM engine or to an external sync signal via the SyncIn and SyncOut terminals. Configuration of the synchronization function is done through a MFR_SPECIFIC PMBus command. See the *DPWM Synchronization* section for more details.

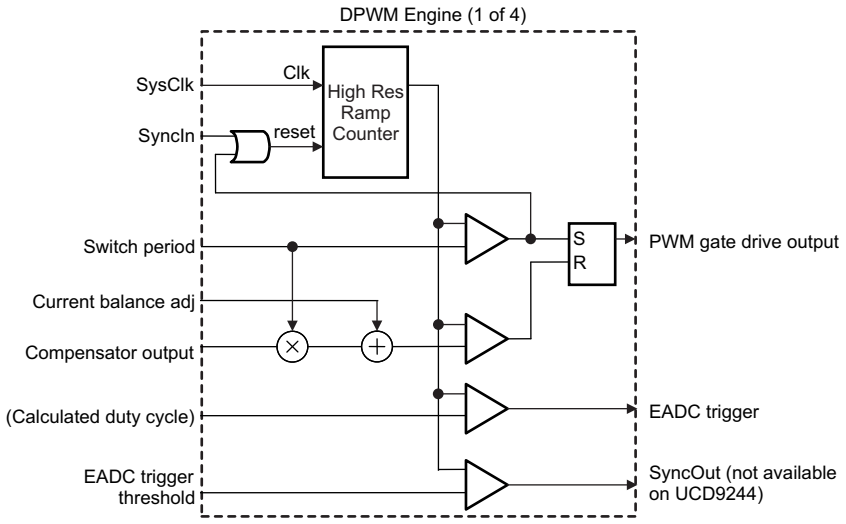


Figure 10. DPWM Engine

8.3.14 Rail/Power Stage Configuration

Unlike many other products in the UCD92xx family, the UCD9244 does not support assigning power stages to arbitrary rails, or combining multiple power stages on the same rail. The UCD9244 supports up to two single-phase rails, and the channel number of each rail's DPWM output must match that of its EAP/EAN feedback inputs.

8.3.15 DPWM Phase Synchronization

DPWM synchronization provides a method to link the timing between voltage rails controlled by the UCD92xx device--either internally or between devices. The configuration of the synchronization between rails is performed by the issuing the SYNC_CONFIG command. For details of issuing this command, see the UCD92xx PMBUS Command Reference (SLUU337). The synchronization behavior can also be configured using the Fusion Digital Power Designer software. Below is a summary of the function.

Each digital pulse width modulator (PWM) engine in the UCD92xx controller can accept a sync signal that resets the PWM ramp generator. The ramp generator can be set to free-run, accept a reset signal from another internal PWM engine, or accept a reset signal from the external SyncIn terminal. In this way the PWM timers can be "daisy-chained" to set up the desired phase relationship between power stages.

The PWM engine reset input can accept the following inputs

Table 3. Sync Trigger Inputs

SYNC SIGNAL
None (free run)
DPWM 1
DPWM 2
DPWM 3
DPWM 4
SyncIn terminal

Table 4. Available Source For SyncOut

SYNC SIGNAL
Disabled
DPWM 1
DPWM 2
DPWM 3
DPWM 4

When configuring a PWM engine to run synchronous to another internal PWM output, set the switching frequency of each PWM output to the same value using the FREQUENCY_SWITCH PMBus command. Set the time point where the controller samples the voltage to be regulated by setting the EADC_SAMPLE_TRIGGER value to the minimum value (228-240 nsec before the end of the switching period).

When configuring a PWM engine to run synchronous to an external sync signal, the switching period must be set to be longer than the period of the sync signal by setting the value of the FREQUENCY_SWITCH command to be lower than the frequency of the sync signal. This way the external sync signal will reset the PWM ramp counter before it is internally reset. In this operating condition, the error ADC sample trigger time must be set to:

$$\text{EADC\_SAMPLE\_TRIGGER} \geq \frac{1}{F_{SW}} - \frac{0.95}{F_{sync}} + 248\text{ns} \tag{8}$$

where F_{sw} is the switching frequency set by FREQUENCY_SWITCH and F_{sync} is the minimum synchronization frequency. The factor of 0.95 is due to the 5% tolerance on the internal clock in the controller. This will ensure that the regulation voltage is sampled "just in time" to calculate the appropriate control effort for each switching period. This is shown in Figure 11.

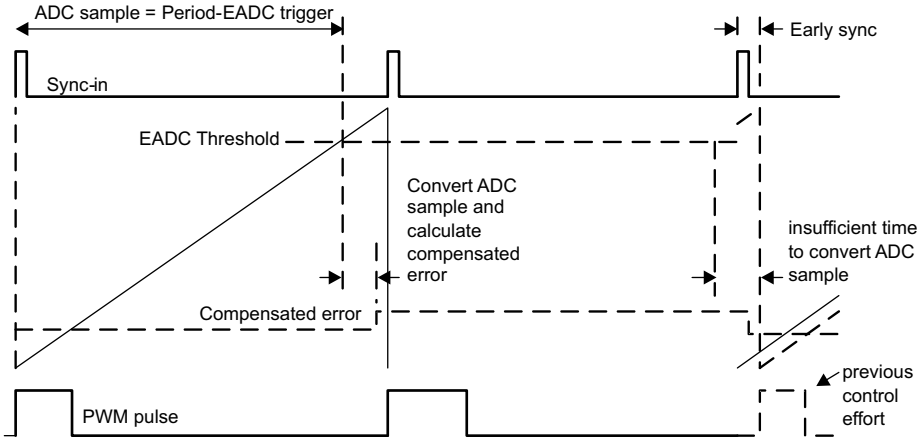


Figure 11. Relationship Of EADC Trigger To External Sync

If two rails share a common sync source other than the SyncIn terminal, they **must** have the same delay. When the SyncIn terminal is used as a sync source, the delay is applied using a different register (EV1) than when using the other sources (which use the PhaseTrig registers). Using the EV1 register introduces delay in the control loop calculation that will introduce phase loss that must be taken into consideration when calculating the loop compensation. Therefore, under most conditions it will be desirable to set the delay to zero for the PWM signal synchronized by the SyncIn terminal.

8.3.16 Output Current Measurement

Terminals CS1A, CS2A, CS3A, and CS4A are used to measure either output current or inductor current in each of the controlled power stages. PMBus commands IOUT_CAL_GAIN and IOUT_CAL_OFFSET are used to calibrate each measurement. See the *UCD92xx PMBus Command Reference* (SLUU337) for specifics on configuring this voltage to current conversion.

When the measured current is outside the range of either the over-current or under-current fault threshold, a current limit fault is declared and the UCD9244 performs the PMBus configured fault recovery. ADC current measurements are digitally averaged before they are compared against the over-current and under-current warning and fault thresholds. The output current is measured at a rate of one output rail per t_{Iout} microseconds. The current measurements are then passed through a digital smoothing filter to reduce noise on the signal and prevent false errors. The output of the smoothing filter asymptotically approaches the input value with a time constant that is approximately 3.5 times the sampling interval.

Table 5. Output Current Filter Time Constants

NUMBER OF OUTPUT RAILS	OUTPUT CURRENT SAMPLING INTERVALS (µs)	FILTER TIME CONSTANT τ (ms)
1	200	0.7
2	400	1.4
3	600	2.1
4	800	2.8

This smoothed current measurement is used for output current fault detection; see the Over-Current Detection section. The smoothed current measurement is also reported in response to a PMBus request for a current reading.

8.3.17 Current Sense Input Filtering

Each power stage current is monitored by the device at the CS terminals. The device monitors the current with a 12-bit ADC and also monitors the current with a digitally programmable analog comparator. The comparator can be disabled by writing a zero to the FAST_OC_FAULT_LIMIT.

Because the current sense signal is both digitally sampled and compared to the programmable over-current threshold, it should be conditioned with an RC network acting as an anti-alias filter. If the comparator is disabled, the CS input should be filtered at 35% of the sampling rate. An RC network with this characteristic can be calculated as

$$R = 0.45 \frac{N_{rails} T_{Iout}}{C} \tag{9}$$

where N_{rails} is the number of rails configured and T_{Iout} is the sample period for the current sense inputs. Therefore, when the comparator is not used, the recommended component values for the RC network are C = 10 nF and R = 35.7 kΩ.

When the fast over-current comparator is used, the filter corner frequency based on the ADC sample rate may be too slow and a corner frequency that is a compromise between the requirements of fast over-current detection and attenuating aliased content in the sampled current must be sought. In this case, the filter corner frequency can be calculated based on the time to cross the over-current threshold.

$$V_{OC\_thres} = V_{CS\_nom} + \Delta V_{Imon}(1 - e^{-t/\tau}) \tag{10}$$

where V_{OC_thres} is the programmed OC comparator threshold, V_{CS_nom} is the nominal CS voltage, ΔV_{Imon} is the change in CS voltage due to an over-current fault and τ is the filter time constant. Using the equation for the comparator voltage above, the RC network values can be calculated as

$$R = \frac{T_{det}}{C} \times \frac{1}{\ln(\Delta V_{Imon}) - \ln(\Delta V_{Imon} - V_{OC\_thres} + V_{CS\_nom})} \tag{11}$$

where T_{det} is the time to cross the over-current comparator threshold. For T_{det} = 10 µs, ΔV_{Imon} = 1.5V, V_{OC_thres} = 2.0V and V_{CS_nom} = 1.5V, the corner frequency is 6.4 kHz and the recommended RC network component values are C = 10 nF and R = 2.49 kΩ.

8.3.18 Over-Current Detection

Several mechanisms are provided to sense output current fault conditions. This allows for the design of power systems with multiple layers of protection.

1. Integrated gate drivers such as the UCD72xx family can be used to generate the FLT signal. The driver monitors the voltage drop across the high side FET and if it exceeds a resistor/voltage programmed threshold, the driver activates its fault output. A logic high signal on the FLT input causes a hardware interrupt to the internal CPU, which then disables the DPWM output. This process takes about 14 microseconds.
2. Inputs CS1A, CS2A, CS3A, and CS4A each drive an internal analog comparator. These comparators can be used to detect the voltage output of a current sense circuit. Each comparator has a separate threshold that can be set by the FAST_OC_FAULT_LIMIT PMBus command. Though the command is specified in amperes, the hardware threshold is programmed with a value between 31mV and 2V in 64 steps. The relationship between amperes to sensed volts is configured by the IOUT_CAL_GAIN command. When the current sense voltage exceeds the threshold, the corresponding DPWM output is driven low on the voltage rail with the fault.
3. Each Current Sense input to the UCD9244 is also monitored by the 12-bit ADC. Each measured value is scaled using the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands and then passed through a digital smoothing filter. The smoothed current measurements are compared to fault and warning limits set by the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT commands. The action taken when an OC fault is detected is defined by the IOUT_OC_FAULT_RESPONSE command.

Because the current measurement is averaged with a smoothing filter, the response time to an over-current condition depends on a combination of the time constant (τ) from Table 5, the recent measurement history, and how much the measured value exceeds the over-current limit. When the current steps from a current (I_1) that is less than the limit to a higher current (I_2) that is greater than the limit, the output of the smoothing filter is

$$I_{smoothed}(t) = I_1 + (I_2 - I_1)(1 - e^{-t/\tau}) \tag{12}$$

At the point when $I_{smoothed}$ exceeds the limit, the smoothing filter lags time, t_{lag} is

$$t_{lag} = \tau \ln\left(\frac{I_2 - I_1}{I_2 - I_{limit}}\right) \quad (13)$$

The worst case response time to an over-current condition is the sum of the sampling interval (Table 5) and the smoothing filter lag, t_{lag} from Equation 13.

8.3.19 Input Voltage Monitoring

The VinMon terminal on the UCD9244 monitors the input voltage. The VinMon terminal is monitored using the internal 12-bit ADC which has a dynamic range of 0 to 2.5V. The fault thresholds for the input voltage are set using the VIN_OV_FAULT_LIMIT and VIN_UV_FAULT_LIMIT commands. The scaling for Vin is set using the VIN_SCALE_MONITOR command.

8.3.20 Input UV Lockout

The input supply lock-out voltage thresholds are configured with the VIN_ON and VIN_OFF commands. When input supply voltage drops below the value set by VIN_OFF, the device starts a normal soft stop ramp. When the input supply voltage drops below the voltage set by VIN_UV_FAULT_LIMIT, the device performs as configured by the VIN_UV_FAULT_RESPONSE command. For example, when the bias supply for the controller is derived from another source, the response code can be set to "Continue" or "Continue with delay," and the controller attempts to finish the soft stop ramp. If the bias voltages for the controller and gate driver are uncertain below some voltage, the user can set the UV fault limit to that voltage and specify the response code to be "shut down immediately," disabling all DPWM outputs. VIN_OFF sets the voltage at which the output voltage soft-stop ramp is initiated, and VIN_UV_FAULT_LIMIT sets the voltage where power conversion is stopped.

8.3.21 Temperature Monitoring

The UCD9244 monitors temperature using the 12-bit ADC. The ADC12 is read every 100us and combined into a running sum. At the end of each 100ms monitoring interval, the ~1000 sample in the running sum are averaged together and the running sum is restarted. These averaged values are used to calculate the temperature from external temperature sensors. These same values may be read directly using the READ_AUX_ADCS PMBus command.

The averaged values are passed through an additional digital smoothing filter to further reduce the chance of reporting false over-temperature events. The smoothing filter has a time constant of 1.55 seconds.

8.3.22 Auxiliary ADC Input Monitoring

Unused external temperature sensor inputs may be used for general-purpose analog monitoring. The READ_AUX_ADCS PMBus command returns a block of four 16-bit values, each of which is the average of multiple raw measurements from the Temp/AuxADC inputs. A value of 0 corresponds to 0.00V and a value of 65535 corresponds to 2.50V. Unlike many other variables that can be monitored via PMBus, no mechanism is provided for adjusting the gain or offset of the Aux ADC measurements.

When using the temperature sensor inputs as Auxiliary ADCs, the temperature warning and faults should be disabled to prevent shut-downs due to non-existent over-temperature conditions.

8.3.23 Soft Start, Soft Stop Ramp Sequence

The UCD9244 performs soft start and soft stop ramps under closed-loop control.

Performing a start or stop ramp or tracking is considered a separate operational mode. The other operational modes are normal regulation and light load regulation. Each operational mode can be configured to have an independent loop gain and compensation. Each set of loop gain coefficients is called a "bank" and is configured using the CLA_GAINS PMBus command.

Start ramps are performed by waiting for the configured start delay TON_DELAY and then ramping the internal reference toward the commanded reference voltage at the rate specified by the TON_RISE time and VOUT_COMMAND. The DPWM outputs are enabled when the internal ramp reference equals the preexisting voltage (pre-bias) on the output and the calculated DPWM pulse width exceeds the pulse width specified by DRIVER_MIN_PULSE. This ensures that a constant ramp rate is maintained, and that the ramp is completed at the same time it would be if there had not been a pre-bias condition.

Figure 12 and Figure 13 show the operation of soft-start and soft-stop ramps.

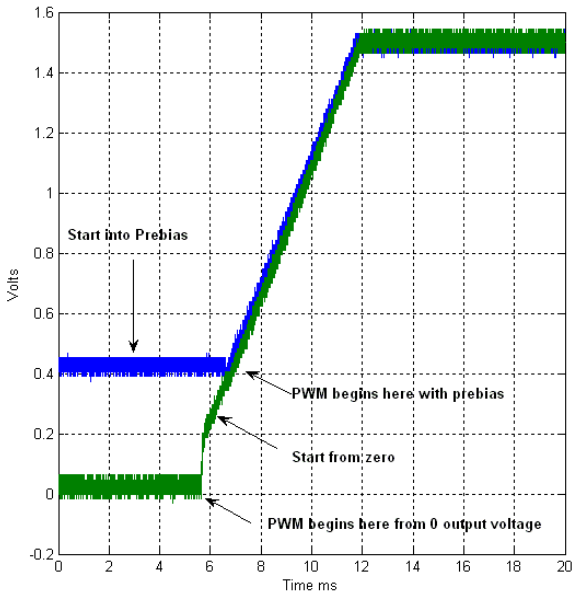


Figure 12. Soft-Start Ramp

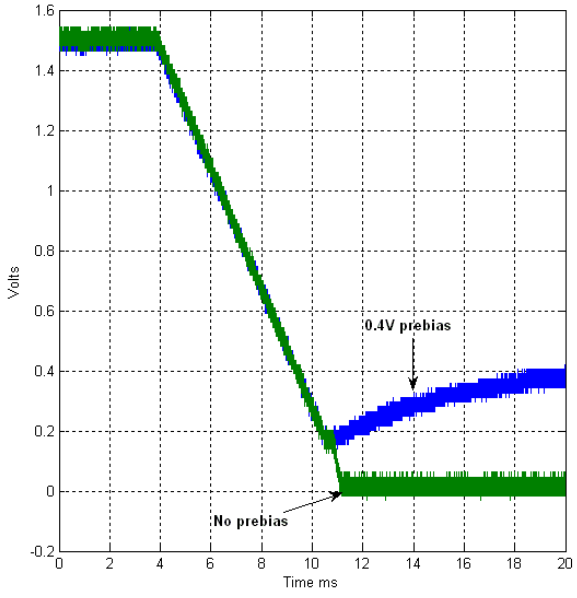


Figure 13. Soft-Stop Ramp

When a voltage rail is in its idle state, the DPWM outputs are disabled, and the differential voltage on the EAP/EAN terminals are monitored by the controller. During idle the Vref DAC is adjusted to match the feedback voltage. If there is a pre-bias (that is, a non-zero voltage on the regulated output), then the device can begin the start ramp from that voltage with a minimum of disturbance. This is done by calculating the duty cycle that is required to match the measured voltage on the rail. Nominally this is calculated as Vout / Vin. If the pre-bias voltage on the output requires a smaller pulse width than the driver can deliver, as defined by the DRIVER_MIN_PULSE PMBus command, then the start ramp is delayed until the internal ramp reference voltage has increased to the point where the required duty cycle exceeds the specified minimum duty.

Once a soft start/stop ramp has begun, the output is controlled by adjusting the Vref DAC at a fixed rate and allowing the digital compensator control engine to generate a duty cycle based on the error. The Vref DAC adjustments are made at a rate of 10 kHz and are based on the TON_RISE or TOFF_FALL PMBus configuration parameters.

Although the presence of a pre-bias voltage or a specified minimum DPWM pulse width affects the time when the DPWM signals become active, the time from when the controller starts processing the turn-on command to the time when it reaches regulation is TON_DELAY plus TON_RISE, regardless of the pre-bias or minimum duty cycle.

During a normal ramp (i.e. no tracking, no current limiting events and no EADC saturation), the set point slews at a pre-calculated rate based on the commanded output voltage and TON_RISE. Under closed loop control, the compensator follows this ramp up to the regulation point.

Because the EADC in the controller has a limited range, it may saturate due to a large transient during a start/stop ramp. If this occurs, the controller overrides the calculated set point ramp value, and adjusts the Vref DAC in the direction to minimize the error. It continues to step the Vref DAC in this direction until the EADC comes out of saturation. Once it is out of saturation, the start ramp continues, but from this new set point voltage; and therefore, has an impact on the ramp time.

8.3.24 Non-Volatile Memory Error Correction Coding

The UCD9244 uses Error Correcting Code (ECC) to improve data integrity and provide high reliability storage of Data Flash contents. ECC uses dedicated hardware to generate extra check bits for the user data as it is written into the Flash memory. This adds an additional six bits to each 32-bit memory word stored into the Flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single bit error to be detected and corrected when the Data Flash is read.

8.3.25 Data Logging

The UCD9244 maintains a data log in non-volatile memory. This log tracks the peak internal and external temperature sensor measurements, peak current measurements and fault history. The PMBus commands and data format for the Data Logging can be found in the *UCD92xx PMBus Command Reference* (SLUU337).

8.4 Device Functional Modes

8.4.1 4-Bit VID Mode

In 4-bit VID mode, the four VID input signals are used to provide the four bits of VID data, as shown in the table below. The VID lines are level-sensitive, and are periodically polled every 400µs. When the VID lines are changed to command a new voltage, there may be a delay of 500 to 600µs while the UCD9244 confirms that the VID signal levels are stable. The output voltage will then slew to the new setpoint voltage at the rate specified by the PMBus VOUT_TRANSITION_RATE command.

TERMINAL	PURPOSE	RAIL 1	RAIL 2	RAIL 3	RAIL 4
VID_A	Data bit 0 (least significant bit)	VID1A	VID2A	VID3A	VID4A
VID_B	Data bit 1	VID1B	VID2B	VID3B	VID4B
VID_C	Data bit 2	VID1C	VID2C	VID3C	VID4C
VID_S	Data bit 3 (most significant bit)	VID1S	VID2S	VID3S	VID4S

8.4.2 6-Bit VID Mode

In 6-bit VID mode, the four VID input signals are used to provide the six bits of VID data, as shown in the table below. Each of the three data lines (VID_A, VID_B, and VID_C) carries two bits of data per VID code. The bits are clocked and selected by the VID_S select line.

TERMINAL	PURPOSE	RAIL 1	RAIL 2	RAIL 3	RAIL 4
VID_A	Data bit 0 when VID_S is low, Data bit 3 when VID_S is high	VID1A	VID2A	VID3A	VID4A
VID_B	Data bit 1 when VID_S is low, Data bit 4 when VID_S is high	VID1B	VID2B	VID3B	VID4B
VID_C	Data bit 2 when VID_S is low, Data bit 5 when VID_S is high	VID1C	VID2C	VID3C	VID4C
VID_S	Select Line: Low= LSB, High = MSB	VID1S	VID2S	VID3S	VID4S

The falling edge of the VID_S line triggers the UCD9244 to read bits 2:0 on the three VID data lines. The rising edge of VID_S triggers the UCD9244 to read bits 5:3 on the three VID data lines and calculate a new VOUT setpoint. This calculation takes from 35 to 135µs. The output voltage will then slew to the new setpoint voltage at the rate specified by the VOUT_TRANSITION_RATE PMBus command.

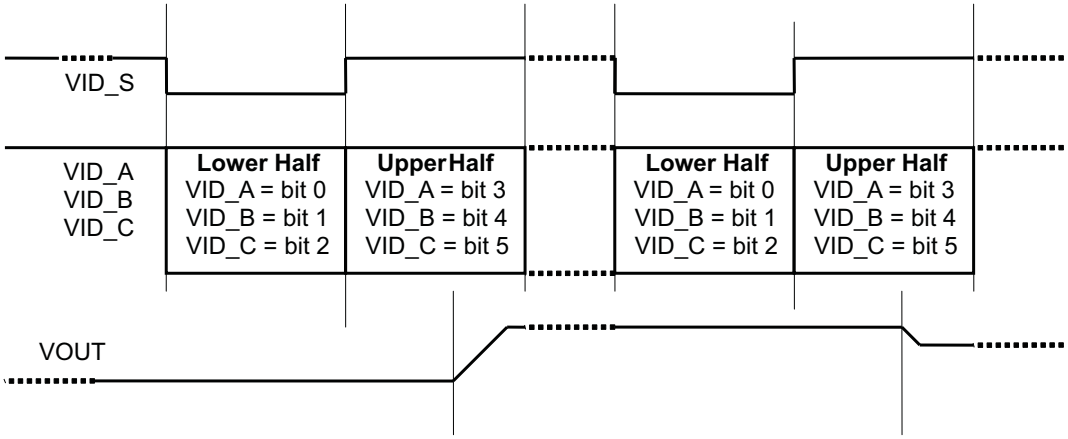


Figure 14. 6-Bit VID Data Transfer

The set-up time on the data lines is 0 µs. All four VID lines must hold at the same level for some time after a change in the VID_S line to allow the UCD9244 to read and validate the data signals and perform necessary voltage calculations. The UCD9244 can tolerate single hold times as short as 70µs, but does not have sufficient computation power to sustain continuous VID messaging that quickly. It is expected that the hold time will be at least 125µs for sustained operations. It is recommended that the DSP only send VID messages when the regulated voltage needs to change; sending the same VID code repeatedly and continuously provides no benefit.

Figure 15 and Table 6 illustrate the critical timing measurements as they apply to the 6-bit VID interface.

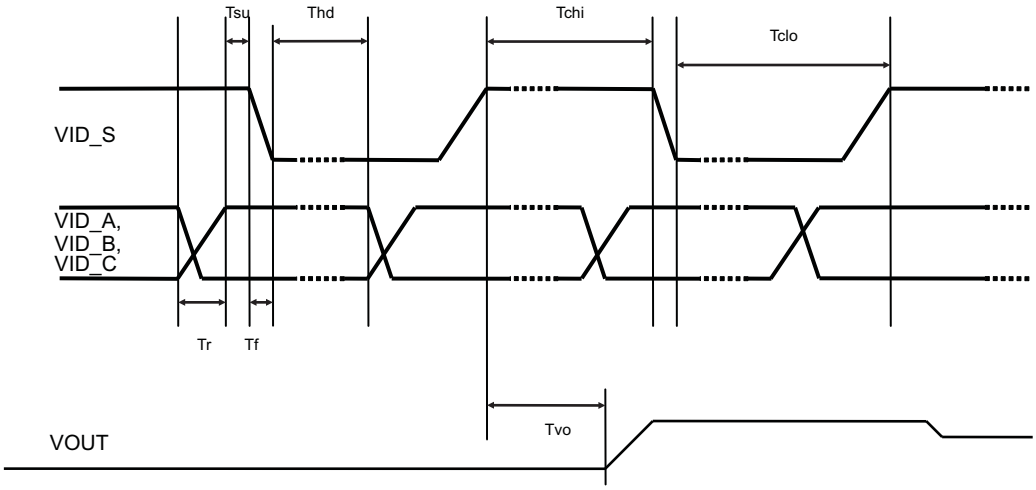


Figure 15. 6-Bit VID Timing

Table 6. 6-Bit VID Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Tr	Data and clock rise time	–		2.5	µs
Tf	Data and clock fall time	–		0.3	µs
Tsu	Data setup before changing clock	0			µs
Thd	Data hold until next clock change	70			µs
Tchi	Clock high time	70	125		µs
Tclo	Clock low time	70	125		µs
Tvo	Response time from rising edge of VID_S to start of Vout slewing to new setpoint	35		135	µs

8.4.3 8-Bit VID Mode

In 8-bit VID mode, the four VID input signals are not used. Instead, an 8-bit VID code is transmitted to the UCD9244 through the PMBus / I2C port using one of the VID_CODE_RAILn commands, where n is the rail number from 1 to 4.

NAME	DESCRIPTION (1)	CODE
VID_CONFIG	Selects the VID mode, sets the upper and lower voltage limits, and the starting voltage code at power-up.	0xBB
VID_CODE_RAIL1	Selects the VID code used to set the output voltage for Rail 1.	0xBC
VID_CODE_RAIL2	Selects the VID code used to set the output voltage for Rail 2.	0xBD
VID_CODE_RAIL3	Selects the VID code used to set the output voltage for Rail 3.	0xBE
VID_CODE_RAIL4	Selects the VID code used to set the output voltage for Rail 4.	0xBF

(1) For a complete description of the serial VID commands, see the UCD92xx PMBus Command Reference(SLUU337)

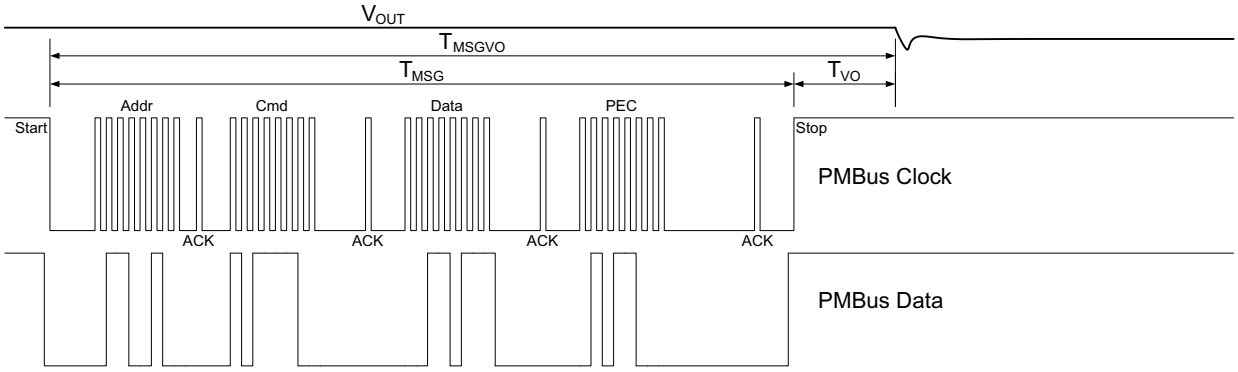


Figure 16. PMBus Timing For VID_CODE_RAILn Command

Table 7. Typical PMBus Timing For VID_CODE_RAILn Command at 400kHz

SYMBOL	PARAMETER	CONDITIONS	TYP	UNITS
T_{msgPEC}	Message Transmit Time, with PEC	400 kHz clock, PEC enabled	162 – 256	µs
	Message Transmit Time, without PEC	400 kHz clock, PEC enabled	126 – 221	
T_{vo}	End of message until Vout starts changing		28 – 140	µs
T_{msgvo}	Start of message until Vout start changing	400 kHz clock, PEC disabled	169 – 314	µs

The total time to transmit the serial VID command will vary depending on the other tasks that the UCD92xx processor is performing. Typical packet times varied from 162 to 256µs when the PMBus is configured for a 400 kb/s transfer rate running and the optional PEC byte is enabled. Disabling the PEC byte saves about 35µs and the transfer times are from 126 to 221µs. Note that these are **not** specified best-case/worst-case timings, but indicate a range given the typical acknowledge overhead in the host and controller.

After the VID packet has been received by the controller there is a delay before the set-point reference DAC is updated. This delay time varies from ~28µs to 140µs (typical) depending on the existing priority of updating set-point reference DAC when the command is received.

With a 221µs packet transfer time, it would seem possible to send 4500 VID messages per second to the device. Very short bursts at this rate might be acceptable, but doing so for sustained periods could overwhelm the available processing resources in the UCD92xx, causing it to be delayed in performing its other monitoring and fault response tasks. In addition, if multiple hosts are trying to talk on the PMBus at such high rates then bus contention will occur with great regularity.

To prevent these issues, it is prudent to limit the total VID messaging rate to less than 4 messages per millisecond. In a system with four independent hosts, each host might need to be limited to less than 1 message per millisecond. Therefore, to minimize PMBus traffic, it is best to only issue the VID command when a voltage change is required. There is no benefit to sending the same VID code continuously and repeatedly.

8.4.4 Current Foldback Mode

When the measured output current exceeds the value specified by the IOUT_OC_FAULT_LIMIT command, the UCD9244 attempts to continue to operate by reducing the output voltage in order to maintain the output current at the value set by IOUT_OC_FAULT_LIMIT. This continues indefinitely as long as the output voltage remains above the minimum value specified by IOUT_OC_LV_FAULT_LIMIT. If the output voltage is pulled down to less than that value, the device responds as programmed by the IOUT_OC_LV_FAULT_RESPONSE command.

9 Applications and Implementation

9.1 Application Information

9.1.1 Automatic System Identification (Auto-ID™)

By using digital circuits to create the control function for a switch-mode power supply, additional features can be implemented. One of those features is the measurement of the open loop gain and stability margin of the power supply without the use of external test equipment. This capability is called automatic system identification or Auto-ID™. To identify the frequency response, the UCD9244 internally synthesizes a sine wave signal and injects it into the loop at the Vref DAC. This signal excites the system, and the closed-loop response to that excitation can be measured at another point in the loop. The UCD9244 measures the response to the excitation at the output of the digital compensator. From the closed-loop response, the open-loop transfer function is calculated. The open-loop transfer function may be calculated from the closed-loop response.

Note that since the compensator and DPWM are digital, their transfer functions are known exactly and can be divided out of the measured open-loop gain. In this way the UCD9244 can accurately measure the power stage/load plant transfer function in situ (in place), on the factory floor or in an end equipment application and send the measurement data back to a host through the PMBus interface without the need for external test equipment. Details of the Auto-ID™ PMBus measurement commands can be found in the *UCD92xx PMBus Command Reference* (SLUU337).

9.2 Typical Applications

Figure 17 shows the UCD9244 power supply controller as part of a system that provides the regulation of two independent power supplies. The loop for each power supply is created by the respective voltage outputs feeding into the differential voltage error ADC (EADC) inputs, and completed by DPWM outputs feeding into the gate drivers for each power stage.

The $\pm V_{sense}$ rail signals must be routed to the EAp/EAn input that matches the DPWM number that controls the output power stage. For example, the power stage driven by DPWM1A must have its feedback routed to EAP1 and EAN1.

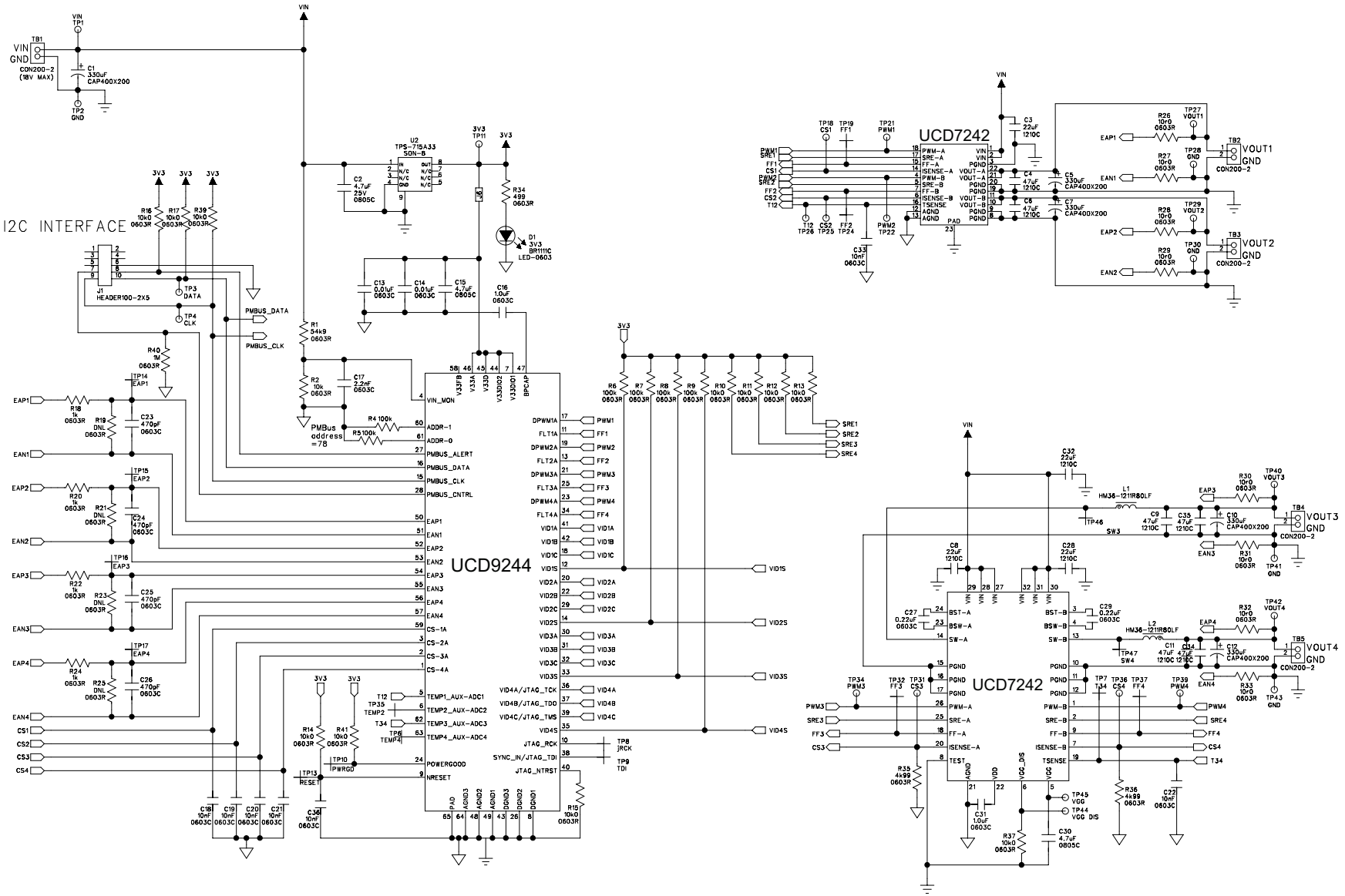


Figure 17. Typical Application Schematic

9.2.1 Design Requirements

DESIGN PARAMETER	APPROXIMATE		UNITS
	LOWER BOUND	UPPER BOUND	
K_{DC}	60	103	dB
F_Z	3 kHz	Fsw/5	kHz
Q_Z	0.1	5.0	n/a

9.2.2 Detailed Design Procedure

9.2.2.1 Digital Compensator

Each voltage rail controller in the UCD9244 includes a digital compensator. The compensator consists of a nonlinear gain stage, followed by a digital filter consisting of a second order infinite impulse response (IIR) filter section cascaded with a first order IIR filter section.

The Texas Instruments Fusion Digital Power™ Designer development tool can be used to assist in defining the compensator coefficients. The design tool allows the compensator to be described in terms of the pole frequencies, zero frequencies and gain desired for the control loop. In addition, the Fusion Digital Power™ Designer can be used to characterize the power stage so that the compensator coefficients can be chosen based on the total loop gain for each feedback system. The coefficients of the filter sections are generated through modeling the power stage and load.

Additionally, the UCD9244 has three banks of filter coefficients: Bank-0 is used during the soft start/stop ramp or tracking; Bank-1 is used while in regulation mode; and Bank-2 is used when the measured output current is below the configured light load threshold.

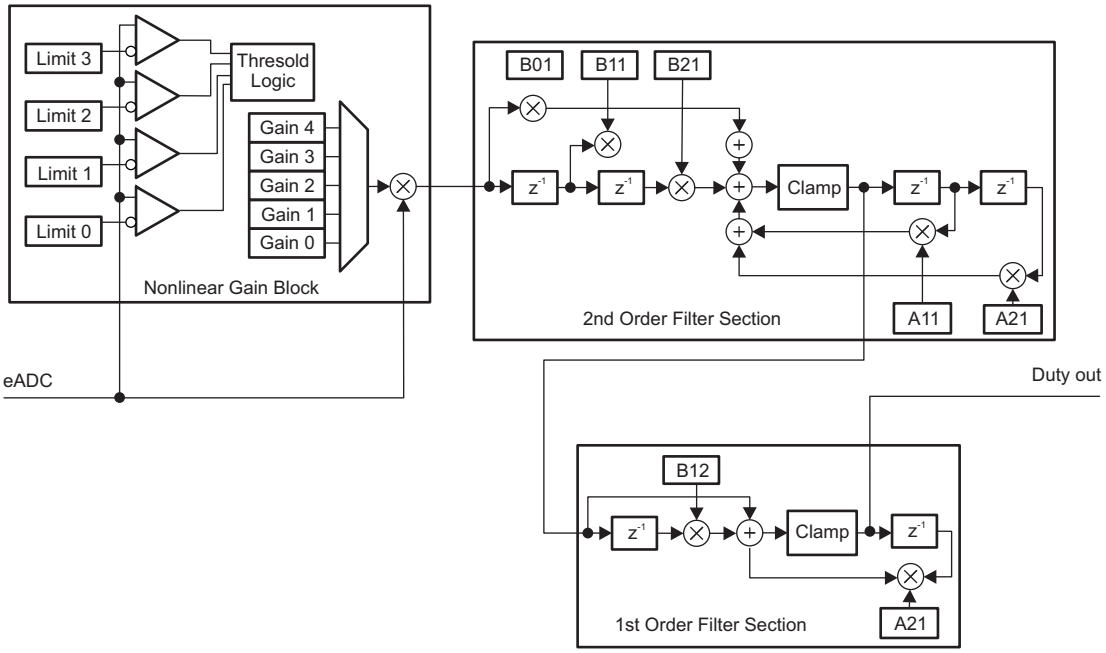


Figure 18. Digital Compensator

To calculate the values of the digital compensation filter continuous-time design parameters K_{DC}, F_Z ands Q_Z are entered into the Fusion Digital Power Designer software (or it calculates them automatically). Where the compensating filter transfer function is

$$H(s) = K_{DC} \frac{\frac{S^2}{\omega_Z^2} + \frac{s}{\omega_Z Q_Z} + 1}{s\left(\frac{s}{\omega_{P2}} + 1\right)} \quad (14)$$

There are approximate limits the design parameters K_{DC}, F_Z ands Q_Z. Though design parameters beyond these upper a lower bounds can be used to calculate the discrete-time filter coefficients, there will be significant round-off error when the continuous-time floating-point design parameters are converted to the discrete-time fixed-point integer coefficients to be downloaded to the controller.

The nonlinear gain block allows a different gain to be applied to the system when the error voltage deviates from zero. Typically Limit 0 and Limit 1 would be configured with negative values between –1 and –32 and Limit 2 and Limit 3 would be configured with positive values between 1 and 31. However, the gain thresholds do not have to be symmetrical. For example, the four limit registers could all be set to positive values causing the Gain 0 value to set the gain for all negative errors and a nonlinear gain profile would be applied to only positive error voltages.

The cascaded 1st order filter section is used to generate the third zero and third pole.

10 Power Supply Recommendations

The recommended power supply for analog and digital is from 3 V to 3.6 V.

11 Layout

11.1 Layout Guidelines

The UCD9244 device has separate analog and digital ground terminals, and separate analog, digital, and I/O power terminals. Tying the analog and digital ground together to a ground plane under the controller has been shown to produce good results. The V33A terminal requires very good decoupling. If desired, this terminal can be separated from the V33D and V33IO terminals with a ferrite bead; in most cases, this bead is not necessary.

11.2 Layout Example

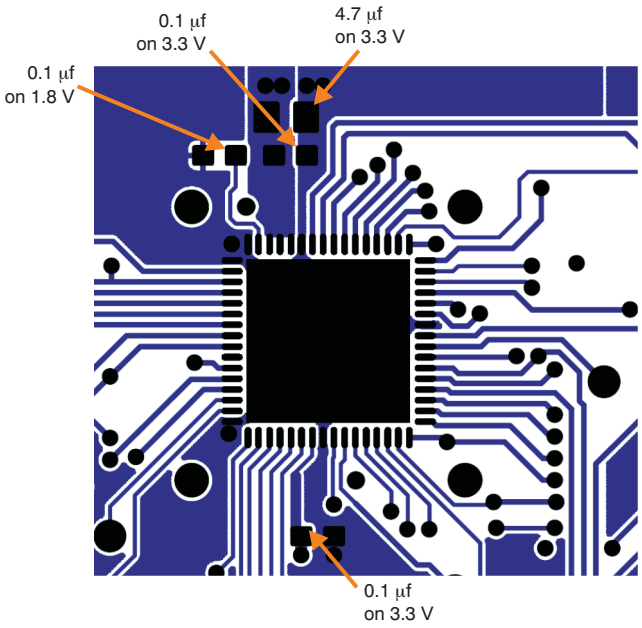


Figure 19. Recommended Decoupling Capacitor Layout

Refer to design guide SLUU490 for details.

12 Device and Documentation Support

12.1 Trademarks

TMS320C6670, TMS320C6678, Fusion Digital Power, Auto-ID are trademarks of Texas Instruments.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD9244MRGCTEP	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	UCD9244EP
UCD9244MRGCTEP.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	UCD9244EP
V62/14603-01XE	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	UCD9244EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCD9244-EP :

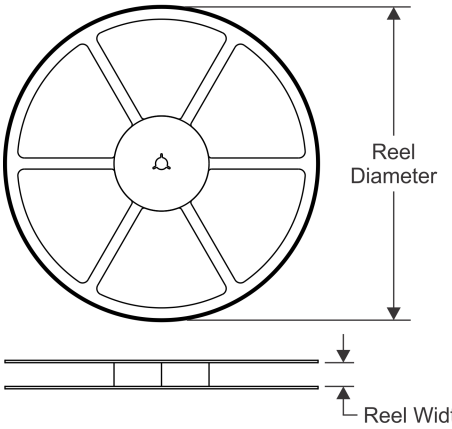
- Catalog : UCD9244

NOTE: Qualified Version Definitions:

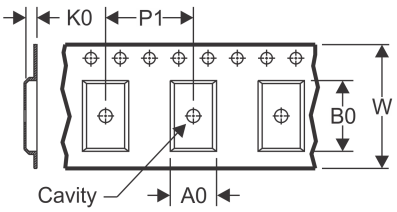
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

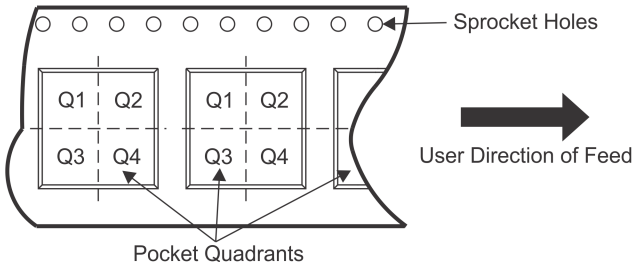


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

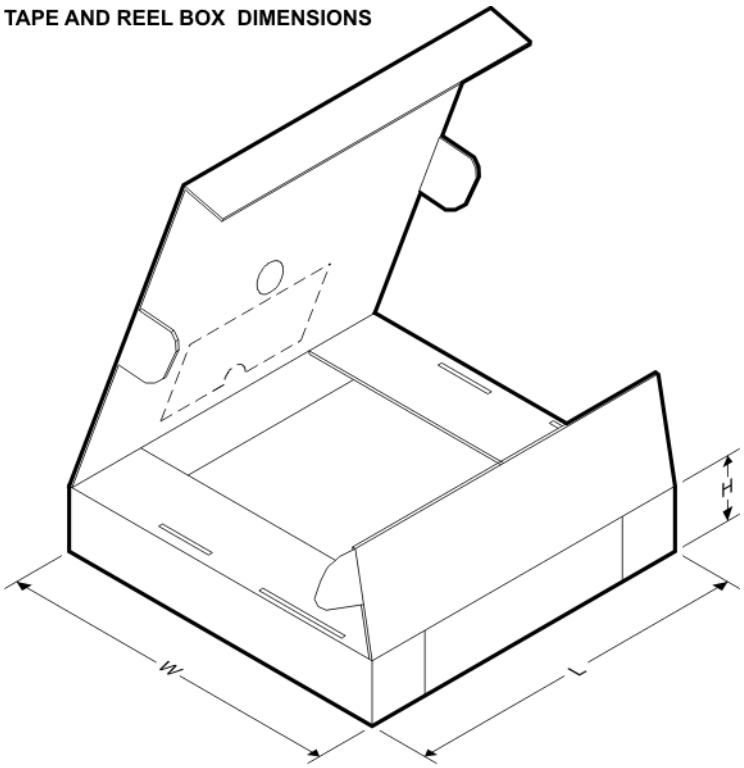
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD9244MRGCTEP	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD9244MRGCTEP	VQFN	RGC	64	250	210.0	185.0	35.0

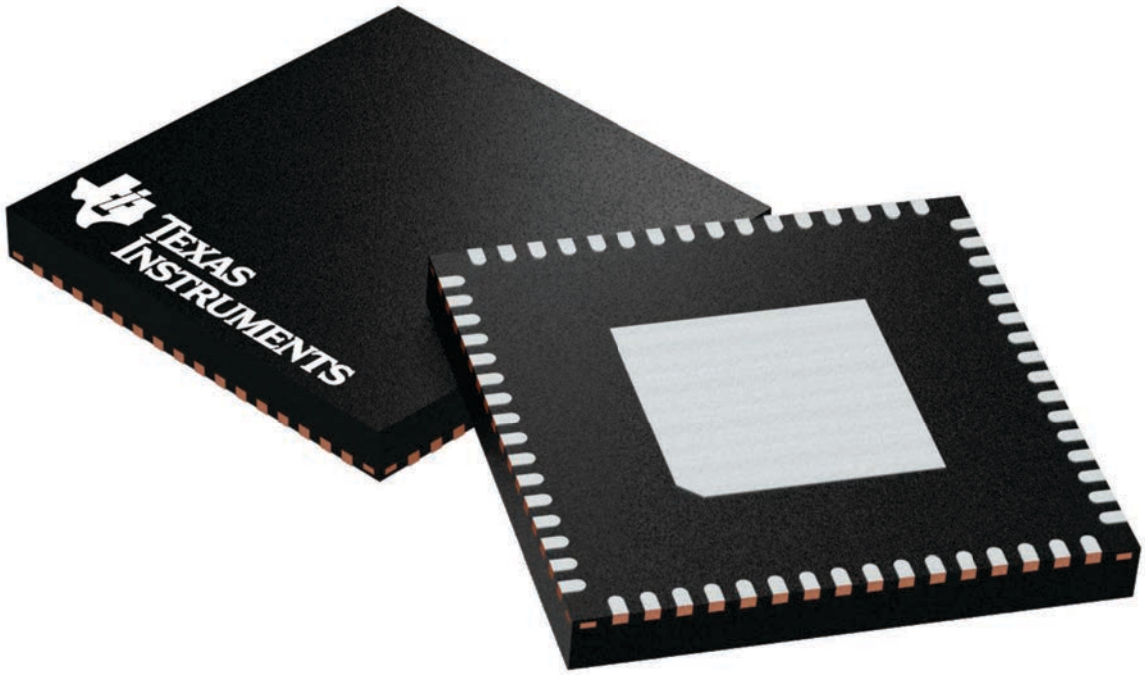
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

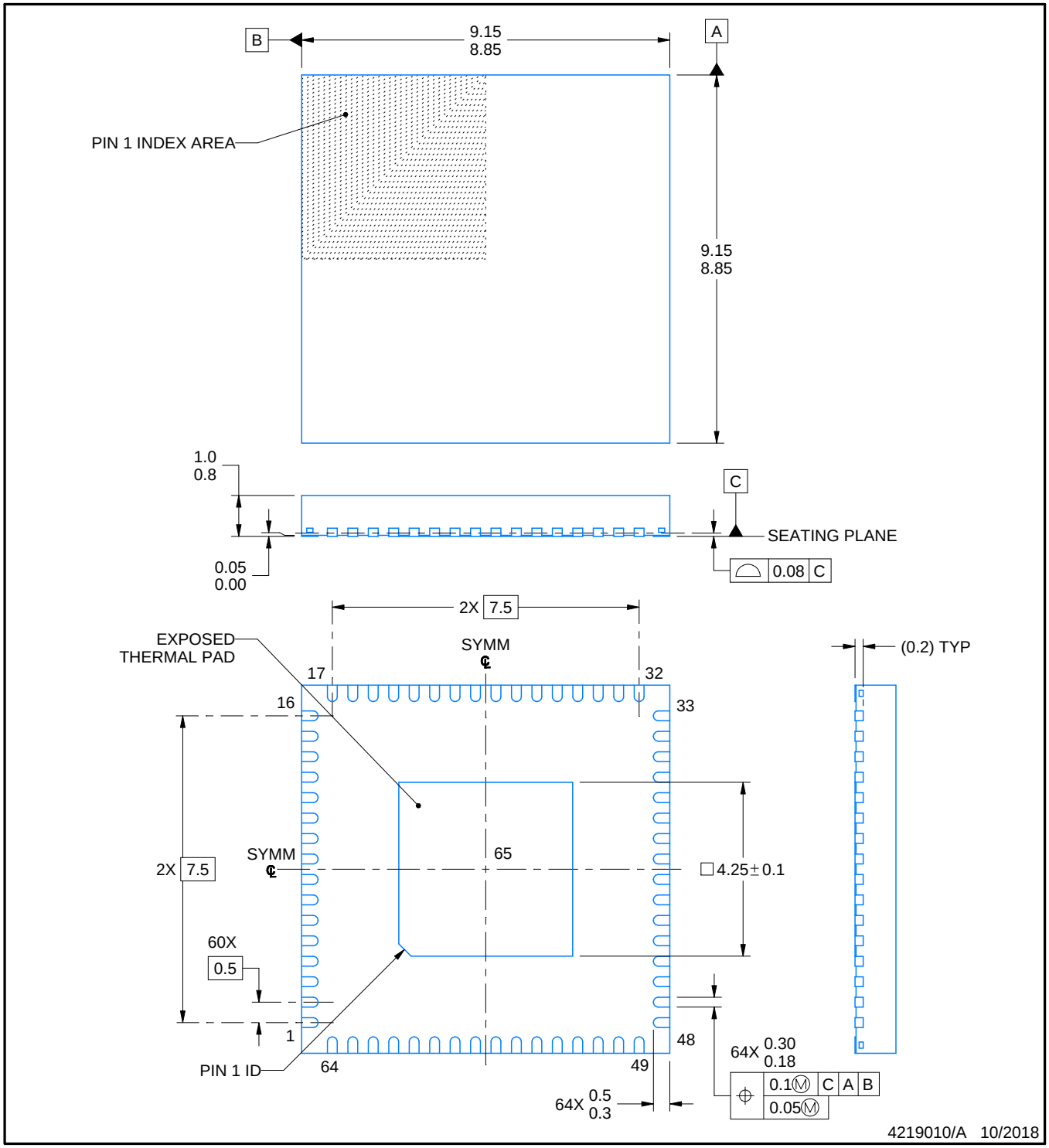
4224597/A

PACKAGE OUTLINE

RGC0064B

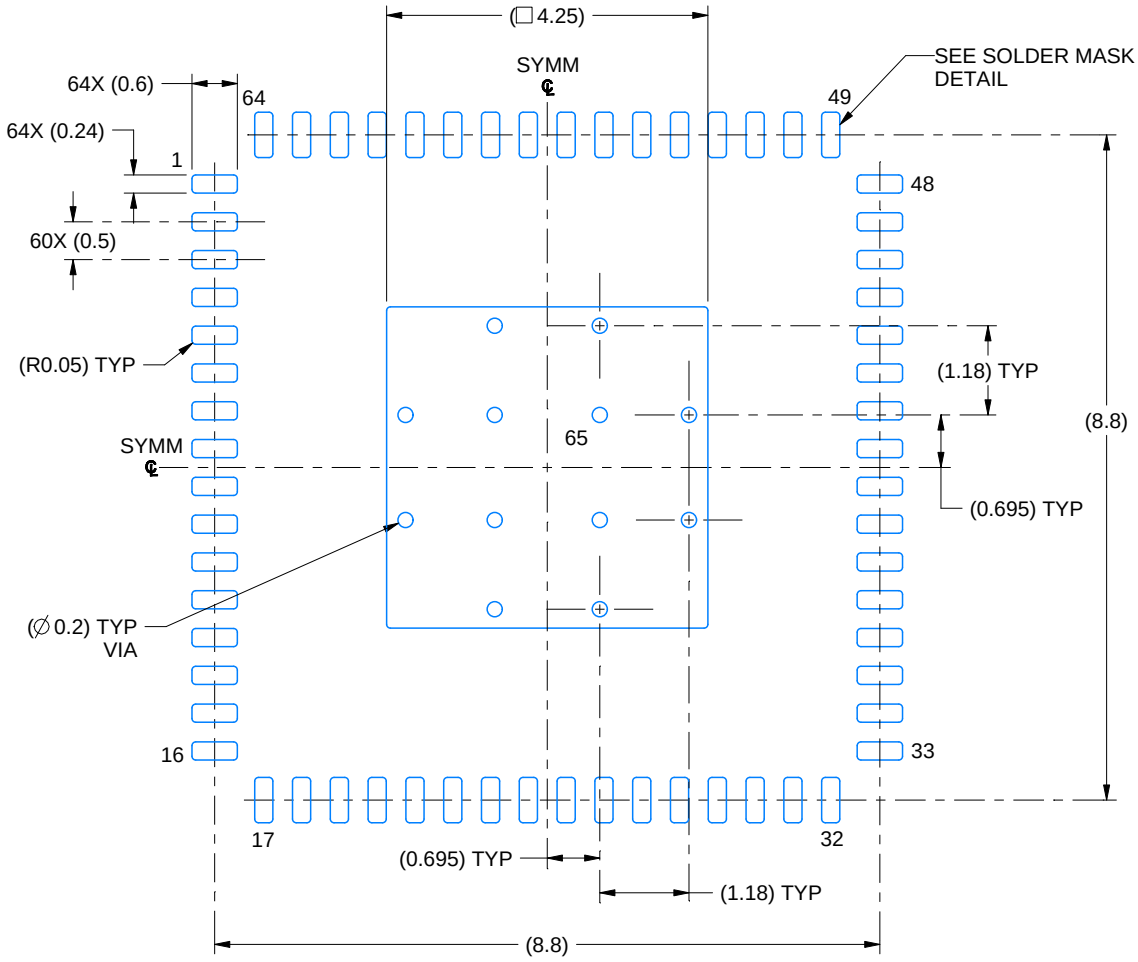
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

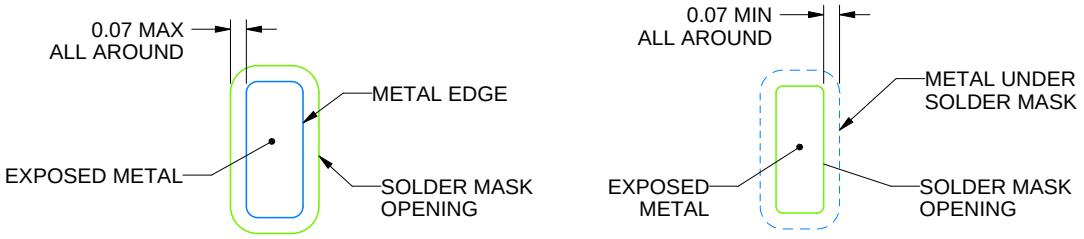


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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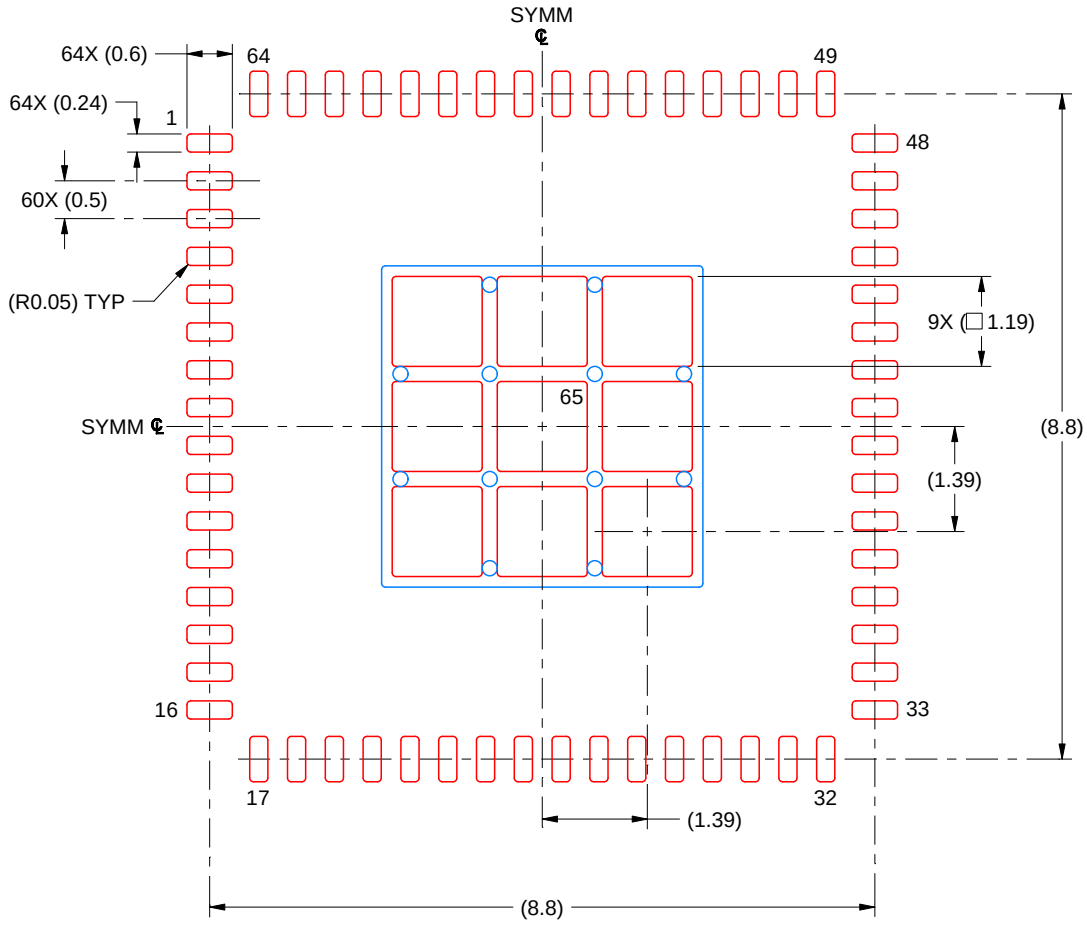
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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