EVM User's Guide: ADS125P08EVM-PDK

ADS125P08EVM-PDK Evaluation Module

Description

The ADS125P08 evaluation module (EVM) is a platform for evaluating the performance of the ADS125P08, which is a 24-bit, 16-channel, 1-MSPS, multiplexed delta-sigma (ΔΣ) analog-to-digital converter (ADC) designed for low-latency, high-precision data acquisition systems. The ADS125P08 integrates a highly-flexible channel sequencer, a low noise voltage reference, a clock oscillator, and many diagnostic features to aid in the design of high-reliability systems. The ADS125P08EVM-PDK eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface.

Get Started

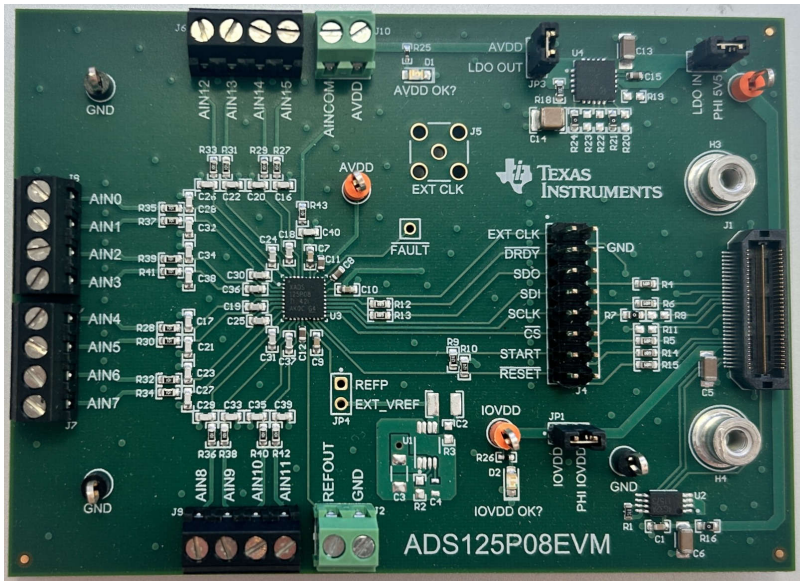
1. Order the EVM from ti.com
2. Download the latest software from the ADS125P08EVM-PDK tool folder
3. Launch the ADS125P08 EVM GUI from the start menu
4. Connect the ADS125P08 EVM to the PHI controller board
5. Connect the PHI board to the computer running the ADS125P08 EVM GUI

Features

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS125P08
- The PHI controller provides a convenient communication interface to the ADS125P08 over USB 2.0 (or higher) for digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft® Windows® 10 operating system
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing

Applications

- PLC analog input modules
- Medical
- Data acquisition



1 Evaluation Module Overview

1.1 Introduction

The ADS125P08EVM-PDK is a platform for evaluating the performance of the ADS125P08, a 24-bit, 16-channel, 1-MSPS multiplexed delta-sigma ADC designed for low-latency, high-precision data acquisition systems. The evaluation kit includes the ADS125P08 EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis. The ADS125P08 EVM includes the ADS125P08 and all the peripheral analog circuits and components required to evaluate the performance of the ADS125P08. The PHI board provides a communication interface from the ADS125P08 EVM to the computer through a USB port.

This EVM user guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS125P08 EVM.

1.2 Kit Contents

Figure 1-1 shows that the ADS125P08EVM-PDK includes the following components:

1. The PHI controller board
2. The ADS125P08 EVM that includes the ADS125P08 and peripheral circuitry required for device operation and communication with the PHI board.
3. An A-to-Micro-B USB cable for communication between the PHI board and the EVM GUI.
4. The EVM GUI, which can be found online in the EVM tool folder

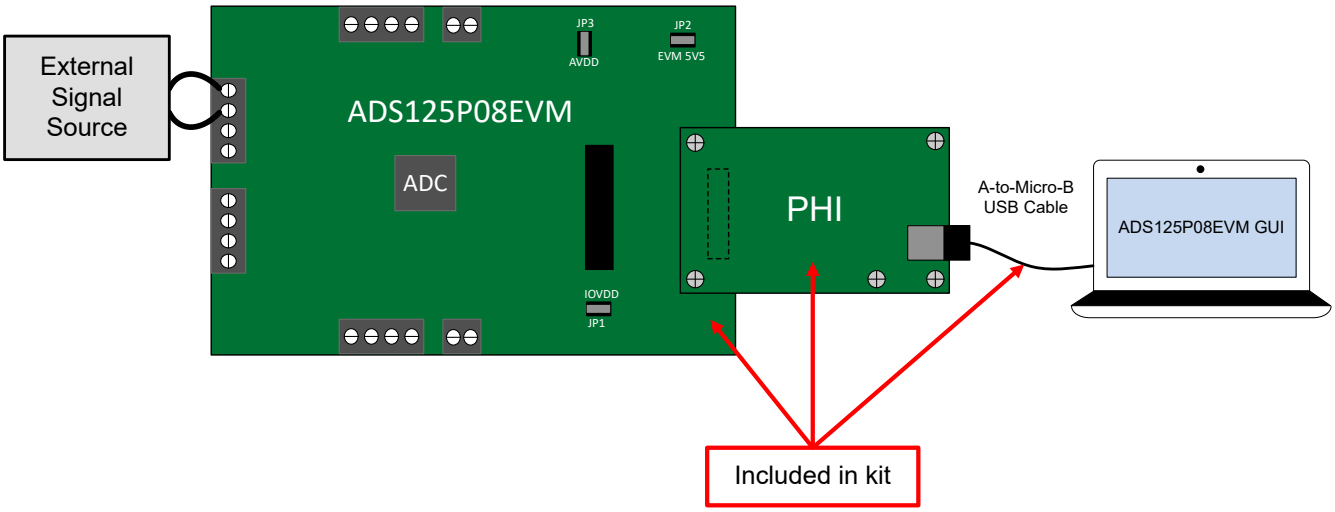


Figure 1-1. System Connection for Evaluation

1.3 EVM Specifications

The following specifications are applicable to the ADS125P08 EVM and the PHI board.

Table 1-1. ADS125P08 EVM Specifications

PARAMETER	CONDITIONS		VALUE
Temperature	Recommended operating free-air temperature range, T_A		15°C ≤ T_A ≤ 35°C
Power supply input range	Recommended voltage input range for JP2-2 with respect to GND		5.5V ≤ +Vin ≤ 6.5V
	Supply current range $\|I_s\|$		0.25A ≤ |Is| ≤ 0.5A
Input voltage range	Absolute input voltage with respect to GND for AIN0 to AIN15 inputs	Input buffer off	AVSS +0.1V ≤ AINx ≤ AVDD - 0.1V
		Input buffer on	AVSS - 0.05V ≤ AINx ≤ AVDD - 0.2V
EXT clock	Recommended frequency range (f_{CLK})		0.5MHz ≤ f_{CLK} ≤ 26.2MHz
External digital IO (including EXT clock)	Recommended logic levels (applied to header J12 or connector J13) with respect to GND	Logic Level Low (V_{IOl})	0V ≤ V_{CLKl} ≤ 0.3×IOVDD
		Logic Level High (V_{IOh})	0.7×IOVDD ≤ V_{CLKh} ≤ IOVDD
ADS125P08 AVDD to AVSS	Recommended voltage range (applied to JP3-2), external source	High-speed or Mid-speed mode	4.5V ≤ AVDD ≤ 5.5V
		Low-speed or Very-low-speed mode	3V ≤ AVDD ≤ 5.5V
ADS125P08 |AVSS/AVDD1| ratio to GND	Recommended absolute ratio range, external source, DGND = GND		|AVSS/AVDD1| ≤ 1.2V/V
ADS125P08 AVSS to GND	Recommended voltage range (JP2 2-3 position), DGND = GND		-2.75V ≤ AVSS ≤ 0V
ADS125P08 IOVDD to GND	Recommended voltage range (applied to JP1-1), external source, DGND = GND		1.65V ≤ IOVDD ≤ 5.5V
ADS125P08 Reference REFP to AVSS	Recommended voltage range (J9 installed, U20 not installed), external source	REFP buffer off	1V ≤ REFP ≤ AVDD + 0.05V
		REFP buffer on	1V ≤ REFP ≤ AVDD - 0.7V

1.4 Device Information

Please refer to ADS125P08 data sheet for complete specifications.

Table 1-2. ADS125P08 Device Specifications

PARAMETER	VALUE
ADC resolution	24 bits
Maximum data rate	1.067 MSPS
Channel count	17 (16 AINx + 1 AINCOM); fully flexible multiplexer
Integrated features	• Flexible channel sequencer • FIFO buffer • Voltage reference • Oscillator • Test DAC • Fault detection
Package	VQFN-36
Package size	5.00mm × 5.00mm
Specified temperature range	-40°C ≤ T_A ≤ 125°C

2 Hardware

2.1 Analog Inputs

The ADS125P08 EVM provides external connection points for all 17 channels so the user can easily apply and measure signals with the ADC. Access channels AIN0 through AIN15 on terminal blocks J6 to J9, and AINCOM through terminal block J10. Figure 2-1 shows the schematic for analog inputs AIN12 to AIN15, which is representative of all other analog inputs not shown in this image. This figure also shows terminal block J10, which allows access to the AINCOM input and an AVDD output.

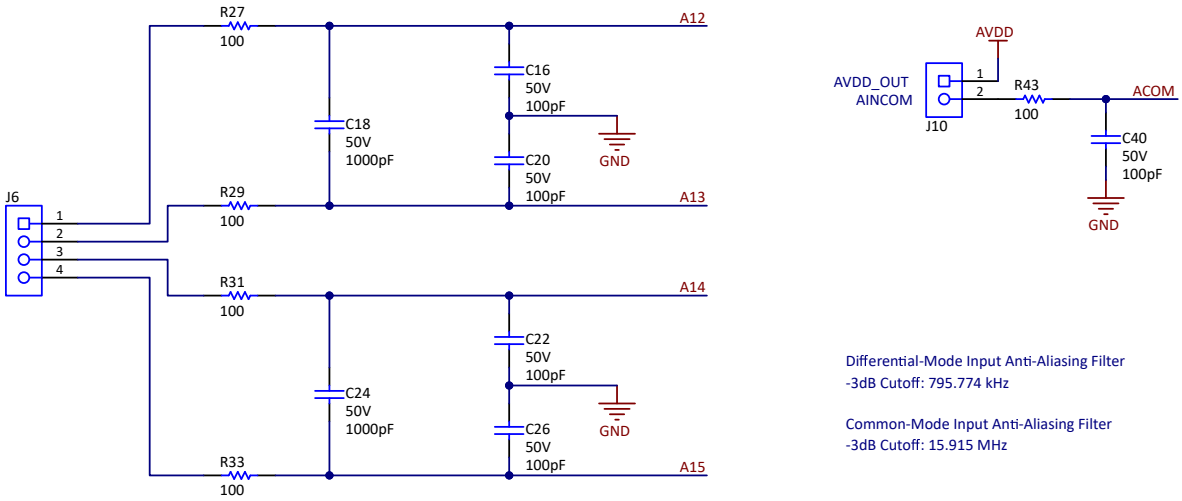


Figure 2-1. Accessing the Analog Inputs (AIN12 to AIN15, and AINCOM)

Each adjacent analog input pair includes a set of low-pass filters to prevent aliasing. The differential filters have a 3dB cutoff of 795.774kHz. As an example, Figure 2-1 shows that capacitor C18 and resistors R27 and R29 create the differential filter between analog inputs AIN12 and AIN13. The common-mode filters have a 3dB cutoff of 15.915MHz. As an example, Figure 2-1 shows that capacitor C16 and resistor R27 create the common-mode filter for analog input AIN12. Precision 5% C0G or NPO-type capacitors and 0.1% resistors are used in the analog signal chain to reduce measurement error.

Verify that the signal source voltage and current levels applied to terminal blocks J6 through J10 meet the specifications listed in Table 1-1.

2.2 ADC Connections and Decoupling

Figure 2-2 shows all connections to the ADS125P08 data converter. AVDD and IOVDD have a 100nF decoupling capacitor, while REFOUT and the internal analog and digital LDOs (CAPA and CAPD, respectively) each have a 1µF decoupling capacitor. Make sure these capacitors are physically close to the device and have a good connection to the GND plane. Each digital pin has a 49.9Ω series resistor near the driving source. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. Although not strictly required, these components can be included in the final design to improve digital signal integrity. Also, digital inputs $\overline{\text{RESET}}$ and START each have a 120kΩ pullup or pulldown resistors to verify that the ADC powers up in a known state.

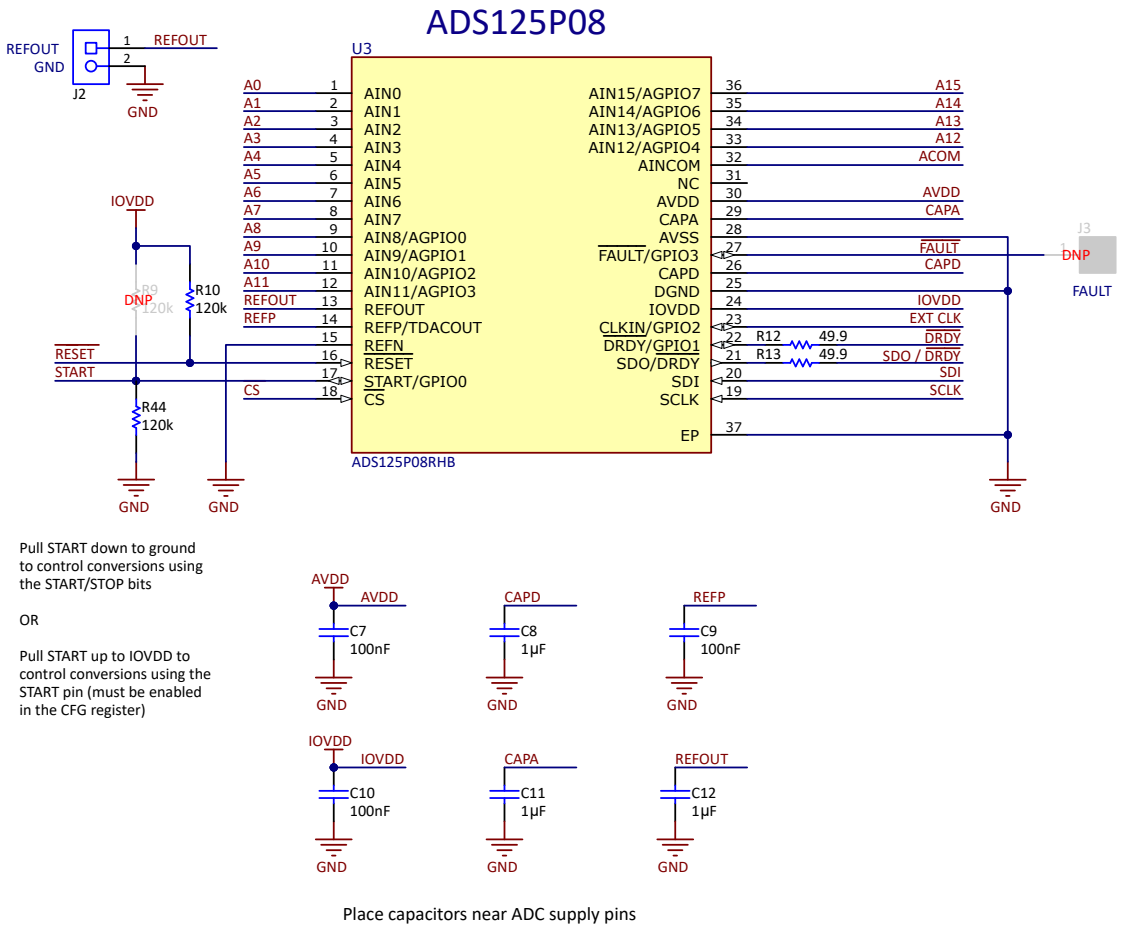


Figure 2-2. ADC Connections and Decoupling

2.3 Digital Interface

As noted in Section 1.1, the EVM interfaces with the PHI and communicates with the computer over the USB. The PHI communicates with two devices on the EVM: the ADS125P08 (over SPI) and the EEPROM (over I2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS125P08 platform. When the hardware is initialized, the EEPROM is no longer used

The ADS125P08 requires SPI serial communication such that CPOL = 0 and CPHA = 1. Header J4, shown in Figure 2-3, provides test points to probe the digital signals with a logic analyzer. Additionally, jumper J4 can be used to connect communication signals from an external controller. Remove the PHI controller card from connector J1 before applying external signals to jumper J4.

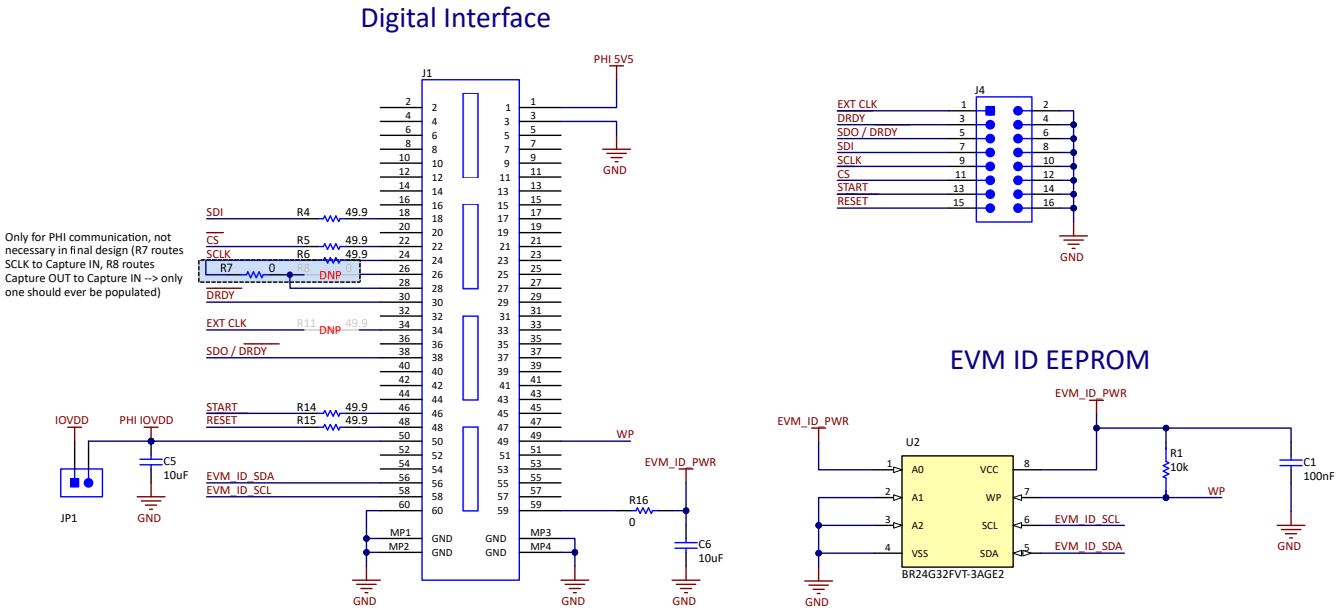


Figure 2-3. EVM Digital Interface and EEPROM

Similar to Figure 2-2, each digital pin has a 49.9Ω series resistor near the driving source. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. Although not strictly required, these components can be included in the final design to improve digital signal integrity.

Figure 2-3 also shows that jumper JP1 connects the PHI_IOVDD and IOVDD nets. By default, the PHI_IOVDD net provides 3.3V to the ADC digital supply (IOVDD) pin through jumper JP1. Remove the shunt on JP1 and apply a current meter (ammeter) to measure the digital current consumed by the ADC. If desired, removing the shunt on jumper JP1 also enables connection of an external IOVDD power source to pin 1 of jumper JP1. Verify that the IOVDD voltage applied to pin 1 of jumper JP1 is the same as the I/O voltage used by the PHI or the external controller, if applicable.

2.4 Power Supplies

Figure 2-4 shows the analog supply circuitry included on the ADS125P08 EVM. The default configuration applies a unipolar, 5V voltage to the ADC analog supply (AVDD) pin. Options are provided for external supplies. LEDs indicate if the supply voltages are valid. Table 2-1 describes the function of important EVM power supply components.

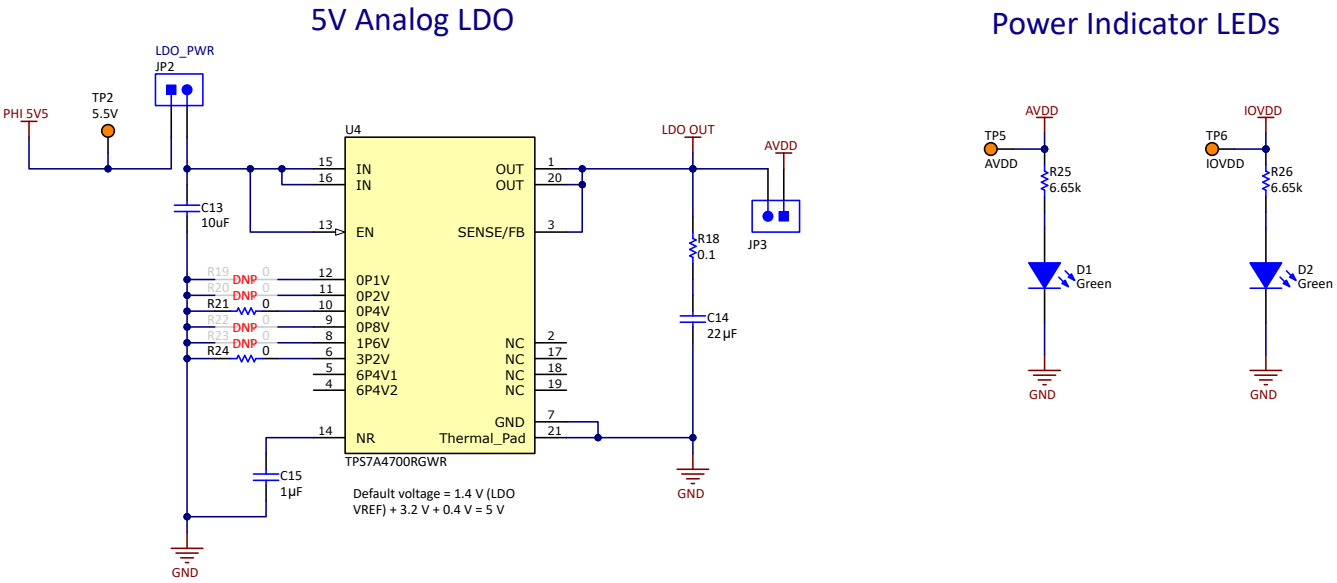


Figure 2-4. EVM Power Supplies

Table 2-1. Important Components (Power Supplies)

Component	Purpose
LDO input jumper (JP2)	Selects the LDO power source: connect the shunt to use the 5.5V voltage from the PHI; alternatively, remove the shunt and connect an external voltage to pin 2 of jumper JP2
TPS7A4700: adjustable, positive LDO (U4)	• Uses the voltage connected to pin 2 of jumper JP2 as the input voltage and outputs 5V to AVDD by default • If necessary, adjust the LDO output voltage using resistors R19 to R24
AVDD jumper (JP3)	• Remove the shunt and apply a current meter (ammeter) to measure the analog current consumed by the ADC • If desired, apply an external voltage directly to the ADC AVDD pin using pin 1. Verify that the input voltage is within the range specified by the ADC datasheet
LEDs (D1 and D2)	Indicates if IOVDD (D2) and AVDD (D1) power supplies are valid

By default, the ADS125P08 EVM is configured to use a unipolar supply voltage that is supplied by a 5.5V voltage from the PHI controller card. However, changing the adjustable LDO (U4) output voltage by removing and replacing resistors R19 to R24 is possible. For example, set the LDO output voltage to 3V by removing 0Ω resistors R21 and R24, then installing 0Ω resistor R23 (1.6V). The LDO output voltage is 1.4V + 1.6V = 3V because the LDO VREF = 1.4V.

2.5 Voltage Reference

Figure 2-5 shows an optional external voltage reference circuit included on the ADS125P08 EVM. The ADS125P08 integrates a low-noise, low-drift voltage reference that is sufficient for most applications. Alternatively, the EVM supports two external voltage reference options if desired. First, install header pin J11 and apply an external voltage source to this pin. Second, the EVM includes the 2.5V voltage reference REF6025 as well as the required passive components. However, these components are not included on the EVM by default and therefore must be installed by the user. Verify that any external reference voltage applied to the ADC meets the voltage requirements as described in Table 1-1. Additionally, the ADC registers need to be configured to use an external reference. See the ADC data sheet for more information.

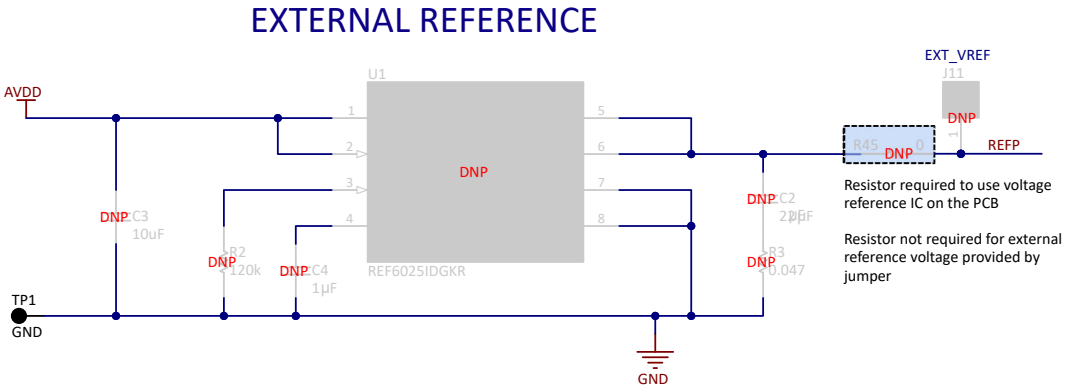


Figure 2-5. Optional External Reference Voltage Circuit

2.6 Clocking

Figure 2-6 shows an optional external clock connection on the ADS125P08 EVM using an SMA connector. The ADS125P08 integrates a high-accuracy oscillator that is sufficient for most applications. If necessary, component footprints are included on the EVM that enable an external clock. By default, the SMA connector and series resistance are not installed, and therefore must be added to the EVM by the user. Verify that any external clock signal applied to the ADC meets the clocking requirements as described in Table 1-1. Additionally, the ADC registers need to be configured to use an external clock. See the ADC data sheet for more information.

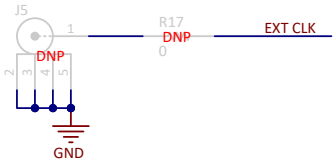


Figure 2-6. Optional External Clock Connection

2.7 Using the ADS125P08 EVM With an External Controller

The ADS125P08 EVM is designed for easy connection to an external controller. This design enables the user to test application code and firmware on the ADS125P08 without having to develop a custom PCB. This section describes the specific connections required to use the ADS125P08 EVM with an external controller. Figure 2-7 shows the location of various headers, connectors, and terminal blocks described in this section.

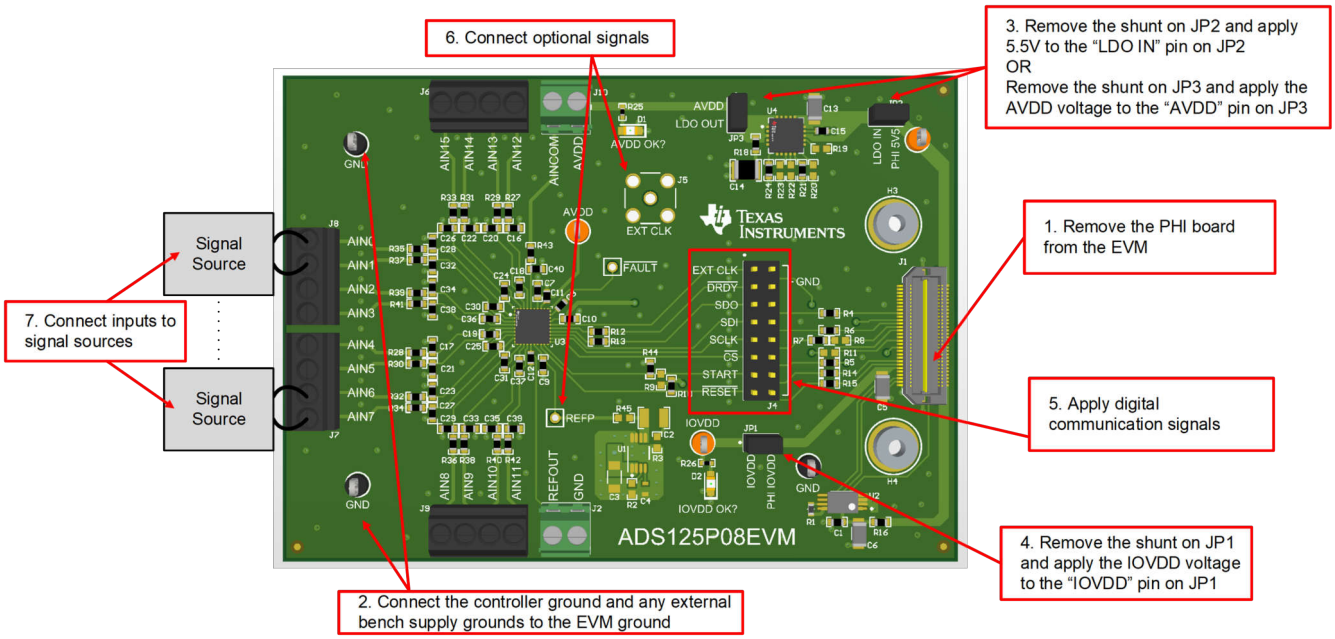


Figure 2-7. Connecting an External Controller to the ADS125P08 EVM

Complete the following steps to prepare the ADS125P08 EVM for use with an external controller:

1. Remove the PHI board if still connected to the EVM
2. Connect the external controller ground and bench supply ground to the GND pins on the EVM
3. Connect an external bench supply to the ADC AVDD pin by performing only one of the following two options:
   a. Remove the shunt on JP2 and apply 5.5V to the "LDO_IN" pin on JP2
   b. Remove the shunt on JP3 and apply the AVDD voltage to the "AVDD" pin on JP3
4. Connect an external bench supply to the ADC IOVDD pin by removing the shunt on JP1 and applying the IOVDD voltage to the "IOVDD" pin on JP1
5. Apply digital communication signals to header J4 on the EVM:
   a. Connect POCI (peripheral out, controller in) from the controller to the SDO pin
   b. Connect PICO (peripheral in, controller out) from the controller to the SDI pin
   c. Connect SCLK from the controller to the SCLK pin
   d. Connect $\overline{CS}$ from the controller to the $\overline{CS}$ pin
   e. Connect an I/O pin from the controller to the $\overline{DRDY}$ pin. $\overline{DRDY}$ is an output from the ADC that indicates when new data are ready to be clocked out of the ADC. Write a user-defined data collection routine that monitors this pin (polling or interrupt) and only transfers data after a falling edge
   f. (Optional) Connect I/O pins from the controller to the START and $\overline{RESET}$ pins to control conversions and reset the device, respectively
6. (Optional) Connect an external Section 2.6 or Section 2.5
7. Connect the signal source to the terminal blocks

Verify that the external power supply voltages, communication signal levels, and applied input signals meet the specifications listed in Table 1-1

3 Software

3.1 Software Description

The ADS125P08EVM-PDK-GUI software suite includes graphical tools for data capture, full ADS125P08 register configuration, time domain analysis, spectral analysis, and histogram analysis. This suite also has a provision for exporting data to a text file for post-processing.

3.2 ADS125P08 GUI Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS125P08 EVM and run the GUI installer to install the EVM GUI software on your computer.

Note

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear or the installer.exe file can be deleted.

Figure 3-1 through Figure 3-4, show the prompts seen by the user during the GUI installation process. Accept the license agreement and follow the on-screen instructions to complete the installation.

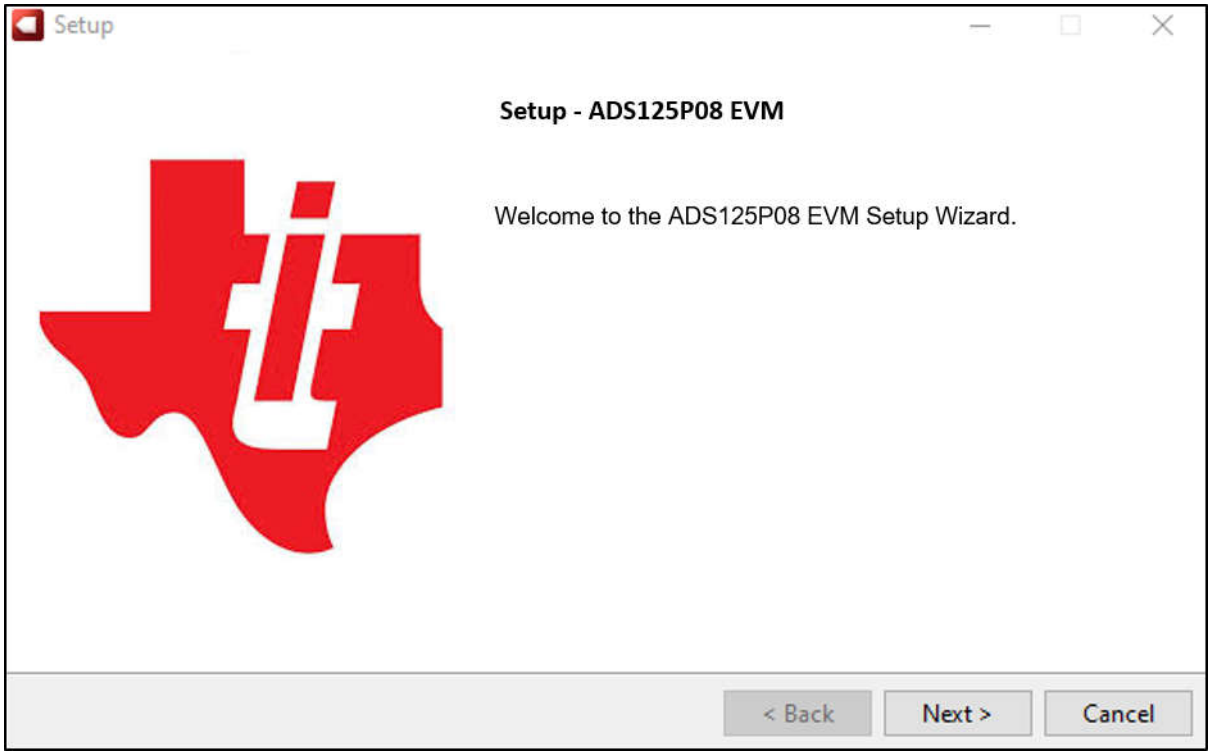


Figure 3-1. ADS125P08 EVM GUI Install Welcome Screen

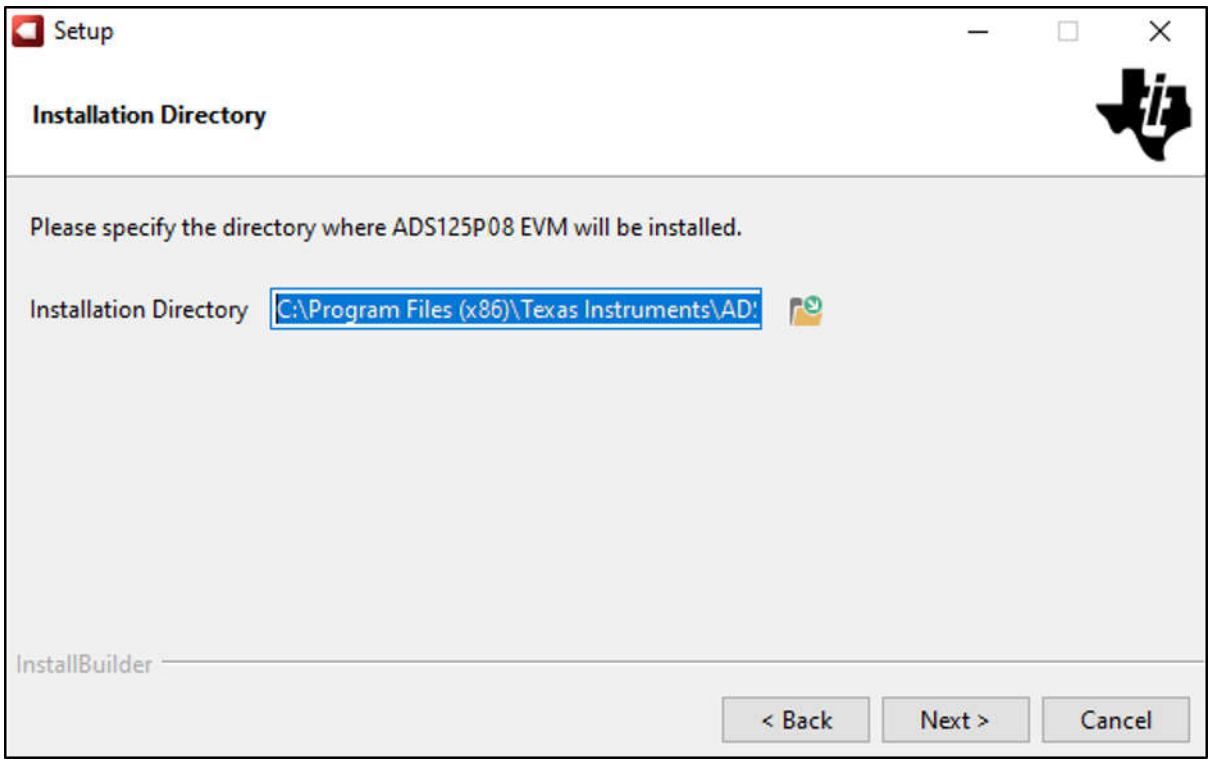


Figure 3-2. ADS125P08 EVM GUI Select Install Directory

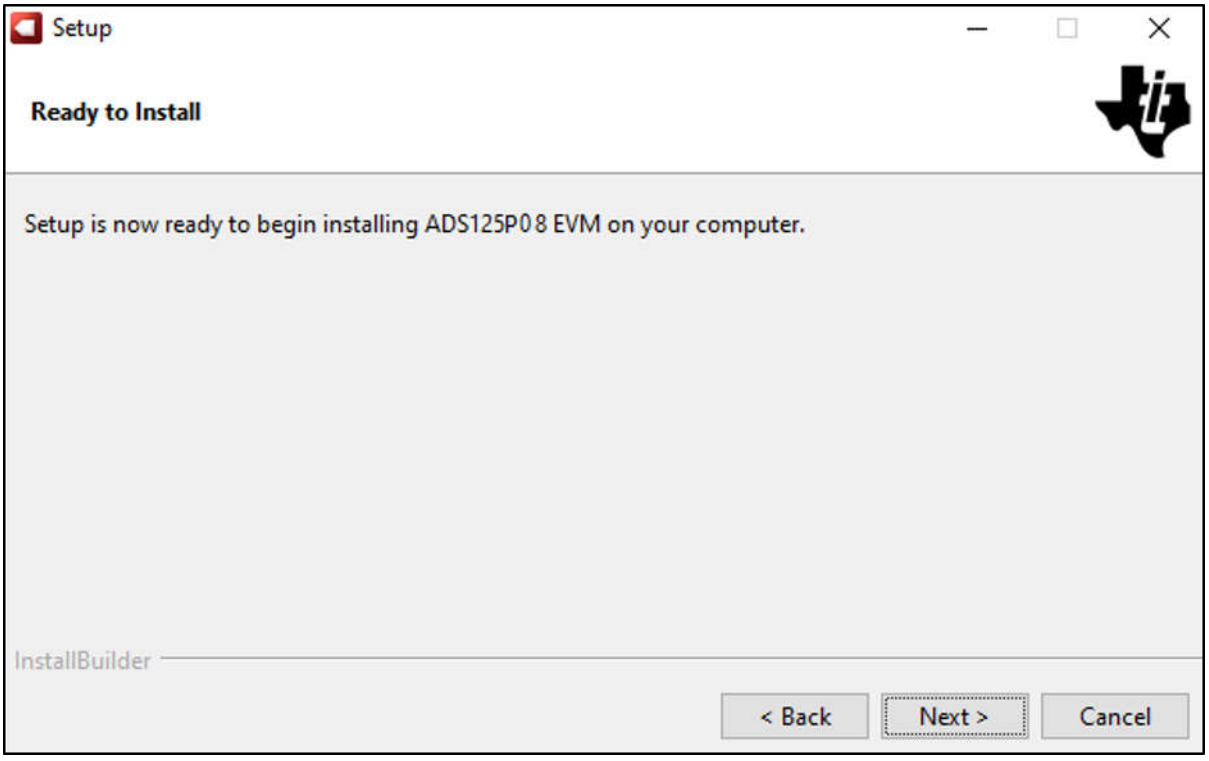


Figure 3-3. ADS125P08 EVM GUI Ready to Install

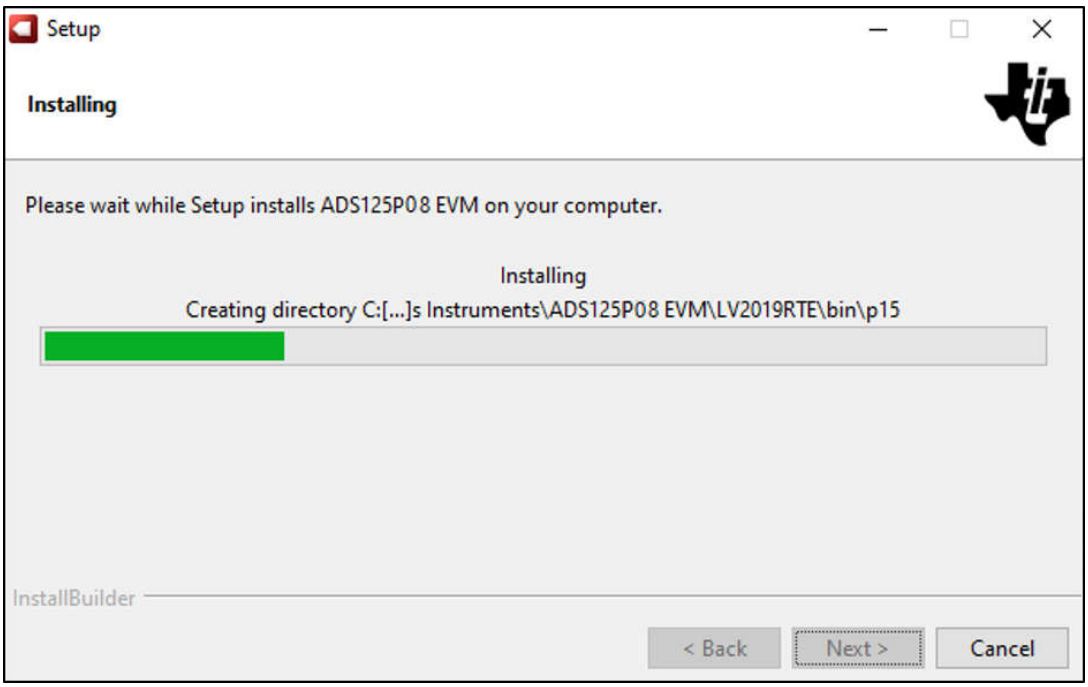


Figure 3-4. ADS125P08 EVM GUI Installing

The ADS125P08 EVM requires the LabVIEW™ run-time engine and can prompt for the installation of this software if not already installed. This prompt occurs during the install process (see Figure 3-4), but is not shown in this document.

Figure 3-5 shows the final prompt after the installation process completes.

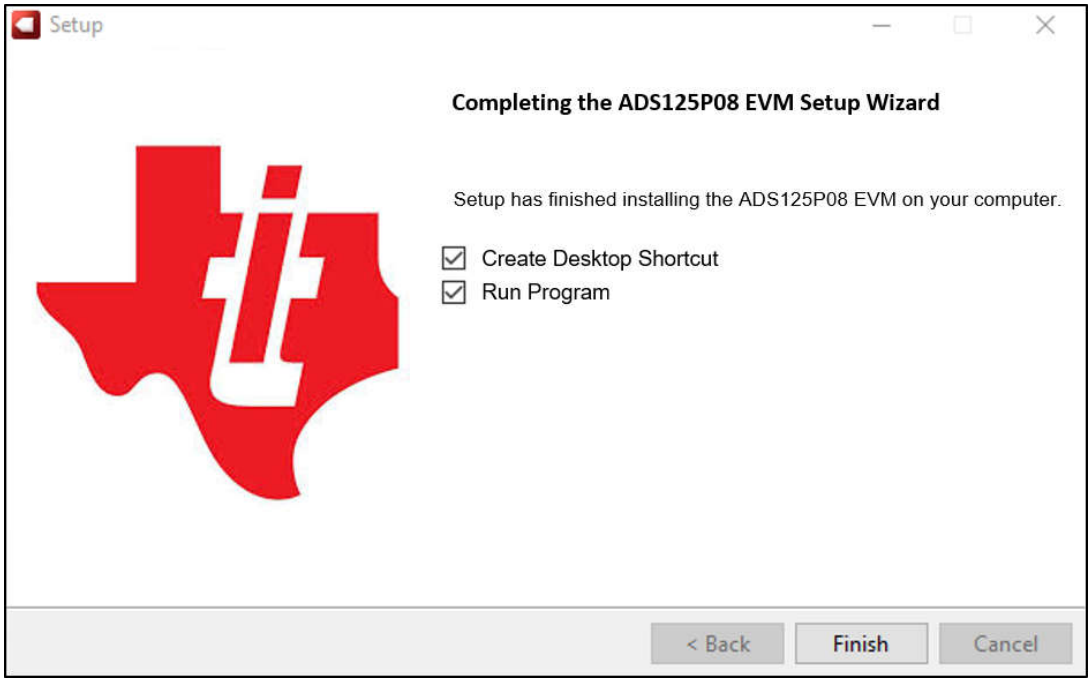


Figure 3-5. ADS125P08 EVM GUI Install Complete

4 Implementation Results

4.1 Hardware Connections

Connect the EVM as shown in Figure 4-1 after installing the software:

1. Physically connect P2 of the PHI to J1 of the ADS125P08 EVM. Install the included screws to provide a robust connection.
2. (Optional) Connect an external Power Supply, Clock, or Voltage Reference, as described in those sections
3. Verify that all shunts are installed on JP1, JP2, and JP3
4. Connect the USB connector on the PHI to the computer
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 4-1 shows the resulting LED indicators
5. Start the software GUI as shown in Figure 4-2. Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This loading takes a few seconds.
6. Connect the signal source to the terminal blocks. Verify that the signal source voltage and current levels meet the specifications listed in Table 1-1.

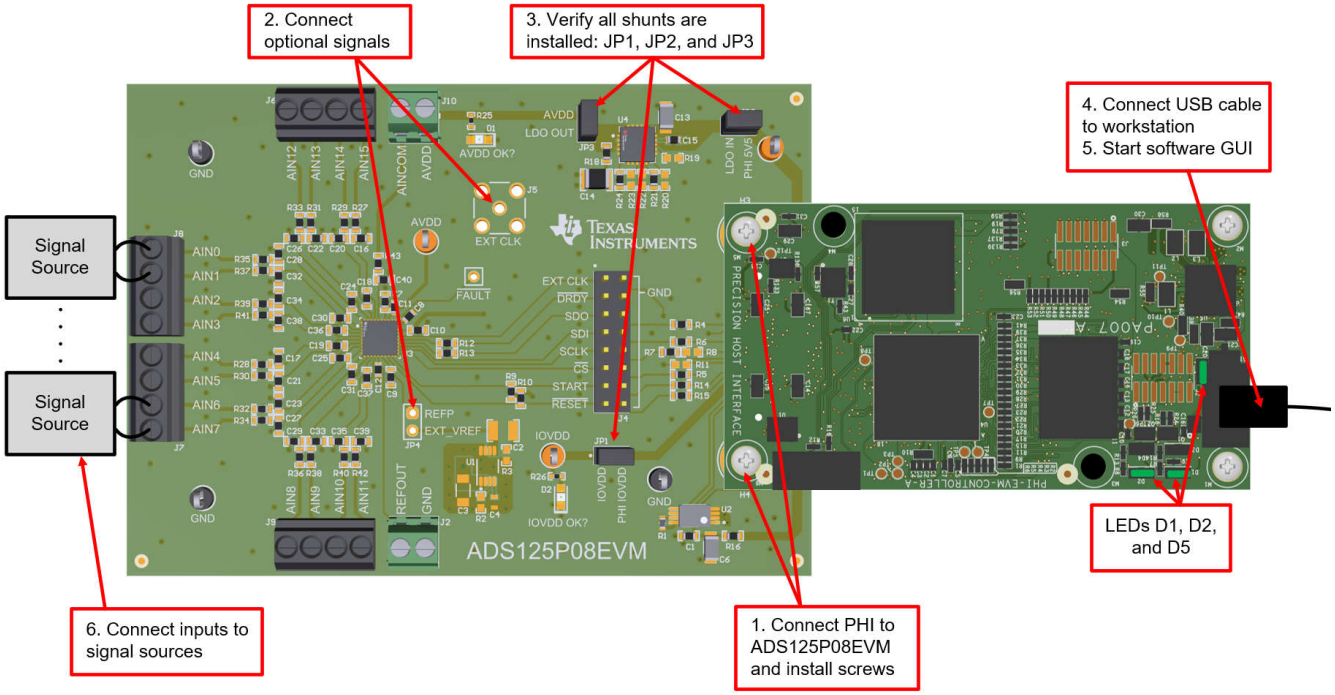


Figure 4-1. Connecting the Hardware to the ADS125P08 EVM

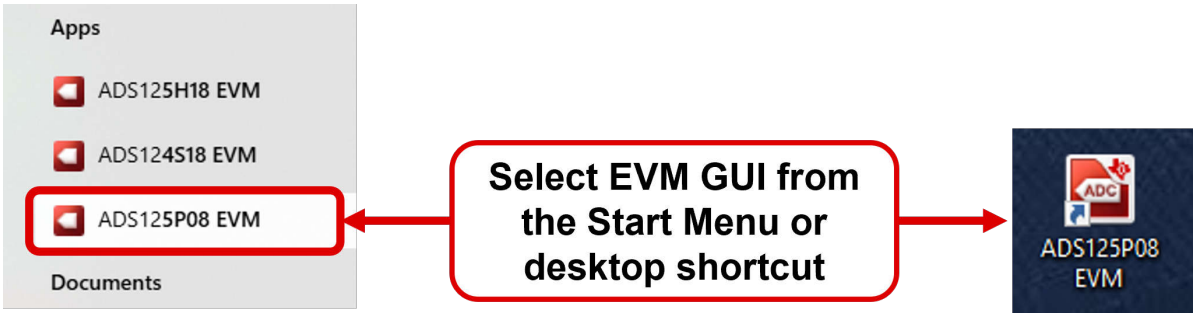


Figure 4-2. Launch the EVM GUI Software

4.2 GUI Operation

The following sections describe the operation and behavior of the ADS125P08 EVM GUI.

4.2.1 ADC Capture Settings and Sequencer Configuration

Figure 4-3 shows how the *Pages* control in the upper-left corner allows access to the other pages in the GUI. Navigate to any of the GUI pages using these controls. Figure 4-3 also shows the *ADC Capture* page. Use this page to easily configure the most important ADC settings, including the General Configuration and Step Configuration parameters, the sequencer mode, and the number of samples or sequences to capture.

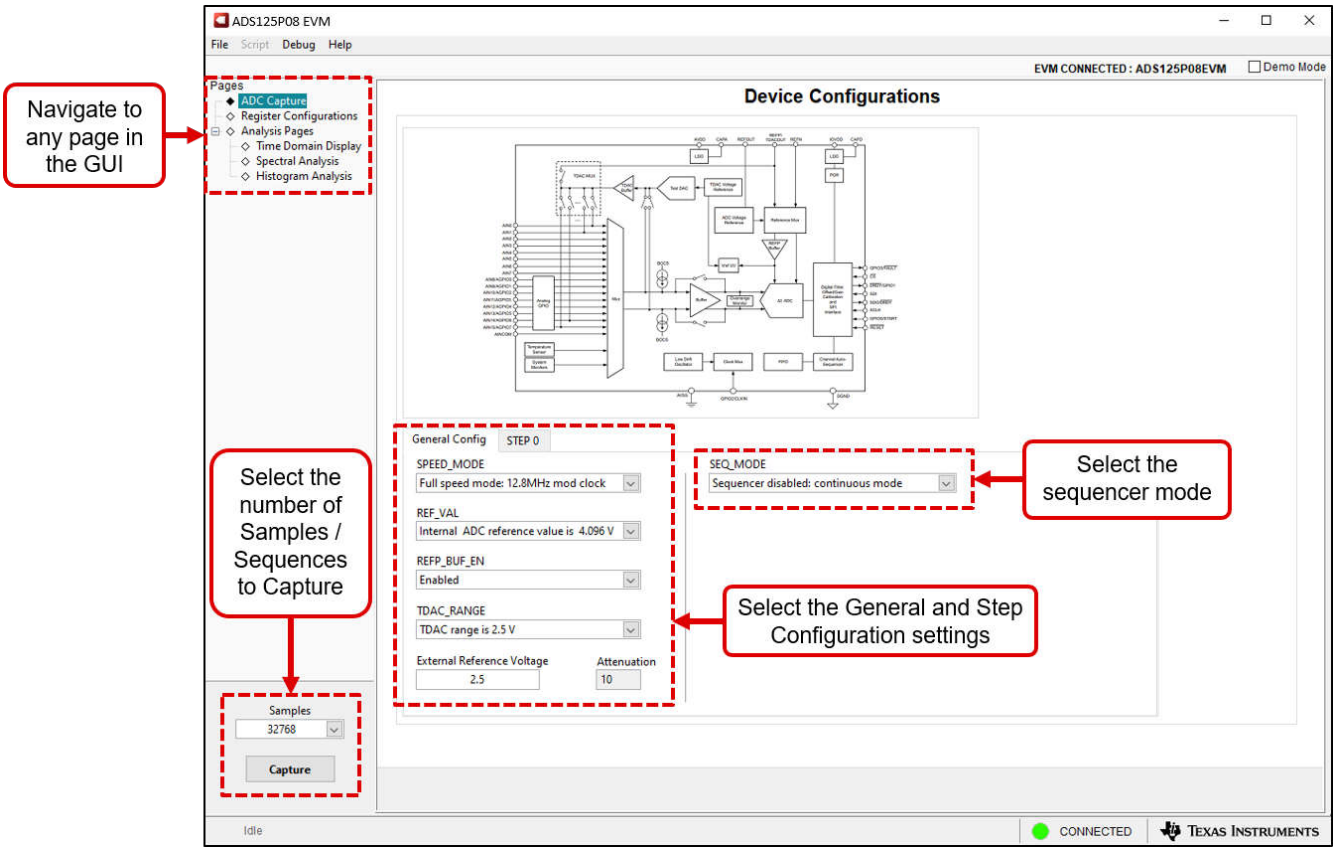


Figure 4-3. ADS125P08 EVM GUI ADC Capture Page - General Configuration

The *General Configuration* tab allows to user to set certain parameters that are used for all steps, including the speed mode, the internal reference voltage, the state of the reference buffer, and the Test DAC range. Additionally, the user can enter the *External Reference Voltage* if applicable. Finally, the ADC Capture page reports the device attenuation by reading the ADC DEVICE_ID register.

The default option in the sequencer mode dropdown in Figure 4-3 allows the user to capture *n* conversions of a single step, where *n* is the number entered in the box in the lower left of the GUI. Alternatively, enable the sequencer to capture *n* complete sequences of all enabled steps.

Figure 4-4 shows the *Step Configuration* tab. Use these controls to configure the settings for each individual step. When the sequencer is disabled, only Step 0 is shown.

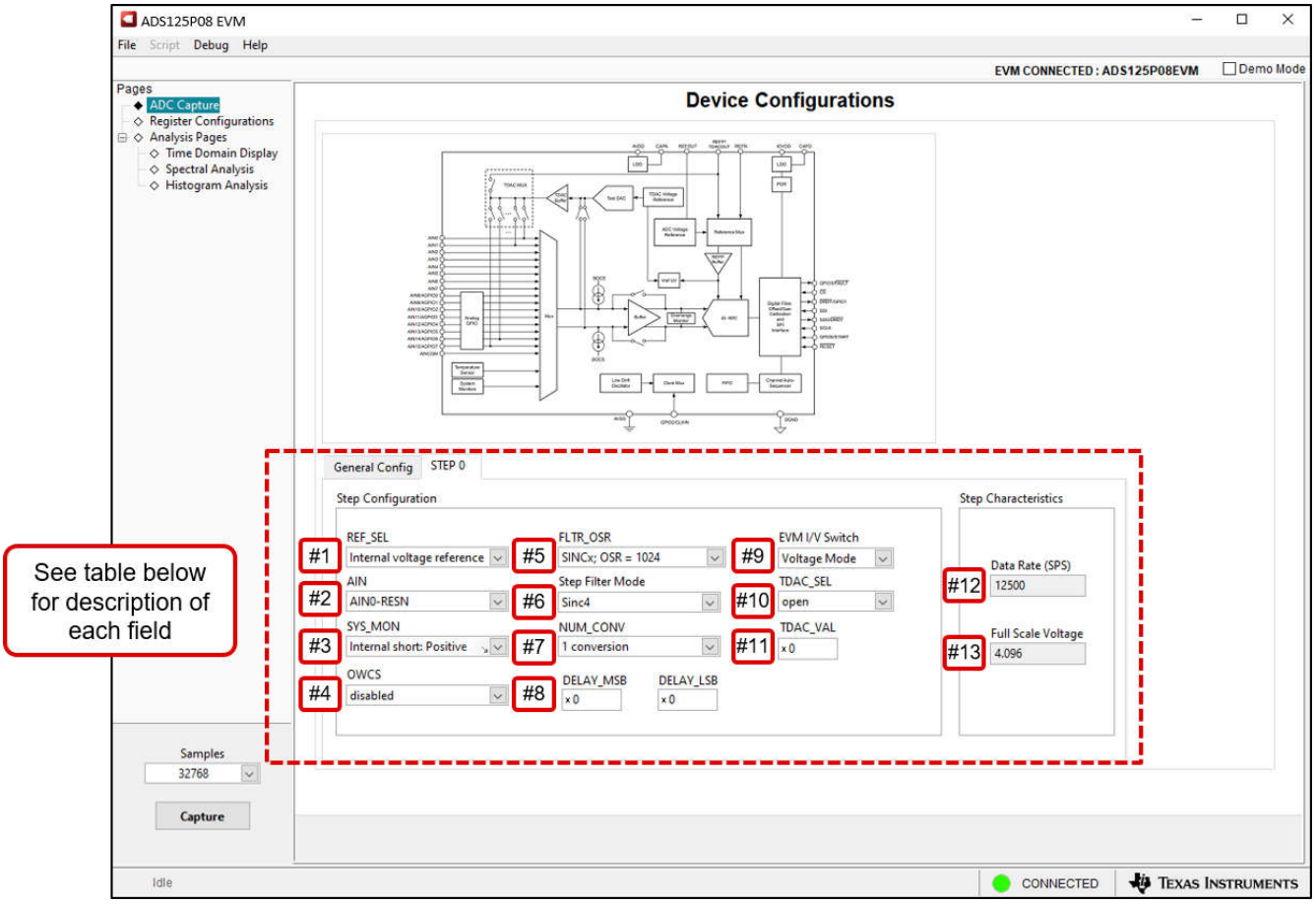


Figure 4-4. ADS125P08 EVM GUI ADC Capture Page - Step Configuration

Table 4-1 explains in more detail each field shown in Figure 4-4:

Table 4-1. Understanding the Step Configuration Page Parameters

ITEM #	PARAMETER	DESCRIPTION
1	REF_SEL	Select the reference voltage source to be used with this step
2	AIN	Select the measurement channel for this step
3	SYS_MON	Select the system monitor option to be measured in this step NOTE: the system monitor takes precedence over the AIN selection (see #2 above), and also uses the internal reference regardless of the selection in REF_SEL
4	OWCS	Enable or disable the open-wire current sources for this step
5	FLTR_OSR	Select the OSR for this step NOTE: the data rate corresponding to this OSR is shown on the right (see #12 below)
6	FLTR_MODE	Select the filter mode for this step
7	NUM_CONV	Enter the number of conversions for this step
8	DELAY	Enter the programmable delay to be used for this step NOTE: the delay value is measured in modulator clock periods (t_{MOD}), is a 16-bit field, and is entered in hex
9	EVM I/V SWITCH	Select the state of the I/V switch on the EVM for this step NOTE: this is a feature of the EVM, not the ADC. These switches are only installed on the EVM on differential channels AIN2/AIN3 and AIN4/AIN5, so this selection only affects those channels
10	TDAC_SEL	Select the location where the Test DAC voltage is output to in this step

Table 4-1. Understanding the Step Configuration Page Parameters (continued)

ITEM #	PARAMETER	DESCRIPTION
11	TDAC_VAL	Enter the value of the Test DAC voltage to be used for this step NOTE: the Test DAC value is a percentage of the reference voltage, is a 5-bit field, and must be entered in hex
12	Data Rate (SPS)	Data rate relative to the selected OSR (see #5 above), the clock frequency, and the clock mode NOTE: the clock mode is selected on the *General Config* tab
13	Full Scale Voltage	Calculates the full-scale voltage (FSV) for this step, where FSV = Reference Voltage * Attenuation NOTE: the reference voltage is set on the *General Config* tab, and the Attenuation factor is determined by reading the DEVICE_ID register

Enable the ADC sequencer by selecting "Sequencer enabled: continuous mode" from the SEQ_MODE dropdown. Multiple step options appear after selecting this configuration. Additionally, the *Capture* parameter changes from "Samples" to "Sequences". As a result, the GUI captures and displays the data for the desired number of sequences defined by the user. Figure 4-5 shows how the GUI changes after enabling the sequencer.

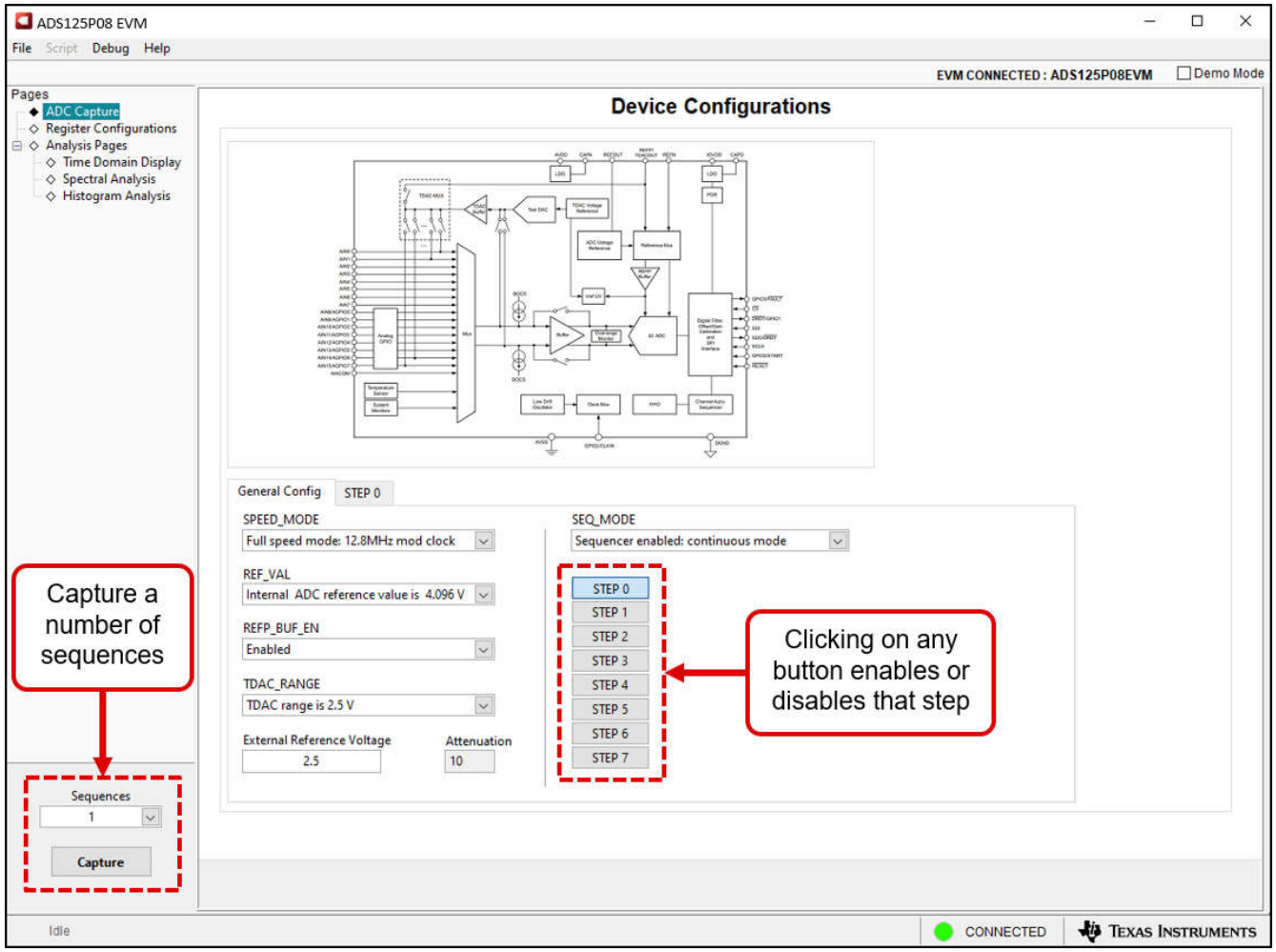


Figure 4-5. ADS125P08 EVM GUI ADC Capture Page - Enable Sequencer

After enabling the sequencer, Figure 4-6 shows how clicking on each individual step opens up a new *Step* tab. Clicking on the same step again closes that step tab. This is true for all steps except Step 0, which cannot be disabled.

Configure each enabled step as shown in Figure 4-4 and described in Table 4-1.

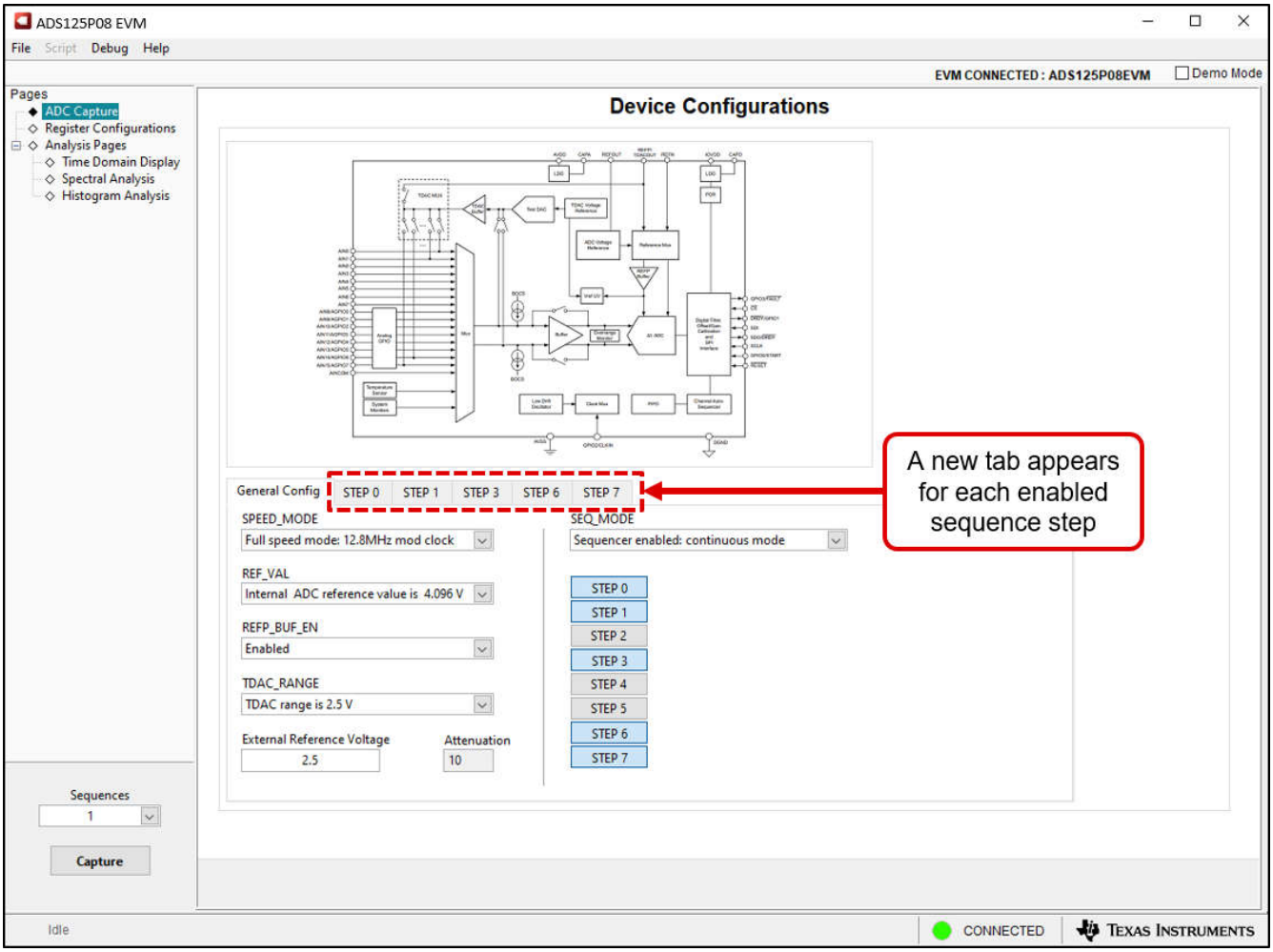


Figure 4-6. ADS125P08 EVM GUI ADC Capture Page - Enabling Multiple Sequence Steps

4.2.2 EVM Register Settings

Figure 4-7 shows a portion of the ADS125P08 register map. The registers can be used to configure any ADC register to change functions such as the data rate, setup the channel sequencer, or enable integrated features. Change the register settings by clicking on each bit, typing a value directly into the *Value* column, or by selecting from the drop-down menus in the *Field View* control.

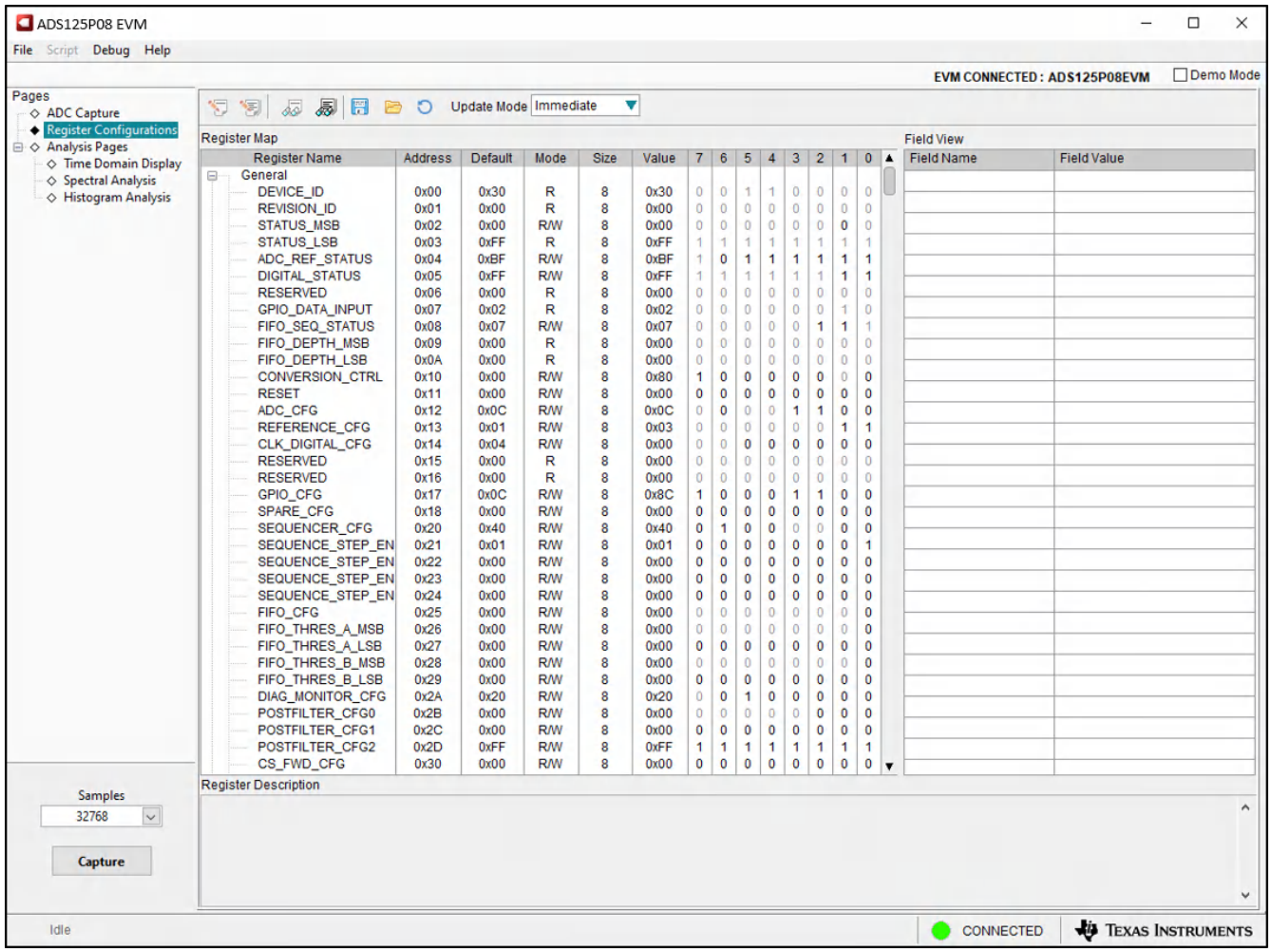


Figure 4-7. ADS125P08 EVM GUI Navigation and Register Map

Figure 4-8 shows a consolidated view of the entire ADS125P08 register map, which includes the General page as well as all 32 Step pages. Navigate to a specific register within a specific step using the scroll bar between the *Register Map* and *Field View* sections.

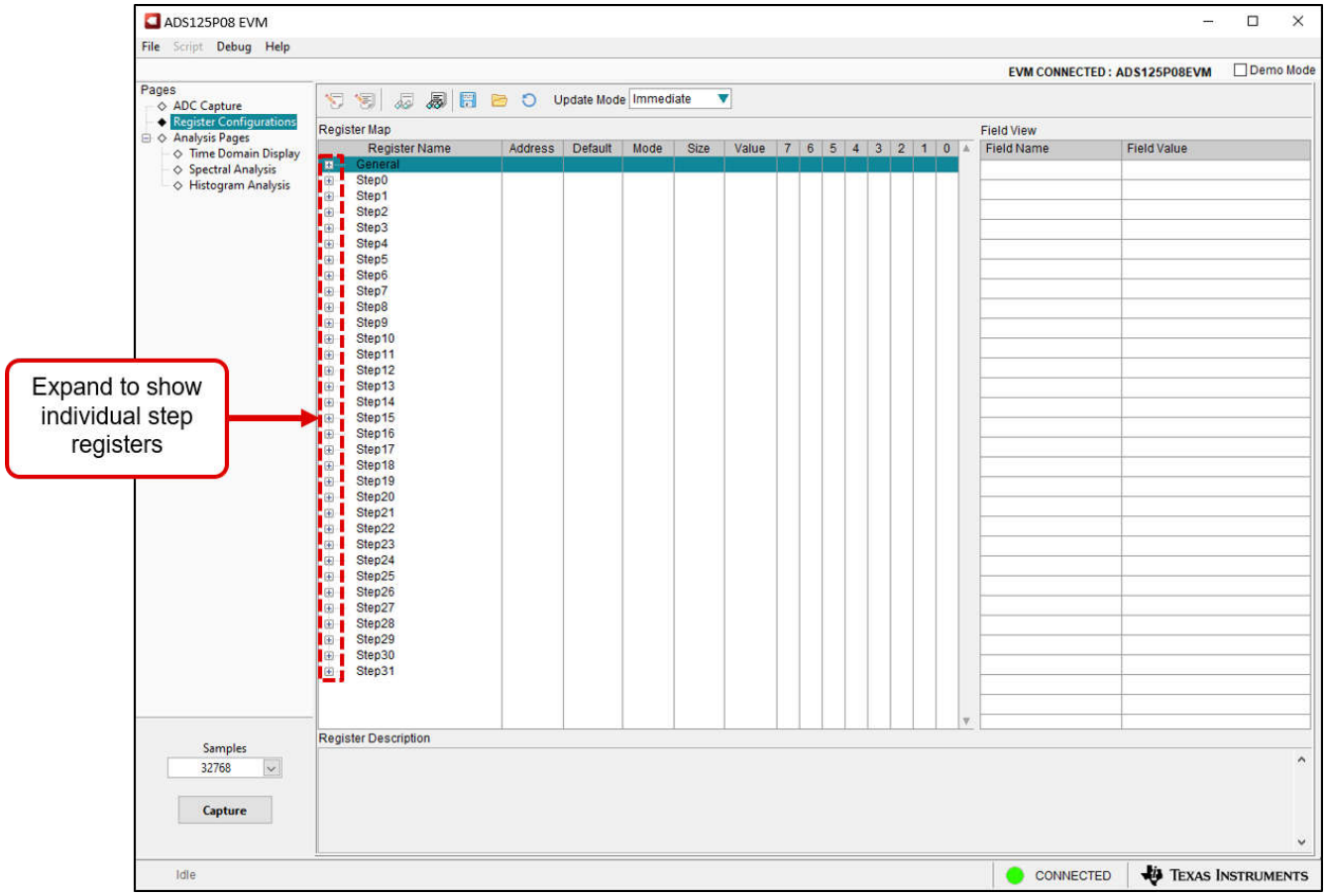


Figure 4-8. ADS125P08 EVM GUI Register Configurations Page - All Steps

4.2.3 Time-Domain Display

The time-domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for studying the behavior of and debugging any gross problems with the ADC or drive circuits. Trigger a data capture of the selected number of samples from the ADS125P08 EVM by using the *Capture* button in Figure 4-9. The time-domain plot has *Time* on the x-axis and by default shows the corresponding *Voltage* on the y-axis relative to the specified reference voltage.

The *Measurements* control on the bottom of Figure 4-9 calculates the code range, the mean code, and the code standard deviation. Switching pages to any of the *Analysis* tools described in the subsequent sections causes calculations to be performed on the same set of data.

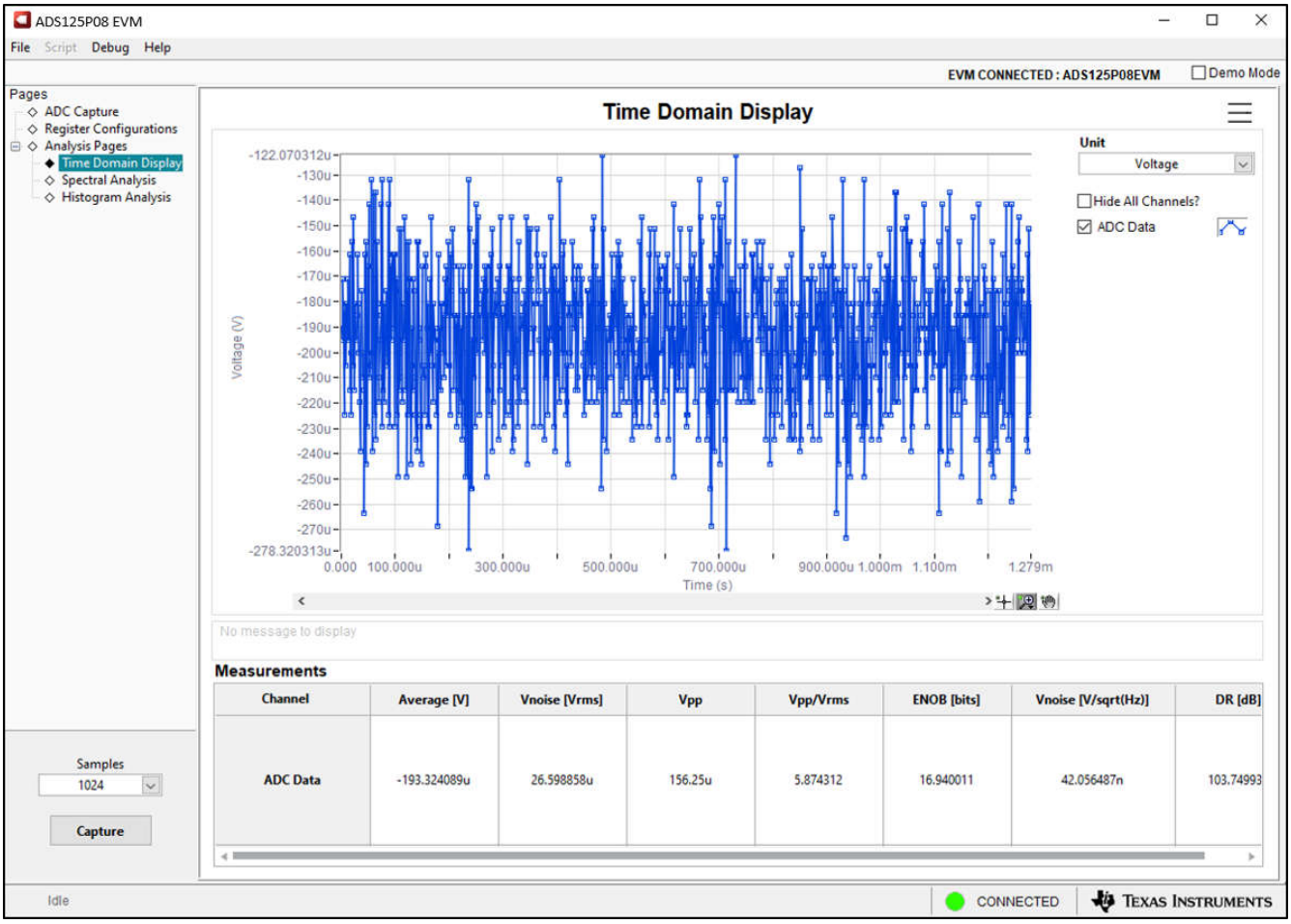


Figure 4-9. ADS125P08 EVM GUI Time-Domain Display Page

4.2.4 Frequency-Domain Display

Figure 4-10 shows the spectral analysis tool that evaluates the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS125P08. This dynamic performance is calculated by single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

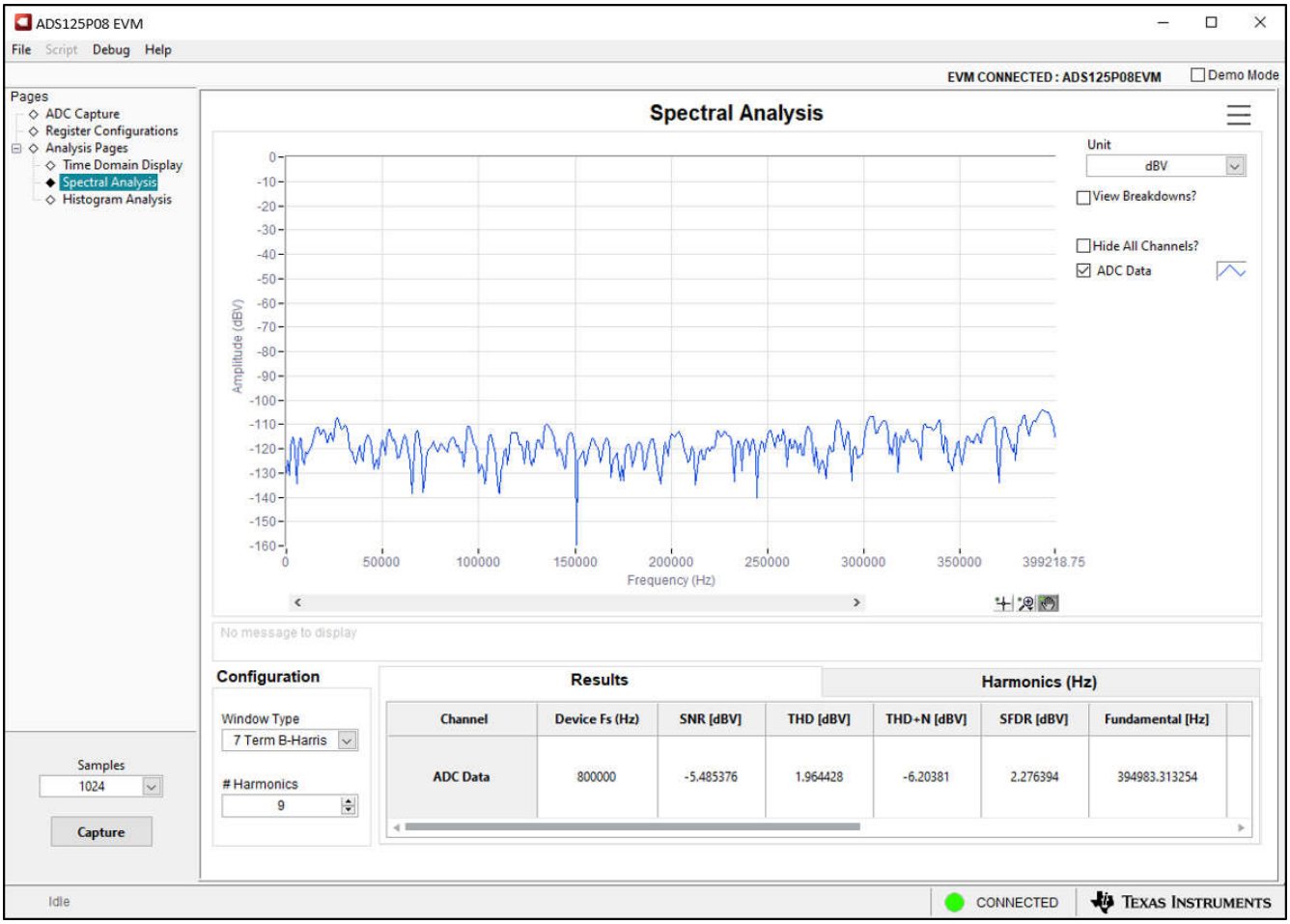


Figure 4-10. ADS125P08 EVM GUI Frequency-Domain Display Page

4.2.5 Histogram Display

Noise degrades ADC resolution and the histogram tool shown in Figure 4-11 can be used to estimate effective resolution. Effective resolution is a metric describing the ADC resolution loss resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

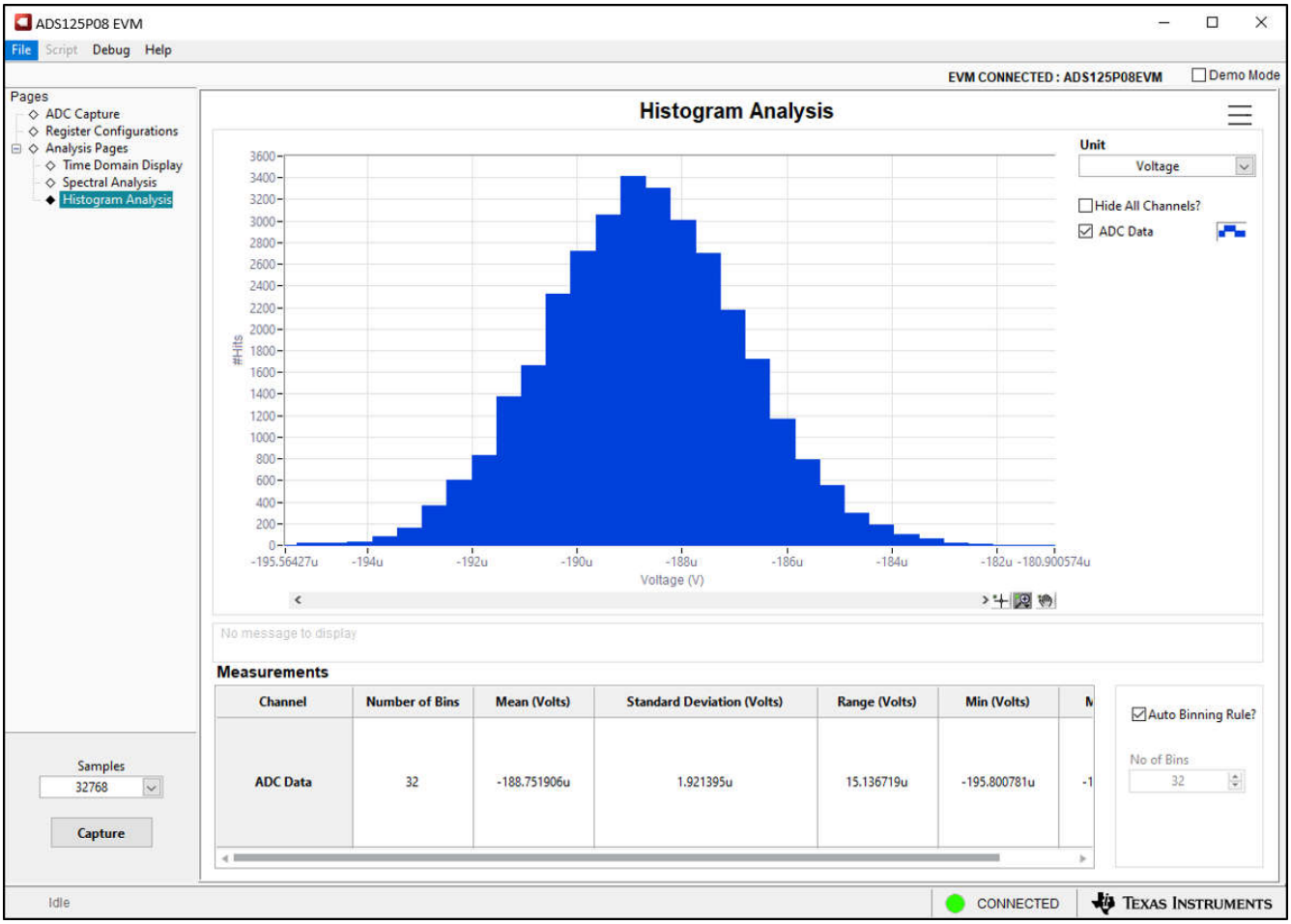


Figure 4-11. ADS125P08 EVM GUI Histogram Display Page

5 Hardware Design Files

This section contains the ADS125P08 EVM schematics, PCB layout, and bill of materials (BOM)

5.1 Schematics

Figure 5-1 to Figure 5-4 show the complete ADS125P08 EVM schematic.

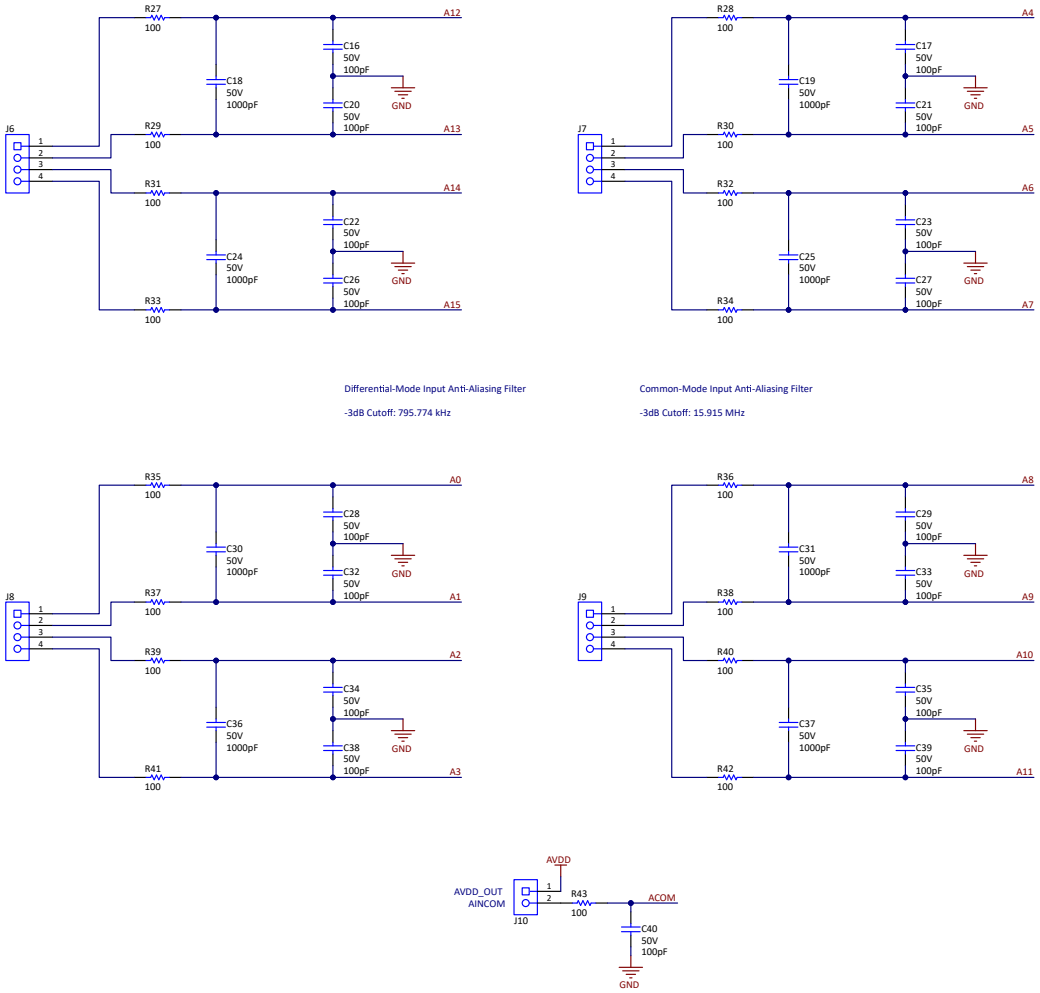


Figure 5-1. EVM Analog Inputs

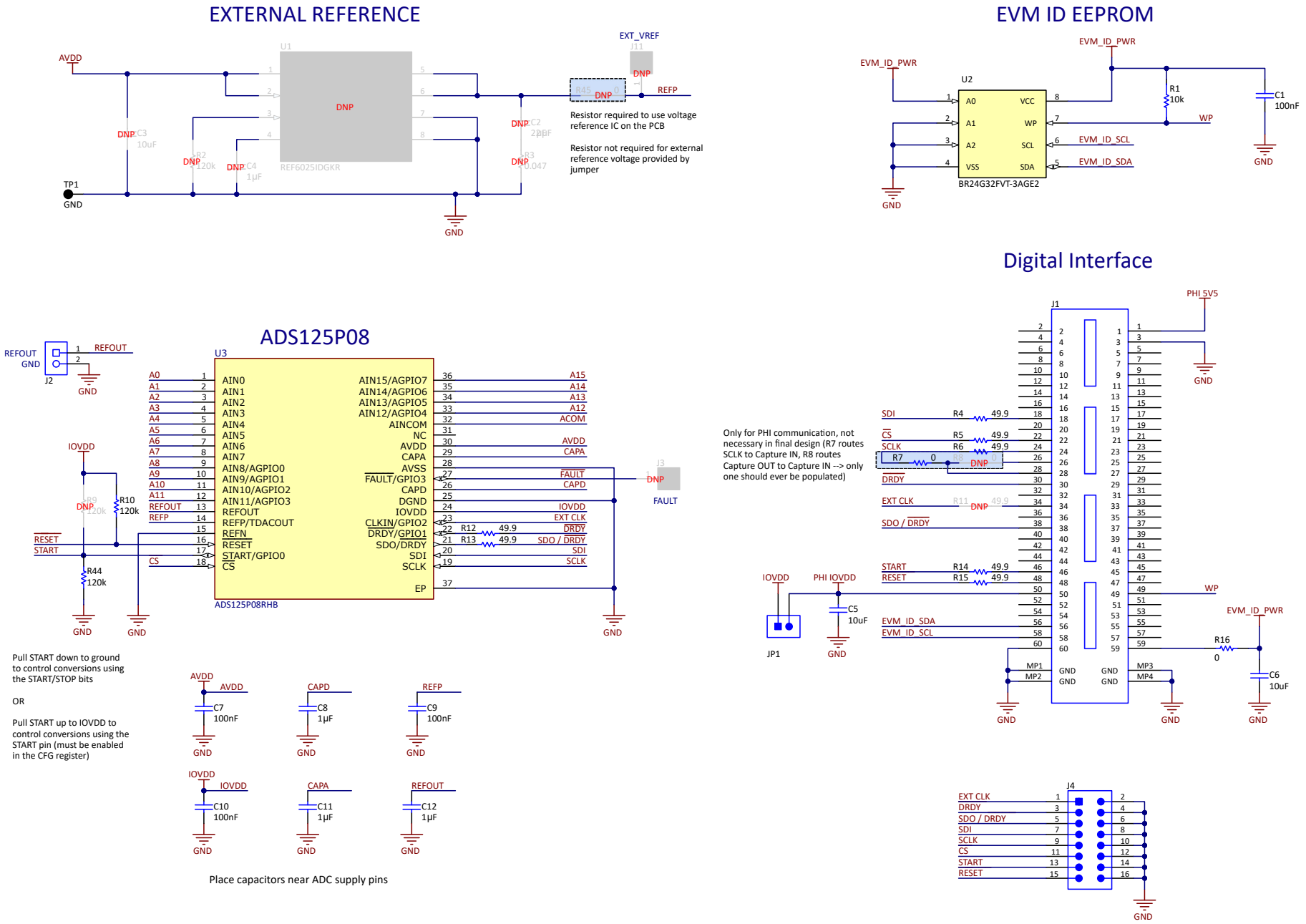


Figure 5-2. EVM ADC, Voltage Reference, and Digital Communication Schematic

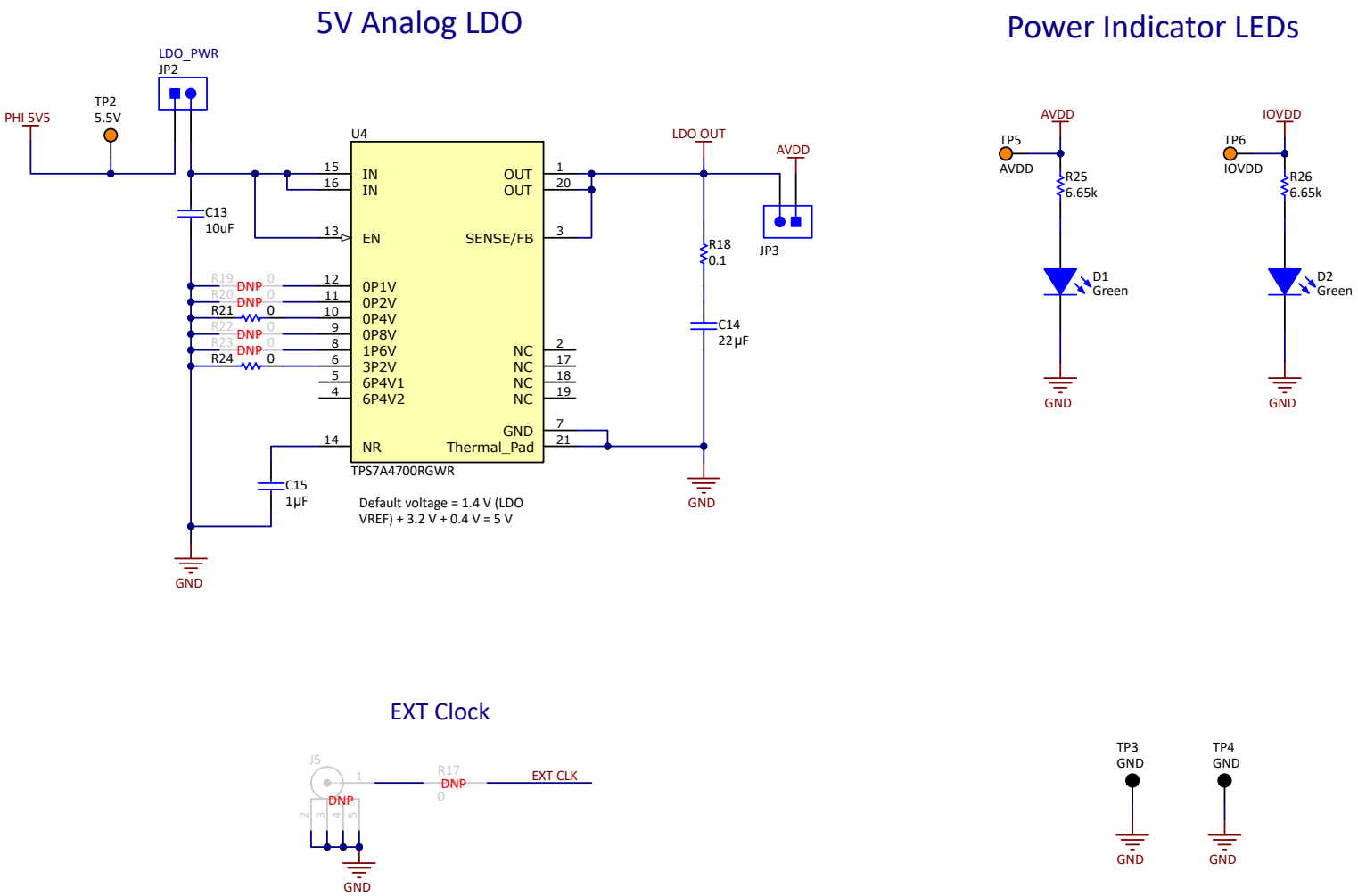
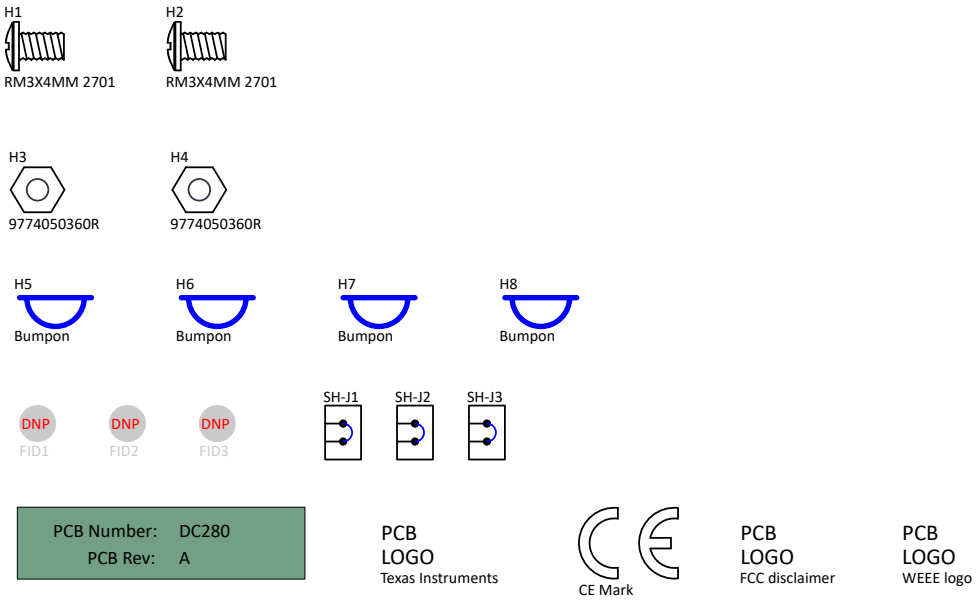


Figure 5-3. EVM Power and External Clock Schematic



ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ4
Assembly Note
Place H1 and H2 screws in H3 and H4 standoffs

ZZ5
Assembly Note
Place SH-J1 on JP1, pins 1-2 : Place SH-J2 on JP2, pins 1-2 : Place SH-J3 on JP3, pins 1-2

Figure 5-4. EVM Hardware

5.2 PCB Layouts

Figure 5-5 to Figure 5-8 show the layout drawings for all ADS125P08 EVM PCB layers

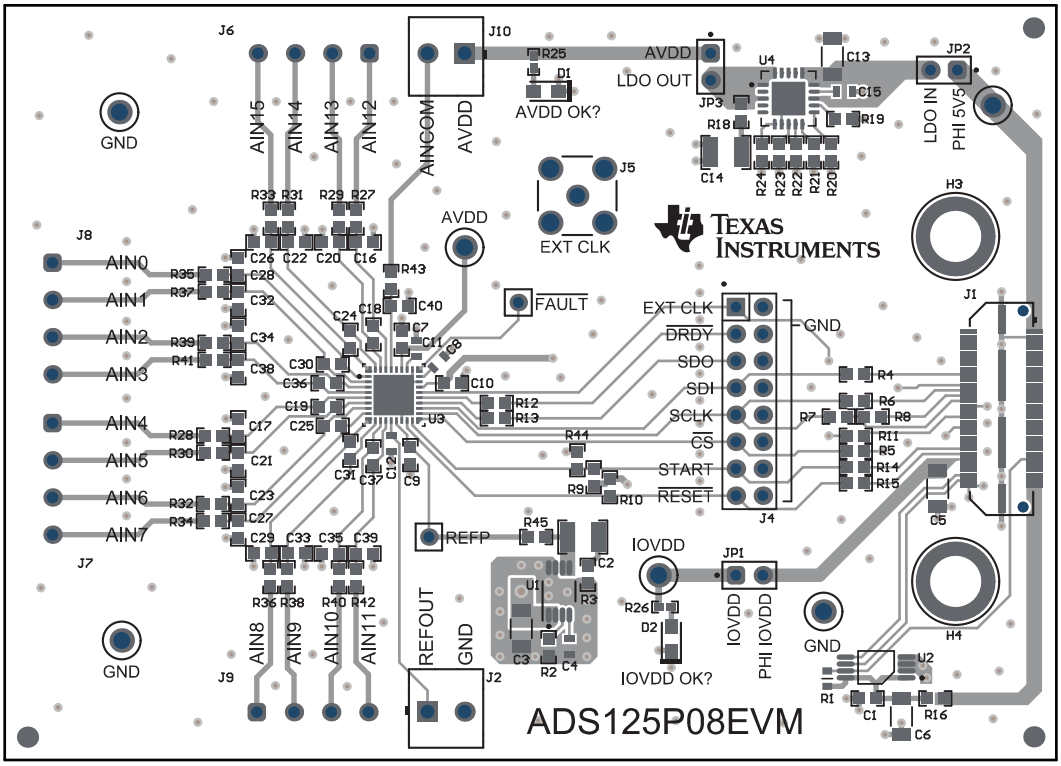


Figure 5-5. ADS125P08 EVM PCB Layout - Top Layer

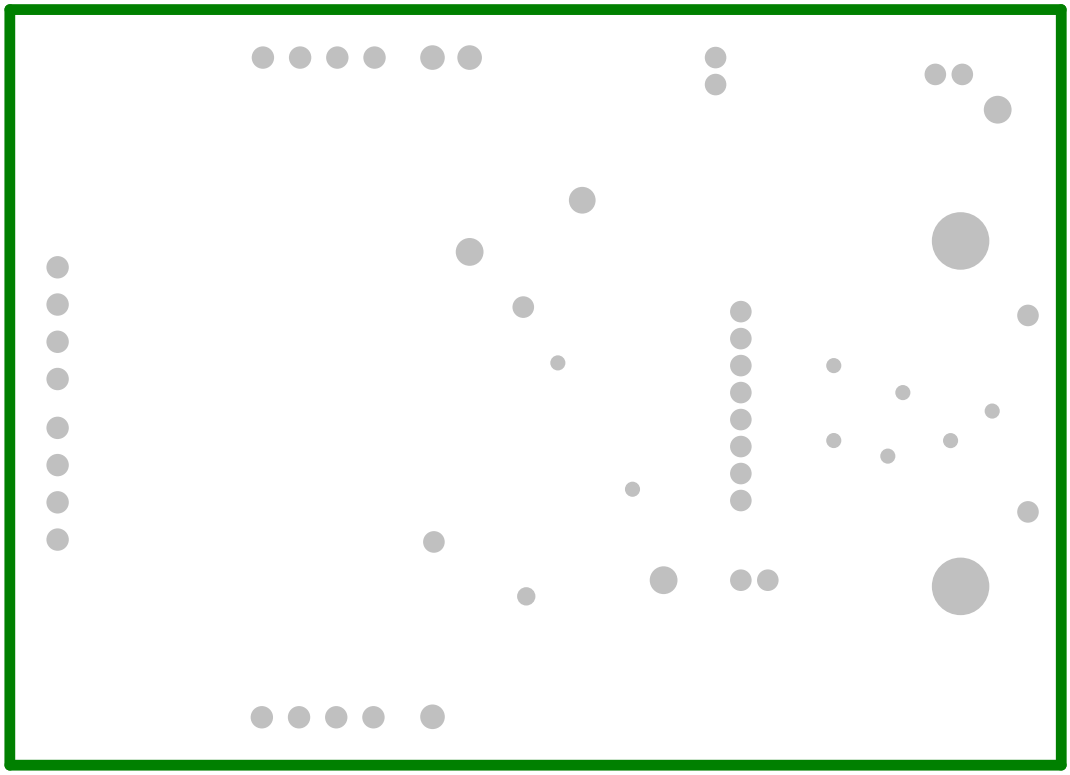


Figure 5-6. ADS125P08 EVM PCB Layout - Ground Layer 1

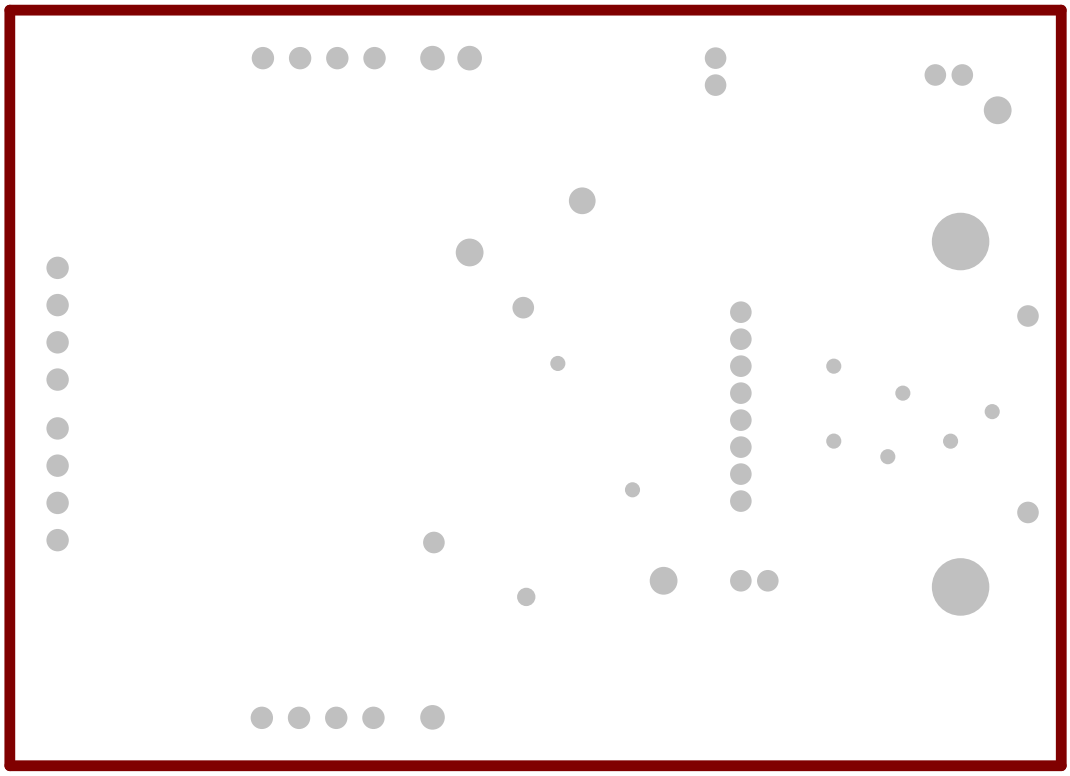


Figure 5-7. ADS125P08 EVM PCB Layout - Ground Layer 2

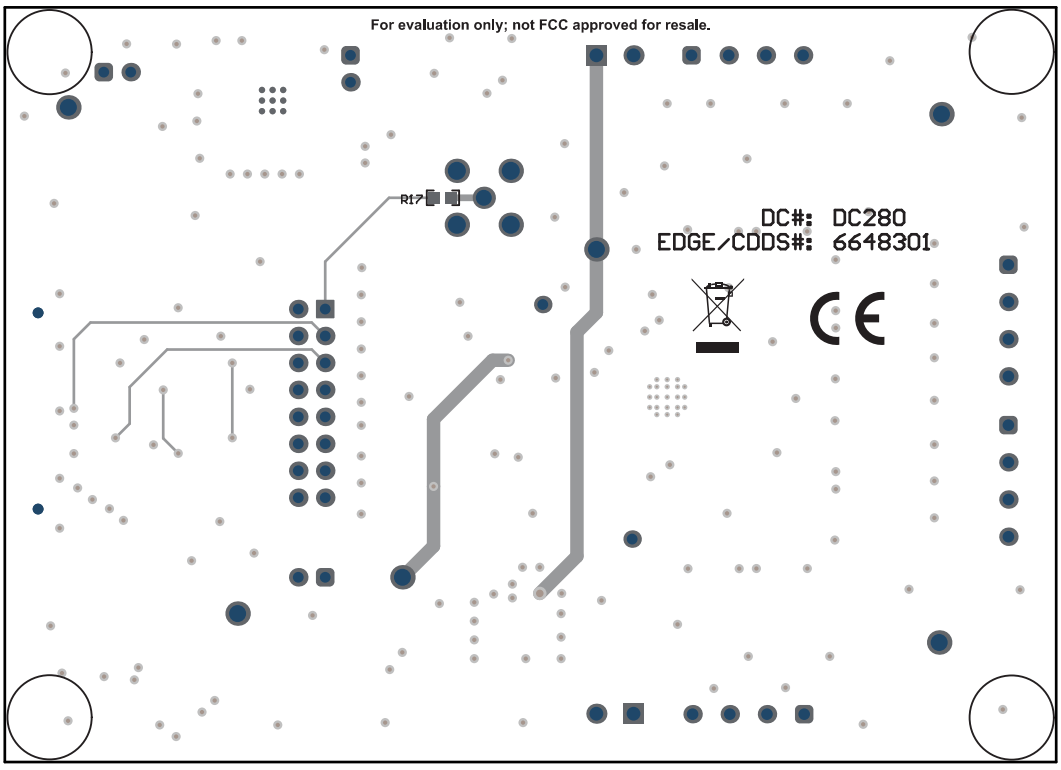


Figure 5-8. ADS125P08 EVM PCB Layout - Bottom Layer

5.3 Bill of Materials (BOM)

Table 5-1 lists the ADS125P08 EVM bill of materials

Table 5-1. ADS125P08 EVM BOM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C7, C9, C10	4	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
C5, C6, C13	3	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C8, C11, C12, C15	4	1uF	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105K080AC	TDK
C14	1	22uF	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C16, C17, C20, C21, C22, C23, C26, C27, C28, C29, C32, C33, C34, C35, C38, C39, C40	17	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	C0603C101J5GACTU	Kemet
C18, C19, C24, C25, C30, C31, C36, C37	8	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	C0603C102J5GACTU	Kemet
D1, D2	2	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H5, H6, H7, H8	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J2, J10	2		Terminal Block, 3.5mm, 2x1, Tin, TH	Receptacle, 3.5mm, 2x1, TH	6.91214E+11	Wurth Elektronik
J4	1		Header, 100mil, 8x2, Gold, TH	8x2 Header	TSW-108-07-G-D	Samtec
J6, J7, J8, J9	4		Terminal Block, 3.5mm, 4x1, Tin, TH	Terminal Block, 3.5mm, 4x1, TH	393570004	Molex
JP1, JP2, JP3	3		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
R1	1	10k	Res Thin Film 0603 10K Ohm 0.1% 1/10W ±10ppm/°C Molded SMD SMD Punched Carrier T/R	603	ERA-3ARB103V	Panasonic
R4, R5, R6, R12, R13, R14, R15	7	49.9	RES, 49.9, 0.5%, 0.1 W, 0603	603	RT0603DRE0749R9L	Yageo America

Table 5-1. ADS125P08 EVM BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R7, R16, R21, R24	4	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic
R10, R44	2	120k	RES, 120 k, 0.1%, 0.1 W, 0603	603	RG1608P-124-B-T5	Susumu Co Ltd
R18	1	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	603	ERJ-L03KF10CV	Panasonic
R25, R26	2	6.65k	RES, 6.65 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04026K65FKED	Vishay-Dale
R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43	17	100	RES, 100, 0.1%, 0.1 W, 0603	603	RG1608P-101-B-T5	Susumu Co Ltd
SH-J1, SH-J2, SH-J3	3	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP3, TP4	3		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone Electronics
TP2, TP5, TP6	3		Test Point, Multipurpose, Orange, TH	Orange Multipurpose Testpoint	5013	Keystone Electronics
U2	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U3	1		ADS125P08IRHBR	VQFN36	ADS125P08IRHBR	Texas Instruments
U4	1		36-V, 1-A, 4.17-µVRMS, RF low-dropout (LDO) voltage regulator 20-VQFN -40 to 125	VQFN20	TPS7A4700RGWR	Texas Instruments
C2	0	22uF	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C3	0	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C4	0	1uF	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105K080AC	TDK
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J3, J11	0		Header, 100mil, 1x1, Gold, TH	Header, 1x1, 2.54mm, TH	HTSW-101-09-G-S	Samtec
J5	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF
R2, R9	0	120k	RES, 120 k, 0.1%, 0.1 W, 0603	603	RG1608P-124-B-T5	Susumu Co Ltd
R3	0	0.047	RES, 0.047, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	603	ERJ-L03KF47MV	Panasonic
R8, R17, R19, R20, R22, R23, R45	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic

Table 5-1. ADS125P08 EVM BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R11	0	49.9	RES, 49.9, 0.5%, 0.1 W, 0603	603	RT0603DRE0749R9L	Yageo America
U1	0		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6025IDGKR	Texas Instruments

6 Additional Information

6.1 Trademarks

LabVIEW™ is a trademark of National Instruments Inc.
Microsoft® and Windows® are registered trademarks of Microsoft Corporation.
All trademarks are the property of their respective owners.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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