Analog Engineer's Circuit

Dual-Supply, Discrete, Programmable Gain Amplifier Circuit

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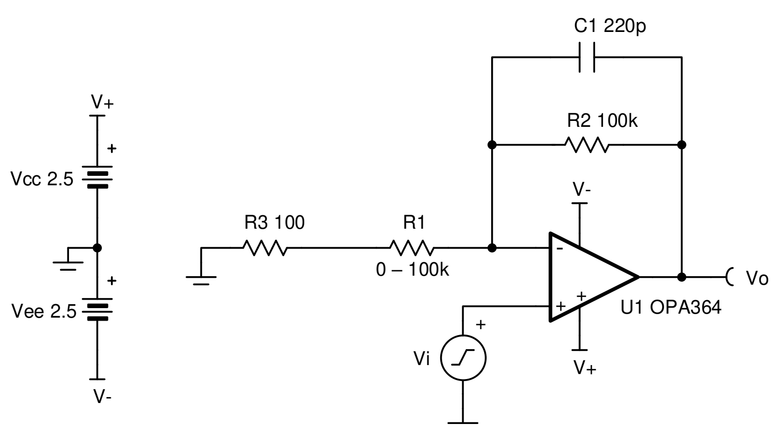
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–1.25V	+1.25V	–2.4V	+2.4V	+2.5V	–2.5V

Gain	Cutoff Frequency
6dB (2V/V) to 60dB (1000V/V)	7kHz

Design Description

This circuit provides programmable, non-inverting gains ranging from 6dB (2V/V) to 60dB (1000V/V) using a variable input resistance. The design maintains the same cutoff frequency over the gain range.



Design Notes

1. Choose a digital potentiometer, such as TPL0102 for R_1 to design a low-cost digital programmable gain amplifier.
2. R_3 sets the maximum gain when R_1 approaches 0 Ω.
3. A feedback capacitor limits the bandwidth and prevent stability issues.
4. Evaluate stability across the selected gain range. The minimum gain setting is likely the most sensitive to stability issues.
5. Some digital potentiometers can vary in absolute value by as much as ±20% so gain calibration may be necessary.

Design Steps

1. Choose R_2 and R_3, to set the maximum gain when R_1 approaches 0:

$$G_{max} = 1 + \frac{R_2}{R_3}$$
$$G_{max} - 1 = \frac{R_2}{R_3} \rightarrow R_2 = \left(G_{max} - 1\right) \times R_3$$
$$\text{Set} \quad R_3 = 100\ \Omega$$
$$R_2 = \left(1000\ \frac{V}{V} - 1\right) \times 100 = 99\ k\Omega \rightarrow R_2 = 100\ k\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$

2. Choose the potentiometer maximum value to set the minimum gain:

$$G_{min} = 1 + \frac{R_2}{R_{1,\,max} + R_3}$$
$$G_{min} - 1 = \frac{R_2}{R_{1,\,max} + R_3}$$
$$R_{1,\,max} + R_3 = \frac{R_2}{G_{min} - 1}$$
$$R_{1,\,max} = \frac{R_2}{G_{min} - 1} - R_3 = \frac{100k\Omega}{2 - 1} - 100\Omega = 99.9k\Omega \rightarrow R_{1,\,max} = 100k\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$
$$R_{1,\,min} = 0\Omega \quad \left(\text{Wiper} \quad \text{resistance,} \quad \text{typically} \quad 25\Omega, \quad \text{will} \quad \text{introduce} \quad \text{some} \quad \text{error}\right)$$

3. Choose the bandwidth with a feedback capacitor:

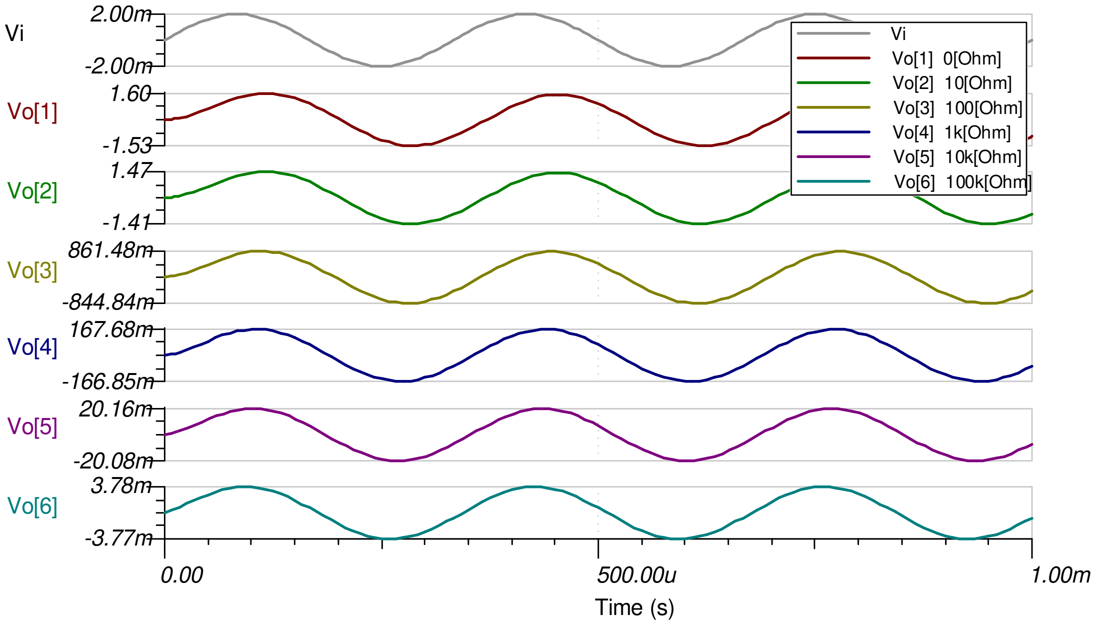
$$f_c = \frac{GBW}{G_{max}} = \frac{7MHz}{1000\frac{V}{V}} = 7kHz$$
$$f_c = 7kHz \rightarrow C_1 = \frac{1}{2\pi \times R_2 \times f_c} = 227pF \quad \rightarrow C_1 = 220pF \quad \left(\text{Standard} \quad \text{Value}\right)$$

4. Check for stability at minimum gain (2V/V), which is when R_1=100kΩ. To satisfy the requirement f_c (circuit bandwidth) must be less than f_{zero} (zero created by the resistive feedback network and the differential and common-mode input capacitances).

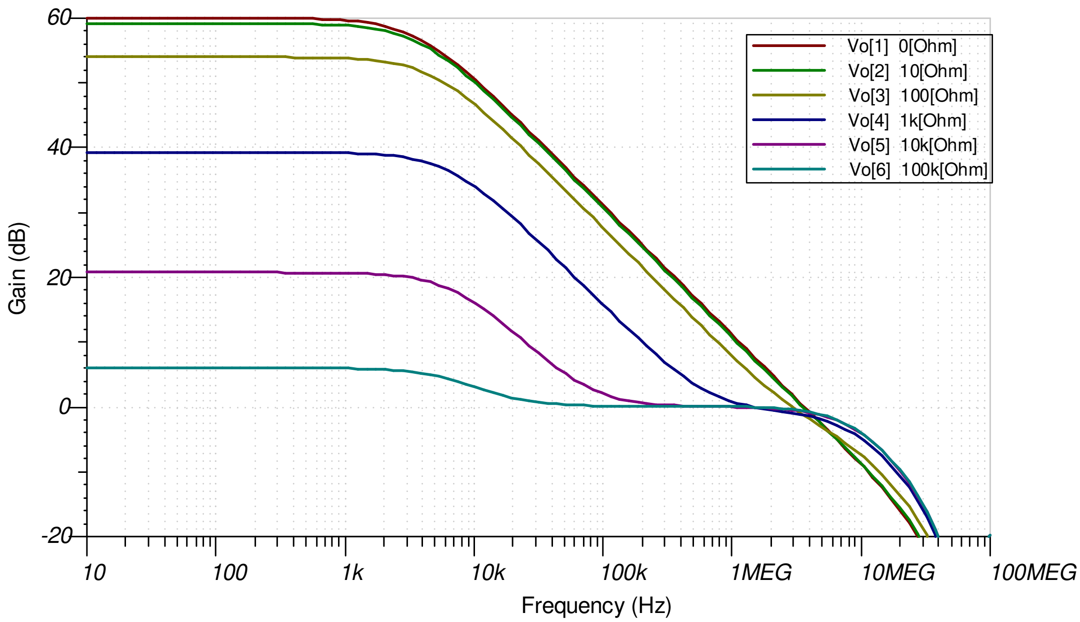
$$f_c = \frac{1}{2\pi \times C_1 \times R_2} = 7\ kHz$$
$$f_{zero} = \frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_2 \parallel R_1)} = \frac{1}{2 \times \pi \times \left(3\ pF + 2\ pF\right) \times \left(\frac{100\ k\Omega \times 100\ k\Omega}{100\ k\Omega + 100\ k\Omega}\right)}$$
$$f_{zero} = 637\ kHz$$
$$7\ kHz < 637\ kHz \rightarrow f_c < f_{zero}$$

Design Simulations

Transient Simulation Results



AC Simulation Results



References:

1. Texas Instruments, Simulation for Discrete Programmable Gain Amplifier Circuit, product page
2. Texas Instruments, Low-Cost Digitally Programmable Gain Amplifier Reference Design, product page

Design Featured Op Amp

OPA364	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	1.1mA
I_b	1pA
UGBW	7MHz
SR	5V/µs
#Channels	1, 2, and 4
OPA364	

Design Alternate Op Amp

OPA376	
V_{ss}	2.2V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	760µA
I_b	0.2pA
UGBW	5.5MHz
SR	2V/µs
#Channels	1, 2, and 4
OPA376	

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