Analog Engineer's Circuit

Output Overvoltage Protection Circuit for Voltage DACs Without an External Feedback Pin

Precision DAC: Factory Automation and Control

Joseph Wu and Art Kay

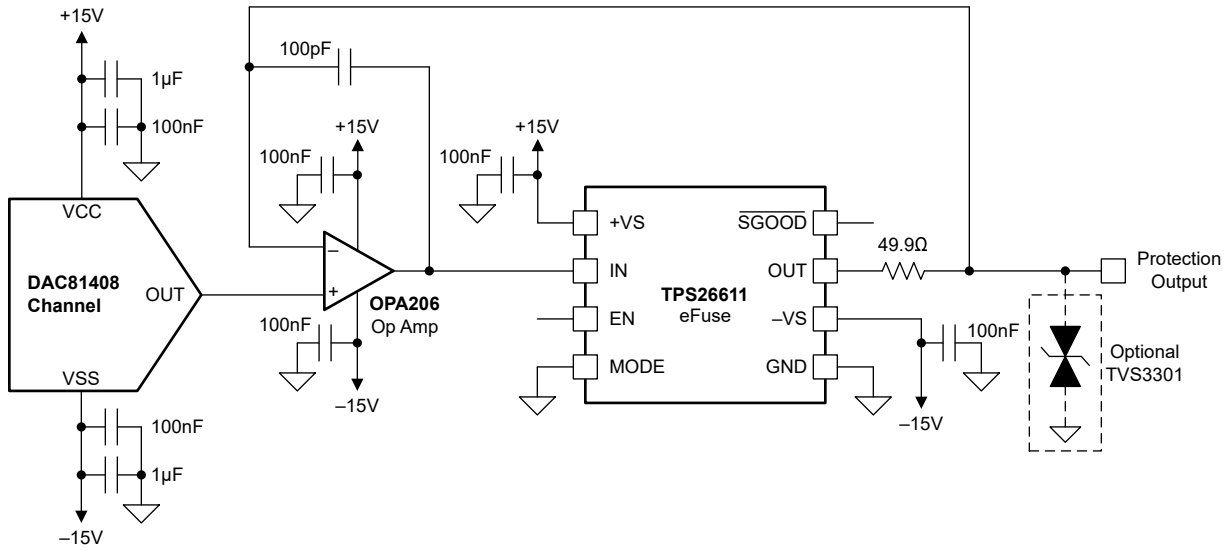
Design Objective

Key Input Parameter	Key Output Signal	Recommended Devices
SPI or I^2C communication to control DAC voltage output	±10V output DAC signal with overvoltage protection	DAC81408, OPA206, TPS26611, TVS3301 (optional)

Objective: Protection of a ±10V signal from a sustained ±32V connection for a digital-to-analog converter (DAC) that does not have a positive sense pin.

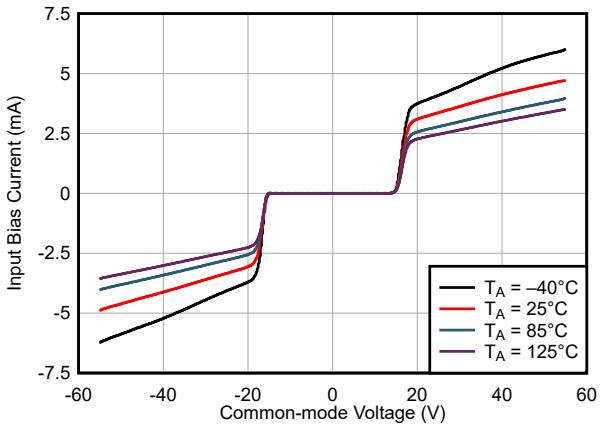
Design Description

This circuit design describes an overvoltage protection circuit for a precision DAC output. This circuit protects the DAC output from a continuous overvoltage above the maximum and below the minimum supply voltages. In a device without a positive sense pin, the DAC output buffer is contained within the device, without pin access to the positive sense feedback pin of the output buffer. The overvoltage protection circuit consists of an op amp set up in unity gain, an eFuse to protect the output, and an optional transient-voltage-suppression (TVS) diode. For a DAC operating on ±15V, the output is protected to ±32V or greater without damaging the DAC and the protection circuit. This type of protective circuit buffer can be used in many industrial factory automation and control applications. This circuit is particularly useful if the output experiences an overvoltage event from miswiring at an output terminal such as in a Programmable Logic Controller (PLC).



Design Notes

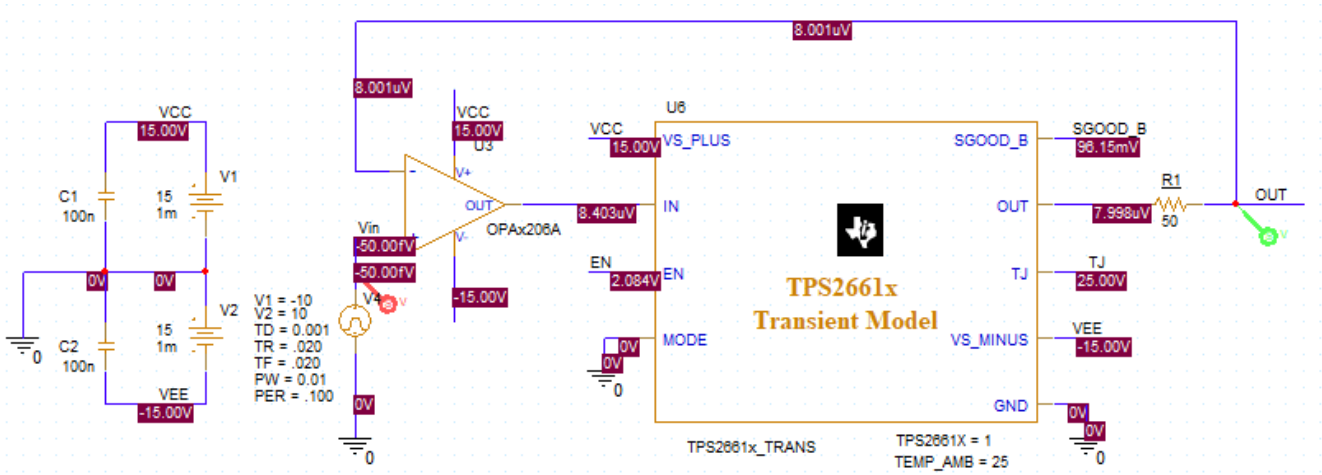
1. This design protects the output of a DAC without a positive sense pin as feedback There are many DACs that are configured without the sense pin, but this circuit uses the DAC81408 as an example. The DAC output is set to a range of ±10V.
2. The DAC81408 has five separate power supply inputs (VIO, VDD, VAA, VCC, and VSS). The *DACx1408 8-Channel, 16-,14-,12-Bit, High-Voltage Output DACs with Internal Reference* data sheet recommends using a 0.1µF decoupling capacitor for each power supply pin. Note that VCC and VSS (set to ± 15V) have two pins each. In addition, a 4.7µF or 10µF bulk capacitor is recommended for each power supply. Tantalum or aluminum capacitor types can be chosen for the bulk capacitors.
3. Connect a 150nF capacitor from the REF pin to ground if the internal reference is used. Connect a 330pF capacitor from the REFCMP pin to the REFGND pin as an additional reference compensation capacitor.
4. The DAC is protected from overvoltage events using an op amp configured as a unity gain buffer. The output overvoltage protection requires protecting the op amp inputs from an overvoltage beyond the supply and from protecting the output from sourcing or sinking excessive currents during these events.
5. In this circuit, the OPA206 is selected for the op amp buffer used for overvoltage protection. This op amp is selected for several characteristics:
   a. The offset voltage is very low and the buffer contributes little error to the DAC output. The OPA206 offset voltage is typically ±4µV (at 25°C) and ±55µV (from –40°C to 125°C).
   b. The OPA206 has an integrated input overvoltage protection that extends up to ±40V beyond the op amp supply voltage. The input bias current relative to the input common-mode voltage for the OPA206 is shown in the following figure.



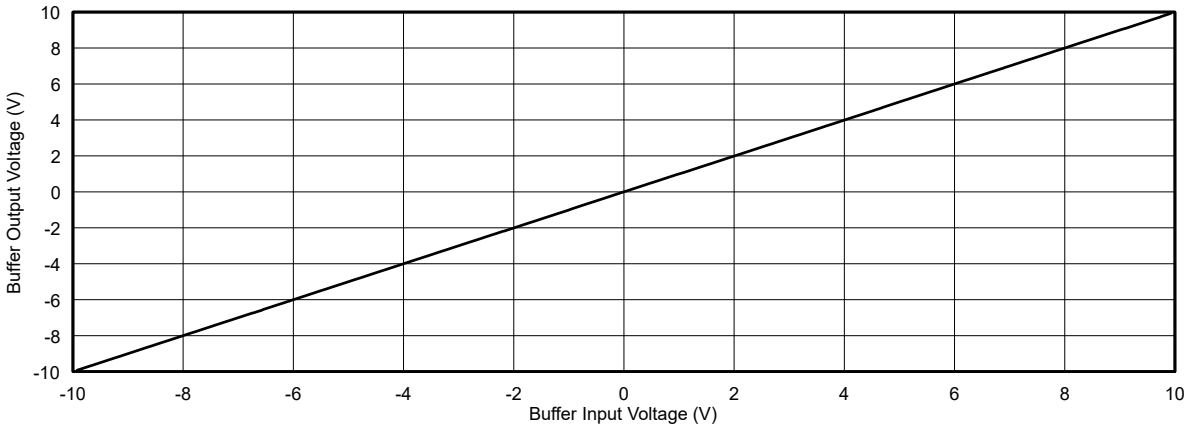
   c. The OPA206 has a short-circuit current limit of 25mA. However, the output is subject to excess current through the op amp internal ESD diodes. An eFuse is used at the op amp output, inside the output feedback to limit the current. This protection also limits the output current beyond the supply voltage.
   d. If an alternate op amp without integrated input overvoltage protection is used, series resistance for the inputs can be used for protection to limit the input current. For more information about overvoltage and electrical overstress in op amps, see the TI Precision Labs – Op Amps video on Electrical Overstress.
6. The TPS26611 is a current loop protector that acts as an eFuse to limit the output current of the op amp.
   a. Even if the short circuit current limit of the op amp is typically 25mA, the current through the ESD diodes to the output is not limited as the output voltage is forced beyond the op amp supply voltage.
   b. The maximum series resistance of the TPS26611 is 12.5Ω. With an additional series resistance of 49.9Ω, the extra headroom needed at the supply output is 0.936V at an output of 15mA.
   c. The EN and $\overline{\text{SGOOD}}$ pins can be left floating.
   d. For more information about using the TPS26611 as protection for an analog output module, see the *Protection for HART I/O in Analog Input and Output Modules with TPS2661x* data sheet.
7. An optional transient voltage suppression diode (TVS) is applied to the circuit for additional surge protection. If a TVS diode is used, the chose breakdown voltage must be higher than any sustained overvoltage. If the breakdown voltage is less than the sustained overvoltage, then the overvoltage can damage the TVS diode. In this circuit, the expected sustained overvoltage is ±32V and an optional TVS3301 device with a bidirectional 33V breakdown is used for surge protection.

Simulation

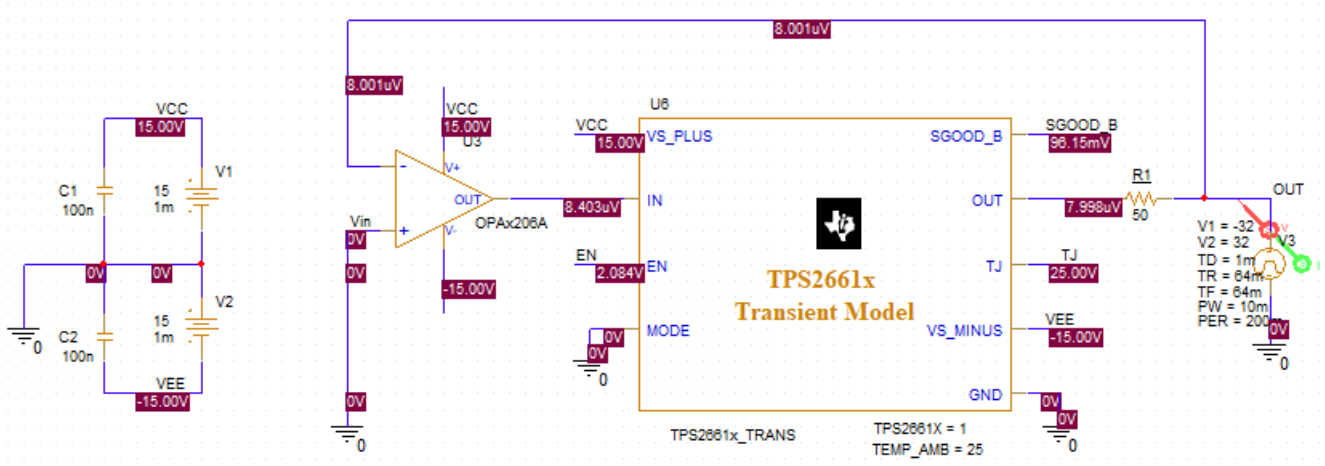
The overvoltage protection buffer is simulated with PSpice®. First, the transfer function of the buffer is simulated using a pulse voltage source as the DAC. The input of the buffer is ramped from –10V to +10V, showing the full output range of the DAC. The buffer schematic is constructed for simulation.



The transfer function from input to output of the buffer is derived from the transient simulation.

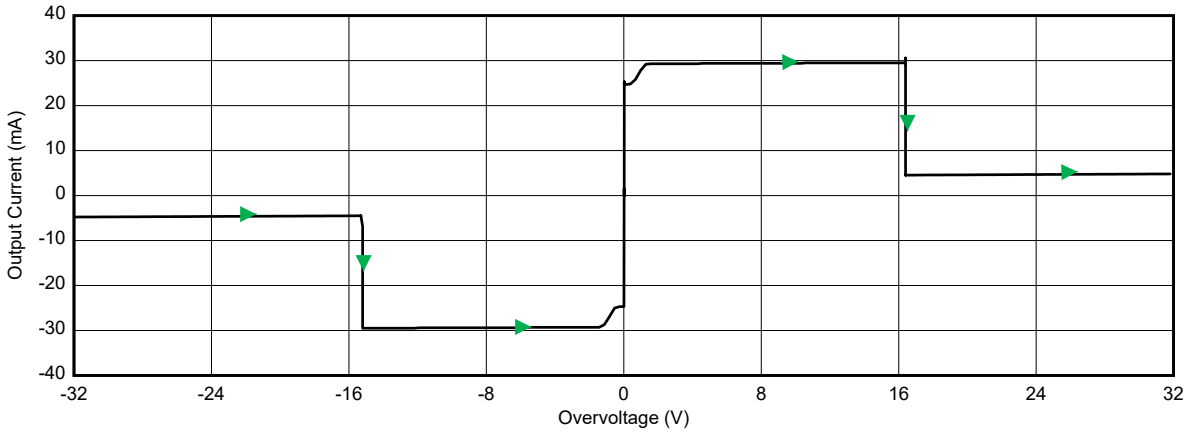


A second transient simulation shows the current during an overvoltage event.



The input is set to 0V and a voltage supply is placed at the output of the buffer. The supply ramp simulates the transition from –32V to +32V.

The simulation begins with the output at –32V, the TPS26611 eFuse is open, preventing any current from being sourced from the output of the OPA206. The residual current comes from the input of the OPA206 which has an integrated input protection, limiting the current to about 5mA. The current seen at the output of the buffer remains at 5mA as the voltage is reduced.



As the voltage increases to near the lower supply voltage of –15V, the TPS26611 begins to conduct current from the OPA206 output. The OPA206, driven by the ramping voltage, immediately reaches the device current limit of 30mA. This current limit is lower than the 32mA current protection level of the TPS26611, and allows the conducted current. The OPA206 sustained current limit is not destructive.

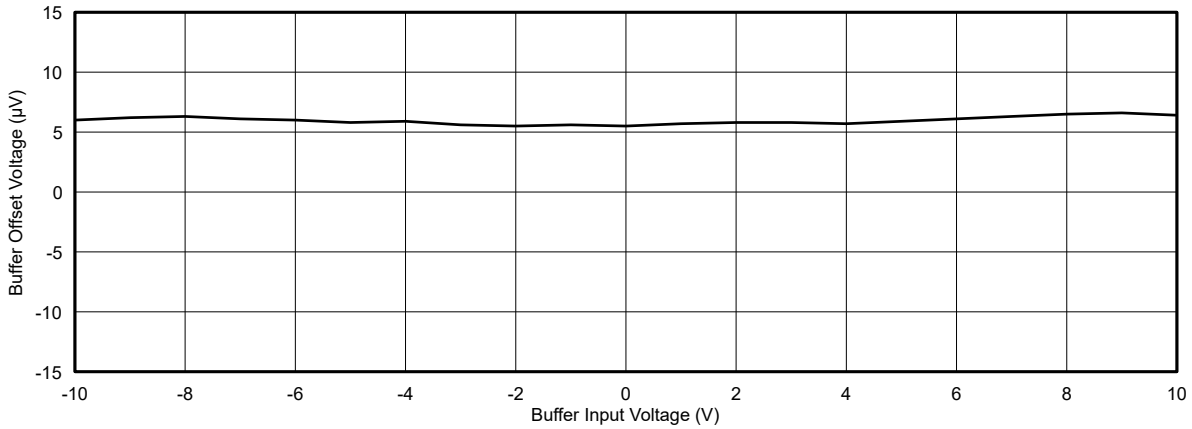
The ramped voltage rises and passes 0V and the output of the OPA206 changes from sourcing current to sinking current. The OPA206 is forced into a 30mA current limit in the opposite direction.

Finally, the ramped voltage rises above the positive supply of +15V. The TPS26611 eFuse opens again and the OPA206 output stops sinking current. Here, the only output current comes from the OPA206 input protection.

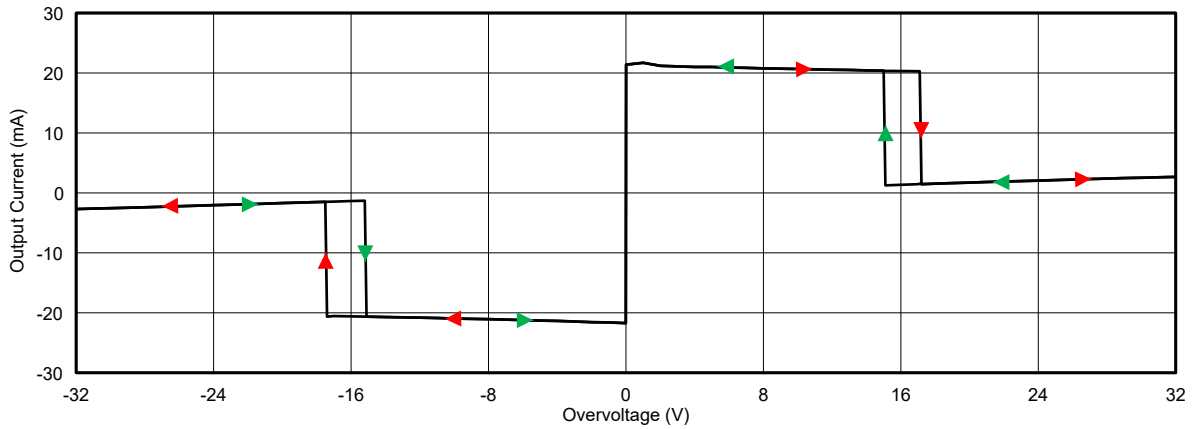
The TVS3301 is not simulated. However, the output is not sent above the protection threshold of 33V, which turns on TVS conduction. At the simulated level of 32V, TVS3301 does not affect the operation of the protection buffer and output of the DAC.

Measured Results

The overvoltage protection buffer is constructed for testing and is attached to the output of the DAC81416-08EVM. First, the output of the DAC is ramped from –10V to 10V to drive the buffer input. The offset seen from the buffer is measured to be less than 10µV over the full range.



The output is then connected to a variable supply. As the output is driven, the current at the output is recorded. The measurement starts with the supply at –32V and the variable supply is raised to +32V. Then the output is changed from +32V back down to –32V. This setup is similar to the schematic in the previously described simulation.



In the test, the OPA206 short-circuit current and input protection current are slightly lower than simulation. There is a hysteresis in the closing and opening of the TPS26611 eFuse. When starting with the TPS26611 eFuse closed and conducting current in normal operation, the eFuse opens when the output rises and is driven to about 2.5V beyond either supply. Here, the TPS26611 shuts off when the output is forced up above 17.2V or below –17.5V. This is partially seen in the simulation, which was run with a single ramp from a low to a high voltage.

Register Settings

The following table shows an example register map for this application with the DAC81408. The values given here are for the design choices made in the *Design Notes* section.

Register Settings for DAC81408

Register Address	Register Name	Setting	Description
0x03	SPICONFIG	0x0A84	[15:12] 0b0000: Reserved
			[11] 0b1: Thermal alarm triggers the $\overline{\text{ALMOUT}}$ pin
			[10] 0b0: $\overline{\text{ALMOUT}}$ is not set between DAC updates
			[9] 0b1: CRC error triggers the $\overline{\text{ALMOUT}}$ pin
			[8:7] 0b01: Reserved
			[6] 0b0: Soft toggle operation disabled
			[5] 0b0: Device is in active mode
			[4] 0b0: CRC is disabled
			[3] 0b0: Streaming mode is disabled
			[2] 0b1: SDO pin is operational
			[1] 0b0: SDO updates during SCLK rising edges
			[0] 0b0: Reserved
0x04	GENCONFIG	0x3F00	[15] 0b0: Reserved
			[14] 0b0: Internal reference enabled
			[13:6] 0b11111100: Reserved
			[5:2] 0b0000: Differential mode disabled for all channels
			[1:0] 0b00: Reserved
0x09	DACPWDWN	0xF00F	[15:12] 0b1111: Reserved
			[11:4] 0b00000000: All channels enabled, not in power-down mode
			[3:0] 0b1111: Reserved
0x0B, 0x0C	DACRANGE0 (Channels 7:4), DACRANGE1 (Channels 3:0)	0xAAAA	[15:12] 0b1010: Set the DAC output range to ±10V
			[11:8] 0b1010: Set the DAC output range to ±10V
			[7:4] 0b1010: Set the DAC output range to ±10V
			[3:0] 0b1010: Set the DAC output range to ±10V
0x14 – 0x1B	DAC0–DAC7 (Channels 0:7)	0x8000	[15:0] Set DAC data code for output voltage of 0V

Pseudocode Example

The following shows a pseudocode sequence to initialize the setup for the DAC81408. This pseudocode sets up the device for one channel for an output of ±10V. The values given here are for the design choices made in the *Design Notes* section.

Pseudocode Example for DAC81408

```
1:  //SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
2:  //Set the device in active mode
3:  WRITE SPICONFIG(0x3), 0x0A, 0x84
4:  //Enable the internal reference
5:  WRITE GENCONFIG(0x04),0x3F, 0x00
6:  //Enable all DAC channels, not in power-down mode
7:  WRITE DACPWDWN(0x09), 0xF0, 0x0F
8:  //Set Channels 7 to 4 to ±10V output range
9:  WRITE DACRANGE0(0x0B), 0xAA, 0xAA
10:  //Set Channels 3 to 0 to ±10V output range
11:  WRITE DACRANGE1(0x0C), 0xAA, 0xAA
12:  //Set DAC0 to output 0V
13:  //Data is configured in straight binary, not two's complement notation
14:  WRITE DAC0(0x14), 0x80, 0x00
15:  //Channels 1 through 7 configured through registers 0x15 - 0x1B
```

Design Featured Devices

Find other possible devices using the Parametric search tool.

Device	Key Features	Link
DAC81408	8-Channel, 16-Bit, High-Voltage Output DACs with Internal Reference	DAC81408
OPA206	Input-Overvoltage-Protected, 4µV, 0.08µV/°C, Low-Power Super Beta, e-trim Operational Amplifiers	OPA206
TPS26611	50V, Universal 4–20mA, ±20mA Current Loop Protector With Input and Output Miswiring Protection	TPS26611
TVS3301	33V Bidirectional Flat-Clamp Surge Protection Device	TVS3301

Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, *DAC81416-08 Evaluation Module User's Guide*
- Texas Instruments, *Protection for HART I/O in Analog Input and Output Modules with TPS2661x Application Report*
- Texas Instruments, *Precision labs series: Digital-to-analog converters (DACs)*
- Texas Instruments, *Precision labs series: Op Amps*
- Planet Analog, *Op-amp input protection can be noisy*

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