Application Brief

Analog Voltage Detection in TI Programmable Logic Devices

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Introduction

One major advantage TPLD has over other programmable logic options such as CPLDs or FPGAs are the analog macro-cells. These macro-cells enable TPLDs to detect and process analog signals alongside digital signals. This document provides an overview of some common macro-cells that can process and detect analog voltages and describes how to use them.

Discrete Analog Comparators

Some TPLDs have discrete analog comparators, shown in Figure 1. These operate in the same way that normal analog comparators do when the **PUP** ("power-up") input is logic high, and can compare an external analog signal provided at the non-inverting input to either an internal bandgap voltage reference or another external analog signal at the inverting input. The comparator outputs logic high when the voltage at the non-inverting input is greater than the voltage at the inverting input, and low otherwise.

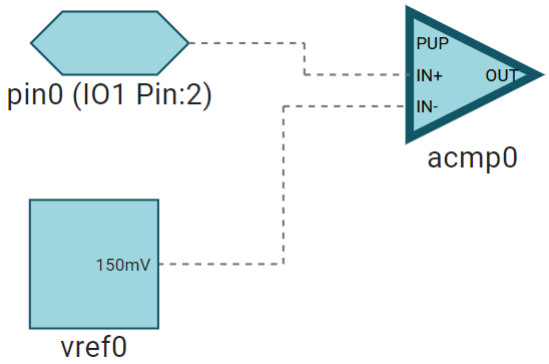

Figure 1. Discrete Analog Comparator Macro-Cell in InterConnect Studio (ICS)

When the **PUP** signal is logic low, the comparator is turned off to save power. A simulation of the discrete analog comparator comparing a 3.3V sine wave against a 1.2V bandgap reference is shown in Figure 2.

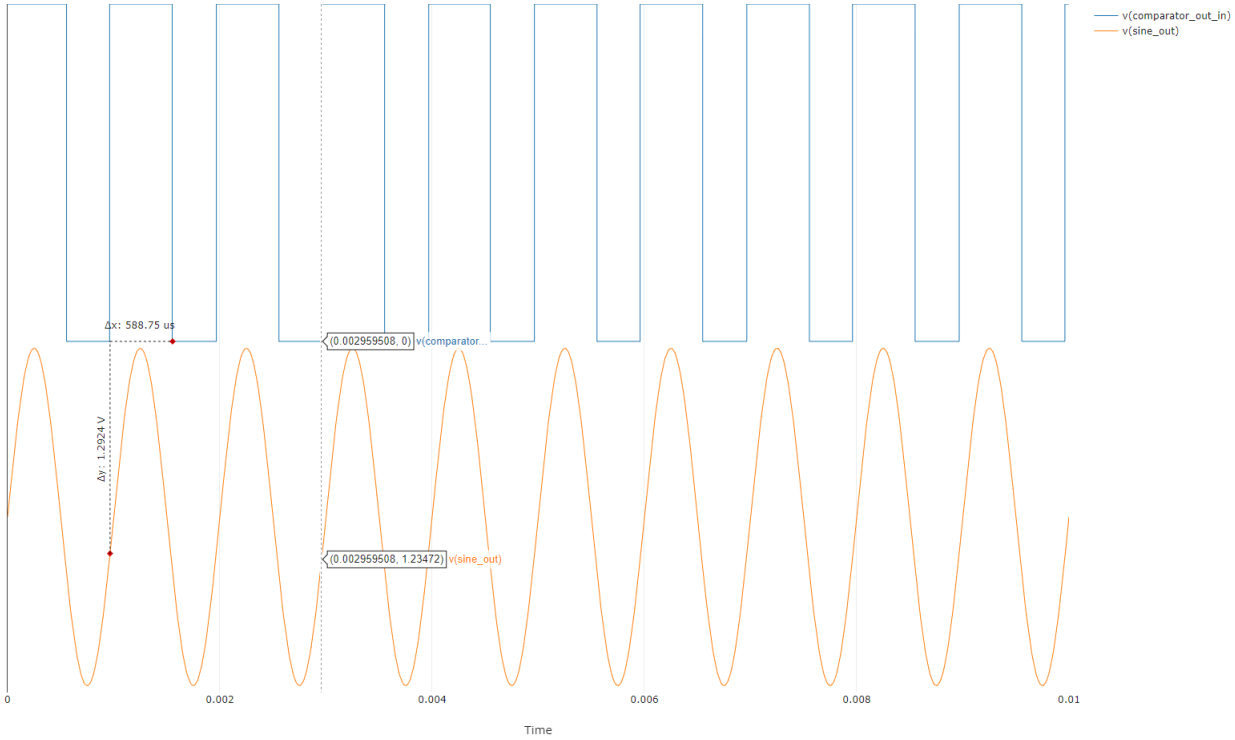

Figure 2. Discrete Analog Comparator Simulation

Configuration options for the discrete analog comparator are shown in Figure 3. These options include source selection for the non-inverting and inverting inputs, input gain options, hysteresis options, and a low bandwidth mode. The *Hysteresis Select* setting provides a small amount of noise margin on the comparator trigger point. For example, if using an internal voltage reference of 1V and a hysteresis of 200mV, the comparator trigger points are at 1.1V and 0.9V. The *Low Bandwidth* mode can be selected to save power and reduce the impact of noise when comparing lower bandwidth signals. The *Positive Input Gain* setting can be used to reduce the voltage of the non-inverting input seen by the comparator.

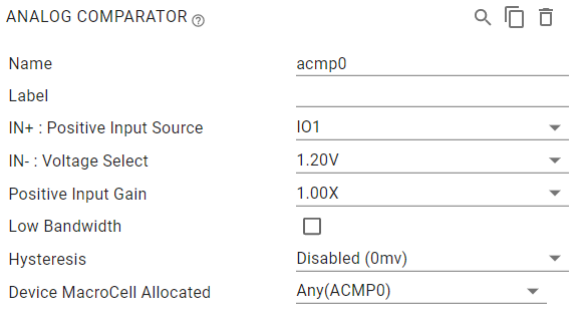

Figure 3. Discrete Analog Comparator Settings

Multi-Channel Analog Comparators

Some TPLDs have multi-channel analog comparators, either instead of or in addition to discrete analog comparators. The multi-channel analog comparator functions like a discrete analog comparator with multiple channels, with each channel having a pair of inverting and non-inverting inputs. Unlike the discrete analog comparator, the outputs are sampled on the rising edge of the selected clock signal, and the comparator also includes a reset input that can be enabled per channel and a data-ready output that asserts high when all outputs have been sampled. A picture of the multi-channel analog comparator with two channels enabled is shown in Figure 4.

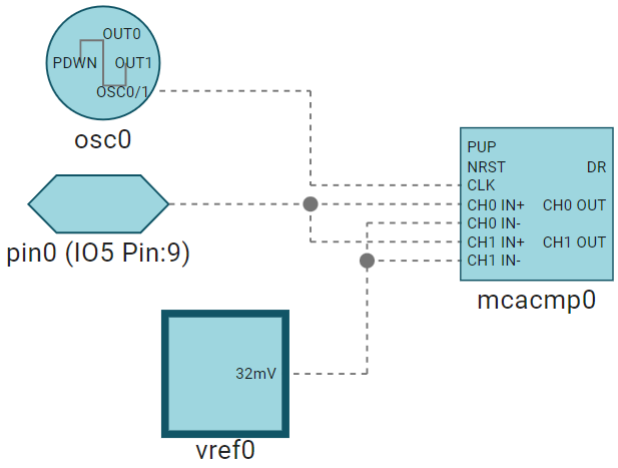

Figure 4. Multi-Channel Analog Comparator in ICS

Configuration options for the comparator are shown in Figure 5. *Channel Amount Sampled* selects the number of channels that are enabled, while *McACMP Clock Select* determines the clock used for sampling. *McACMP Trigger Mode* can be set to "Level sensitive" or "Edge sensitive". If level sensitive is selected, the comparator operates as long as **PUP** is asserted high, while if edge sensitive is selected, the comparator samples all outputs a single time after **PUP** sees a rising edge. *Temperature Sensor Input Enable* and *VCC Input Enable* causes one of the non-inverting input pins to reference the integrated temperature sensor or VCC, respectively.

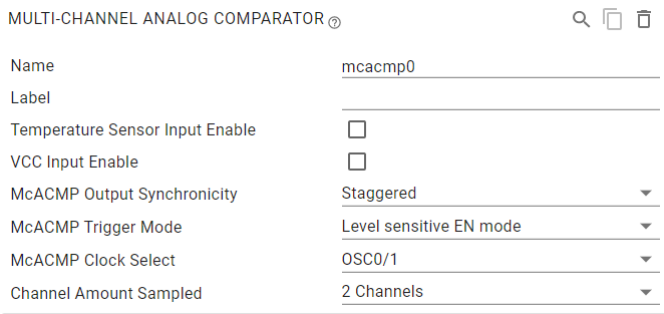

Figure 5. Multi-Channel Analog Comparator Settings

McACMP Output Synchronicity can be set to "Staggered" or "Simultaneous"; staggered means the outputs are asserted immediately as each channel is sampled, whereas simultaneous means the outputs are not be asserted until all of the enabled channels have been sampled. Simultaneous behavior of two channels is shown in Figure 6, while staggered behavior is shown in Figure 7. In both simulations, the input sine wave is being compared against 1.634V. Notice how in Figure 7 (staggered behavior) the second channel in yellow asserts one clock cycle after the first channel in blue, and how the channel one assert one clock cycle sooner in staggered mode than it does in simultaneous mode.

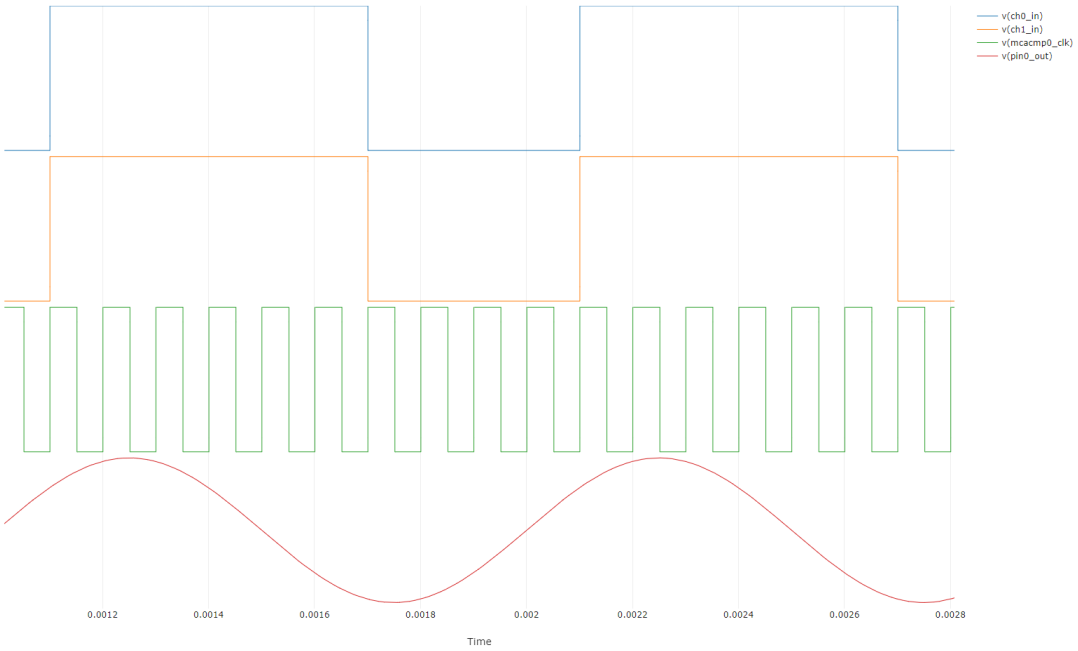

Figure 6. Multi-Channel Analog Comparator Simultaneous Sampling Simulation

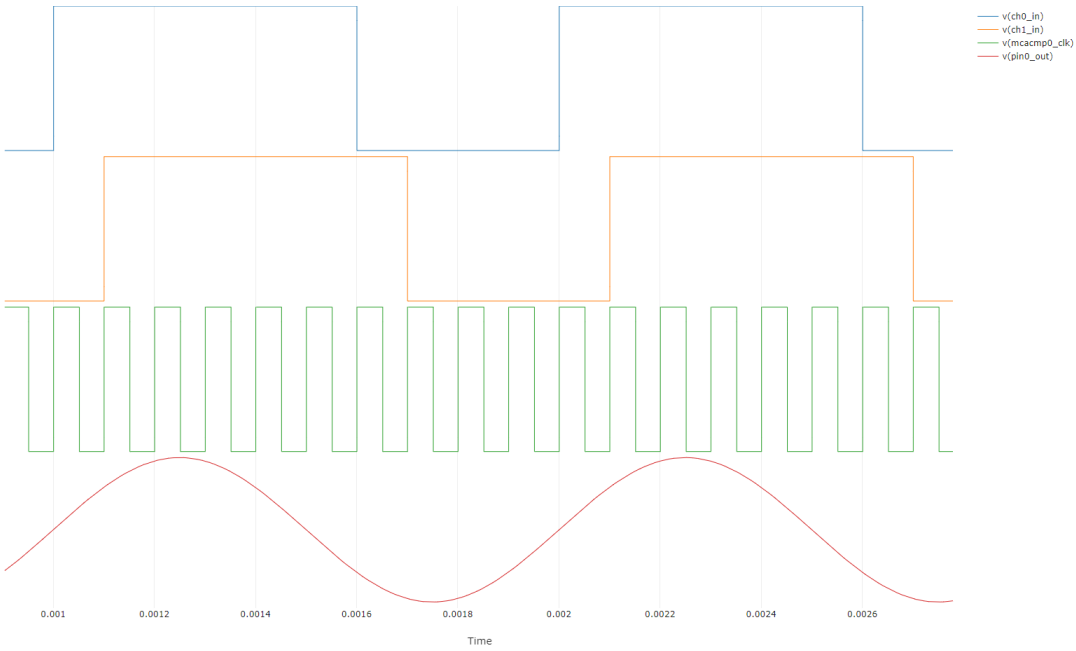

Figure 7. Multi-Channel Analog Comparator Sequential Sampling Simulation

Figure 8 shows the settings for each individual comparator channel. Note these are the same as the settings as shown in Figure 8 for the Discrete Analog Comparator, with the addition of the option to enable the asynchronous reset for that channel (and with the exclusion of a low bandwidth setting). If the asynchronous reset is enabled for a given channel, that channel's output asserts low regardless of the input while **NRST** is low.

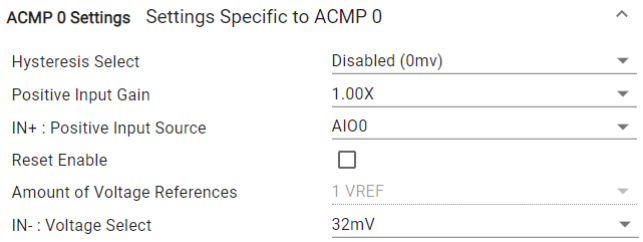

Figure 8. Multi-Channel Analog Comparator Channel Settings

Additional Considerations

When using either a discrete or multi-channel analog comparator for analog signal detection, make sure to adhere to the analog input voltage limits established by V_{AI} in the *Recommended Operation Conditions* section of the device-specific data sheet. Typically, the voltage on the non-inverting input cannot exceed VCC, while the voltage on the inverting input cannot exceed the value of the largest voltage provided by the TPLDs internal bandgap reference.

Both the discrete and multi-channel comparators must have the **PUP** input asserted high (or provided with a rising edge, if in rising edge mode) to operate. If this signal is low, the outputs of the comparators are low. The power-up signal can be asserted high all the time through connection to VCC, low all the time through connection to GND, or changed dynamically by a digital signal coming from an input pin or elsewhere in the device. The comparator outputs become valid within around 100µs after the power-up signal is asserted high; refer to the device-specific data sheet for the proper startup time and verify that the internal oscillator is not powered down during this time.

If hysteresis is enabled, the hysteresis must be less than the reference voltage provided on the inverting input. If the reference voltage is smaller, the negative trigger point is pushed below ground, which can place the device outside of the Recommended Operation Conditions and result in reduced lifetime or damage. Finally, the positive input gain setting reduces the voltage seen at the input of the comparator internally, but does not allow V_{AI} to be exceeded.

Conclusion

Through use of the integrated discrete and multi-channel analog comparators, TPLD can be used to detect a wide range of low-voltage analog signals. In combination with the digital elements, these comparators allow TPLD to service a wide range of sensing and voltage level detection applications in a mixed-signal environment.

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