*Application Note*

# *DC-Link Capacitor Pre-Charge Designs in Automotive Systems*

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**ABSTRACT**

In hybrid electric vehicles and electric vehicles (HEV/EV), pre-charging the DC-link capacitor is essential. Traditional pre-charge circuits incorporate costly electromechanical relays (EMR) and substantial high-power resistors, which contradict requirements for high-power density and reduced bill of materials (BOM) cost. This application note presents several alternative pre-charge designs, including isolated switching drivers, active pre-charge controllers, high voltage (HV) buck converters, and isolated DC/DC converters, along with respective control methodologies. These designs demonstrate distinct comparative advantages regarding power density, component costs, and functional safety parameters.

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## Trademarks

# 1 Introduction

In HEV/EV systems, high-voltage loads are not directly powered by the energy stored in the HV battery. A DC-link capacitor is positioned between the HV battery and HV load to function as a buffer stage. DC-link capacitors serve two primary functions: decoupling parasitic inductance effects between the HV battery and HV load, and providing a low-impedance path for high-frequency current. The DC-link capacitance typically ranges from several hundred microfarads to thousands of microfarads.

However, when HV loads are inactive, no voltage exists on the DC-link capacitor. As shown in Figure 1-1, the main contactor positive (MCP) and main contactor negative (MCN) remain open, disconnecting the HV battery from the HV load at both terminals, while the DC-link capacitor maintains a discharged state. When MCP and MCN close, this effectively creates a direct short circuit of the DC-link capacitor, resulting in extremely high current. Without appropriate limitation of this inrush current, damage to cables, connectors, and fuses can occur.

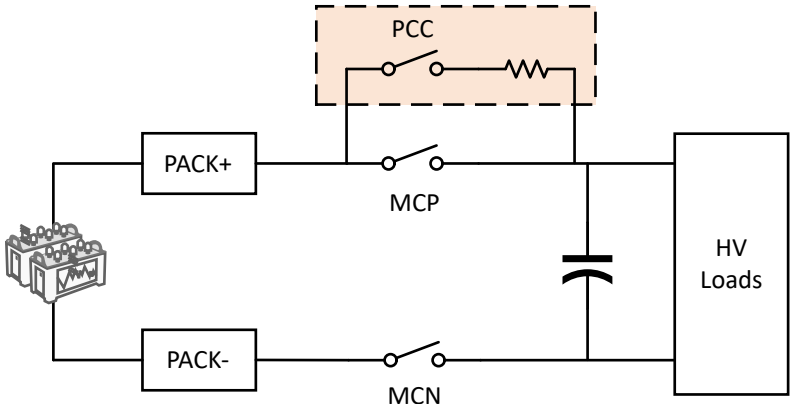


**Figure 1-1. DC-Link Capacitor in HEV/EV System**

Therefore, HV systems require pre-charge circuits to limit inrush current. A conventional pre-charge circuit comprises a pre-charge contactor (PCC) and current-limiting resistor. During the pre-charge phase, the PCC and MCN close, charging the DC-link capacitor to a voltage approximating that of the HV battery. The current-limiting resistor in the circuit restricts inrush current during this phase. Following the pre-charge phase, the PCC opens and MCP closes, allowing the HV battery to power the load. The current-limiting resistor is bypassed to reduce circuit impedance. Traditional pre-charge circuits typically incorporate costly EMRs and substantial high-power resistors, which contradict requirements for high-power density and reduced BOM cost.

## 2 System Challenge on DC-Link Capacitor Pre-charge

The capacitance of DC-link capacitors varies according to the output power of the traction inverter, ranging from several hundred microfarads to thousands of microfarads. The pre-charging duration for DC-link capacitors must not exceed 400ms. The conventional methodology employed for pre-charging DC-link capacitors utilizes Electromechanical Relays. The operational principles of this approach were addressed in Chapter One, and the parameter design methodology is elaborated upon in the following sections. As shown in Figure 2-1, when the pre-charge contactor closes, the equivalent circuit constitutes a standard RC series configuration.

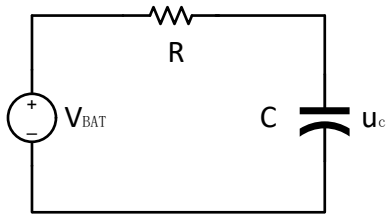


**Figure 2-1. Equivalent Circuit of Pre-Charge Circuit**

The voltage across the DC-link capacitor is expressed as:

$$u_C = V_{BAT}\left(1 - e^{-\frac{t}{\tau}}\right), \tau = RC \quad (1)$$

Suppose the HV battery is 800V, the DC-link capacitance is 1000uF, the pre-charge time requirement is 150ms. Select the resistance according to the pre-charge time requirement:

$$t = 3\tau \leq 150ms \quad (2)$$

$$R \leq \frac{t/3}{C} = 50\Omega \quad (3)$$

Select the average power of pre-charge resistor:

$$P_{AVG} = \frac{E}{t} = \frac{1}{2}C(0.95V_{BAT})^2/t = 1925W \quad (4)$$

Select the peak current of pre-charge resistor and relay:

$$I_{PEAK} = \frac{V_{BAT}}{R} = 16A \quad (5)$$

According to the calculation, for the preset parameters, the resistor and 16A relay must be selected. In practical circuit design implementation, parameter derating must be considered, which requires the use of costly relays and substantial high-power resistors in this pre-charge circuit.

With increasing demands for cost reduction and volume optimization in HEV/EV systems, several alternative designs have emerged to replace traditional pre-charge circuits. These designs will be analyzed and compared in subsequent sections.

# 3 System Approach

Multiple pre-charge designs exist in the market, either using specialized pre-charging circuits or leveraging existing circuits within HEV/EV systems. This application note examines the operational principles of various designs and the primary devices offered by Texas Instruments.

## 3.1 Isolated Switch Driver

The TPSI3050-Q1 represents a fully integrated, isolated switch driver. When combined with an external power switch, it forms a comprehensive isolated Solid-State Relay (SSR). SSRs offer three significant advantages over EMRs:

- Isolated Switch Driver: It provides flexibility to drive external Field-Effect Transistors (FETs) or Insulated Gate Bipolar Transistors (IGBTs). Compared to mechanical relays, SSRs demonstrate enhanced reliability, reduced weight, and smaller dimensions. The absence of mechanical moving contacts eliminates audible noise and physical circuit degradation.
- Rapid Switch Deactivation: The response time is less than 3µs, whereas relays typically operate in the range of 1-50ms, which is critical for protection during events such as overheating or overcurrent conditions.
- Secondary Bias Supply Generation: It generates secondary bias supply from power received on its primary side. The secondary side provides a regulated floating supply rail of 10V for driving various power switches.

Figure 3-1 illustrates the block diagram of this application. The TPSI3050-Q1 is controlled via an EN signal from a microcontroller. The VDRV pin drives the back-to-back MOSFETs in a common source configuration.

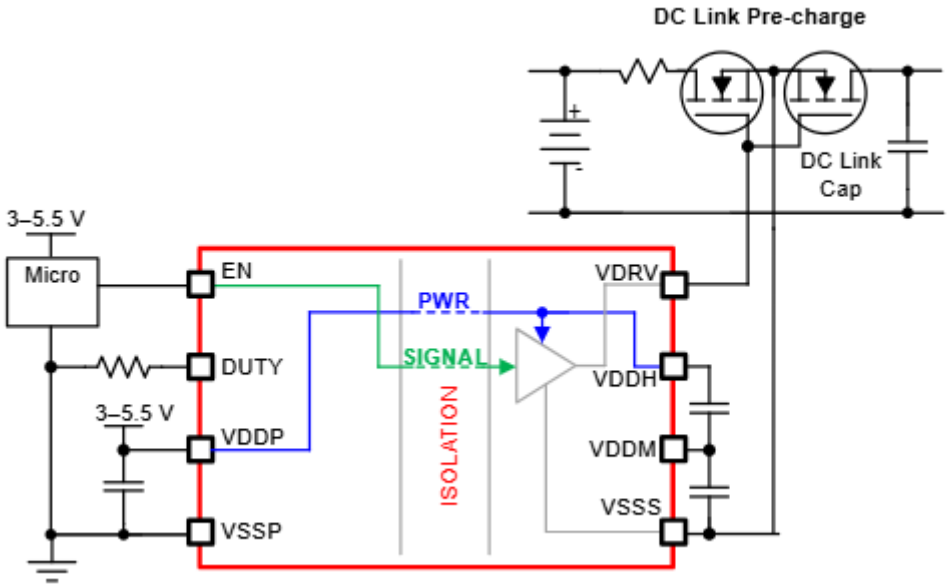


**Figure 3-1. Block diagram of TPSI3050-Q1 in application**

In summary, the principal distinction between this design and the approach described in Figure 1-1 lies in component selection. The TPSI3050-Q1 can replace traditional pre-charged mechanical relays, offering enhanced reliability, reduced dimensions, and improved response characteristics. For additional details, reference TIDA-050080 .

### 3.2 Active Pre-charge Controller

The TPSI31P1-Q1 functions as an active pre-charge controller with 17V isolated gate driver and bias supply. When combined with external power switches, power inductor, and diode, this constitutes an active pre-charge design. Compared to the TPSI3050-Q1, the TPSI31P1-Q1 incorporates two additional features specifically designed for pre-charge applications.

- The inductor current undergoes continuous monitoring and control in a hysteretic operational mode to linearly charge the substantial capacitance of the DC-link capacitor.
- This integrates a communication back-channel that transmits status information from the secondary side to the primary side to indicate power status on the secondary side.

Figure 3-2 shows the block diagram of this application. The TPSI31P1-Q1 receives control signals via the EN input from a microcontroller. The external power inductor (L1), in conjunction with power diode (D1) and power FET (M1), forms a bulk converter. M2 represents an optional MOSFET for reverse blocking functionality. The shunt resistor facilitates current monitoring in L1 through voltage measurement at the IS+ pin.

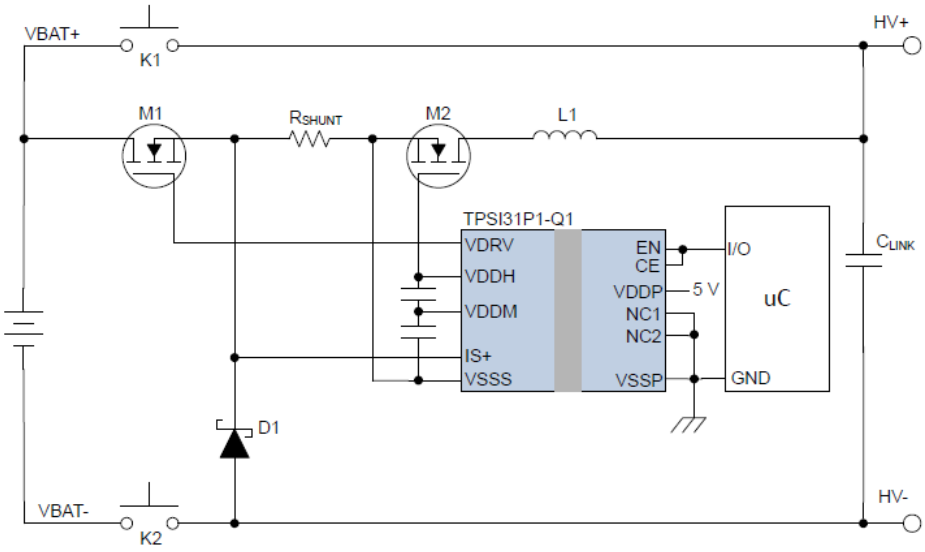


**Figure 3-2. Block Diagram of TPSI31P1-Q1 in Application**

The key operational feature is the buck converter configuration. When IS+ falls below VREF-, VDRV is asserted high to activate M1, initiating the energy storage cycle of the buck converter. When IS+ exceeds VREF+, VDRV is asserted low to deactivate M1, commencing the power transfer cycle of the buck converter. This process continues throughout the entire pre-charge cycle to regulate the charging current.

Suppose the HV battery is 800V, the DC-link capacitance is 1000uF, the pre-charge time requirement is 150ms. The average charging current can be computed as follows:

$$I_{AVG} \geq \frac{C \times V_{BAT}}{t} = 5.33A \quad (6)$$

The shunt resistor required to set the inductor current can be calculated:

$$R_{SNS} \leq \frac{V_{REF+} + V_{REF-}}{2 \times I_{AVG}} = 130m\Omega \quad (7)$$

The maximum inductor current is:

$$I_{PEAK} = \frac{V_{REF+}}{R_{SNS}} = 9.46A \quad (8)$$

The minimum inductor current is:

$$I_{MIN} = \frac{V_{REF} -}{R_{SNS}} = 1.23A \quad (9)$$

The maximum switching frequency occurs when the voltage across the link capacitance reaches the midpoint value, which can be determined by the minimum power transfer capability of TPSI31P1, the total gate charge of the FET, and the gate-to-source voltage. Suppose P = 55mW, Vgs=15V, Qg = 14nC, the maximum switching frequency is:

$$f_{MAX} = \frac{P}{V_{gs} \times Q_g} = 261.9kHz \quad (10)$$

Based on the maximum switching frequency, the minimum inductance can be calculated:

$$L_{MIN} \geq \frac{V_{BAT}}{4 \times f_{MAX} \times (I_{PEAK} - I_{MIN})} = 92.8\mu H \quad (11)$$

Therefore, 100uH inductance value can be selected. The $C_{DIV1}$ and $C_{DIV2}$ capacitors depends on the VDDH drop requirement. For example, the total capacitance formed by the series combination of $C_{DIV1}$ and $C_{DIV2}$ must result in 0.5V drop of VDDH supply rail:

$$C_{DIV1} \parallel C_{DIV2} \geq \frac{Q_G}{\Delta V} = 28nF \quad (12)$$

To reduce the voltage drop further, the capacitance can be selected as $C_{DIV1}$ = 330nF, $C_{DIV2}$ = 1µF .

The TPSI31P1-Q1 includes a calculator that incorporates these equations and generates the anticipated charging waveform. For additional details, see TPSI31P1-CALC.

### 3.3 Discrete High Voltage Buck Design

The discrete HV Buck design presents another option for pre-charging DC-link capacitors. This approach shares similarities with the TPSI31P1-Q1 in terms of power stage design but differs significantly in control methodology.

Figure 3-3 depicts the block diagram for one discrete HV Buck design. The microcontroller unit (MCU) for OBC/DCDC/Inverter acquires HV battery voltage information from the Battery Management System (BMS), configures the output voltage for the HV Buck converter, then closes RELAY2 and initiates DC-link capacitor pre-charging. Upon completion, this transmits a READY signal to the BMS to close RELAY1.

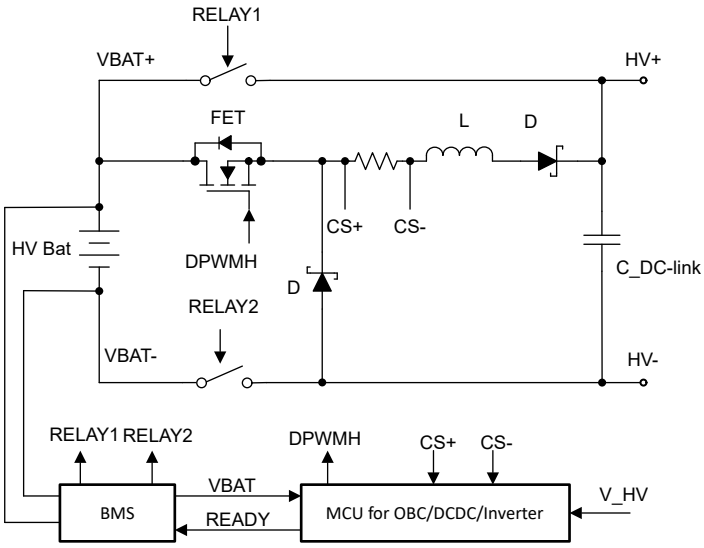


**Figure 3-3. Block Diagram for Discrete HV Buck Design 1**

Figure 3-4 illustrates an alternative discrete HV Buck design for pre-charging DC-link capacitors. The MCU for OBC/DCDC/Inverter receives HV battery voltage data from the BMS, establishes the output voltage parameters for the HV Buck converter, then activates RELAY1 and initiates the pre-charging process for the DC-link capacitor. Upon completion, this transmits a READY signal to the BMS to activate RELAY2. In this configuration, the controller and FET are referenced to VBAT-, requiring only a low-side driver for FET activation, whereas the HV Buck design 1 requires an isolated driver for FET activation.

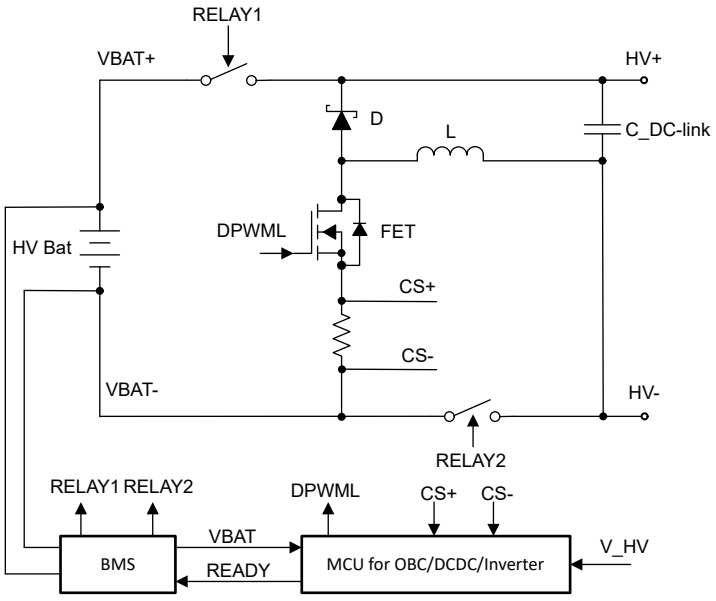


**Figure 3-4. Block diagram for Discrete HV Buck Design 2**

For example, assuming a DC bus voltage of 400V, DC-link capacitor capacitance of 600µF, and a pre-charging time requirement of less than 200ms, the average current can be calculated:

$$I = \frac{C \times U}{t} = \frac{600uF \times 400V}{200ms} = 1.2A \quad (13)$$

The average current is about 1.2A, making an average power of 480W. Suppose the switching frequency is 200kHz, output voltage is 380V. The inductance of Buck inductor can be calculated :

$$L = \frac{Vout \times toff}{\Delta I} = \frac{380V \times (1 - 380V/400V)}{0.4 \times 1.2A \times 200kHz} = 197uH \quad (14)$$

Figure 3-5 presents the SIMetrix Simulation circuit based on the aforementioned calculations, while Figure 3-6 displays the simulation results. The maximum inrush current through the inductor is 4A. For a PQ32 core with a cross-sectional area (Ae) of 154mm², the turn ratio can be calculated:

$$N = \frac{L \times \Delta I}{Ae \times \Delta B} = \frac{197uH \times 4A}{154mm^2 \times 0.3T} = 17 \quad (15)$$

Considering a margin for inrush current, the turn ratio can be established at 20. It is imperative to note that the Buck inductor must be rated for high voltage applications. A lower inductance value can be selected for the Buck inductor, provided verification verifies adequate saturation current capacity for the inductor.

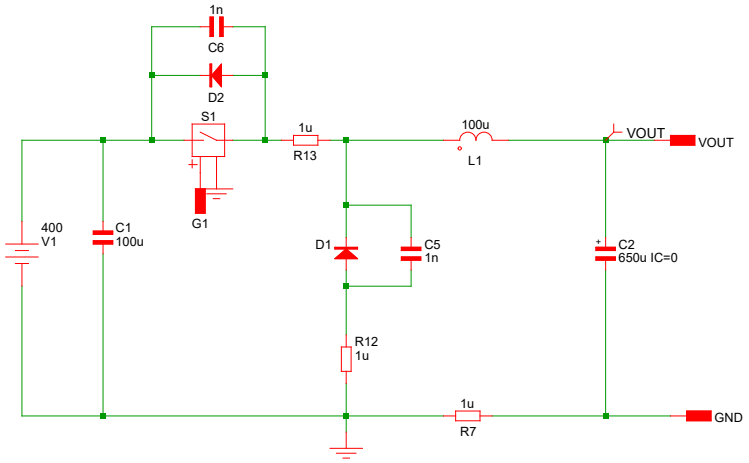


**Figure 3-5. SIMetrix Simulation Circuit for HV Buck Design**

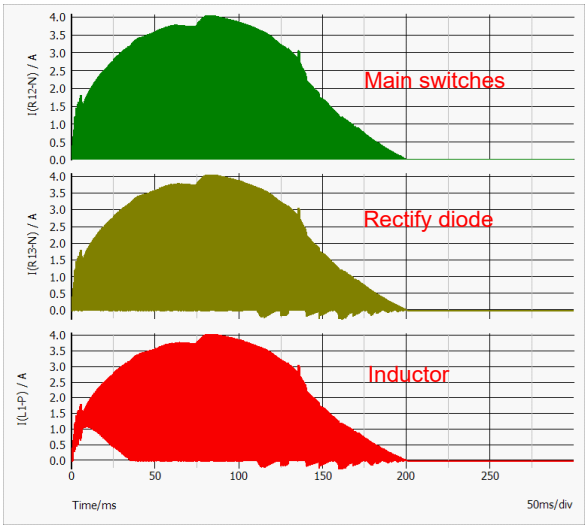


**Figure 3-6. SIMetrix Simulation Results for HV Buck Designs**

Table 3-1 enumerates the primary components used in discrete HV Buck designs. The existing MCU in OBC/DCDC/Inverter can be repurposed. The isolated driver facilitates high-side FET activation. In the block diagrams shown in Figure 3-3 and Figure 3-4, the SHUNT component can alternatively be implemented as a Hall sensor.

**Table 3-1. TI Components**

| | Part Number | Spec |
|---|---|---|
| MCU | F29H859TU-Q1 | C2000 series |
| Controller | UCC28740-Q1 | 1. HV Buck controller<br>2. Bias supply, transfer 400V/800V to 12V/24V |
| Isolated Driver | UCC21351-Q1 | Basic Isolation |
| Isolated Driver | UCC21551-Q1 | Reinforced Isolation |
| Isolated Driver | UCC5350L-Q1 | Reinforced Isolation |
| Hall sensor | TMCS1133-Q1 | Replace CT |
| LLC Converter | UCC25800-Q1 | Bias supply, transfer 12V to 12V/24V |

## 3.4 Independent Isolated DCDC Boost Design

In systems where the HV-LV DCDC converter lacks bidirectional capability, an independent isolated DCDC Boost design represents a viable alternative. This approach also facilitates the utilization of LV batteries for pre-charging DC-link capacitors. Given the average power requirements, push-pull topology is generally preferred.

Figure 3-7 shows the block diagram for an independent isolated DCDC design. The MCU for OBC/DCDC/Inverter receives HV battery voltage information from the BMS, configures the output voltage for the isolated DCDC converter, and initiates the pre-charging process for the DC-link capacitor. Upon completion, this transmits a READY signal to the BMS to activate RELAY1 and RELAY2.

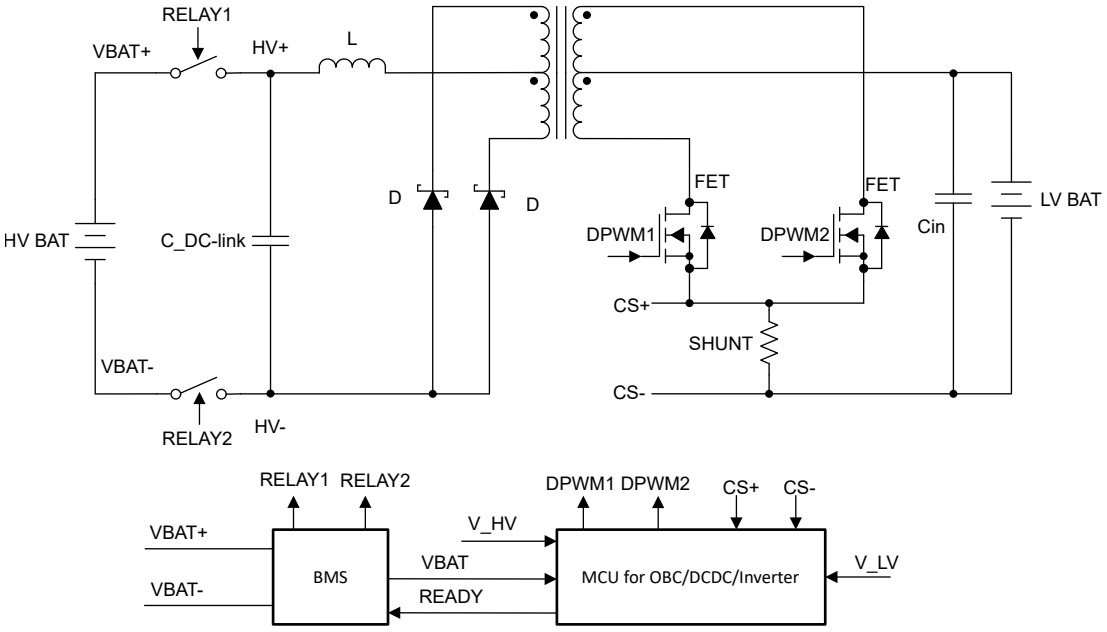


**Figure 3-7. Block Diagram for Independent DCDC Design**

Using a 400V DC Bus voltage and 600µF DC-link capacitor as an example, with LV battery voltage ranging from 9V to 16V, a transformer turn ratio of 1:50 can be established. According to Equation 1 , the average current is 1.2A. Setting delta IL to 0.3Iout and the switching frequency to 100kHz:

$$\mathrm{D} = \frac{\mathrm{Nps} \times (\mathrm{Vout} + \mathrm{Vd})}{\mathrm{Vin}} = \frac{400\mathrm{v} + 1\mathrm{v}}{50 \times 12\mathrm{V}} = 0.668 \tag{16}$$

$$\mathrm{Lout} = \frac{(\mathrm{Vout} + \mathrm{Vd}) \times (1 - \mathrm{D})/2}{\Delta \mathrm{I} \times \mathrm{fsw}} = \frac{(400\mathrm{v} + 1\mathrm{v}) \times (1 - 0.668)/2}{0.3 \times 1.2\mathrm{A} \times 200\mathrm{kHz}} = 924\mathrm{uH} \tag{17}$$

The calculated inductance is 924µH; however, in simulation, considering inrush current and winding turns of the inductor, 500µH is used. Figure 3-8 presents the SIMetrix Simulation circuit based on these calculations, while Figure 3-9 displays the simulation results.

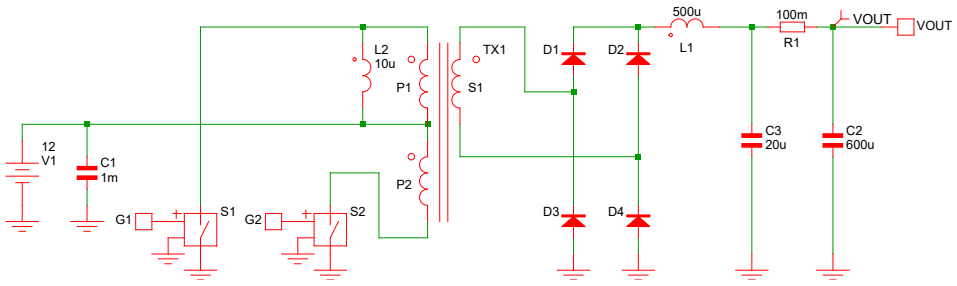


**Figure 3-8. SIMetrix Simulation Circuit for Independent DCDC Design**

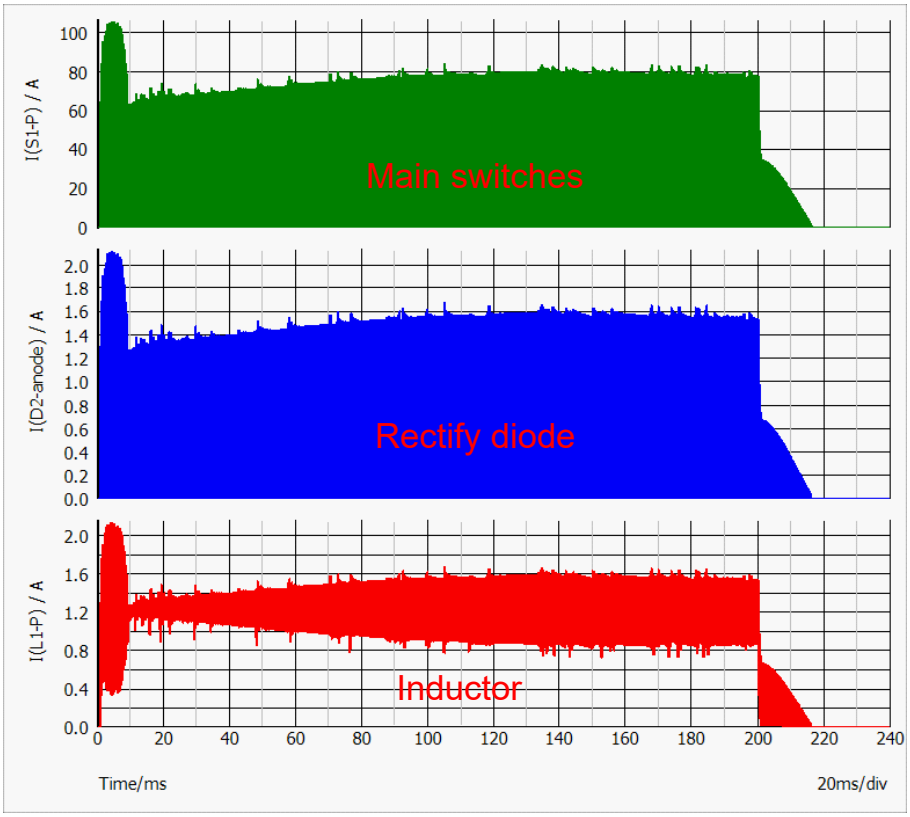


**Figure 3-9. SIMetrix Simulation Results for Independent DCDC Design**

Table 3-2 enumerates the primary components used in independent DCDC design. The existing MCU of OBC/DCDC/Inverter can be repurposed to generate PWM signals and implement closed-loop control. If MCU bandwidth constraints exist, LM25037-Q1 can be used for control functions and ISOM8110-Q1 for isolated feedback.

**Table 3-2. TI Components**

| | Part Number | Spec |
|---|---|---|
| MCU | F29H859TU-Q1 | C2000 series |
| Low side driver | UCC27524A-Q1 | Two channels |
| Low side driver | UCC27518A-Q1 | One channel |
| Push-pull controller | LM25037-Q1 | |
| Optical emulator | ISOM8110-Q1 | Optocoupler |

## 3.5 Integrated Pre-charge Design

Rather than implementing dedicated hardware, automotive manufacturers can leverage existing vehicle ECUs, such as the Battery Management System (BMS), HV-LV DC/DC converter—to orchestrate the pre-charge sequence through sophisticated software algorithms. By embedding pre-charge functionality within the vehicle's existing electronic architecture, manufacturers can achieve more efficient system design while maintaining robust protection for high-voltage powertrain components.

### *3.5.1 Bidirectional High-Voltage to Low-Voltage (HV-LV) DCDC*

In HEV/EV systems, the HV-LV DCDC converter interfaces with the HV battery to transform power from the HV battery to the LV battery and supply LV loads. The bidirectional functionality can be leveraged for pre-charging the DC-link capacitor, as shown in Figure 3-10.

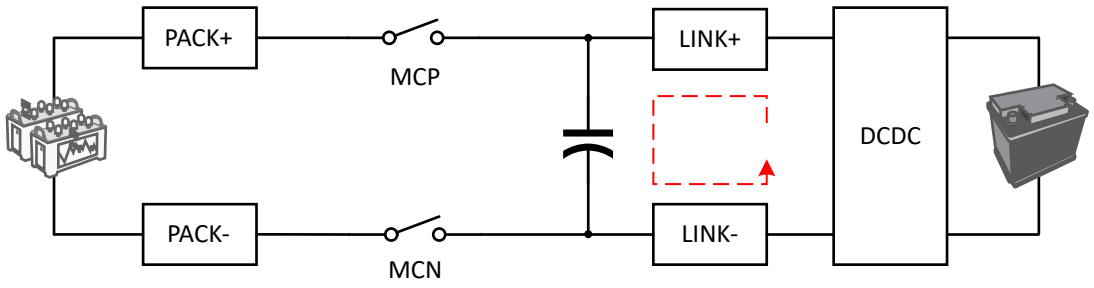


**Figure 3-10. Pre-charge Circuit with HV-LV DCDC**

Assuming the HV-LV DCDC topology uses a phase-shifted full bridge (PSFB) configuration, Figure 3-11 depicts the block diagram of reverse control operation. This process can be segmented into energy storage and power transfer cycles.

- Energy storage cycle:
  - In secondary side, Q5, Q6, Q7, Q8 are switched on. The secondary side operates as boost converter to charge the output inductor.
  - In primary side, Q2 and Q4 are switched on. The primary side is in freewheeling stage to conduct the current on the leakage inductance.
- Power transfer cycle:
  - The red line in Figure 3-11 is an example of current path.
  - Q1, Q4, Q5, Q8 are switch on to transfer the energy from LV battery and output inductor to the HV battery.

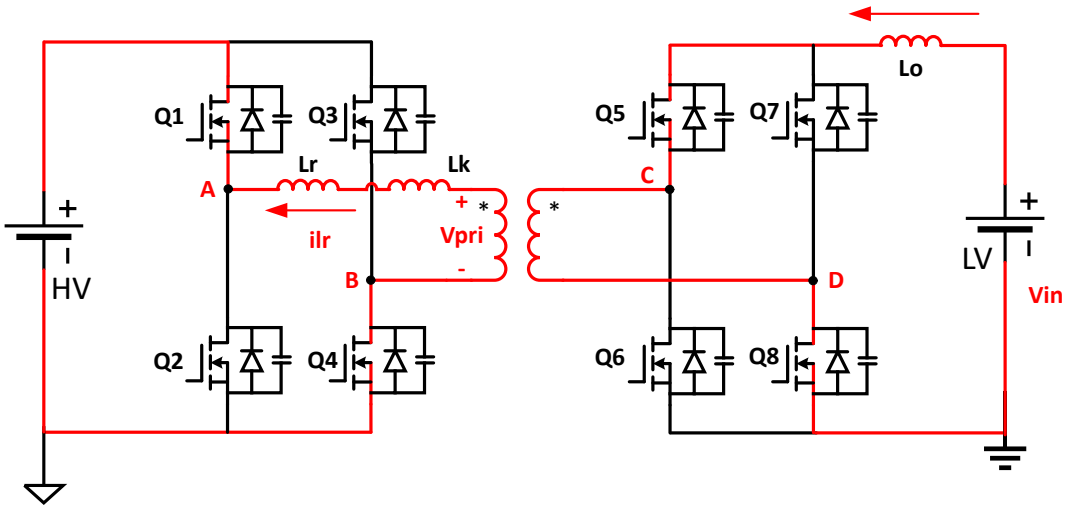


**Figure 3-11. Block Diagram of PSFB Reverse Control**

A primary concern with this design is the voltage spike occurrence on secondary-side power switches due to current mismatch. PMP41078 represents a 3.5kW 400V to 14V HV-LV DCDC reference design capable of reverse mode operation. For additional details, see PMP41078 .

### *3.5.2 Battery Heater*

Figure 3-12 shows the block diagram for an integrated design to pre-charge the DC-link capacitor from the positive direction. Initially, KL1 is closed, and Q7 and Q3 are activated to charge inductor L1. Subsequently, Q7 is deactivated, causing the inductor current to flow through Q3, HV_BAT, KL1, C_DC_link, and Q4. This process pre-charges C_DC_link to battery voltage. Thereafter, Q1 and Q2 are activated to establish a parallel connection between HV_BAT and C_DC_link.

When battery heating is required, Q1 and Q2 are deactivated, while Q3 and Q7 are activated to charge L1. Next, Q7 is deactivated and Q4 is activated, resulting in a voltage on the DC-link capacitor that exceeds HV_BAT. After the current in L1 reverses direction, the DC-link capacitor discharges into HV_BAT. Subsequently, Q4 is deactivated and Q7 is activated, causing the voltage on HV_BAT to exceed that of the DC-link capacitor. Following another current reversal in L1, the next cycle commences. This control methodology facilitates energy oscillation between HV_BAT and the DC-link capacitor, thereby heating HV_BAT.

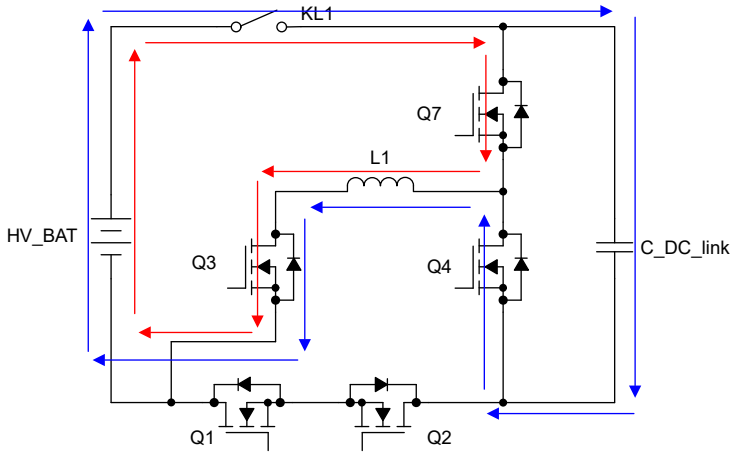


**Figure 3-12. Block Diagram for Integrated Pre-charge Design 1**

Figure 3-13 presents the block diagram for an integrated design to pre-charge the DC-link capacitor from the negative direction. Initially, KL1 is activated, and Q5 and Q8 are activated to charge inductor L1. Subsequently, Q8 is deactivated, causing the inductor current to flow through Q6, C_DC_link, KL1, HV_BAT, and Q5. This process pre-charges C_DC_link to battery voltage. Thereafter, Q1 and Q2 are activated to establish a parallel connection between HV_BAT and C_DC_link.

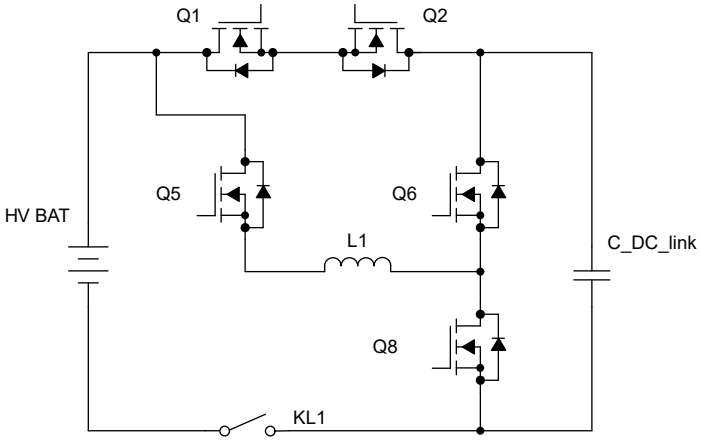


**Figure 3-13. Block Diagram for Integrated Pre-charge Design 2**

The integrated design represents a system-level approach. To achieve DC-link capacitor pre-charging and HV_BAT heating, a microcontroller is essential. Additionally, various isolated or non-isolated drivers are required. For the back-to-back FETs Q1/Q2, bi-directional GaN LMG3660-Q1 can be substituted. Table 3-3 enumerates the primary TI components used in this integrated design, including microcontrollers, drivers, and sensors.

**Table 3-3. TI Components**

| | Part Number | Spec |
|---|---|---|
| MCU | F29H859TU-Q1 | C2000 series |
| Low side driver | UCC27524A-Q1 | Two channels |
| Low side driver | UCC27518A-Q1 | One channel |
| Isolated Driver | UCC21351-Q1 | Basic Isolation |

**Table 3-3. TI Components (continued)**

| | Part Number | Spec |
|---|---|---|
| Isolated Driver | UCC21551-Q1 | Reinforced Isolation |
| Isolated Driver | UCC5350L-Q1 | Reinforced Isolation |
| Hall sensor | TMCS1133-Q1 | Replace CT |
| Bidirectional GaN | LMG3660-Q1 | |

## 4 Summary

This application note has analyzed seven distinct designs for pre-charging DC-link capacitors. The conventional design, characterized by large power resistors, exhibits the lowest power density, while the bidirectional HV-LV DCDC ranks highest in this aspect. Regarding bill of materials (BOM) cost, the conventional design ranks highest. Table 4-1 lists a comprehensive comparison of each design across various parameters including BOM cost, power density, and power loss.

**Table 4-1. Pre-charge Designs**

| Designs | Original | Isolated Switch Driver | Active Pre-charge Controller | Discrete HV Buck | Independent Isolated DCDC | Bidirectional HV-LV DCDC | Integrated Pre-charge |
|---|---|---|---|---|---|---|---|
| Bom cost | High | High | Medium | Medium | High | Low | Medium |
| Power density | Low | Low | Medium | Medium | Medium | High | High |
| Power Loss | High | High | Low | Low | Low | Low | Low |

## 5 Terminology

HEV/EV - Hybrid Electric Vehicles and Electric Vehicles

HV - High Voltage

PCC - Pre-Charge Contactor

EMR - Electromechanical Relay

MCP - Main Contactor Positive

MCN - Main Contactor Negtive

SSR - Solid-State Relay

## 6 References

1. Texas Instruments, *Why Pre-Charge Circuits are Necessary in High-Voltage Systems*, application brief.
2. Texas Instruments, *TIDA-050080: High-voltage passive pre-charge with overcurrent protection reference design*, reference design.
3. Texas Instruments, *TPSI31P1-Q1 Automotive Active Pre-charge Controller With 17V Isolated Gate Driver and Bias Supply*, data sheet.
4. Texas Instruments, *TPSI31P1-CALC*, calculation tool.
5. Texas Instruments, *LM25037-Q1 Dual-Mode PWM Controller With Alternating Outputs Data Sheet* , data sheet.
6. Texas Instruments, *PMP41078*, product page.

# 7 Revision History

| Changes from Revision * (October 2025) to Revision A (April 2026) | Page |
|---|---|
| • Updated the part number of isolator and added the hyperlink | 10 |

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