Application Note

Leveraging 8-Pin MSPM0 MCU as Laptop PC Watchdog

Ryan Kim *Korea Sales – Major Account*

ABSTRACT

This application note introduces a low-power laptop PC watchdog implementation using the MSPM0C1103 8-pin MCU. It also demonstrates how to remap the two SWD pins as GPIO (or SPI/Timer) to overcome the device's limited pin count. By remapping these pins, a total of six usable pins become available: three dedicated to the watchdog function (WDT signal input, power-button input, and reset-signal output) and three that can be configured as UART, I²C, SPI, or GPIO.

Compared to a conventional Watchdog (Reset) IC, this MCU-based approach enables users to add more advanced features through firmware and leverage various communication interfaces, providing significantly greater flexibility and functional benefits.

This solution also uses a timer in capture mode to implement the watchdog functionality while maximizing low-power operation in STANDBY0 mode.

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

A watchdog IC is typically used in laptop PCs to monitor the Embedded Controller (EC). The EC periodically sends a square-wave or similar signal to indicate normal operation. If the EC becomes unresponsive, the square-wave signal stops, causing the line to remain stuck at either a logic high or low level. In such cases, the PC user usually presses the power button to reset the system.

The MSPM0C1103 8-pin MCU is one of the smallest and most cost-effective devices available (part number: MSPM0C1103S8YCJR), helping minimize both cost and PCB footprint. Despite its compact size, the MSPM0C1103 offers rich peripherals such as UART, I²C, SPI, and GPIO, allowing users to easily add more functionality. For example, it can send reset information to EC via UART after performing a system reset. In addition, users can update firmware using the secondary BSL without requiring a hardware debugger (SWD).

Compared to a conventional watchdog (reset) IC which typically provides fixed or limited reset behavior, the MCU-based approach allows users to add more advanced features through firmware customization. Users can also take advantage of multiple communication interfaces (UART, I²C, SPI) to log system events, report reset reasons, interact with the EC, or support advanced diagnostics, making the solution far more flexible and beneficial.

The MSPM0 series is based on the Arm® Cortex®-M0+ core and supports SWD (Serial Wire Debug) for debugging and flashing. By default, SWD is enabled and occupies two pins (SWDIO and SWCLK). While this is not an issue for devices with many pins, it becomes a limitation for the 8-pin MSPM0C1103, where only four pins remain available for user functions. For simple applications this may be acceptable, but for designs requiring additional capability, the SWD pins can be remapped as GPIO, SPI, or Timer to maximize the MCU's functionality.

However, users must be aware that once SWD is disabled in SysConfig (control panel, CCS IDE), it cannot be re-enabled after power-up (RUN mode, refer to section 2.4 System Controller in the TRM). This means that program data in flash memory cannot be read back or verified, which may cause issues during mass production. To address this, it is important to distinguish between the pre-programming state (standalone, not mounted on the PCB) and the watchdog running state (mounted on the PCB), and determine whether SWD should be enabled or disabled through firmware logic rather than only through SysConfig.

Please download Example codes from this link: https://e2e.ti.com/cfs-file/__key/communityserver-discussions-components-files/908/Laptop_5F00_PC_5F00_WDT_5F00_IC_5F00_MSPM0C1103SDSGR_5F00_v1.zip .

2 Detailed Description

2.1 Block Diagram

The following figure shows the system block diagram for the notebook PC watchdog supervisor.

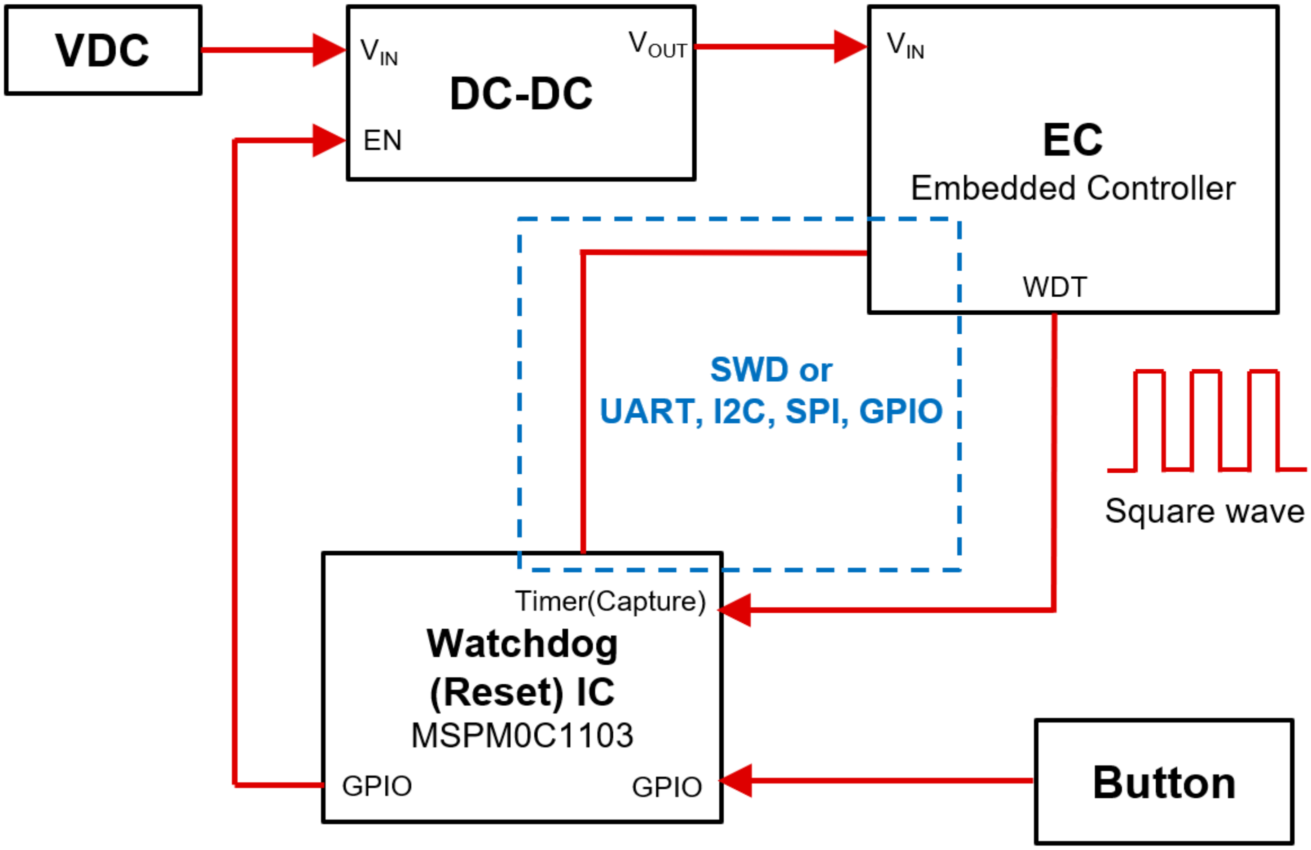

Figure 2-1. System Block Diagram

2.2 Typical Application Schematic

TI recommends connecting a combination of a 10-µF and a 0.1-µF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used but can affect the supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins (within a few millimeters).

PA1 and NRST are double bonded for some variants. If it's used as a NRST, it must connect an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor.

Reset (Output) pin is connected with Enable pin of DC-DC IC. Typically, we use a 10 kΩ resistor, but please use a proper resistor based on the user’s circumstances.

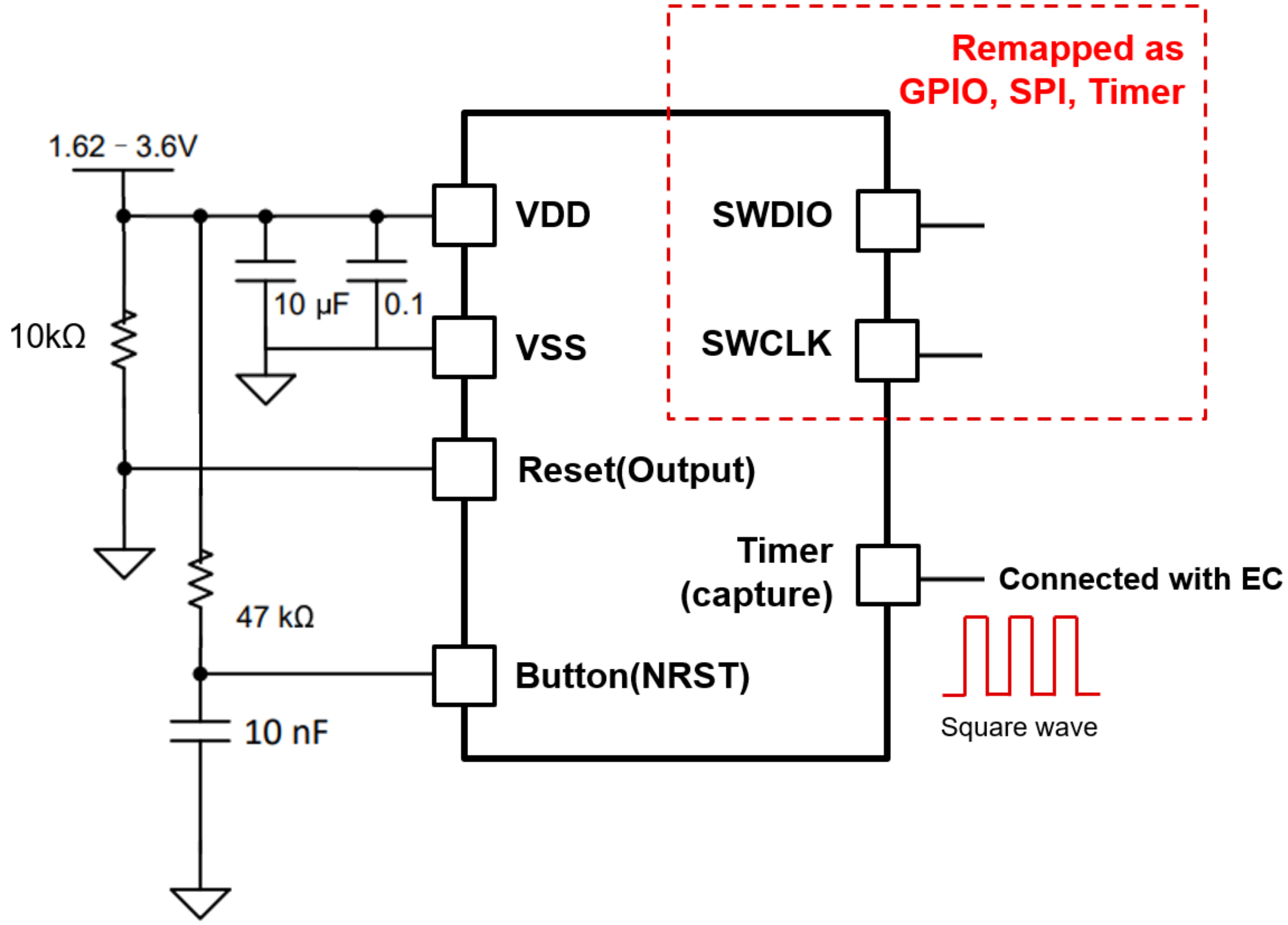

Figure 2-2. Typical Application Schematic

2.3 Flow Chart

2.3.1 Flow Chart - SWD is Activated

If the user does not require complex functionality, it is not necessary to remap the SWD pins as GPIO, SPI, or Timer pins.

The following flowcharts illustrate the operation when SWD is activated.

The system consists of four parts: the main function, GPIO ISR, Timer(capture) ISR, and WDT ISR.

Button input recognition is based on a GPIO interrupt. To further enhance system stability, a fallback mechanism is also implemented. MSPM0C1103’s WDT module is modified to operate like a general timer, allowing the system to check the pin status every 7.81 ms (polling).

The fallback system is optional, so the user may remove this feature if not required.

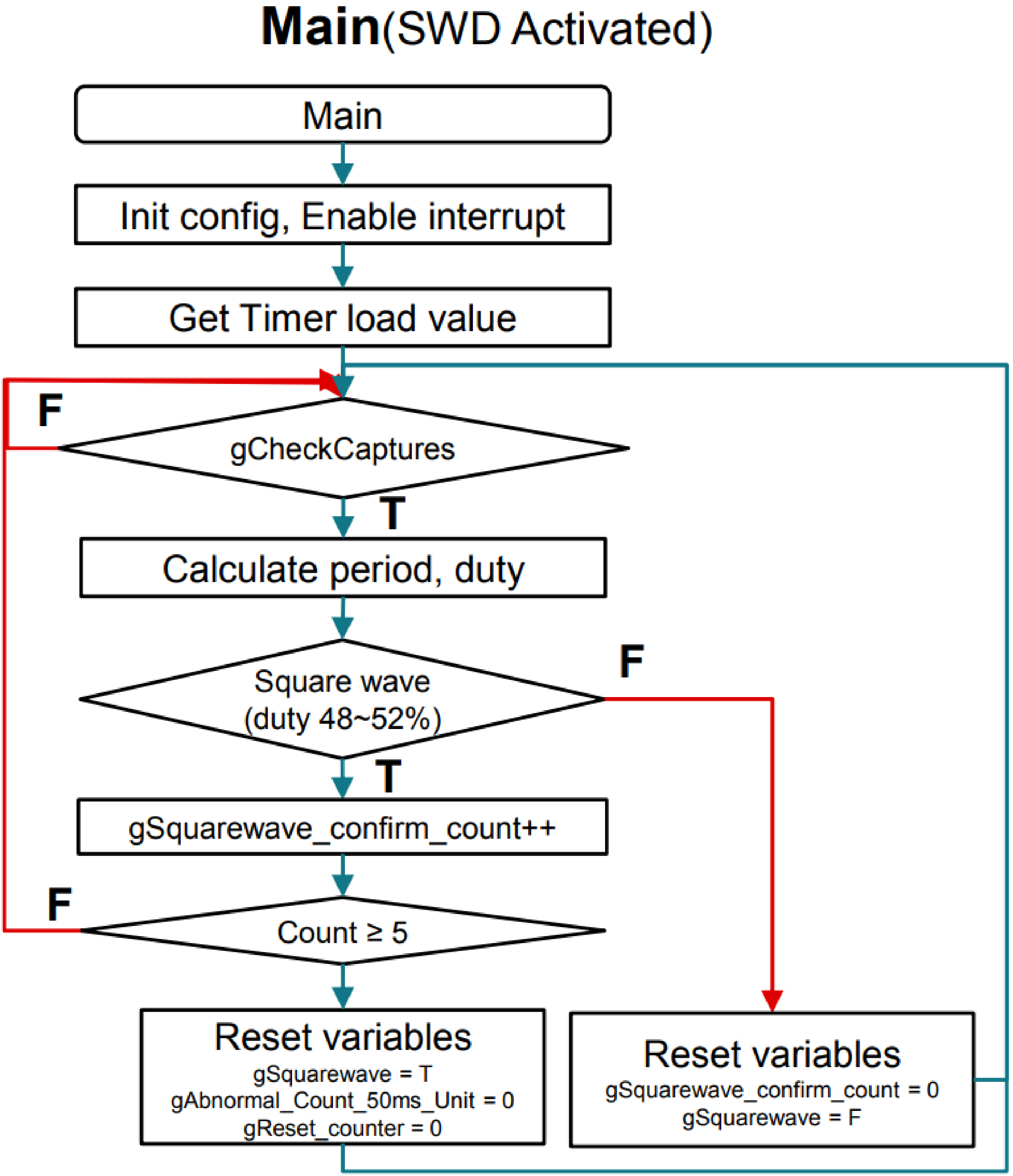

Figure 2-3. Main Function (SWD Activated) Flow Chart

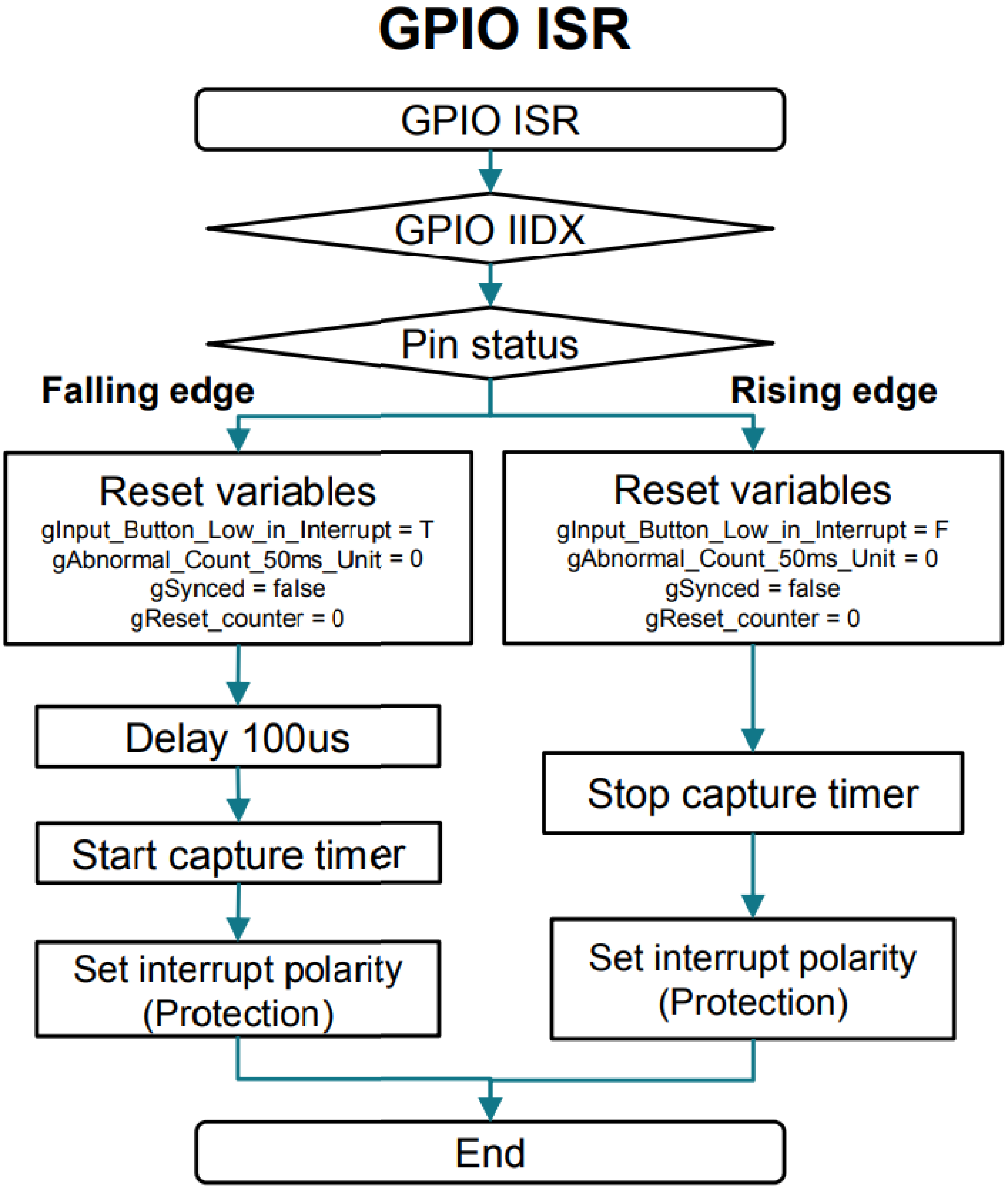

Figure 2-4. GPIO Interrupt ISR Flow Chart

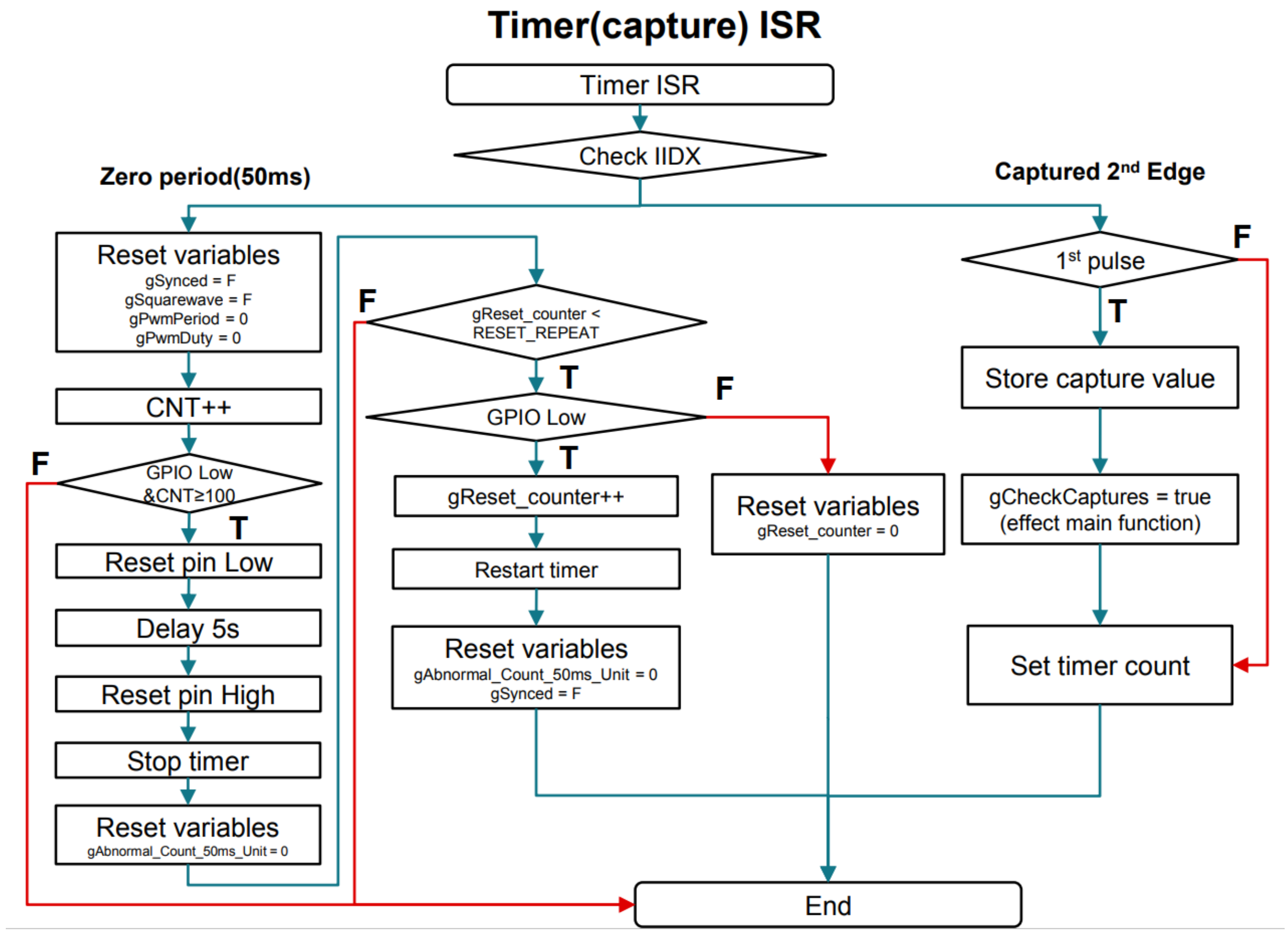

Figure 2-5. Timer Interrupt ISR Flow Chart

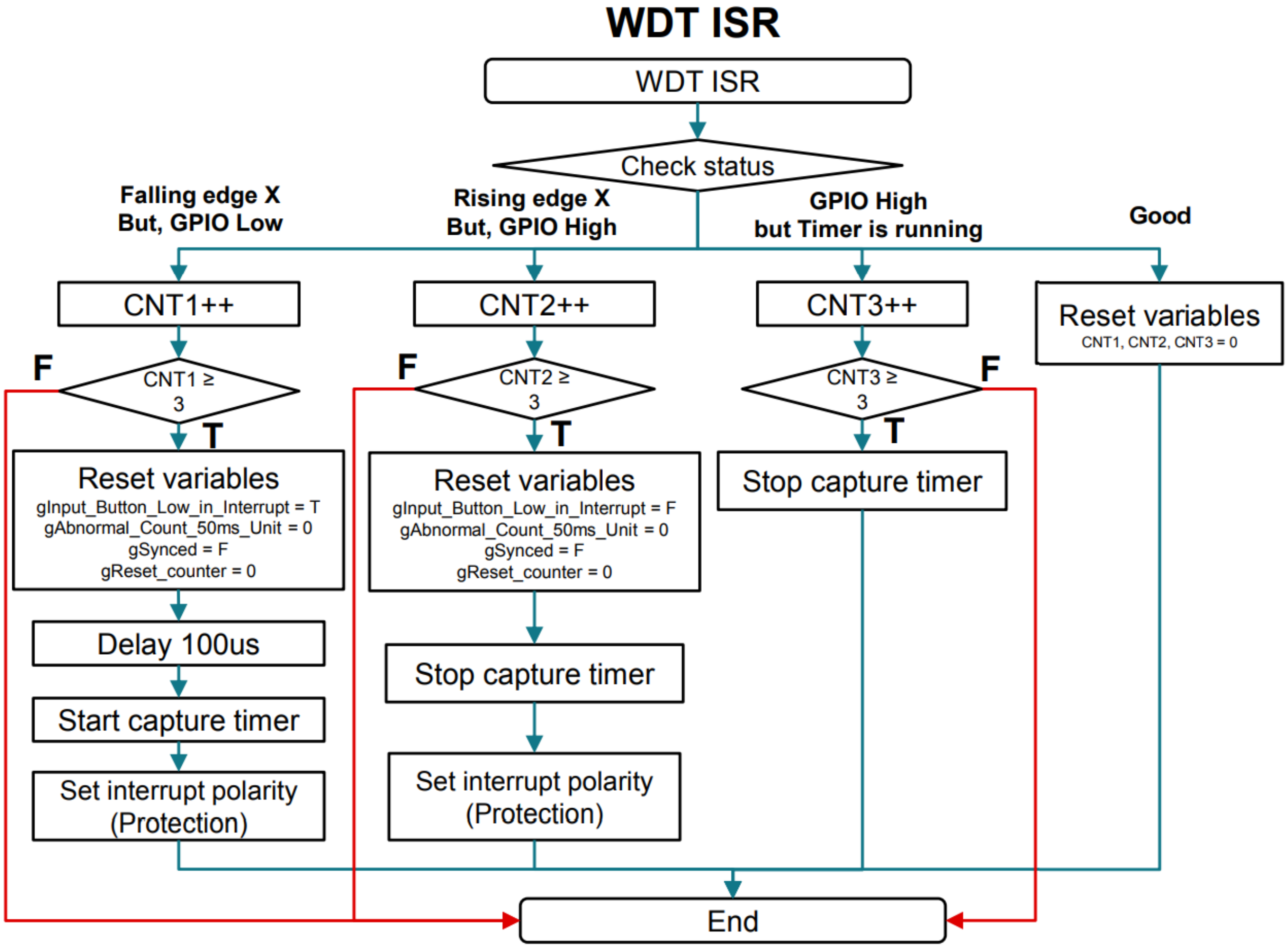

Figure 2-6. WDT Interrupt ISR Flow Chart

2.3.2 Flow Chart - SWD Pins are Remapped to GPIO

The flow is similar to when SWD is activated. The GPIO ISR, Timer (capture) ISR, and WDT ISR remain the same. However, the main function differs in two major aspects. First is check reset pin status and Second is remapping pin in main function.

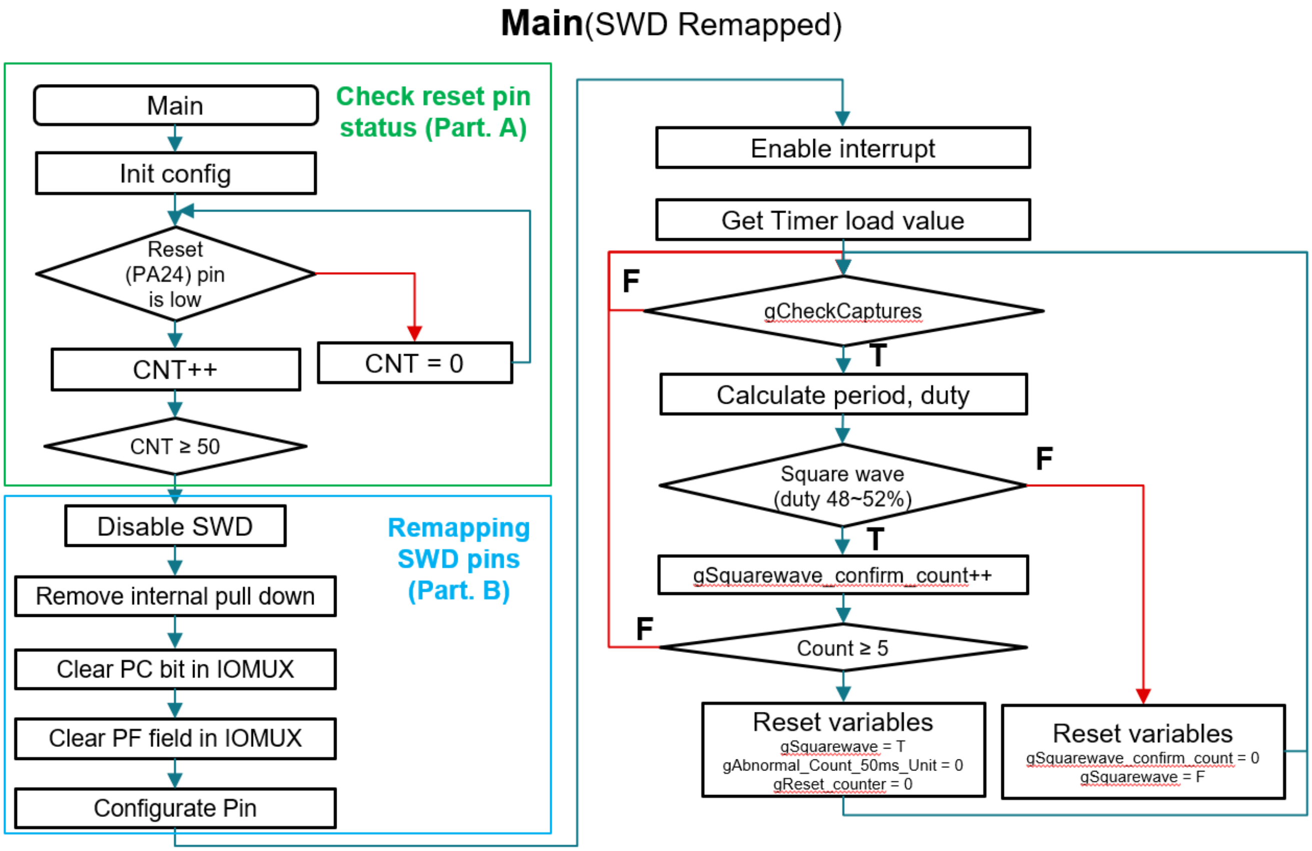

Figure 2-7. Main Function (SWD remapped) Flow Chart

Check reset pin status (Part. A): If the MSPM0C1103 is installed on the PCB, its RESET pin (PA24-output, not NRST) is connected to an external pull-up resistor. At startup, configure the RESET pin (PA24-output, not NRST) as an input with an internal 40 kΩ pull-down resistor enabled, and check the GPIO input level of the pin.

- Input High → Indicates that the MSPM0C1103 is mounted on the PCB (Watchdog running state).
- Input Low → Indicates that the MSPM0C1103 is in a standalone (pre-programming state).

If the MSPM0C1103 determines that it is in the PCB-installed state (Input High), exit the detection loop. Or not Input Low), stay in the loop and keep with SWD enabled to read back and verify FW.

```
Check reset pin status (Part. A) example code

/* Check wheather go to debug mode. Check the Reset pin level */
/* Debug mode - SWD enabled */
if (GPIO_Output_Reset_PIN != (DL_GPIO_readPins(GPIO_Output_PORT, GPIO_Output_Reset_PIN))) {
    while (1) {
        /* If Reset(EC) pin is high x 50 times -> go to Reset function */
        if (GPIO_Output_Reset_PIN == (DL_GPIO_readPins(GPIO_Output_PORT, GPIO_Output_Reset_PIN))) {
            gDebug_escape_counter++;
            if (gDebug_escape_counter >= 50) {
                break;
            }
        }
        else {
            gDebug_escape_counter = 0;
        }
    }
}
```

Remapping SWD pins (Part. B): After detection, disable the SWD function, reset the IOMUX configuration, and reconfigure the pin as required. For more details, refer to Chapter 9.2: IOMUX Operation in the MSPM0 C-Series

24 MHz Microcontrollers Technical Reference Manual. MSPM0 C-Series 24 MHz Microcontrollers Technical Reference Manual.

```
Remapping SWD pins (Part. B) example code

/* Defines for Reset2: GPIOA.20 with pinCMx 21 on package pin 7 */
#define GPIO_Output_Reset2_PIN                                 (DL_GPIO_PIN_20)
#define GPIO_Output_Reset2_IOMUX                            (IOMUX_PINCM21)

/* Application mode - SWD disabled, Reset pin becomes GPIO Output */
DL_SYSCTL_disableSWD();

/* Initialize Reset Pin direction from input to output */
/* Refer TRM in '9.2.1 Peripheral Function (PF) Assignment' */

// 1st remove internal pull down resistor
DL_GPIO_setDigitalInternalResistor(GPIO_Output_Reset_IOMUX, DL_GPIO_RESISTOR_NONE);

// 2nd clear the PC bit
IOMUX -> SECCFG.PINCM[GPIO_Output_Reset_IOMUX] &= ~(IOMUX_PINCM_INENA_MASK | IOMUX_PINCM_PC_MASK);

// 3rd clear the PF field
IOMUX -> SECCFG.PINCM[GPIO_Output_Reset_IOMUX] &= ~(IOMUX_PINCM_PF_MASK);

// 4th restart reset pin
DL_GPIO_initDigitalOutput(GPIO_Output_Reset_IOMUX);
DL_GPIO_setPins(GPIOA, GPIO_Output_Reset_PIN); // Reset pin init condition - High
DL_GPIO_enableOutput(GPIOA, GPIO_Output_Reset_PIN);

/* Initialize Reset inform pin(Remap from SWD) */
DL_GPIO_initDigitalOutput(GPIO_Output_Reset2_IOMUX);
DL_GPIO_setPins(GPIOA, GPIO_Output_Reset2_PIN);
DL_GPIO_enableOutput(GPIOA, GPIO_Output_Reset2_PIN);
```

2.4 Test Result

- Condition: Square wave with 5ms period
- Waveform:

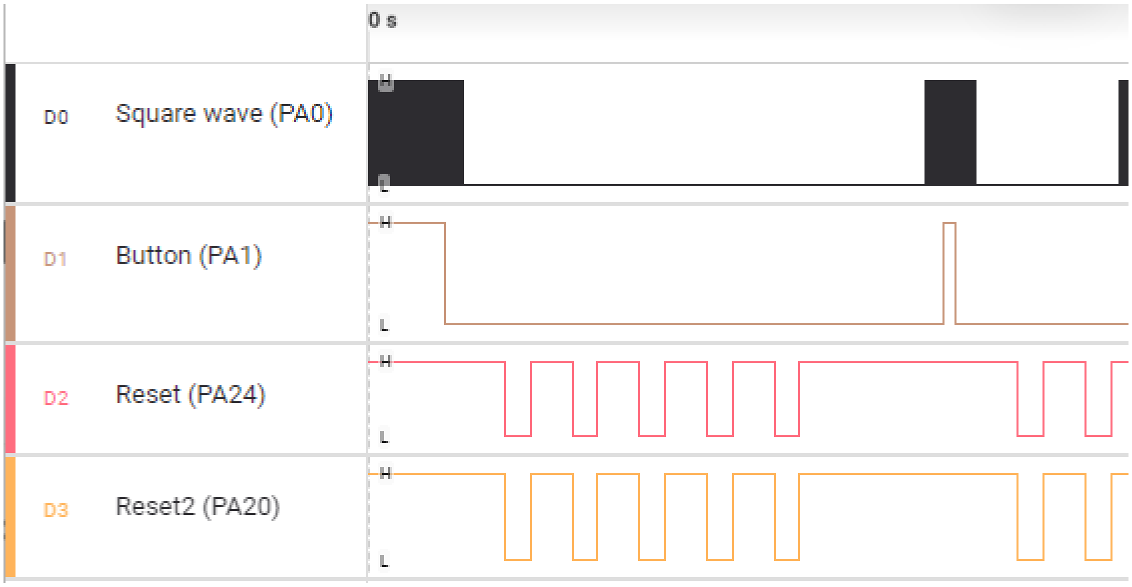

Figure 2-8. SWD Remapped – Laptop_PC_WDT_IC_SWD_Remapped_MSPM0C1103SDSGR_v1

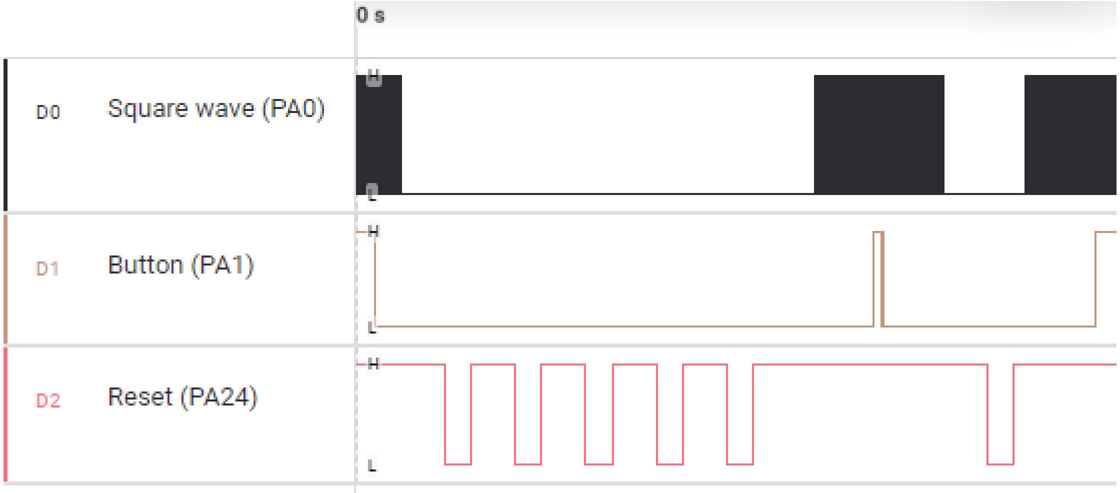

Figure 2-9. SWD Activated – Laptop_PC_WDT_IC_SWD_Activated_MSPM0C1103SDSGR_v1

3 Summary

This document provides a watchdog (reset) IC solution for laptop PCs that monitors the status of the EC (Embedded Controller) and performs an EC reset by toggling the Enable pin of the DC-DC component.

The user can select either the SWD activated (Normal) mode or the SWD remapped (Compact) mode. In SWD remapped mode, two SWD pins are remapped as GPIO, SPI, or Timer pins, allowing the user to utilize up to six functional pins on an 8-pin MCU. This helps minimize both cost and PCB footprint.

In addition, a fallback mechanism is implemented to handle cases where the interrupt is not detected, thereby improving overall system stability.

4 References

- MSPM0 SDK 'timx_timer_mode_capture_duty_and_period' - https://dev.ti.com/tirex/explore/node?node=A__AESmksLo7OFHYDsNXaAhjg__MSPM0-SDK__a3PaaoK__LATEST
- Using MSPM0 as a Watchdog Timer - https://www.ti.com/lit/sd/slaaer8/slaaer8.pdf?ts=1761930719336&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FMSPM0G3507%253FkeyMatch%253DMSPM0G3507%2526tisearch%253Duniversal_search%2526usecase%253DGPN
- MSPM0 C-Series 24-MHz Microcontrollers Technical Reference Manual (Rev. C) - https://www.ti.com/lit/ug/slau893c/slau893c.pdf?ts=1762235733312&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252Fko-kr%252FMSPM0C1103

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025