Application Note

VCO Design Basic and Key Parameter for GSM Application

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ABSTRACT

This application note describes the design and measurement of a VCO (Voltage Controlled Oscillator) that meets the phase noise specification for GSM band applications, a key specification. This begins with the role of PLLs and VCOs in a transmitter, and then explains the function of each block, including the VCO frequency range, varactor, and capacitor bank. This note is for users who want to understand the basic operating principles of clock devices such as VCOs and PLLs, as well as the simple chip fabrication process. RF PLLs that meet the phase noise specification for the GSM band include the LMX family (LMX2820, LMX2594, and so on.)

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Trademarks

1 Introduction

This application note demonstrates VCO basic theory, key factors and how to design a LC CMOS VCO. This note is structured as follows. Section 2 describes the basic theory of VCOs and the factors that determine performance. Section 3 describes the structure of a CMOS LC VCO that satisfies four bandwidths, the circuitry and operating principles of each block, the layout, and the evaluation results of the fabricated chip. Finally, Section 4 concludes this note.

Figure 1-1 shows the transmitter structure, including the VCO. In a PLL, the VCO receives the VTUNE voltage and outputs the desired frequency.

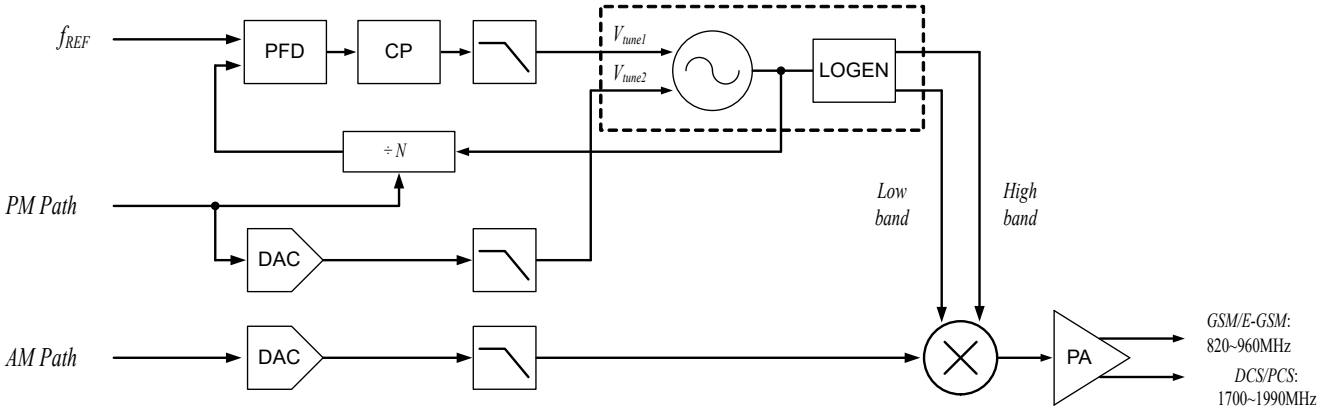

Figure 1-1. Transmitter TOP Block Diagram

2 VCO Basic Theory and Key Factors

2.1 VCO

Most communication systems require an oscillator with a controllable output frequency. This is achieved by applying an input signal to the oscillator to produce the desired output frequency. An oscillator whose output frequency varies with the input voltage is called a VCO (Voltage Controlled Oscillator). An ideal output frequency of the VCO varies consistently with the input voltage, as expressed by Equation 1

$$f_{out} = f_0 + K_{VCO} \times V_{tune} \quad (1)$$

In Equation 1, f_0 represents the state when the V_{tune} voltage is 0. K_{VCO} represents the gain or sensitivity of the VCO, expressed as the rate of change in output frequency with changes in the V_{tune} voltage. Figure 2-1 shows the operating characteristics of a VCO.

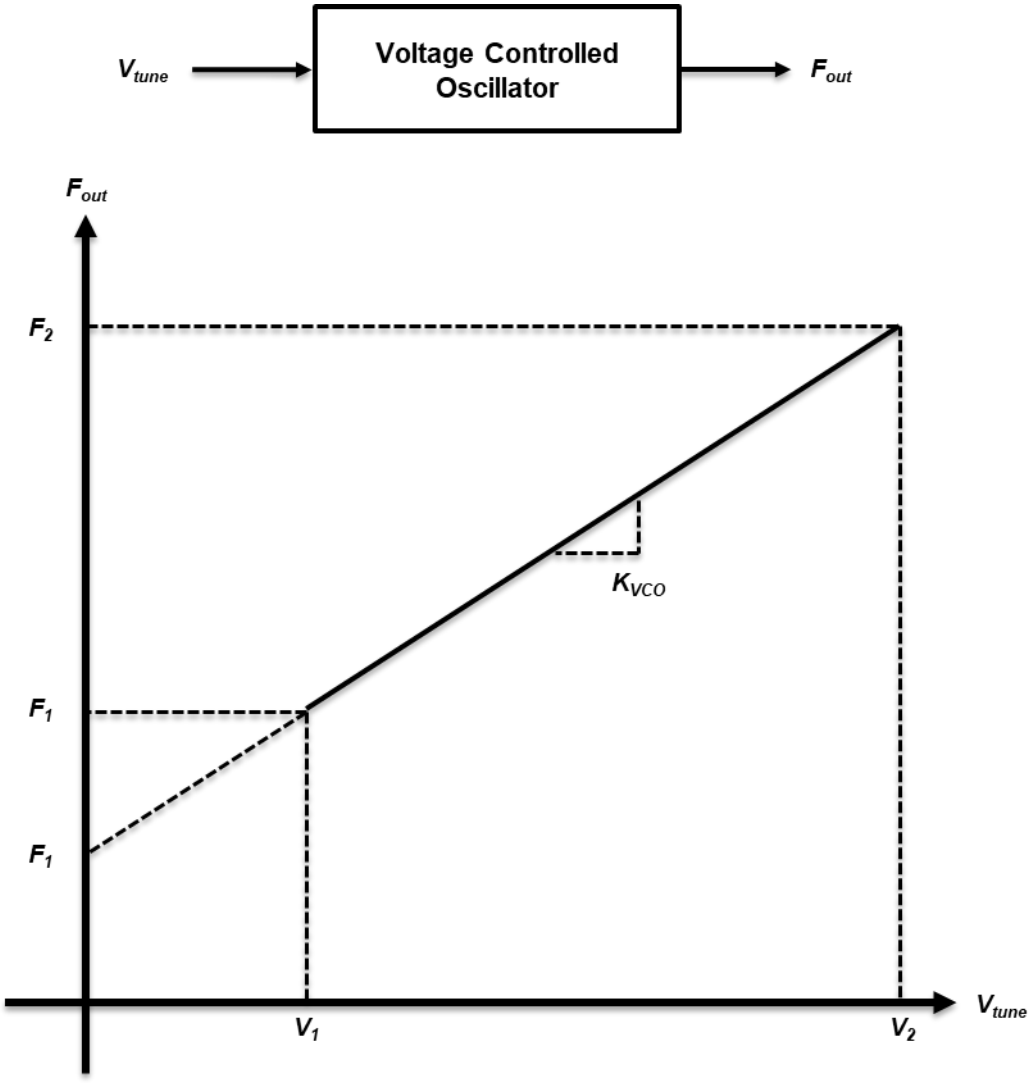

Figure 2-1. VCO Basic Definition and Characteristic Curve

2.2 VCO Frequency Range

The VCO frequency range is determined by the center frequency of the VCO and the resulting frequency variation. The range of output frequency variation according to the voltage applied to the VCO determines the overall frequency range of the VCO. Several factors must be considered when determining the VCO frequency range. One is the variation of the VCO center frequency due to process and temperature variations, and the other is the frequency range required by the applicable system. These two factors determine the overall VCO frequency range.

Figure 2-2 shows the VCO frequency plan for 2G communications, calculated considering the division ratio of the final output stage. 2G communications include GSM, EGSM, DCS, and PCS.

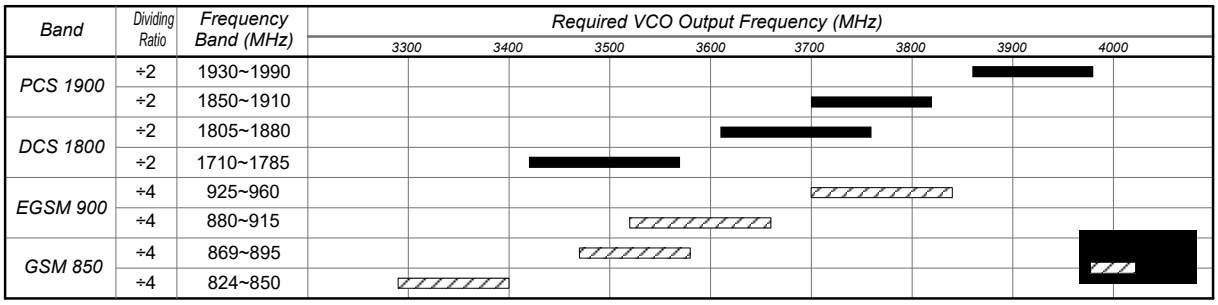

Figure 2-2. System Frequency Range and VCO Frequency Range Plan

2.3 Phase Noise

Phase noise refers to unwanted energy sources, not signal components, that appear near the desired frequency. The primary sources of phase noise are thermal noise and 1/f noise. Phase noise is measured in the frequency domain and is expressed as the ratio of the noise component to the signal output within a 1Hz bandwidth at a point offset from the center frequency. The unit is dBc/Hz.

Phase noise is a critical design factor in VCO design. Each VCO must satisfy the system phase noise requirements. According to the GSM05.05 standard, the final VCO phase noise must be calculated using equations appropriate for in-band and out-of-band.

For in-band, the specification is -60dBc/30kHz at a 400kHz offset. To convert this value to dBc/Hz, the VCO phase noise unit, use Equation 2

$$\mathrm{dBc/Hz} = \mathrm{dBc} - 10\mathrm{kog}(\mathrm{BW}) - 8 \tag{2}$$

Converting the given value at a 400kHz offset frequency to VCO phase noise yields 11.8dBc/Hz. The value converted from dBc/BW is a GMSK modulation value. Therefore, a difference of 8dBc occurs during the conversion to continuous wave.

For out-of-band, the specification is -79dBm/100kHz at a 20MHz offset frequency. To convert the given value to dBc/Hz, the VCO phase noise unit, use Equation 3

$$\mathrm{dBc/Hz} = \mathrm{TXMaxPower} + \mathrm{TXPowerLevel} - 10\log(\mathrm{BW}) \tag{3}$$

Converting the given value at a 20MHz offset to VCO phase noise yields -162.0dBc/Hz. For out-of-band, the maximum transmitter power (33dBm) must be taken into account. The GSM band phase noise determined through these conversions is shown in Table 2-1.

Table 2-1. GSM Band Phase Noise Requirements

Band	Offset Frequency	GSM05.05 Specification	Converted Phase Noise
GSM	400kHz	-60dBc/30kHz	-112.8dBc/Hz
	10MHz	-67dBm/100kHz	-150.0dBc/Hz
	20MHz	-79dBm/100kHz	-162.0dBc/Hz

3 CMOS LC VCO Design

3.1 PLL Structure

Figure 1-1 shows the basic blocks of a transmitter. To synthesize a digital signal into an RF signal, a VCO (Variable Coefficient of Frequency) and a PLL (Phase-Like Loop) are essential.

3.2 LC VCO Structure and Operation

Figure 3-1 shows a basic CMOS LC VCO circuit diagram. This circuit diagram was designed to satisfy the GSM band using a single-stage VCO. It uses a cross-coupled negative-GM structure and generates a negative-GM signal for oscillation. A low-pass filter consisting of R1 and C1 was designed to block noise from the current mirror. L1, L2, and C2 were designed to minimize harmonic components generated at the VCO common-mode node and thermal noise from the MOSFET.

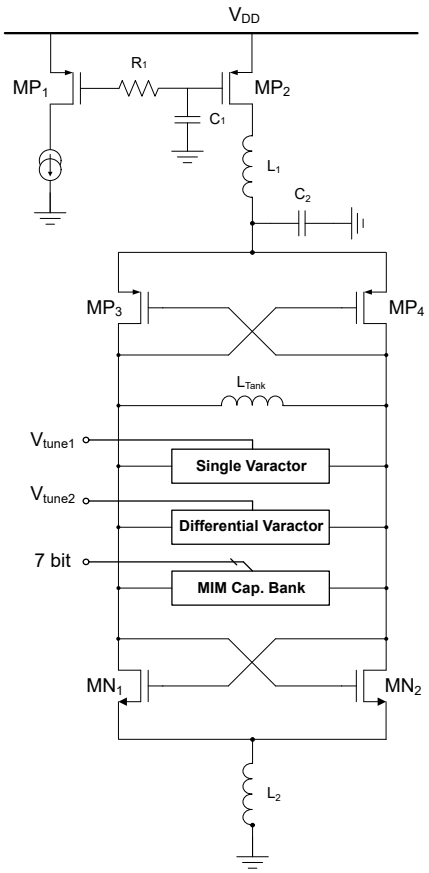

Figure 3-1. VCO Schematic

The capacitor bank of the LC tank, which determines the resonant frequency, consists of a variable-capacitance diode port and a MIM capacitor bank that can be digitally adjusted to satisfy a wide frequency range. The MIM capacitor bank is designed with a 7-bit binary weighting structure. The 7-bit MIM capacitor bank maintains a low K_{VCO} value while satisfying a wide frequency range. Consequently, the low K_{VCO} also reduces the overall VCO phase noise, resulting in improved overall performance. The oscillation frequency of the LC VCO is determined by Equation 4

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (4)$$

The VCO output frequency is determined by the values of the LC tank's inductor and capacitor. Because frequency adjustment by varying the inductor value in a CMOS process is difficult, the desired oscillation frequency can be achieved using a capacitor whose capacitance is relatively easy to vary. Therefore, a variable-capacitance diode for frequency adjustment and an MIM capacitor array that can satisfy a wide frequency range

using digital adjustment are required. And if we also consider the capacitance of the parasitic components considered in the design, the final oscillation frequency formula follows:

$$f_c = \frac{1}{2\pi\sqrt{L(C_{fix} + C_{VAR} + C_{MIM})}} \quad (5)$$

In the above equation, L represents the inductor value of the LC tank, and C_{fix} represents the parasitic component. C_{VAR} represents the value of the variable-capacitance diode, and C_{MIM} represents the value of the digitally controlled MIM capacitor array.

Figure 3-2 shows the variable-capacitance diode circuit for the K_{VCO}. The DC voltage generated through the charge pump and loop filter of the phase-locked loop varies the C_{VAR} capacitance, thereby determining the oscillation frequency of the VCO. A coupling capacitor is used to provide a reference voltage for the variable-capacitance diode.

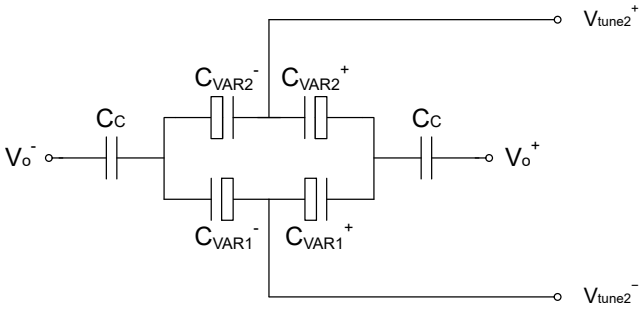

Figure 3-2. Differentially Tuned Varactor

3.3 Each Circuit and Block Operation

3.3.1 Tuning Varactor Bias Circuit

Figure 3-3 $_{BIAS}$ shows the characteristics of a variable capacitor diode according to the V_{BIAS} voltage. The characteristic graph of the variable capacitor diode shifts horizontally toward the V_{tune} voltage depending on the reference V_{BIAS} voltage. Therefore, selecting an appropriate adjustment voltage range and applying a reference voltage is crucial for achieving linearity. Operating the VCO in this linear range yields a relatively wider output frequency adjustment range for the same voltage change than in the nonlinear range.

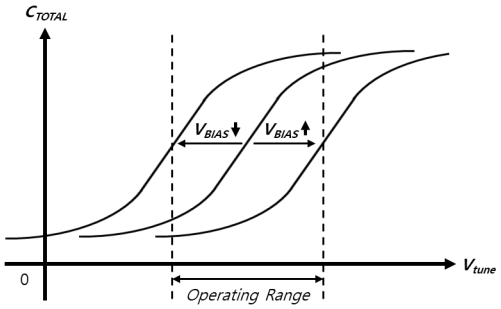

Figure 3-3. Varactor Characteristic Curve with V_{BIAS}

3.3.2 7 Bit MIM Capacitor Bank

Figure 3-4 shows a binary-weighted 7-bit MIM capacitor structure. The 7-bit MIM capacitor array occupies a larger area than a lower-bit MIM capacitor array, but the frequency range required per bit narrows, resulting in a lower K_{VCO} value. Therefore, in a VCO where phase noise is a critical factor, a lower K_{VCO} value can also improve phase noise.

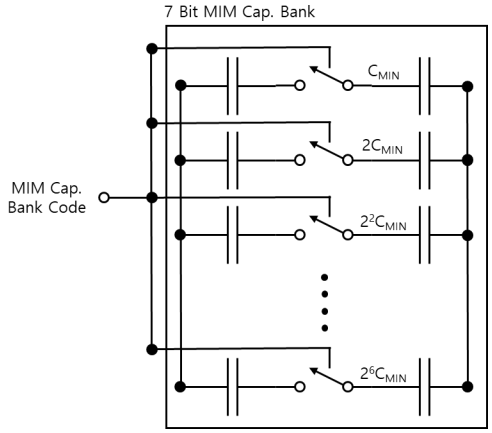

Figure 3-4. Binary Weighted 7 Bit MIM Capacitor Array

3.4 Simulation

Figure 3-5 shows the results of a simulation confirming the VCO frequency range using a variable-capacitance diode and a binary-weighted 7-bit MIM capacitor. The desired range was achieved when V_{tune} was varied from 0.3V to 0.9V.

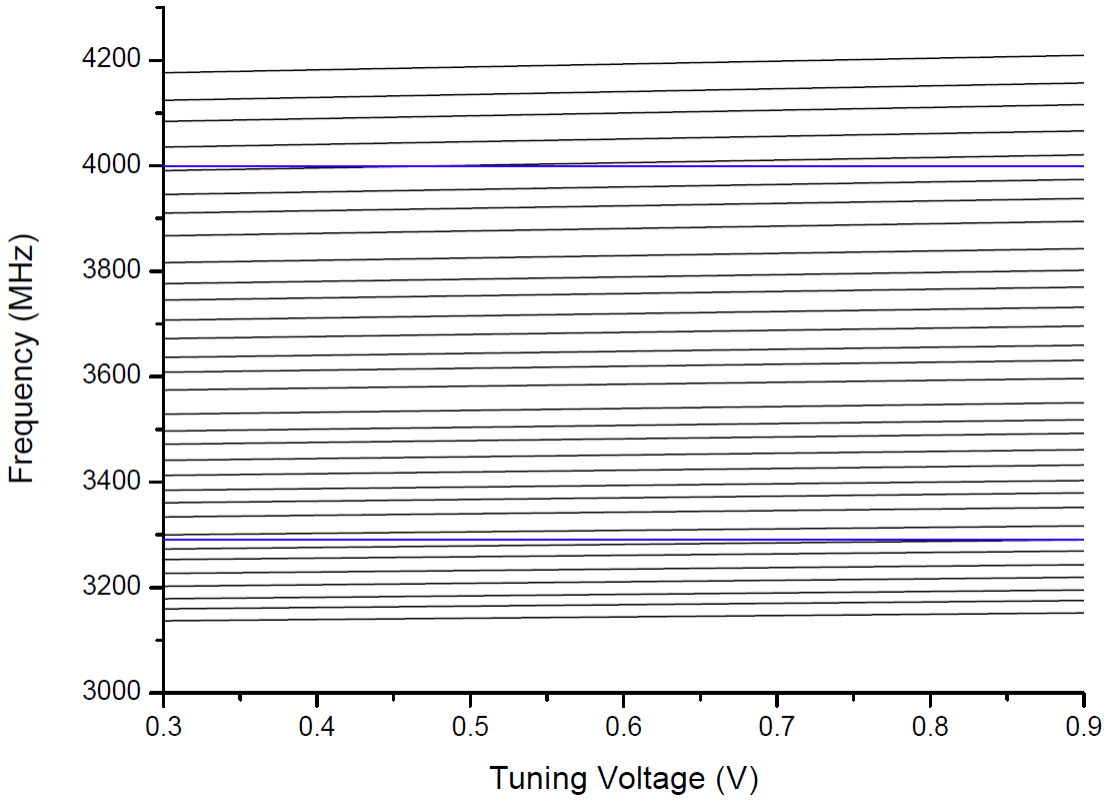

Figure 3-5. VCO Frequency Range Simulation

Figure 3-6 shows the simulation results for phase noise, the most important performance characteristic of a VCO. Phase noise was -113dBc/Hz at a 400kHz offset, -147dBc/Hz at a 10MHz offset, and -155dBc/Hz at a 20MHz offset.

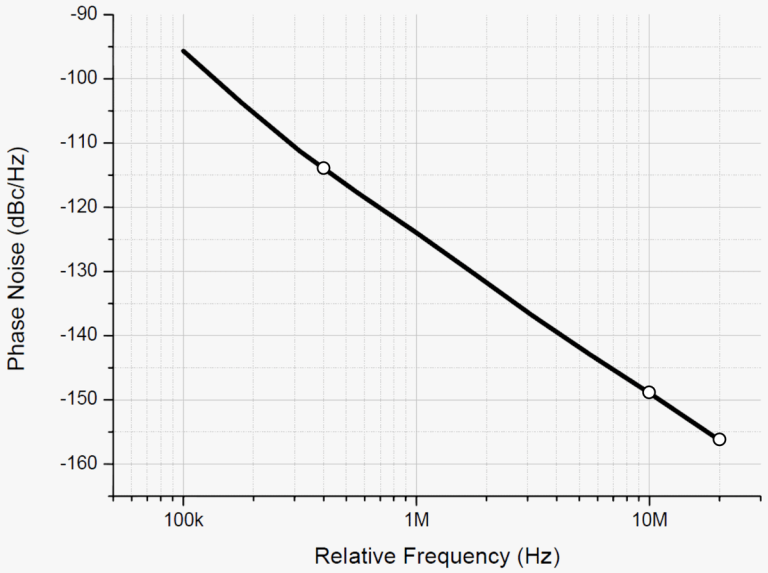

Figure 3-6. VCO Phase Noise Simulation

3.5 Implementation and Measurement Results

3.5.1 Layout

Figure 3-7 shows the layout of the designed chip. Since the cross-coupled LC VCO outputs a differential frequency signal, symmetry was considered in the design. The variable-capacitance diode bank, MIM capacitor bank, and transistor were connected in this order, starting directly below the LC tank inductor. Additionally, the digital control and current control sections were placed to the right of the VCO.

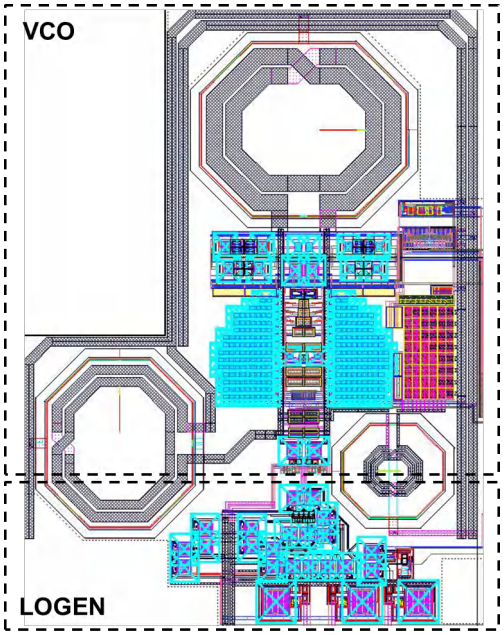

Figure 3-7. VCO and LOGEN Layout

3.5.2 Fabrication and Measurement Results

Figure 3-8 shows the results of frequency range measurements of the LC VCO. The voltage applied to the variable capacitor diode was fixed at 0.6V, and the frequency range was measured by digitally controlling the MIM capacitor bank code. The measured VCO frequency ranged from 2930 to 4150MHz. Figure 3-9 shows the phase noise measurements. The phase noise values were -108.54dBc/Hz at a 400kHz offset and -142.18dBc/Hz at a 10MHz offset from a 3.9GHz output frequency.

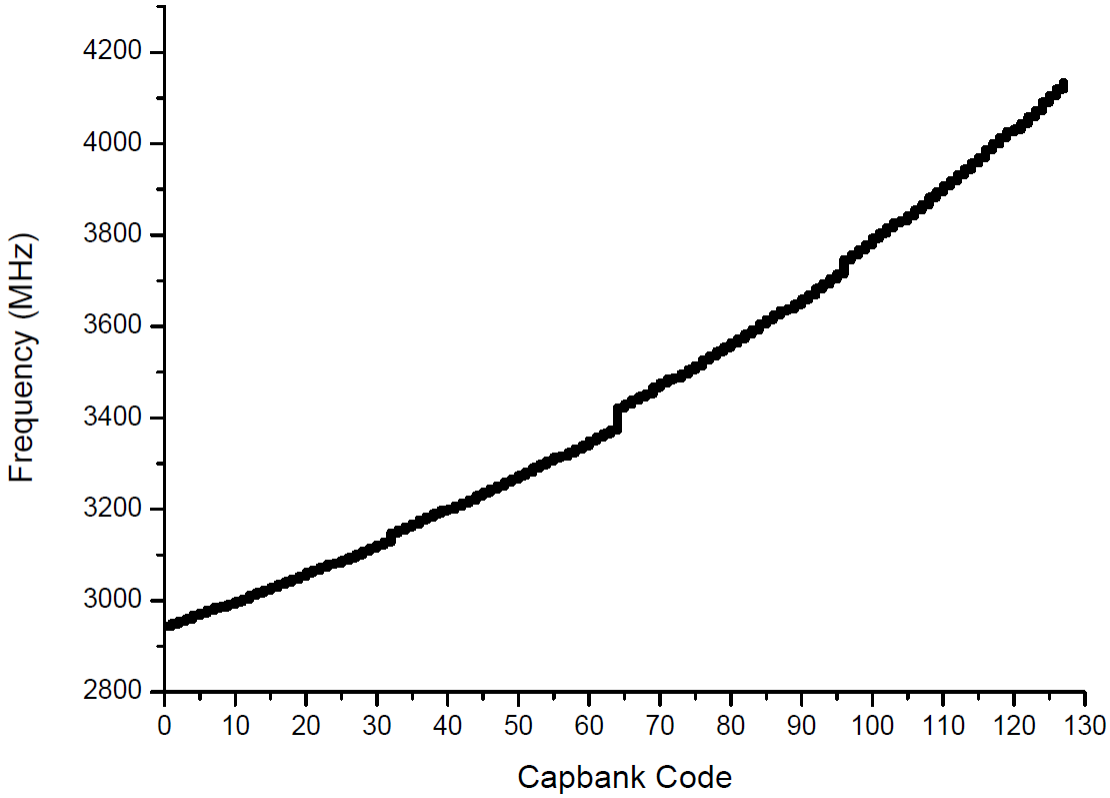

Figure 3-8. Measured VCO Frequency Range

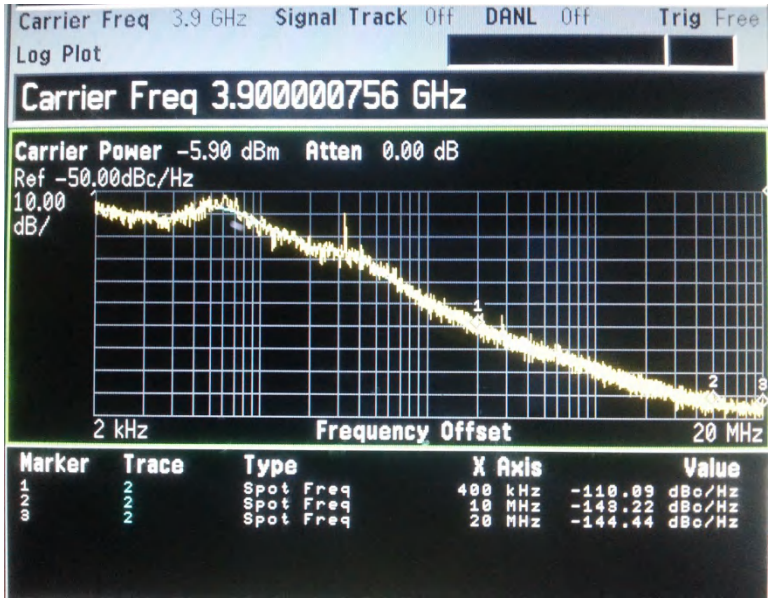

Figure 3-9. Measured VCO Phase Noise

4 Summary

This application note describes the critical elements of VCO design and the process from actual design to measurement. A low-pass filter consisting of R and C elements was designed to remove noise from the current mirror stage. Furthermore, L_1, L_2, and C_2 were used to minimize 1/F, thermal noise, and harmonic components. A differential variable-capacitance diode structure was used to minimize common-mode noise from other circuits. Furthermore, a 7-bit MIM capacitor bank was designed to improve phase noise performance, maintaining a low K_{VCO}.

The LC VCO has a frequency range of 2.93 to 4.15GHz and has a figure of merit of -181.7dBc/Hz at a carrier frequency of 3.9GHz at 10MHz offset.

5 References

1. IEEE, *A Two-Point Tuning LC VCO with Minimum Variation of K VCO2 for Quad-Band GSM/GPRS/EDGE Polar Transmitter in 65-nm CMOS*
2. Texas Instruments, *Fractional/Integer-N PLL Basics*, technical brief.
3. Texas Instruments, *LMX2594 15-GHz Wideband PLLATINUM™ RF Synthesizer With Phase Synchronization and JESD204B Support*, data sheet.
4. Texas Instruments, *LMX2594 EVM Instructions – 15-GHz Wideband Low Noise PLL With Integrated VCO*, user's guide.

6 Revision History

Changes from Revision * (January 2026) to Revision A (April 2026)	Page
• Changed "Voltage Coupled Circuit" to "Voltage Controlled Oscillator"	1

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