*Application Note*

# *A Practical Application Example to Obtain Positive and Negative Output Voltages Using A Single TPS61170*

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**ABSTRACT**

This report introduces a practical application example for the both positive and negative output voltages using the TPS61170, and this is achieved by using two different topologies in parallel with one TPS61170. Inverting Buck-Boost and SEPIC topologies are used to obtain +/- 9V output from the input voltage range from 3V to 18V. The core concept of this approach is to use Inverting Buck-Boost topology for a negative 9V output and SEPIC for a positive 9V output with the wide input voltage range. This approach is also an excellent design for the input supply voltages of TI PMICLOADBOARDEVM (SLUUC92). This application report demonstrates that the proposed application method performs well, as verified through simulation and experimental validation.

## Table of Contents



## Trademarks

# 1 Introduction

The TPS61170 is a monolithic, high-voltage switching regulator with integrated 1.2A, 40V power MOSFET. This device is mainly configured in Boost or SEPIC topologies with 1.2MHz fixed switching frequency, and external loop compensation components provide the application flexibility to optimize the performance.

The Boost topology is widely used when the input voltage is lower than the output voltage, while the SEPIC topology offers a wide operating range in which the input voltage can be either higher or lower than the output voltage. However, these approaches do not always satisfy all of the diverse input and output requirements demanded in system design.

For example, if a 9V output is required from a 12V input, an efficient design can be achieved using a simple buck converter without the need for a SEPIC topology. However, when the output voltage is fixed at 9V and the input voltage varies widely from 3V to 18V, and when both a positive 9V and a negative −9V outputs are required simultaneously, meeting these system requirements can necessitate a more complex circuit and additional control circuitry.

This application note presents a highly efficient and cost-competitive design that implements two output voltages over a wide input voltage range of 3V to 18V using a single TPS61170 device, and Figure 1-1 shows the brief concept of the application.

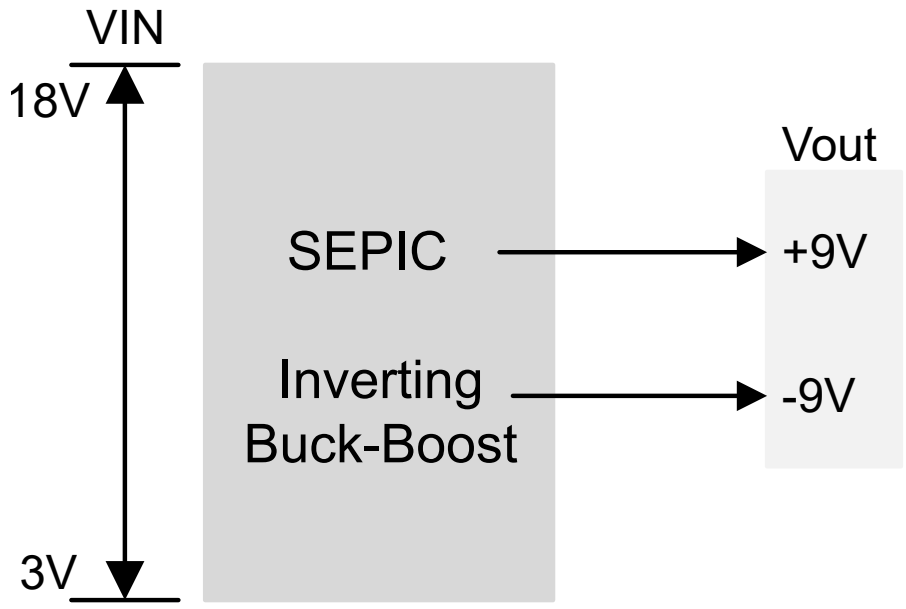


**Figure 1-1. Proposed Concept**

## 2 The Proposed Application Schematic

Figure 2-1 shows the proposed application schematic using the TPS61170 to have the both +9V and -9V from the wide input voltage range. Inverting Buck-Boost is achieved by adding C4 to generate the negative output voltage (-9V) while SEPIC is used for 9V output. The main feedback signal comes from the output of SEPIC converter, and Figure 2-2 shows the main waveforms to achieve the both positive and negative output voltages.

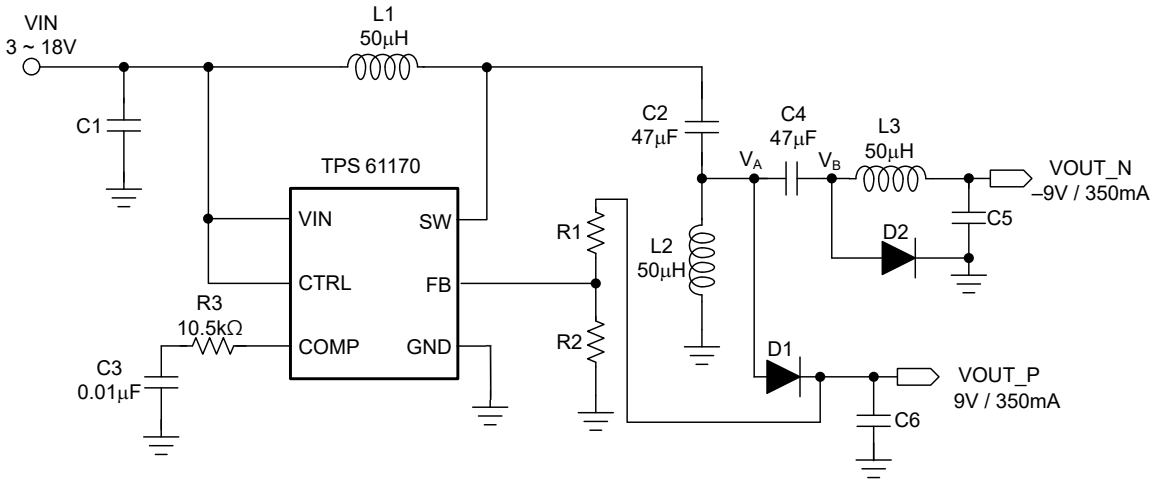


**Figure 2-1. Proposed Application Circuit**

When the internal switch of the TPS61170 is turned on, energy is stored in the inductor L1. Also, when the internal switch is turned off, the input voltage (VIN) and the voltage across L1 ($v_L$) are added together and applied to $V_{SW}$. During the off period of the internal switch, the stored energy in L1 is transferred to the two outputs.

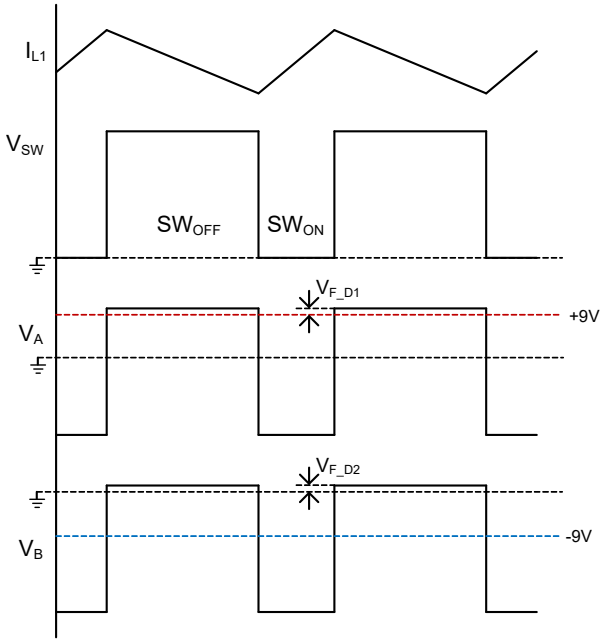


**Figure 2-2. Principal Waveforms of the Proposed Method**

The voltage on SW pin ($V_{SW}$) is given by Equation 1:

$$V_{SW} = VIN + v_L \quad (1)$$

Where:

$$v_L = L\frac{di}{dt} \quad (2)$$

The on-duty ratio at an input voltage of 18V is calculated as shown in Equation 3.

$$D_{on} = \frac{V_{out}}{VIN + V_{out}} = 0.333 \quad (3)$$

The required inductance for L1 is determined by Equation 4:

$$L1 = \frac{VIN \cdot D_{on}}{\Delta I_{pk.to.pk} \cdot f_S} = 47.62\mu H \quad (4)$$

Where:

$$\Delta I_{pk.to.pk} = I_{OUT} \cdot Ripple_{rate(\%)} \quad (5)$$

$$f_S = 1.2MHz(SwitchingFrequency) \quad (6)$$

A value of 50µH was used for L1, and L2 and L3 were also selected to have the same value as L1 in this application. The SEPIC converter is a fourth-order system that incorporates two inductors (L1 and L2) and a coupling capacitor (C2). In CCM (Continuous Conduction Mode), the converter exhibits a right-half-plane zero (RHPZ). Therefore, the crossover frequency must be selected sufficiently lower than the RHPZ frequency to verify stable operation.

Figure 2-3 shows the variation of on-duty ratio and $V_{SW}$ with changes in the VIN voltage. Since the maximum absolute voltage rating on SW pin of the TPS61170 is 40V, sufficient margin must be considered to verify that $V_{SW}$ voltage remains well below 40V, taking into account switching-induced overshoot and PCB layout conditions and so on.

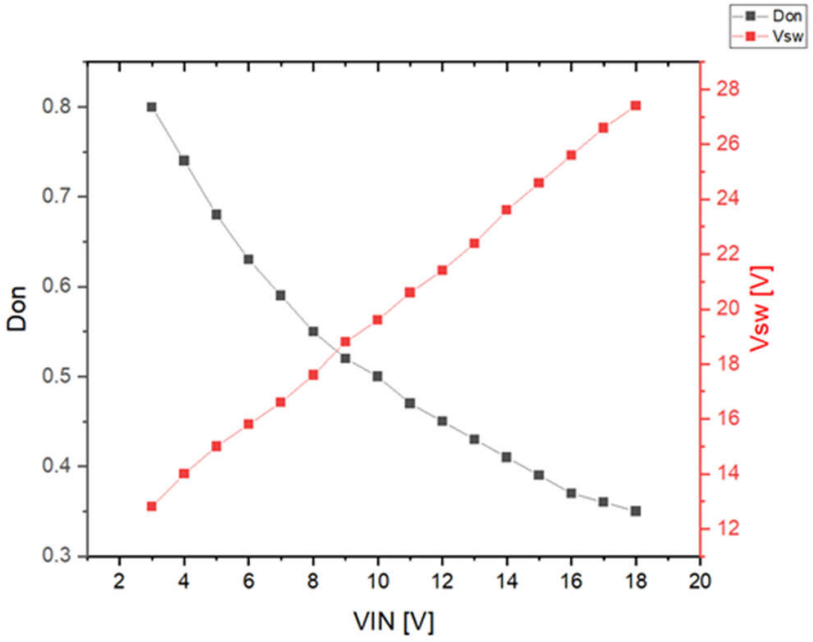


**Figure 2-3. $D_{ON}$ and $V_{SW}$ Variations as VIN Changes**

# 3 Simulation Results

Figure 3-1 shows the simulation results during initial startup. When the input voltage is 12V and the CTRL pin of the TPS61170 transitions from Low to High, the results demonstrate that both 9V and -9V outputs are properly regulated and stabilize normally.

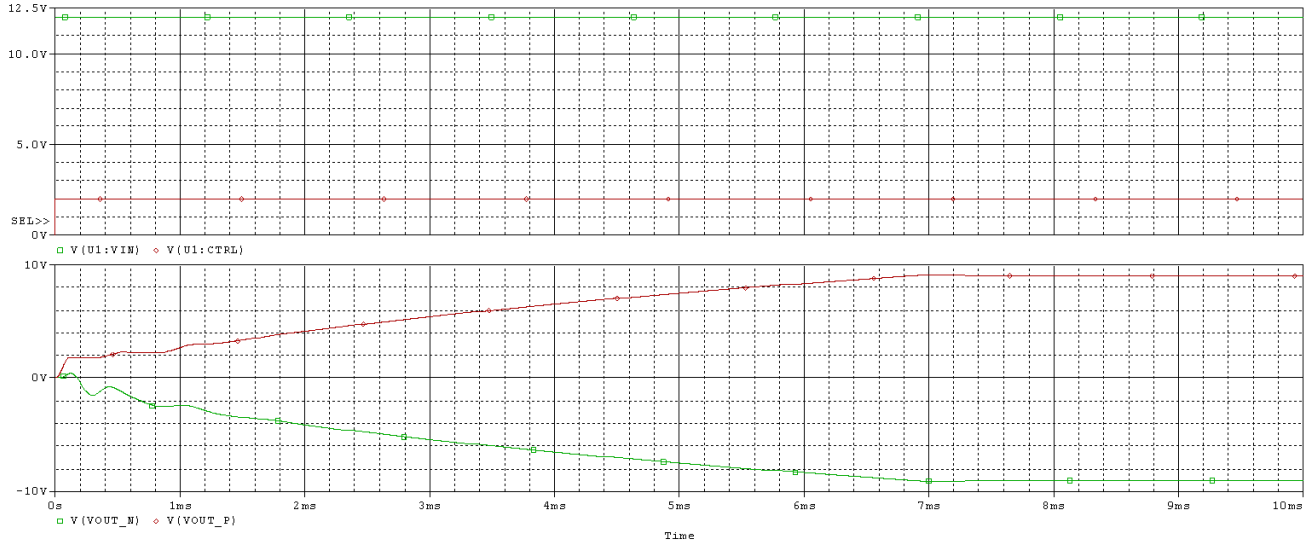


**Figure 3-1. Initial Startup for the Both 9V and -9V**

Figure 3-2 shows the principal current and voltage waveforms in steady-state operation. The 9V and -9V outputs are properly regulated, and the voltage waveforms of VSW, VA and VB are also operating normally at a switching frequency of 1.2MHz. In addition, the inductor current of L1 is observed to operate in CCM.

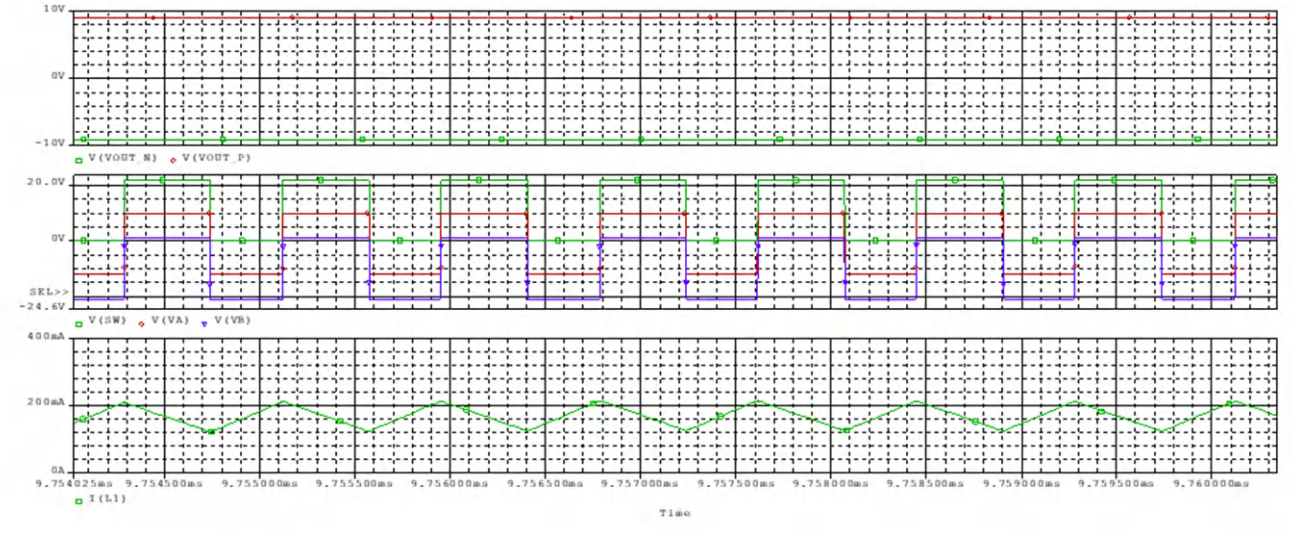


**Figure 3-2. Principal Waveforms Under Steady-State Operation**

# 4 Experimental Results

Figure 4-1 shows the experimental results (VIN: Ch1 in blue with 2V/div, $V_{OUT\ (+9V)}$ : Ch2 in light blue with 5V/div, $V_{OUT\ (-9V)}$: Ch3 in purple with 5V/div, $I_{L1}$: Ch4 in green with 0.5A/div), demonstrating that both output voltages (9V and -9V) are properly regulated at an input voltage of 3V. Ch4 represents the current flowing through L1. Since the internal MOSFET current limit of the TPS61170 is minimum 0.96A, the output load must be carefully considered to make sure that this limit is not exceeded.

In addition, during initial startup, the output current is required not only to supply the output load but also to charge the output capacitors, resulting in a higher inductor current than that under normal steady-state operation.

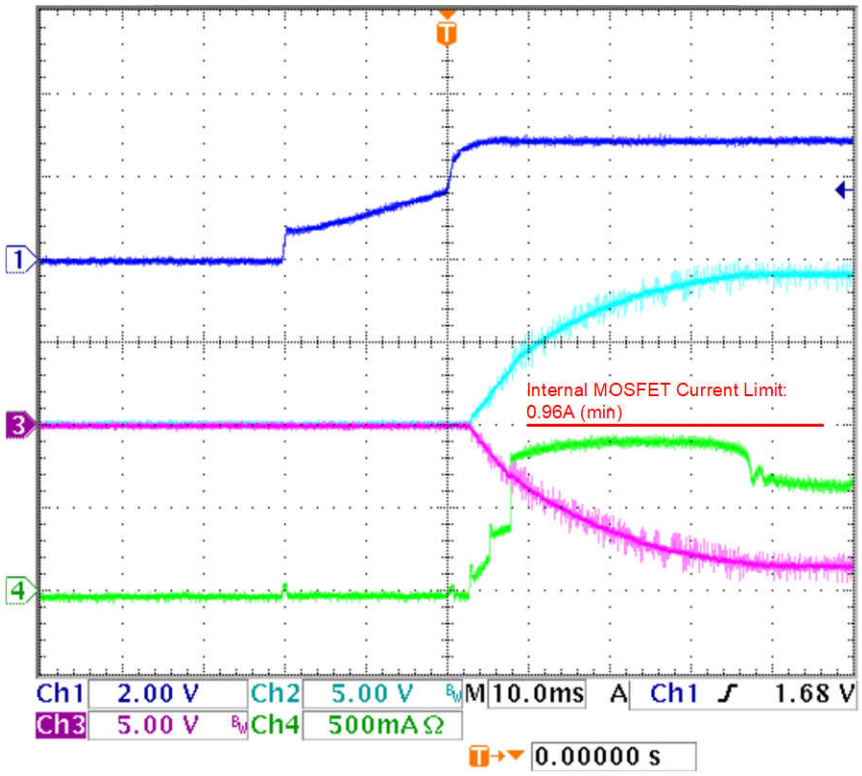


**Figure 4-1. Startup Waveforms With 3V Input**

Figure 4-2 shows the initial startup results at an input voltage of 18V, demonstrating the both 9V and -9V outputs are operating and regulating properly (VIN: Ch1 in blue with 10V/div, VOUT (9V): Ch2 in light blue with 5V/div, VOUT (-9V): Ch3 in purple with 5V/div).

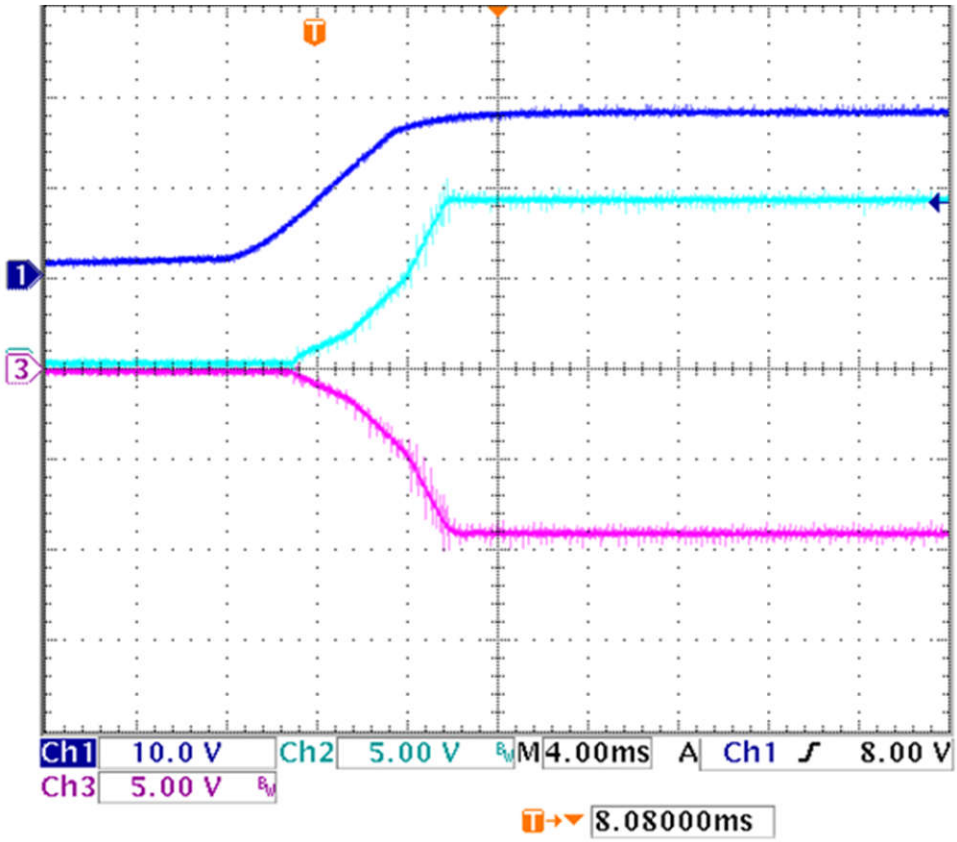


**Figure 4-2. Startup Waveforms With 18V Input**

Figure 4-3 shows the key voltage and current waveforms under steady-state operation ($V_{SW}$: Ch1 in blue with 10V/div, $V_{OUT\ (+9V)}$: Ch2 in light blue with 10V/div, $V_{OUT\ (-9V)}$: Ch3 in purple with 10V/div, $I_{L1}$: Ch4 in green with 0.5A/div). The 9V and -9V outputs are properly regulated, and the waveforms of VSW and inductor current of L1 are also operating normally at a switching frequency of 1.2MHz.

As the input voltage increases, the SW pin voltage of the TPS61170 also rises. Therefore, considering the voltage overshoot during switching on the SW pin, sufficient voltage margin must be maintained to make sure that the SW pin voltage always remains below 40V which is the absolute maximum voltage rating of the TPS61170.

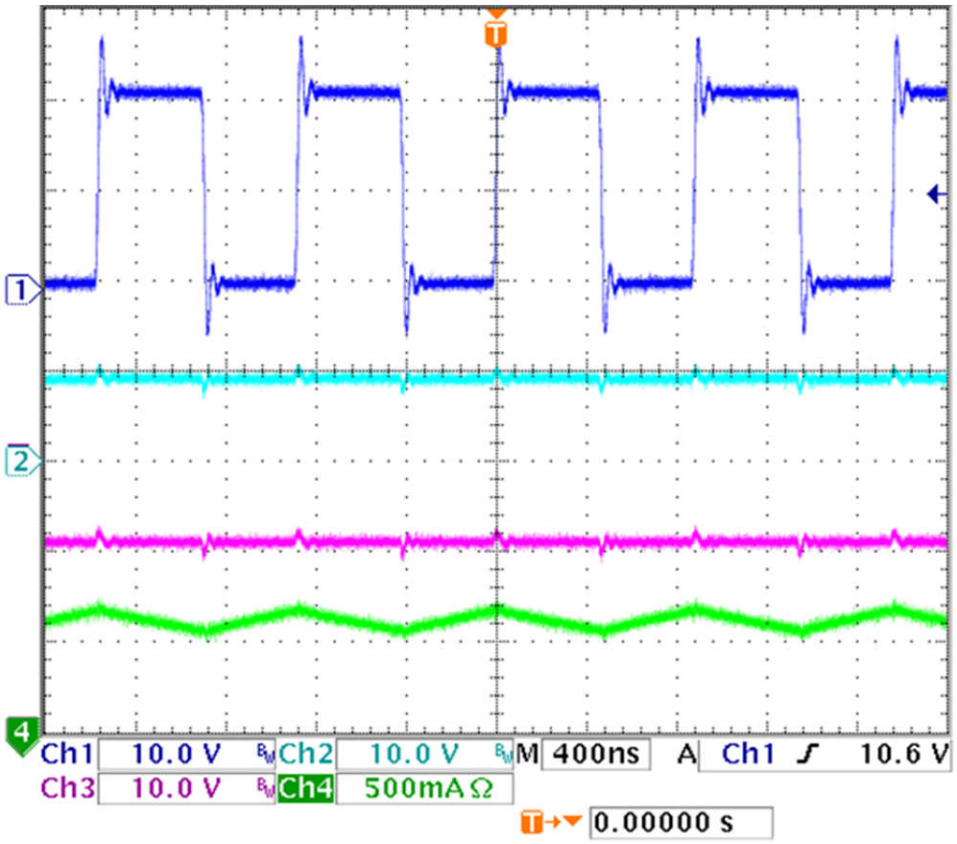


**Figure 4-3. Key Waveforms Under Steady-State Operation**

Figure 4-4 shows gain and phase margin, and the crossover frequency is about 2kHz with 70-degree phase margin. To verify sufficient phase margin, a relatively low crossover frequency is therefore selected. This is because a SEPIC converter is a fourth-order system that contains multiple energy-storage elements (two inductors and a coupling capacitor).

In CCM, the SEPIC converter has an energy transfer mechanism that is structurally similar to that of a boost converter. As a result, when the duty cycle increases, the output voltage does not increase immediately but instead rises after a delay.

This behavior leads to the presence of a RHPZ which limits the achievable control bandwidth. Consequently, the crossover frequency must be set well below the RHPZ frequency.

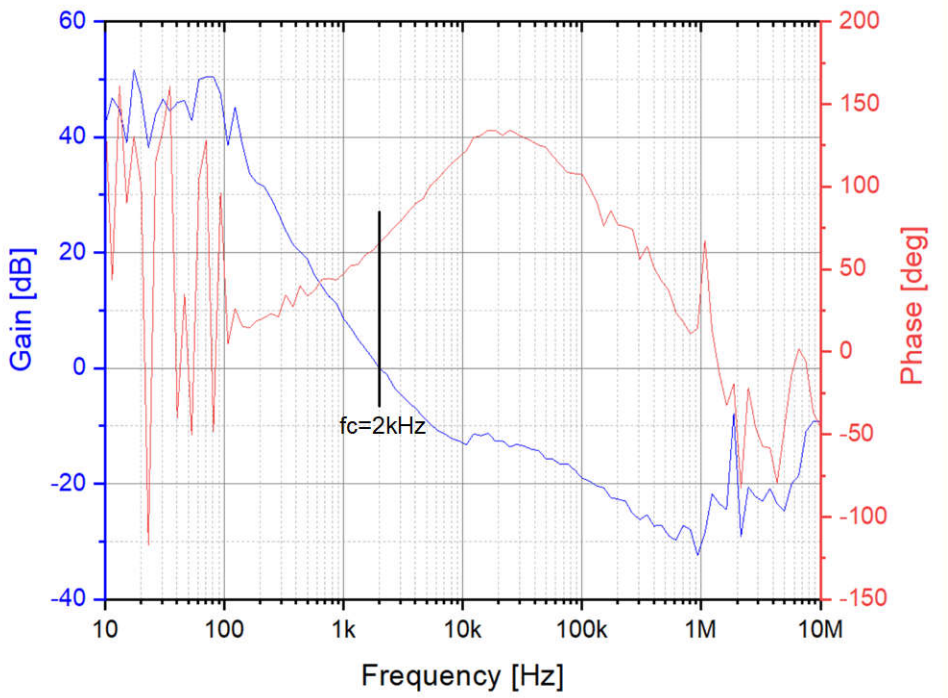


**Figure 4-4. Loop Gain and Phase Margin**

## 5 Summary

A practical approach to achieving positive and negative output voltages (9V and -9V) with wide input voltage range (3 ~ 18 VIN) is proposed in this application report. As the actual application case using TI PMICLOADBOARDEVM has been confirmed, the design operates properly and provides accurate output voltage regulation. The key point is that an inverting Buck-Boost topology was used to generate -9V output, while a SEPIC topology was employed to generate 9V output. To regulate the output voltages, the feedback signal was taken from 9V output, and all of these functions are achieved using a single TPS61170, making this design a highly efficient approach in terms of overall cost and the total design size. This application report demonstrates that the proposed application method performs well, as verified through simulation and experimental validation.

## 6 References

1. Texas Instruments, *TPS61170 1.2-A High-Voltage Boost Converter in 2-mm x 2-mm2 QFN Package*, datasheet.
2. Texas Instruments, *TPS61170EVM-280*, user's guide.
3. Texas Instruments, *PMICLOADBOARDEVM Evaluation Module User's Guide*, user's guide.

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