Application Note

Optimizing the High Side Switch Gate Ringing

Alan Xia

ABSTRACT

This paper provides an in-depth analysis of the high-side switch gate ringing issue commonly encountered in typical boost converter designs and proposes optimization solutions. When the low-side FET is closed, the excessive dv/dt creates a gate ringing voltage spike in the high-side MOSFET gate. When the ringing voltage is higher than the MOSFET's Vgsth, the MOSFET will be turned on. Based on the experimental results, a solution is proposed to optimize gate ringing. Considering efficiency and safety, this paper recommends the HO Gate parallel 1.5nF solution and the HO gate parallel PNP Solution.

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1 Introduction

The LM5125A-Q1/LM5126A-Q1 is a stackable dual-identical step-up controller. The device provides a stable output dropout when the input voltage is less than or equal to the output voltage and supports VI to VOUT bypass modes to save power consumption. The VOUT can be dynamically programmed using analog or digital ATRK/DTRK functions when using Class H topologies commonly used for automotive external amplifier audio. When VBIAS < 4.5V, the internal VCC power supply automatically switches from VBIAS to VOUT, so this can support VIN as low as 2.5V after boot. A fixed switching frequency can be set between 100kHz and 2.2MHz by means of a resistor on the RT pin or SYNPIN clock. The FPWM mode or diode emulation can be changed during operation. The achieved protection peak current limits, average input current limits, average inductor current monitoring, over- and under-voltage protection, and thermal shutdown protect devices and applications.

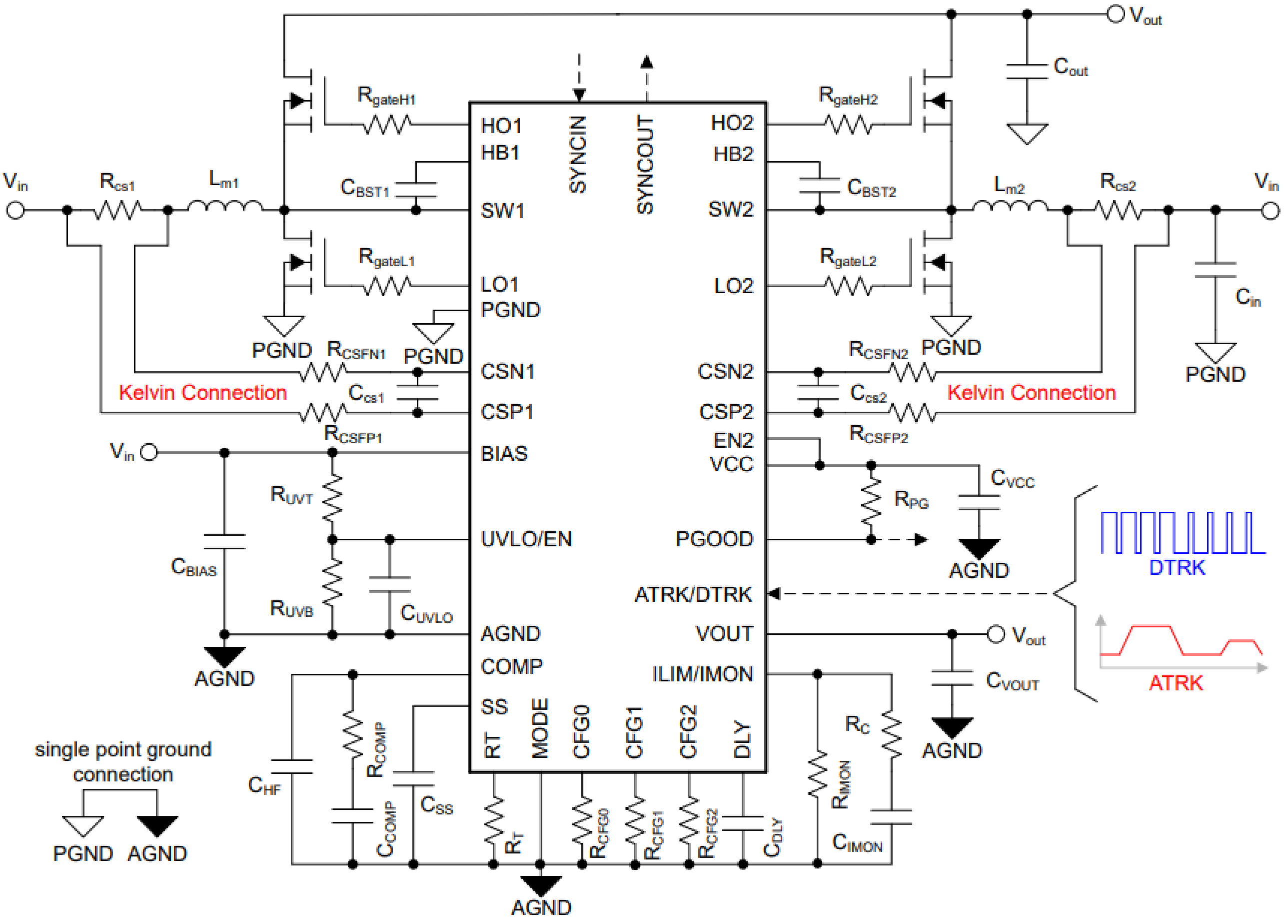


Figure 1-1. LM5125A-Q1 Typical Application Block Diagram

In DCDC applications, significant ringing is frequently observed at the MOSFET gate. Such voltage pulses can trigger the MOSFET to turn on, this paper presents measurements of the ringing waveforms captured on an external amplifier board. Building upon these observations, the paper provides a theoretical analysis and validated through testing on an EVM (Evaluation Module) to propose the design.

2 LM5125/6A-Q1 Gate Ringing Issues

Testing of switching waveforms in automotive external amplifier applications found that during high-side MOSFETs turn on and low-side MOSFETs turn off. The gate of the high-side MOSFET detects a significant pulse voltage, which exceeds 1.2V.

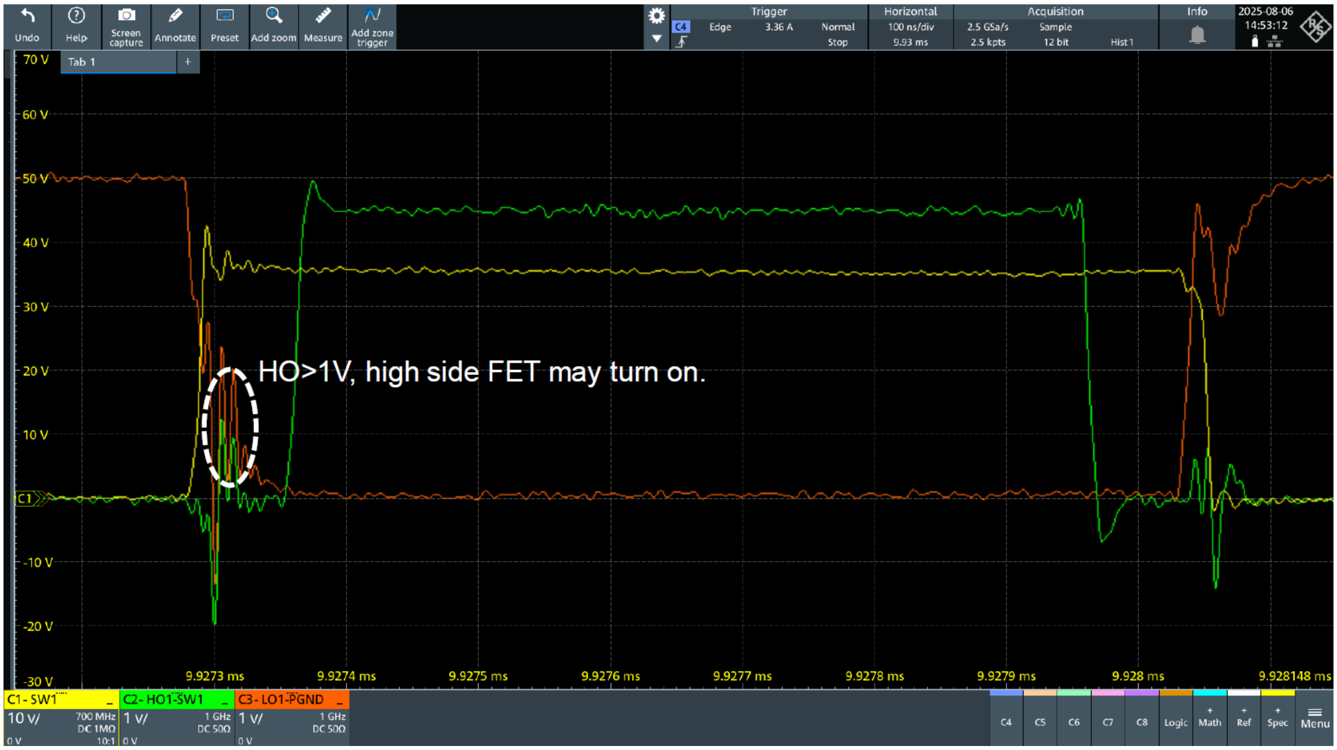
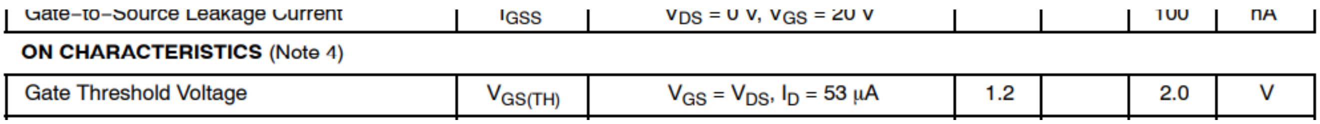


Figure 2-1. Gate Ringing Test Waveform

As shown in Figure 2-2 , the MOSFET used for the test was NVMFS5C670NL with VGSTH of 1.2-2V, so when VGSTH is greater than 1.2V, there is a risk that MOSFETs may be incorrectly turned on. As can be seen from the waveform, the low side is not completely shut off at this time, so a shot through is formed, and the high side and low side MOS are connected at the same time. There is a short circuit that can occur, and there is a significant current flow through the MOSFET, and there is a risk of damaging the MOSFET.



Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 53 μA	1.2		2.0	V

Figure 2-2. NVMFS5C670NL Parameters

3 Root Cause of Gate Ringing Issues

As shown in Figure 3-1, Boost switches when the LS MOS is switched off, and the HS MOS is switched on. At this point, there is a prominent dv/dt at the SW point, as indicated by the red dotted line:

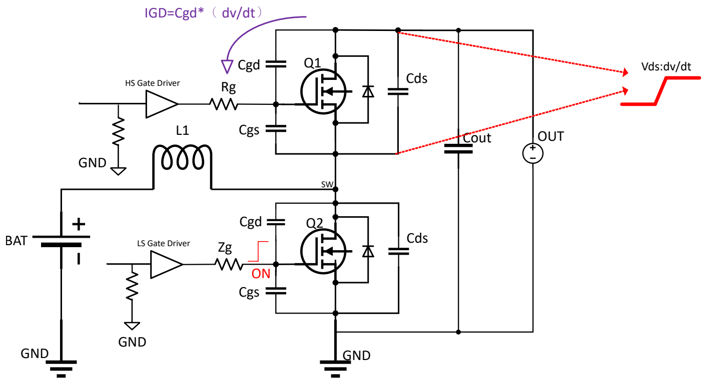


Figure 3-1. Gate Ringing Voltage Root Cause Analysis

This voltage change dv/dt creates a significant current through the body diode of the HS MOS and the parasitic capacitance Cgd of Q1, which can be calculated by Equation 1 :

$$I = Cgd\left(\frac{\mathrm{dv}}{\mathrm{di}}\right)\#\left(1\right) \tag{1}$$

This current creates a distinct voltage spike at Q1 Gate and Rg; see Equation 2:

$$Ugs = IRg\#\left(2\right) \tag{2}$$

When the HS MOS is switched on, it is constantly charged at the Q1 Gate, and this current first causes the HS MOS to slow down charging and even reverse the voltage. So, it can be seen from the blue dashed waveform that the Vgs is inverted first, then a large voltage spike will be formed, and when this voltage spike exceeds the Vgsth of the MOSFET, it causes Q1 to open prematurely, if Q2 is not completely shut off. The large current will directly break through the MOSFET.

As can be seen from Equation 1 and Equation 2, the way to reduce this risk is to reduce **I**, so this ringing on MOSFETs can be reduced by reducing Cgd and dv/dt, or by reducing the Rg appropriately.

This can typically be avoided in the design and in the selection of MOSFETs in the following ways:

1. In terms of layout design, a Kelvin connection can be employed for the gate-to-Source loop, as illustrated in the LM5125A-Q1 EVM layout design shown in Figure 3-2

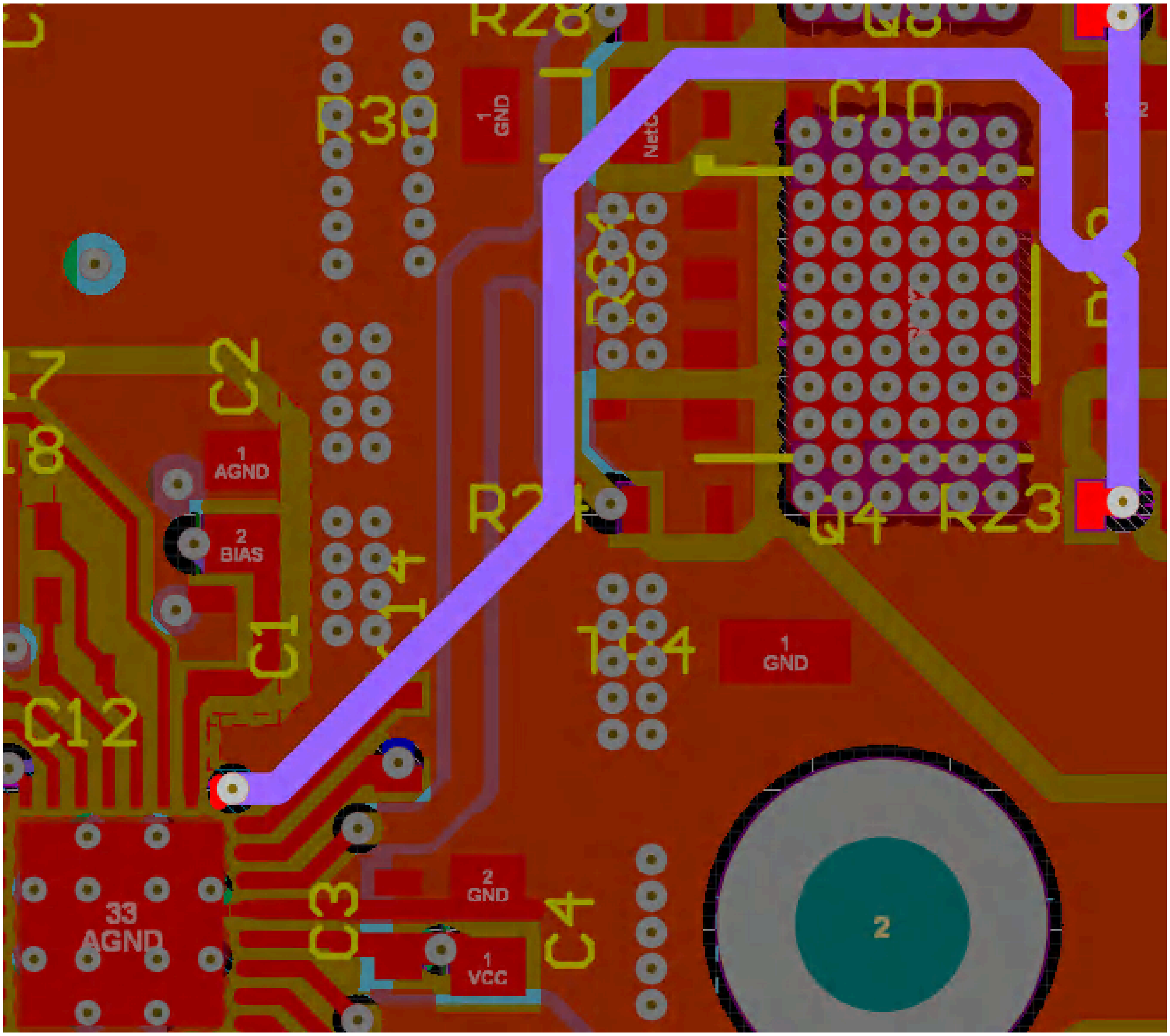


Figure 3-2. LM5125A-Q1 EVM HO-GND Kelvin Connection Design (Layer 5)

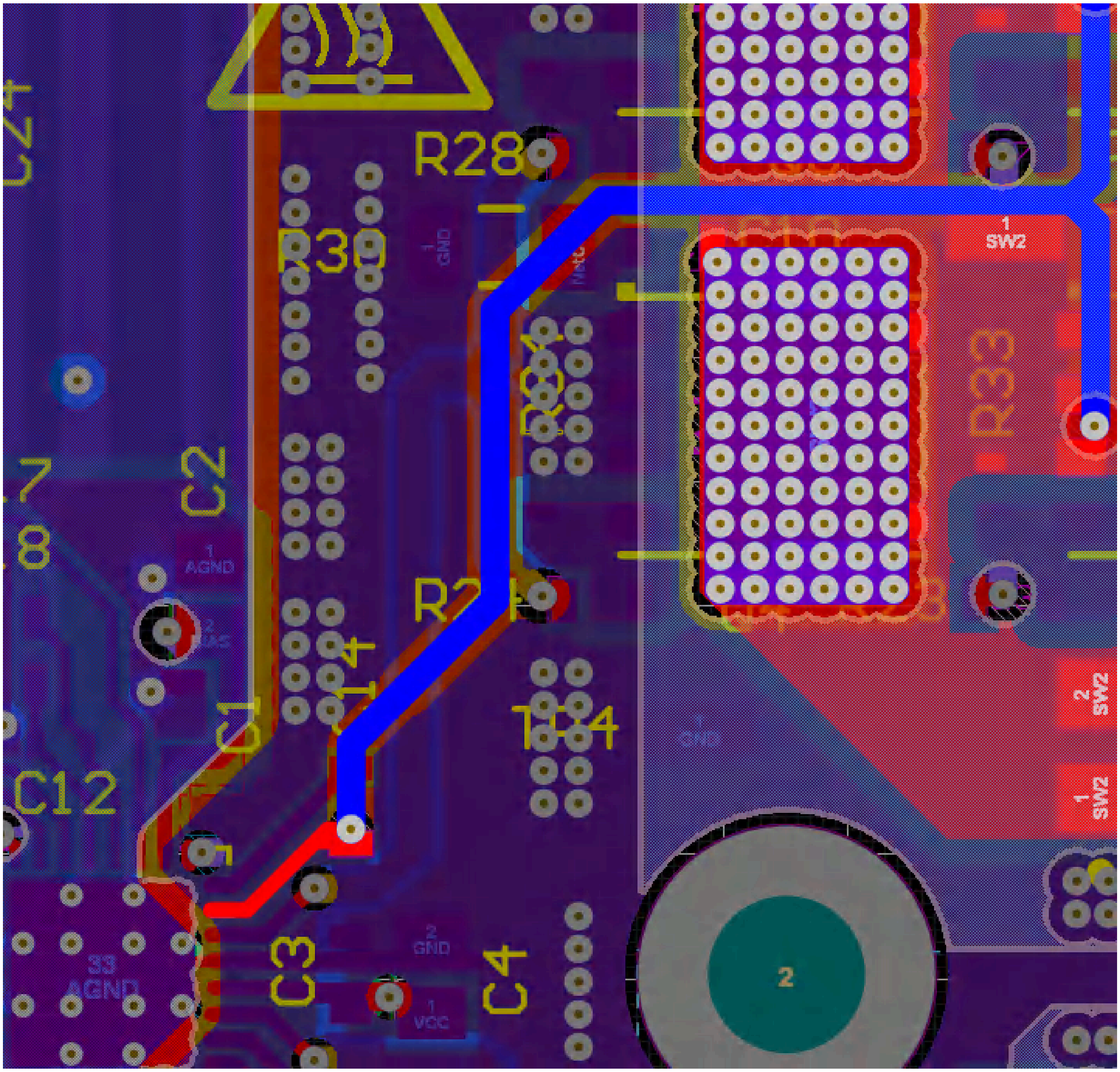


Figure 3-3. LM5125A-Q1 EVM Source-SW Kelvin Connection Design (Layer 6)

As shown in Figure 3-3, the loop design from the Gate to SW utilizes adjacent layers and employs an identical trace layout; this approach minimizes the loop area, thereby reducing induced parasitic inductance.

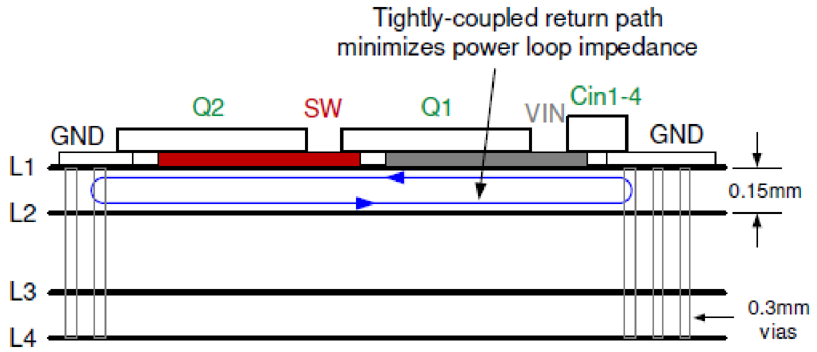


Figure 3-4. PCB Stack-Up Depicting Switching Loop With Low Area Using Layers L1 and L2

Figure 3-4 shows a side view to illustrate the concept of creating a low profile, self-canceling loop in a multilayer PCB structure. The L2 GND plane layer provides a tightly coupled current return path directly under the MOSFETs to the source terminals of Q2.

2. Select a higher device in Vgsth when selecting MOSFETs to raise the ringing voltage to the open threshold and reduce the risk.
3. Select the MOSFET with less Cgd/Cgs ratio.
4. Lower Rg appropriately.
5. Parallel capacitance between Gate and Source, artificially increasing Cgs. Additional continuity losses must be considered.

Above several ways, most of the recommendations have some limitations of MOSFETs in the design. So the simplest and most effective way is the parallel capacitance solution proposed by 5. This document provides recommendations on the design of gate ringing for LM5125A-Q1 and LM5126A-Q1 based on the results.

4 Design of Gate Ringing Issues

LM5125A-Q1 and LM5126A-Q1 are widely used in automotive external amplifiers. The test follows the design scenarios of the application as a reference, as the main test setup in Table 4-1

Table 4-1. Test Setup

Parameter	Value
Input voltage	14.4V
Output voltage	35V
Switching frequency	400kHz
Inductor L_m	3.3µH
HS Rg	2.2Ω
LS Rg	10Ω
MOSFET	NVMFS5C670NL

Based on the original design, 1nF, 1.5nF, 2.2nF, and 3.3nF capacitors connected in parallel with Q1 were tested, and gate ringing tests were conducted on the turn-on and turn-off processes of the high-side MOSFET.

1. Original Design Test:

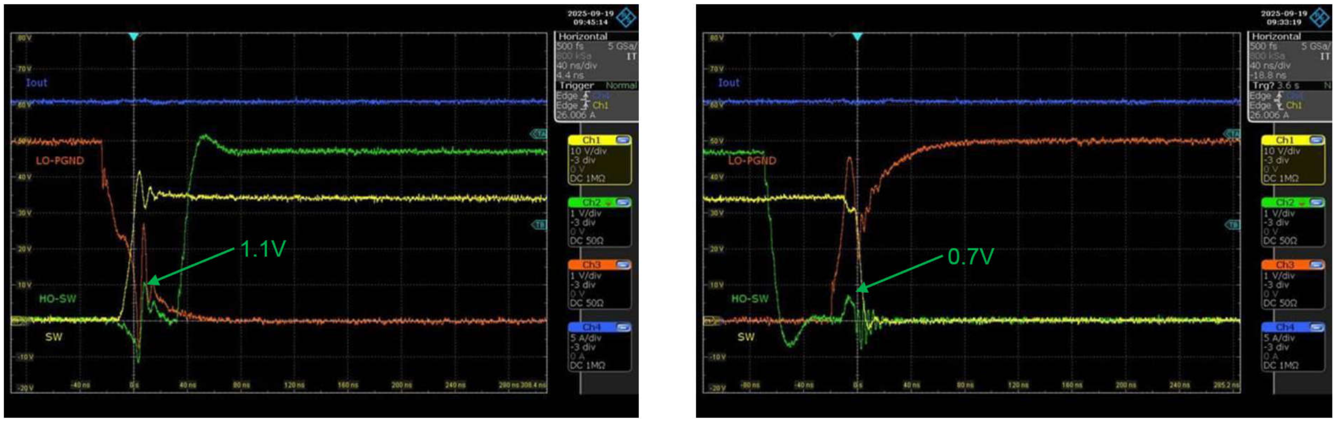


Figure 4-1. Original Design Test Results (HS ON/LS OFF (Left), HS OFF/LS ON (Right))

2. HO+1nf:

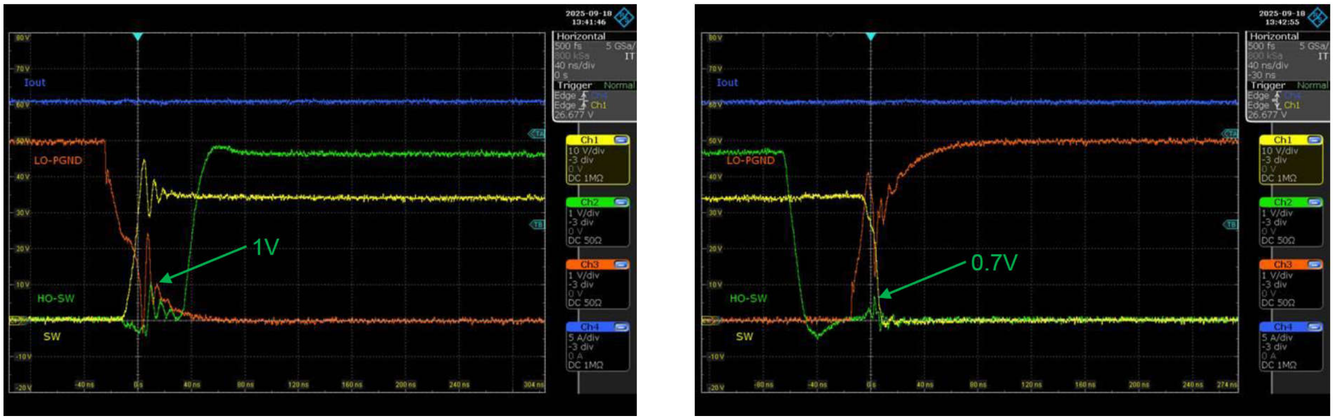


Figure 4-2. HO+1nf Test Results: HS ON/LS OFF (Left), HS OFF/LS ON (Right)

3. HO+1.5nf:

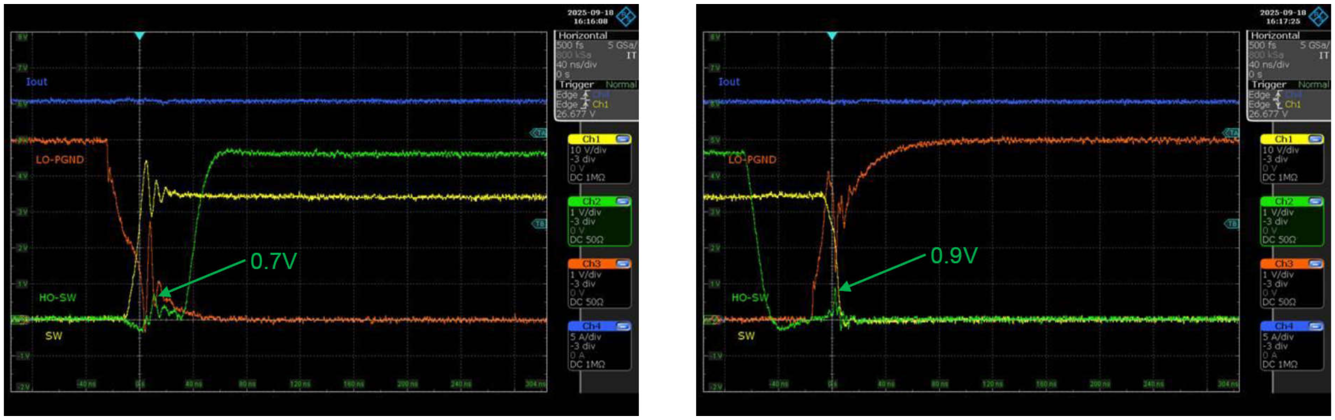


Figure 4-3. HO+1.5nf Test Results: HS ON/LS OFF (Left), HS OFF/LS ON (Right)

4. HO+2.2nf:

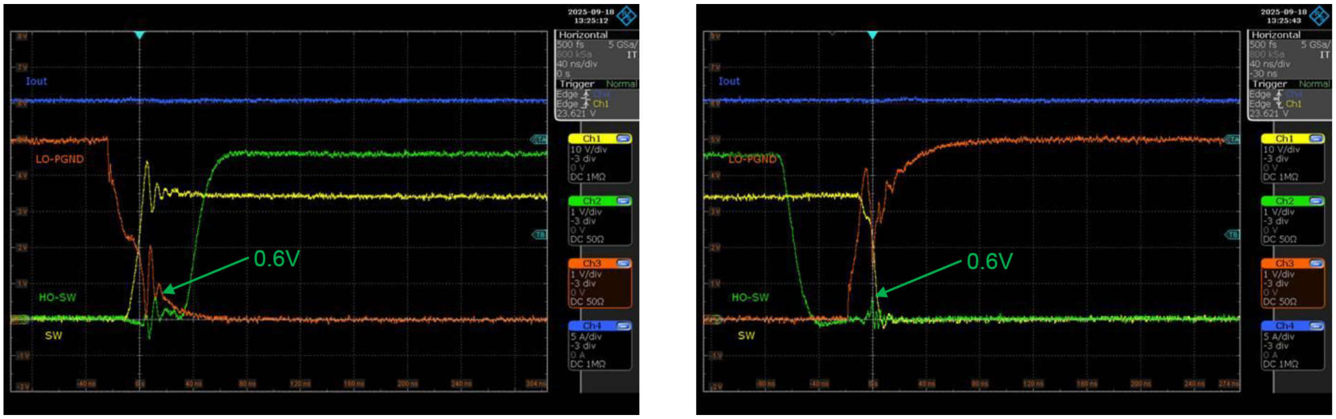


Figure 4-4. HO+2.2nf Test Results: HS ON/LS OFF (Left), HS OFF/LS ON (Right)

5. HO+3.3nf:

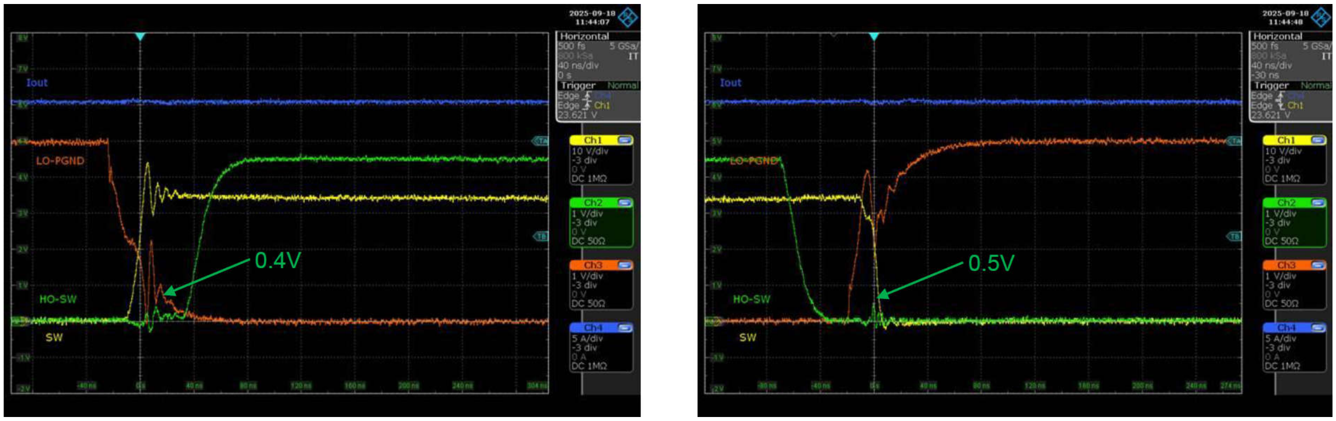


Figure 4-5. HO+3.3nf Test Results: HS ON/LS OFF (Left), HS OFF/LS ON (Right)

The test results are summarized in Table 4-2

Table 4-2. Summary of Test Results

HO Status Design	ON	OFF
Original	1.1V	0.7V
HO+1nF	1V	0.7V
HO+1.5nF	0.7V	0.9V
HO+2.2nF	0.6V	0.6V
HO+3.3nF	0.4V	0.5V

Therefore, considering the additional losses and the impact on switching speeds, it is calculated by

External 1.5nF only increases the HO gate driver loss.

$$P = 14V \times 1.5nF \times 5V \times 400kHz = 42mW \quad (3)$$

TI recommends incorporating a provision for this capacitor during the design phase; this facilitates debugging and eliminates risk if issues such as gate ringing arise. of HO+1.5nF as shown in Figure 4-6

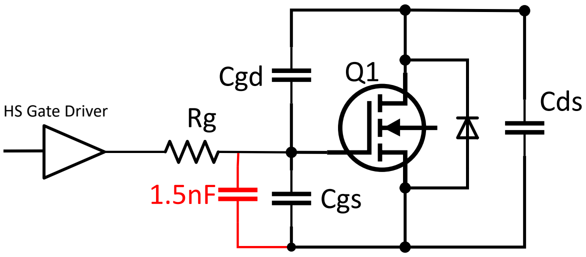


Figure 4-6. Design of HS MOS Parallel 1.5nF

TI recommends another design.

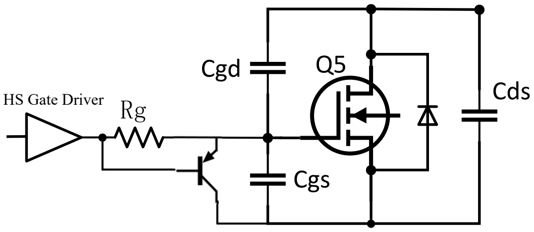


Figure 4-7. Design of HO and PNP Design

As shown in Figure 4-7, an alternative design approach involves incorporating a PNP transistor on the drive side of the high-side switch. This design serves to enhance noise immunity and prevent spurious turn-on. When the HO output is in the OFF state, the current is coupled to GND through the PNP transistor, thereby preventing the buildup of a gate-source voltage (Ugs). This common-base PNP pull-down configuration effectively suppresses coupled interference, thereby preventing the inadvertent activation of the HO output.

5 Summary

This paper combined with the LM5125A-Q1/LM5126A-Q1 actual case, measured gate ringing issues, conducted a full theoretical analysis, based on the actual test results, to give the best design for overall efficiency and safety. Engineers can refer directly to the design in the actual development to help design a safe and efficient system.

6 References

1. Texas Instruments, *LM5125A-Q1, Wide-VIN, Dual-Phase, Automotive, Boost Controller With VOUT Tracking*, datasheet.
2. Texas Instruments, *LM5126A-Q1, Wide-VIN, Single-Phase, Boost Controller with VOUT Tracking*, datasheet.
3. Article" Design Considerations of a Dual-Phase Interleaved Boost Converter in Class-H Audio Amplifier System"
4. Texas Instruments, *自适应死区在 DCDC 中对效率的提升*, technical article.
5. Texas Instruments, *汽车音频功放系统升压电路功能介绍*, application note.
6. Texas Instruments, *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout*, application brief.

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