Application Note

TAS2x20: Extending Battery Life in Portable Audio Applications

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ABSTRACT

As battery-powered devices evolve to include more features, designers are increasingly seeking new options for improving power consumption. However, every added function increases strain on battery life, making efficient power management a critical aspect of product design. Texas Instruments (TI) addresses this challenge with efficiency improvement features, offering designs that reduce power usage in audio amplifiers. These features enhance energy efficiency while delivering high-quality sound, making TI products an excellent choice for modern portable devices, such as Bluetooth® speakers, cell phones, PCs, and other handheld electronics.

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1 Introduction

Texas Instruments continues to push the boundaries of audio amplifiers with advanced features and algorithms that set new benchmarks for efficiency and performance. The TAS2x20 family integrates several proprietary modes that significantly improve power utilization without compromising audio quality. At the core of these devices are a set of exclusive efficiency-boosting technologies:

- Internal Class-H
- Music efficiency mode
- Noise gate
- Y-bridge

Together, these features intelligently adapt to operating conditions, so the amplifier delivers maximum efficiency while preserving exceptional sound quality.

This application note provides an inside look at the algorithms that drive these technologies, the external system interface, and the PurePath™ Console 3 (PPC3) software that simplifies evaluation and tuning. This document includes performance results that demonstrate the benefits of these efficiency improvement techniques, which enable designers to create smaller, cooler, and longer-lasting audio products without compromise.

2 Internal and External Class-H

The TAS2x20 integrates an advanced Class-H boost control algorithm, which dynamically adjusts the boost supply with a minimum step size of 33mV by tracking the audio signal levels in real time. By reducing unnecessary power overhead, this approach significantly improves system efficiency and extends battery life—an important advantage for portable and power-sensitive designs.

The Class-H operation is enabled through the *BST_MODE[1:0]* register. The max boost voltage the device generates is controlled by *VBOOST_MAX_CTRL[7:0]* and can be configured with a step size of 66mV. In Class-H mode of operation, the boost voltage does not exceed this set value.

Table 2-1. Boost Mode Enable

BST_MODE [1:0]	BOOST MODE
00	Class-H – High efficiency (default)
01	Class-G – Low in-rush
10	Always On
11	Always Off – Pass-through

Table 2-2. Max Boost Voltage Configuration

VBOOST_MAX_CTRL[7:0]	BOOST VOLTAGE (V)
0x00 – 0x53	Reserved
0x54	5.54V
0x55	5.61V
…	…steps of 66mV per LSB step…
0xA7	11.02V
…	…steps of 66mV per LSB step…
0xE3	14.98V (default)
0xE4	15.05V
0xE5	15.11V
0xE6 – 0xFF	Reserved

The algorithm incorporates signal buffering to provide the necessary look-ahead time, so the boost output capacitor is charged in advance; preventing clipping under dynamic audio conditions. This signal buffering continuously monitors the input signal and applies system-level parameters—such as boost output voltage, output capacitor size, and channel gain—configured through the PPC3 software. From this, PPC3 automatically computes the appropriate Class-H tuning coefficients and programs the coefficients into the *CLASSH_TUNING_x[23:0]* registers.

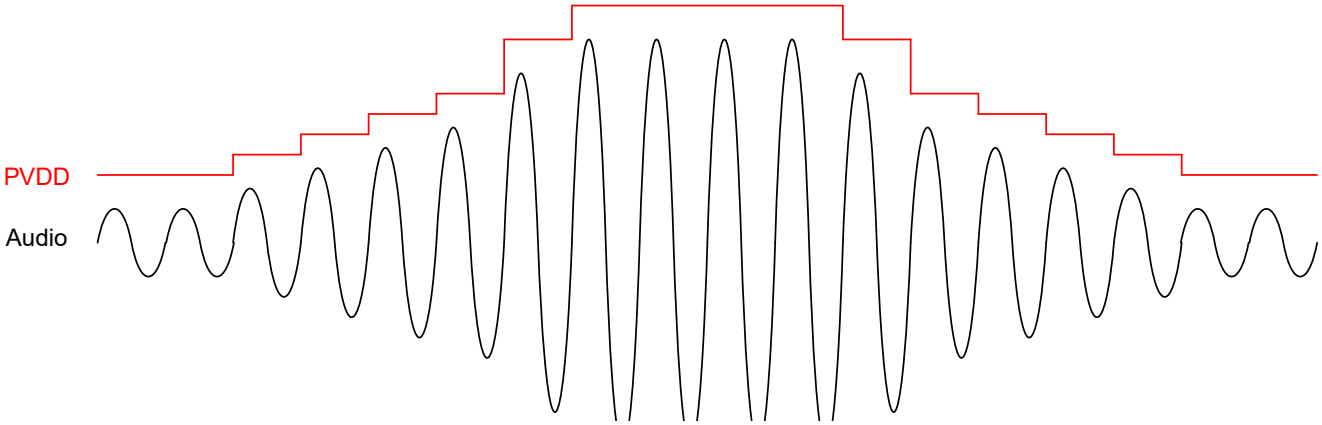

Figure 2-1. Class-H Operation

The TAS2120 and TAS2320 audio amplifier devices support Class-H operations, but differ in implementations of the necessary boost circuitry. The TAS2120 device has an integrated boost converter, enabling internal implementation of the Class-H control algorithm. This implementation allows for closed-loop control of the boost voltage directly within the device.

Conversely, the TAS2320 device does not have an integrated boost converter. Instead, the device provides a pulse-width modulation (PWM) control signal output designed to drive an external boost circuit. This external circuitry is then responsible for generating the Class-H boost output voltage.

This implementation distinction impacts the system design, with the TAS2120 offering a more compact design due to on-chip integration, while the TAS2320 offers greater flexibility in boost converter selection and configuration.

3 Music Efficiency Mode

The music efficiency mode in TAS2x20 devices is designed to reduce quiescent current (IQ) consumption during active playback, extending battery life without compromising audio quality. This feature is particularly effective for dynamic audio content, such as music, movies, and voice calls, where audio signal levels naturally vary over time.

The device continuously monitors the input audio level against a user-defined threshold set by the *MUSIC_EFF_MODE_THR[23:0]* register. When the signal falls below this threshold, an internal hysteresis timer is activated. If the signal level remains below the threshold for the full duration defined by the *MUSIC_EFF_MODE_TIMER[23:0]* register, the device transitions into music efficiency mode.

In this state, internal sensing blocks, such as I-sense and V-sense, enter a low IQ state to reduce the overall device IQ power consumption. While in this mode, the I-V sense output data is held at zero, and the MUSIC_EFF_STATUS bit is set to high to indicate entry. When the audio signal rises above the configured threshold, the device comes out of music efficiency mode and the status bit is set to low.

When the signal level increases above the *MUSIC_EFF_MODE_THR[23:0]* threshold, the device automatically wakes up the blocks in low IQ mode and continues playing out the audio input signals. The transition from music efficiency mode to normal operation occurs with minimal click and pop. While the device is in music efficiency mode, the audio channel performance is maintained and does not impact the output signal level or noise.

The *MUSIC_EFF_MODE_THR[23:0]* and *MUSIC_EFF_MODE_TIMER[23:0]* registers can be configured using the PPC3 software.

4 Noise Gate

When the noise gate feature is enabled, the device automatically detects periods of silence during active playback mode and reduces the idle channel power consumption significantly to extend the battery life. This feature is particularly effective for audio content with extended quiet intervals, such as voice calls or movie soundtracks.

The device monitors the input audio level against a threshold defined in the *NG_TH_LVL[2:0]* register. When the audio signal falls below the threshold, an internal hysteresis timer is enabled. If the signal level remains below the configured *NG_TH_LVL[2:0]* threshold for the entire duration of the *NG_HYST_TIMER[1:0]* timer, the device enters the noise gate mode and reduces the idle channel power consumption. In this state, high-power switching blocks, including the Class-D PWM output stage, are shut down and the outputs are driven low. The output impedance of the Class-D stage, while in noise gate mode, can be configured through the *CLASSD_HIZ_MODE* register, allowing designers to improve system behavior depending on load requirements. When the device is in noise gate mode, the *NG_STATUS* bit is set as high and when the device comes out of noise gate mode, the status bit is set to low.

When the signal level increases above the *NG_TH_LVL[1:0]* threshold, the device automatically wakes up the blocks in low IQ mode and starts playing out the audio input signals. The wake up from noise gate maintains the signal fidelity by buffering the input signal data during the transition time from noise gate mode to active playback mode. The return to active playback is designed with proper sequencing to avoid audible clicks or pops, maintaining signal fidelity throughout.

The noise gate feature reduces idle current without compromising playback quality, while giving system designers precise control of threshold, hysteresis timing, and output impedance behavior through register configuration.

Table 4-1. Noise Gate Threshold

NG_TH_LVL[2:0]	Configuration
000	-85dBFs
001	-90dBFs
010	-95dBFs
011	-100dBFs
100 (default)	-105dBFs
101	-110dBFs
110	-115dBFs
111	-120dBFs

Table 4-2. Noise Gate Hysteresis Timer

NG_HYST_TIMER[1:0]	Configuration
00	10ms
01 (default)	50ms
10	100ms
11	1000ms

Both music efficiency mode and noise gate mode are controlled through the *EFFICIENCY_MODE[1:0]* register, which allows configuration of the desired efficiency mode of operation.

Table 4-3. Efficiency Mode Configuration

Bit	Field	Type	Reset	Description
7-6	EFFICIENCY_MODE[1:0]	R/W	2h	Device operational mode. 0h = Music efficiency and noise gate mode disabled 1h = Noise gate mode only 2h = Music efficiency only 3h = Music efficiency and noise gate mode

5 Y-Bridge

The Y-bridge amplifier architecture improves efficiency by dynamically switching between two supply rails, a high-voltage rail (PVDD) and a low-voltage rail (VDD), based on real-time output power demand. A programmable power threshold determines the rail selection, enabling the amplifier to improve efficiency at low power levels and reduce consumption during idle states. The architecture resembles a Y-shape, distinguishing

this architecture from the traditional linear half-bridge design. Figure 5-1 shows the difference between a traditional Class-D amplifier versus the amplifier with Y-bridge architecture.

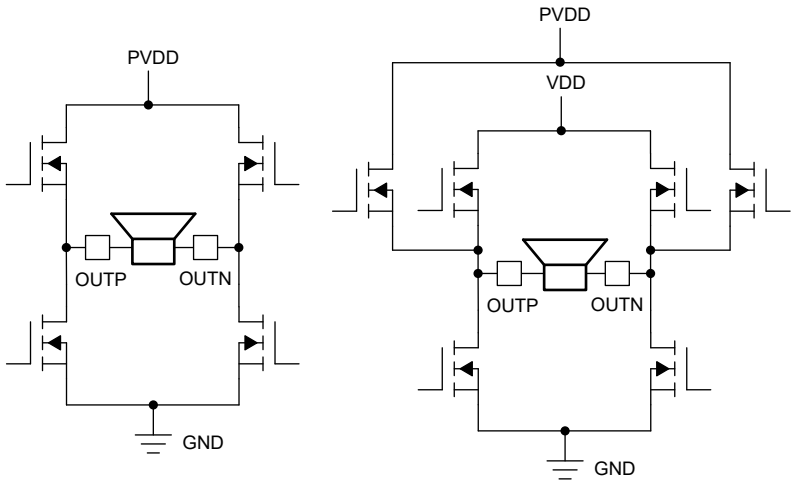

Figure 5-1. Traditional Class-D Amplifier Versus Simplified Y-Bridge Architecture

For a classic half-bridge architecture, the output stage relies solely on a high-voltage supply (PVDD) for switching. In contrast, the Y-bridge architecture utilizes both a high-voltage supply (PVDD) and a fixed low-voltage rail (VDD). During low-power playback or idle conditions, when headroom requirements are minimal, the output stage operates solely from VDD without causing any clipping, significantly improving efficiency. When power demand rises and greater headroom is required, the amplifier transitions seamlessly to the PVDD rail, achieving the same maximum output capability as a conventional Class-D design. This dual-rail operation allows the Y-bridge to maintain high efficiency across a much wider dynamic range, with the largest gains realized at low output power levels where traditional Class-D architectures are least efficient.

The *EN_Y_BRIDGE_MODE* register enables or disables the Y-bridge architecture.

Table 5-1. VDD Y-Bridge Mode Configuration

EN_Y_BRIDGE_MODE	Configuration
0	Y-bridge mode is disabled
1 (default)	Y-bridge mode is enabled

The device continuously monitors the input audio signal level against the Y-bridge mode threshold configured in the *VDD_MODE_THR_LVL [23:0]* register. When the audio signal drops below this threshold, an internal hysteresis timer is activated. If the signal remains below the threshold for the duration specified by the *YBRIDGE_HYST_TIMER [1:0]* register, the device switches to a lower voltage (1.8V) VDD supply-based PWM switching mode. Once the signal level exceeds the threshold defined by the *VDD_MODE_THR_LVL [23:0]* register plus the *VDD_MODE_HYST [23:0]* register, the device starts switching the output PWM signal on PVDD supply without introducing any signal clipping. Both the *VDD_MODE_THR_LVL [23:0]* and *VDD_MODE_HYST [23:0]* registers can be configured using the PPC3 software tool.

Table 5-2. VDD_MODE_THR_LVL Register

Bit	Field	Type	Reset	Description
23-0	VDD_MODE_THR_LVL[23:0]	R/W	50A3D7h	Addresses 0x8 to 0xA are combined. Can be configured using the PPC3 software.

Table 5-3. VDD_MODE_HYST Register

Bit	Field	Type	Reset	Description
23-0	VDD_MODE_HYST[23:0]	R/W	DA74h	Addresses 0xC to 0xE are combined. Can be configured using the PPC3 software.

Table 5-4. VDD Y-Bridge Hysteresis Timer

YBRIDGE_HYST_TIMER[1:0]	Configuration
00	100µs
01 (default)	500µs
10	5ms
11	50ms

6 Device Configuration with PurePath™ Console 3 (PPC3) Software

The features and device-level configurations of the TAS2x20 family are managed through the PurePath™ Console 3 (PPC3) software. PPC3 can be downloaded and installed directly from the Texas Instruments' website. Once installed, the TAS2x20 application can be added within the PPC3 environment to provide device-specific configuration and tuning capabilities.

PPC3 calculates the necessary register coefficients based on the system configuration options selected through the graphical user interface (GUI). This method is the recommended approach for initial device configuration, so all advanced features, such as Class-H, music efficiency, noise gate, and Y-bridge operate correctly. Once the TAS2x20 application calculates and updates the device, the values of the registers can be read back using the PPC3 tool for final system integration.

7 Efficiency Results Using the Advanced Device Features

This experiment used the TAS2120EVM evaluation board to characterize the input power consumption of the device under varying conditions. VBAT was set to 4.4V and IOVDD and VDD were set to 1.8V. Two distinct audio tracks were employed: a commercially available song ("Music Track") and a recorded speech sample ("Voice/Speech Track"). The TAS2120EVM was configured to output audio at three volume levels: 100%, 70%, and 30% of maximum output power.

A thorough evaluation of power consumption was performed for different volume settings, with all integrated power-saving features enabled, including internal Class-H, music efficiency mode, noise gate, and Y-bridge. Additionally, a baseline measurement was obtained with all features disabled, allowing for a direct comparison of the power-saving benefits. To further quantify the advantages of the advanced Class-H technology of TAS2x20 devices, a comparative power consumption analysis was conducted using a conventional 500mV Class-H design, representative of existing market offerings.

Table 7-1. Test Setup and Test Cases

Test Setup	Test Cases	Features	Volume
VBAT = 4.4V, IOVDD = VDD = 1.8V, Amplifier level = 18dBV, RL = 4Ω + 33µH, I2C mode, no output filter	Test Case: 1	No efficiency features	30%, 70%, 100%
	Test Case: 2	Existing 500mV Class-H design	30%, 70%, 100%
	Test Case: 3	TAS2120 with advanced efficiency features	30%, 70%, 100%

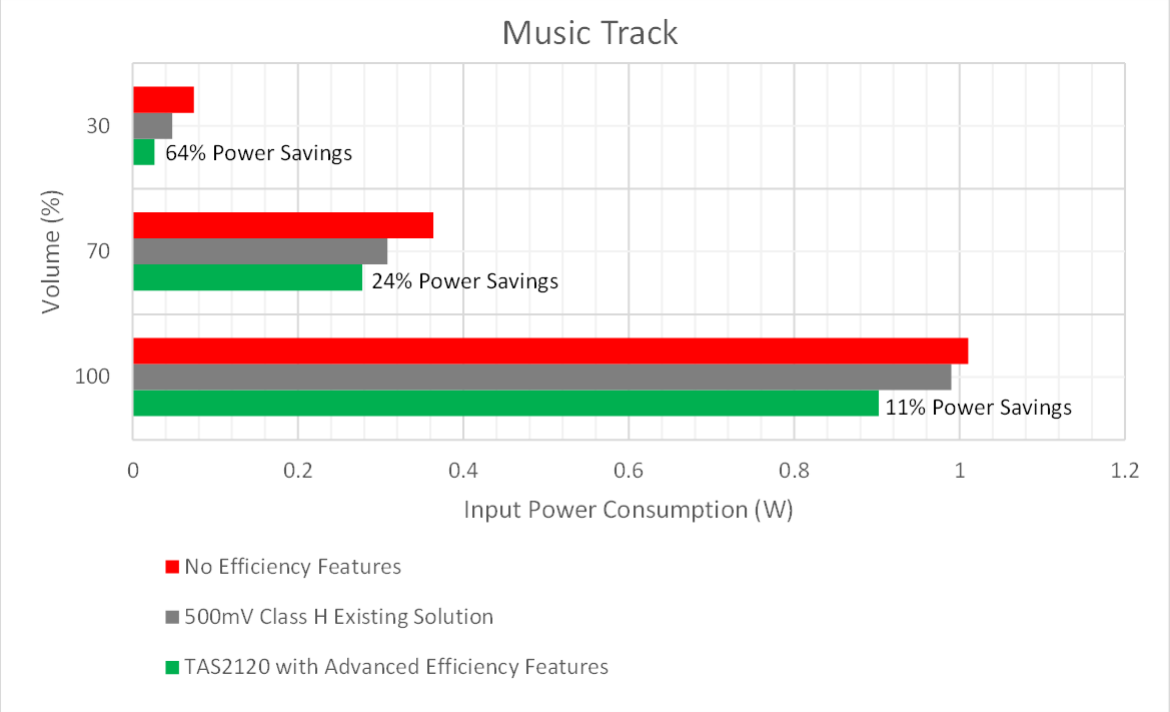

Figure 7-1. Power Consumption Comparison with Music Track

Power consumption measurements, conducted while playing the Music Track, demonstrated a significant improvement with the advanced efficiency settings. Enabling all available power-saving features reduced the overall power consumption by 64% for 30% volume, 24% for 70% volume, and 11% for 100% volume, relative to a configuration with all features disabled. Furthermore, comparing against the existing 500mV Class-H design, the TAS2120 device can achieve reduced power consumption by 45% for 30% volume, 10% for 70% volume, and 9% for 100% volume.

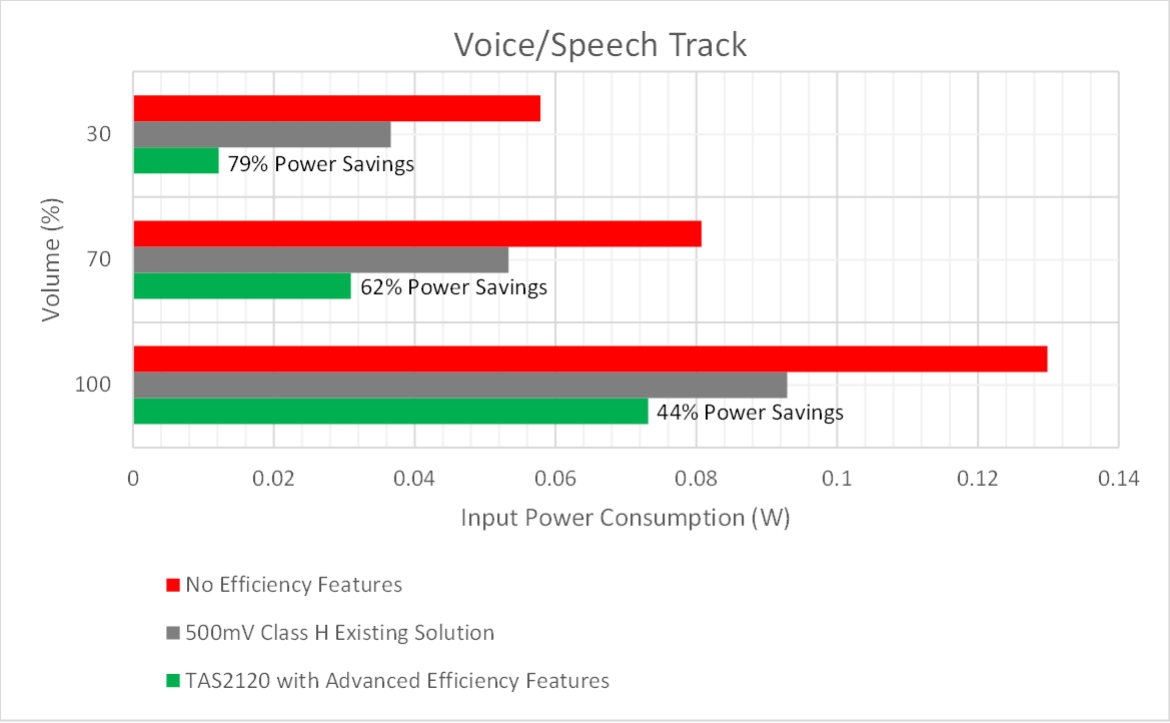

Figure 7-2. Power Consumption Comparison with Voice/Speech Track

Enabling all power-saving features, when playing the Voice/Speech Track, resulted in a significantly greater power consumption reduction when compared to disabling all features. Enabling all efficiency features reduced the overall power consumption by 79% for 30% volume, 62% for 70% volume, and 44% for 100% volume, relative to a configuration with all efficiency features disabled. Furthermore, comparing against the existing 500mV Class-H design, the TAS2120 device can achieve reduced power consumption by 67% for 30% volume, 42% for 70% volume, and 21% for 100% volume.

8 Summary

In conclusion, the TAS2x20 family of audio amplifiers demonstrates a substantial leap forward in power efficiency and performance by consuming less input power compared to the existing designs available in the market. The integration of proprietary technologies, including internal or external Class-H control, music efficiency mode, noise gate, and Y-bridge allows for significant reductions in power consumption while maintaining exceptional audio fidelity. These advanced features empower engineers to create next-generation audio products characterized by reduced size and extended battery life for portable and power-sensitive audio applications ultimately delivering a better user experience.

9 References

1. Texas Instruments, TAS2120: 8.2W Mono Digital Input Class-D Speaker Amp With Integrated 14.75V ClassH Boost, datasheet.
2. Texas Instruments, TAS2320: 15W Mono Digital Input Class-D Speaker Amp With 15V Support, datasheet.
3. Texas Instruments, Efficiency Improvement With Y-Bridge in TAS2x20, TAS257x, application note.

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