AN-2250 LM3533 Evaluation Kit

1 Introduction

The LM3533 Evaluation Module (LM3533EVM) is designed to fully evaluate the LM3533 Dual String backlight driver + 5 indicator LED driver. The LM3533EVM consists of the USB Interface Board and the LM3533 Evaluation Board. The USB Interface Board Rev 1.1 provides the hardware link between a PC and LM3533 Evaluation Board. On the PC side, the LM3533.exe software communicates to the LM3533EVM to provide an easy control over all the features of the LM3533. Both the USB Interface Board and the LM3533 Evaluation Board plug together at the USBL and USBR connectors and are keyed so the boards can only fit together one way.

2 LM3533 Evaluation Board Schematics

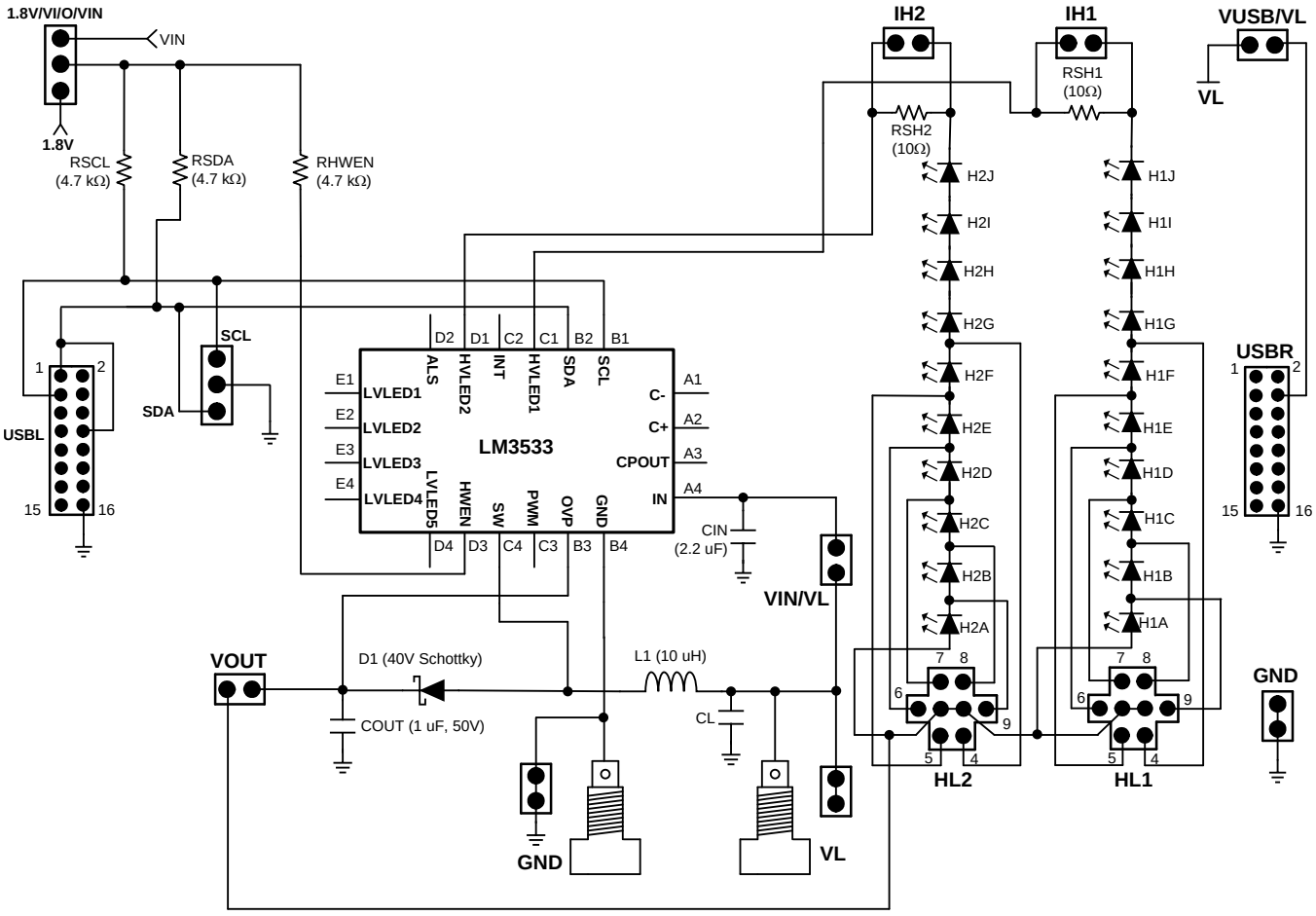

Figure 1. Boost Circuit with Dual 10 Series White LED Strings

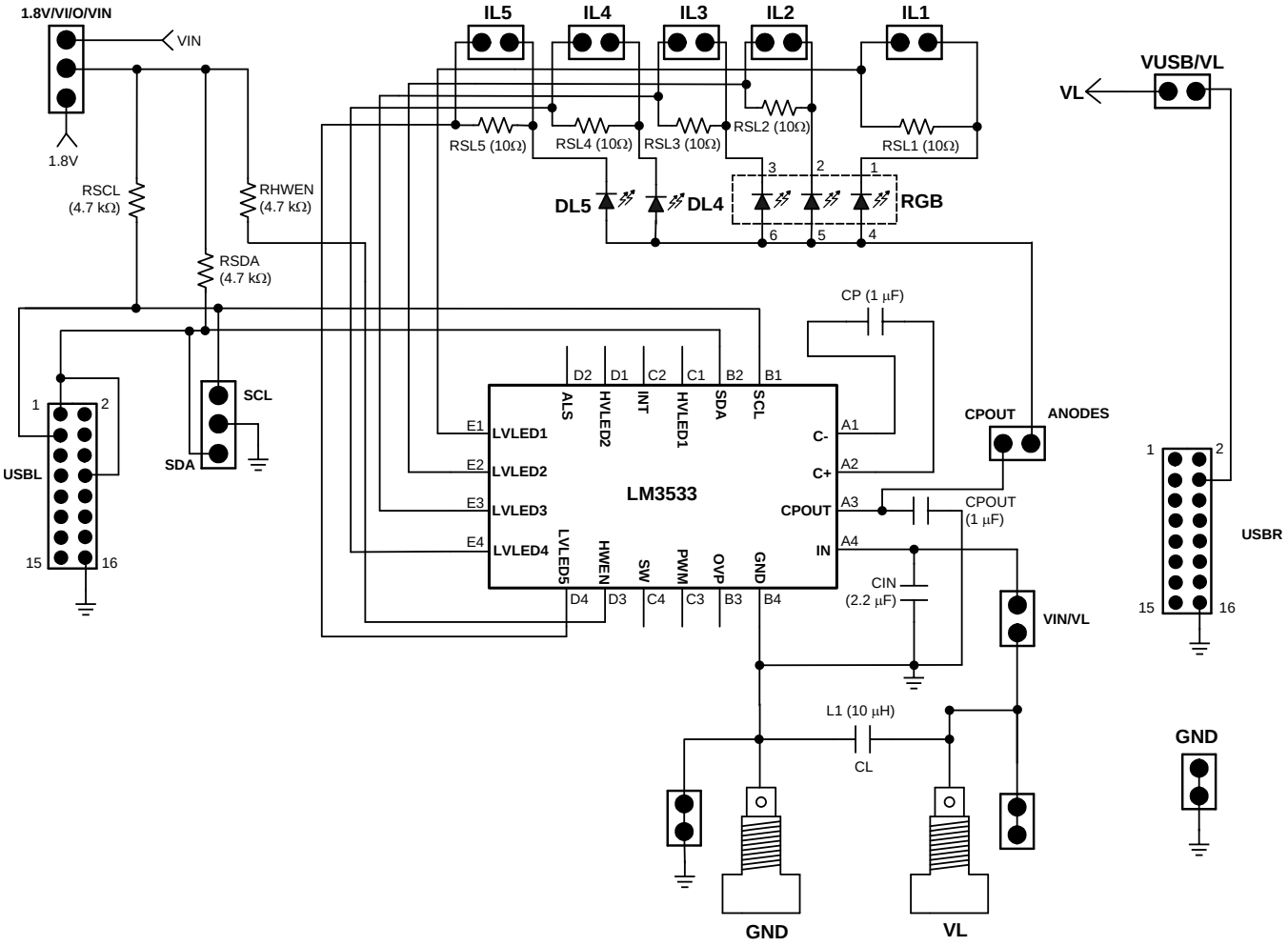

Figure 2. Charge Pump and Low Voltage Indicator LEDs

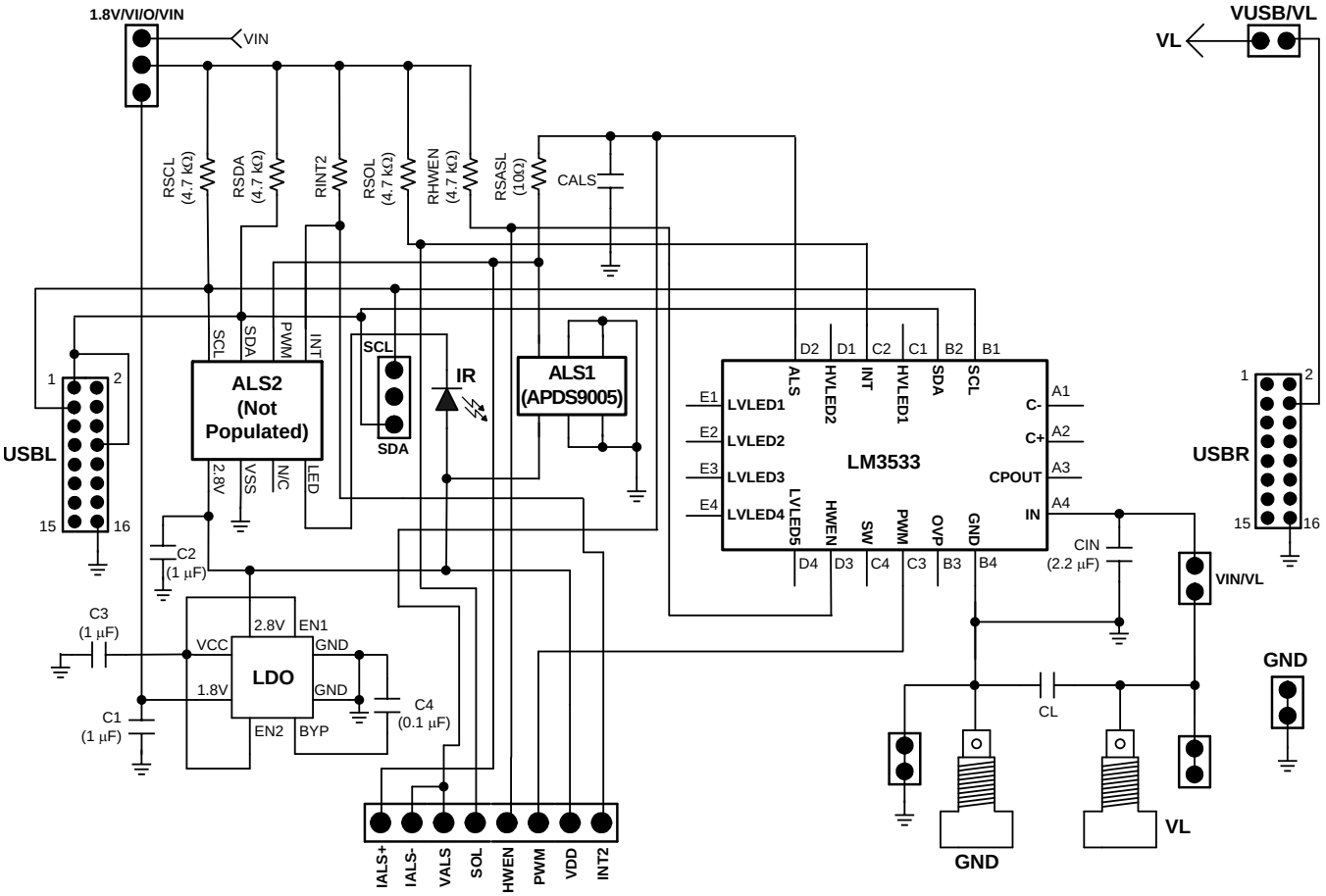

Figure 3. Ambient Light Sensor and Logic Pull-ups

3 Bill of Materials

Component Symbol	Value	Manufacturer	Part #	Size/Package (L x W x H)
LM3533	LED Driver	Texas Instruments	LM3533	(2.015mm × 1.755mm x 0.6mm)
LDO	1.8V/2.8V dual linear regulator	Texas Instruments	LP3986	(1.55mm x 1.55mm x 0.6mm)
RGB	RGB Indicator LEDs	Kingbright	APF3236SURKZGQBDC	(3.6mm x 3.2mm x 1.1mm)
DL4, DL5	Red Indicator LED	Rohm	SML-310VTT86	0603
L1	10µH, I_{SAT} = 1A, R_L = 0.22Ω	TDK	VLF4014ST-100M1R0	(3.8mm x 3.6mmx 1.4mm)
CIN	2.2µF, 10V, X5R	TDK	C1005X5R1A225M	0402
COUT	1µF, 50V, X7R	TDK	C3216X7R1H105M	0805
CPOUT	1µF, 10V, X5R	TDK	C1005X5R1A105K	0402
CP	1µF, 10V, X5R	TDK	C1005X5R1A105K	0402
CL	10µF, 10V	TDK	C1608X5R1A106K	0603
C1 - C4	1µF, 10V, X5R	TDK	C1005X5R1A105K	0402
D1	Schottky, 40V, 250mA	On-Semi	NSR0240V2T1GOSCT-ND	SOD-523
H1A - H1J	White LED	Rohm	SML312WBCW1	0603
H2A - H2J	White LED	Rohm	SML312WBCW1	0603
ALS1	Ambient Light Sensor	Avago	APDS-9005-020	(1.6mm x 1.5mm x 0.55mm)
ALS2	Ambient Light Sensor	N/A	N/A	N/A
RHWEN	4.7kΩ	Vishay	CRCW06034K70JNEA	0603
RSDA	4.7kΩ	Vishay	CRCW06034K70JNEA	0603
RSCL	44.7kΩ	Vishay	CRCW06034K70JNEA	0603
RSOL	4.7kΩ	Vishay	CRCW06034K70JNEA	0603
RSASL	10Ω, 1%	Panasonic	ERJ-3EKF10R0V	0603
RSH1, RSH2	10Ω, 0.01%	Bourns	CRT0805-BY-10R0ELF	0805
RSL1 - RSL5	10Ω, 0.01%	Bourns	CRT0805-BY-10R0ELF	0805

4 Board Layout

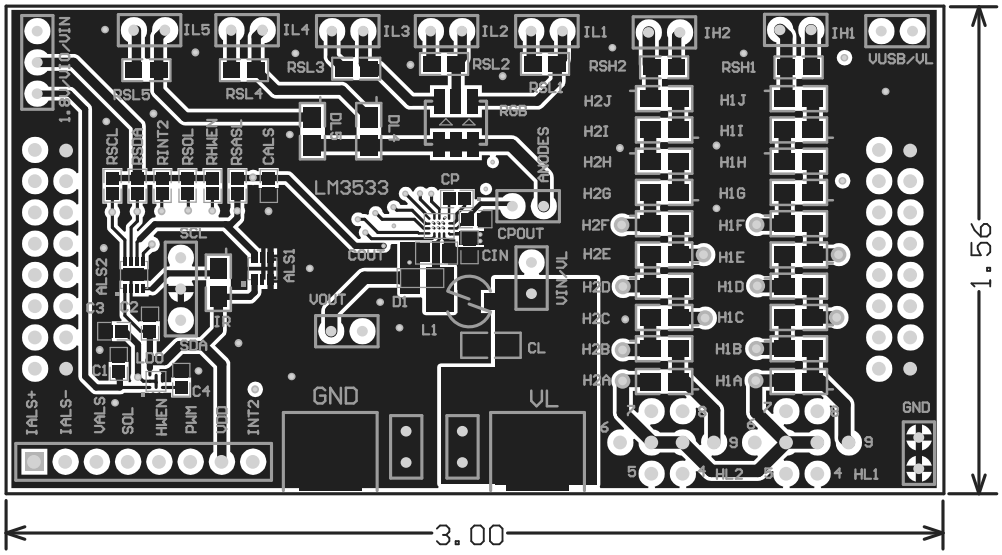

Figure 4. Top Layer

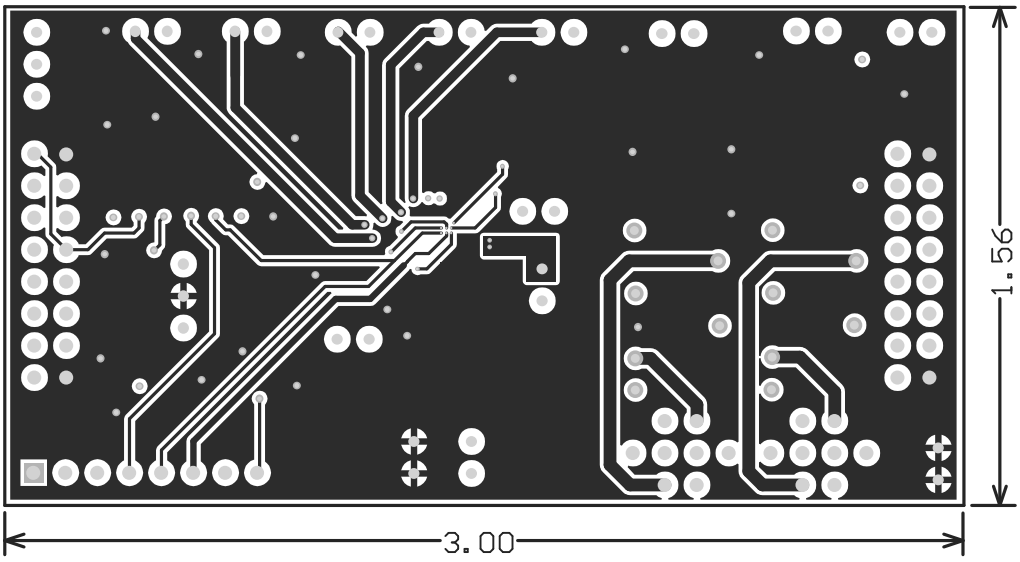

Figure 5. Mid Layer 1

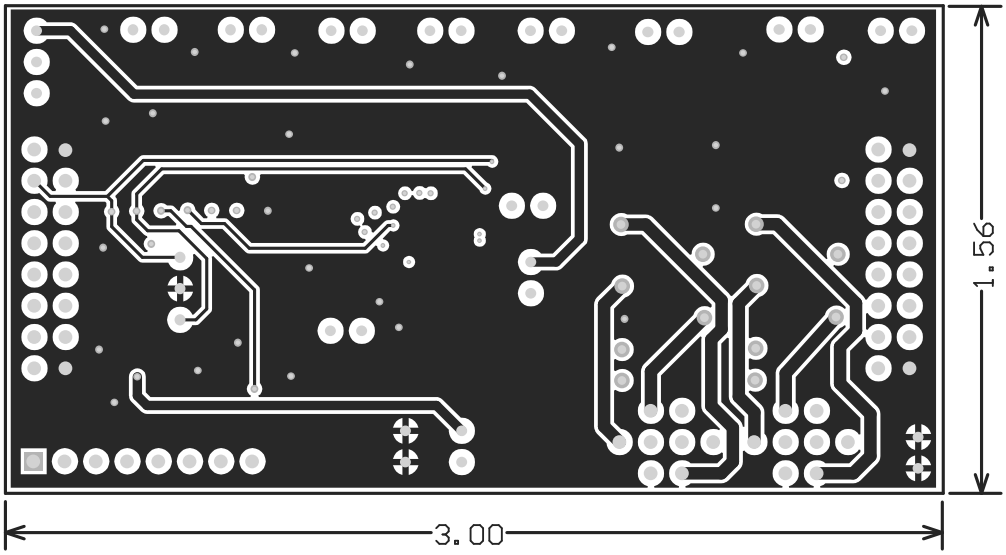

Figure 6. Mid Layer 2

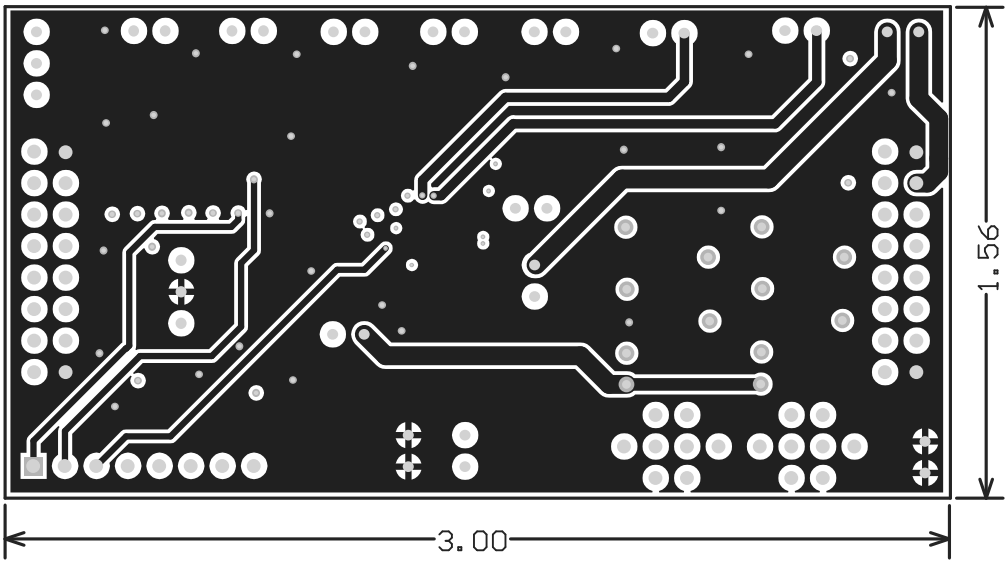

Figure 7. Bottom Layer

5 Board Set-Up

The LM3533EVM requires jumpers installed at the following headers for proper operation:

1. **1.8V/VIO/VIN:** The center pin (VIO) of this three position header connects to the top side of the pull-up resistors (RSCL, RSDA, RSOL, and RHWEN). Jumper this pin to either the 1.8V output from the on board LDO or to VIN.
2. **VOUT:** The VOUT header connects the LM3533's boost output to the top side of the high voltage LED strings (HL1 and HL2)
3. **VIN/VL:** This header jumpers the voltage at VL to the LM3533's IN bump (VIN)
4. **ANODES:** This header jumpers the LM3533's charge pump output to the top side of the low voltage indicator LEDs (RGB, DL4, and DL5)

Once the jumpers are installed, connect a 2.5V to 5.5V power supply to the banana plug inputs (VL) and (GND).

6 USB Interface Board

The LM3533 Evaluation Board can be controlled via an I^2C master by connecting directly to the I^2C header (SCL SDA) or it can be controlled with the USB Interface Board. The USB Interface Board requires the use of the LM3533.exe software that operates from a PC.

To operate the LM3533 Evaluation Board with the USB Interface Board, ensure the LM3533 Evaluation Board is connected to the USB Interface Board. The boards are keyed so they will only fit together one way. Next, follow the jumper settings in Section 5. After this, apply power to the board and open the LM3533.exe program. The LM3533.exe software is grouped into tabs, see the following sections for each tab description.

7 LM3533 Graphical User Interface

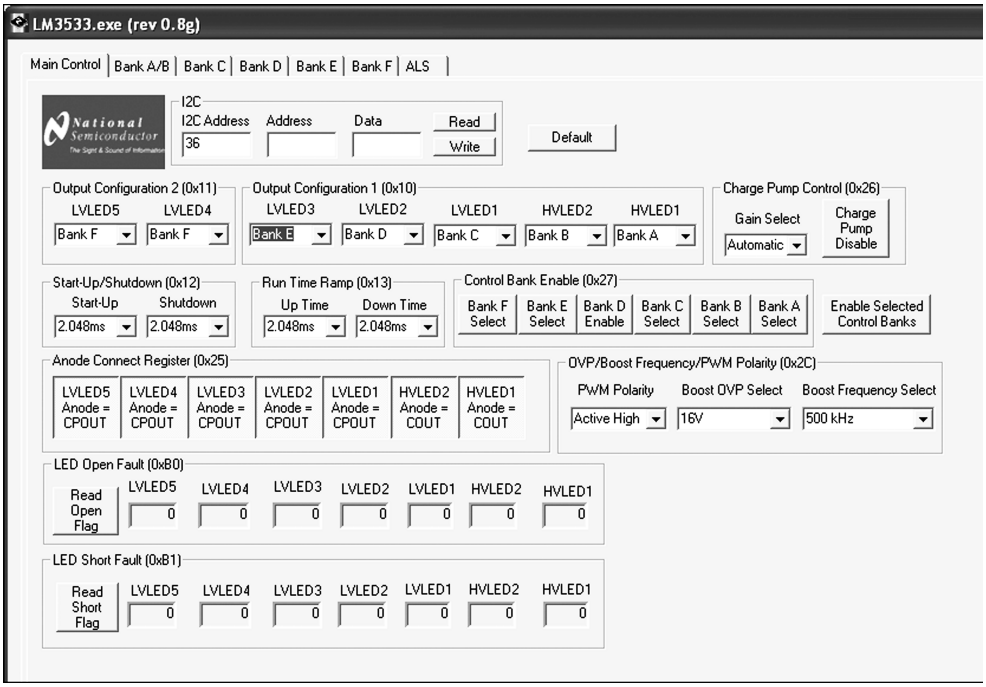

Figure 8. Main Control Tab

7.1 Main Control Tab

The Main Control tab (Figure 8) contains the pulldown menu's and buttons for configuring the LM3533's global registers. The main tab is separated into different sections, where each section represents a specific register within the LM3533. When any of the pulldown menus or buttons are selected the specific data will get written to the LM3533. The exception is for the Control Bank Enable Buttons. These must first be selected and then the Enable Selected Control Banks button must be pressed to write the data. A button that is pushed indicates a 1 is written to the register. A button un-pushed indicates a 0. Table 1 through Table 10 show the break down of each register in the Main Control Tab.

Table 1. Output Configuration 1 (0x10)

Bit [7:6] LVLED3	Bits [5:4] LVLED2	Bits [3:2] LVLED1	Bit [1] HVLED2	Bit 0 HVLED1
00 = LVLED3 is controlled by Control Bank C	00 = LVLED2 is controlled by Control Bank C	00 = LVLED1 is controlled by Control Bank C **(Default)**	0 = HVLED2 is controlled by Control Bank A	0 = HVLED1 is controlled by Control Bank A **(Default)**
01 = LVLED3 is controlled by Control Bank D	01 = LVLED2 is controlled by Control Bank D **(Default)**	01 = LVLED1 is controlled by Control Bank D	1 = HVLED2 is controlled by Control Bank B **(Default)**	1 = HVLED1 is controlled by Control Bank B
10 = LVLED3 is controlled by Control Bank E **(Default)**	10 = LVLED2 is controlled by Control Bank E	10 = LVLED1 is controlled by Control Bank E		
11 = LVLED3 is controlled by Control Bank F	11 = LVLED2 is controlled by Control Bank F	11 = LVLED1 is controlled by Control Bank F		

Table 2. Output Configuration 2 (0x11)

Bits [3:2] LVLED5	Bits [1:0] LVLED4
00 = LVLED5 is controlled by Control Bank C	00 = LVLED4 is controlled by Control Bank C
01 = LVLED5 is controlled by Control Bank D	01 = LVLED4 is controlled by Control Bank D
10 = LVLED5 is controlled by Control Bank E	10 = LVLED4 is controlled by Control Bank E
11 = LVLED5 is controlled by Control Bank F **(Default)**	11 = LVLED4 is controlled by Control Bank F **(Default)**

Table 3. Charge Pump Control (0x26)

Bits [2:1] Gain Select	Bit 0 Charge Pump Disable
0X = Automatic gain select **(Default)** 10 = Gain set at 1x 11 = Gain set at 2x	0 = Charge pump enabled **(Default)** 1 = Charge pump disabled (high impedance from IN to CPOUT)

Table 4. Start-Up/Shutdown (0x12)

Bits [5:3] Start-up Transition Time	Bits [2:0] Shutdown Transition Time
000 = 2.048ms **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 = 2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s Startup time is from when the device is enabled via I^2C to when the initial target current is reached.	000 = 2.048ms **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 = 2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s Shutdown ramp time is from when the device is shutdown via I^2C until the current sink ramps to 0.

Table 5. Run Time Ramp (0x13)

Bits [5:3] Transition Time Ramp Up	Bits [2:0] Transition Time Ramp Down
000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s

Table 6. Control Bank Enable (0x27)

Bit 5 Control F Select	Bit 4 Control E Select	Bit 3 Control D Select	Bit 2 Control C Select	Bit 1 Control B Select	Bit 0 Control A Select
0 = Control Bank F is disabled **(Default)**	0 = Control Bank E is disabled **(Default)**	0 = Control Bank D is disabled **(Default)**	0 = Control Bank C is disabled **(Default)**	0 = Control Bank B is disabled **(Default)**	0 = Control Bank A is disabled **(Default)**
1 = Control Bank F is enabled	1 = Control Bank E is enabled	1 = Control Bank D is enabled	1 = Control Bank C is enabled	1 = Control Bank B is enabled	1 = Control Bank A is enabled

Table 7. Anode Connect (0x25)

Bit 6 LVLED5 Anode Connect	Bit 5 LVLED4 Anode Connect	Bit 4 LVLED3 Anode Connect	Bit 3 LVLED2 Anode Connect	Bit 2 LVLED1 Anode Connect	Bit 1 HVLED2 Anode Connect	Bit 0 HVLED1 Anode Connect
0 = LVLED5 LED anode is not connected to CPOUT	0 = LVLED4 LED anode is not connected to CPOUT	0 = LVLED3 LED anode is not connected to CPOUT	0 = LVLED2 LED anode is not connected to CPOUT	0 = LVLED1 LED anode is not connected to CPOUT	0 = HVLED2 LED string anode is not connected to COUT	0 = HVLED1 LED string anode is not connected to COUT
1 = LVLED5 LED anode is connected to CPOUT **(Default)**	1 = LVLED4 LED anode is connected to CPOUT **(Default)**	1 = LVLED3 LED anode is connected to CPOUT **(Default)**	1 = LVLED2 LED anode is connected to CPOUT **(Default)**	1 = LVLED1 LED anode is connected to CPOUT **(Default)**	1 = HVLED2 LED string anode is connected to COUT **(Default)**	1 = HVLED1 LED string anode is connected to COUT **(Default)**

Table 8. OVP/Boost Frequency/PWM Polarity (0x2C)

Bit 3 PWM Polarity	Bit [2:1] Boost OVP Select	Bit 1 Boost Frequency Select
0 = Active Low Polarity 1 = Active High Polarity **(Default)**	00 = 16V **(Default)** 01 = 24V 10 = 32V 11 = 40V	0 = 500 kHz **(Default)** 1 = 1MHz

Table 9. LED Open Fault (0xB0)

Bit 6 (LVLED5)	Bit 5 (LVLED4)	Bit 4 (LVLED3)	Bit 3 (LVLED2)	Bit 2 (LVLED1)	Bit 1 (HVLED2)	Bit 0 (HVLED1)
0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open

Table 10. LED Short Fault (0xB1)

Bit 6 (LVLED5)	Bit 5 (LVLED4)	Bit 4 (LVLED3)	Bit 3 (LVLED2)	Bit 2 (LVLED1)	Bit 1 (HVLED2)	Bit 0 (HVLED1)
0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short

7.2 Bank A/B Control Tab

The Bank A/B Control Tab (Figure 9) contains all the register options that are unique to the High Voltage Control Banks (A and B). Table 11 through Table 15 describe these registers.

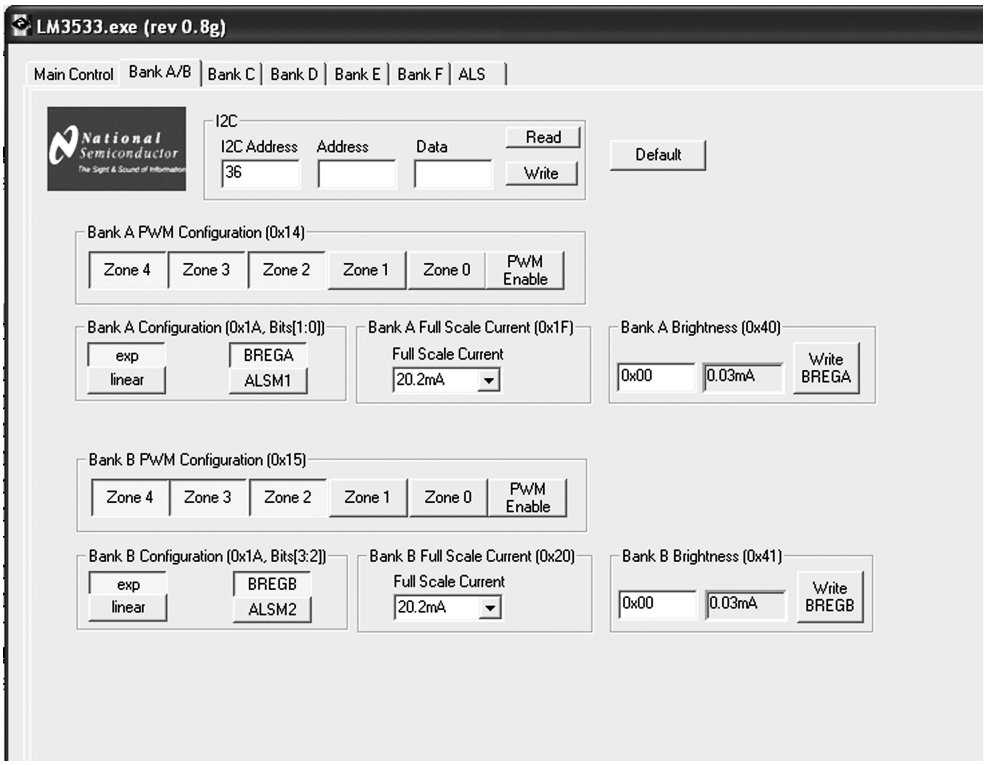

Figure 9. Bank A/B Control Tab

Table 11. Bank A or Bank B PWM Configuration (0x14, 0x15)

Bit 5 Zone 4 PWM Enabled	Bit 4 Zone 3 PWM Enabled	Bit 3 Zone 2 PWM Enabled	Bit 2 Zone 1 PWM Enabled	Bit 1 Zone 0 PWM Enabled	Bit 0 PWM Enabled
0 = PWM input is disabled in Zone 4	0 = PWM input is disabled in Zone 3	0 = PWM input is disabled in Zone 2	0 = PWM input is disabled in Zone 1 **(Default)**	0 = PWM input is disabled in Zone 0 **(Default)**	0 = PWM Input is disabled **(Default)**
1 = PWM input is enabled in Zone 4 **(Default)**	1 = PWM input is enabled in Zone 3 **(Default)**	1 = PWM input is enabled in Zone 2 **(Default)**	1 = PWM input is enabled in Zone 1	1 = PWM input is enabled in Zone 0	1 = PWM Input is enabled

Table 12. Bank A Configuration (0x1A, Bits[1:0])

Bit 1 Control Bank A Mapping Mode	Bit 0 BREGA/ALSM1 Control
0 = Exponential Mapping **(Default)**	0 = Control Bank A is configured for Brightness Register Current Control **(Default)**
1 = Linear Mapping	1 = Control Bank A is configured for ALS current control via the ALSM1 Zone Target Registers

Table 13. Bank A or Bank B Full Scale Current (0x1F, 0x20)

Bits [4:0] Full-Scale Current (800µA per setting)
00000 = 5mA
:
:
10011 = 20.2mA **(Default)**
:
:
11111 = 29.8mA

Table 14. Bank B Configuration (0x1A, Bits[3:2])

Bit 3 Control Bank B Mapping Mode	Bit 2 BREGB/ALSM2 Control
0 = Exponential Mapping **(Default)**	0 = Control Bank B is configured for Brightness Register Current Control **(Default)**
1 = Linear Mapping	1 = Control Bank B is configured for ALS current control via the ALSM2 Zone Target Registers

Table 15. Bank A and Bank B Brightness (0x40, 0x41)

Brightness Code Bits[7:0}
When the Mapping Mode is set for exponential mapping (Control Bank X Brightness Configuration Register, Bit [2] = 0), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code$ (1)
When the Mapping Mode is set for linear mapping (Control Bank X Brightness Configuration Register, Bit [2] = 1), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]}$ (2)

7.3 Bank C, D, E, and F Tab

Each low voltage Control Bank (C, D, E, and F) has its own tab. Each tab has all the register options that are unique to each of the low voltage control banks and the pattern generators. Table 16 through Table 24 describe these registers.

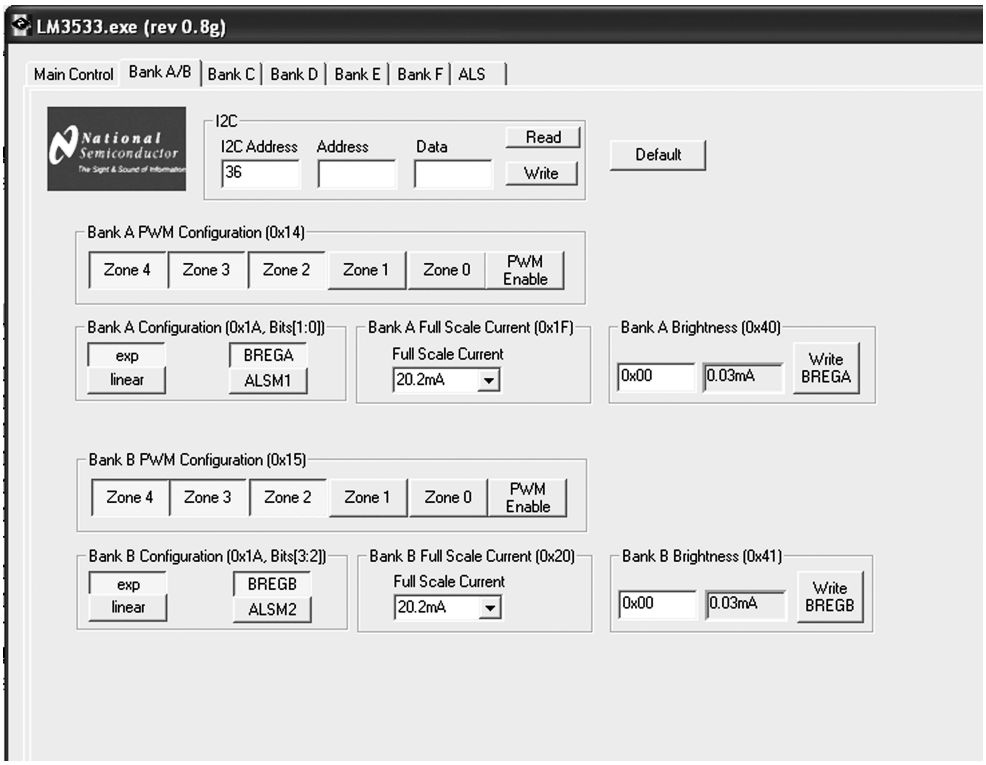

Figure 10. Low Voltage Control Bank Tab

Table 16. Bank (C/D/E/F) Configuration (0x1B, 0x1C, 0x1D, 0x1E), Bits[2:0]

Bit 2 Mapping Mode	Bits [1:0] Current Control
0 = Exponential Mapping **(Default)**	0X = Control Bank_ is configured for Brightness Register Current Control via the respective Brightness Register **(Default)**
1 = Linear Mapping	10 = Control Bank_ is configured for ALS current control via the ALSM2 Zone Target Registers
	11 = Control Bank_ is configured for ALS current control via the ALSM3 Zone Target Registers

Table 17. Bank C/D/E/F High Brightness (0x42, 0x43, 0x44, 0x45)

Brightness Code Bits[7:0}
When the Mapping Mode is set for exponential mapping (Control Bank_Brightness Configuration Register Bit [2] = 0), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code$ (3)
When the Mapping Mode is set for linear mapping (Control Bank_Brightness Configuration Register Bit [2] = 1), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]}$ (4)

Table 18. Bank (C/D/E/F) Full Scale Current (0x21, 0x22, 0x23, 0x24)

Bits [4:0] Full-Scale Current (800µA per setting)
00000 = 5mA
:
:
10011 = 20.2mA **(Default)**
:
:
11111 = 29.8mA

Table 19. Bank (C/D/E/F) PWM Configuration (0x16, 0x17, 0x18, 0x19)

Bit 5 Zone 4	Bit 4 Zone 3	Bit 3 Zone 2	Bit 2 Zone 1	Bit 1 Zone 0	Bit 0 PWM Enabled
0 = PWM input is disabled in Zone 4	0 = PWM input is disabled in Zone 3	0 = PWM input is disabled in Zone 2	0 = PWM input is disabled in Zone 1 **(Default)**	0 = PWM input is disabled in Zone 0 **(Default)**	0 = PWM Input is disabled **(Default)**
1 = PWM input is enabled in Zone 4 **(Default)**	1 = PWM input is enabled in Zone 3 **(Default)**	1 = PWM input is enabled in Zone 2 **(Default)**	1 = PWM input is enabled in Zone 1	1 = PWM input is enabled in Zone 0	1 = PWM Input is enabled

The PGEN Enable field in the low voltage control bank tabs is mirrored for each tab. Once a check box is selected, the Enable Selected Patterns button must be pushed to write the specific bit to register 0x28. A checked box means a 1 is being written and an empty box means a 0 is bing written.

Table 20. PGEN Enable (0X28, Bits[0, 2, 4, 6])

Bit 6 Pattern 4 Enable	Bit 4 Pattern 3 Enable	Bit 2 Pattern 2 Enable	Bit 0 Pattern 1 Enable
0 = Pattern 4 Disabled **(Default)**	0 = Pattern 3 Disabled **(Default)**	0 = Pattern 2 Disabled **(Default)**	0 = Pattern 1 Disabled **(Default)**
1 = Pattern 4 Enabled	1 = Pattern 3 Enabled	1 = Pattern 2 Enabled	1 = Pattern 1 Enabled

Each low voltage control bank has its own pattern generator control. Bank C has Pattern Generator 1, Bank D has Pattern Generator 2, Bank E has Pattern Generator 3, and Bank F has Pattern Generator 4. Each pattern generator has registers that control the pulse high time, pulse low time, pulse rise time, pulse fall time, pulse delay from when the pattern is enabled, and the pulse low brightness. The pulse high brightness is the same as the high brightness register for the particular Control Bank.

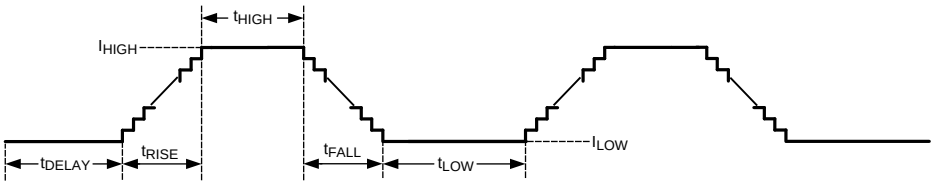

Figure 11. Pattern Generator Timing

Table 21. Low Time(s) (0x71, 0x81, 0x91, 0xA1)

Bit [7:0] t_{LOW} times
0x00 = 16.384ms (16.384ms/step) **(Default)**
0x01 = 32.768ms
:
0x3B = 983.05ms
0x3C = 999.424ms
0x3D = 1130.496ms (131.072ms/step)
0x3E = 1261.568ms
:
0x7F = 9781.248ms
0x80 = 10.305536s (524.288ms/step)
:
0xFF = 76.890112s

Table 22. High Time(s) (0x72, 0x82, 0x92, 0xA2)

Bit [6:0] t_{HIGH} times
0x00 = 16.384ms (16.384ms/step) **(Default)**
0x01 = 32.768ms
:
0x3B = 983.05ms
0x3C = 999.424ms
0x3D = 1130.496ms (131.072ms/step)
0x3E = 1261.568ms
:
0x7F = 9781.248ms

For Exponential Mapping Mode the low-level current becomes:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \quad (5)$$

For Linear Mapping Mode the low-level current becomes:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]} \quad (6)$$

7.4 LOW BRIGHTNESS (0x73, 0x83, 0x93, 0xA3)

Table 23. Rise Time (0x74, 0x84, 0x94, 0xA4)

Bits [2:0] t_{RISE} (from I_{LOW} to I_{HIGH})
000 = 2048µs **(Default)**
001 = 262ms
010 = 524ms
011 = 1.049s
100 = 2.097s
101 = 4.194s
110 = 8.389s
111 = 16.78s

Table 24. Fall Time (0x75, 0x85, 0x95, 0xA5)

Bits [2:0] t_{FALL} (from I_{HIGH} to I_{LOW})
000 = 2048µs **(Default)**
001 = 262ms
010 = 524ms
011 = 1.049s
100 = 2.097s
101 = 4.194s
110 = 8.389s
111 = 16.78s

7.5 ALS TAB

The Ambient Light Sensor (ALS) tab (Figure 12) contains all the registers that are applicable to the LM3533's ALS interface. Table 25 through Table 34 describe these registers.

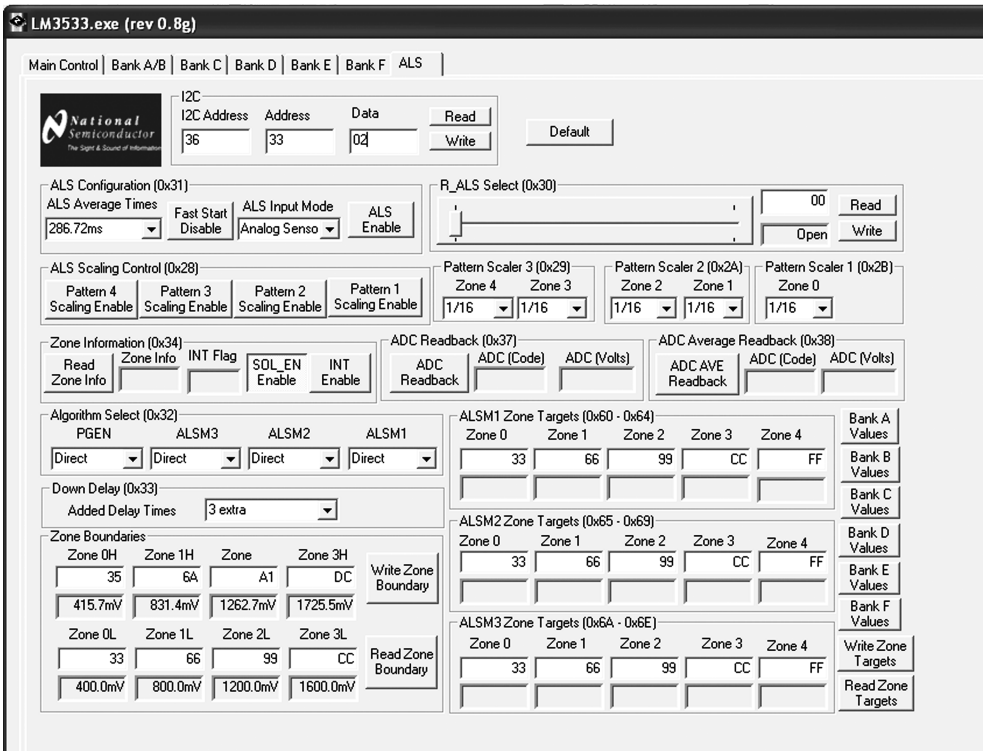

Figure 12. ALS Tab

Table 25. ALS Configuration (0x31)

Bits [5:3] ALS Average Times	Bit 2 Fast startup Enable/Disable	Bit 1 ALS Input Mode	Bit 0 ALS Enable/Disable
000 = 17.92 ms 001 = 35.84ms 010 = 71.68ms 011 = 143.36ms 100 = 286.72ms **(Default)** 101 = 573.44ms 110 = 1146.88ms 111 = 2293.76ms	0 = ALS fast startup is enabled **(Default)** 1 = ALS fast startup is disabled	0 = ALS is set for Analog Sensor Input Mode **(Default)** 1 = ALS is set for PWM Sensor Input Mode	0 = ALS is disabled **(Default)** 1 = ALS is enabled

Table 26. Algorithm Select (0X32)

Bits [7:6] PGEN	Bits [5:4] ALSM3	Bits [3:2] ALSM2	Bits [1:0] ALSM1
00 = Direct Control **(Default)**	00 = Direct Control **(Default)**	00 = Direct Control **(Default)**	00 = Direct Control (**default**)
01 = Up Only Control	01 = Up Only Control	01 = Up Only	01 = Up Only
1X = Down Delay Control	1X = Down Delay Control	1X = Down Delay	1X = Down Delay

Table 27. Down Delay (0x33)

Bits [4:0] Down Delay Settings (# Indicates total average periods required to force a change in the down direction)
00000 = 6 **(Default)**
:
:
:
11111 = 37

Table 28. Zone Information (0x34)

Bits [4:2] Average Zone Information Bits	Bit 1 Zone Change Bit	Bit 0 Interrupt Enable Bit
000 = Zone 0 **(Default)** 001 = Zone 1 010 = Zone 2 011 = Zone 3 1XX = Zone 4	0 = no change in the ALS zone since the last read back of this register **(Default)** 1 = the ALS zone has changed. A read back of this	0 = INT Mode Disabled **(Default)** 1 = INT Mode Enabled

Table 29. ADC Readback (0x37)

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Data	Data	Data	Data	Data	Data	Data	Data

Table 30. Read-Average ADC Register (ADDRESS 0x38)

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Data	Data	Data	Data	Data	Data	Data	Data

Table 31. Zone Boundaries

Name	Address	Function
Zone 0H	0x50	ALS Zone Boundary 0 High
Zone 0L	0x51	ALS Zone Boundary 0 Low
Zone 1H	0x52	ALS Zone Boundary 1 High
Zone 1L	0x53	ALS Zone Boundary 1 Low
Zone 2H	0x54	ALS Zone Boundary 2 High
Zone 2L	0x55	ALS Zone Boundary 2 Low
Zone 3H	0x56	ALS Zone Boundary 3 High
Zone 3L	0x57	ALS Zone Boundary 3 Low

Note: Each Zone Boundary register is 8 bits with a maximum voltage of 2V. This gives a step size for each Zone Boundary Register bit of:

$$\text{ZoneBoundaryLSB} = \frac{2V}{255} = 7.8\ \text{mV} \quad (7)$$

Table 32. ALSM1 Zone Target Registers (ADDRESS 0x60 - 0x64)

Address	Function
0x60	ALSM1 Zone Target 0
0x61	ALSM1 Zone Target 1
0x62	ALSM1 Zone Target 2
0x63	ALSM1 Zone Target 3
0x64	ALSM1 Zone Target 4

Table 33. ALSM2 Zone Target Registers (ADDRESS 0x65 - 0x69)

Address	Function
0x65	ALSM2 Zone Target 0
0x66	ALSM2 Zone Target 1
0x67	ALSM2 Zone Target 2
0x68	ALSM2 Zone Target 3
0x69	ALSM2 Zone Target 4

Table 34. ALSM3 Zone Target Registers (ADDRESS 0x6A - 0x6E)

Address	Function
0x6A	ALSM3 Zone Target 0
0x6B	ALSM3 Zone Target 1
0x6C	ALSM3 Zone Target 2
0x6D	ALSM3 Zone Target 3
0x6E	ALSM3 Zone Target 4

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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