# bq24170EVM Stand-Alone Synchronous, Switch-Mode, Battery-Charge Controller With Integrated N-MOSFETs and Power Path Selector

This user's guide describes the features and operation of the bq24170EVM Evaluation Module (EVM). The EVM assists users in evaluating the bq24170 synchronous battery charger. The EVM is also called the HPA610A. The manual includes the bq24170EVM bill of materials, board layout, and schematic.

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# 1 Introduction

## 1.1 EVM Features

- Evaluation module for bq24170
- Stand-alone synchronous switch-mode, battery-charge controller
- Integrated N-MOSFETs and power path selector
- CELL pin setting up to 12.6-V battery voltage; 1, 2, or 3 cells with 4.2 V/cell
- Input operating range: 4.5 V–16 V
- LED indication for charge status
- Test points for key signals available for testing purposes; easy probe hook-up.
- Jumpers available; easy-to-change setting

## 1.2 General Description

The bq24170 is highly integrated stand-alone Li-ion and Li-polymer switch-mode battery charge controllers with two integrated N-channel power MOSFETs and power path selector gate driver. It offers a constant-frequency synchronous PWM controller with high accuracy regulation of input current, charge current and voltage. It also provides battery detection, pre-conditioning, charge termination, and charge status monitoring.

The bq24170 automatically enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage. The bq24170 charges one, two or three cells (selected by CELL pin), supporting up to a 4-A charge current. The bq24170 is available in a 24-pin, 3.5 x 5.5 $mm^2$, thin QFN package.

For details, see the bq24170 data sheet (SLUSAD2).

## 1.3 I/O Description

**Table 1. I/O Description**

| Jack | Description |
|---|---|
| J1–VIN | Positive input |
| J1–PGND | Negative input |
| J2–VSYS | Connected to system |
| J2–VBAT | Connected to charger output |
| J2–PGND | Ground |
| J2–TS_EXT | Temperature qualification voltage Input |

## 1.4 Control and Key Parameters Settings

**Table 2. Control and Key Parameters Settings**

| Jack | Description | Factory Setting |
|---|---|---|
| JP1 | Select external TS input or internal valid TS setting<br>1-2 : External TS input<br>2-3 : Internal valid TS setting | Jumper ON 1-2 (external TS) |
| JP2 | The pullup power source supplies the LEDs when JP2 is ON. LED has no power source when JP2 is OFF. | Jumper ON (LED power available) |
| JP3 | TTC setting<br>2-3 : Connect TTC to VREF to enable termination and disable timer<br>1-2 : Connect TTC to GND to disable termination and disable timer<br>OPEN : Enable timer and termination | Jumper OPEN (enable timer and termination) |
| JP4 | Charger enable/disable setting. ISET is pulled to GND and the charger is disabled when JP4 OPEN; charger is enabled when JP4 is ON. | Jumper OPEN (disable charger) |
| JP5 | CELL selection<br>1-2 : CELL-GND, 1CELL<br>2-3 : CELL-VREF, 3CELL<br>OPEN: CELL- FLOAT, 2CELL | Jumper ON 1-2 (1 CELL) -001<br>Jumper ON 2-3 (3 CELL) -002 |

## 1.5 Recommended Operating Conditions

**Table 3. Recommended Operating Conditions**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage, $V_{BUS}$ | Input voltage | 4.5 | | 8 | V | 001 |
| Supply voltage, $V_{BUS}$ | Input voltage | 6 | | 18 | V | 002 |
| Battery voltage, $V_{BAT}$ | Voltage applied at VBAT terminal of J2 | 2.1 | | 4.2 | V | 001 |
| Battery voltage, $V_{BAT}$ | Voltage applied at VBAT terminal of J2 | 2.1 | | 12.6 | V | 002 |
| Supply current | Maximum input current | 0 | | 8 | A | |
| Charge current, $I_{chrg}$ | Battery charge current | 0 | 2 | 4 | A | |
| Operating junction temperature range, $T_J$ | | 0 | | 125 | °C | |

The bq2410 EVM board requires a regulated supply approximately 1 V minimum above the regulated voltage of the battery pack to a maximum input voltage of 16 Vdc. The bq24170 uses the CELL pin to select the number of cells with a fixed 4.2 V/cell. Connecting CELL to AGND gives a 1-cell configuration, a floating CELL pin gives a 2-cell configuration, and connecting to VREF gives a 3-cell configuration. The CELL pin adjusts the internal resistor voltage divider from the BAT pin to AGND pin for voltage feedback and regulate to internal 2.1-V voltage reference.

| CELL Pin | Voltage Regulation |
|---|---|
| AGND | 4.2V |
| Floating | 8.4V |
| VREF | 12.6V |

For Noye 001, the BAT voltage is set to 4.2 V and for Note 002, the BAT voltage is set to 12.6 V.

The ISET input sets the maximum charging current. Battery current is sensed by current sensing resistor $R_{SR}$ connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 40 mV maximum. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET}}{20 \times R15} \quad (1)$$

For bq24170, the precharge current is set as 1/10 of the fast-charge rate set by ISET voltage, according to the formula

$$I_{PRECHARGE} = \frac{V_{ISET}}{200 \times R15} \quad (2)$$

The default setting is 2 Adc for fast-charge current and 0.2 Adc for precharge current.

In the bq24170, once the voltage on OVPSET is above the 1.6-V ACOV threshold or below the 0.5-V ACUV threshold, the charge is disabled, and the battery is switched to the system instead of the adapter.

$$V_{ACUV} = 0.5\ V \times \left( 1 + \frac{R6}{R9} \right) \quad (3)$$

For Note 001, ACUV = 2.51 V; for Note 002, ACUV = 5.87 V.

$$V_{ACOV} = 1.6\ V \times \left( 1 + \frac{R6}{R9} \right) \quad (4)$$

For Note 001, ACOV = 8.03 V; for Note 002, ACOV = 18.80 V.

Similar to setting battery regulation current, the adapter current is set by the voltage on ACSET pin using the following equation:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R2} \quad (5)$$

The default setting on the EVM is 2 Adc (Note 001), 4 Adc (Note 002) for adapter current regulation.

# 2 Test Summary

## 2.1 Definitions

This procedure details how to configure the HPA610A evaluation board. On the test procedure the following naming conventions are followed.

| | |
|---|---|
| VXXX : | External voltage supply name (VIN, VBAT, VTS) |
| LOADW: | External load name (LOADR, LOADI) |
| V(TPyyy): | Voltage at internal test point TPyyy. For example, V(TP1) means the voltage at TP1. |
| V(Jxx): | Voltage at jack terminal Jxx. |
| V(TP(XXX)): | Voltage at test point XXX. For example, V(ACSET) means the voltage at the test point which is marked as ACSET. |
| V(XXX, YYY): | Voltage across point XXX and YYY. |
| I(JXX(YYY)): | Current going out from the YYY terminal of jack XX. |
| Jxx(BBB): | Terminal or pin BBB of jack xx |
| Jxx ON : | Internal jumper Jxx terminals are shorted |
| Jxx OFF: | Internal jumper Jxx terminals are open |
| Jxx (-YY-) ON: | Internal jumper Jxx adjacent terminals marked as YY are shorted |
| Measure:→A,B | Check specified parameters A, B. If measured values are not within specified limits, the unit under test has failed. |
| Observe: →A,B | Observe if A, B occur. If they do not occur, the unit under test has failed. |

Assembly drawings have location for jumpers, test points, and individual components.

## 2.2 Safety

1. Safety Glasses are to be worn.
2. This test must be performed by qualified personnel who are trained in electronics theory and understand the risks and hazards of the assembly to be tested.
3. ESD precautions must be followed while handling electronic assemblies and performing this test.
4. Precautions must be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

## 2.3 Quality

1. Test data can be made available on request from Texas Instruments.

## 2.4 Safety Apparel

1. Electrostatic smock
2. Electrostatic gloves or finger cots
3. Safety glasses
4. Ground ESD wrist strap.

## 2.5 Equipment

### 2.5.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 30 V at 5 A is required.

### 2.5.2 Loads

LOAD#1 A 30-V (or greater), 5-A (or greater) electronic load that can operate at constant current and constant voltage mode.

LOAD#2: An HP 6060B 3-V to 60-V/0-A to 60-A, 300-W system dc electronic load or equivalent.

### 2.5.3 Meters

Seven Fluke 75 multimeters (equivalent or better) or four equivalent voltage meters and three equivalent current meters.

The current meters must be capable of measuring 5-A+ current.

## *2.6 Equipment Setup*

1. Set the Power Supply #1 (PS#1) for 6-V ±200-mVdc (001), or 16-V ±0.200-mV (002),4.5-A ±0.1-A current limit, and then turn off supply.
2. Connect the output of PS#1 in series with a current meter (multimeter) to J1 (VIN, PGND).
3. Connect a voltage meter across J1 (VIN, PGND).
4. Connect Load#1 in series with a current meter to J2 (VBAT, PGND). Turn off Load#1.
5. Connect Load#2 in series with a current meter to J2 (VSYS, PGND). Turn off Load#2.
6. Connect a voltage meter across J2 (VBAT, PGND).
7. Connect a voltage meter across J2 (VSYS, PGND).
8. Check all jumper shunts. JP1: connect 2-3 (External TS); JP2: ON; JP3: OPEN; JP4: OPEN. JP5: connect 1-2 for 001 and connect 2-3 for 002.

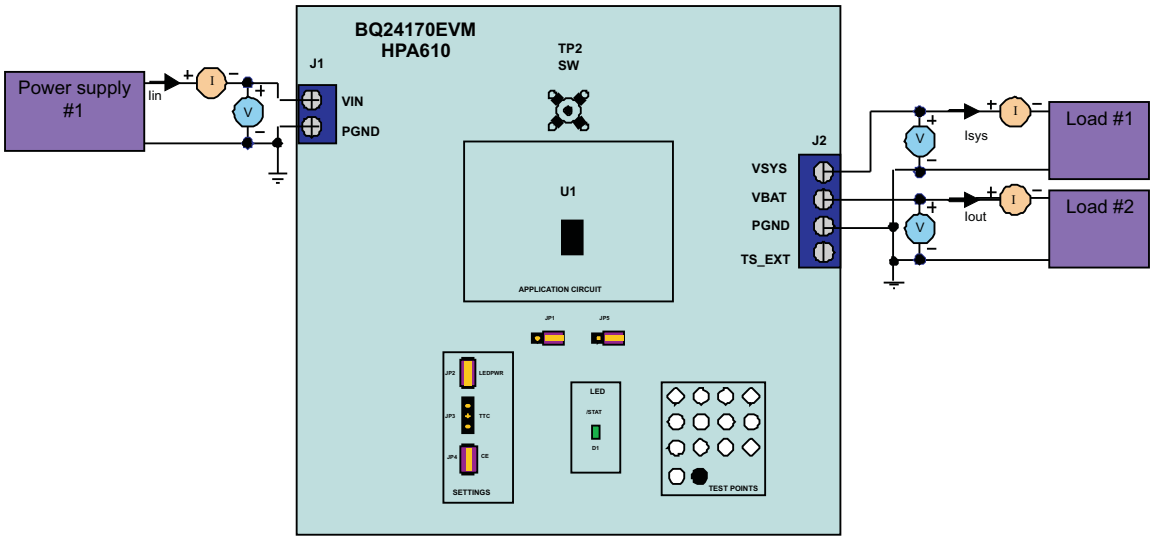


**Figure 1. Original Test Setup for HPA610A (bq24710EVM)**

## 2.7 Procedure

Disconnect the load and power supply. Use diode-function of multimeter to check the resistance between J1-VIN and J2-VSYS. Pass only if both OPEN for bi-direction (positive J1-VIN and negative on J2-VSYS; negative J1-VIN and positive on J2-VSYS).

### 2.7.1 Power Supply and VREF

Make sure that Section 2.6 steps are followed.

Disconnect LOAD#1#2. Turn on PS#1 (6 V for 001 and 16 V for 002).

*Measure* → V(J2(VSYS)) = 6 V ±500 mV (001)
V(J2(VSYS)) = 16 V ±500 mV (002)
*Measure* → V(J2(VBAT)) = 0.5 V ±500 mV
*Measure* → V(TP(VREF)) = 3.3 V ±200 mV
*Measure* → V(TP(REGN)) = 0.5 V ±500 mV

### 2.7.2 Charger Enable and Battery Detection

Connect 2-3 of JP1 (Internal TS); short JP4 (Charger Enable)

*Measure* → V(TP(VREF)) = 3.3 V ±200 mV
*Measure* → V(TP(REGN)) = 6 V ±200 mV
*Observe* → V(J2(VBAT)) = 4.2 V ±200 mV (001)
V(J2(VBAT)) = 12.6 V ±200 mV (002)
*Observe* → D1 (/STAT) BLINK

### 2.7.3 Charge Current/Voltage Regulation and Battery Temperature Qualification

Reconnect LOAD#2, and turn on. Use the constant voltage mode. Set the output voltage to 2.5 V for 001 and 8 V for 002.

*Measure* → I(J2(VBAT)) = 0.2 A ±100 mA
*Observe* → D1 (/STAT) ON

Increase the voltage of LOAD#2 to 3.5 V for 001 and 10.5 V for 002.

*Measure* → I(J2(VBAT)) = 2 A ±200 mA
*Observe* → D1 (/STAT) ON

Open 2-3 of JP1 (External TS)

*Measure* → I(J2(VBAT)) = 0 A ±100 mA
*Observe* → D1 (/STAT) BLINK

Connect 2-3 of JP1 (Internal TS)

*Measure* → I(J2(VBAT)) = 2 A ±200 mA
*Observe* → D1 (/STAT) ON

### 2.7.4 Charger Termination and Recharge

Increase the voltage of LOAD#2 slowly to approximately 4.2 V for Note 001 and 12.6 V for Note 002.

*Observe* → I(J2(VBAT)) decreases from 2 A while V(J2(VBAT)) becomes constant.
*Observe* → I(J2(VBAT)) drops to zero when LOAD#2 current is less than 0.2 A.

Decrease the voltage of LOAD#2 slowly to approximately 3.5 V for Note 001 and 10.5 V for Note 002.

*Measure* → I(J2(VBAT)) = 2 A ±200 mA.

*Observe* → D1 (/STAT) ON.

### 2.7.5 OVP - Input Overvoltage Protection

Increase the voltage of PS#1 to 9 V for Note 001 or 20 V for Note 002.

*Measure* → I(J1(VIN)) = 0 A ±200 mA.

*Observe* → D1 (/STAT) BLINK.

### 2.7.6 DPM - Input Current Regulation

Connect the output of the Load#1 in series with a current meter (multimeter) to J2 (SYS, PGND). Ensure that a voltage meter is connected across J2 (SYS, PGND). Resume other status as in Section 2.7.3.

Turn on the power of Load#1. Set the load current to 0.1 A (Note 001) or 1.5 A (Note 002). Increase the load current until I(J1(VIN)) = 2 A (Note 001) or 4 A (Note 002).

*Observe* → I(J2(VBAT)) decreases from 2 A to 0 A and I(J1(VIN)) and keeps 2 A (Note 001) or 4 A (Note 002) unchanged.

### 2.7.7 Test Complete

Turn off the power supply, and remove all connections from the unit under test (UUT).

## 3 PCB Layout Guideline

1. It is critical that the exposed thermal pad on the backside of the bq24170 package be soldered to the PCB ground. Ensure that sufficient thermal vias are right underneath the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage must be routed separately. At each layer, the signal ground and the power ground are connected only at the thermal pad.
3. Charge current sense resistor must be connected to SRP and SRN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins must be placed as close to the IC as possible.
4. Input current sense resistor must be connected to ACP, ACN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.
5. Decoupling capacitors for VREF, AVCC, and REGN must make the interconnections to the IC as short as possible.
6. Decoupling capacitors for BAT must be placed close to the corresponding IC pins, and make the interconnections to the IC as short as possible.
7. Decoupling capacitor(s) for the charger input must be placed close to SW and PGND.
8. Take the EVM layout for design reference.

# 4 Bill of Materials, Board Layout, and Schematic

## 4.1 Bill of Materials

**Table 4. Bill of Materials**

| Count | | | | | | | |
|---|---|---|---|---|---|---|---|
| -001 | -002 | RefDes | Value | Description | Size | Part Number | MFR |
| 4 | 4 | C1, C7, C14, C15 | 10uF | Capacitor, Ceramic, 25V, X7R, 10% | 1206 | STD | STD |
| 0 | 0 | C2 | Open | | | | |
| 1 | 1 | C3 | 2.2uF | Capacitor, Ceramic, 25V, X7R, 10% | 0805 | STD | STD |
| 1 | 1 | C4 | 330pF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | STD | STD |
| 2 | 2 | C5, C18 | 0.1uF | Capacitor, Ceramic, 16V, X7R, 10% | 0603 | STD | STD |
| 2 | 2 | C6,C13 | 0.047uF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | STD | STD |
| 3 | 3 | C8, C16, C17 | 1.0uF | Capacitor, Ceramic, 25V, X7R, 10% | 0805 | STD | STD |
| 1 | 1 | C9 | 4700pF | Capacitor, Ceramic, 25V, X7R, 10% | 0603 | STD | STD |
| 3 | 3 | C10, C20, C24 | 0.1uF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | STD | STD |
| 0 | 0 | C11, C12, C21, C23 | Open | | | | |
| 2 | 2 | C22, C19 | 1.0uF | Capacitor, Ceramic, 16V, X7R, 20% | 0805 | STD | STD |
| 1 | 1 | C25 | 0.1uF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | STD | STD |
| 1 | 1 | C26 | 22pF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | STD | STD |
| 1 | 1 | D1 | LTST-C190GKT | Diode, LED, Green, 2.1V, 20mA, 6mcd | 0603 | LTST-C190GKT | Lite On |
| 1 | 1 | D2 | B220A-13-F | Diode, Schottky, 2A, 20V | SMA | B220A-13-F | Diodes In |
| 0 | 1 | D3 | BAT54C | Diode, Dual Schottky, 200-mA, 30-V | SOT23 | BAT54C | Vishay-Liteon |
| 1 | 1 | J1 | ED120/2DS | Terminal Block, 2 pin, 15A, 5.1mm | 0.40 x 0.35 inch | ED120/2DS | OST |
| 1 | 1 | J2 | ED120/4DS | Terminal Block, 4 pin, 15A, 5.1mm | 0.80 x 0.35 inch | ED120/4DS | OST |
| 2 | 2 | JP1, JP3 | PEC03SAAN | Header, 3 pin, 100mil spacing | 0.100 inch x 3 | PEC03SAAN | Sullins |
| 2 | 2 | JP2, JP4 | PEC02SAAN | Header, 2 pin, 100mil spacing | 0.100 inch x 2 | PEC02SAAN | Sullins |
| 1 | 1 | L1 | 3.3uH | Inductor, SMT, 5A, 55milliohm | 0.204 x 0.216 inch | IHLP2020CZER3R3M01 | Vishay |
| 1 | 1 | Q1 | BSS138W | MOSFET, Nch, 30V, 0.5A, 700 milliohms | SOT323 | BSS138W-7-F | Vishay |
| 2 | 2 | Q2, Q3 | CSD17313Q2 | Trans, Nch, 30V, 5A, 26milliohm | SON-6 | CSD17313Q2 | TI |
| 1 | 1 | Q4 | CSD25401Q3 | MOSFET, PChan, -20V, 60A, 8.7 mΩ | QFN3.3X3.3mm | CSD25401Q3 | TI |
| 1 | 1 | Q5 | 2N7002DICT | MOSFET, N-ch, 60V, 115mA, 1.2 Ω | SOT23 | 2N7002DICT | Vishay-Liteon |
| 1 | 1 | R1 | 1.00M | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 1 | 0 | R2 | 0.02 Ohm | Resistor, Metal Film, 1/2 watt, 1% | 2010 | WSL2010R0200FEA | Vishay |
| 0 | 1 | | 0.01 Ohm | Resistor, Metal Film, 1/2 watt, 1% | 2010 | WSL2010R0100FEA | Vishay |
| 4 | 4 | R3, R16, R20, R29 | 0 | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 2 | 2 | R4, R5 | 3.9 | Resistor, Chip, 1/4W, 5% | 1206 | STD | STD |
| 1 | 1 | R6 | 402k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 1 | R7 | 499k | Resistor, Chip, 1/8W, 5% | 0603 | STD | STD |
| 1 | 0 | R8 | 100k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 0 | R9 | 100k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 0 | 1 | | 37.4k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 0 | R10 | 10k | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 0 | 1 | | 1M | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 1 | 1 | R11 | 1.00k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 0 | 0 | R12 | Open | | | STD | STD |
| 2 | 2 | R13, R14 | 4.02k | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 1 | 1 | R15 | 0.01 | Resistor, Metal Film, 1/4 watt, 1% | 1206 | WSL1206R0100FEA | Vishay |
| 1 | 1 | R17 | 10 | Resistor, Chip, 1/16W, 5% | 0805 | STD | STD |

**Table 4. Bill of Materials (continued)**

| Count | | | | | | | |
|---|---|---|---|---|---|---|---|
| -001 | -002 | RefDes | Value | Description | Size | Part Number | MFR |
| 1 | 0 | R19 | 10 | Resistor, Chip, 1/16W, 5% | 0805 | STD | STD |
| 1 | 1 | R21 | 5.23k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 0 | 1 | R22 | 499k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 0 | | 0 | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 1 | 1 | R23 | 100 | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 1 | 1 | R24 | 30.1k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 1 | R25 | 3.01M | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 1 | 1 | R26 | 10k | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 1 | 1 | R27 | 4.99k | Resistor, Chip, 1/16W, 5% | 0603 | STD | STD |
| 2 | 2 | R28, R31 | 100k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 1 | R30 | 232k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 2 | 2 | R32, R18 | 32.4k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 1 | R33 | 0 | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 0 | R34 | 100k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | 1 | R35 | 100k | Resistor, Chip, 1/16W, 1% | 0603 | STD | STD |
| 0 | 0 | TP1, TP3 - TP6 | TP-SMALL | Test Point, 0.020 Hole | 0.100 x 0.100 inch | N/A | N/A |
| 1 | 1 | TP2 | 131-5031-00 | Adaptor, 3.5-mm probe clip | 0.200 inch | 131-4244-00 or 131-5031-00 | Tektronix |
| 13 | 13 | TP7 - TP19 | 5002 | Test Point, White, Thru Hole Color Keyed | 0.100 x 0.100 inch | 5002 | Keystone |
| 1 | 1 | TP20 | 5001 | Test Point, Black, Thru Hole Color Keyed | 0.100 x 0.100 inch | 5001 | Keystone |
| 1 | 1 | U1 | BQ24170RHL | IC, Power Path Selector Stand-alone Charger | VQFN | BQ24170RHL | TI |
| 1 | 1 | -- | | PCB, 2.65 In x 3.00 In x 0.062 In | | HPA610A | Any |
| 4 | 4 | | | Bumper foot (install after final wash) | 0.440 x 0.2 | SJ-5303 | 3M |
| 4 | 4 | | | Shunt, 100-mil, Black | 0.100 | 929950-00 | 3M |
| 1 | 1 | -- | | Label (See Note 5) | 1.25 x 0.25 inch | THT-13-457-10 | Brady |

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants.
Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted.
All other components can be substituted with equivalent MFG's components.
5. Install label after final wash. Text shall be 8 pt font. Text shall be per Table 1.

## 4.2 Board Layout

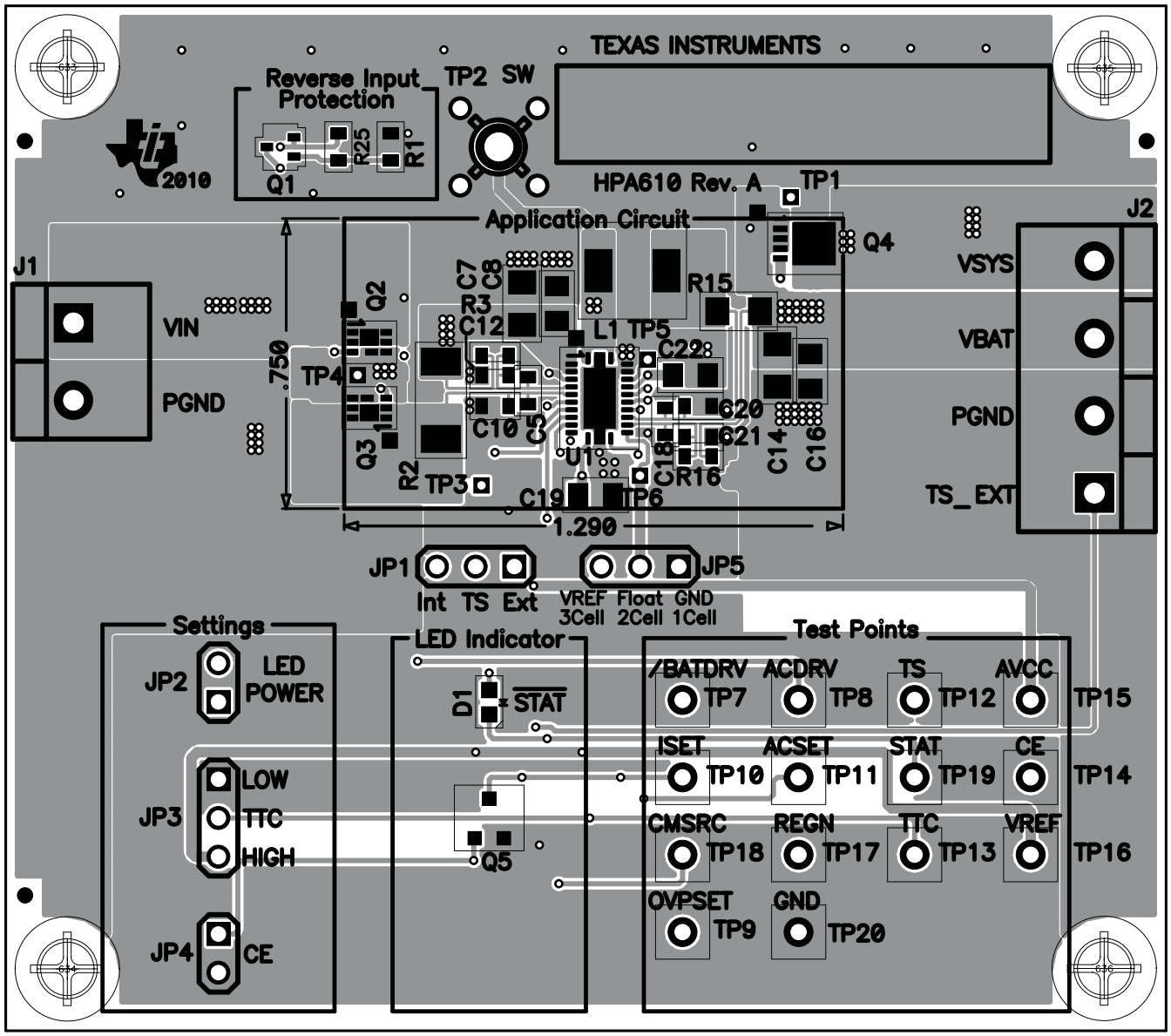


**Figure 2. Top Assembly**

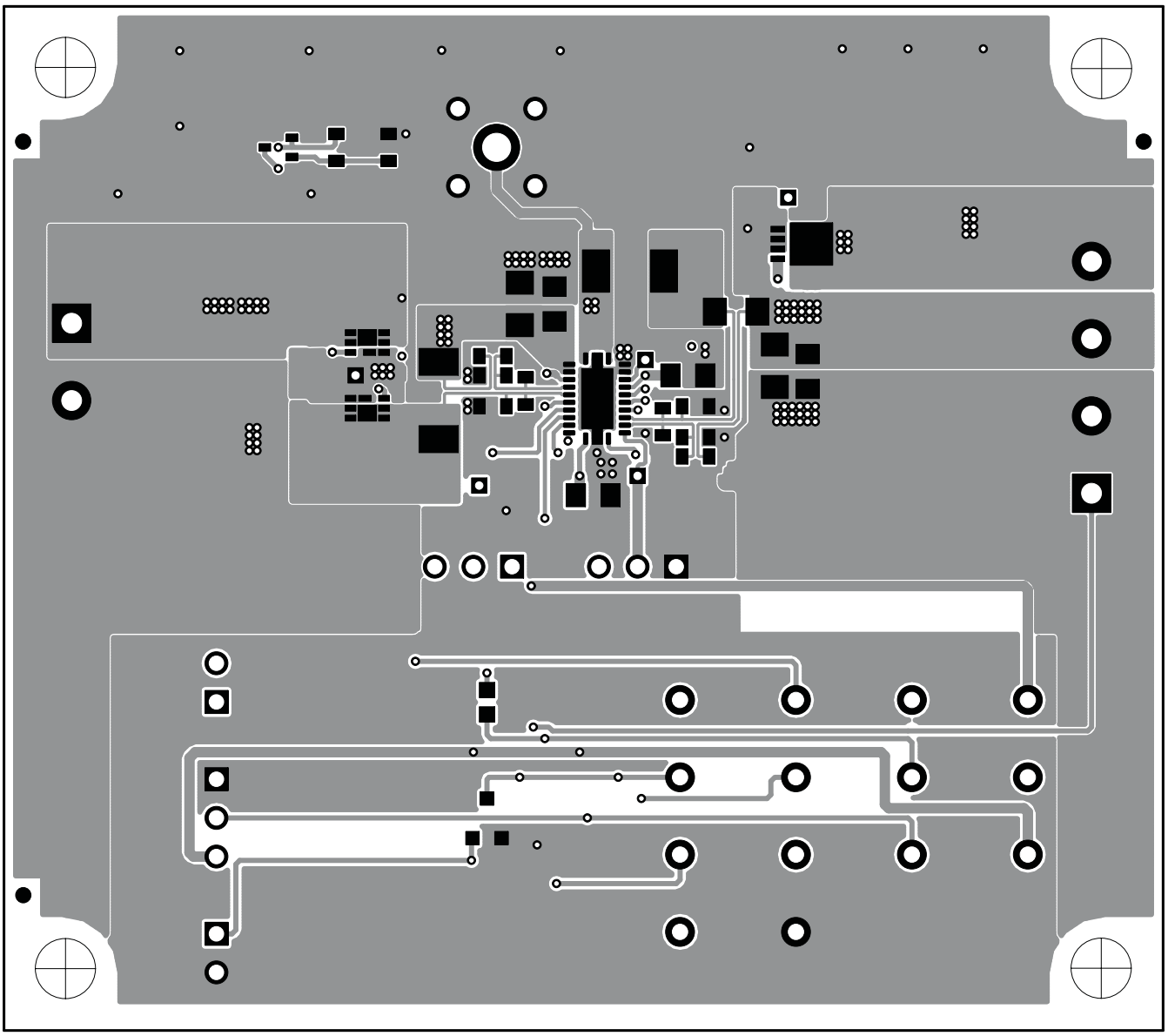

**Figure 3. Top Layer**

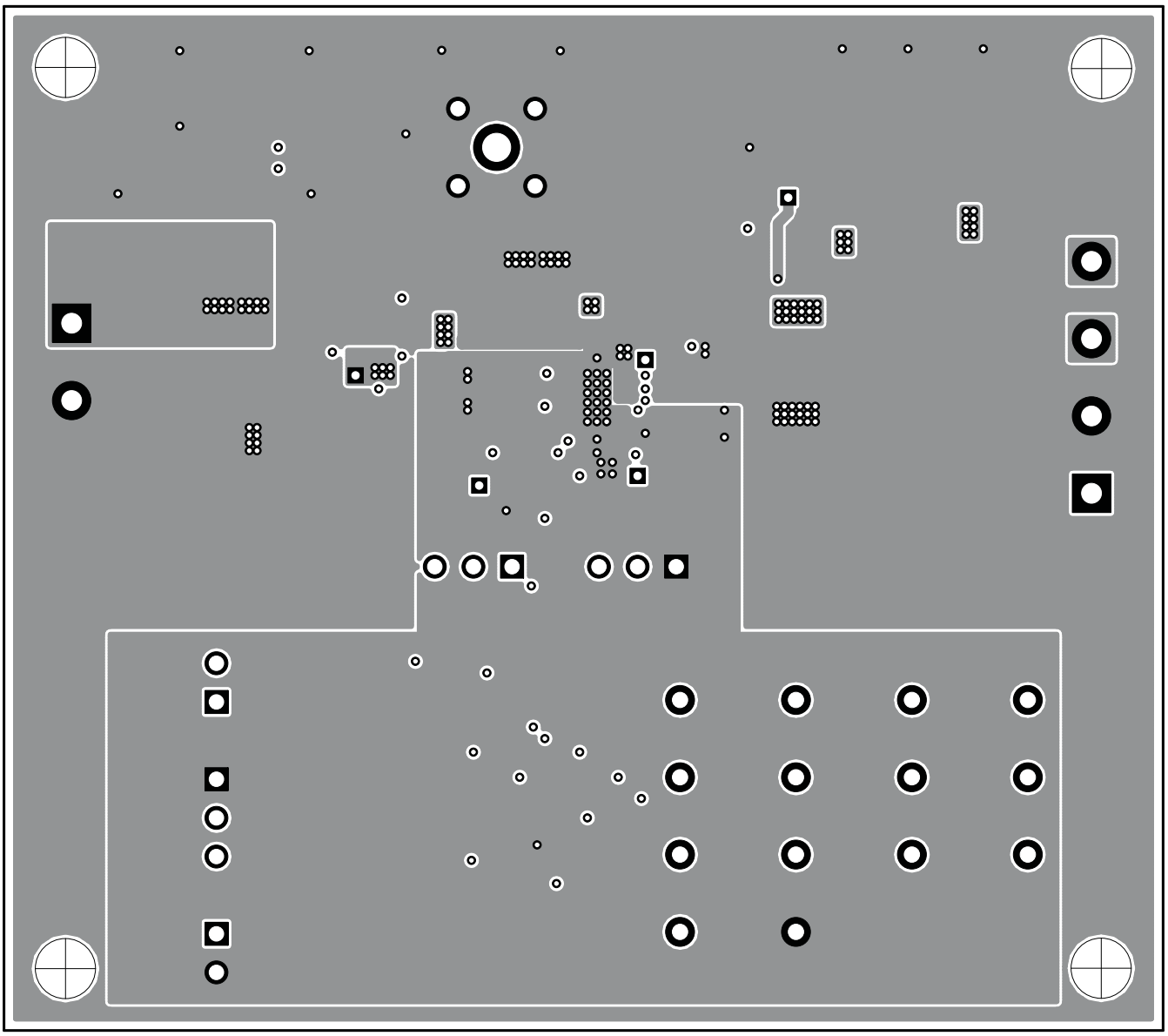

**Figure 4. Second Layer**

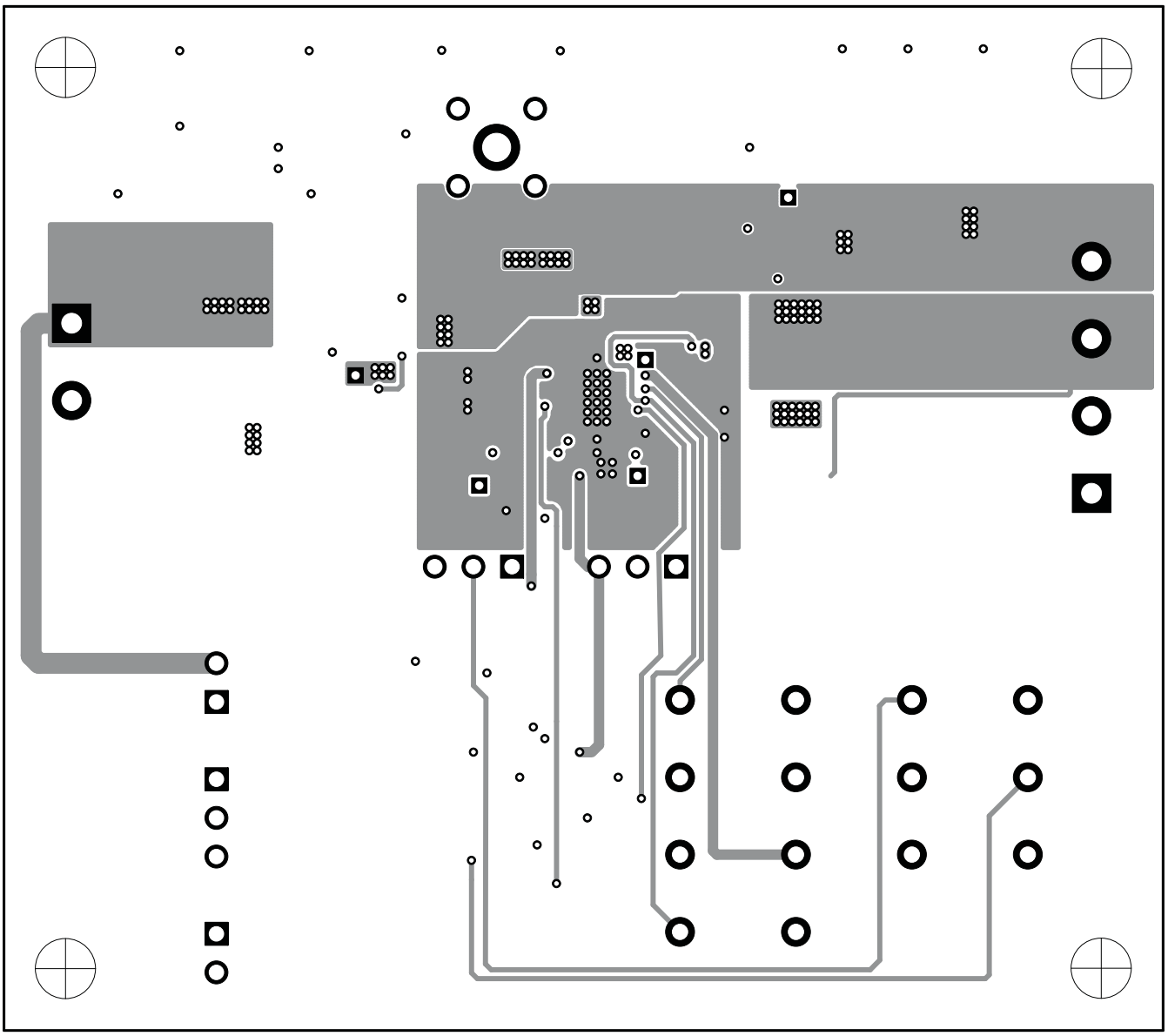

**Figure 5. Third Layer**

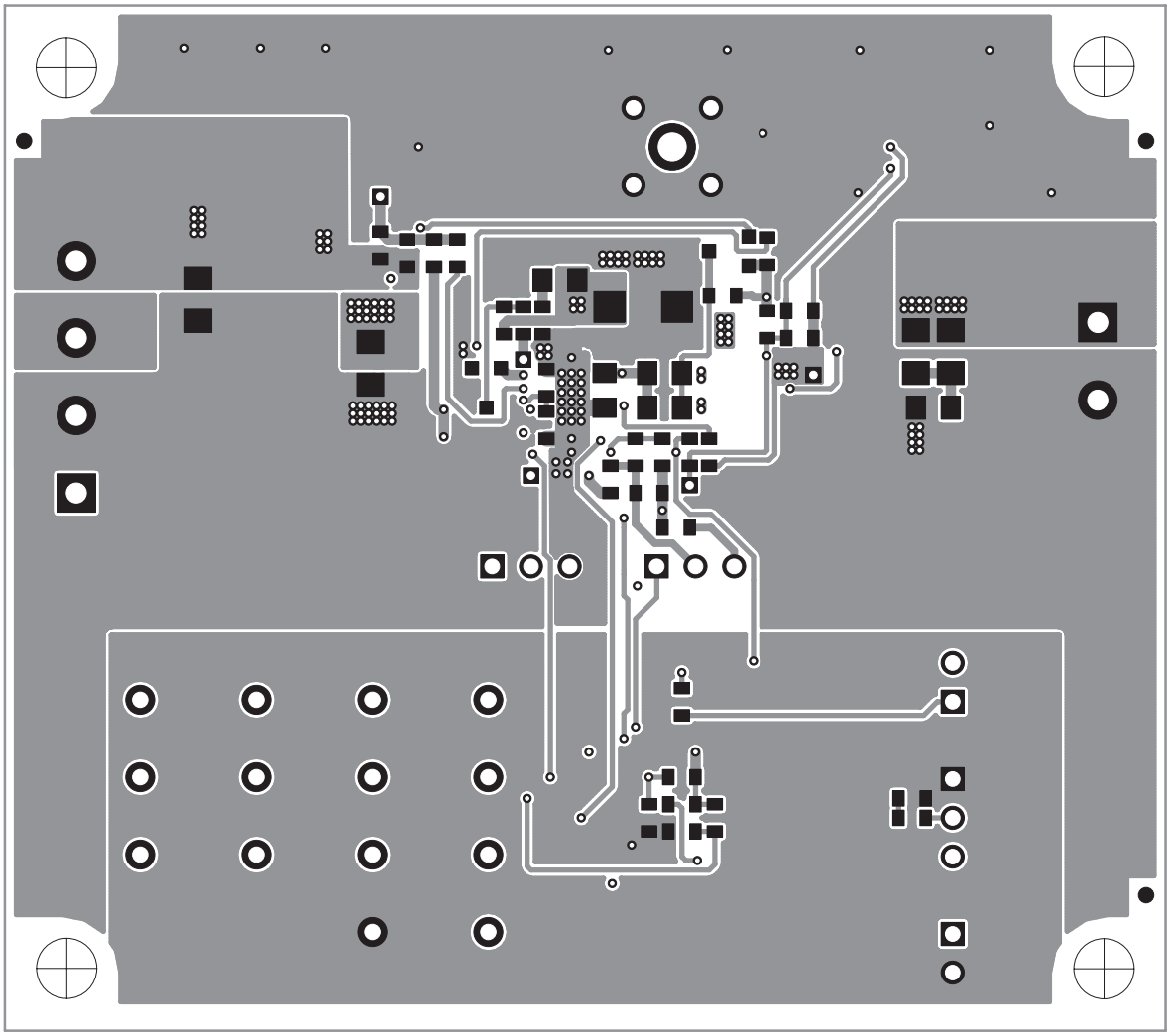

**Figure 6. Bottom Layer**

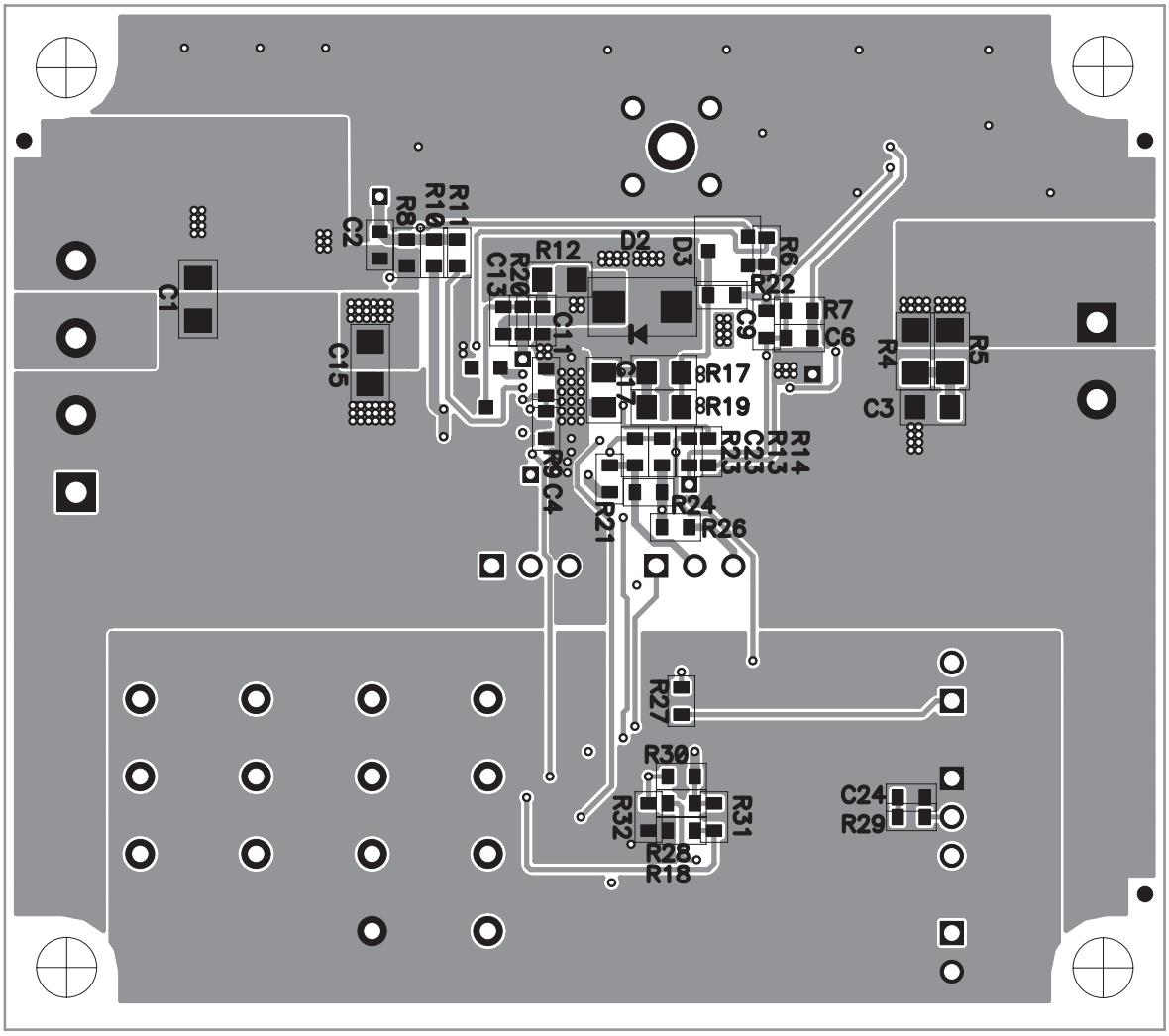


**Figure 7. Bottom Assembly**

## 4.3 Schematic

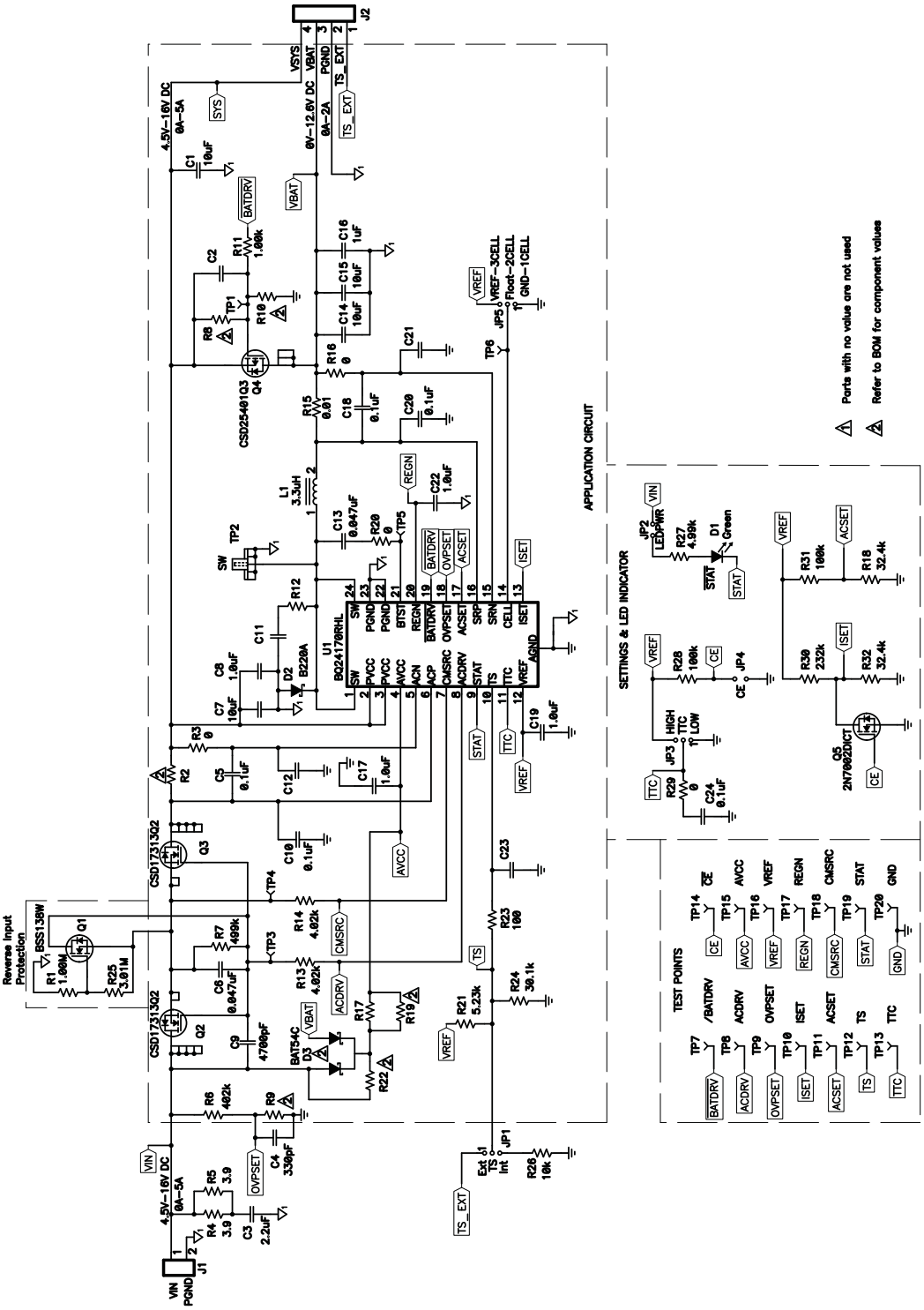


**Figure 8. bq24170EVM Schematic**

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## EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 20 V and the output voltage range of 0 V to 12.6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

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**WARNING**

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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