

500W, 12V Output ZVS Full-Bridge with Current-Doubler Converter Reference Design for 100kRad Applications



Description

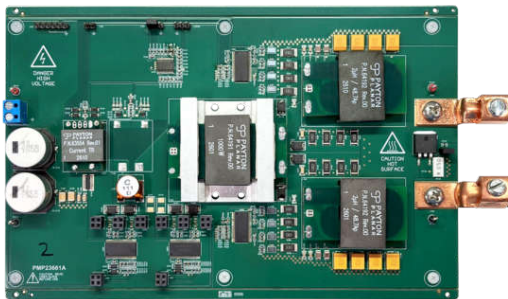
This reference design is a full-bridge topology that is comprised of a TPS7H5005-SEP referenced on secondary ground that controls four TPS7H6005-SEP half-bridge gate drivers. The two drivers referenced to the primary side operate in PWM mode which allows for the design to achieve zero-voltage switching (ZVS) at higher loading conditions. On the secondary side the other driver controls a pair of secondary rectifiers in a current-doubler configuration to further improve the conversion efficiency. In this design the controller, half-bridge drivers and GaN field-effect transistors (FET) are chosen to meet radiation for geostationary orbit (GEO). These components can be swapped out to meet other mission specifications.

Features

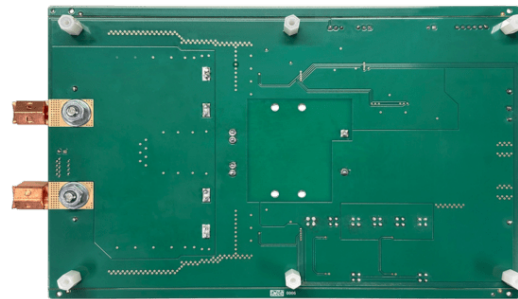
- Current-doubler output configuration
- < 1% voltage ripple on output
- >90% efficiency at full load across input voltage
- Secondary-side controller for faster control loop
- GEO class radiation performance

Applications

- [Satellite electrical power system \(EPS\)](#)
- [Command and data handling \(C and DH\)](#)
- [Radar imaging payload](#)



Top of Board



Bottom of Board

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input voltage	70V to 110V
Output voltage	12V
Maximum output current	42A
Switching frequency	300kHz (primary side)

1.2 Considerations

- Unless noted, all tests were conducted with 42A loading on the output
- Local airflow used, measured 3 m/s airflow average across test board
- External 12V bias applied to primary and secondary sides

1.3 Dimensions

PMP23661A is a four layer, 209 × 127mm PCB. The design size is 160 × 111mm, max component height is 15mm.

1.4 Test Setup

Test setup is shown. Note two fans used to introduce airflow to both primary and secondary side FETs. 12V primary and secondary bias provided on the top left corner of the board.

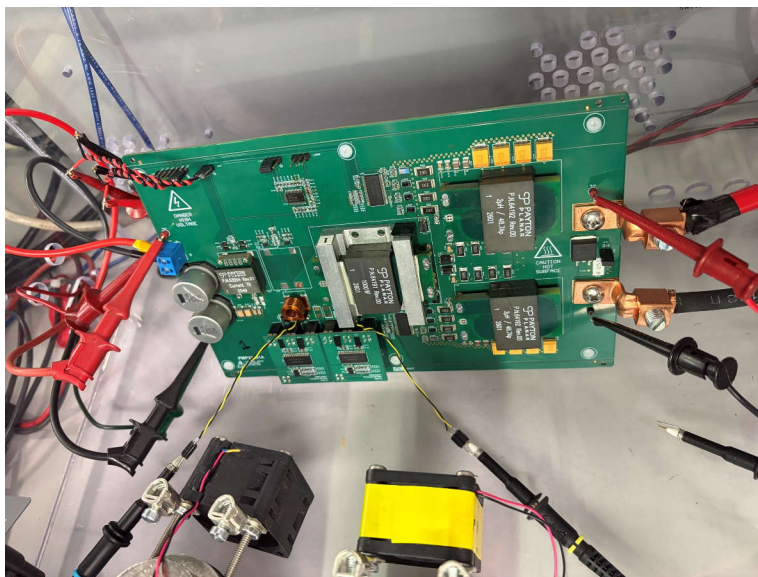


Figure 1-1. Test Setup

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in [Figure 2-1](#) and [Figure 2-2](#).

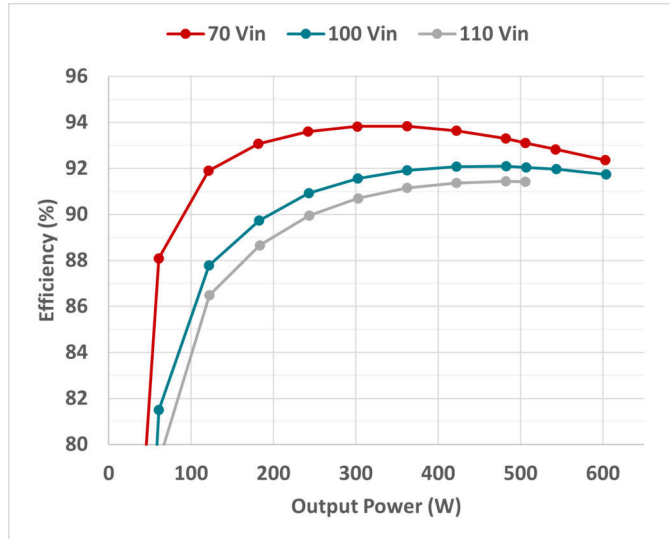


Figure 2-1. Efficiency Across the Input Range

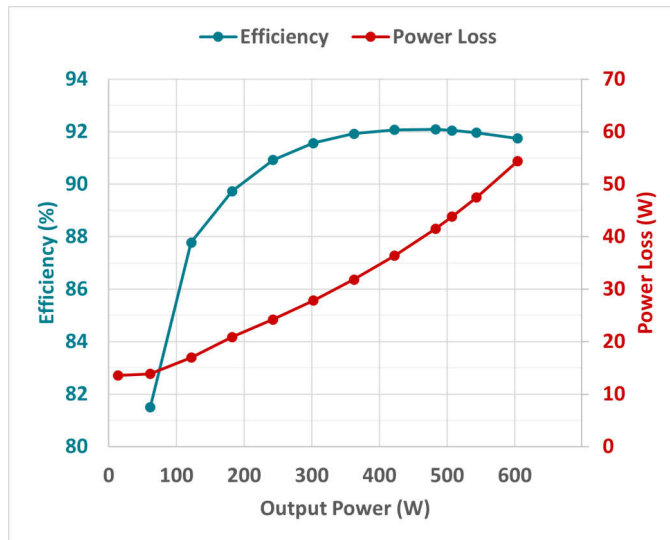


Figure 2-2. Efficiency and Power Loss at Nominal Input Voltage

2.2 Efficiency Data

Efficiency data is shown in [Table 2-1](#) and [Table 2-3](#).

Table 2-1. Efficiency Data at Minimum Input Voltage

Input			Output					Total	
Voltage (V)	Current (A)	Power (W)	Voltage (V)	V, Isense (mV)	Rsense (mOhm)	Current (A)	Power (W)	Loss (W)	Efficiency (%)
69.93	0.3034	21.22	12.024	2.213	1.998746	1.11	13.31	7.90	62.75
69.93	0.9862	68.96	12.023	10.100	1.998746	5.05	60.75	8.21	88.09
69.93	1.8888	132.08	12.022	20.182	1.998746	10.10	121.39	10.69	91.90
69.93	2.7925	195.28	12.021	30.217	1.998746	15.12	181.73	13.55	93.06
69.93	3.6948	258.38	12.020	40.213	1.998746	20.12	241.83	16.55	93.60
69.93	4.6009	321.74	12.019	50.201	1.998746	25.12	301.87	19.87	93.82
69.93	5.5179	385.87	12.018	60.213	1.998746	30.13	362.05	23.82	93.83
69.93	6.4482	450.92	12.017	70.231	1.998746	35.14	422.25	28.67	93.64
69.92	7.3910	516.78	12.016	80.207	1.998746	40.13	482.19	34.59	93.31
69.92	7.7740	543.56	12.016	84.185	1.998746	42.12	506.10	37.46	93.11
69.92	8.3550	584.18	12.016	90.205	1.998746	45.13	542.29	41.89	92.83
69.92	9.3340	652.63	12.015	100.270	1.998746	50.17	602.75	49.88	92.36

Table 2-2. Efficiency Data at Nominal Input Voltage

Input			Output					Total	
Voltage (V)	Current (A)	Power (W)	Voltage (V)	V, Isense (mV)	Rsense (mOhm)	Current (A)	Power (W)	Loss (W)	Efficiency (%)
99.96	0.2739	27.38	12.024	2.292	1.998746	1.15	13.79	13.59	50.37
99.96	0.7488	74.85	12.024	10.141	1.998746	5.07	61.01	13.84	81.50
99.95	1.3890	138.83	12.023	20.259	1.998746	10.14	121.86	16.97	87.78
99.94	2.0367	203.55	12.021	30.371	1.998746	15.20	182.66	20.89	89.74
99.94	2.6717	267.01	12.020	40.372	1.998746	20.20	242.79	24.22	90.93
99.93	3.3061	330.38	12.019	50.308	1.998746	25.17	302.52	27.86	91.57
99.93	3.9444	394.16	12.018	60.260	1.998746	30.15	362.33	31.83	91.92
99.93	4.5905	458.73	12.017	70.253	1.998746	35.15	422.38	36.35	92.08
99.93	5.2465	524.28	12.016	80.310	1.998746	40.18	482.81	41.48	92.09
99.93	5.5119	550.80	12.016	84.335	1.998746	42.19	507.00	43.80	92.05
99.93	5.9124	590.83	12.015	90.388	1.998746	45.22	543.35	47.48	91.96
99.93	6.5890	658.44	12.015	100.491	1.998746	50.28	604.08	54.36	91.74

Table 2-3. Efficiency Data at Maximum Input Voltage

Input			Output					Total	
Voltage (V)	Current (A)	Power (W)	Voltage (V)	V, Isense (mV)	Rsense (mOhm)	Current (A)	Power (W)	Loss (W)	Efficiency (%)
109.96	0.2725	29.96	12.023	2.340	1.998746	1.17	14.08	15.89	46.98
109.95	0.7038	77.38	12.023	10.204	1.998746	5.11	61.38	16.00	79.32
109.94	1.2865	141.44	12.022	20.337	1.998746	10.17	122.32	19.12	86.48
109.93	1.8821	206.90	12.021	30.501	1.998746	15.26	183.44	23.46	88.66
109.92	2.4603	270.44	12.020	40.447	1.998746	20.24	243.24	27.20	89.94
109.92	3.0378	333.91	12.019	50.366	1.998746	25.20	302.86	31.05	90.70
109.92	3.6173	397.61	12.018	60.281	1.998746	30.16	362.46	35.16	91.16
109.92	4.2032	462.02	12.017	70.216	1.998746	35.13	422.16	39.86	91.37
109.92	4.7966	527.24	12.016	80.193	1.998746	40.12	482.10	45.14	91.44
109.92	5.0364	553.60	12.016	84.188	1.998746	42.12	506.12	47.48	91.42

2.3 Thermal Images

The thermal image was captured after operating at full load for 15 minutes with airflow.

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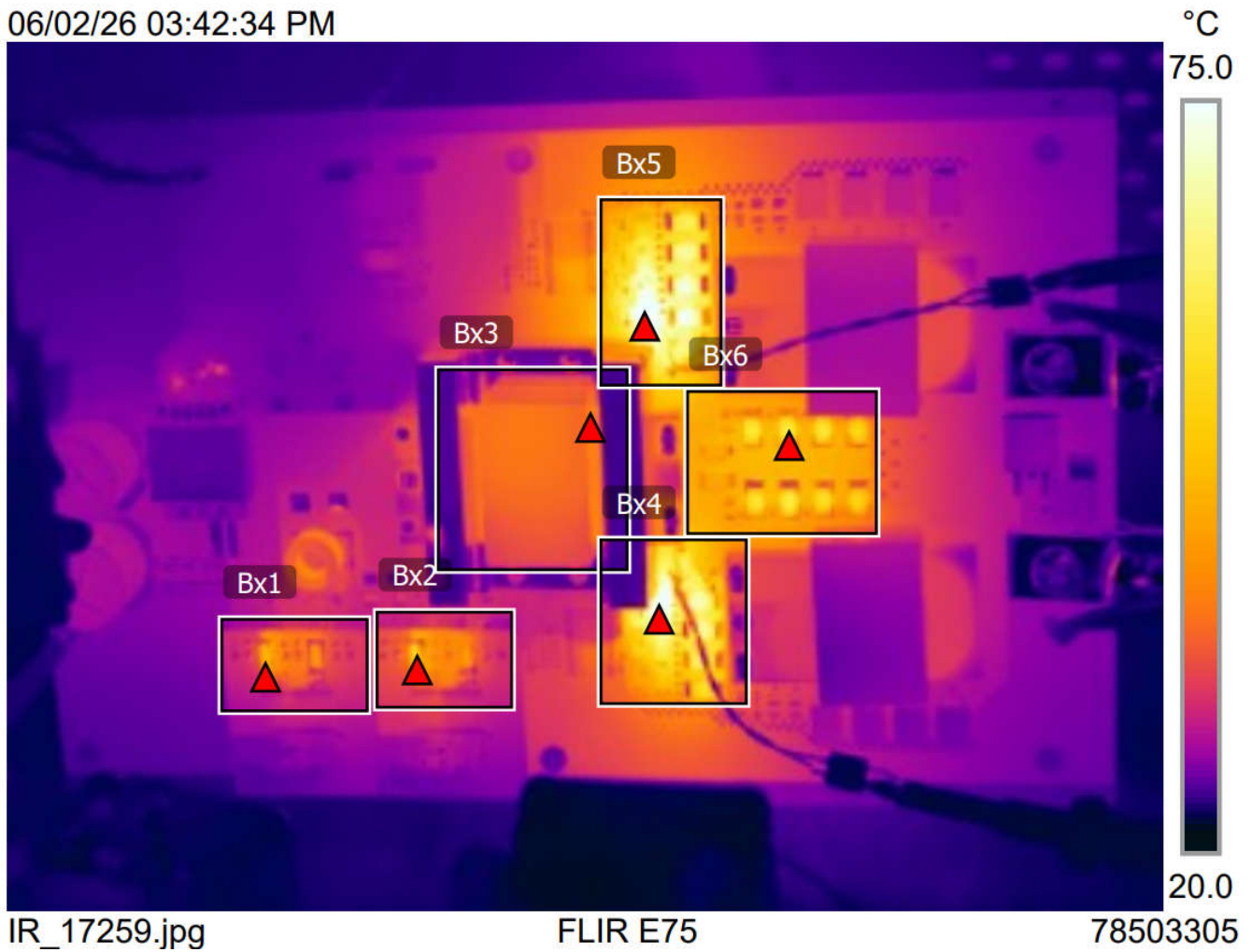


Figure 2-3. Thermal Image

Table 2-4. Temperature by Section

Area	Component	Maximum Temperature (°C)
Bx1	Primary Bridge A	51.7
Bx2	Primary Bridge B	56.2
Bx3	Bridge Transformer	42.6
Bx4	Secondary Rectifier + Snubber A	91.3
Bx5	Secondary Rectifier + Snubber B	93.3
Bx6	Secondary Clamp	63.3

2.4 Bode Plots

The Bode plot is measured at full load with nominal input voltage. Phase margin = 82.1° at 10.1kHz. Gain margin = -21.5dB at 66.1kHz.

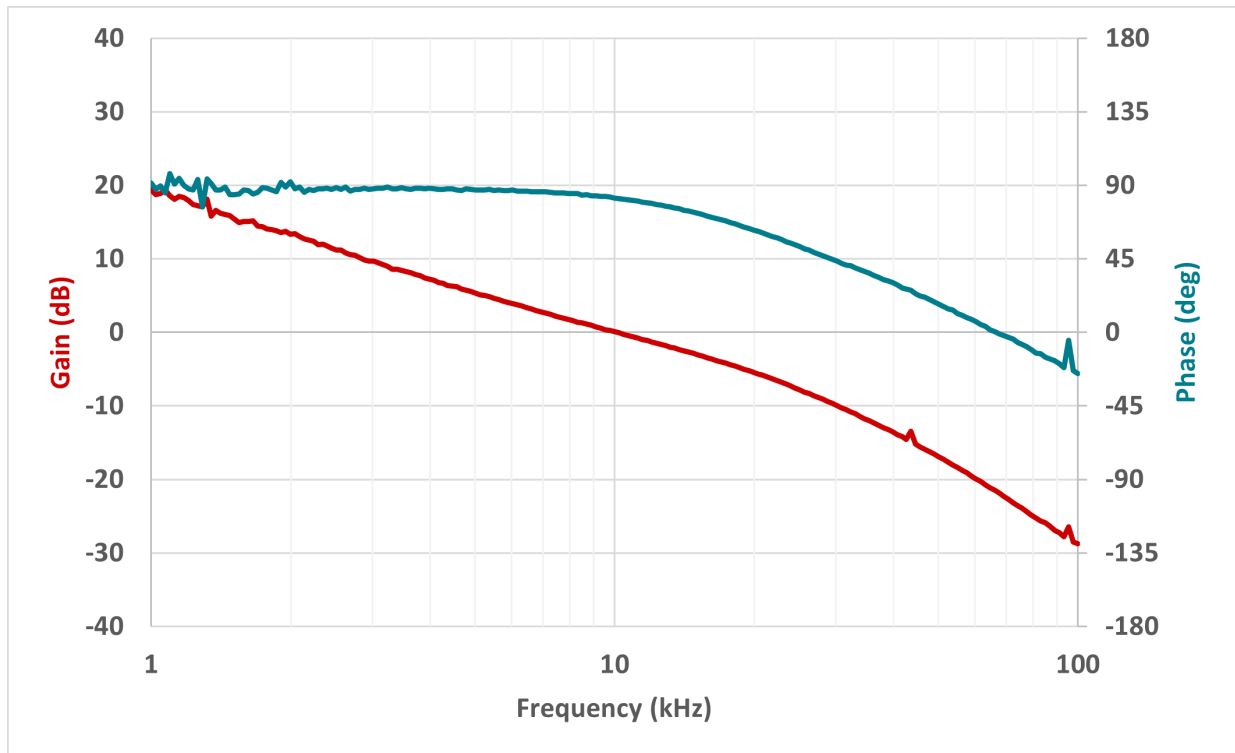


Figure 2-4. Bode Plot

3 Waveforms

3.1 Switching

Switching behavior waveforms are shown in [Figure 3-1](#) and [Figure 3-2](#).

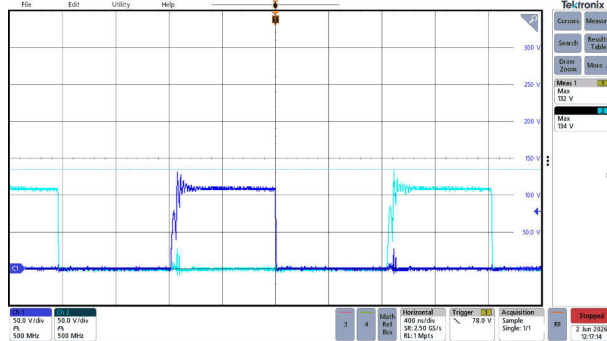


Figure 3-1. Primary Switch Nodes at Maximum Input Voltage

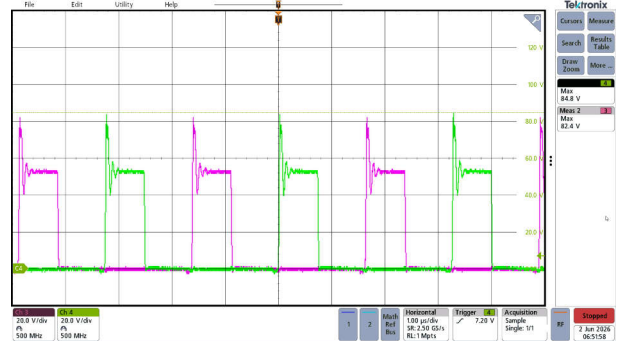


Figure 3-2. Secondary Switch Nodes at Maximum Input Voltage

3.2 Output Voltage Ripple

Output voltage ripple waveforms are shown in [Figure 3-3](#). Measured 0.87% ripple on 12V output.

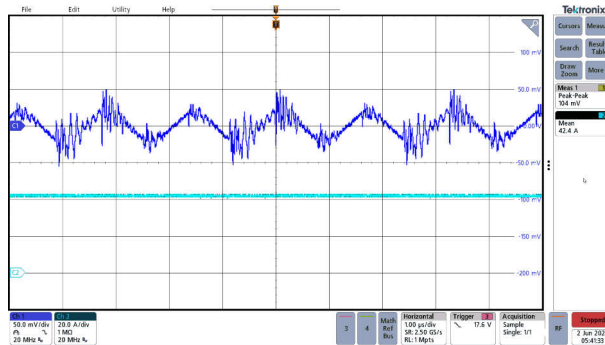


Figure 3-3. Output Voltage Ripple

3.3 Load Transients

Load transient response is shown for a 5A to 42A step. Measured 5% voltage deviation.

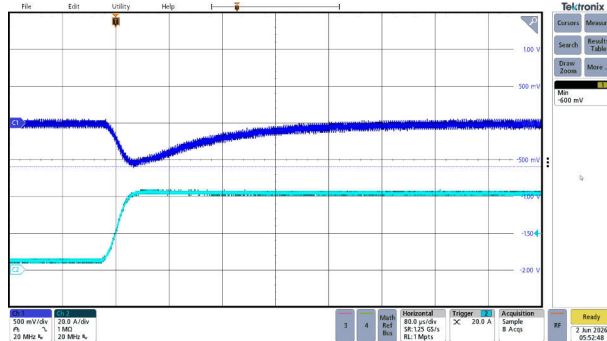


Figure 3-4. Load Step Up

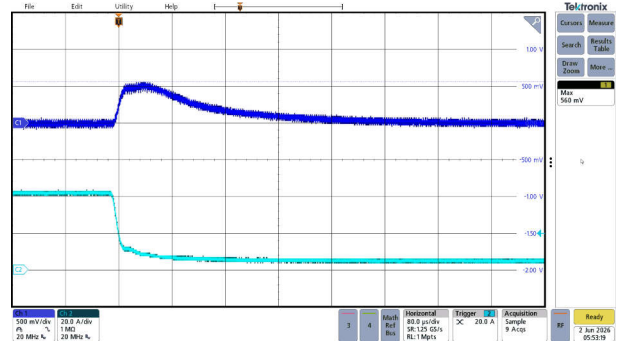


Figure 3-5. Load Step Down

3.4 Start-up Sequence

Start-up behavior is shown in [Figure 3-6](#). This was tested at nominal input voltage, 12V bias present on primary and secondary sides, with no loading on the output. Channel 1 (dark blue) shows the output voltage ramping up. The enable pin of the TPS7H5006-SEP is toggled to initiate the start-up sequence, shown on channel 2 (light blue). Channels 3 and 4 are measuring the maximum voltage stress on the secondary rectifiers.

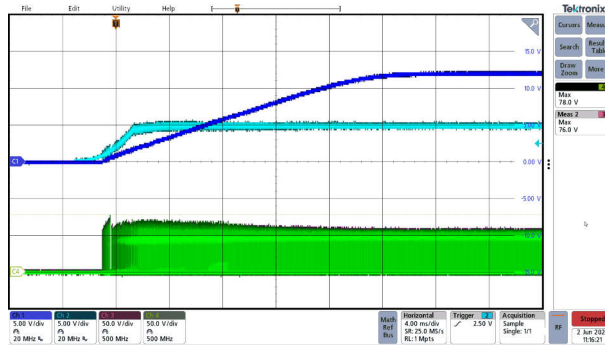


Figure 3-6. Start-Up

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