Design Guide: TIPA-050067

J7200 DRA821 Power-Supply Design Using the TPS6594-Q1

Description

The TPS65941515-Q1 PMIC provides comprehensive power management for the Automotive Jacinto™ 7 DRA821 processor. This single PMIC delivers five BUCKs and four LDOs, supporting functional safety up to ASIL-D level. The system includes discrete components for load switching and LDO functions, enabling multiple power states including Active, Standby, and Retention modes with advanced sequencing capabilities.

Resources

TIPA-050067	Design Folder
TPS65941515-Q1, DRA821	Product Folder
TPS22965-Q1, TPS74501P-Q1	Product Folder
TLV73318P-Q1	Product Folder

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Features

- Comprehensive power resources
- Advanced functional safety
- Multiple power states
- Flexible I/O support
- Comprehensive error monitoring
- Advanced protection features
- Configurable GPIO control
- Dual I2C communication

Applications

- Domain gateway
- ADAS domain controller
- Body control module (BCM)
- Vehicle to everything (V2X)
- Smart telematics gateway

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1 System Description

This design guide describes a power distribution network (PDN), PDN-2A, using a single TPS6594-Q1 PMIC and a few discrete components to power the DRA821 processor and peripherals.

Note

PDN-2A for DRA821 is recommended for designs not requiring board level isolation of the MCU power for an additional lower power mode.

The following topics are described to clarify platform system operation:

1. PDN power resource connections
2. PDN digital control connections
3. Primary and secondary PMIC static NVM contents
4. PMIC sequencing settings to support different PDN power state transitions for an advanced processor system

PMIC and processor datasheets provide recommended operating conditions, electrical characteristics, recommended external components, package details, register maps, and overall component functionality. In the event of any inconsistency between any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

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2 Highlighted Products

2.1 Device Versions

There are different versions of the TPS6594-Q1 device available with unique NVM settings to support different processor solutions. The unique NVM settings for each PMIC device are optimized per PDN design to support different processors, processing loads, SDRAM types, system functional safety levels, and end product features (such as low power modes, processor voltages, and memory subsystems). The NVM settings can be identified by both the TI_NVM_ID and NVM_REV registers.

Table 2-1. TPS6594-Q1 NVM Settings and Orderable Part Number

PDN USE CASE	Orderable Part Number	TI_NVM_ID	TI_NVM_REV
• Up to 5.95 A(1) on the CORE rail • Up to 5.95 A(1) on the CPU rails • Up to 1.7 A(1) on the SDRAM, with support for LPDDR4 • Supports Functional Safety up to ASIL-D level • Supports low power modes including GPIO Retention, and DDR Retention states • Supports I/O level of 3.3 V or 1.8 V • Supports use of SD card	TPS65941515	0x15	0x03

(1) TI recommends having 15% margin between the maximum expected load current and the maximum current allowed per each PMIC output rail.

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3 Processor Connections

This section details how the TPS65941515-Q1 power resources and GPIO signals are connected to the processor and other peripheral components.

3.1 Power Mapping

Figure 3-1 shows the power mapping between the TPS65941515-Q1 PMIC and peripheral regulators to power the processor and associated accessories. In this configuration, the PMIC and additional resources use a 3.3 V input voltage. For Functional Safety applications, there is a protection FET before VCCA that connects to the OVPGDRV pin of the PMIC, allowing voltage monitoring of the input supply to the system.

This PDN uses five discrete power components with four being required and one is optional depending upon end product features. The two TPS22965-Q1 Load Switches connect VCCA_3V3 power rail to supply 3.3 V to processor I/O domains. The third discrete device is a TPS274501-Q1 LDO is used to supply power in low-power retention mode. The fourth discrete device is a TLV73318-Q1 LDO which supplies the LPDDR4 SDRAM component with required 1.8V supply. The last discrete power component is an optional TLV73318-Q1 LDO that can be used if an end product uses a high security processor type and desires the capability to program EFUSE values on-board. If this feature is not desired, then this LDO can be omitted and processor pins terminated per data manual recommendations.

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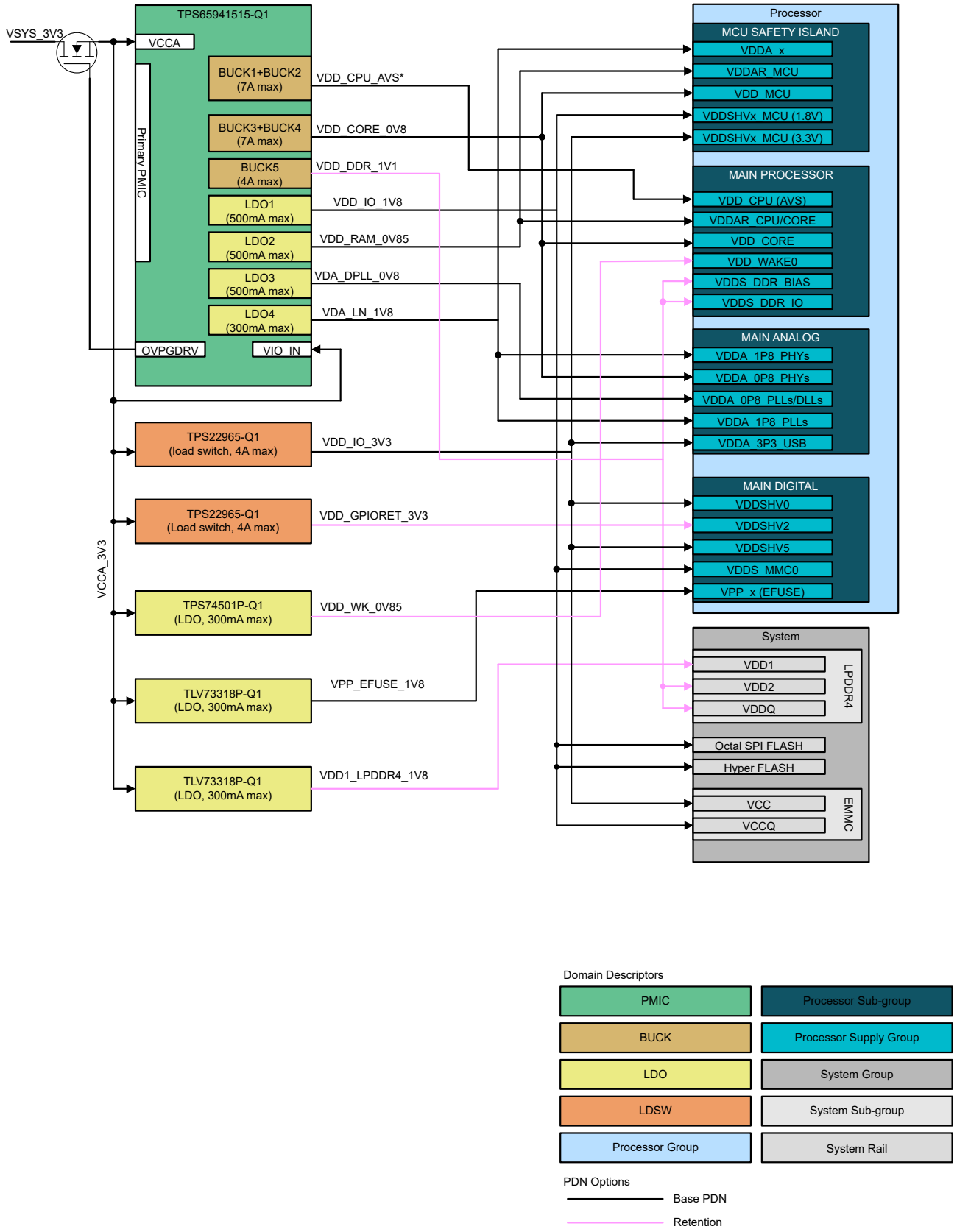

Figure 3-1. Power Connections

- * VDD_CPU_AVS, boot voltage of 0.8 V then software sets device specific AVS

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- ** VPP_EFUSE_1V8, is optional

Table 3-1 identifies which power resources are required to support different system features. In the Active SoC column, there is an additional option for including or excluding the VPP_x(EFUSE) rail.

Table 3-1. PDN Power Mapping and System Features

Power Mapping				System Features(1)				
Device	**Power Resource**	**Power Rails**	**Processor and Memory Domains**	**Active SoC**	**GPIO Retention**	**DDR Retention**	**SD Card**	**USB Interface**
TPS65941515-Q1	BUCK12	VDD_CPU_AVS	VDD_CPU	R				
	BUCK34	VDD_CORE_0V8	VDD_MCU, VDDA_SERDES	R				
	BUCK5	VDD_DDR_1V1	VDDS_DDR	R		R		
			Mem: LPDDR4_VDD2 and VDDQ					
	LDO1	VDD_IO_1V8	VDDS_MMC0, VDDSHVx_MCU(1.8V)	R				
			Mem: VCC					
	LDO2	VDD_RAM_0V85	VDDAR_MCU, VDDAR_CPU/CORE	R				
	LDO3	VDA_DPLL_0V8	VDDA_0P8_PLLs/DLLs	R				
	LDO4	VDA_LN_1V8	VDDA_x(1.8V)	R				
TPS22965-Q1	Load Switch-A	VDD_IO_3V3	VDDSHVx_MCU (3.3 V), VDDSHV0, VDDSHV5	R			R	R
			Mem: EMMC VCC					
TPS22965-Q1	Load Switch-B	VDD_GPIORET_3V3	VDDSHV0-4,VDDSHV6 (3.3 V)	R	R			
TPS74501P-Q1	LDO-A	VDD_WK_0V8	VDDSHV2	R	R			
TLV73318P-Q1	LDO-B	VDD1_LPDDR4_1V8	Mem: LPDDR4_VDD1	R				
TLV73318P-Q1	LDO-C	VPP_EFUSE_1V8	VPP_x(EFUSE)	O				

(1) 'R' is required and 'O' is optional.

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3.2 Control Mapping

Figure 3-2 shows the digital control signal mapping between processor, PMIC, and discrete power devices. Connections from the TPS65941515 PMIC to the processor provide error monitoring, processor reset, processor wake up, and system low-power modes. Specific GPIO pins have been assigned to key signals in order to ensure proper operation during low power modes when only a few GPIO pins remain operational.

The digital connections shown in Figure 3-2 allow system features including GPIO and DDR Retention modes, functional safety up to ASIL-D, and compliant dual voltage SD card operation.

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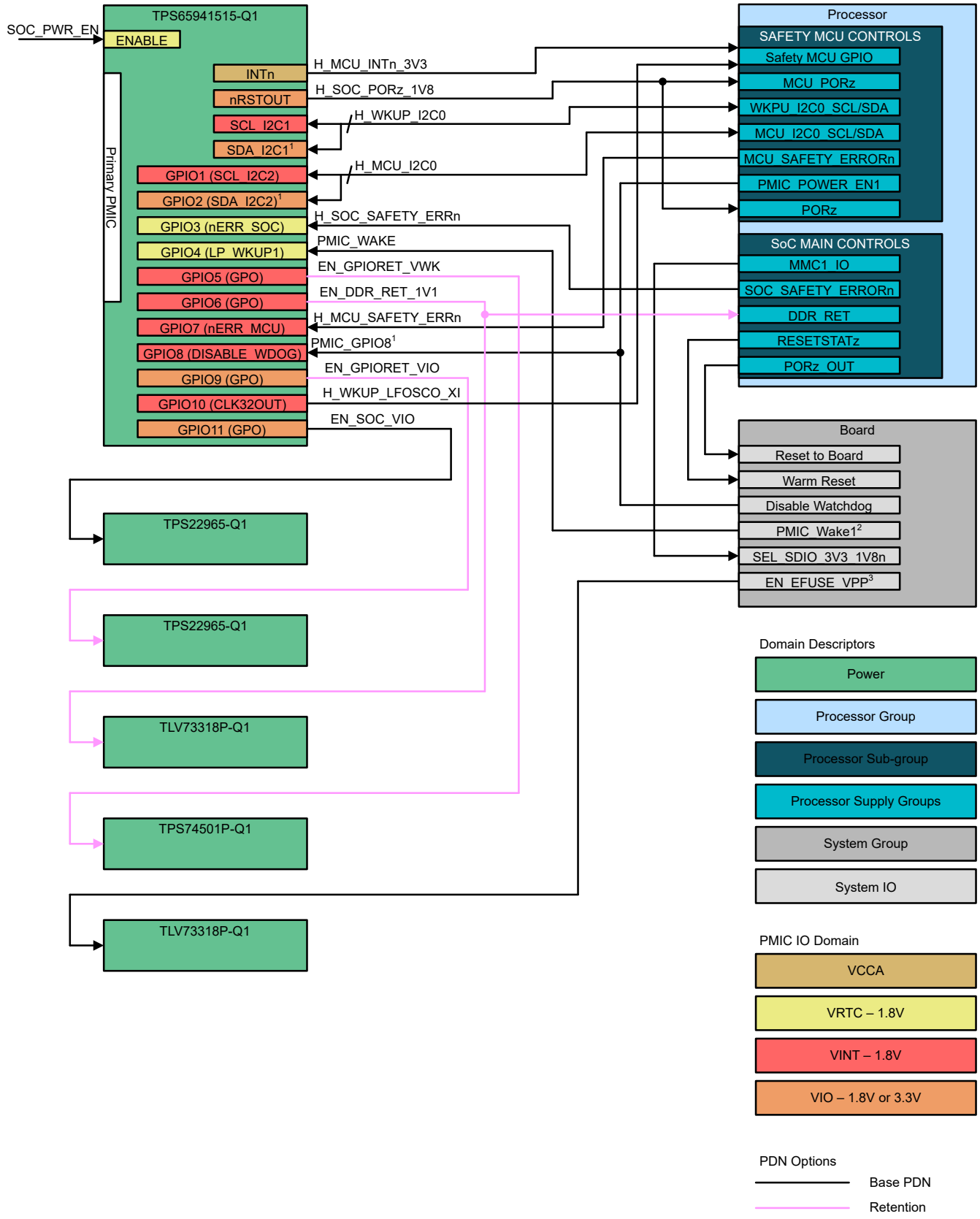

Figure 3-2. TPS65941515-Q1 Digital Connections

1. PMIC IO can have distinct power domains for input and output functionality. The SDA function for I2C1 and I2C2 use the VINT voltage domain as an input and the VIO voltage domain as an output. Please refer to the

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device data sheet for a complete description. The PMIC voltage domains indicated are for the TPS65941515 NVM configuration.
2. PMIC_Wake1 is typically a CAN PHY INH output.
3. The EFUSE LDO is an optional feature and must be enabled by another signal in the system

Note

In addition to the I^2C signals, three additional signals are open-drain outputs and require a pullup to a specific power rail. Please refer to Table 3-2 for a list of the signals and the specific power rail.

Table 3-2. Open-drain signals and Power Rail

PDN Signal	Pullup Power Rail
H_MCU_INTn_3V3	VDD_IO_3V3
H_SOC_PORz_1V8	VDA_LN_1V8
EN_DDR_RET_1V1	VDD_DDR_1V1_REG
H_WKUP_I2C0	VDD_IO_3V3
H_MCU_I2C0_SCL/SDA	VDD_IO_3V3

Please use Table 3-3 as a guide to understand GPIO assignments required for each PDN system feature. If the feature listed is not required, the digital connection can be removed; however, the GPIO pin is still configured per NVM defined default function shown. After the processor has booted up, the processor can reconfigure unused GPIOs to support new functions. Reconfiguring unused GPIOs is possible as long as that function is only needed after boot and default function does not cause any conflicts with normal operations (for example, two outputs driving same net). For details on how functional safety related connections help achieve functional safety system-level goals, see Section 4.

Table 3-3. Digital Connections by System Feature

Device	GPIO Mapping			System Features(1)			
	PMIC Pin	NVM Function	PDN Signals	Active SoC	Functional Safety	DDR Retention	GPIO Retention
TPS659415 15-Q1	nPWRON/ ENABLE	Enable	SOC_PWR_ON	R			
	INT	INT	H_MCU_INTn		R		
	nRSTOUT	nRSTOUT	H_SOC_PORz_1V8	R			
	SCL_I2C1	SCL_I2C1	H_WKUP_I2C0	R			
	SDA_I2C1	SDA_I2C1	H_WKUP_I2C0	R			
	GPIO_1	SCL_I2C2	H_MCU_I2C0_SCL		R		
	GPIO_2	SDA_I2C2	H_MCU_I2C0_SDA		R		
	GPIO_3	nERR_SoC	H_SOC_SAFETY_ERRn		O		
	GPIO_4	LP_WKUP1 (2)	PMIC_WAKE1			R	R
	GPIO_5	GPO	EN_GPIORET_VWK	R			R
	GPIO_6	GPO	EN_DDR_RET_1V1			R	
	GPIO_7	nERR_MCU	H_MCU_SAFETY_ERRn		R		
	GPIO_8	DISABLE_W DOG	PMICA_GPIO8	(3)	(3)		
	GPIO_9	GPO	EN_GPIORET_VIO	R			R
	GPIO_10	CLK32OUT	H_WKUP_LFOSCO_XI	O			
	GPIO_11	GPO	EN_SOC_VIO	R			R

(1) R is Required.
(2) LP_WKUP1 function is masked in the static settings. Instructions for unmasking the function are provided in RETENTION, Entering and Exiting Standby and Entering and Existing LP_STANDBY.

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(3) If it is desired to disable the watchdog through hardware, GPIO_8 is required and must be set high by the time nRSTOUT goes high. After nRSTOUT is high, the watchdog state is latched and the pin can be configured for other functions through software. If GPIO_8 is not set high, then the processor must service the watch dog before the long window expires.

4 Supporting Functional Safety Systems

By using the TPS65941515-Q1 solution to power the DRA821 processor, the system can leverage the following PMIC functional safety features:

- Input Supply Monitoring
- Output Voltage and Current Monitoring
- Question and Answer Watchdog
- Fault Reporting Interrupts
- Enable Drive Pin that provides an independent path to disable system actuators
- Error Pin Monitoring
- Internal Diagnostics including voltage monitoring, temperature monitoring, and Built-In Self-Test

Refer to the Safety Manual of the TPS6594-Q1 device for full descriptions and analysis of the PMIC functional safety features. These functional safety features can assist in achieving up to ASIL-D rating for a system. Additionally, these features help in achieving the functional safety assumptions utilized by the processor to achieve up to ASIL-D rating. See the DRA821 Safety Manual for Jacinto™ 7 Processors for a complete list of functional safety system assumptions.

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4.1 Achieving ASIL-B System Requirements

To achieve a system functional safety level of ASIL-B, the following PDN features are available:

- PMIC over voltage and under voltage monitoring on the power resource voltage outputs
- PMIC over-voltage monitoring and protection on the input to the PMIC (VCCA)
- Watchdog monitoring of safety processor
- MCU error monitoring
- MCU reset
- I^2C communication
- Error indicator for driving external circuitry (optional)

The PDN has an in-line, external power FET, as shown in Figure 3-1, between the input supply and PMICs. The voltage before and after the FET is monitored by the PMIC, and the PMIC controls the FET through the OVPGDRV pin. The FET can quickly isolate the PMIC when an over-voltage event greater than 6 V is detected on the input supply to protect the system from being damaged. Any power connected upstream from the FET is not protected from over voltage events. In Figure 3-1 the load switches that supply power to the MCU and Main I/O domains, the discrete buck supplying the DDR, and the discrete LDO supplying EFUSE are all connected after the FET to extend the over voltage protection to these processor domains and discrete power resources.

The PMIC internal over voltage and under voltage monitoring and their respective monitoring threshold levels are enabled by default and can be updated through I^2C after startup. PMIC power rails connected directly to the processor are monitored by default.

The steps for configuring and starting the watchdog can be found in the TPS6594-Q1 data sheet. Setting the DISABLE_WDOG signal high on GPIO_8 disables the watchdog timer if this feature needs to be suspended during initial development or is not required in the system. An example of re-purposing GPIO_8 is provided in Section 7.4.

GPIO_7 is configured as the MCU error signal monitor, but must be enabled though the ESM_MCU_EN register bit. MCU reset is supported through the connection between the primary PMIC nRSTOUT pin and the MCU_PORz of the processor. Lastly, there are two I^2C ports between the TPS6594-Q1 and the processor. The first is used for all non-watchdog communication, such as voltage level control, and the second allows the watchdog monitoring to be on an independent communication channel.

There is an option to use the EN_DRV pin to indicate an error has been detected and the system is entering SAFE state. This signal can be utilized if the system has external circuitry that needs to be driven by an error event. In this PDN, the EN_DRV is not utilized, but available if needed.

4.2 Achieving up to ASIL-D System Requirements

For ASIL-C or ASIL-D systems, the following features in addition to the ones described in Section 4.1 can be used:

- PMIC current monitoring on all output power rails
- SoC error monitoring
- Residual Voltage Monitoring
- Read-back of Logic Output Pins
  - nINT
  - nRSTOUT
  - EN_DRV (when used)

The current monitoring is enabled by default for all BUCKs and LDOs for the PMIC. Additionally, Figure 3-1 shows that the MCU domain of the processor is powered by different power resources of the PMICs than the main power domain of the processor.

GPIO_3 is configured as the SoC error signal monitor. Similar to the MCU error signal monitor, this feature is enabled through I^2C using the ESM_SOC_EN register bit. For the TPS65941515, an SoC reset is not supported but an interrupt fires and the nINT pin driven low.

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Table 4-1. System Level Safety Features

ASIL-B					ASIL-D	
External SW Wdog	INTn	Safety MCU Processing ESM Safety MCU Reset	Safety Status Signal	System Input Voltage Monitoring	SoC Main Processing ESM	IO Read-Back Feature
Q&A Watchdog and I2C2	nINT Pin	nERR_MCU connected to SOC:MCU_SAFETY_ERRz nRSTOUT connected to MCU_PORz_1V8	ENDRV	VSYS_SENSE -OV with Safety FET OVPGDRV VCCA OV & UV and	nERR_SoC connected to SOC: SOC_SAFETY_ERRz	PMICA: nINT, nRSTOUT, EN_DRV

Table 4-2. Power Monitoring Safety Features

				ASIL-B	ASIL-D Adds	
Device	Power Resource	PDN Power Rail	Safe State Power Group1	Supply Voltage Monitoring	Supply Current Monitoring	Residual Voltage Monitoring
TPS65941515-Q1	BUCK1-2	VDD_CPU_AVS	MCU	OV & UV	YES	YES
	BUCK3-4	VDD_CORE_0V8	MCU	OV & UV	YES	YES
	BUCK5	VDD_DDR_1V1	MCU	OV & UV	YES2	YES
	LDO1	VDD_IO_1V8	MCU	OV & UV	YES	YES
	LDO2	VDD_RAM_0V85	MCU	OV & UV	YES	YES
	LDO3	VDA_DPLL_0v8	MCU	OV & UV	YES	YES
	LDO4	VDA_LN_1V8	MCU	OV & UV	YES	YES
TPS22965W-Q1	Ld Sw A	VDD_IO_3V3	None	NO	NO3	
TPS22965W-Q1	Ld Sw B	VDD_GPIORET_3V3	None	NO	NO4	
TLV73318P-Q1	LDO-A	VDD1_LPDDR4_1V8	None	NO 2	NO2	
TPS74501P-Q1	LDO-B	VDD_WK_0V8	None	NO	NO	
TLV73318P-Q1	LDO-C	VPP_EFUSE_1V8	None	NO5	NO5	

1. Rail Group settings for the TPS65941515-Q1 are found in Table 5-7.
2. Power rails VDD_DDR_1V1 and VDD1_LPDDR4_1V8 are *safety critical* but do not required direct voltage or current monitoring since other means are available (for example, SoC internal *timeout gaskets* and *ECC checkers*) provide diagnostic coverage to detect faults in the DDR voltage.
3. Power rails VDD_IO_1V8/3V3 is typically *not safety critical* since other means are available (for example, *black-channel checkers*) to provide diagnostic coverage to detect faults in SoC signaling interfaces (for example, CAN, UART, and SPI).
4. If an SoC GPIO control signal is used in a *safety critical* interface, then adding voltage and current monitoring to specific VIO power rail may be needed per customer's end product design.
5. Power rail VPP_EFUSE_1V8 is *not safety critical* since Efuse programming does not occur during safety critical processing.

5 Static NVM Settings

The TPS6594-Q1 devices consist of user register space and an NVM. The settings in NVM, which are loaded into the user registers during the transition from INIT to BOOT BIST, are provided in this section. Note: The user registers can be changed during state transitions, such as moving from STANDBY to ACTIVE mode. The user register map is described in the TPS6594-Q1 data sheet.

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5.1 Application-Based Configuration Settings

In the TPS6594-Q1 data sheet, there are seven application-based configurations for each BUCK to operate within. The following list includes the different configurations available:

- 2.2 MHz Single Phase for DDR Termination
- 4.4 MHz VOUT Less than 1.9 V, Multiphase or High COUT Single Phase
- 4.4 MHz VOUT Less than 1.9 V, Low COUT, Single Phase Only
- 4.4 MHz VOUT Greater than 1.7 V, Single Phase Only
- 2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase
- 2.2 MHz Full VOUT Range and VIN Greater than 4.5 V, Single Phase Only
- 2.2 MHz Full VOUT and Full VIN Range, Single Phase Only

The seven configurations also have optimal output inductance values that optimize the performance of each buck under these various conditions. Table 5-1 shows the default configurations for the BUCKs. These settings cannot be changed after device startup.

Table 5-1. Application Use Case Settings

Device	BUCK Rail	Default Application Use Case	Recommended Inductor Value
TPS65941515-Q1	BUCK1	4.4 MHz VOUT Less than 1.9 V Single Phase	220 nH
	BUCK2	4.4 MHz VOUT Less than 1.9 V Single Phase	220 nH
	BUCK3	4.4 MHz VOUT Less than 1.9 V Single Phase	220 nH
	BUCK4	4.4 MHz VOUT Less than 1.9 V Single Phase	220 nH
	BUCK5	4.4 MHz VOUT Less than 1.9 V Single Phase	220 nH

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5.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup.

Table 5-2. Device Identification NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
DEV_REV	DEVICE_ID	0x82	
NVM_CODE_1	TI_NVM_ID	0x15	
NVM_CODE_2	TI_NVM_REV	0x03	
PHASE_CONFIG	MP_CONFIG	0x4	2+2+1

5.3 BUCK Settings

These settings describe the voltages, configurations, and monitoring of the BUCK rails stored in the NVM. All these settings can be changed though I^2C after startup. Some settings, typically the enable bits, are also changed by the PFSM, as described in Section 6.3.

After the Section 6.3.4 sequence has completed, the BUCKx_EN and BUCKx_VMON_EN bits are set for BUCK1, BUCK3, and BUCK5. The BUCKx_RV_SEL bit is cleared for all BUCKs. The other bits remain unchanged, but are still accessible via I^2C.

Table 5-3. BUCK NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
BUCK1_CTRL	BUCK1_EN	0x0	Disabled; BUCK1 regulator
	BUCK1_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK1_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK1_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK1_VSEL	0x0	BUCK1_VOUT_1
	BUCK1_PLDN	0x1	Enabled; Pull-down resistor
	BUCK1_RV_SEL	0x1	Enabled
BUCK1_CONF	BUCK1_SLEW_RATE	0x3	5.0 mV/µs
	BUCK1_ILIM	0x5	5.5 A
BUCK2_CTRL	BUCK2_EN	0x0	Disabled; BUCK2 regulator
	BUCK2_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK2_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK2_VSEL	0x0	BUCK2_VOUT_1
	BUCK2_PLDN	0x1	Enabled; Pull-down resistor
	BUCK2_RV_SEL	0x1	Enabled
BUCK2_CONF	BUCK2_SLEW_RATE	0x3	5.0 mV/µs
	BUCK2_ILIM	0x5	5.5 A
BUCK3_CTRL	BUCK3_EN	0x0	Disabled; BUCK3 regulator
	BUCK3_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK3_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK3_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK3_VSEL	0x0	BUCK3_VOUT_1
	BUCK3_PLDN	0x1	Enabled; Pull-down resistor
	BUCK3_RV_SEL	0x1	Enabled
BUCK3_CONF	BUCK3_SLEW_RATE	0x3	5.0 mV/µs
	BUCK3_ILIM	0x5	5.5 A

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Table 5-3. BUCK NVM Settings (continued)

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
BUCK4_CTRL	BUCK4_EN	0x0	Disabled; BUCK4 regulator
	BUCK4_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK4_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK4_VSEL	0x0	BUCK4_VOUT_1
	BUCK4_PLDN	0x1	Enabled; Pull-down resistor
	BUCK4_RV_SEL	0x1	Enabled
BUCK4_CONF	BUCK4_SLEW_RATE	0x3	5.0 mV/µs
	BUCK4_ILIM	0x5	5.5 A
BUCK5_CTRL	BUCK5_EN	0x0	Disabled; BUCK5 regulator
	BUCK5_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK5_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK5_VSEL	0x0	BUCK5_VOUT_1
	BUCK5_PLDN	0x1	Enable Pull-down resistor
	BUCK5_RV_SEL	0x1	Enabled
BUCK5_CONF	BUCK5_SLEW_RATE	0x3	5.0 mV/µs
	BUCK5_ILIM	0x3	3.5 A
BUCK1_VOUT_1	BUCK1_VSET1	0x37	0.800 V
BUCK1_VOUT_2	BUCK1_VSET2	0x37	0.800 V
BUCK2_VOUT_1	BUCK2_VSET1	0x37	0.800 V
BUCK2_VOUT_2	BUCK2_VSET2	0x37	0.800 V
BUCK3_VOUT_1	BUCK3_VSET1	0x37	0.800 V
BUCK3_VOUT_2	BUCK3_VSET2	0x37	0.800 V
BUCK4_VOUT_1	BUCK4_VSET1	0x37	0.800 V
BUCK4_VOUT_2	BUCK4_VSET2	0x37	0.800 V
BUCK5_VOUT_1	BUCK5_VSET1	0x73	1.10 V
BUCK5_VOUT_2	BUCK5_VSET2	0x73	1.10 V
BUCK1_PG_WINDOW	BUCK1_OV_THR	0x3	+5% / +50 mV
	BUCK1_UV_THR	0x3	-5% / -50 mV
BUCK2_PG_WINDOW	BUCK2_OV_THR	0x3	+5% / +50 mV
	BUCK2_UV_THR	0x3	-5% / -50 mV
BUCK3_PG_WINDOW	BUCK3_OV_THR	0x3	+5% / +50 mV
	BUCK3_UV_THR	0x3	-5% / -50 mV
BUCK4_PG_WINDOW	BUCK4_OV_THR	0x3	+5% / +50 mV
	BUCK4_UV_THR	0x3	-5% / -50 mV
BUCK5_PG_WINDOW	BUCK5_OV_THR	0x3	+5% / +50 mV
	BUCK5_UV_THR	0x3	-5% / -50 mV

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5.4 LDO Settings

These settings detail the voltages, configurations, and monitoring of the LDO rails stored in the NVM. All these settings can be changed though I^2C after startup. Some settings, typically the enable bits, are also changed by the PFSM, as described in Section 6.3.

After the Section 6.3.4 sequence has completed, the LDOx_EN and LDOx_VMON_EN bits are set and the LDOx_RV_SEL bit is cleared for all LDOs. The other bits remain unchanged, but are still accessible via I^2C.

Table 5-4. LDO NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
LDO1_CTRL	LDO1_EN	0x0	Disabled; LDO1 regulator.
	LDO1_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDO1_VSET
	LDO1_PLDN	0x1	125 Ohm
	LDO1_VMON_EN	0x0	Disable OV and UV comparators.
	LDO1_RV_SEL	0x1	Enabled
LDO2_CTRL	LDO2_EN	0x0	Disabled; LDO2 regulator.
	LDO2_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDO2_VSET
	LDO2_PLDN	0x1	125 Ohm
	LDO2_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO2_RV_SEL	0x1	Enabled
LDO3_CTRL	LDO3_EN	0x0	Disabled; LDO3 regulator.
	LDO3_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDO3_VSET
	LDO3_PLDN	0x1	125 Ohm
	LDO3_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO3_RV_SEL	0x1	Enabled
LDO4_CTRL	LDO4_EN	0x0	Disabled; LDO4 regulator.
	LDO4_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDO4_VSET
	LDO4_PLDN	0x1	125 Ohm
	LDO4_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO4_RV_SEL	0x1	Enabled
LDO1_VOUT	LDO1_VSET	0x1c	1.80 V
	LDO1_BYPASS	0x0	Linear regulator mode.
LDO2_VOUT	LDO2_VSET	0x9	0.85 V
	LDO2_BYPASS	0x0	Linear regulator mode.
LDO3_VOUT	LDO3_VSET	0x8	0.80 V
	LDO3_BYPASS	0x0	Linear regulator mode.
LDO4_VOUT	LDO4_VSET	0x38	1.800 V
LDO1_PG_WINDOW	LDO1_OV_THR	0x3	+5% / +50 mV
	LDO1_UV_THR	0x3	-5% / -50 mV
LDO2_PG_WINDOW	LDO2_OV_THR	0x3	+5% / +50 mV
	LDO2_UV_THR	0x3	-5% / -50 mV
LDO3_PG_WINDOW	LDO3_OV_THR	0x3	+5% / +50 mV
	LDO3_UV_THR	0x3	-5% / -50 mV
LDO4_PG_WINDOW	LDO4_OV_THR	0x3	+5% / +50 mV
	LDO4_UV_THR	0x3	-5% / -50 mV

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5.5 VCCA Settings

These settings detail the default monitoring enabled on VCCA. All these settings can be changed though I^2C after startup.

Table 5-5. VCCA NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
VCCA_VMON_CTRL	VMON_DEGLITCH_SEL	0x1	20 us
	VCCA_VMON_EN	0x1	Enabled; OV and UV comparators.
VCCA_PG_WINDOW	VCCA_OV_THR	0x7	+10%
	VCCA_UV_THR	0x7	-10%
	VCCA_PG_SET	0x0	3.3 V

5.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. All these settings can be changed though I^2C after startup. Note that the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the *Digital Signal Descriptions* section in TPS6594-Q1 data sheet.

Table 5-6. GPIO NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
GPIO1_CONF	GPIO1_OD	0x0	Push-pull output
	GPIO1_DIR	0x0	Input
	GPIO1_SEL	0x1	SCL_I2C2/CS_SPI
	GPIO1_PU_SEL	0x0	Pull-down resistor selected
	GPIO1_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO1_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO2_CONF	GPIO2_OD	0x0	Push-pull output
	GPIO2_DIR	0x0	Input
	GPIO2_SEL	0x2	SDA_I2C2/SDO_SPI
	GPIO2_PU_SEL	0x0	Pull-down resistor selected
	GPIO2_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO2_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO3_CONF	GPIO3_OD	0x0	Push-pull output
	GPIO3_DIR	0x0	Input
	GPIO3_SEL	0x2	NERR_SOC
	GPIO3_PU_SEL	0x0	Pull-down resistor selected
	GPIO3_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO3_DEGLITCH_EN	0x1	8 us deglitch time.
GPIO4_CONF	GPIO4_OD	0x0	Push-pull output
	GPIO4_DIR	0x0	Input
	GPIO4_SEL	0x6	LP_WKUP1
	GPIO4_PU_SEL	0x0	Pull-down resistor selected
	GPIO4_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO4_DEGLITCH_EN	0x1	8 us deglitch time.

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Table 5-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
GPIO5_CONF	GPIO5_OD	0x0	Push-pull output
	GPIO5_DIR	0x1	Output
	GPIO5_SEL	0x0	GPIO5
	GPIO5_PU_SEL	0x0	Pull-down resistor selected
	GPIO5_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO5_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO6_CONF	GPIO6_OD	0x1	Open-drain output
	GPIO6_DIR	0x1	Output
	GPIO6_SEL	0x0	GPIO6
	GPIO6_PU_SEL	0x0	Pull-down resistor selected
	GPIO6_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO6_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO7_CONF	GPIO7_OD	0x0	Push-pull output
	GPIO7_DIR	0x0	Input
	GPIO7_SEL	0x1	NERR_MCU
	GPIO7_PU_SEL	0x0	Pull-down resistor selected
	GPIO7_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO7_DEGLITCH_EN	0x1	8 us deglitch time.
GPIO8_CONF	GPIO8_OD	0x0	Push-pull output
	GPIO8_DIR	0x0	Input
	GPIO8_SEL	0x3	DISABLE_WDOG
	GPIO8_PU_SEL	0x0	Pull-down resistor selected
	GPIO8_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO8_DEGLITCH_EN	0x1	8 us deglitch time.
GPIO9_CONF	GPIO9_OD	0x0	Push-pull output
	GPIO9_DIR	0x1	Output
	GPIO9_SEL	0x0	GPIO9
	GPIO9_PU_SEL	0x0	Pull-down resistor selected
	GPIO9_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO9_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO10_CONF	GPIO10_OD	0x0	Push-pull output
	GPIO10_DIR	0x0	Input
	GPIO10_SEL	0x0	GPIO10
	GPIO10_PU_SEL	0x0	Pull-down resistor selected
	GPIO10_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO10_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO11_CONF	GPIO11_OD	0x0	Push-pull output
	GPIO11_DIR	0x1	Output
	GPIO11_SEL	0x0	GPIO11
	GPIO11_PU_SEL	0x0	Pull-down resistor selected
	GPIO11_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO11_DEGLITCH_EN	0x0	No deglitch, only synchronization.

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Table 5-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
NPWRON_CONF	NPWRON_SEL	0x0	ENABLE
	ENABLE_PU_SEL	0x0	Pull-down resistor selected
	ENABLE_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	ENABLE_DEGLITCH_EN	0x1	8 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.
	ENABLE_POL	0x0	Active high
	NRSTOUT_OD	0x0	Push-pull output
GPIO_OUT_1	GPIO1_OUT	0x0	Low
	GPIO2_OUT	0x0	Low
	GPIO3_OUT	0x0	Low
	GPIO4_OUT	0x0	Low
	GPIO5_OUT	0x0	Low
	GPIO6_OUT	0x0	Low
	GPIO7_OUT	0x0	Low
	GPIO8_OUT	0x0	Low
GPIO_OUT_2	GPIO9_OUT	0x0	Low
	GPIO10_OUT	0x0	Low
	GPIO11_OUT	0x0	Low

5.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed though I^2C after startup.

Table 5-7. FSM NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
RAIL_SEL_1	BUCK1_GRP_SEL	0x1	MCU rail group
	BUCK2_GRP_SEL	0x1	MCU rail group
	BUCK3_GRP_SEL	0x1	MCU rail group
	BUCK4_GRP_SEL	0x1	MCU rail group
RAIL_SEL_2	BUCK5_GRP_SEL	0x1	MCU rail group
	LDO1_GRP_SEL	0x1	MCU rail group
	LDO2_GRP_SEL	0x1	MCU rail group
	LDO3_GRP_SEL	0x1	MCU rail group
RAIL_SEL_3	LDO4_GRP_SEL	0x1	MCU rail group
	VCCA_GRP_SEL	0x1	MCU rail group
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	0x2	MCU power error
	SOC_RAIL_TRIG	0x3	SOC power error Not used in this NVM configuration.
	OTHER_RAIL_TRIG	0x3	SOC power error Not used in this NVM configuration.
	SEVERE_ERR_TRIG	0x0	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	0x1	Orderly shutdown

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5.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed though I^2C after startup.

Table 5-8. Interrupt NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	0x1	Masked
	GPIO1_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO2_FSM_MASK	0x1	Masked
	GPIO2_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO3_FSM_MASK	0x1	Masked
	GPIO3_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO4_FSM_MASK	0x1	Masked
	GPIO4_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	0x1	Masked
	GPIO5_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO6_FSM_MASK	0x1	Masked
	GPIO6_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO7_FSM_MASK	0x1	Masked
	GPIO7_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO8_FSM_MASK	0x1	Masked
	GPIO8_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	0x1	Masked
	GPIO9_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO10_FSM_MASK	0x1	Masked
	GPIO10_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO11_FSM_MASK	0x1	Masked
	GPIO11_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
MASK_BUCK1_2	BUCK1_ILIM_MASK	0x0	Interrupt generated
	BUCK1_OV_MASK	0x0	Interrupt generated
	BUCK1_UV_MASK	0x0	Interrupt generated
	BUCK2_ILIM_MASK	0x0	Interrupt generated
	BUCK2_OV_MASK	0x0	Interrupt generated
	BUCK2_UV_MASK	0x0	Interrupt generated
MASK_BUCK3_4	BUCK3_ILIM_MASK	0x0	Interrupt generated
	BUCK3_OV_MASK	0x0	Interrupt generated
	BUCK3_UV_MASK	0x0	Interrupt generated
	BUCK4_OV_MASK	0x0	Interrupt generated
	BUCK4_UV_MASK	0x0	Interrupt generated
	BUCK4_ILIM_MASK	0x0	Interrupt generated
MASK_BUCK5	BUCK5_ILIM_MASK	0x0	Interrupt generated
	BUCK5_OV_MASK	0x0	Interrupt generated
	BUCK5_UV_MASK	0x0	Interrupt generated

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Table 5-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
MASK_LDO1_2	LDO1_OV_MASK	0x0	Interrupt generated
	LDO1_UV_MASK	0x0	Interrupt generated
	LDO2_OV_MASK	0x0	Interrupt generated
	LDO2_UV_MASK	0x0	Interrupt generated
	LDO1_ILIM_MASK	0x0	Interrupt generated
	LDO2_ILIM_MASK	0x0	Interrupt generated
MASK_LDO3_4	LDO3_OV_MASK	0x0	Interrupt generated
	LDO3_UV_MASK	0x0	Interrupt generated
	LDO4_OV_MASK	0x0	Interrupt generated
	LDO4_UV_MASK	0x0	Interrupt generated
	LDO3_ILIM_MASK	0x0	Interrupt generated
	LDO4_ILIM_MASK	0x0	Interrupt generated
MASK_VMON	VCCA_OV_MASK	0x1	Interrupt not generated.
			Set to 0x0 after entering ACTIVE state.
	VCCA_UV_MASK	0x1	Interrupt not generated.
			Set to 0x0 after entering ACTIVE state.
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	0x1	Interrupt not generated.
	GPIO2_FALL_MASK	0x1	Interrupt not generated.
	GPIO3_FALL_MASK	0x1	Interrupt not generated.
	GPIO4_FALL_MASK	0x1	Interrupt not generated.
	GPIO5_FALL_MASK	0x1	Interrupt not generated.
	GPIO6_FALL_MASK	0x1	Interrupt not generated.
	GPIO7_FALL_MASK	0x1	Interrupt not generated.
	GPIO8_FALL_MASK	0x1	Interrupt not generated.
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	0x1	Interrupt not generated.
	GPIO2_RISE_MASK	0x1	Interrupt not generated.
	GPIO3_RISE_MASK	0x1	Interrupt not generated.
	GPIO4_RISE_MASK	0x1	Interrupt not generated.
	GPIO5_RISE_MASK	0x1	Interrupt not generated.
	GPIO6_RISE_MASK	0x1	Interrupt not generated.
	GPIO7_RISE_MASK	0x1	Interrupt not generated.
	GPIO8_RISE_MASK	0x1	Interrupt not generated.
MASK_GPIO9_11 / MASK_GPIO9_10	GPIO9_FALL_MASK	0x1	Interrupt not generated.
	GPIO9_RISE_MASK	0x1	Interrupt not generated.
	GPIO10_FALL_MASK	0x1	Interrupt not generated.
	GPIO11_FALL_MASK	0x1	Interrupt not generated.
	GPIO10_RISE_MASK	0x1	Interrupt not generated.
	GPIO11_RISE_MASK	0x1	Interrupt not generated.
MASK_STARTUP	NPWRON_START_MASK	0x1	Interrupt not generated.
	ENABLE_MASK	0x0	Interrupt generated
	FSD_MASK	0x1	Interrupt not generated.
	SOFT_REBOOT_MASK	0x0	Interrupt generated
MASK_MISC	TWARN_MASK	0x0	Interrupt generated
	BIST_PASS_MASK	0x0	Interrupt generated
	EXT_CLK_MASK	0x1	Interrupt not generated.

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Table 5-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
MASK_MODERATE_ERR	BIST_FAIL_MASK	0x0	Interrupt generated
	REG_CRC_ERR_MASK	0x0	Interrupt generated
	SPMI_ERR_MASK	0x1	Interrupt not generated.
	NINT_READBACK_MASK	0x0	Interrupt generated
	NRSTOUT_READBACK_MASK	0x0	Interrupt generated
	NPWRON_LONG_MASK	0x1	Interrupt not generated.
MASK_FSM_ERR	IMM_SHUTDOWN_MASK	0x0	Interrupt generated
	MCU_PWR_ERR_MASK	0x0	Interrupt generated
	SOC_PWR_ERR_MASK	0x0	Interrupt generated
	ORD_SHUTDOWN_MASK	0x0	Interrupt generated
MASK_COMM_ERR	COMM_FRM_ERR_MASK	0x0	Interrupt generated
	COMM_CRC_ERR_MASK	0x0	Interrupt generated
	COMM_ADR_ERR_MASK	0x0	Interrupt generated
	I2C2_CRC_ERR_MASK	0x0	Interrupt generated
	I2C2_ADR_ERR_MASK	0x0	Interrupt generated
MASK_READBACK_ERR	EN_DRV_READBACK_ MASK	0x0	Interrupt generated
	NRSTOUT_SOC_ READBACK_MASK	0x0	Interrupt generated
MASK_ESM	ESM_SOC_PIN_MASK	0x1	Interrupt not generated.
	ESM_SOC_RST_MASK	0x1	Interrupt not generated.
	ESM_SOC_FAIL_MASK	0x1	Interrupt not generated.
	ESM_MCU_PIN_MASK	0x1	Interrupt not generated.
	ESM_MCU_RST_MASK	0x1	Interrupt not generated.
	ESM_MCU_FAIL_MASK	0x1	Interrupt not generated.
GENERAL_REG_1	PFSM_ERR_MASK	0x0	Interrupt generated

5.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though I^2C after startup.

Table 5-9. POWERGOOD NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
PGOOD_SEL_1	PGOOD_SEL_BUCK1	0x0	Masked
	PGOOD_SEL_BUCK2	0x0	Masked
	PGOOD_SEL_BUCK3	0x0	Masked
	PGOOD_SEL_BUCK4	0x0	Masked
PGOOD_SEL_2	PGOOD_SEL_BUCK5	0x0	Masked
PGOOD_SEL_3	PGOOD_SEL_LDO1	0x0	Masked
	PGOOD_SEL_LDO2	0x0	Masked
	PGOOD_SEL_LDO3	0x0	Masked
	PGOOD_SEL_LDO4	0x0	Masked

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Table 5-9. POWERGOOD NVM Settings (continued)

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
PGOOD_SEL_4	PGOOD_SEL_VCCA	0x0	Masked
	PGOOD_SEL_TDIE_WARN	0x0	Masked
	PGOOD_SEL_NRSTOUT	0x0	Masked
	PGOOD_SEL_NRSTOUT_ SOC	0x0	Masked
	PGOOD_POL	0x0	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	0x1	Both undervoltage and overvoltage are monitored

5.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, PFSM delays, and LDO timeout. All these settings can be changed though I^2C after startup.

Table 5-10. Miscellaneous NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
PLL_CTRL	EXT_CLK_FREQ	0x0	1.1 MHz
CONFIG_1	TWARN_LEVEL	0x0	130C
	I2C1_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.
	I2C2_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.
	EN_ILIM_FSM_CTRL	0x0	Buck/LDO regulator ILIM interrupts do not affect FSM triggers.
	NSLEEP1_MASK	0x0	NSLEEP1(B) affects FSM state transitions.
	NSLEEP2_MASK	0x0	NSLEEP2(B) affects FSM state transitions.
CONFIG_2	BB_CHARGER_EN	0x0	Disabled
	BB_VEOC	0x0	2.5V
	BB_ICHR	0x0	100uA
RECOV_CNT_REG_2	RECOV_CNT_THR	0xf	0xf
BUCK_RESET_REG	BUCK1_RESET	0x0	0x0
	BUCK2_RESET	0x0	0x0
	BUCK3_RESET	0x0	0x0
	BUCK4_RESET	0x0	0x0
	BUCK5_RESET	0x0	0x0
SPREAD_SPECTRUM_1	SS_EN	0x0	Spread spectrum disabled
	SS_DEPTH	0x0	No modulation
FSM_STEP_SIZE	PFSM_DELAY_STEP	0xb	0xb
LDO_RV_TIMEOUT_ REG_1	LDO1_RV_TIMEOUT	0xf	16ms
	LDO2_RV_TIMEOUT	0xf	16ms
LDO_RV_TIMEOUT_ REG_2	LDO3_RV_TIMEOUT	0xf	16ms
	LDO4_RV_TIMEOUT	0xf	16ms
USER_SPARE_REGS	USER_SPARE_1	0x0	0x0
	USER_SPARE_2	0x0	0x0
	USER_SPARE_3	0x0	0x0
	USER_SPARE_4	0x0	0x0

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Table 5-10. Miscellaneous NVM Settings (continued)

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
ESM_MCU_MODE_ CFG	ESM_MCU_EN	0x0	ESM_MCU disabled.
ESM_SOC_MODE_ CFG	ESM_SOC_EN	0x0	ESM_SoC disabled.
RTC_CTRL_2	XTAL_EN	0x1	Crystal oscillator is enabled
	LP_STANDBY_SEL	0x1	Low Power Standby state is used as STANDBY state (LDOINT is disabled)
	FAST_BIST	0x0	Logic and analog BIST is run at BOOT BIST
	STARTUP_DEST	0x3	ACTIVE
	XTAL_SEL	0x1	9 pF
PFSM_DELAY_REG_1	PFSM_DELAY1	0x58	0x58
PFSM_DELAY_REG_2	PFSM_DELAY2	0x9d	0x9d
PFSM_DELAY_REG_3	PFSM_DELAY3	0x0	0x0
PFSM_DELAY_REG_4	PFSM_DELAY4	0x0	0x0
GENERAL_REG_0	EN_OVP	0x1	OVP Enabled
	VSYS_DEAD_LOCK_EN	0x1	Turn off VCCA with external FET in case of VCCA OVP
	PFSM_ERR_RESET_DIS	0x0	PFSM_ERR causes reset to logic
	DIS_UVLO_OVP_RESET	0x0	UVLO/OVP cause reset to logic
	FAST_BOOT_BIST	0x0	LBIST is run during boot BIST
	VMON_ABIST_EN	0x1	VMON ABIST enabled
	ABIST_ERROR_MASK	0x0	ABIST errors not masked
GENERAL_REG_1	REG_CRC_EN	0x1	Register CRC enabled
	FAST_VCCA_OVP	0x0	Slow; 4us deglitch filter enabled

5.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings **cannot** be changed after device startup.

Table 5-11. Interface NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
SERIAL_IF_CONFIG	I2C_SPI_SEL	0x0	I2C
	I2C1_SPI_CRC_EN	0x0	CRC disabled
	I2C2_CRC_EN	0x0	CRC disabled
I2C1_ID_REG	I2C1_ID	0x48	0x48
I2C2_ID_REG	I2C2_ID	0x12	0x12

5.12 Watchdog Settings

These settings detail the default watchdog addresses. These settings can be changed though I^2C after startup.

Table 5-12. Watchdog NVM Settings

Register Name	Field Name	TPS65941515-Q1	
		Value	Description
WD_LONGWIN_CFG	WD_LONGWIN	0xff	0xff
WD_THR_CFG	WD_EN	0x1	Watchdog enabled.

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6 Pre-Configurable Finite State Machine (PFSM) Settings

This section describes the default PFSM settings of the TPS6594-Q1 devices. These settings cannot be changed after device startup.

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6.1 Configured States

In this PDN, the PMIC has the following configured power states:

- Standby
- Active
- Retention (both DDR and GPIO retention modes)

In Figure 6-1, the configured PDN power states are shown, along with the transition conditions to move between the states. Additionally, the transitions to hardware states, such as SAFE RECOVERY and LP_STANDBY are shown. The hardware states are part of the fixed device power Finite State Machine (FSM) and described in the TPS6594-Q1 data sheet, see Section 8.

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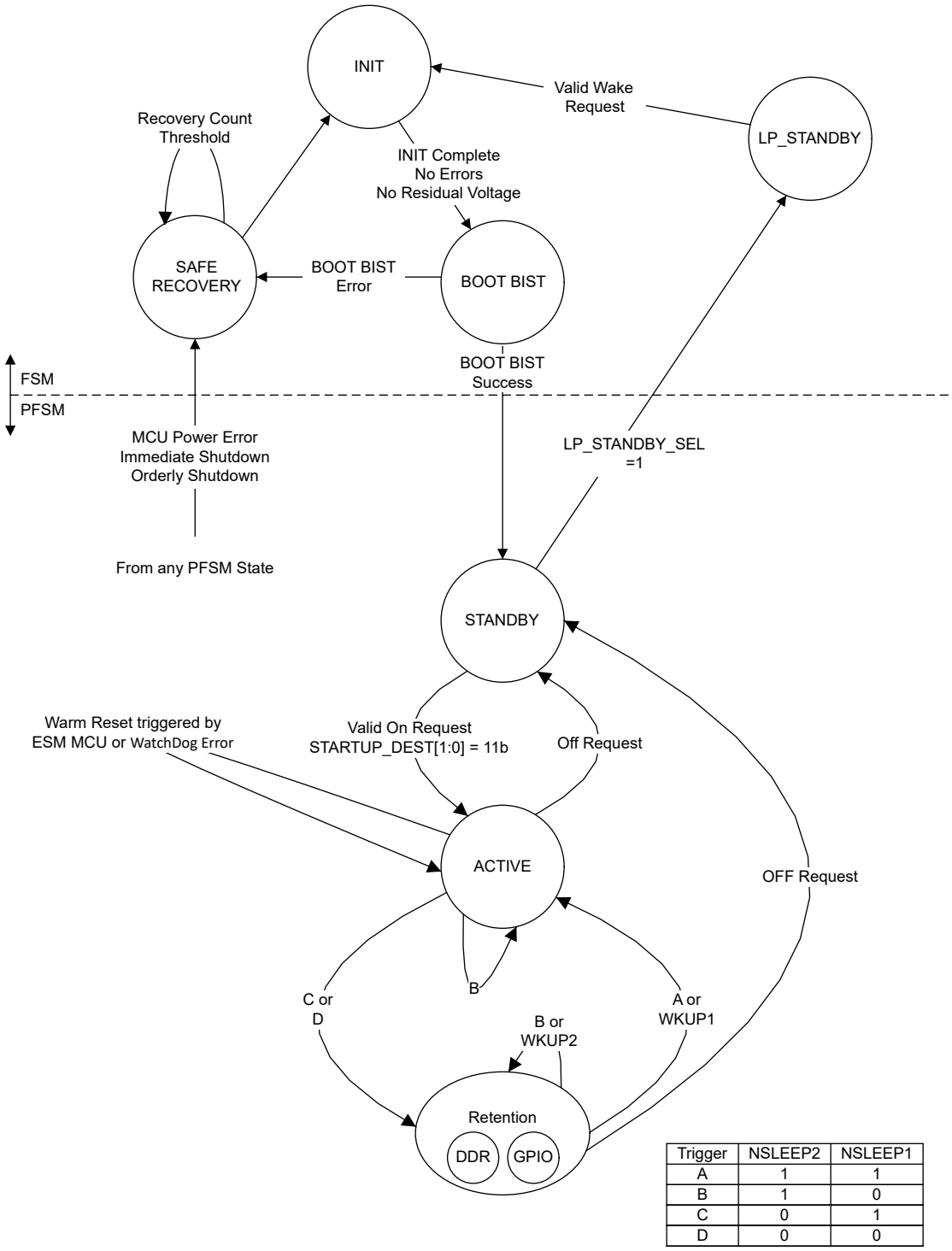

Trigger	NSLEEP2	NSLEEP1
A	1	1
B	1	0
C	0	1
D	0	0

Figure 6-1. Pre-Configurable Finite State Machine (PFSM) Mission States and Transitions

When the PMIC transitions from the FSM to the PFSM, several initialization instructions are performed to disable the residual voltage checks on both the BUCK and LDO regulators and set the FIRST_STARTUP_DONE bit. After these instructions are executed the PMIC waits for a valid ON Request before entering the ACTIVE state. The definition for each power state is described below:

STANDBY The PMICs are powered by a valid supply on the system power rail (VCCA > VCCA_UV). All device resources are powered down in the STANDBY state. EN_DRV is forced low in this state. The

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processor is in the Off state, no voltage domains are energized. Refer to the Section 6.3.2 sequence description.

The STANDBY state is also entered when an error occurs and the PMIC transitions out of the PFSM mission states and into the FSM states. When the device returns from the FSM state the to PFSM the first state is represented by STANDBY with all of the resources powered down and EN_DRV forced low. The sequence Section 6.3.1 is performed before the PMIC leaves the PFSM and enters the FSM state SAFE_RECOVERY.

ACTIVE The PMICs are powered by a valid supply. The PMICs are fully functional and supply power to all PDN loads. The processor has completed a recommended power up sequence with all voltage domains energized in both MCU and Main processor sections. The MCU can now set the ENABLE_DRV bit high. Refer to the Section 6.3.4 sequence description.

Retention The PMIC is powered by a valid supply. Only the power resources assigned to the retention rails are on or in LPM depending on the specific resource setting. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit is cleared by the device in this state. If the I2C_6 bit is set high, the PMIC enters GPIO retention state. If the I2C_7 bit is set high, the PMICs enters DDR retention state. These bits need to be set before a trigger for the retention state occurs. Refer to the Section 6.3.5 sequence description.

6.2 PFSM Triggers

As shown in Figure 6-1, there are various triggers that can enable a state transition between configured states. Table 6-1 describes each trigger and its associated state transition from highest priority (Immediate Shutdown) to lowest priority (I2C_3). Active triggers of higher priority block triggers of lower priority and the associated sequence.

Table 6-1. State Transition Triggers

Trigger	Priority (ID)	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
Immediate Shutdown	1	True	False	STANDBY, ACTIVE, Suspend-to-RAM	SAFE(1)	TO_SAFE_SEVERE
MCU Power Error	2	True	False	STANDBY, ACTIVE, Suspend-to-RAM	SAFE(1)	TO_SAFE
Orderly Shutdown	4	True	False	STANDBY, ACTIVE, Suspend-to-RAM	SAFE(1)	TO_SAFE_ORDERLY
OFF Request	5	False	False	STANDBY, ACTIVE, Suspend-to-RAM	STANDBY(2)	TO_STANDBY
WDOG Error	6	False	True	ACTIVE	ACTIVE	ACTIVE_TO_WARM
ESM MCU Error	7	False	True	ACTIVE	ACTIVE	
I2C_1 bit is high(3)	8	False	True	ACTIVE	No State Change	Execute RUNTIME BIST
I2C_2 bit is high(3)	9	False	True	ACTIVE	No State Change	Enable I2C CRC on I2C1 and I2C2 on all devices.
ON Request	10	False	False	STANDBY, ACTIVE, Suspend-to-RAM	ACTIVE	TO_ACTIVE
WKUP1 goes high	11	False	False	STANDBY, ACTIVE, Suspend-to-RAM	ACTIVE	
NSLEEP1 and NSLEEP2 are high(4)	12	False	False	STANDBY, ACTIVE, Suspend-to-RAM	ACTIVE	
NSLEEP1 goes low and NSLEEP2 goes high(4)	13	False	False	ACTIVE, Suspend-to-RAM	No State Change	No Sequence Executed

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Table 6-1. State Transition Triggers (continued)

Trigger	Priority (ID)	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
NSLEEP1 goes low and NSLEEP2 goes low(4)	14	False	False	ACTIVE	Suspend-to-RAM	TO_RETENTION
NSLEEP1 goes high and NSLEEP2 goes low(4)	15	False	False	ACTIVE	Suspend-to-RAM	
I2C_0 bit goes high(3)	16	False	False	STANDBY, ACTIVE	LP_STANDBY(2)	TO_STANDBY
I2C_3 bit goes high(3)	17	False	False	ACTIVE	No State Change	Devices are prepared for OTA NVM update.(5)

(1) From the SAFE state, the PFSM automatically transitions to the hardware FSM state of SAFE_RECOVERY. From the SAFE_RECOVERY state, the recovery counter is incremented and compared to the recovery count threshold (see RECOV_CNT_REG_2, in Table 5-10). If the recovery count threshold is reached, then the PMIC halts recovery attempts and requires a power cycle. Refer to the data sheet for more details.
(2) If the LP_STANDBY_SEL bit is set (see RTC_CTRL_2, in Table 5-10), then the PFSM transitions to the hardware FSM state of LP_STANDBY. When LP_STANDBY is entered, then please use the appropriate mechanism to wakeup the device as determined by the means of entering LP_STANDBY. Refer to the data sheet for more details.
(3) I2C_0, I2C_1, I2C_2 and I2C_3 are self-clearing triggers.
(4) NSLEEP1 and NSLEEP2 of the PMIC can be accessed through the GPIO pin or through a register bit. If either the register bit or the GPIO pin is pulled high, the NSLEEPx value is read as a *high* logic level.
(5) After completion of an OTA update, the processor is required to initiate a reset of the PMICs to apply the new NVM settings.

6.3 Power Sequences

6.3.1 TO_SAFE_SEVERE and TO_SAFE

The TO_SAFE_SEVERE and TO_SAFE are distinct sequences which occur when transition to the SAFE state. Both sequences shut down all rails without delay. To prevent any damage of the PMIC in case of over voltage on VCCA or thermal shutdown, the TO_SAFE_SEVERE sequence immediately ceases BUCK switching and enables the pulldown resistors of the BUCKs and LDOs. The timing is illustrated in Figure 6-2. The TO_SAFE sequence does not reset the BUCK regulators until after the regulators are turned off.

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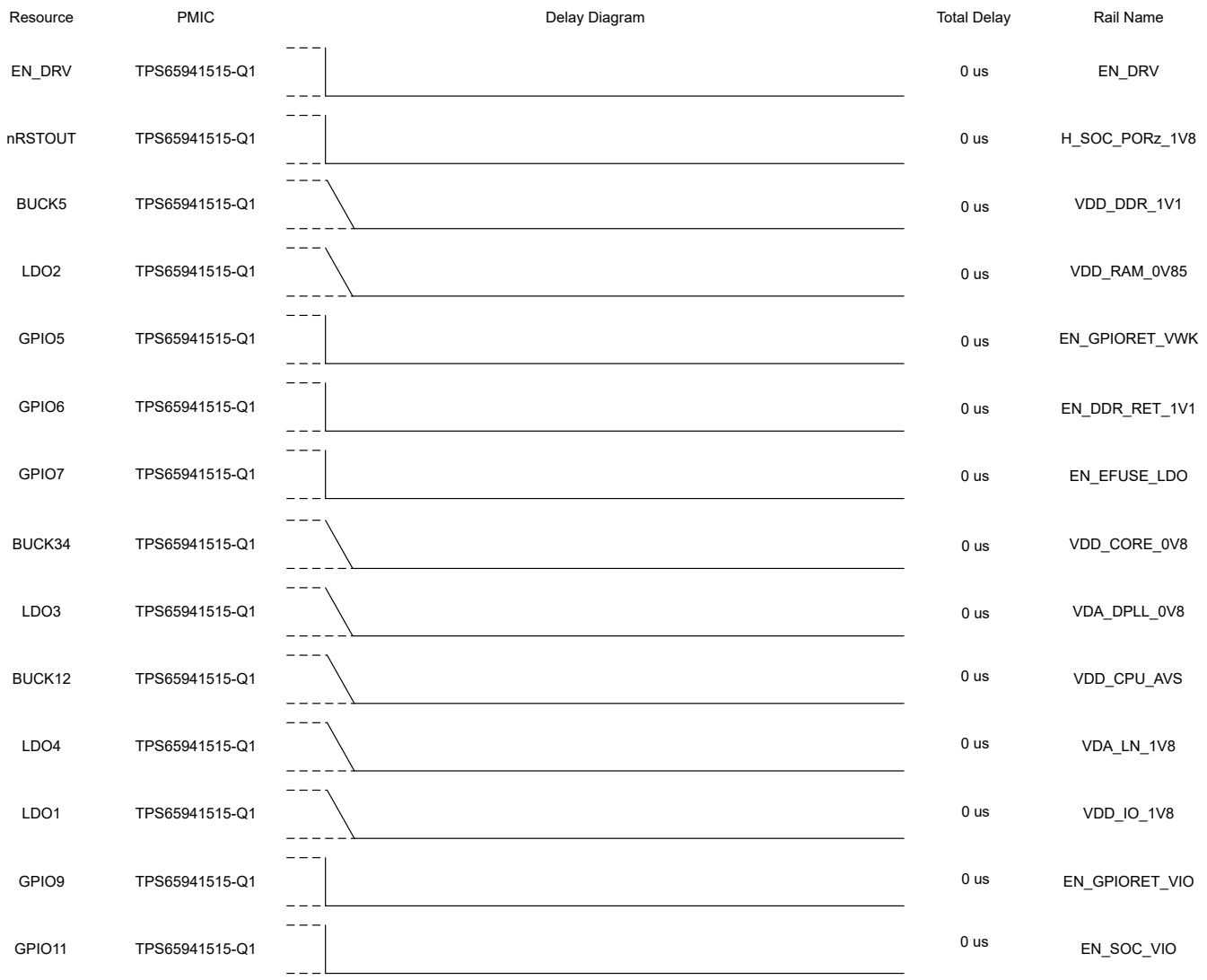

Figure 6-2. TO_SAFE_SEVERE and TO_SAFE Power Sequences

After the power sequence shown in Figure 6-2, the TO_SAFE sequence executes the following instructions:

```
// Clear AMUXOUT_EN, CLKMON_EN, set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
// Reset all BUCK regulators
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x1F MASK=0xE0
```

The TO_SAFE_SEVERE sequence executes the following instruction after the power sequence:

```
// Clear AMUXOUT_EN, CLKMON_EN, set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
```

The TPS65941515 has an additional delay of 500 ms at the end of the TO_SAFE_SEVERE sequence. It is important to note that the recovery is not attempted until after the sequence delay is complete.

6.3.2 TO_SAFE_ORDERLY and TO_STANDBY

If a moderate error occurs, an orderly shutdown trigger is generated. This trigger shuts down the PMIC outputs using the recommended power down sequence and proceed to the SAFE state.

If an OFF request occurs, such as the TPS65941515 ENABLE pin being pulled low, the same power down sequence occurs, except the PMIC goes to STANDBY (LP_STANDBY_SEL=0) or LP_STANDBY

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(LP_STANDBY_SEL=1) states, rather than going to the SAFE state. The power sequence for both of these events is shown in Figure 6-3.

Both the TO_SAFE_ORDERLY and TO_STANDBY sequences set the SPMI_LP_EN and FORCE_EN_DRV_LOW bits.

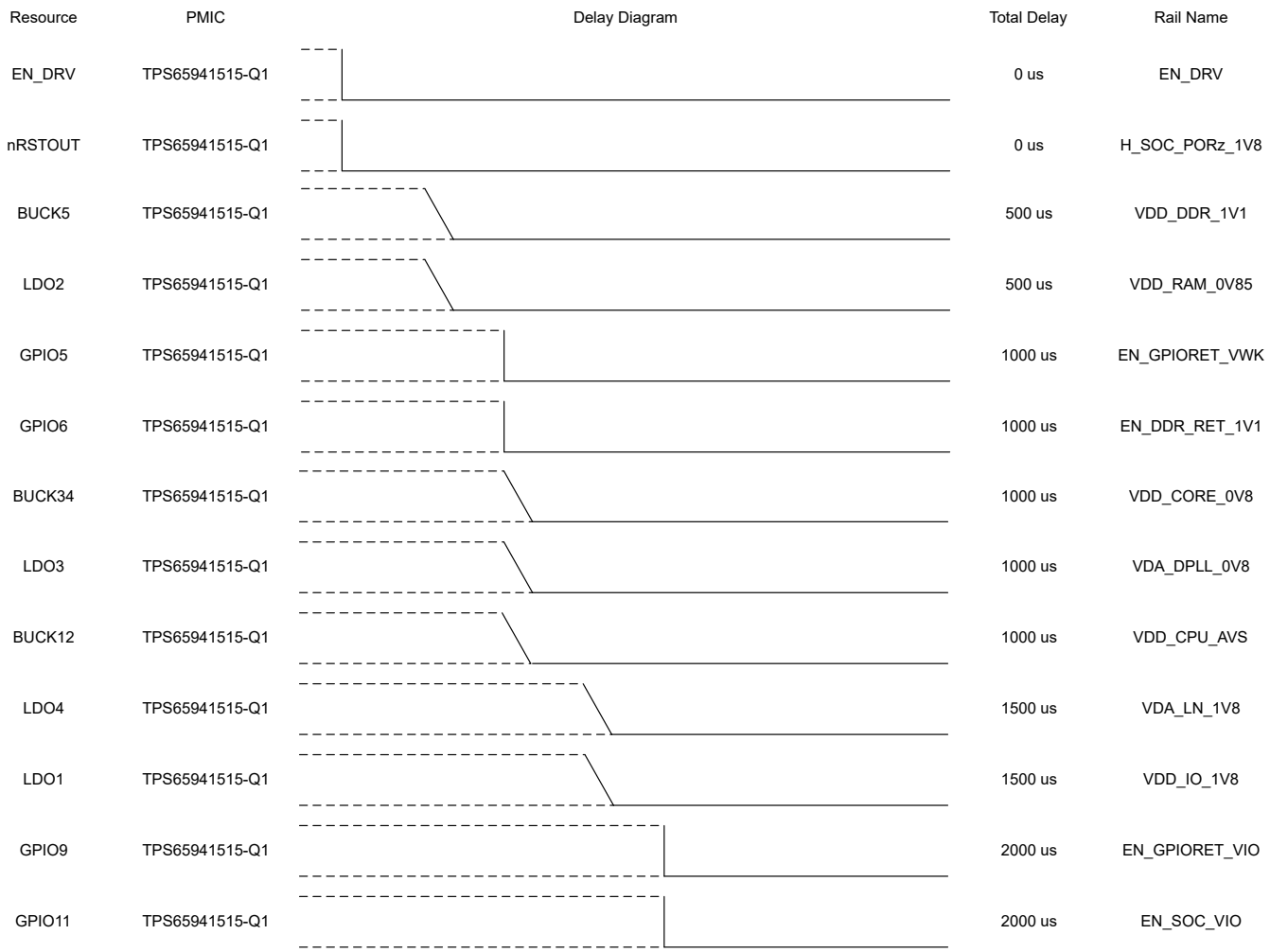

Figure 6-3. TO_SAFE_ORDERLY and TO_STANDBY Power Sequence

At the end of the TO_SAFE_ORDERLY sequence, the PMIC waits approximately 16 ms before executing the following instructions:

```
// Clear AMUXOUT_EN and CLKMON_EN and set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
// Reset all BUCKs
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x1F MASK=0xE0
```

The resetting of the BUCK regulators is done in preparation to transitioning to the SAFE_RECOVERY state. Transitioning to the SAFE_RECOVERY state means that the PMIC leaves the mission state. The SAFE_RECOVERY state is where the recovery mechanism increments the recovery counter and determine if the recovery count threshold (see Table 5-10) was achieved before attempting to recover.

At the end of the TO_STANDBY sequence, the TPS65941515 device waits approximately 16 ms before executing the same AMUXOUT_EN, CLKMON_EN, and LPM_EN bit manipulations. The BUCKs are not reset. After these instructions, the PMIC performs an additional check to determine if the LP_STANDBY_SEL (see Table 5-10) is true. If true, then the PMIC enters the LP_STANDBY state and leave the mission state. If the LP_STANDBY_SEL is false, then the PMIC remains in the mission state defined by STANDBY in Configured States.

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6.3.3 ACTIVE_TO_WARM

The ACTIVE_TO_WARM sequence can be triggered by either a watchdog or ESM_MCU error. In the event of a trigger, the nRSTOUT signal are driven low and the recovery count (register RECOV_CNT_REG_1) increments. Then, all BUCKs and LDOs are reset to their default voltages. The PMIC remains in the ACTIVE state.

Note

GPIOs do not reset during the sequence as shown in Figure 6-4

At the beginning of the sequence the following instructions are executed:

```
// Set FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x08 MASK=0xF7
// Clear nRSTOUT
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFC
// Increment the recovery counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
```

Note

The watchdog or ESM error is an indication of a significant error which has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery as with an MCU_POWER_ERR, however, in order to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented. If the recovery counter exceeds the recovery count threshold the PMIC stays in the safe recovery state.

Note

After the ACTIVE_TO_WARM sequence, the MCU is responsible for managing the EN_DRV and recovery counter. At the end of the sequence the 'FORCE_EN_DRV_LOW' bit is cleared so that the MCU can set the ENABLE_DRV bit.

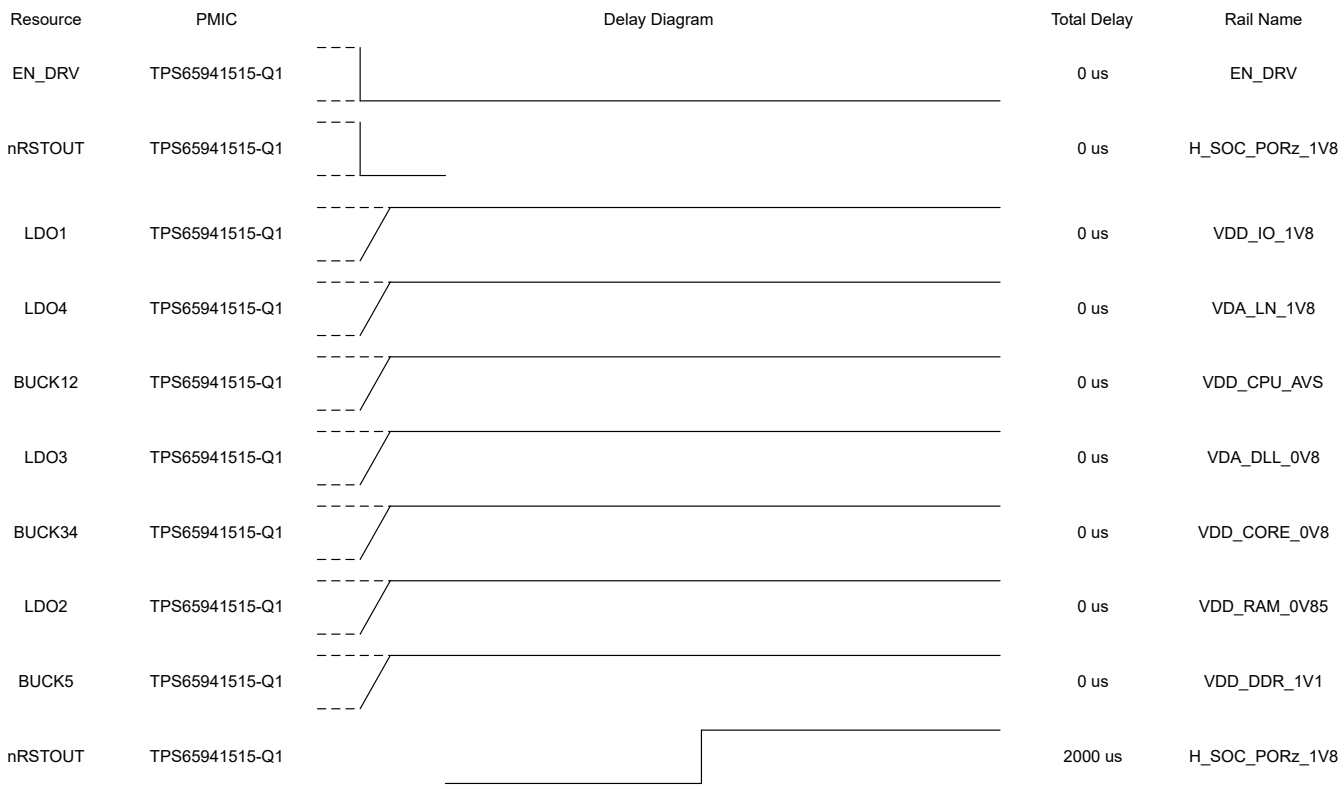

Figure 6-4. ACTIVE_TO_WARM Power Sequence

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Note

The regulator transitions do not represent enabling of the regulators but the time at which the voltages are restored to their default values. Since this sequence originates from the ACTIVE state all of the regulators are on.

6.3.4 TO_ACTIVE

When a trigger causes the TO_ACTIVE sequence to execute, all rails power up in the recommended power up sequence as shown in Figure 6-5.

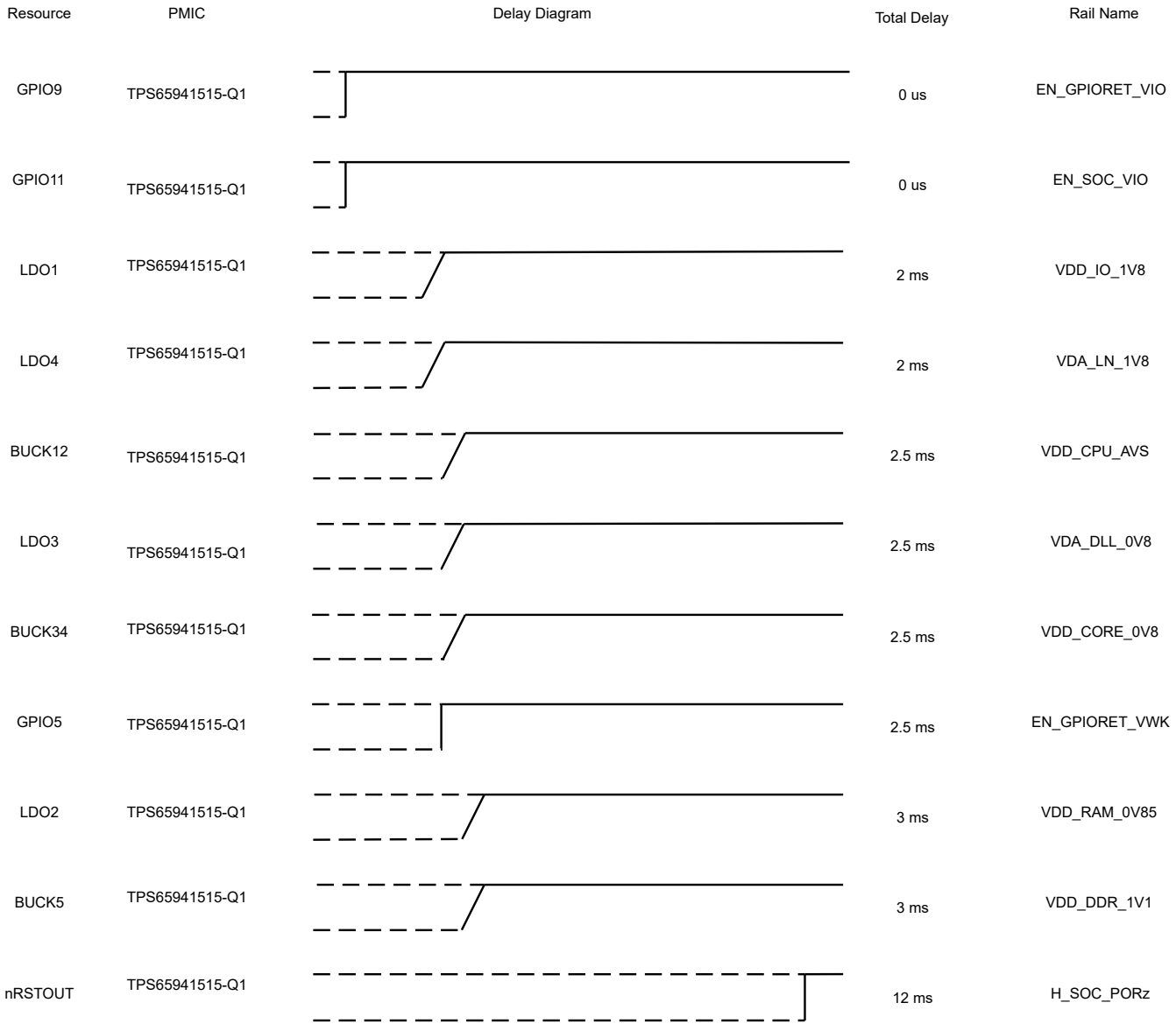

Figure 6-5. TO_ACTIVE Sequence

At the end of the TO_ACTIVE sequence the 'FORCE_EN_DRV_LOW' bit is cleared.

Note

After the TO_ACTIVE sequence the MCU is responsible for managing the EN_DRV.

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6.3.5 TO_RETENTION

The C and D triggers, defined by the NSLEEPx bits or pins, trigger the TO_RETENTION sequence. This sequence disables all power rails and GPIOs that are not supplying the retention rails, as described in Figure 3-1. The sequence can be modified using the I2C_7 and I2C_6 bits found in register FSM_I2C_TRIGGERS. These bits need to be set by I^2C before a trigger for the retention state occurs. If the I2C_7 bit is set high, the PMIC enters the DDR retention state. If I2C_6 bit is set high, the PMIC enters the GPIO retention state. TO_RETENTION sequence with GPIO and DDR retention is shown in Figure 6-7. If I2C_6 and I2C_7 are set low, the components associated with DDR and GPIO retention do not remain active, as shown in Figure 6-6.

Note

The I2C_6 and I2C_7 bits need to be set or cleared by I^2C in the PMIC before a trigger to the retention state occurs. The triggers are not self-clearing and must be maintained during operation.

In addition to the I2C_7, the processor must also configure the EN_DDR_RET_1V1 signal on GPIO6. This signal is included in the Section 3.2 but is not part of the power sequence.

The following PMIC PFSM instructions are executed automatically in the beginning of the power sequence to configure the PMIC:

```
// Clear NRSTOUT
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFE
// Set SPMI_LP_EN and FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x18 MASK=0xE7
```

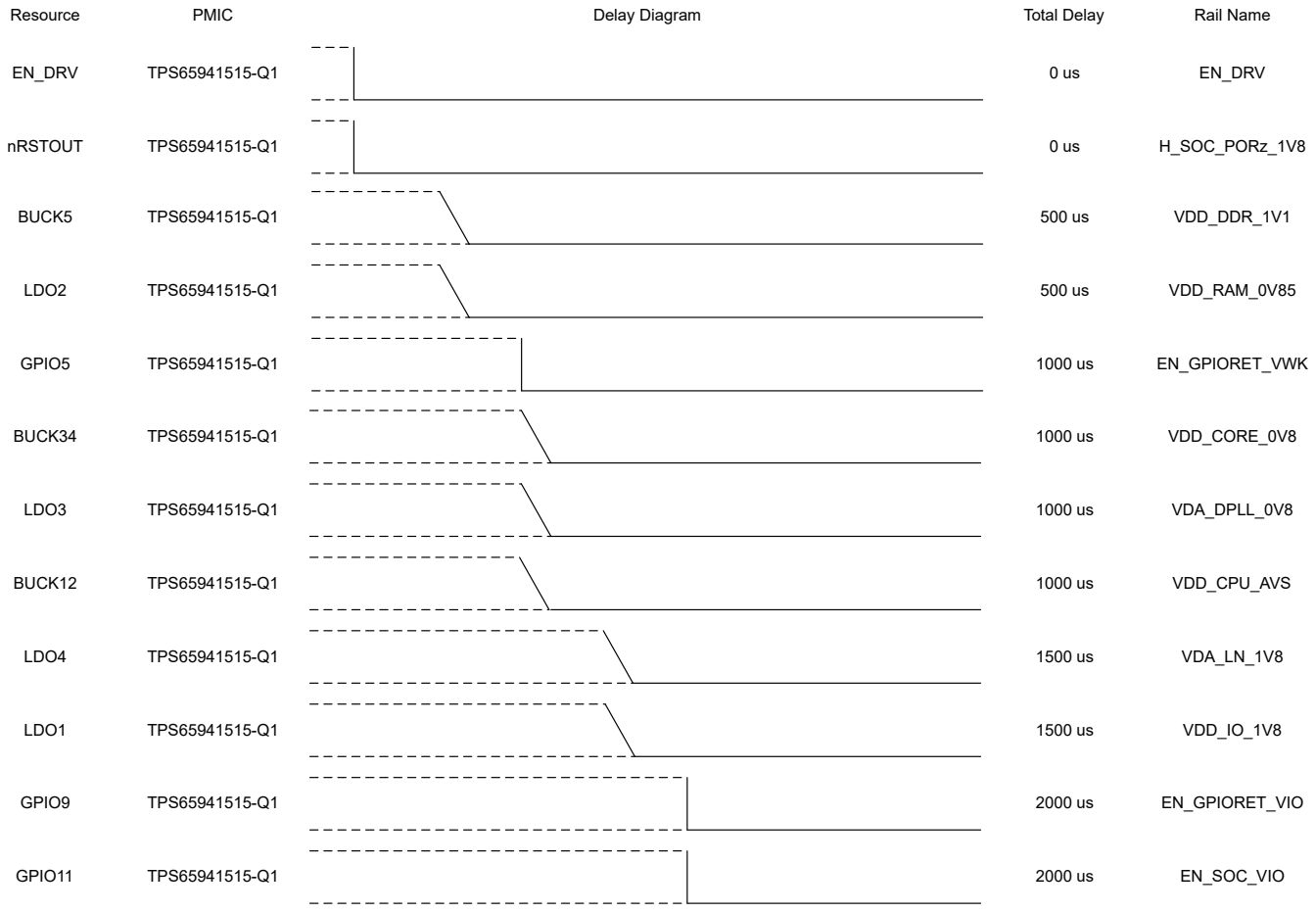

Figure 6-6. TO_RETENTION when I2C_6 and I2C_7 are Low

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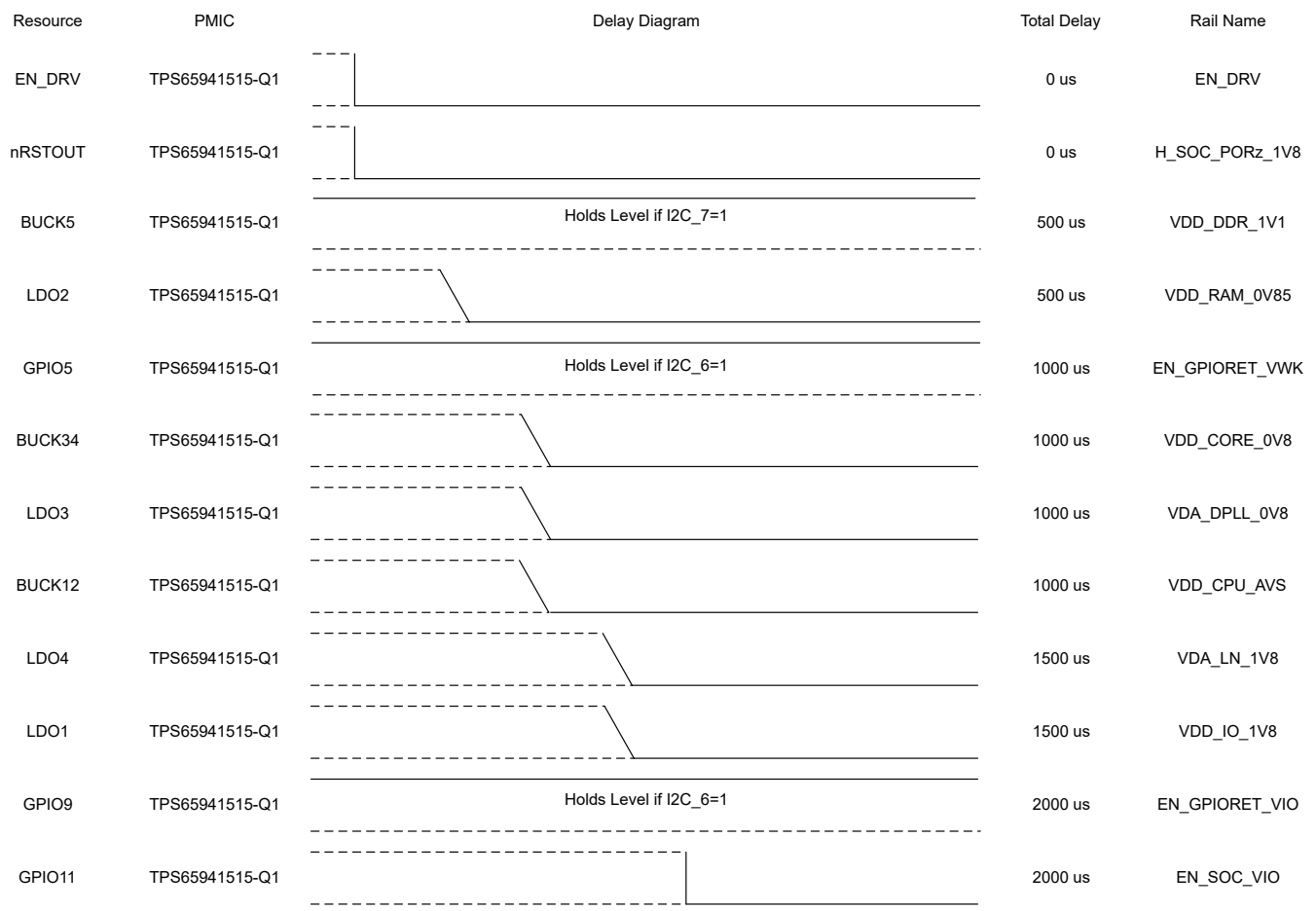

Figure 6-7. TO_RETENTION when I2C_6 and I2C_7 are High

At the end of the sequence, PMIC sets the LPM_EN and clears the CLKMON_EN and AMUXOUT_EN bits.

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7 Application Examples

This section provides examples of how to interact with the PMICs from the perspective of the MCU and over I^{2}C. I ^{2} C Instruction Format shows how the I^{2}C commands are presented in the following sections. These examples, when used in conjunction with the data sheet, can be generalized and applied to other use cases.

Table 7-1. I^{2}C Instruction Format

I2C Address	Register Address	Data	Mask
0x48 or 0x4C	0x00 - 0xFF	0x00 - 0xFF	0x00 - 0xFF

7.1 Moving Between States: ACTIVE and RETENTION

The default configuration of the NVM transitions the PMICs to the ACTIVE state when the ENABLE pin on the TPS65941515 goes high (rising edge triggered). The nINT pin goes high to indicate to the MCU that interrupts have occurred in the PMICs. After a normal power up sequence the interrupts are the ENABLE_INT and BIST_PASS_INT. The ENABLE_INT prohibits the PMICs from processing any lower priority triggers below the 'ON Request' in State Transition Triggers. Once the ENABLE_INT is cleared the state is defined by Table 7-2. The following sections describe the I^{2}C commands for transitioning between the different states.

Table 7-2. State Table

NSLEEP1	NSLEEP2	I2C_7	I2C_6	State
1	1	NA	NA	ACTIVE
0	1	NA	NA	No State Change
Do not Care	0	1	NA	DDR Retention
	0	NA	1	GPIO Retention
	0	0	0	Retention

7.1.1 ACTIVE

In this example the, PMIC is already in the ACTIVE state after a normal power up event. The PMIC is kept in the ACTIVE state by setting the NSLEEP1 and NSLEEP2 bits before clearing the ENABLE_INT.

```
Write 0x48:0x86:0x03:0xFC    // Set NSLEEP1 and NSLEEP2 in TPS65941515
Write 0x48:0x66:0x01:0xFE    // Clear BIST_PASS_INT
Write 0x48:0x65:0x26:0xD9    // Clear all potential sources of the On Request
```

7.1.2 RETENTION

As shown in TO_RETENTION, the MCU is powered off and therefore the transition out of the RETENTION to the ACTIVE state must be configured before entering RETENTION. The I2C_6 and I2C_7 triggers must be set depending on the type of retention mode. Below is an example of entering GPIO RETENTION (I2C_6=1) and using TPS65941515 GPIO4 to wake the PMIC into the ACTIVE state.

```
Write 0x48:0x85:0x40:0x7F    //I2C_6 is high
Write 0x48:0x34:0xC0:0x3F    //Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0x64:0x08:0xF7    //clear interrupt for GPIO4 falling edge
Write 0x48:0x4F:0x00:0xF7    //unmask interrupt for GPIO4 falling edge
Write 0x48:0x86:0x00:0xFC    //trigger the TO_RETENTION power sequence
After the GPIO4 has gone low and the PMIC returns to the ACTIVE state
Write 0x48:0x86:0x03:0xFC    //Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7    //clear interrupt of GPIO4
```

Below is example of entering DDR RETENTION (I2C_7 = 1) and using the TPS65941515 RTC Timer to wake the PMIC into the ACTIVE state.

```
Write 0x48:0x85:0x80:0x7F     // I2C_7 is high
Write 0x48:0xC3:0x01;0xFE     // Enable Crystal
Write 0x48:0xC5:0x05:0xF8     // minute timer, enable TIMER interrupts
Write 0x48:0xC2:0x01:0xFE     // start timer, if the timer values are non-zero clear before starting
Write 0x48:0x86:0x00:0xFC     // trigger the TO_RETENTION power sequence
```


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```
After the RTC Timer interrupt has occurred and the PMIC returns to the ACTIVE state
Write 0x48:0x86:0x03:0xFC     // Set NSLEEPx bits for ACTIVE state
Write 0x48:0xC5:0x00:0xFB     // disable timer interrupt, clear bit 2
Write 0x48:0xC4:0x00:0xDF     // clear timer interrupt, clear bit 5
```

7.2 Entering and Exiting Standby

STANDBY can be entered from the ACTIVE or the RETENTION states. To stay in the mission state of STANDBY and not enter the hardware state LP_STANDBY, the LP_STANDBY_SEL bit must be cleared.

When the ENABLE pin goes low, the TO_STANDBY sequence is triggered. When the ENABLE pin goes high again, the destination state is dependent upon the STARTUP_DEST bits. For the TPS65941515, the STARTUP_DEST must be set for the ACTIVE state. The TO_STANDBY sequence is also triggered by the I2C_0 trigger. When triggered from I2C_0 the PMIC can be triggered to return to the ACTIVE state by GPIO4 or the RTC timer or alarm. In this example, I2C_0 trigger is used to enter the STANDBY state and the GPIO4 is used to enter the ACTIVE state.

```
Write 0x48:0xC3:0x00:0xF7  // LP_STANDBY_SEL=0
Write 0x48:0x7D:0xC0:0x3F  // Mask NSLEEP bits
Write 0x48:0x34:0xC0;0x3F  // Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x4F:0x00:0xF7  // unmask interrupt for GPIO4 falling edge
Write 0x48:0x85:0x01:0xFE  // set I2C_0 trigger, trigger TO_STANDBY sequence
After the GPIO4 has gone low and the PMIC has returned to the ACTIVE state
Write 0x48:0x7D:0x00:0x3F  // unmask NSLEEP bits
Write 0x48:0x86:0x03:0xFC  // Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
```

7.3 Entering and Existing LP_STANDBY

Entering the LP_STANDBY hardware state is the same as entering STANDBY. Exiting LP_STANDBY is different and requires different initializations before entering LP_STANDBY. Also, when the PMIC returns from LP_STANDBY the PFSM triggers are gated by the ENABLE_INT while in STANDBY the triggers were gated by the GPIO interrupt.

```
Write 0x48:0xC3:0x08:0xF7  // LP_STANDBY_SEL=1
Write 0x48:0x7D:0xC0:0x3F  // Mask NSLEEP bits
Write 0x48:0x34:0xC0;0x3F  // Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0xC3:0x60;0x9F  // Set the STARTUP_DEST=ACTIVE
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x4F:0x00:0xF7  // unmask interrupt for GPIO4 falling edge
Write 0x48:0x85:0x01:0xFE  // set I2C_0 trigger, trigger TO_STANDBY sequence
After the GPIO4 has gone low and the PMIC has returned to the ACTIVE state
Write 0x48:0x7D:0x00:0x3F  // unmask NSLEEP bits
Write 0x48:0x86:0x03:0xFC  // Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x65:0x02:0xFD  // clear ENABLE_INT
```

7.4 GPIO8 and Watchdog

The TPS65941515 GPIO8 is configured as an input to disable the watchdog. Typically, during development this pin is tied high, so that when the nRSTOUT bit is set WD_PWRHOLD is also set. The configuration of this pin can be utilized for other features or functions but this requires servicing the watchdog before it expires. The watchdog long window is 772 seconds.

```
Write 0x12:0x09:0x00:0xBF // Disable Watchdog
Write 0x48:0x38:0x01:0x00 // configure GPIO8 as a pushpull output
```

When it is time to enable and configure the watchdog, then in addition to enabling the watchdog the WD_PWR_HOLD must be cleared.

```
Write 0x12:0x09:0x00:0xFB // Clear WD_PWRHOLD
Write 0x12:0x09:0x40:0xBF // Enable Watchdog
```


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8 References

For additional information regarding the PMIC or processor devices, use the following:

- Texas Instruments, *DRA821Jacinto™ Processors Datasheet*
- Texas Instruments, DRA821 Safety Manual Jacinto™ 7 Processors (request through mySecure)
- Texas Instruments, *J7200 DRA821 Processor Silicon Revision 1.0 Technical* Reference Manual
- Texas Instruments, *TPS6594-Q1 Power Management IC (PMIC) with 5 Bucks and 4 LDOs for Safety-Relevant Automotive Applications* data sheet
- Texas Instruments, TPS6594-Q1 Safety Manual (request through mySecure)
- Texas Instruments, *TPS6594-Q1 Schematic PCB Checklist* application note

9 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2022) to Revision A (July 2026)	Page
• Updated the document title.	1
• Updated the document format to a design guide.	1
• Added Description, Features, and Applications topics.	1
• Orderable part numbers and corresponding TI_NVM_ID and TI_NVM_REV register values were updated.	3

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