

AM62A Power-Supply Proof-of-Concept Design Using the TPS6593-Q1



Description

The TPS65931211-Q1 PMIC is an automotive-grade power management IC designed for the AM62A processor. This design provides multiphase buck conversion up to 10.5A, supports ASIL-B functional safety requirements, and offers multiple low-power modes including suspend-to-RAM and partial I/O operation for automotive applications.

Resources

TIPA-050066	Design Folder
TPS6593-Q1	Product Folder
AM62A	Product Folder
TPS22965-Q1	Product Folder
TPS62824	Product Folder
LM5141-Q1	Product Folder

Features

- Multiphase buck configuration
- Functional safety ASIL-B support
- Multiple low power modes
- Flexible power supply options
- Programmable GPIO control
- Pre-Configurable Finite State Machine (PFSM)

Applications

- [Advanced driver assistance systems \(ADAS\)](#)
- [In-cabin monitoring ECU](#)



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1 System Description

This user's guide describes a power distribution network (PDN), using the TPS65931211-Q1 PMIC to supply the Sitara™ AM62A processor.

The following topics are described to clarify platform system operation:

1. PDN power resource connections
2. PDN digital control connections
3. PMIC static NVM configuration
4. PMIC Pre-configurable Mission States

PMIC and processor data manuals provide recommended operating conditions, electrical characteristics, recommended external components, package details, register maps, and overall component functionality. In the event of any inconsistency between any user's guide, application brief, or other referenced material, the datasheet specification is the definitive source.

2 Device Versions

There are different orderable part numbers (OPNs) of the TPS6593-Q1 device available with unique NVM settings to support different end product use cases and processor types. The unique NVM settings for each PMIC device are optimized per PDN design to support different processors, processing loads, SDRAM types, system functional safety levels, and end product features (such as low power modes, processor voltages, and memory subsystems). The NVM settings can be identified by both NVM_ID and NVM_REV registers. Each TPS6593 PMIC device is distinguished by the part number, NVM_ID, and NVM_REV.

Table 2-1. TPS6593-Q1 Orderable Part Number for AM62A

PDN USE CASE	Orderable Part Number	TI_NVM_ID (TI_NVM_REV)
<ul style="list-style-type: none"> • Supports Functional Safety up to ASIL-B level. • Supports AM62A low power modes (including Partial IO and Suspend to RAM). • Up to 10.5A⁽¹⁾ in multiphase (3-phase) configuration to supply the processor CORE rail with selectable 0.75V or 0.85V. • Up to 4A⁽¹⁾ to supply the VDDSD_DDR with selectable 1.1V for LPDDR4. • Supports I/O level of 3.3V and 1.8V. • Supports optional end product features: <ul style="list-style-type: none"> – Compliant high-speed SD Card memory – eMMC – eFuse ROM programming supply – Compliant USB 2.0 Interface – Ethernet PHY – HDMI 	TPS65931211 RWERQ1	0x11 (0x05)

(1) TI recommends having 15% margin between the maximum expected load current and the maximum current allowed per each PMIC output rail.

3 Processor Connections

This section details how the TPS65931211-Q1 power resources and GPIO signals are connected to the processor and other peripheral components.

3.1 Power Mapping

Figure 3-1 shows the power mapping between the TPS65931211-Q1 PMIC power resources and processor voltage domains. Some of the external peripherals like uSD card, Ethernet PHY and HDMI are optional and can be omitted if the peripherals are not needed for the end product. These optional systems peripherals are included in the AM62A SK EVM for development and testing purposes.

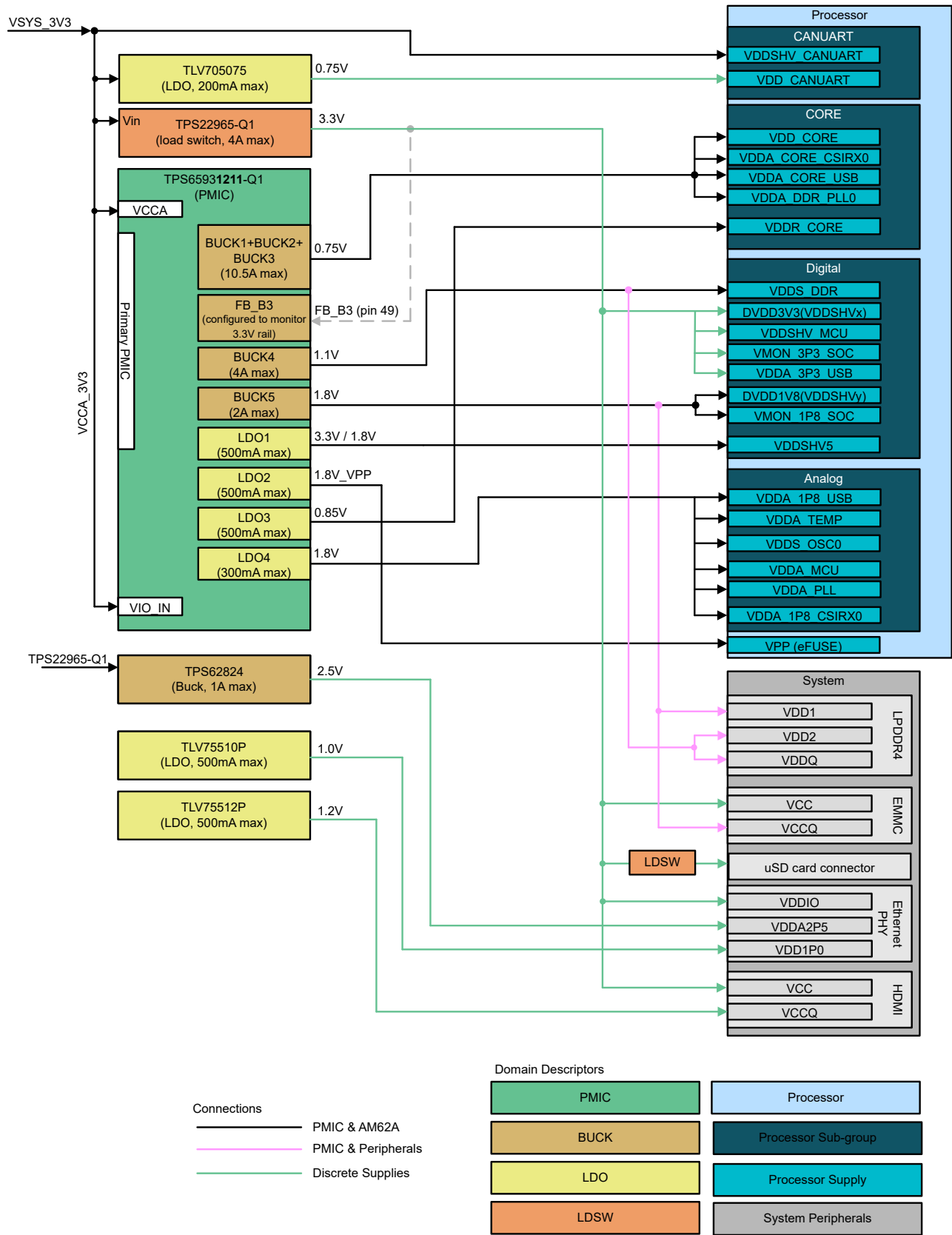
This PDN uses the TPS6593-Q1 PMIC and discrete power components to meet the power/sequence requirements of the processor and system peripherals. Some of the discrete components are optional depending upon end product features. In this configuration, PMIC uses a 3.3V input voltage. The TPS22965 Load Switch connects the 3.3V pre-regulator (VSYS_3V3) to the processor 3.3V IO domains. The unused feedback pin, FB_B3, of the TPS65931211-Q1 has been configured per NVM settings, Table 5-3, to provide voltage monitoring for the 3.3V IO domain. This monitoring function enables all of the processor CORE, digital and analog supplies to have voltage monitoring coverage as needed for functional safety ASIL-B systems.

LDO1 of the TPS65931211-Q1 PMIC is configured as bypass to supply the SD card dual-voltage I/O (3.3V and 1.8V). A processor GPIO control signal with a logic high default value and an external pull-up is used to set SD IO to 3.3V initially. After the power-up sequence, the processor can set GPIO signal low to select 1.8V level as needed for high-speed card operation per SD specification. This bypass configuration allows control of the LDO1 voltage from 3.3V to 1.8V without the need to establish I2C communication during boot from SD card operations. The bypass configuration on LDO1 requires connecting the input supply pin (PVIN_LDO12) to 3.3V.

The AM62A processor supports multiple low power modes. For the Partial I/O low power mode, the entire SoC is OFF except I/O pins in CANUART I/O bank to maintain wakeup capability. This mode is supported by turning OFF the PMIC and keeping the 3.3V pre-regulator ON to supply VDDSHV_CANUART (3.3V) and an external discrete to supply VDD_CANUART (0.75V or 0.85V).

Note

The PMIC voltage monitor on FB_B3 must be connected to 3.3V. If 3.3V is not connected to FB_B3 when the monitor is enabled then the device goes to the hardware SAFE RECOVERY state, and the processor voltages are disabled.



Note

The external discrete that supplies VDD_CANUART is only needed for Partial IO. When not using Partial IO, VDD_CANUART needs to be connected to the multi-phase Buck1/2/3 and VDDSHV_CANUART can be connected to the same 3.3V rail that supplies the DVDD3V3(VDDSHVx).

Figure 3-1. Example Power Connections

Table 3-1 identifies which power resources are required to support different system features.

Table 3-1. PDN Power Mapping and System Features

Power Mapping				System Features			
Device	Power Resource	Voltage	Processor Domains	Active SoC	Partial IO (Low Power Mode)	IO + DDR (Low Power Mode)	SD Card interface
3.3V pre-regulator (LM5141-Q1)	BUCK	3.3V	VDDSHV_CANUART PMIC Supply	Required	Required	Required	
TLV705075	LDO	0.75V	VDD_CANUART	Required	Required	Required	
TPS65931211-Q1	BUCK123	0.75V or 0.85V ⁽¹⁾	VDD_CORE	Required			
			VDDA_CORE_CSIRX0	Required			
			VDDA_CORE_USB	Required			
			VDDA_DDR_PLL0	Required			
	FB_B3	3.3V	monitors 3.3V IO domain	Required		Required	
	BUCK4	1.1V or 1.2V	VDDS_DDR	Required		Required	
	BUCK5	1.8V	DVDD1V8(VDDSHVy)	Required		Required	
			VMON_1P8_SOC ⁽²⁾	Optional			
	LDO1	3.3V / 1.8V	VDDSHV5	Optional			Required
	LDO2	1.8V	VPP (eFUSE)	Optional			
	LDO3	0.85V ⁽¹⁾	VDDR_CORE	Required			
	LDO4	1.8V	VDDA_1P8_USB	Required			
			VDDA_TEMP	Required			
VDDS_OSC0			Required				
VDDA_MCU			Required				
VDDA_PLL			Required				
VDDA_1P8_CSIRX0			Required				
TPS22965-Q1	Load Switch	3.3V	DVDD3V3(VDDSHVx)	Required			
			VDDSHV_MCU	Required			
			VMON_3P3_SOC ⁽²⁾	Optional			
			VDDA_3P3_USB	Required			
TPS62824	BUCK	2.5V	VDD_2V5_ETHERNET PHY	Optional			
TLV75510P	LDO	1.0V	VDD1P0_ETHERNET PHY	Optional			
TLV75512P	LDO	1.2V	CVCC12_HDMI TRANSMITTER	Optional			

- (1) If the multiphase Buck1/2/3 is configured to output 0.85V, both CORE rails on the AM62A (VDD_CORE and VDDR_CORE) are supplied by Buck1/2/3. In this case, LDO3 becomes a free power resource.
- (2) VMON_3P3_SOC and VMON_1P8_SOC are not supply pins but voltage monitor inputs for the 1.8V and 3.3V SoC power supply. If VMON_1P8_SOC and VMON_3P3_SOC are not used to monitor the SOC power rails, the pins must still be connected to the respective 1.8V and 3.3V power rails.

3.1.1 Supporting 0.85V on VDD_CORE

In this PDN, VDD_CORE is operating at 0.75V and supplied by the multi-phase Buck1/2/3. VDDR_CORE is supplied by LDO3 (0.85V). However, if BUCK1/2/3 is configured to output 0.85V, then both CORE rails (VDD_CORE and VDDR_CORE) must be supplied by BUCK1/2/3 and LDO3 becomes a free resource. According to the [AM62Ax datasheet](#), VDD_CORE and VDDR_CORE are expected to be powered by the same source so both pins ramp together when VDD_CORE is operating at 0.85V. LDO3 is configured to be part of the TPS65931211-Q1 power-up sequence and requires an input supply as well as the input/output capacitors to prevent an LDO3 fault condition. The state of GPIO6 sets the output voltage on the multi-phase Buck1/2/3. See [Section 3.2](#) for information about polarity of digital pins.

3.1.2 Using 5V Input Supply

The PDN described in this user's guide was designed for 3.3V input supply. However the TPS65931211-Q1 NVM also supports 5V input supply. The default NVM settings on TPS65931211-Q1 have the UV/OV disabled on VCCA so PMIC can use either voltage (3.3V or 5V). If 5V supply is used, then a 3.3V discrete Buck is required for the 3.3V IO domain instead of a power switch. The external 3.3V Buck can be enabled by GPIO4 and needs to ramp from 0V to 3.3V within the 10ms delay that was assigned to GPIO4 in the any2active sequence.

LDO1 is configured as “bypass” and requires a 3.3V supply. This LDO can be supplied by the output of the discrete 3.3V regulator. TI also recommends supplying the remaining LDOs (LDO3 and LDO4) with the discrete 3.3V regulator to reduce power dissipation. VIO_IN must be supplied by 3.3V as well.

When using 5V instead of 3.3V, the voltage from the pre-regulator cannot be directly connected to VDDSHV_CANUART. In this case, VDDSHV_CANUART can be supplied by the same discrete 3.3V Buck that supplies the remaining 3.3V signals on the processor.

3.2 Control Mapping

Figure 3-2 shows the digital control signal mapping between processor and PMIC. Specific GPIO pins have been assigned to key signals for proper operation. The digital connections allow system features including Partial IO, I/O plus DDR, functional safety up to ASIL-B, and compliant dual voltage SD card operation. GPIO4 was configured as push-pull output to enable the external 3.3V power-switch at the beginning of the sequence.

GPIO9 and GPIO11 are configured to enable LDO2 (VPP) and LDO1 (SD card interface). The TPS65931211-Q1 enables LDO1 when a rising edge is detected on GPIO11 after nRSTOUT is released and PMIC is in Active state. Similarly, the PMIC enables LDO2 when a rising edge is detected on GPO9 after nRSTOUT is released.

GPIO5, GPIO6 and GPIO10 are configured to set the output voltages on some of the PMIC power resources and the state (high or low) for these GPIOs need to be set before the assigned rail turns ON. GPIO5 is configured to set the output voltage on LDO1 to support UHS-I SD cards (3.3V or 1.8V). GPIO6 is configured to set the voltage on the multiphase Buck1/2/3 to support either VDD_CORE voltage (0.75V or 0.85V). GPIO10 is configured to set the voltage on Buck4 to support LPDDR4 (1.1V) or DDR4 (1.2V).

The PMIC_LPM_EN0 on the AM62A processor is a dual function control signal used to trigger a Low Power Mode (active low) or PMIC enable (active high). This signal drives the PMIC GPIO3 (nSLEEP2) when triggering IO+DDR mode (suspend to RAM). Alternatively, the PMIC_LPM_EN0 signal can drive the PMIC enable pin when triggering Partial IO low power mode.

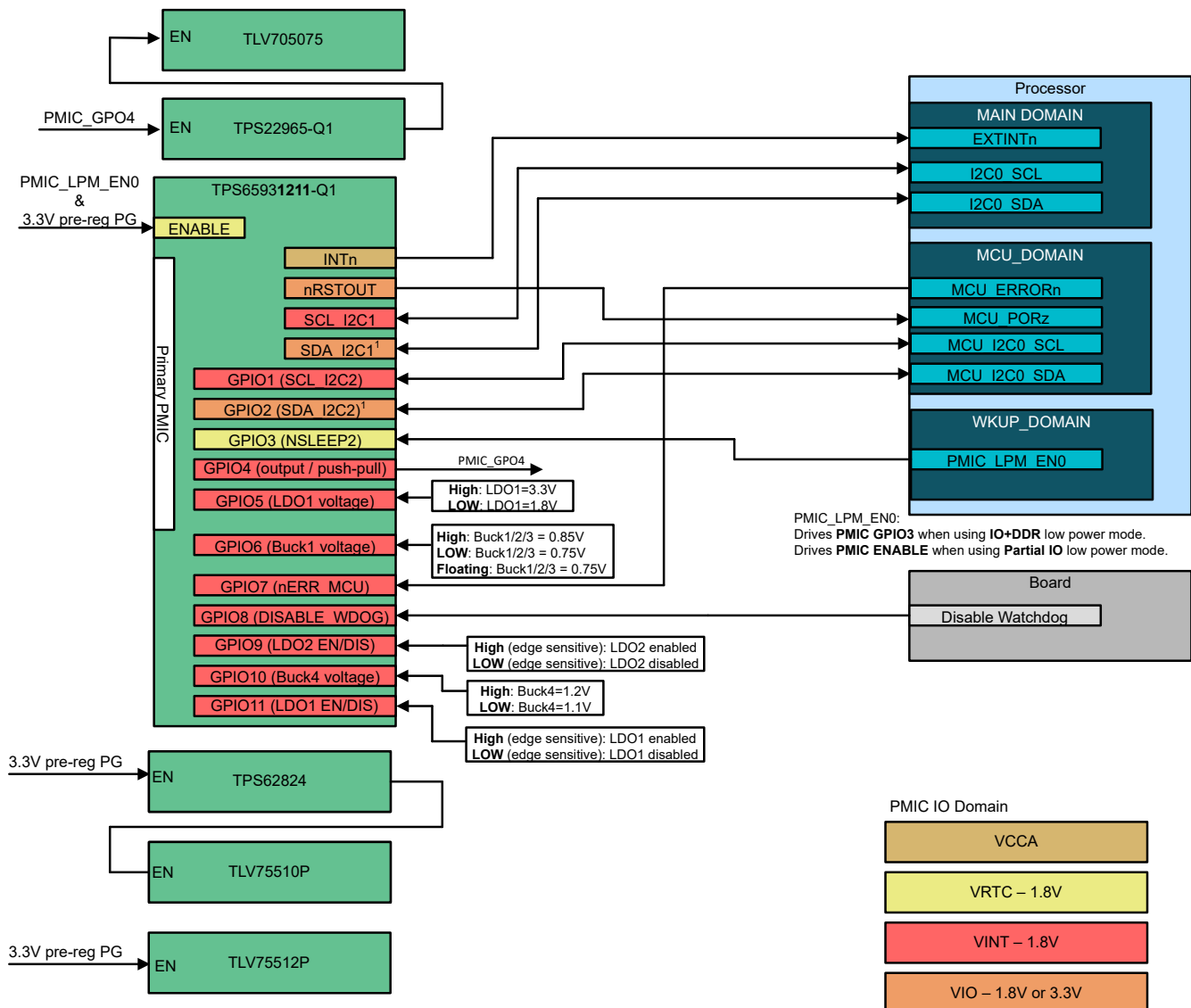


Figure 3-2. TPS65931211-Q1 Digital Connections

Note

PMIC IO can have distinct power domains for input and output functionality. The SDA function for I2C1 and I2C2 use the VINT voltage domain as an input and the VIO voltage domain as an output. When configured as an input GPIO3 is in the VRTC domain. When configured as an output, GPIO4 is in the VINT domain. Please refer to the device [datasheet](#) for a complete description.

[Table 3-2](#) shows the digital signals on the TPS65931211-Q1 and the AM62A domain that the signals must be pulled up to. These digital signals were configured as open drain.

Table 3-2. Open-drain signals and AM62 Power Domain

PMIC open drain signal	AM62A signal name	AM62A Power Domain
nINT	EXTINTn	VDDSHV0
nRSTOUT	MCU_PORz	VDDS_OSC (1.8V)
SCL_I2C1	I2C0_SCL	VDDSHV0
SDA_I2C1	I2C0_SDA	VDDSHV0
GPIO1 (SCL_I2C2)	MCU_I2C0_SCL	VDDSHV_MCU
GPIO2 (SDA_I2C2)	MCU_I2C0_SDA	VDDSHV_MCU

Please use [Table 3-3](#) as a guide to understand GPIO assignments required for each PDN system feature. If the feature listed is not required, the digital connection can be removed; however, the GPIO pin is still configured per NVM defined default function shown. After the processor has booted up, the processor can reconfigure unused GPIOs to support new functions. Reconfiguring a GPIO function is possible as long as that function is only needed after boot and default function does not cause any conflicts with normal operations (for example, two outputs driving same net).

Table 3-3. Digital Connections by System Feature

Device	GPIO Mapping		System Features			
	PMIC Pin	NVM Function	Active SoC	Functional Safety	IO + DDR	SD Card
TPS65931211-Q1	nPWRON/ ENABLE	Enable	Required	Required		
	INT	INT	Required	Required		
	nRSTOUT	nRSTOUT	Required			
	SCL_I2C1	SCL_I2C1	Required			
	SDA_I2C1	SDA_I2C1	Required			
	GPIO_1	SCL_I2C2		Required		
	GPIO_2	SDA_I2C2		Required		
	GPIO_3	nSLEEP2			Required	
	GPIO_4	GPO (enables 3.3V power-switch)	Required			
	GPIO_5	GPI (sets output voltage on LDO1)	Optional ⁽²⁾			Required
	GPIO_6	GPI (sets output voltage on BUCK1/2/3)	Required			
	GPIO_7	nERR_MCU			Required	
	GPIO_8	DISABLE_WDOG			Optional ⁽¹⁾	
GPIO_9	GPI (enables/disables LDO2)					
GPIO_10	GPI (sets output voltage on BUCK4)	Required				
GPIO_11	GPI (enables/disables LDO1)				Required	

- (1) To disable the watchdog through hardware, GPIO_8 is required and must be set high by the time nRSTOUT goes high. After nRSTOUT is high, the watchdog state is latched and the pin can be configured for other functions through software.
- (2) GPIO5 from the PMIC does not need to be connected to the processor if LDO1 is not used to supply the uSD card interface.

4 Supporting Functional Safety ASIL-B Requirements

To achieve a system functional safety level of ASIL-B, the following PDN features are available:

- PMIC over voltage and under voltage monitoring on the power resource voltage outputs
- Watchdog monitoring of safety processor
- MCU error monitoring
- MCU and Main Domain cold reset
- I²C communication
- Error indicator, EN_DRV, for driving external circuitry (optional)
- Read-back of EN_DRV pin

4.1 Additional Safety Features

- PMIC current monitoring on all output power rails
- Switch short-to-ground detection on BUCK regulator pins (SW_Bx)
- Read-back of nINT and nRSTOUT logic output pins

The PMIC internal over voltage and under voltage monitoring and the respective monitoring threshold levels are enabled by default and can be updated through I²C after startup. PMIC power rails connected directly to the processor are monitored by default. The unused feedback pin of BUCK3 on TPS65931211-Q1, FB_B3, is assigned to monitor the load switch output voltage that supplies the 3.3V I/O domain. A 3.3V supply must be connected to the feedback pin to prevent an error since the PMIC is expecting the 3.3V to be present.

The internal Q&A Watchdog is enabled on the TPS65931211-Q1 NVM. Once the device is in ACTIVE state, the trigger or Q&A watchdog settings can be configured through the secondary I2C (GPIO1/GPIO2) in the device. The primary and secondary I2C CRC is not enabled by default but must be enabled with the I2C_2 trigger described in [Section 6.2](#). Once enabled the secondary I2C is disabled for 2ms. TI recommends enabling I2C CRC and wait a minimum of 2ms before starting the Q&A Watchdog. The steps for configuring and starting the watchdog can be found in the TPS6593-Q1 datasheet. Setting the DISABLE_WDOG signal high disables the watchdog timer if this feature needs to be suspended during initial development or is not required in the system.

GPIO_7 of the primary TPS65931211-Q1 PMIC is configured as the MCU error signal monitor, and must be enabled through the ESM_MCU_EN register bit. MCU and Main Domain reset is supported through the connection between the nRSTOUT pin of the PMIC and the MCU_PORz pin of the processor.

An option exists to use the EN_DRV to indicate an error and that the system is entering SAFE state. Use this signal if the system has external circuitry that needs to be driven by an error event. In this PDN, the EN_DRV is not utilized but is available.

The current monitoring is enabled by default for all BUCKs and LDOs.

Table 4-1. PMIC System Level Safety Features

ASIL-B				
External SW Wdog	INTn	Safety MCU Processing ESM Safety MCU Reset	Safety Status Signal with IO Read-Back feature	System Input Voltage Monitoring
PMIC: Q&A Watchdog and I2C2.	PMIC: nINT pin connected to EXTINTn on the processor	PMIC: nERR_MCU connected to MCU_ERRORn on the processor	PMIC: ENDRV	VCCA OV/UV is disabled by default but can be enabled by I2C.

Table 4-2. PMIC Power Monitoring Safety Features

Device	Power Resource	PDN Power Rail	ASIL-B Supply Voltage Monitoring
TPS65931211-Q1 (PMIC)	BUCK1-3	VDD_CORE	PMIC - OV and UV
	BUCK4	VDDS_DDR	PMIC - OV and UV
	BUCK5	DVDD1V8(VDDSHVy)	PMIC - OV and UV
	LDO1	VDDSHV5	PMIC - OV and UV check with mike if UV/OV are monitored when LDO is configured as bypass
	LDO2	VPP (eFUSE)	PMIC - OV and UV
	LDO3	VDDR_CORE	PMIC - OV and UV
	LDO4	VDDA_MCU	PMIC - OV and UV
TPS22965-Q1	Load Switch	DVDD3V3 (VDDSHVx)	PMIC (FB_B3) - OV and UV

Note

Refer to the Safety Manual of the TPS6593-Q1 device for full descriptions and analysis of the PMIC functional safety features. These functional safety features can assist in achieving up to ASIL-B rating for a system.

5 Static NVM Settings

The TPS6593-Q1 PMIC consist of user register space and an NVM. The settings in NVM, which are loaded into the user registers during the transition from INIT to BOOT BIST, are provided in this section. Note: The user registers can be changed during state transitions, such as moving from STANDBY to ACTIVE mode. The user register map is described in the [TPS6593-Q1 Datasheet](#).

5.1 Application-Based Configuration Settings

In the TPS6593-Q1 datasheet, there are seven application-based configurations for each BUCK to operate within. The following list includes the different configurations available:

- 2.2MHz single phase for DDR termination
- 4.4MHz VOUT less than 1.9V, multiphase or high COUT single phase
- 4.4MHz VOUT less than 1.9V, low COUT, single phase only
- 4.4MHz VOUT Greater than 1.7V, single phase only
- 2.2MHz VOUT less than 1.9V multiphase or single phase
- 2.2MHz Full VOUT range and VIN Greater than 4.5V, single phase only
- 2.2MHz Full VOUT and full VIN Range, single phase only

The seven configurations also have output inductance values that optimize the performance of each buck under these various conditions. [Table 5-1](#) shows the default configurations for the BUCKs. These settings cannot be changed after device startup.

Table 5-1. Application Use Case Settings

Device	BUCK Rail	Default Application Use Case	Recommended Inductor Value
TPS65931211-Q1	BUCK1	2.2MHz VOUT less than 1.9V multiphase or single phase	470nH
	BUCK2	2.2MHz VOUT less than 1.9V multiphase or single phase	470nH
	BUCK3	2.2MHz VOUT less than 1.9V multiphase or single phase	470nH
	BUCK4	2.2MHz VOUT less than 1.9V multiphase or single phase	470nH
	BUCK5	2.2MHz VOUT less than 1.9V multiphase or single phase	470nH

5.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup.

Table 5-2. Device Identification NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
DEV_REV	DEVICE_ID		
NVM_CODE_1	TI_NVM_ID	0x11	
NVM_CODE_2	TI_NVM_REV	0x5	
PHASE_CONFIG	MP_CONFIG	0x3	3+1+1

5.3 BUCK Settings

These settings detail the voltages, configurations, and monitoring of the BUCK rails stored in the NVM. All these settings can be changed though I²C after startup. Some settings, typically the enable bits, are also changed by the PFSM, as described in [Section 6.3](#).

Table 5-3. BUCK NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
BUCK1_CTRL	BUCK1_EN	0x0	Disabled; BUCK1 regulator
	BUCK1_FPWM	0x1	PWM operation only.
	BUCK1_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK1_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK1_VSEL	0x0	BUCK1_VOUT_1
	BUCK1_PLDN	0x1	Enabled; Pull-down resistor
	BUCK1_RV_SEL	0x0	Disabled
BUCK1_CONF	BUCK1_SLEW_RATE	0x3	5.0mV/μs
	BUCK1_ILIM	0x5	5.5A
BUCK2_CTRL	BUCK2_EN	0x0	Disabled; BUCK2 regulator
	BUCK2_FPWM	0x1	PWM operation only.
	BUCK2_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK2_VSEL	0x0	BUCK2_VOUT_1
	BUCK2_PLDN	0x1	Enabled; Pull-down resistor
	BUCK2_RV_SEL	0x0	Disabled
BUCK2_CONF	BUCK2_SLEW_RATE	0x3	5.0mV/μs
	BUCK2_ILIM	0x5	5.5A
BUCK3_CTRL	BUCK3_EN	0x0	Disabled; BUCK3 regulator
	BUCK3_FPWM	0x1	PWM operation only.
	BUCK3_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK3_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK3_VSEL	0x0	BUCK3_VOUT_1
	BUCK3_PLDN	0x1	Enabled; Pull-down resistor
	BUCK3_RV_SEL	0x0	Disabled
BUCK3_CONF	BUCK3_SLEW_RATE	0x0	33mV/μs
	BUCK3_ILIM	0x5	5.5A

Table 5-3. BUCK NVM Settings (continued)

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
BUCK4_CTRL	BUCK4_EN	0x0	Disabled; BUCK4 regulator
	BUCK4_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK4_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK4_VSEL	0x0	BUCK4_VOUT_1
	BUCK4_PLDN	0x1	Enabled; Pull-down resistor
	BUCK4_RV_SEL	0x0	Disabled
BUCK4_CONF	BUCK4_SLEW_RATE	0x3	5.0mV/μs
	BUCK4_ILIM	0x5	5.5A
BUCK5_CTRL	BUCK5_EN	0x0	Disabled; BUCK5 regulator
	BUCK5_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK5_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK5_VSEL	0x0	BUCK5_VOUT_1
	BUCK5_PLDN	0x1	Enable Pull-down resistor
	BUCK5_RV_SEL	0x0	Disabled
BUCK5_CONF	BUCK5_SLEW_RATE	0x3	5.0mV/μs
	BUCK5_ILIM	0x3	3.5A
BUCK1_VOUT_1	BUCK1_VSET1	0x2d	0.750V
BUCK1_VOUT_2	BUCK1_VSET2	0x2d	0.750V
BUCK2_VOUT_1	BUCK2_VSET1	0x2d	0.750V
BUCK2_VOUT_2	BUCK2_VSET2	0x2d	0.750V
BUCK3_VOUT_1	BUCK3_VSET1	0xfd	3.30V
BUCK3_VOUT_2	BUCK3_VSET2	0xfd	3.30V
BUCK4_VOUT_1	BUCK4_VSET1	0x73	1.10V
BUCK4_VOUT_2	BUCK4_VSET2	0x73	1.10V
BUCK5_VOUT_1	BUCK5_VSET1	0xb2	1.80V
BUCK5_VOUT_2	BUCK5_VSET2	0xb2	1.80V
BUCK1_PG_WINDOW	BUCK1_OV_THR	0x3	+5% / +50mV
	BUCK1_UV_THR	0x3	-5% / -50mV
BUCK2_PG_WINDOW	BUCK2_OV_THR	0x3	+5% / +50mV
	BUCK2_UV_THR	0x3	-5% / -50mV
BUCK3_PG_WINDOW	BUCK3_OV_THR	0x3	+5% / +50mV
	BUCK3_UV_THR	0x3	-5% / -50mV
BUCK4_PG_WINDOW	BUCK4_OV_THR	0x4	+6% / +60mV
	BUCK4_UV_THR	0x4	-6% / -60mV
BUCK5_PG_WINDOW	BUCK5_OV_THR	0x4	+6% / +60mV
	BUCK5_UV_THR	0x4	-6% / -60mV

5.4 LDO Settings

These settings detail the voltages, configurations, and monitoring of the LDO rails stored in the NVM. All these settings can be changed through I²C after startup. Some settings, typically the enable bits, are also changed by the PFSM, as described in [Section 6.3](#).

After the [Section 6.3.4](#) sequence has completed, the LDOx_EN and LDOx_VMON_EN bits are set and the LDOx_RV_SEL bit is cleared for all LDOs. The other bits remain unchanged, but are still accessible via I²C.

Table 5-4. LDO NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
LDO1_CTRL	LDO1_EN	0x0	Disabled; LDO1 regulator.
	LDO1_SLOW_RAMP	0x1	3mV/μs max ramp up slew rate for LDO output from 0.3V to 90% of LDO _{on} _VSET
	LDO1_PLDN	0x1	125Ω
	LDO1_VMON_EN	0x0	Disable OV and UV comparators.
	LDO1_RV_SEL	0x0	Disabled
LDO2_CTRL	LDO2_EN	0x0	Disabled; LDO2 regulator.
	LDO2_SLOW_RAMP	0x1	3mV/μs max ramp up slew rate for LDO output from 0.3V to 90% of LDO _{on} _VSET
	LDO2_PLDN	0x0	50kΩ
	LDO2_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO2_RV_SEL	0x0	Disabled
LDO3_CTRL	LDO3_EN	0x0	Disabled; LDO3 regulator.
	LDO3_SLOW_RAMP	0x1	3mV/μs max ramp up slew rate for LDO output from 0.3V to 90% of LDO _{on} _VSET
	LDO3_PLDN	0x1	125Ω
	LDO3_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO3_RV_SEL	0x0	Disabled
LDO4_CTRL	LDO4_EN	0x0	Disabled; LDO4 regulator.
	LDO4_SLOW_RAMP	0x1	3mV/μs max ramp up slew rate for LDO output from 0.3V to 90% of LDO _{on} _VSET
	LDO4_PLDN	0x1	125Ω
	LDO4_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO4_RV_SEL	0x0	Disabled
LDO1_VOUT	LDO1_VSET	0x3a	3.30V
	LDO1_BYPASS	0x1	Bypass mode.
LDO2_VOUT	LDO2_VSET	0x1c	1.80V
	LDO2_BYPASS	0x0	Linear regulator mode.
LDO3_VOUT	LDO3_VSET	0x9	0.85V
	LDO3_BYPASS	0x0	Linear regulator mode.
LDO4_VOUT	LDO4_VSET	0x38	1.800V
LDO1_PG_WINDOW	LDO1_OV_THR	0x4	+6% / +60mV
	LDO1_UV_THR	0x4	-6% / -60mV
LDO2_PG_WINDOW	LDO2_OV_THR	0x4	+6% / +60mV
	LDO2_UV_THR	0x4	-6% / -60mV
LDO3_PG_WINDOW	LDO3_OV_THR	0x4	+6% / +60mV
	LDO3_UV_THR	0x4	-6% / -60mV
LDO4_PG_WINDOW	LDO4_OV_THR	0x4	+6% / +60mV
	LDO4_UV_THR	0x4	-6% / -60mV

5.5 VCCA Settings

These settings detail the default monitoring enabled on VCCA. All these settings can be changed through I²C after startup.

Table 5-5. VCCA NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
VCCA_VMON_CTRL	VMON_DEGLITCH_SEL	0x1	20µs
	VCCA_VMON_EN	0x0	Disabled; OV and UV comparators.
VCCA_PG_WINDOW	VCCA_OV_THR	0x7	+10%
	VCCA_UV_THR	0x7	-10%
	VCCA_PG_SET	0x1	5.0V
GENERAL_REG_1	FAST_VCCA_OVP	0x0	Slow, 4µs deglitch filter enabled
GENERAL_REG_3	LPM_EN_DISABLES_VCCA_VMON	0x1	VCCA_VMON enabled if VCCA_VMON_EN=1 and LPM_EN=0

5.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. Note that the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the *Digital Signal Descriptions* section in TPS6593-Q1 datasheet.

Table 5-6. GPIO NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
GPIO1_CONF	GPIO1_OD	0x0	Push-pull output
	GPIO1_DIR	0x0	Input
	GPIO1_SEL	0x1	SCL_I2C2/CS_SPI
	GPIO1_PU_SEL	0x0	Pull-down resistor selected
	GPIO1_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO1_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO2_CONF	GPIO2_OD	0x0	Push-pull output
	GPIO2_DIR	0x0	Input
	GPIO2_SEL	0x2	SDA_I2C2/SDO_SPI
	GPIO2_PU_SEL	0x0	Pull-down resistor selected
	GPIO2_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO2_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO3_CONF	GPIO3_OD	0x1	Open-drain output
	GPIO3_DIR	0x0	Input
	GPIO3_SEL	0x5	NSLEEP2
	GPIO3_PU_SEL	0x0	Pull-down resistor selected
	GPIO3_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO3_DEGLITCH_EN	0x1	8µs deglitch time.
GPIO4_CONF	GPIO4_OD	0x0	Push-pull output
	GPIO4_DIR	0x1	Output
	GPIO4_SEL	0x0	GPIO4
	GPIO4_PU_SEL	0x0	Pull-down resistor selected
	GPIO4_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO4_DEGLITCH_EN	0x0	No deglitch, only synchronization.

Table 5-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
GPIO5_CONF	GPIO5_OD	0x1	Open-drain output
	GPIO5_DIR	0x0	Input
	GPIO5_SEL	0x0	GPIO5
	GPIO5_PU_SEL	0x0	Pull-down resistor selected
	GPIO5_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO5_DEGLITCH_EN	0x1	8 μ s deglitch time.
GPIO6_CONF	GPIO6_OD	0x0	Push-pull output
	GPIO6_DIR	0x0	Input
	GPIO6_SEL	0x0	GPIO6
	GPIO6_PU_SEL	0x0	Pull-down resistor selected
	GPIO6_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO6_DEGLITCH_EN	0x1	8 μ s deglitch time.
GPIO7_CONF	GPIO7_OD	0x1	Open-drain output
	GPIO7_DIR	0x0	Input
	GPIO7_SEL	0x1	NERR_MCU
	GPIO7_PU_SEL	0x0	Pull-down resistor selected
	GPIO7_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO7_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO8_CONF	GPIO8_OD	0x1	Open-drain output
	GPIO8_DIR	0x0	Input
	GPIO8_SEL	0x3	DISABLE_WDOG
	GPIO8_PU_SEL	0x0	Pull-down resistor selected
	GPIO8_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO8_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO9_CONF	GPIO9_OD	0x1	Open-drain output
	GPIO9_DIR	0x0	Input
	GPIO9_SEL	0x0	GPIO9
	GPIO9_PU_SEL	0x0	Pull-down resistor selected
	GPIO9_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO9_DEGLITCH_EN	0x1	8 μ s deglitch time.
GPIO10_CONF	GPIO10_OD	0x1	Open-drain output
	GPIO10_DIR	0x0	Input
	GPIO10_SEL	0x0	GPIO10
	GPIO10_PU_SEL	0x0	Pull-down resistor selected
	GPIO10_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO10_DEGLITCH_EN	0x1	8 μ s deglitch time.
GPIO11_CONF	GPIO11_OD	0x1	Open-drain output
	GPIO11_DIR	0x0	Input
	GPIO11_SEL	0x0	GPIO11
	GPIO11_PU_SEL	0x0	Pull-down resistor selected
	GPIO11_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO11_DEGLITCH_EN	0x1	8 μ s deglitch time.

Table 5-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
NPWRON_CONF	NPWRON_SEL	0x0	ENABLE
	ENABLE_PU_SEL	0x0	Pull-down resistor selected
	ENABLE_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	ENABLE_DEGLITCH_EN	0x1	8 μ s deglitch time when ENABLE, 50ms deglitch time when NPWRON.
	ENABLE_POL	0x0	Active high
	NRSTOUT_OD	0x1	Open-drain output
GPIO_OUT_1	GPIO1_OUT	0x0	Low
	GPIO2_OUT	0x0	Low
	GPIO3_OUT	0x0	Low
	GPIO4_OUT	0x0	Low
	GPIO5_OUT	0x0	Low
	GPIO6_OUT	0x0	Low
	GPIO7_OUT	0x0	Low
	GPIO8_OUT	0x0	Low
GPIO_OUT_2	GPIO9_OUT	0x0	Low
	GPIO10_OUT	0x0	Low
	GPIO11_OUT	0x0	Low

5.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed through I²C after startup.

Table 5-7. FSM NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
RAIL_SEL_1	BUCK1_GRP_SEL	0x1	MCU rail group
	BUCK2_GRP_SEL	0x1	MCU rail group
	BUCK3_GRP_SEL	0x1	MCU rail group
	BUCK4_GRP_SEL	0x1	MCU rail group
RAIL_SEL_2	BUCK5_GRP_SEL	0x1	MCU rail group
	LDO1_GRP_SEL	0x1	MCU rail group
	LDO2_GRP_SEL	0x3	OTHER rail group
	LDO3_GRP_SEL	0x1	MCU rail group
RAIL_SEL_3	LDO4_GRP_SEL	0x1	MCU rail group
	VCCA_GRP_SEL	0x0	No group assigned
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	0x1	Orderly shutdown
	SOC_RAIL_TRIG	0x3	SOC power error
	OTHER_RAIL_TRIG	0x2	MCU power error
	SEVERE_ERR_TRIG	0x0	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	0x1	Orderly shutdown

5.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed through I²C after startup.

Table 5-8. Interrupt NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	0x1	Masked
	GPIO1_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO2_FSM_MASK	0x1	Masked
	GPIO2_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO3_FSM_MASK	0x1	Masked
	GPIO3_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO4_FSM_MASK	0x1	Masked
	GPIO4_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	0x0	Not masked
	GPIO5_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO6_FSM_MASK	0x0	Not masked
	GPIO6_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO7_FSM_MASK	0x1	Masked
	GPIO7_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO8_FSM_MASK	0x1	Masked
	GPIO8_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'

Table 5-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	0x0	Not masked
	GPIO9_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO10_FSM_MASK	0x0	Not masked
	GPIO10_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO11_FSM_MASK	0x0	Not masked
	GPIO11_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
MASK_BUCK1_2	BUCK1_ILIM_MASK	0x0	Interrupt generated
	BUCK1_OV_MASK	0x0	Interrupt generated
	BUCK1_UV_MASK	0x0	Interrupt generated
	BUCK2_ILIM_MASK	0x0	Interrupt generated
	BUCK2_OV_MASK	0x0	Interrupt generated
	BUCK2_UV_MASK	0x0	Interrupt generated
MASK_BUCK3_4	BUCK3_ILIM_MASK	0x0	Interrupt generated
	BUCK3_OV_MASK	0x0	Interrupt generated
	BUCK3_UV_MASK	0x0	Interrupt generated
	BUCK4_OV_MASK	0x0	Interrupt generated
	BUCK4_UV_MASK	0x0	Interrupt generated
	BUCK4_ILIM_MASK	0x0	Interrupt generated
MASK_BUCK5	BUCK5_ILIM_MASK	0x0	Interrupt generated
	BUCK5_OV_MASK	0x0	Interrupt generated
	BUCK5_UV_MASK	0x0	Interrupt generated
MASK_LDO1_2	LDO1_OV_MASK	0x0	Interrupt generated
	LDO1_UV_MASK	0x0	Interrupt generated
	LDO2_OV_MASK	0x0	Interrupt generated
	LDO2_UV_MASK	0x0	Interrupt generated
	LDO1_ILIM_MASK	0x0	Interrupt generated
	LDO2_ILIM_MASK	0x0	Interrupt generated
MASK_LDO3_4	LDO3_OV_MASK	0x0	Interrupt generated
	LDO3_UV_MASK	0x0	Interrupt generated
	LDO4_OV_MASK	0x0	Interrupt generated
	LDO4_UV_MASK	0x0	Interrupt generated
	LDO3_ILIM_MASK	0x0	Interrupt generated
	LDO4_ILIM_MASK	0x0	Interrupt generated
MASK_VMON	VCCA_OV_MASK	0x0	Interrupt generated
	VCCA_UV_MASK	0x0	Interrupt generated
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	0x1	Interrupt not generated.
	GPIO2_FALL_MASK	0x1	Interrupt not generated.
	GPIO3_FALL_MASK	0x1	Interrupt not generated.
	GPIO4_FALL_MASK	0x1	Interrupt not generated.
	GPIO5_FALL_MASK	0x1	Interrupt not generated.
	GPIO6_FALL_MASK	0x1	Interrupt not generated.
	GPIO7_FALL_MASK	0x1	Interrupt not generated.
	GPIO8_FALL_MASK	0x1	Interrupt not generated.

Table 5-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	0x1	Interrupt not generated.
	GPIO2_RISE_MASK	0x1	Interrupt not generated.
	GPIO3_RISE_MASK	0x1	Interrupt not generated.
	GPIO4_RISE_MASK	0x1	Interrupt not generated.
	GPIO5_RISE_MASK	0x1	Interrupt not generated.
	GPIO6_RISE_MASK	0x1	Interrupt not generated.
	GPIO7_RISE_MASK	0x1	Interrupt not generated.
	GPIO8_RISE_MASK	0x1	Interrupt not generated.
MASK_GPIO9_11 / MASK_GPIO9_10	GPIO9_FALL_MASK	0x1	Interrupt not generated.
	GPIO9_RISE_MASK	0x1	Interrupt not generated.
	GPIO10_FALL_MASK	0x1	Interrupt not generated.
	GPIO11_FALL_MASK	0x1	Interrupt not generated.
	GPIO10_RISE_MASK	0x1	Interrupt not generated.
	GPIO11_RISE_MASK	0x1	Interrupt not generated.
MASK_STARTUP	NPWRON_START_MASK	0x1	Interrupt not generated.
	ENABLE_MASK	0x0	Interrupt generated
	FSD_MASK	0x1	Interrupt not generated.
	SOFT_REBOOT_MASK	0x0	Interrupt generated
MASK_MISC	TWARN_MASK	0x0	Interrupt generated
	BIST_PASS_MASK	0x0	Interrupt generated
	EXT_CLK_MASK	0x1	Interrupt not generated.
MASK_MODERATE_ERR	BIST_FAIL_MASK	0x0	Interrupt generated
	REG_CRC_ERR_MASK	0x0	Interrupt generated
	SPMI_ERR_MASK	0x1	Interrupt not generated.
	NPWRON_LONG_MASK	0x1	Interrupt not generated.
	NINT_READBACK_MASK	0x0	Interrupt generated
	NRSTOUT_READBACK_MASK	0x0	Interrupt generated
MASK_FSM_ERR	IMM_SHUTDOWN_MASK	0x0	Interrupt generated
	MCU_PWR_ERR_MASK	0x0	Interrupt generated
	SOC_PWR_ERR_MASK	0x0	Interrupt generated
	ORD_SHUTDOWN_MASK	0x0	Interrupt generated
MASK_COMM_ERR	COMM_FRM_ERR_MASK	0x1	Interrupt not generated.
	COMM_CRC_ERR_MASK	0x0	Interrupt generated
	COMM_ADR_ERR_MASK	0x0	Interrupt generated
	I2C2_CRC_ERR_MASK	0x0	Interrupt generated
	I2C2_ADR_ERR_MASK	0x0	Interrupt generated
MASK_READBACK_ERR	EN_DRV_READBACK_MASK	0x0	Interrupt generated
	NRSTOUT_SOC_READBACK_MASK	0x1	Interrupt not generated.
MASK_ESM	ESM_SOC_PIN_MASK	0x1	Interrupt not generated.
	ESM_SOC_RST_MASK	0x1	Interrupt not generated.
	ESM_SOC_FAIL_MASK	0x1	Interrupt not generated.
	ESM_MCU_PIN_MASK	0x0	Interrupt generated
	ESM_MCU_RST_MASK	0x0	Interrupt generated
	ESM_MCU_FAIL_MASK	0x0	Interrupt generated
GENERAL_REG_1	PFSM_ERR_MASK	0x0	Interrupt generated

5.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though I²C after startup.

Table 5-9. POWERGOOD NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
PGOOD_SEL_1	PGOOD_SEL_BUCK1	0x1	Voltage only
	PGOOD_SEL_BUCK2	0x1	Voltage only
	PGOOD_SEL_BUCK3	0x1	Voltage only
	PGOOD_SEL_BUCK4	0x1	Voltage only
PGOOD_SEL_2	PGOOD_SEL_BUCK5	0x1	Voltage only
PGOOD_SEL_3	PGOOD_SEL_LDO1	0x1	Voltage only
	PGOOD_SEL_LDO2	0x1	Voltage only
	PGOOD_SEL_LDO3	0x1	Voltage only
	PGOOD_SEL_LDO4	0x1	Voltage only
PGOOD_SEL_4	PGOOD_SEL_VCCA	0x1	VCCA OV/UV threshold affecting PGOOD signal
	PGOOD_SEL_TDIE_WARN	0x1	Thermal warning affecting to PGOOD signal
	PGOOD_SEL_NRSTOUT	0x1	nRSTOUT pin low state forces PGOOD signal to low
	PGOOD_SEL_NRSTOUT_SOC	0x0	Masked
	PGOOD_POL	0x0	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	0x1	Both undervoltage and overvoltage are monitored

5.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, BUCK frequency, and LDO timeout. All these settings can be changed though I²C after startup.

Table 5-10. Miscellaneous NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
PLL_CTRL	EXT_CLK_FREQ	0x0	1.1MHz
CONFIG_1	TWARN_LEVEL	0x1	140C
	I2C1_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode primary code.
	I2C2_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode primary code.
	EN_ILIM_FSM_CTRL	0x0	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.
	NSLEEP1_MASK	0x1	NSLEEP1(B) does not affect FSM state transitions.
	NSLEEP2_MASK	0x0	NSLEEP2(B) affects FSM state transitions.
CONFIG_2	BB_CHARGER_EN	0x0	Disabled
	BB_VEOC	0x0	2.5V
	BB_ICHR	0x0	100uA
RECOV_CNT_REG_2	RECOV_CNT_THR	0xf	0xf

Table 5-10. Miscellaneous NVM Settings (continued)

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
BUCK_RESET_REG	BUCK1_RESET	0x0	0x0
	BUCK2_RESET	0x0	0x0
	BUCK3_RESET	0x0	0x0
	BUCK4_RESET	0x0	0x0
	BUCK5_RESET	0x0	0x0
SPREAD_SPECTRUM_1	SS_EN	0x0	Spread spectrum disabled
	SS_MODE	0x1	Mixed dwell
	SS_DEPTH	0x0	No modulation
SPREAD_SPECTRUM_2	SS_PARAM1	0x7	0x7
	SS_PARAM2	0xc	0xc
FREQ_SEL	BUCK1_FREQ_SEL	0x0	2.2MHz
	BUCK2_FREQ_SEL	0x0	2.2MHz
	BUCK3_FREQ_SEL	0x0	2.2MHz
	BUCK4_FREQ_SEL	0x0	2.2MHz
	BUCK5_FREQ_SEL	0x0	2.2MHz
FSM_STEP_SIZE	PFSM_DELAY_STEP	0xb	0xb
LDO_RV_TIMEOUT_REG_1	LDO1_RV_TIMEOUT	0xf	16ms
	LDO2_RV_TIMEOUT	0xf	16ms
LDO_RV_TIMEOUT_REG_2	LDO3_RV_TIMEOUT	0xf	16ms
	LDO4_RV_TIMEOUT	0xf	16ms
USER_SPARE_REGS	USER_SPARE_1	0x0	0x0
	USER_SPARE_2	0x0	0x0
	USER_SPARE_3	0x0	0x0
	USER_SPARE_4	0x0	0x0
ESM_MCU_MODE_CFG	ESM_MCU_EN	0x0	ESM_MCU disabled.
ESM_SOC_MODE_CFG	ESM_SOC_EN	0x0	ESM_SoC disabled.
CUSTOMER_NVM_ID_REG	CUSTOMER_NVM_ID	0x0	0x0
RTC_CTRL_2	XTAL_EN	0x0	Crystal oscillator is disabled
	LP_STANDBY_SEL	0x0	LDOINT is enabled in standby state.
	FAST_BIST	0x0	Logic and analog BIST is run at BOOT BIST.
	STARTUP_DEST	0x3	ACTIVE
	XTAL_SEL	0x0	6pF
PFSM_DELAY_REG_1	PFSM_DELAY1	0x0	0x0
PFSM_DELAY_REG_2	PFSM_DELAY2	0x0	0x0
PFSM_DELAY_REG_3	PFSM_DELAY3	0x0	0x0
PFSM_DELAY_REG_4	PFSM_DELAY4	0x0	0x0
GENERAL_REG_0	FAST_BOOT_BIST	0x0	LBIST is run during boot BIST
GENERAL_REG_1	REG_CRC_EN	0x0	Register CRC disabled

5.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings cannot be changed after device startup.

Table 5-11. Interface NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
SERIAL_IF_CONFIG	I2C_SPI_SEL	0x0	I2C
	I2C1_SPI_CRC_EN	0x0	CRC disabled
	I2C2_CRC_EN	0x0	CRC disabled
I2C1_ID_REG	I2C1_ID	0x48	0x48
I2C2_ID_REG	I2C2_ID	0x12	0x12

5.12 Watchdog Settings

These settings detail the default watchdog addresses. These settings can be changed though I²C after startup.

Table 5-12. Watchdog NVM Settings

Register Name	Field Name	TPS65931211-Q1	
		Value	Description
WD_LONGWIN_CFG	WD_LONGWIN	0xff	0xff
WD_THR_CFG	WD_EN	0x1	Watchdog enabled.

6 Pre-Configurable Finite State Machine (PFM) Settings

This section describes the default PFM settings of the TPS65931211-Q1 devices. These settings cannot be changed after device startup.

6.1 Configured States

In this PDN, the PMIC have the following configured power states:

- PFM_START
- wait4Enable
- Active (Active SoC)
- S2R (IO + DDR)
- Standby (Partial IO, PMIC OFF)
- TO_SAFE

[Figure 6-1](#) shows the configured PDN power states along with the transition conditions to move between the states. Additionally, the transitions to hardware states, such as SAFE RECOVERY and LP_STANDBY are shown. The hardware states are part of the fixed device power Finite State Machine (FSM) and described in the [TPS6593-Q1 datasheet](#).

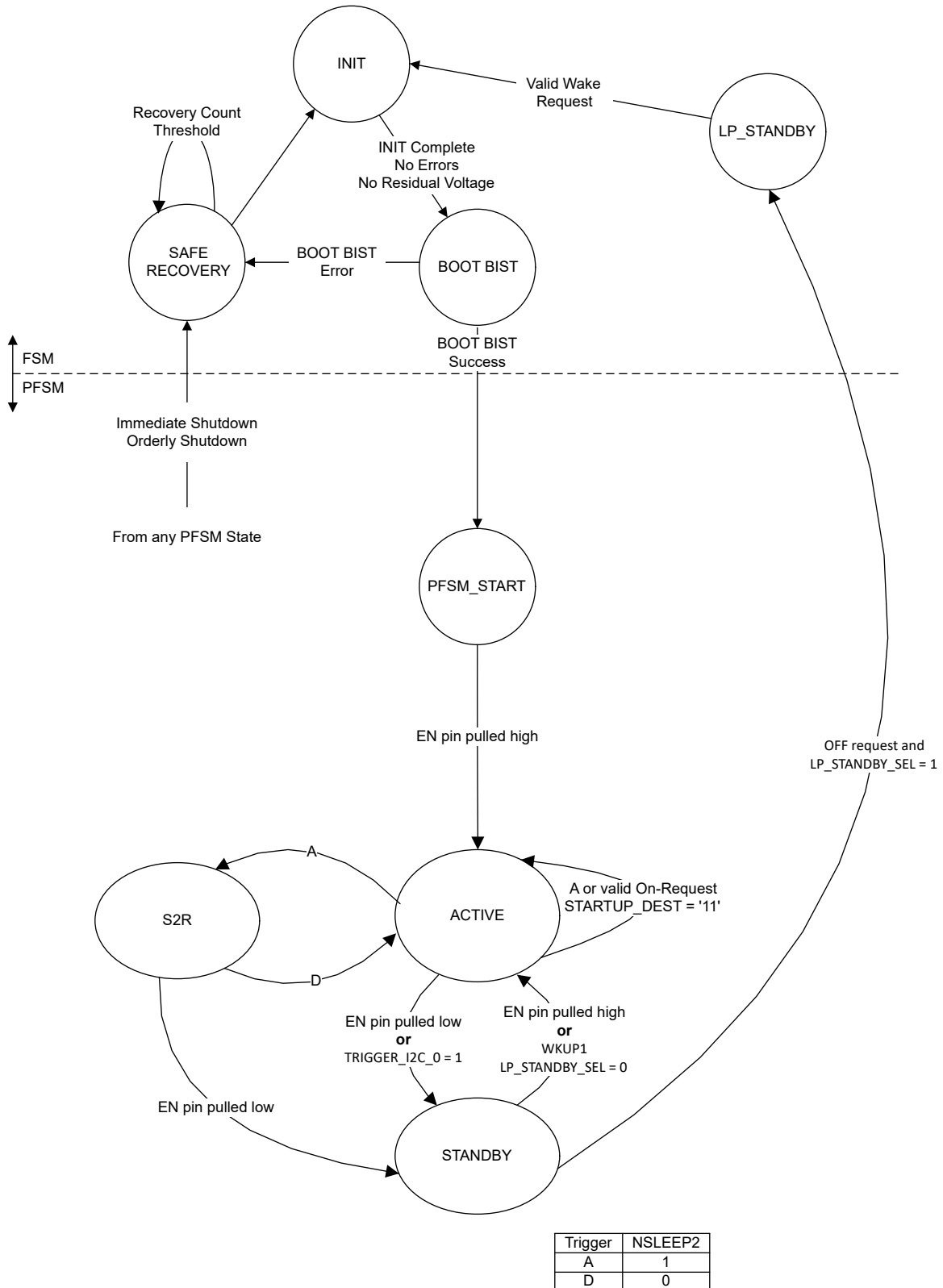


Figure 6-1. Pre-configurable Finite State Machine (PFSM) Mission States and Transitions

When the PMIC transition from the FSM to the PFSM, the PMIC waits for a valid ON Request before entering the ACTIVE state. The definition for each power state is described below:

- PFSM_START** PFSM_START is the first state of the pre-configurable mission states. In this state the PMIC is powered by a valid supply. This state is entered when PMIC transitions from the FSM into PFSM. Once the PMIC arrives the PFSM_START, the PMIC waits for a valid ON request before transitioning to the next state.
- ACTIVE** The PMIC is powered by a valid supply. The PMIC is fully functional and supply power to all PDN loads. The processor has completed a recommended power up sequence with all voltage domains energized. Refer to the [Section 6.3.4](#) sequence description.
- S2R** The PMIC is powered by a valid supply. When the GPIO3 (nSLEEP2) is pulled low, only the power resources assigned to the 1.8V IO domain (Buck5) and the DDR (Buck4) are energized while all other domains are OFF to minimize total system power. EN_DRV is forced low in this state. This state supports the IO+DDR (suspend to RAM) low power mode on the AM62A.
- STANDBY** The PMIC is powered by a valid supply on the system power rail ($VCCA > VCCA_{UV}$). All device resources are powered down in the STANDBY state. EN_DRV is forced low in this state. The processor is in the Off state, no voltage domains are energized. Refer to the [Section 6.3.2](#) sequence description.
- TO_SAFE** If there is an event which causes MODERATE_ERR_INT = '1' or severe error from any of the previous described states, PMIC executes a orderly or immediate sequence and transitions out of the PFSM onto the FSM. MCU power errors and moderate errors result in the orderly shutdown trigger. Severe errors result in the immediate shutdown trigger.

6.2 PFSM Triggers

There are various triggers that can enable a state transition between configured states. [Table 6-1](#) describes each trigger and the associated state transition from highest priority (Immediate Shutdown) to lowest priority. Active triggers of higher priority block triggers of lower priority and the associated sequence.

Table 6-1. State Transition Triggers

Trigger	Priority (ID)	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
Immediate Shutdown	0	True	False	ANY	TO_SAFE	immediateOff2Safe_pd
Orderly Shutdown	1	True	False	ANY	TO_SAFE	orderlyOff2safe
1 = High (Always True)	2	False	False	STANDBY	LP STANDBY	enterLPstandby
FORCE_STANDBY	3	False	False	ACTIVE, STANDBY, S2R	STANDBY	orderlyOff
WD_ERROR	4	False	True	ACTIVE	ACTIVE	warmReset
ESM MCU Error	5	False	True	ACTIVE	ACTIVE	warmReset
I2C_1	6	False	True	ACTIVE	RUNTIME_BIST	Execute RUNTIME BIST
I2C_2	7	False	True	ACTIVE	ACTIVE	Enable I2C CRC on I2C1 and I2C2
SU_ACTIVE	8	False	False	STANDBY	ACTIVE	any2active
WKUP1	9	False	False	STANDBY, ACTIVE	ACTIVE	any2active
I2C_0	10	False	False	ACTIVE	STANDBY	orderlyOff
I2C_3	11	False	False	ACTIVE	ACTIVE	Device is prepared for OTA NVM update
FORCE_STANDBY = LOW	12	False	False	PFSM_START	ACTIVE	any2active
MCU_POWER_ERROR	13	False	False	ACTIVE	ACTIVE	warmReset
GPIO9 (rise)	14	False	True	ACTIVE	ACTIVE	ENVPP
GPIO9 (fall)	15	False	True	ACTIVE	ACTIVE	DISVPP
GPIO5 (fall)	16	False	True	ACTIVE	ACTIVE	SD_1V8
GPIO5 (rise)	17	False	True	ACTIVE	ACTIVE	SD_3V3
GPIO11 (fall)	18	False	True	ACTIVE	ACTIVE	RST_SDCARD
GPIO11 (rise)	19	False	True	ACTIVE	ACTIVE	EN_SDCARD
A	20	False	False	ACTIVE, S2R	ACTIVE	any2active
D	21	False	False	ACTIVE, S2R	S2R	any2_s2r
1 = High (Always True)	22	True	False	TO_SAFE	SAFE_RECOVER_Y	NA

6.3 Power Sequences

6.3.1 Sequence: *immediateOff2Safe_pd*

The *immediateOff2Safe_pd* sequence occur when transition to the TO_SAFE state. The TPS65931211-Q1 PMIC immediately ceases BUCK switching and enables the pulldown resistors of the BUCKs and LDOs without delay. All rails are immediately shut down to prevent any damage of the PMICs in case of over voltage on VCCA or thermal shutdown. The timing is illustrated in [Figure 6-2](#).

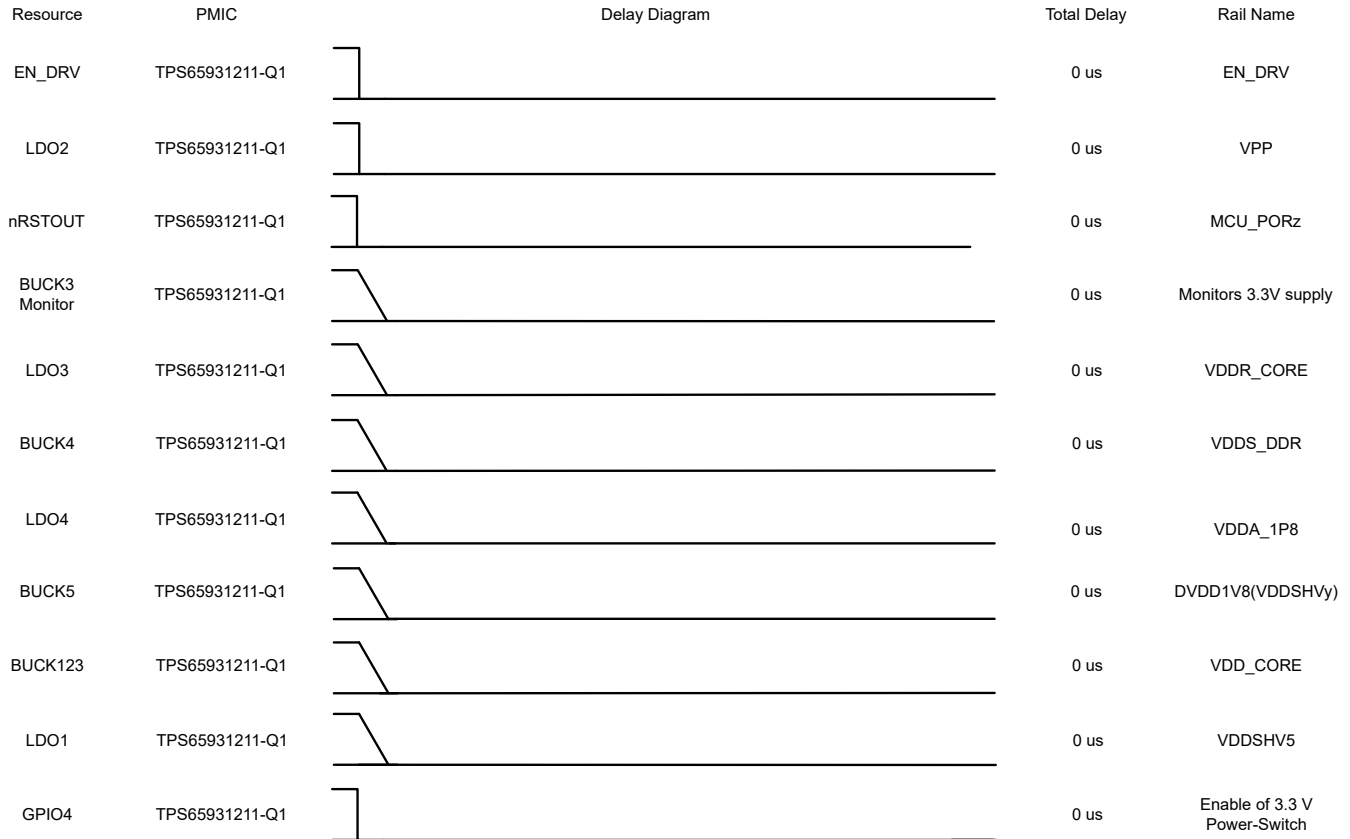


Figure 6-2. ImmediateOff Sequence

6.3.2 Sequence: orderlyOff2safe

If a moderate error occurs, an orderly shutdown trigger is generated. This trigger shuts down the PMIC outputs using the recommended power down sequence and proceed to the TO_SAFE state.

If an OFF request occurs, such as the ENABLE pin of the TPS6593-Q1 device being pulled low, the same power down sequence occurs, except that the PMICs go to STANDBY (LP_STANDBY_SEL=0) or LP_STANDBY (LP_STANDBY_SEL=1) states, rather than going to the TO_SAFE state. The power sequence for both of these events is shown in [Figure 6-3](#).

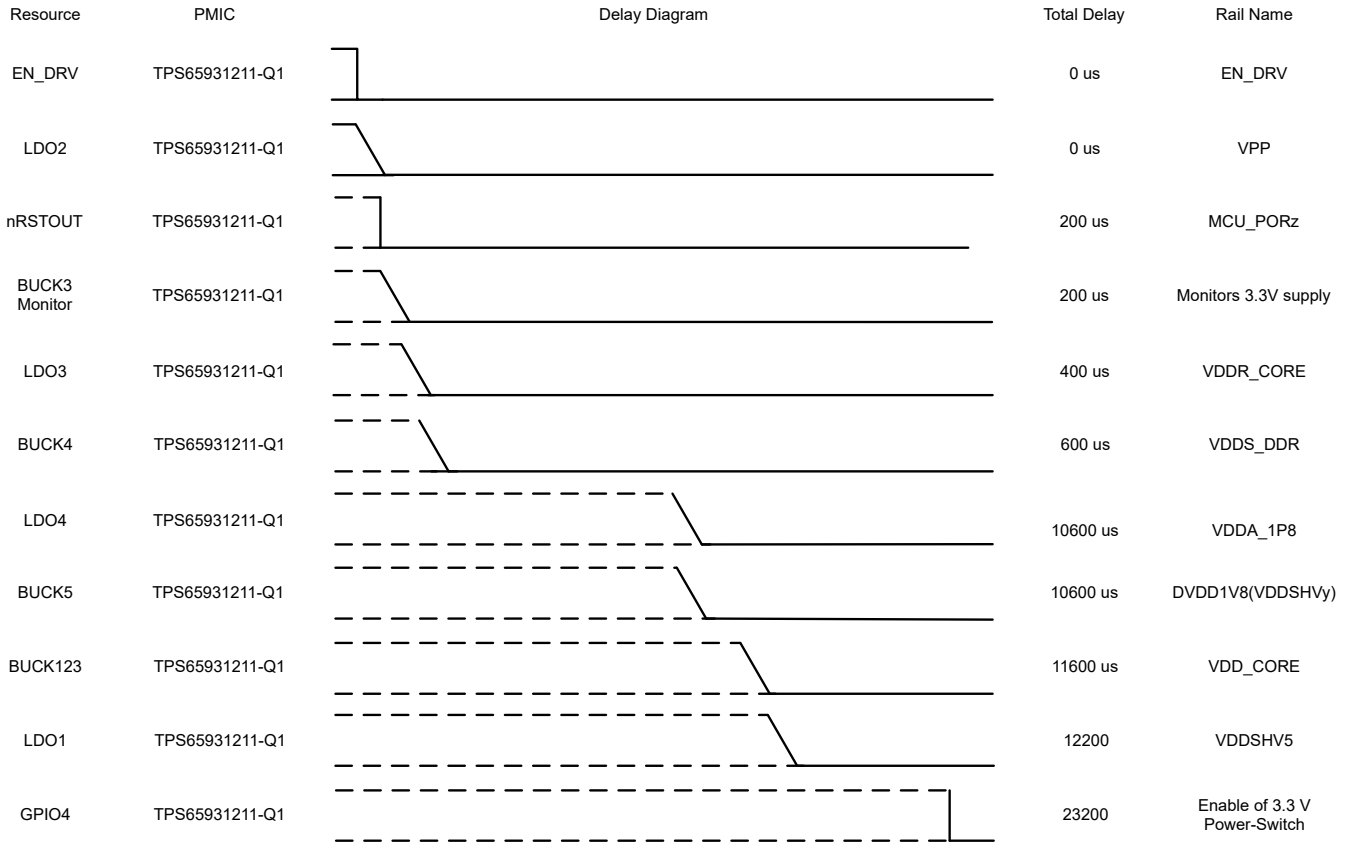


Figure 6-3. OrderlyOff Sequence

6.3.3 Sequence: warmReset

The warmReset sequence can be triggered by either a watchdog, ESM_MCU or MCU_POWER_ERROR. An output failure detection on LDO2 is a valid condition for the MCU_POWER_ERROR trigger which executes a warm reset. An output failure on any of the remaining power resources (Buck1/2/3/4/5 and LDO1/3/4) executes an orderly shutdown. In the event of a warm reset trigger, the nRSTOUT is driven low and the recovery count (register RECOV_CNT_REG_1) increments. Then, all BUCKs and LDOs are reset to the default voltages. The PMICs remain in the ACTIVE state.

At the beginning of the sequence the following instructions are executed:

```

\\ Mask LDO1 UV/OV
REG_WRITE_MASK_IMM ADDR=0x04C DATA=0x03 MASK=0xFC
\\ Set SPMI_LPM_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x10 MASK=0xEF
\\ Set LPM_EN and AMUXOUT_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xEB
// Increment the recovery counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
    
```

Note

The watchdog or ESM error is an indication of a significant error which has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery, however, to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented. If the recovery counter exceeds the recovery count threshold the PMICs stay in the safe recovery state. After the sequence, the MCU is responsible for managing the EN_DRV and recovery counter. At the end of the sequence the 'FORCE_EN_DRV_LOW' bit is cleared so that the MCU can set the ENABLE_DRV bit.

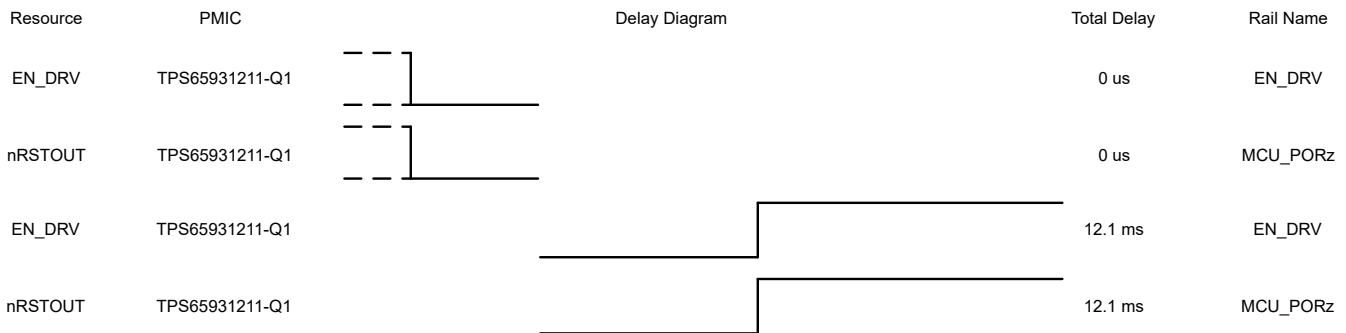


Figure 6-4. Warm reset Sequence

6.3.4 Sequence: any2active

When a trigger causes the any2active sequence to execute, all Buck converters, LDO3 and LDO4 power up in the recommended power up sequence as shown in Figure 6-5. LDO1 can be enabled with a rising edge on GPIO11 after nRSTOUT goes high. LDO2 can be enabled with a rising edge on GPIO9 after nRSTOUT goes high.

At the beginning of the any2active sequence, the PMIC clear SPMI_LP_EN and LPM_EN and set AMUXOUT_EN and CLKMON_EN.

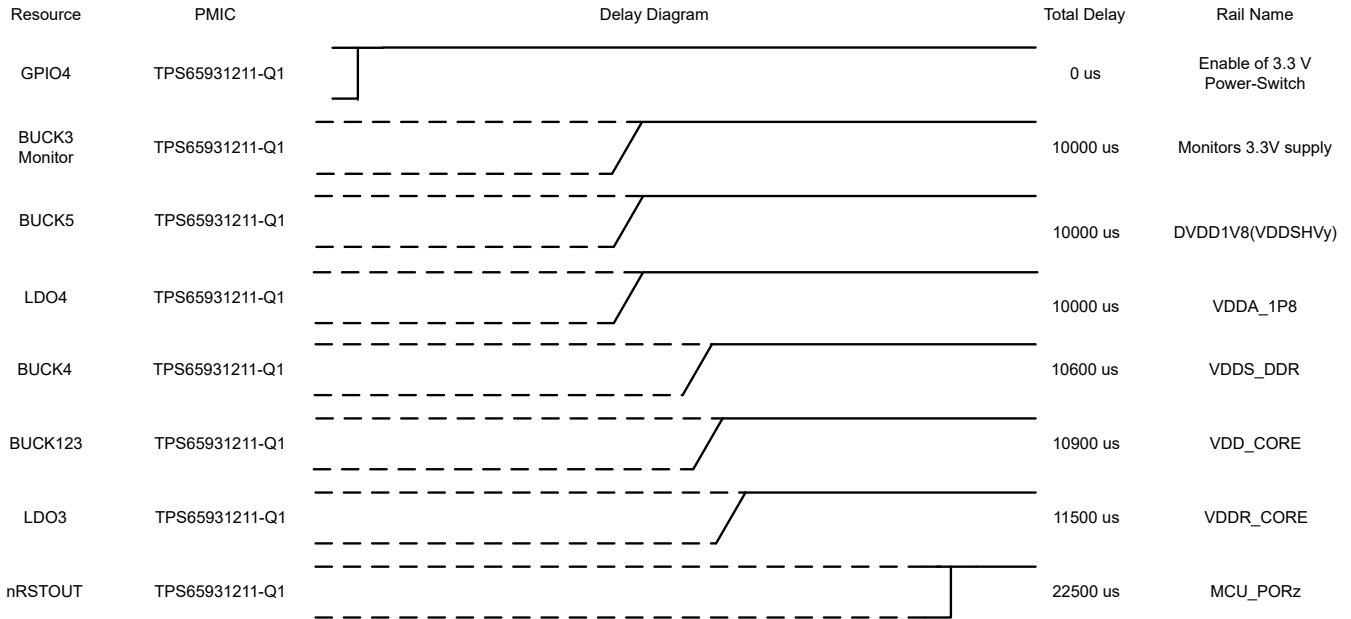


Figure 6-5. any2active Sequence

At the end of the any2active sequence the 'FORCE_EN_DRV_LOW' bit is cleared.

Note

After the any2active sequence the MCU is responsible for managing the EN_DRV.

6.3.5 Sequence: any2_s2r

The D and A triggers, defined by the NSLEEP2 bit or pin, trigger the any2_s2r sequence to support the IO+DDR low power mode on the processor. This sequence disables all power rails except Buck4 and Buck5 which supplies the 1.8V IO domain and DDR rails.

The following PMIC PFSM instructions are executed automatically in the beginning and at the end of the power sequence:

```
//Instructions executed at the beginning of the sequence:
//mask NSLEEP2 pin and NSLEEP2B bit
REG_WRITE_MASK_IMM ADDR=0x07D DATA=0x80 MASK=0x7F
```

```
// Instructions executed at the end of the sequence:
// unmask NSLEEP2 pin and NSLEEP2B bit
REG_WRITE_MASK_IMM ADDR=0x07D DATA=0x00 MASK=0x7F
// set SPMI_LPM_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x10 MASK=0xEF
// Clear AMUXOUT_EN, CLKMON_EN, set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xEB
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
```

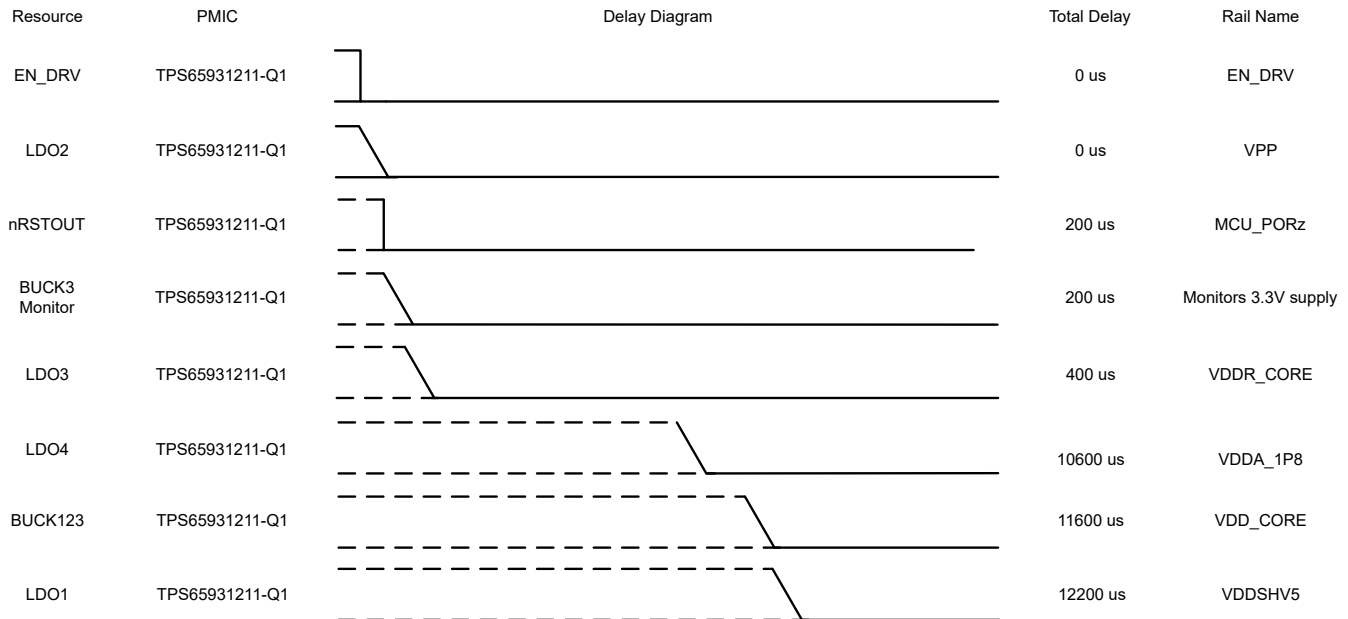


Figure 6-6. Suspend to RAM Sequence

7 Application Examples

This section provides examples of how to interact with the PMICs from the perspective of the MCU and over I²C. [Table 7-1](#) shows how the I²C commands are presented in the following sections. These examples, when used in conjunction with the [datasheet](#), can be generalized and applied to other use cases.

Table 7-1. I²C Instruction Format

I2C Address	Register Address	Data	Mask
0x48 or 0x4C	0x00 - 0xFF	0x00 - 0xFF	0x00 - 0xFF

7.1 Entering and Exiting S2R (Suspend to RAM)

The default configuration of the NVM transitions the PMICs to the ACTIVE state when the ENABLE pin on the TPS65931211 goes high. The nINT pin goes low to indicate that an interrupt has occurred in the PMICs. After a normal power up sequence the BIST_PASS_INT field in the INT_MISC register is set. This interrupt bit indicates that BIST has been completed. Once the BIST_PASS_INT is cleared, the nINT pin is released (goes high) and PMIC can transition to a different state like S2R or Standby. The following section describe how to enter and exit the S2R state by hardware (using the GPIO3 pin) or by software (writing to the NSLEEP2B bit).

Table 7-2. State Table

NSLEEP2 (GPIO3)	NSLEEP2B (register field)	NSLEEP1B (register field)	NSLEEP1_MASK (register field)	NSLEEP2_MASK (register field)	State / Trigger
High	Don't care	Don't care	1	0	ACTIVE State / Trigger A
Low	1	Don't care	1	0	ACTIVE State / Trigger A
Low	0	Don't care	1	0	S2R State / Trigger D

Note

The NSLEEP1_MASK bit on register CONFIG_1 is set by default so the NSLEEP1 trigger does not affect FSM state transition. The mask settings can be changed by I2C when the PMIC is in Active state.

The following code block shows how to execute triggers A and D using I2C commands to transition in and out of the S2R state. In this example the, PMIC is already in the S2R state after the GPIO3 was pulled low. The NSLEEP2B register field has effect only if GPO3 (NSLEEP2) is low.

```
write 0x48:0x86:0x01:0xFE // Set NSLEEP2B to transition out of the S2R state (Trigger A)
write 0x48:0x86:0x00:0xFE // Clear NSLEEP2B to trigger "any2_s2r" sequence (Trigger D)
```

Instead of writing to the NSLEEP2B bit to return to the ACTIVE state, using the GPIO3 pin to return the PMIC to the ACTIVE state is also possible.

7.2 Entering and Exiting Standby

STANDBY can be entered from ACTIVE, or the S2R states. to stay in the mission state of STANDBY and not enter the hardware state LP_STANDBY, the LP_STANDBY_SEL bit must be cleared.

The STANDBY state turns off all regulators. Therefore, selecting the state that the STANDBY state returns to is required. When the ENABLE pin goes low, the orderlyOff sequence is triggered. When the ENABLE pin goes high again, the destination state is dependent upon the STARTUP_DEST bits. The orderlyOff sequence is also triggered by the I2C_0 trigger. In this example, I2C_0 trigger is used to enter the STANDBY state.

```
write 0x48:0xC3:0x00:0xF7 // LP_STANDBY_SEL=0
write 0x48:0x85:0x01:0xFE // set I2C_0 trigger, trigger orderlyoff sequence
Once the PMIC is in standby state, a wakeup request can be triggered with a rising edge on the Enable pin.
```

7.3 Entering and Existing LP_STANDBY

Entering the LP_STANDBY hardware state follows the same power-down sequence as entering STANDBY. Exiting LP_STANDBY is different and requires different initializations before entering LP_STANDBY.

When entering LP_STANDBY, the PFSM automatically transitions to the hardware FSM state of SAFE_RECOVERY. From the SAFE_RECOVERY state, the recovery counter is incremented and compared to the recovery count threshold (see RECOV_CNT_REG_2, in [Table 5-10](#)). If the recovery count threshold is reached, then the PMICs halt recovery attempts and require a power cycle. Refer to the [TPS6593 datasheet](#) for more details.

```
write 0x48:0xc3:0x08:0xf7 // LP_STANDBY_SEL=1
write 0x48:0xc3:0x60:0x9f // Set the STARTUP_DEST=ACTIVE
write 0x48:0x85:0x01:0xfe // set I2C_0 trigger
```

8 Design and Documentation Support

8.1 Documentation Support

For additional information regarding the PMIC or processor devices, use the following:

- Texas Instruments, [AM62A starter kit for low-power Sitara processors](#)
- Texas Instruments, [TPS6593 Datasheet](#)
- Texas Instruments, TPS6593-Q1 Safety Manual (request through mySecure)
- Texas Instruments, [AM62Ax Datasheet](#)
- Texas Instruments, [AM62Ax Sitara Processors Technical Reference Manual](#)

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2023) to Revision A (November 2025)	Page
• Updated the document title.	1
• Updated the document format to a design guide.	1
• Added Description , Features , and Applications topics.	1

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