*Application Note*

# *112G and 224G PAM4 SerDes Clocking for Rapid Data Center Switches*

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**ABSTRACT**

Hyperscale data centers and telecommunication market sectors are currently driving the need for high speed serial links using 112G and 224G Pulse Amplitude Modulation with 4-Levels Serializer and Deserializer (PAM4 SerDes). The higher data speeds lower the jitter budget for the 312.5MHz reference clock to less than 100fs RMS for 112G and 35fs RMS with 4MHz high pass filter (HPF) for 224G PAM4 SerDes.

TI's Bulk Acoustic Wave (BAW) technology offers industry-leading, ultra-low jitter clocks critical for the 112G and 224G PAM4 SerDes. The LMK5B33216 achieves 42fs RMS typical and 24fs RMS typical with 4MHz HPF filter for 312.5MHz outputs, meeting the 112G and 224G PAM4 SerDes requirements with a greater margin. In addition, the LMK5B33216 meets the jitter, rise or fall time, hit less switching, and holdover requirements of the 112G and 224G PAM4 SerDes reference clocks.

TI offers a complete clocking design for data center applications as shown in Figure 1-1. This application note examines the clocking design specifically for 800G switches (ToR, leaf, spine, fabric, edge, or aggregation). The switch clocking design includes the LMK5B33216 or LMK5B33414 network synchronizer, single-ended and differential buffers, BAW-based oscillators and reference-less clock generators.

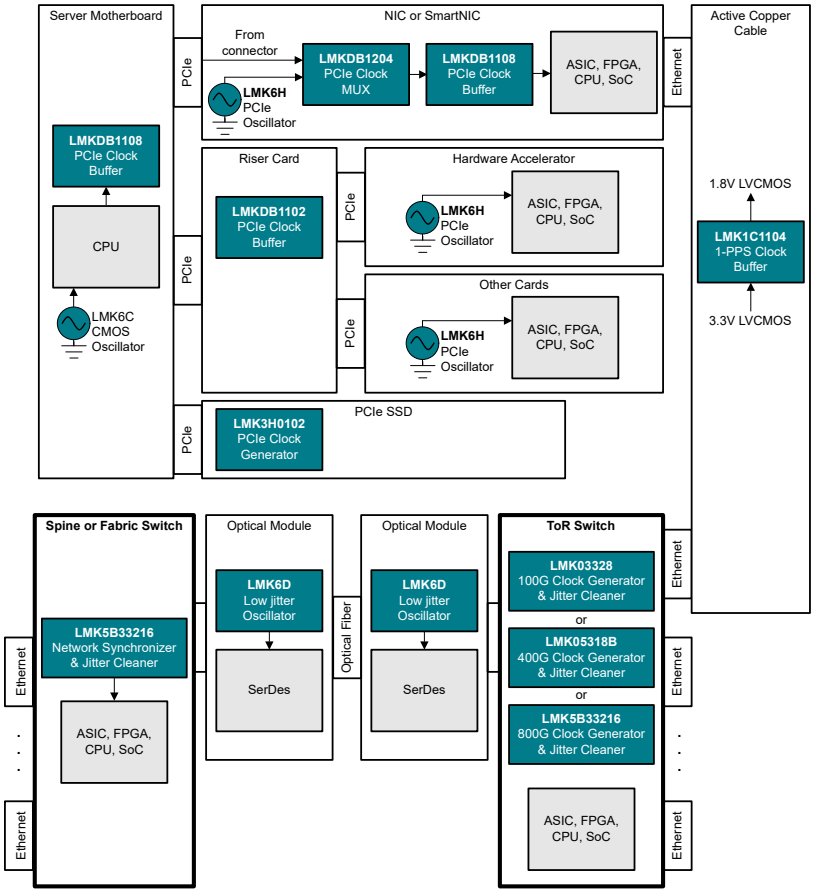


**Figure 1-1. Data Center Clocking Design**

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## Trademarks

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# 1 800G Market Trend

800G switches have made significant leaps forward in data networking by leveraging 112G and 224G PAM4 SerDes technology. The 112G PAM4 SerDes is designed to transmit data at 112 gigabits per second (Gbps) whereas the 224G PAM4 transmits data at 224Gbps. For more details on PAM4 SerDes applications, refer to *Understanding Clocking Needs for High-Speed 56G PAM4 Serial Links*.

The 800G high-speed switches are engineered to meet increasing data center and telecommunication demands. The 800G switches have a port speed of 800Gbps that provides bandwidth for rapid data transmission which reduces network congestion for data processing, storage, and distribution. The 800G switches have fast transmission rates, often measured in terabits per second, that handle immense volumes of data generated by virtualization and high-performance computing.

Clocking in high-speed SerDes systems plays an important role in data synchronization and communication reliability. A SerDes has an integrated PLL that clocks out high-speed serial data while maintaining phase-lock to a reference clock. A high-speed SerDes relies on a precise clocking mechanism to maintain proper timing and accurate serialization and deserialization of data. Therefore, providing a low-jitter clock to the integrated SerDes PLL is necessary.

Incorporating a low-jitter clock is achievable by using an external-network synchronizer or jitter cleaner to reduce the noise propagated onto the serial data. A network synchronizer allows the flexibility of switching between various inputs of different frequencies and phase domains without disrupting the SerDes reference.

TI network synchronizers and jitter cleaners with integrated BAW, such as the LMK5B33216, are designed to provide the reference clocks to the SerDes and to support 800G or higher throughputs of data in real-time communication, AI, or IOT applications.

Figure 1-1 demonstrates a simplified block diagram of a 112G and 224G PAM4 SerDes clock input sourced from the LMK5B33216.

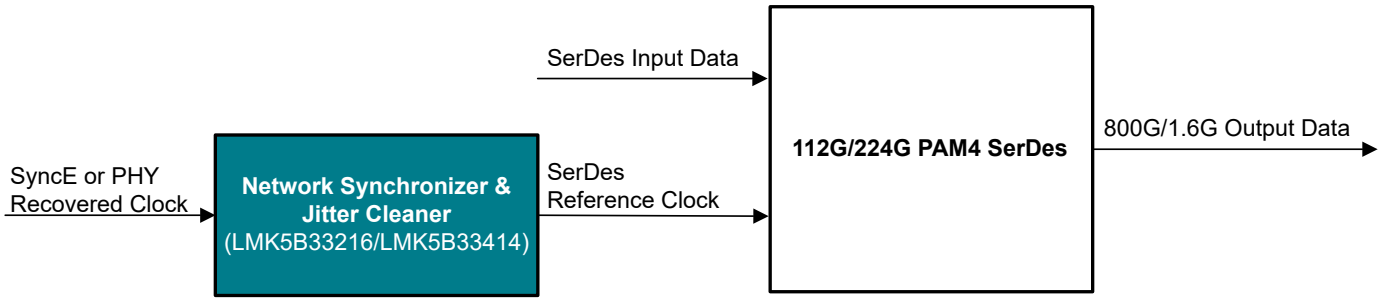



**Figure 1-1. 112G and 224G PAM4 SerDes Simplified Block Diagram**

# 2 LMK5B33216 for 112G and 224G PAM4 SerDes Applications

The LMK5B33216 is used to jitter-clean SyncE or PHY recovered clocks and provide synchronized, low-jitter, outputs to the ASIC and CPU.

Figure 2-1 shows the full system design for an 800G switch using the LMK5B33216. Pairing the LMK6Cx (TI's BAW-based LVCMOS oscillator family) with the LMK5B33216 yields a low-cost option for the XO input. Additional clocks can be fanned out to the ASIC through a 4, 8, 12, or 16 output, low additive jitter, and clock buffer from the LMK1Dxxxx family, such as the LMK1D1204.

The LMK3H0102 is a reference-less, BAW-based, clock generator used to clock up to two PCIe Gen 1 to PCIe Gen 6 compliant outputs. Each LMK3H0102 output is capable of generating any frequency between 2.5MHz and 400MHz by dividing down from two fractional output dividers (FODs).

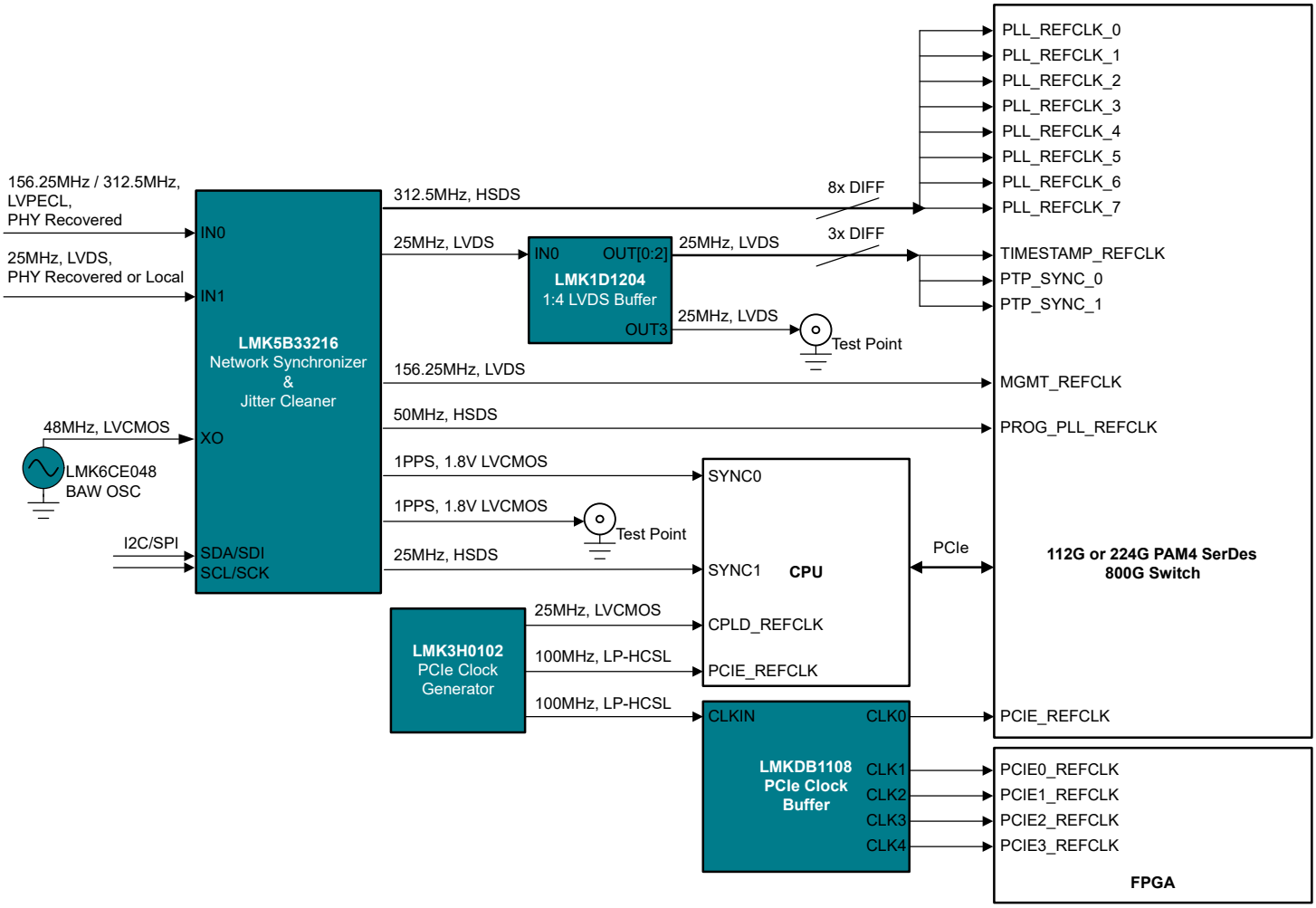



**Figure 2-1. Full System Design for 800G Switch Applications**

## 3 LMK5B33216 Overview

Bit error rates (BER) are minimized in applications involving high-speed SerDes links with the excellent jitter performance of the LMK5B33216. The LMK5B33216, along with the TI PTP Stack option, achieves better than Class D accuracy with sub 5ns timing accuracy. The device is compliant with the ITU-T G.8373.2 standard using the G8275.1 and G8275.2 profiles for full timing and partial timing support (see the application note, *LMK5XXXXXS1 Network Synchronizer Compliance Test Report for PTP Profiles G.8275.1 and G.8275.2*). For more information on TI's complete IEEE-1588 PTP and SyncE clocking options, visit TI's *Clocks and Timing* page.

TI's network synchronizers leverage a Digital Phase-Locked Loop (DPLL) and an Analog Phase-Locked Loop (APLL) combination to maintain phase lock with a reference clock. The DPLL steers the clock output phase by making continuous updates to the APLL numerator as the DPLL tracks the phase of the reference clock. The LMK5B33216 contains three pairs of DPLL + APLL to support up to three synchronization and frequency domains.

The clock outputs can phase-lock between either two inputs (LMK5B33216) or four inputs (LMK5B33414) when using the DPLL + APLL pair. Alternatively, the outputs can lock to a single reference, or oscillator, when using only the APLL. The device can operate in three modes: normal operation with the DPLL active, holdover when the input clocks are unavailable, and free-run where the DPLL is turned off and only the internal APLL is functioning.

Additionally, the LMK5B33216 provides input clock detection and monitoring, wander and jitter filtering, hitless switching, holdover, and Zero-Delay Mode (ZDM) functionality. Each DPLL includes a programmable loop bandwidth (LBW) to maximize flexibility and ease of use, which can be set between 1MHz to 4kHz without external loop filter components. For SyncE input clocks, TI recommends setting the DPLL LBW between 1Hz and 3Hz to filter out SyncE transient noise. The APLL loop filter is also fully integrated except for one external capacitor.

The LMK5B33216 clock outputs are configurable from several output formats: 1.8V or 2.65V LVCMOS, HCSL, and AC-LVPECL, AC-CML, or LVDS using the High Swing Differential Signaling (HSDS) driver. The output swing and common-mode voltage are programmable to meet various receiver requirements with the HSDS format.

## 4 LMK5B33216 Performance

Designed for 800G switch applications, the LMK5B33216 is a high-performance network synchronizer that meets the stringent Ethernet-based networking requirements for jitter, rise or fall time, hitless switching, and holdover.

Table 4-1 compares the performance of the LMK5B33216 output clock with the SerDes core reference clock requirements used in 800G switch applications. Figure 4-1 and Figure 4-2 show the LMK5B33216 output phase noise performance meeting the 112G and 224G PAM4 SerDes requirements, respectively. Both output phase noise plots are attained when using a 48MHz TCXO input clock. The LMK5B33216 exceeds the requirements of the 112G and 224G PAM4 SerDes reference clock with the low-noise performance of the Voltage-Controlled BAW Oscillator (VCBO).

**Table 4-1. Comparison Between an Example SerDes Core Reference Clock and LMK5B33216 Output**

| Parameter | Example 112G and 224G PAM4 SerDes Core Reference Clock | | | LMK5B33216[1] | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| Frequency | – | 312.5 | – | – | 312.5 | – | MHz |
| RMS jitter (12kHz to 20MHz) | – | – | 100 | – | 42[2] | 60[2] | fs |
| RMS jitter (12kHz to 20MHz) with 4MHz HPF | – | – | 112G PAM4: 90<br>224G PAM4: 35 | – | 24 | – | fs |
| Reference clock phase noise at 100kHz | – | – | -137 | – | -146 | – | dBc/Hz |
| Reference clock phase noise at 1MHz | – | – | -143 | – | -159 | – | dBc/Hz |
| Reference clock phase noise at 10MHz | – | – | -158 | – | -160 | — | dBc/Hz |
| Differential peak-to-peak voltage swing | 800 | – | 1400 | 670 | – | 2300 | mVpp |
| Rise or fall time (20% to 80%) | – | 300 | 400 | 175 | 230 | 300 | ps |

**Table 4-1. Comparison Between an Example SerDes Core Reference Clock and LMK5B33216 Output (continued)**

| Parameter | Example 112G and 224G PAM4 SerDes Core Reference Clock | | | LMK5B33216[1] | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| Operating ambient temperature | – | – | – | -40 | – | 85 | °C |

(1) The measurements are taken using a 48MHz TCXO as the XO input. All LMK5B33216 outputs are set to the same frequency and sourced from the BAW APLL (APLL3).
(2) The BAW APLL post divider is 8 and the output swing (VOD) is ≥ 800mV.

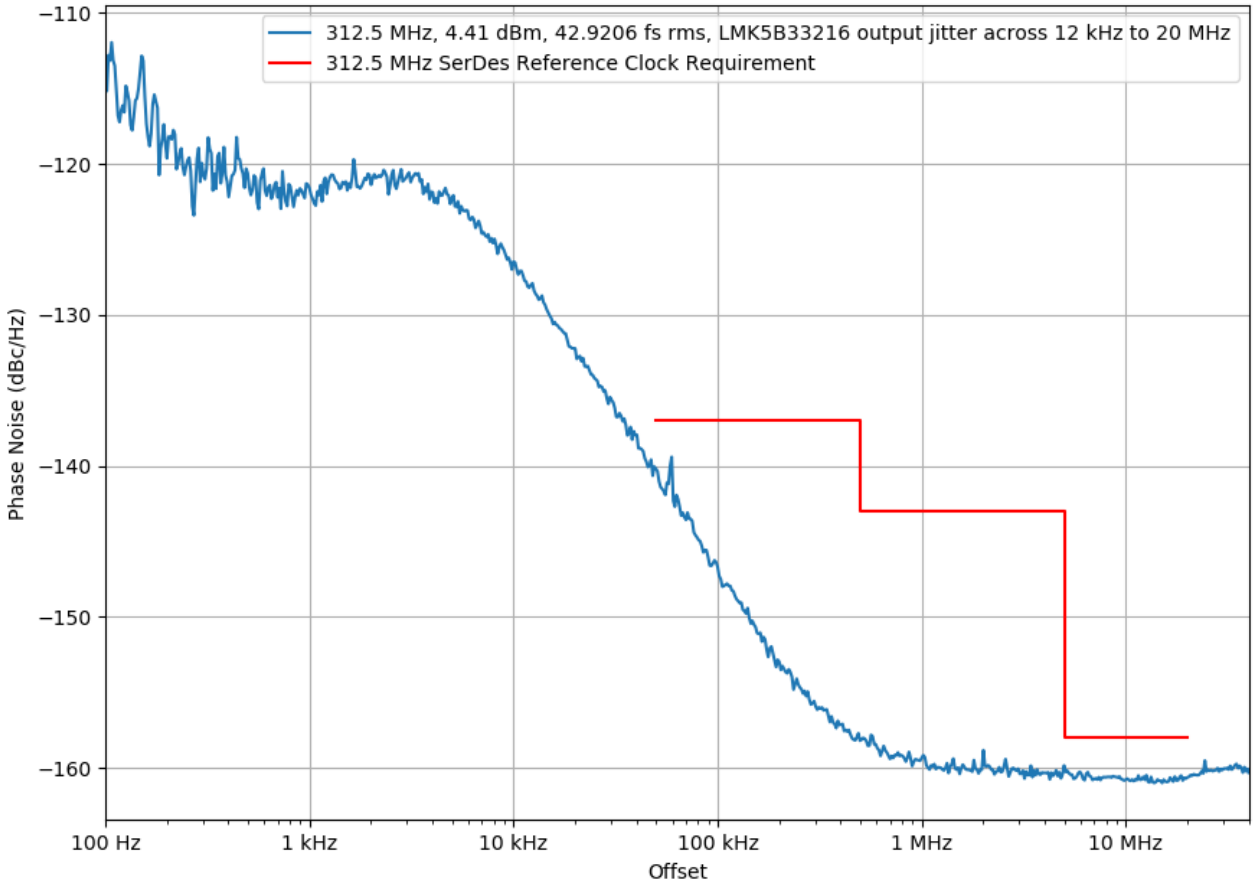



**Figure 4-1. LMK5B33216 Output Phase Noise Plot with 112G PAM4 SerDes Mask Overlayed**

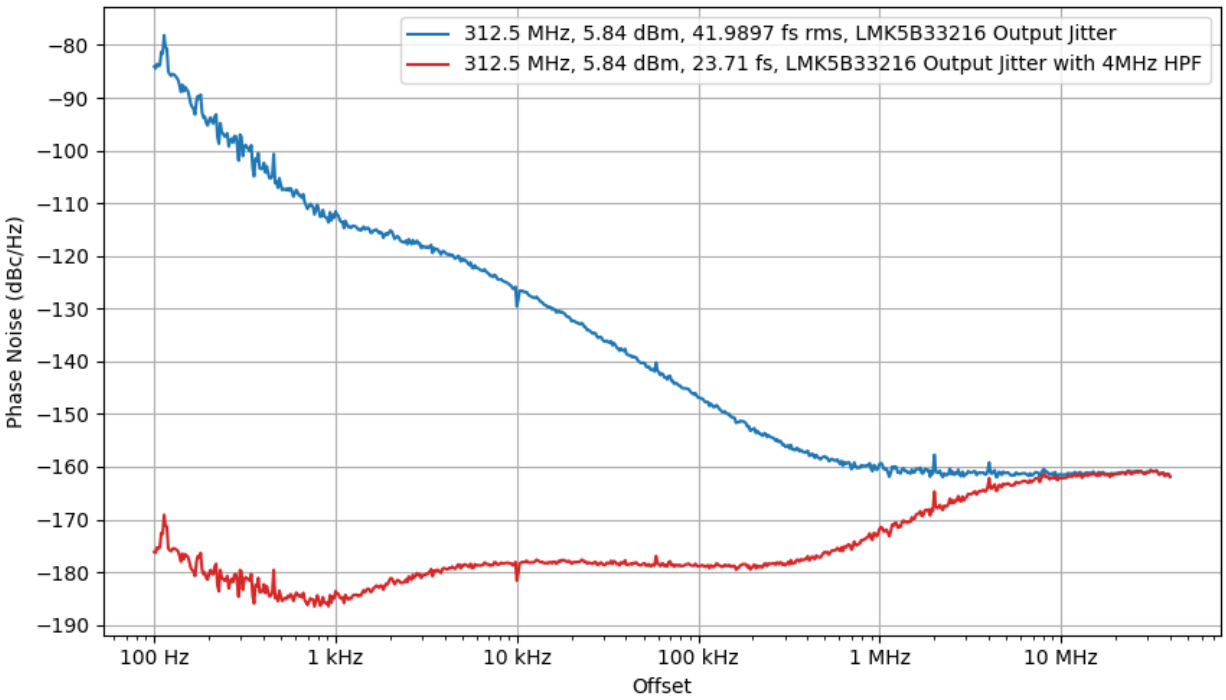



**Figure 4-2. LMK5B33216 Output Phase Noise with 4MHz HPF**

## 4.1 RMS Jitter

Table 4-2 demonstrates additional RMS jitter data across various integration ranges.

**Table 4-2. Jitter Performance of the LMK5B33216 Across Different Integration Ranges**

| Output Clock Frequency [MHz] | RMS Jitter (typ.) [fs](1) | Jitter Integration Range [MHz] |
|---|---|---|
| 156.25(2) | 47 | 0.012 to 20 |
| | 26 | 0.100 to 5 |
| | 31 | 0.750 to 10 |
| | 71 | 0.200 to 50 |
| | 15 | 2 to 4 |
| | 39 | 4 to 20 |
| 312.5(3) | 42 | 0.012 to 20 |
| | 19 | 0.100 to 5 |
| | 21 | 0.750 to 10 |
| | 47 | 0.200 to 50 |
| | 10 | 2 to 4 |
| | 26 | 4 to 20 |
| 625(4) | 35 | 0.012 to 20 |
| | 12 | 0.100 to 5 |
| | 11 | 0.750 to 10 |
| | 25 | 0.200 to 50 |
| | 5 | 2 to 4 |
| | 13 | 4 to 20 |

(1) The measurements were taken using an XO input frequency of 48MHz with all LMK5B33216 outputs set to the same frequency with an output swing (VOD) ≥ 800mV.
(2) The APLL3 post divider is 16.
(3) The APLL3 post divider is 8.
(4) The APLL3 post divider is 4.

## 4.2 BAW Technology

The LMK5B33216 meets the challenging requirements for advanced high-speed communication networks by leveraging the BAW technology. The LMK5B33216 integrates a VCBO into APLL3 (the BAW APLL) to achieve ultra-low phase noise and jitter. The VCBO is a high-Q BAW resonator that is co-packaged with the LMK5B33216 silicon IC. Output clocks generated from the BAW APLL achieve excellent output RMS jitter and phase noise performance for the telecom industries.

The VCBO operates at 2500MHz (± 100ppm) and can be divided down to output 312.5MHz clocks with 42fs typical and 60fs maximum RMS jitter (12kHz to 20MHz) regardless of the DPLL reference clock frequency and jitter characteristics. The remaining APLLs are LC-VCOs and can be used for additional frequency domains outside the Ethernet domain or when the output frequency cannot be sourced from the BAW APLL.

Figure 4-3 shows the composition of the BAW resonator technology. The structure includes a thin layer of piezoelectric film between two metal films and other layers that confine the mechanical energy. The BAW utilizes this piezoelectric transduction to generate a vibration, therefore, outputting a clock frequency. For more information on the BAW, refer to our list of *BAW Application Notes*.

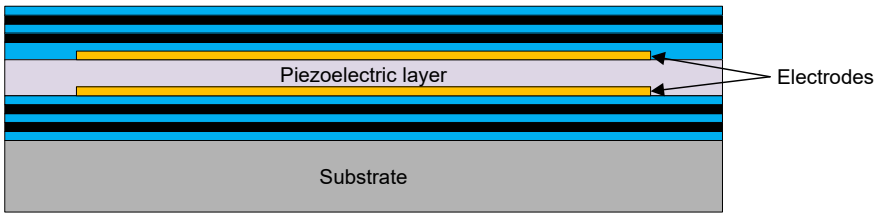



**Figure 4-3. Basic Structure of a Bulk Acoustic Wave Resonator**

The BAW technology in the LMK5B33216 greatly reduces the phase noise and RMS jitter of the synchronized output clock, thereby meeting and exceeding the challenging system requirements for 400Gbps and 800Gbps systems by a comfortable margin.

## 4.3 Phase Noise Profile

The output phase noise profile of a network synchronizer like the LMK5B33216 can be broken down into four dominating regions:

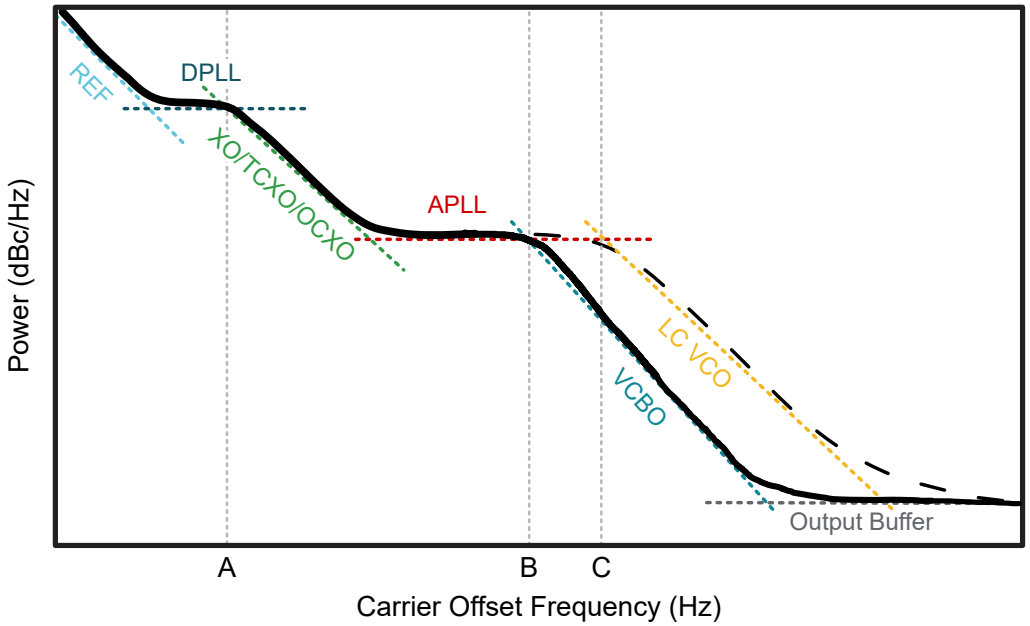
- Below the DPLL LBW
- Between the DPLL and APLL LBWs
- Above the APLL LBW
- Output noise floor

The quality of the DPLL reference and XO, TCXO, and OCXO inputs impact the close-in phase noise of an output clock. The DPLL LBW is a low-pass filter to the DPLL reference clocks. The DPLL reference primarily impacts the output noise profile at carrier offsets less than the DPLL LBW. The DPLL can be configured with a narrower LBW (such as 10Hz) for applications where close-in phase noise matters and noisy references are used as the DPLL inputs. Otherwise, either 10Hz or 100Hz are common settings that can be used since the DPLL reference does not impact the jitter at carrier offsets from 12kHz to 20MHz. Figure 4-5 and Figure 4-5 are examples of phase noise plots with outputs sourced from the VCBO. These plots demonstrate the negligible effect of jitter across 12kHz to 20MHz with different DPLL LBWs.

Above the DPLL LBW, the DPLL reference is attenuated and a combination of the XO/TCXO/OCXO input and the APLL noise dominates up until the APLL LBW. To take advantage of the excellent VCBO performance, the BAW APLL is configured with a narrow LBW, typically 3kHz to 5kHz; as a result, the VCBO dominates the phase noise in the carrier offset range of 8kHz to around 400kHz. Lastly, the noise floor is set by the output buffer, beginning at approximately 1MHz carrier offset.

Thanks to the ultra-low noise VCBO, a low frequency XO (such as 12.8MHz) can be used for the LMK5B33216 without significantly impacting the total RMS jitter, thereby lowering the total design cost.

Figure 4-4 provides a summarized illustration of how each region affects the phase noise of an output clock.




A: DPLL loop bandwidth can be set between 1mHz to 4kHz.
B: APLL loop bandwidth for VCBO can be set between 1kHz and 10kHz.
C: APLL loop bandwidth for LC VCO can be set between 100kHz and 1MHz.

**Figure 4-4. General Phase Noise Plot of a Network Synchronizer Output Clock**

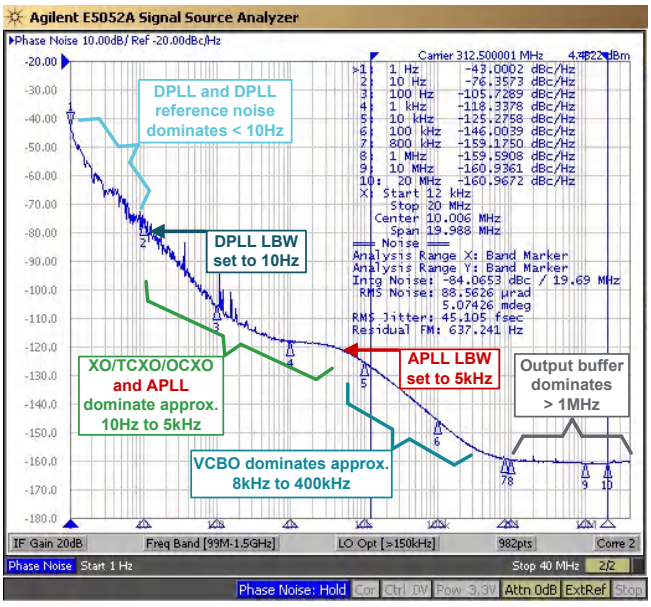



**Figure 4-5. Phase Noise Breakdown of an LMK5B33216 Output Using a 10Hz DPLL LBW**

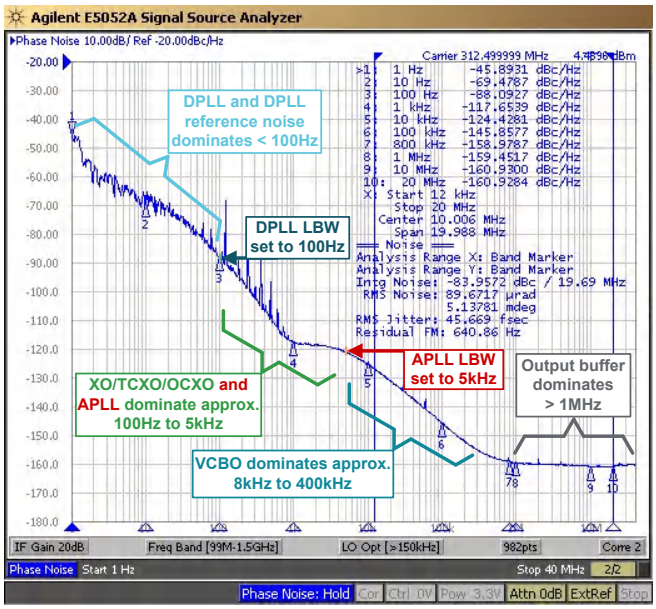



**Figure 4-6. Phase Noise Breakdown of an LMK5B33216 Output Using a 100Hz DPLL LBW**

# 5 LMK5B33216 Features

## 5.1 Frequency and Phase Adjustments

To support IEEE-1588 PTP or other clock steering applications, each DPLL allows precise frequency and phase adjustments through register, or pin control, by using a Digitally-Controlled Oscillator (DCO), as shown in Figure 5-1. Adjustments with less than 1ppt (part per trillion) frequency resolution are supported by the DPLL DCO. The

DPLL DCO feature allows increments and decrements to the numerator of the DPLL fractional N-divider. Such frequency adjustments are effectively propagated through the APLL domain and onto the output clocks or any cascaded DPLL/APLL domains.

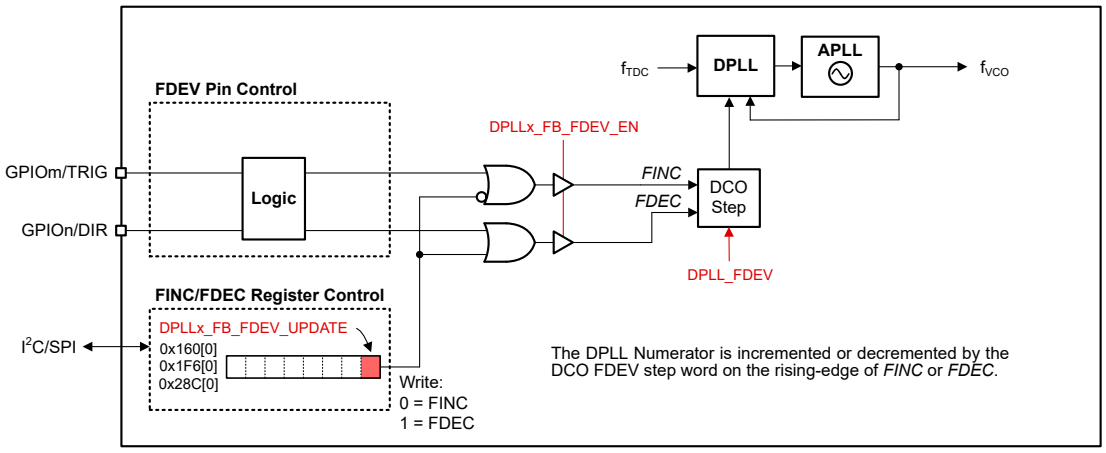
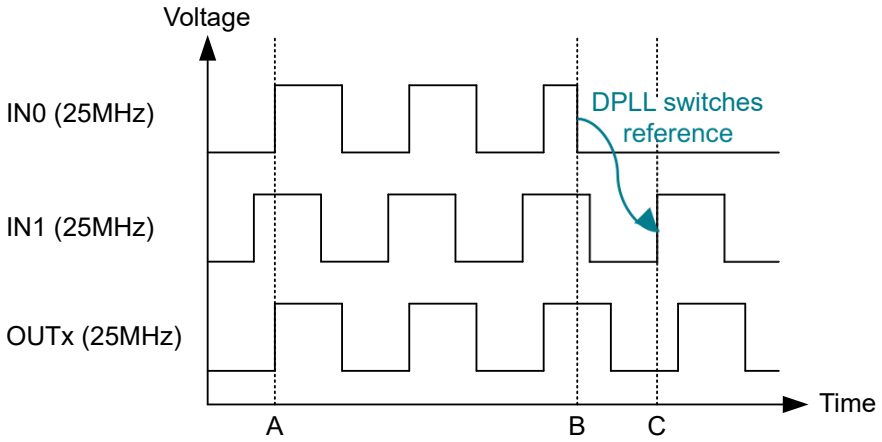



**Figure 5-1. Overview of the DPLL DCO**

## 5.2 Input Reference Switching

Each DPLL supports hitless reference switching with a minimal phase hit through a phase cancellation scheme (also known as phase buildout) and offers an optional phase slew control feature.

The outputs maintain the same phase with hitless switching, with only minor disturbance from before the reference switch, to after the reference switch, as illustrated in Figure 5-2. Without hitless switching, there is a risk of the outputs getting phase hits, which can propagate to the downstream clocks and cause misalignment across data packets. The phase hit is equal to the phase offset between the two reference clocks.



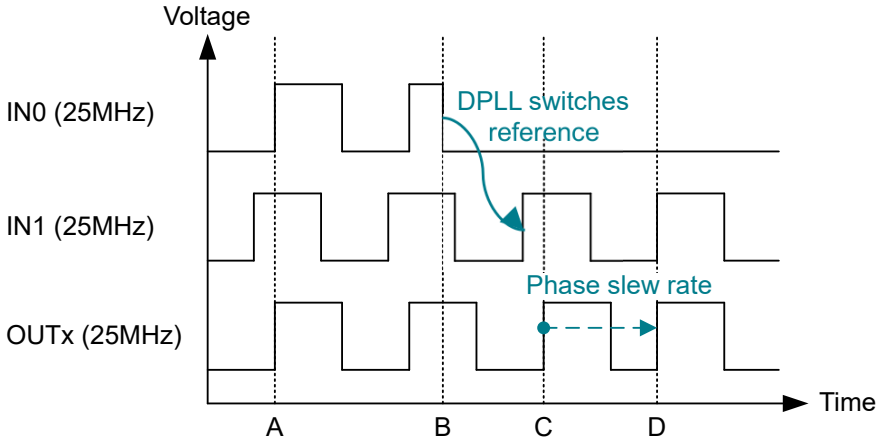

A: OUTx is locked to IN0 with the same phase.

B: IN0 is lost and the DPLL switches reference from IN0 to IN1 without affecting the phase on OUTx.

C: OUTx is locked to IN1 without changing the phase.

**Figure 5-2. Phase Cancellation Enabled for Switching Reference With Minor Phase Hits**

The outputs gradually adjust phase after a hitless switch when using the phase slew control feature. The phase transitions from the original to the new reference at a rate defined by the programmed phase slew rate. This feature is demonstrated in Figure 5-3.




A. OUTx is locked to IN0 with the same phase.
B. IN0 is lost and the DPLL switches reference from IN0 to IN1.
C. The phase of OUTx gradually changes at a rate defined by the programmed phase slew rate.
D. OUTx is locked to IN1 with the same phase.

**Figure 5-3. Phase Slew Control Enabled to Provide a Steady Output Phase Change When Switching Inputs**

## 5.3 Holdover

Holdover occurs when the DPLL reference clocks become unavailable, as seen in Figure 5-4. During holdover, the APLL numerator is set by the DPLL tuning word history, which determines the output frequency accuracy upon entry into holdover—any error on entry is considered a short-term holdover error. The tuning word history can be configured as either the accumulated averaged reference phase history, a user-specified value, or the last APLL numerator value.

The quality of the external oscillator (provided to XO input) determines the long-term frequency stability and accuracy of the output frequency. Over time, temperature fluctuations impact the frequency accuracy of the output clocks. Hence, the decision to choose between an XO, TCXO, or OCXO lies primarily on the long-term holdover requirements of the system.

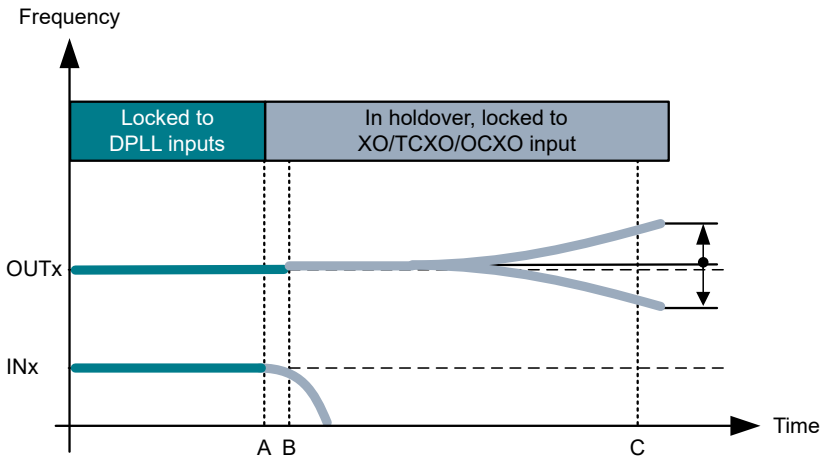



**Figure 5-4. Holdover Functionality**

A. Reference failure is detected by the device as the DPLL references (INx) are lost.
B. The DPLL enters holdover and outputs remain phase or frequency locked with a small frequency delta.
C. The output frequency drifts; the long-term holdover stability is based on the XO/TCXO/OCXO input accuracy.

For applications requiring output frequency correction during long-term holdover, the output frequency can be corrected by making APLL DCO adjustments through software to compensate for temperature variations, as shown in Figure 5-5.

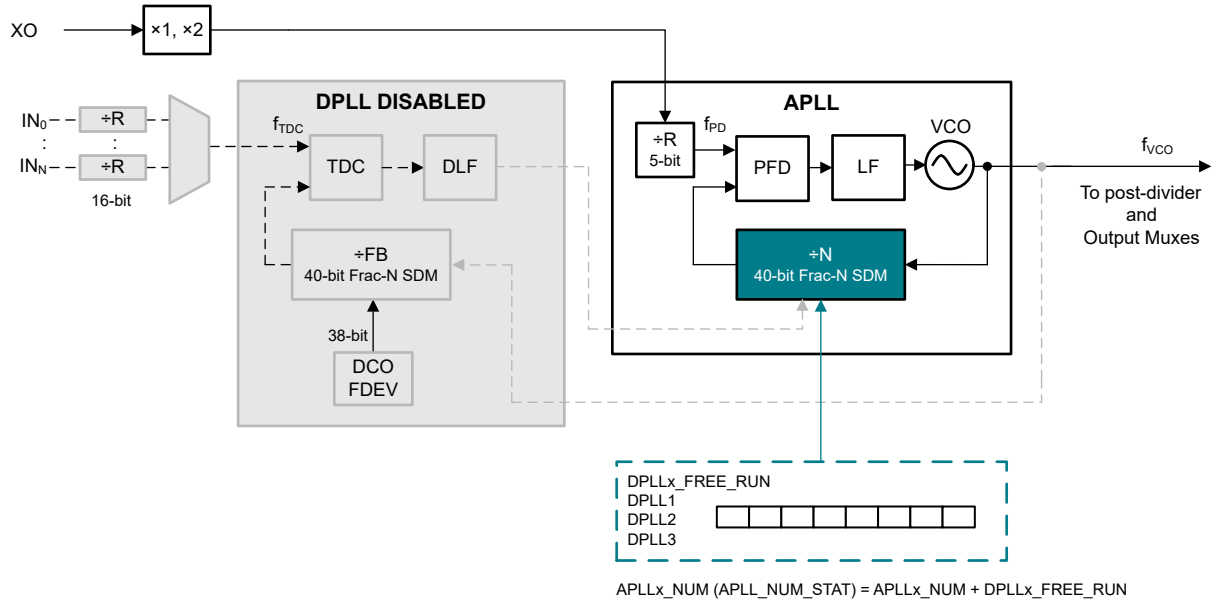



**Figure 5-5. APLL DCO Operation During Holdover**

### 5.4 Zero-Delay Mode

Each DPLL supports Zero Delay Mode (ZDM) to achieve a deterministic phase relationship between the DPLL reference clock and the ZDM feedback output clock at every boot-up or software reset. All output clocks sourced from a ZDM-configured DPLL become phase aligned through the synchronization (SYNC) feature. A zero-phase delay is attainable across all clocks by inserting analog or digital delays available on the LMK5B33216.

Figure 5-6 demonstrates how select outputs, such as OUT0, can internally feed back to any DPLL as a zero-delay output clock. For additional details on ZDM theory, refer to *Multi-Clock Synchronization*.

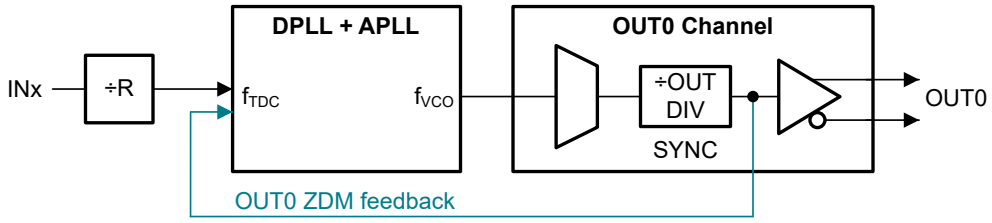



**Figure 5-6. DPLL ZDM Synchronization Between Reference Input and OUT0**

## 6 Summary

The role of clocks are critical in supporting the high-speed data links using the 112G and 224G PAM4 SerDes. Clocks must deliver low jitter and phase noise signals to maintain integrity of the PAM4 symbols and minimize errors. TI's BAW technology enables network synchronizer designs with greater system noise margins (such as the LMK5B33216) to meet the stringent SerDes reference clock jitter and phase noise requirements.

Precise frequency and phase adjustments are possible with integrated DCOs and this supports IEEE-1588 PTP designs. The network synchronizer outputs can be configured to lock between different domains (including SyncE and PTP) and hitless switching can occur between references with minimal disturbance to the downstream clocks. The LMK5B33216 leverages a DPLL history feature which sets frequency accuracy to minimize the short-term holdover errors in the event reference clocks are lost.

## 7 References


- Texas Instruments, LMK5B33216, product page
- Texas Instruments, LMK5B33414, product page
- Texas Instruments, LMK6Cx, product page
- Texas Instruments, LMK1D1204, product page
- Texas Instruments, LMKDB1108, product page
- Texas Instruments, LMK3H0102, product page
- Texas Instruments, *Understanding Clocking Needs for High-Speed 56G PAM-4 Serial Links*, application note
- Texas Instruments, *TI BAW Technology Enables Ultra-Low Jitter Clocks for High- Speed Networks*, white paper
- Texas Instruments, *BAW Oscillator Solutions for Network Interface Card*, application brief
- Texas Instruments, *Multi-Clock Synchronization*, application note

# 8 Revision History

| Changes from Revision * (February 2024) to Revision A (January 2025) | Page |
|---|---|
| • Added data center clocking design block diagram | 1 |
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added 224G PAM4 SerDes description throughout the document | 1 |
| • Changed from PAM-4 to PAM4 | 1 |
| • Updated by combining *Introduction* into the *800G Market Trend* section | 3 |
| • Changed *LMK5B33216 for Ethernet Applications* title to *LMK5B33216 for 112G and 224G PAM4 SerDes Applications* | 4 |
| • Added LMKDB1108 description | 4 |
| • Updated the full system design block diagram | 4 |
| • Changed *LMK5B33216 for SerDes Applications* title to *LMK5B33216 Overview* and rearranged text | 5 |
| • Changed *LMK5B33216 for SerDes Applications* title to *LMK5B33216 Performance* and rearranged text | 5 |
| • Changed figure title from *General Phase Noise Plot* to *General Phase Noise Plot of a Network Synchronizer Output Clock* | 8 |

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