Application Note

Oscillator Power Considerations for PLL Devices

Jennifer Bernal *Clock and Timing Solutions*

ABSTRACT

An oscillator with poor power supply noise rejection (PSNR) is vulnerable to noisy supplies and can degrade the phase noise at the both the oscillator output and the analog phase locked loop (APLL) output. Oscillators, such as the LMK6Cx and CDC6Cx, simplify power supply design by integrating LDOs. Enhancing the oscillator supply filter further reduces the output clock phase noise. For systems with limited power supply flexibility, high-performance network synchronizers, like the LMK5B33216, allow low-jitter clock generation even with noisy supplies by using the internal LDO to power the oscillator. Additionally, the BAW-based jitter cleaner enables an APLL configuration with a narrow loop bandwidth, minimizing the impact of the oscillator on APLL output clocks.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

An APLL is a clocking device used to generate output clocks that are synchronized to an input. Typically, the APLL reference is provided by a crystal oscillator (XO), temperature-controlled oscillator (TCXO), or oven-controlled oscillator (OCXO). Figure 1-1 illustrates a block diagram of a network synchronizer which consists of a digital phase-locked loop (DPLL) and APLL pair. The APLL input clock provides the frequency accuracy and stability of the PLL output clocks during free-run or long-term holdover.

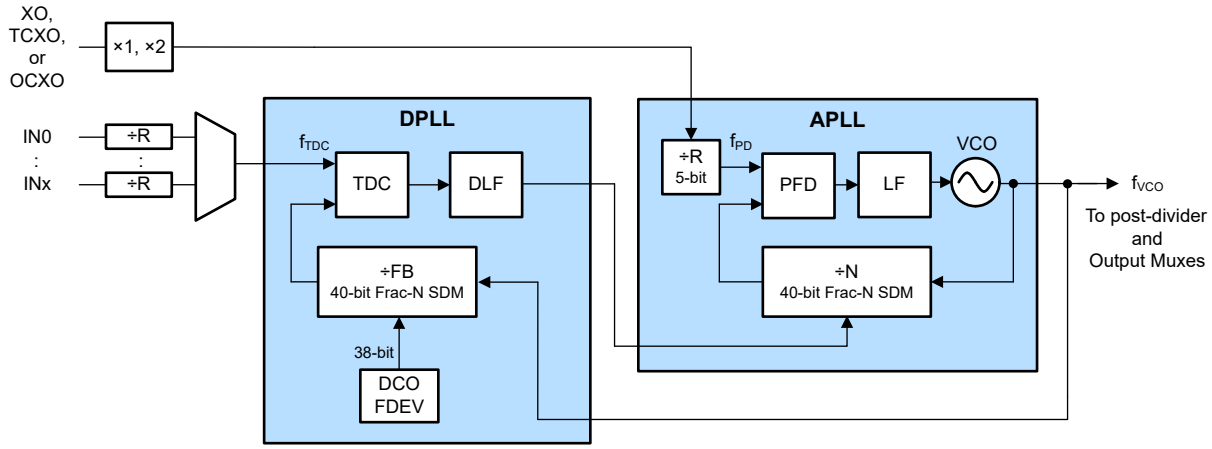


Figure 1-1. Generic Block Diagram of a Network Synchronizer

The close-in phase noise (< 10kHz offset) of the PLL outputs depends on the quality of the APLL reference (XO, TCXO, or OCXO). The power supply of the APLL reference can also affect the quality of the output clocks. If the supply is noisy, then the PLL output clock phase noise can degrade. The next sections explain how the oscillator supply impacts the PLL performance and how to optimize clocking designs.

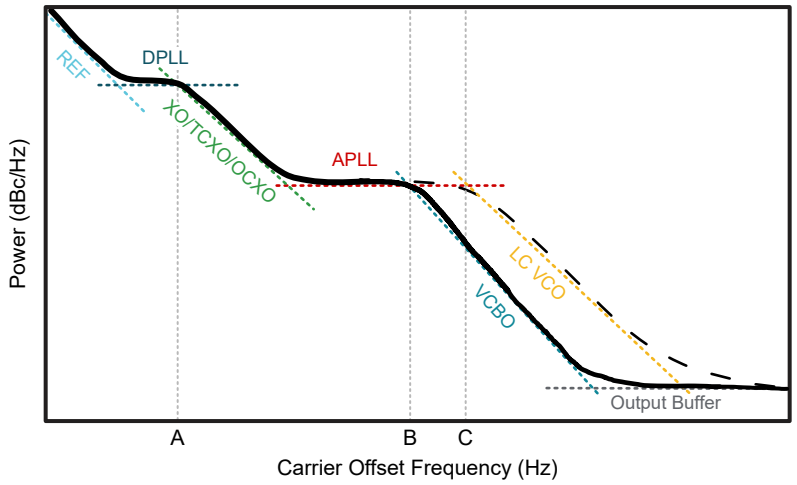
Note

For the remainder of this application note, the term "XO" is used for simplicity, but the concepts apply to any XO, TCXO, OCXO, or other APLL reference clock source.

2 Impact of Oscillator Noise on PLL Performance

Figure 2-1 shows the phase noise contributors of a network synchronizer output clock. Up to the APLL loop bandwidth (LBW), the synchronizer output noise comes from the XO output noise and APLL noise. This means APLL outputs are sensitive to XO noise below the APLL LBW (Marker B/C). The XO output noise typically dominates the close-in phase noise of APLL outputs. For example, if the APLL LBW is set to 5kHz, then the XO noise dominates the APLL output clock below the 5kHz offset. Above 5kHz, the APLL loop filter reduces the XO noise. For devices with a DPLL, the XO noise and APLL noise dominate between the DPLL LBW and the APLL LBW (between Marker A and B/C).

Configure the APLL with a wider LBW (> 10kHz offset) when the XO noise profile is better than the VCO noise to mitigate the VCO noise. For most applications, where the XO noise is worse than the VCO noise, use a narrow LBW (< 10kHz offset).



A. Marks the DPLL LBW (configurable between 1mHz to 4kHz on the LMK5B33216)
B. Marks the APLL LBW for the VCBO (configurable between 1kHz and 10kHz on the LMK5B33216)
C. Marks the APLL LBW for the LC VCO (configurable between 100kHz and 1MHz on the LMK5B33216)

Figure 2-1. General Phase Noise Plot of a Network Synchronizer (DPLL and APLL) Output Clock

For more details on PLL output clock phase noise, see the *Phase Noise Profile* section from the *112G and 224G PAM4 SerDes Clocking for Rapid Data Center Switches* application note.

3 Consideration #1: XO PSNR

One important design factor for PLLs is the PSNR performance of the XO. The PSNR defines how much the XO output is affected by the supply noise. An XO with a poor PSNR can cause higher noise and worsen the PLL output noise.

A recommended practice is to use an XO with a good PSNR or integrated LDO. For example, the LMK6C and CDC6C oscillators include an internal LDO and have excellent PSNR, as shown in Figure 3-1 and Table 3-1. Using an oscillator with these features reduces the supply noise and provides a low-noise output clock. This approach is beneficial for early design stages or systems where the supply filter cannot be changed.

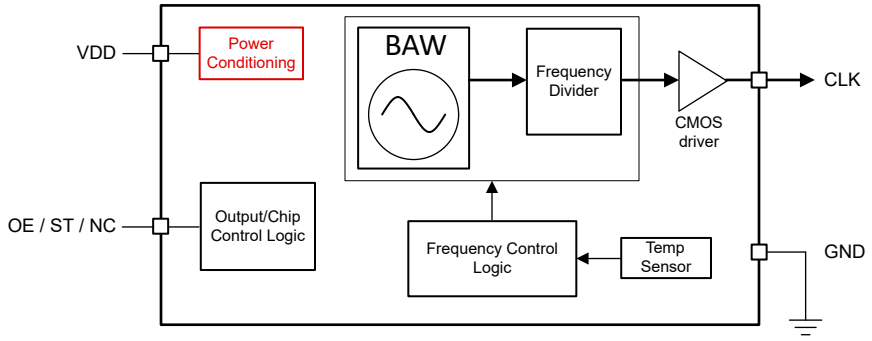


Figure 3-1. Functional Block Diagram of LMK6C and CDC6C Oscillators

Table 3-1. PSNR Characteristics of CDC6C Oscillator

Power Supply Ripple Frequency[1] [kHz]	Induced Spur, TYP [dBc]	
	LMK6C	CDC6C
50	–72	–80
100	–71	–75
500	–70	–63
1000	–69	–59

(1) Spur induced by 50mV power supply ripple applied to 50MHz LVCMOS output clock, VDD = 2.5V (LMK6C) or 2.5V/3.3V (CDC6C), no power supply decoupling capacitor

Alternatively, the LMK5B33216 can power an external XO to deliver low jitter outputs with noisy supplies. The LMK5B33216 is a network synchronizer and jitter cleaner with three DPLL and APLL pairs. Each VDD and VDDO pin includes an internal LDO, which improves the PSNR and minimizes output noise. Pin 22 (CAP1_APLL2) is the LDO output of APLL2 that can be used to power the XO, providing nominal 2.65V nominal and sourcing up to 20mA.

Test data on the Impact on the XO Phase Noise Performance using the LMK5B33216 is discussed in the respective section. The results show that CAP1_APLL2 has exceptional PSNR and provides a low jitter XO output regardless of the supply filter.

4 Consideration #2: XO Supply Filter

Another key factor is the power supply filter (such as capacitors, ferrite beads) used for the XO. Without proper filtering, the XO phase noise can degrade.

A power supply with a noise-reduction (NR) pin is recommended to lower XO supply noise. The supply can be an LDO or a switching DC/DC converter IC. The NR pin is necessary to connect a bypass capacitor to the supply voltage reference. Low-frequency (< 10kHz) noise is reduced with the RC filter formed from the bypass capacitor. In many TI power supplies, the capacitor is labeled as $C_{NR/SS}$ and sets the soft-start (SS) time. As an example, the TPS62913 is a DC/DC converter that has an NR pin available. Figure 4-1 shows the block diagram and highlights the NR pin.

Test data on the Impact on the Power Supply Performance and Impact on the XO Phase Noise Performance is discussed in the respective sections. The results show that a properly designed XO supply yields the best RMS jitter performance.

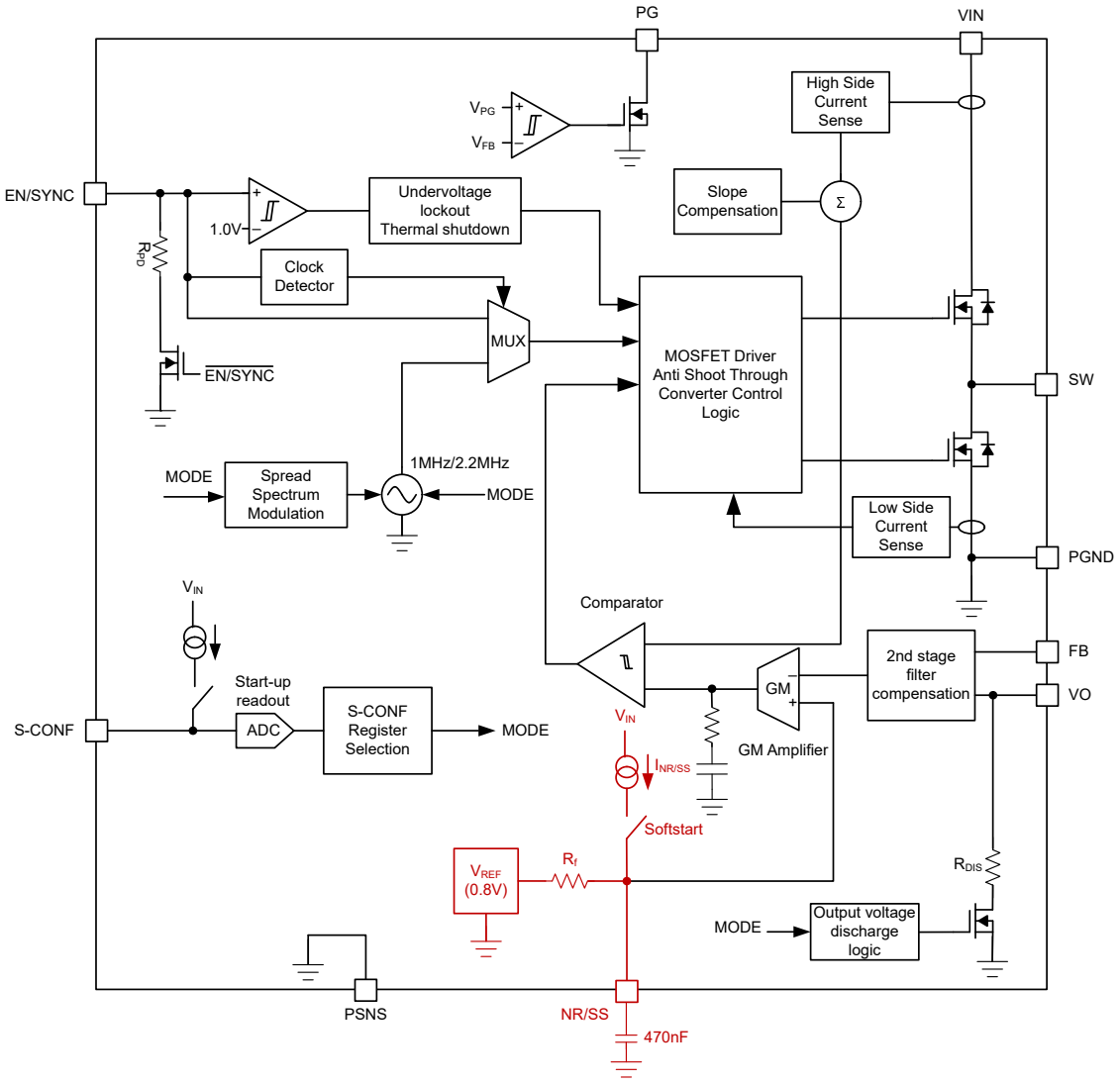


Figure 4-1. TPS62913 Functional Block Diagram

5 Consideration #3: APLL LBW

Another best practice is to use a high-performance PLL with a narrow LBW, such as the LMK5B33216, to reduce the impact of noisy XOs on PLL outputs. For further optimization, compare the noise profile of the XO, APLL, and VCO to determine the best APLL LBW setting.

The device can generate 156.25MHz outputs with 47fs typical RMS jitter using the Voltage Controlled BAW Oscillator (VCBO). Low noise outputs are achieved by operating the APLL with a narrow LBW, enabling the VCBO to dominate at phase noise offsets > 8kHz. Because of the VCBO, the device can use a high-jitter XO without degrading the PLL output jitter across 12kHz to 20MHz.

Test data on the *Impact on the PLL Phase Noise Performance* is discussed in the respective section. The results show that a narrow LBW setting yields the best RMS jitter performance when working with noisy XOs. Alternatively, clean XO outputs can be achieved regardless of the loop bandwidth when using the LMK5B33216 to power the XO.

6 Test Results Across Different XO Supply Filters

The following subsections provide test results for the three test conditions:

1. Different XO supply filters to see the Impact on the Power Supply Performance.
2. Different XO supply filters to see the Impact on the XO Phase Noise Performance.
3. Different XO supply filters to see the Impact on the PLL Phase Noise Performance.

6.1 Test Setup

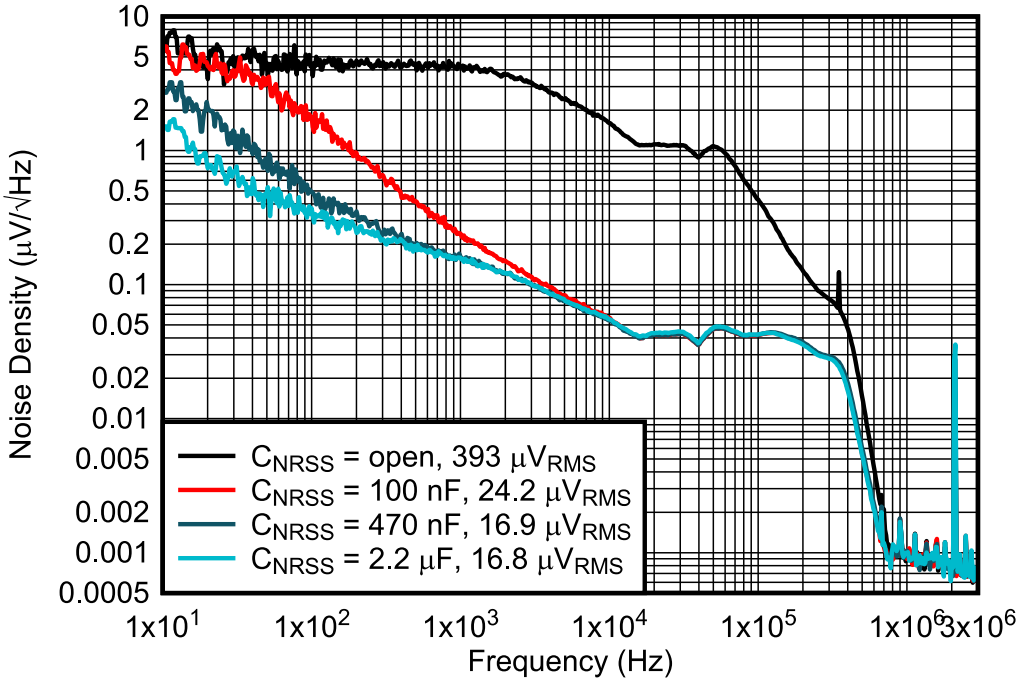
For each test, the $C_{NR/SS}$ value is adjusted to model different XO supply filters. Each value creates a unique XO noise profile. Table 6-1 lists the devices used in the tests.

Table 6-1. Parts Used for Testing

Vendor	Part Number	Description	Input Supply Voltage (v)	Output Supply Voltage (v)	Output Clock Swing (v)	Frequency [MHz]
TI	TPS62913	DC/DC Supply	12	3.3	—	2.2 (f_{SW})
TXC	8W48070009	XO	1.8 to 3.3	—	3.3	48 (f_{OUT})
TI	LMK5B33216	Network Synchronizer	3.3	—	0.8 (V_{OH}– V_{OL})	156.25 (f_{OUT})

6.2 Impact on the Power Supply Performance

The best XO and PLL output performance is achieved by properly designing the XO supply filter to reduce low-frequency noise. Figure 6-1 illustrates the output power noise density across different noise profiles. When the XO supply filter is missing (no $C_{NR/SS}$), the noise increases significantly between 100Hz and 100kHz. With the recommended 470nF filter value, the supply noise improves to 4.6µV/√Hz.

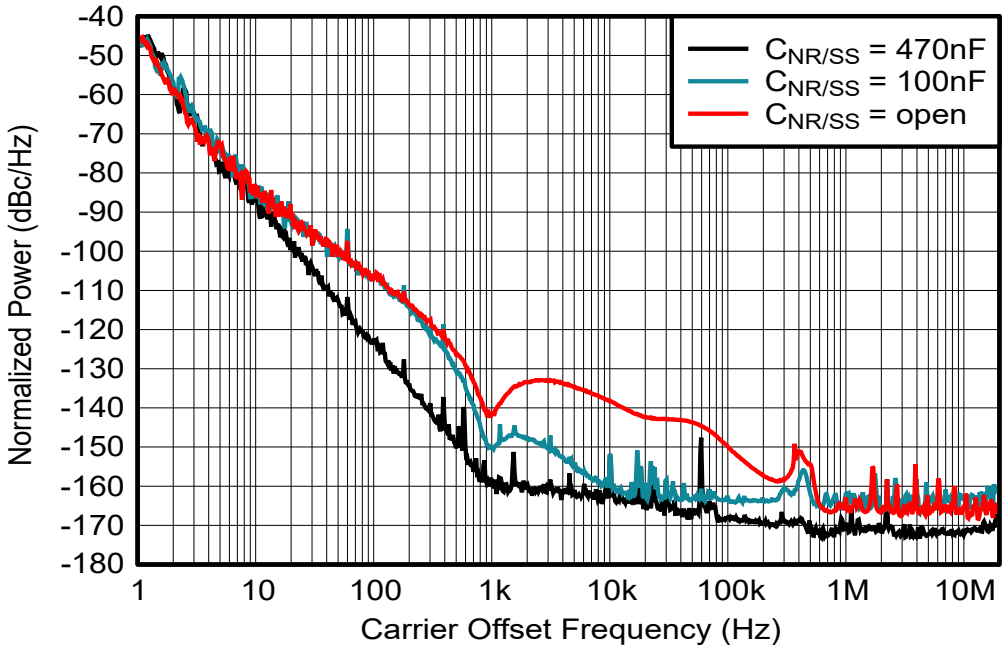


L = 2.2µH, f_{SW} = 2.2MHz, BW = 100Hz to 100kHz
The data is collected with a supply input voltage of 12V and an output voltage of 3.3V.
The noise is measured after the ferrite bead filter of V_{OUT} from TPS62913.

Figure 6-1. TPS62913 Power Supply Performance, $C_{NR/SS}$ Varied

6.3 Impact on the XO Phase Noise Performance

The effect of the XO supply filter is further examined by measuring the phase noise of the XO output clock. Figure 6-2 illustrates the phase noise across different noise profiles and Figure 6-3 provides the measurement setup. The RMS jitter more than doubles with little to no supply filtering. With the recommended 470nF filter value, the XO phase noise floor improves by 20dB across 1kHz to 100kHz offsets.



$C_{NR/SS}$ (nF)	RMS Jitter (Typical) Across 12kHz to 20MHz (fs)
470	62
100	152
0 (open)	158

Figure 6-2. XO Phase Noise, $C_{NR/SS}$ Varied, with TPS62913 supply

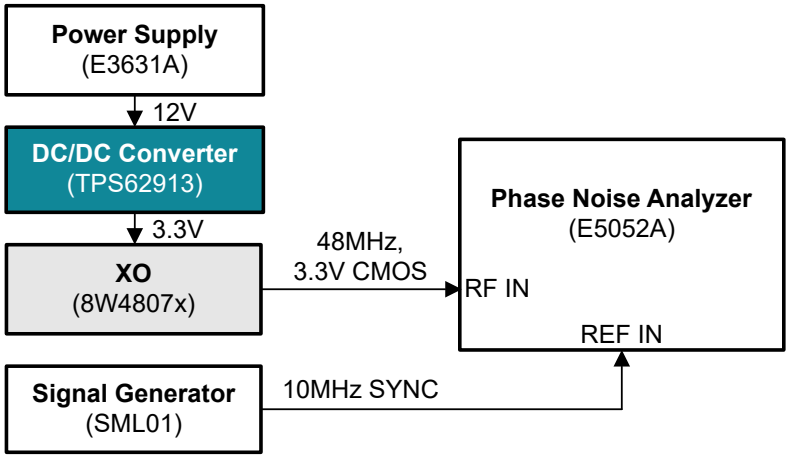
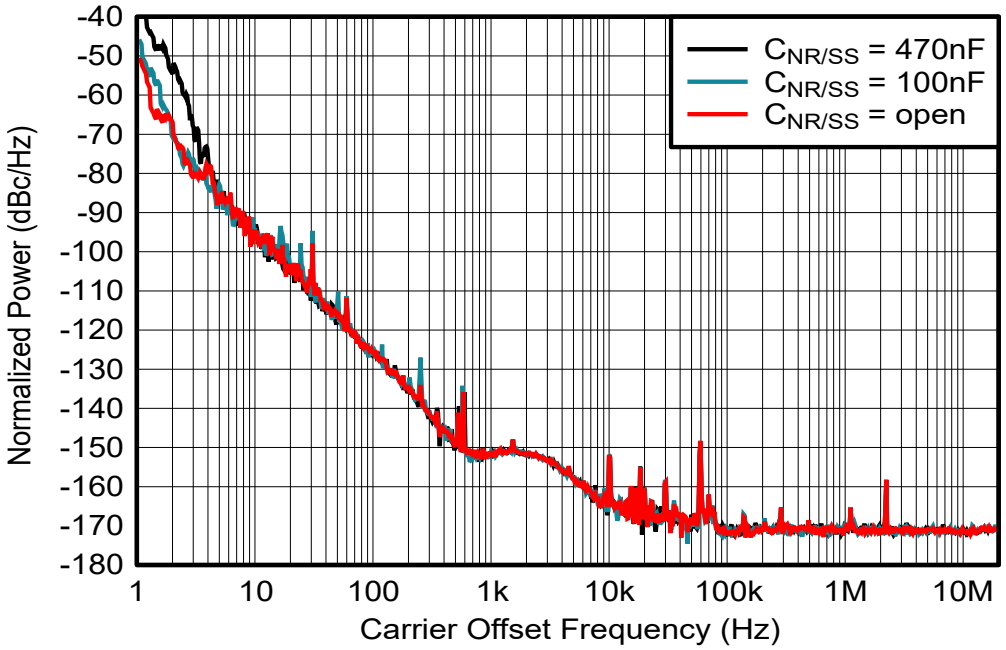


Figure 6-3. XO Test Setup With TPS62913 Supply

Low-noise XO outputs can be achieved regardless of the supply filter by using the LMK5B33216 to power the XO. Figure 6-4 shows the XO phase noise when powered by the LMK5B33216 and Figure 6-5 provides the test setup.



$C_{NR/SS}$ [nF]	RMS Jitter (typ) Across 12kHz to 20MHz [fs]
470	61
100	61
0 (open)	61

Figure 6-4. XO Phase Noise, $C_{NR/SS}$ Varied, With LMK5B33216 Supply

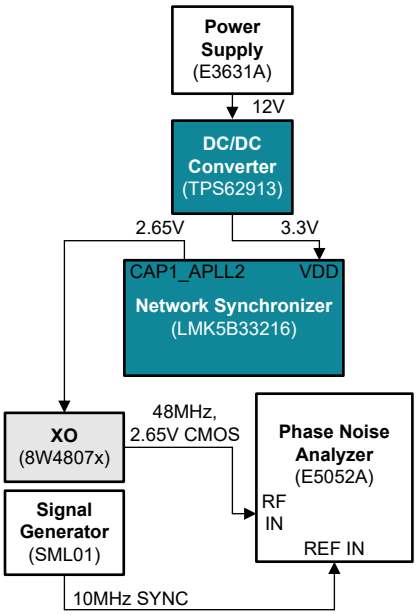
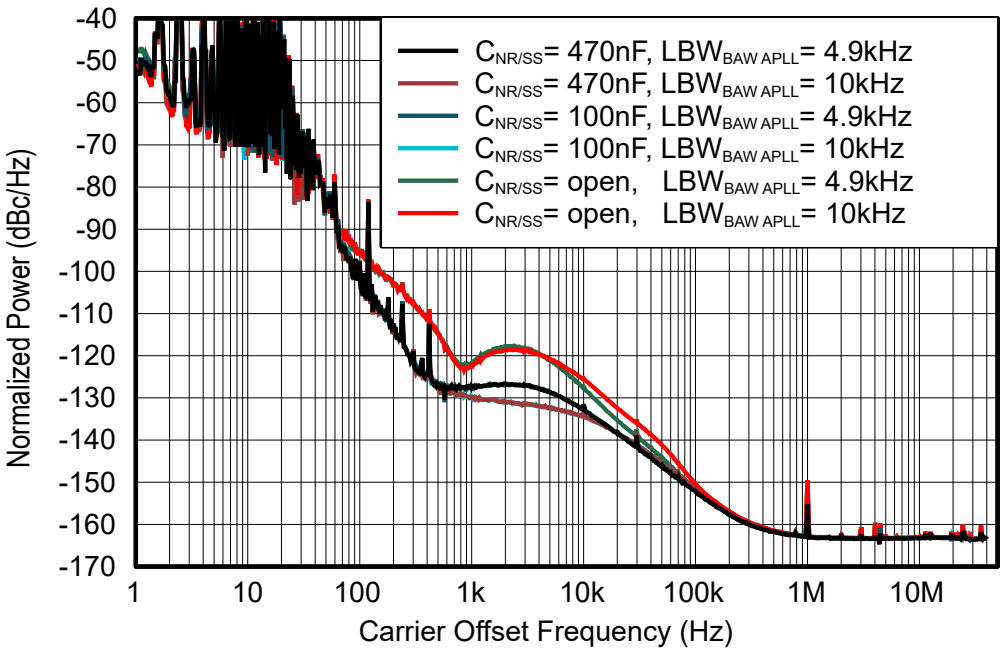


Figure 6-5. XO Test Setup With LMK5B33216 Supply

6.4 Impact on the PLL Phase Noise Performance

Figure 6-6 demonstrates that RMS jitter is minimally affected by a noisy XO supply ($C_{NR/SS}$ = open) when the APLL has a narrow APLL LBW. Figure 6-7 provides the measurement setup. The PLL output noise further improves (by 20fs) when a proper XO supply filter is used.



$C_{NR/SS}$ (nF)	$LBW_{BAW\ APLL}$ (kHz)	RMS Jitter (Typical) Across 12kHz to 20MHz (fs)
470	4.9	54
470	10	56
100	4.9	54
100	10	56
0 (open)	4.9	62
0 (open)	10	75

Figure 6-6. LMK5B33216 Phase Noise, $C_{NR/SS}$ Varied, XO With TPS62913 Supply

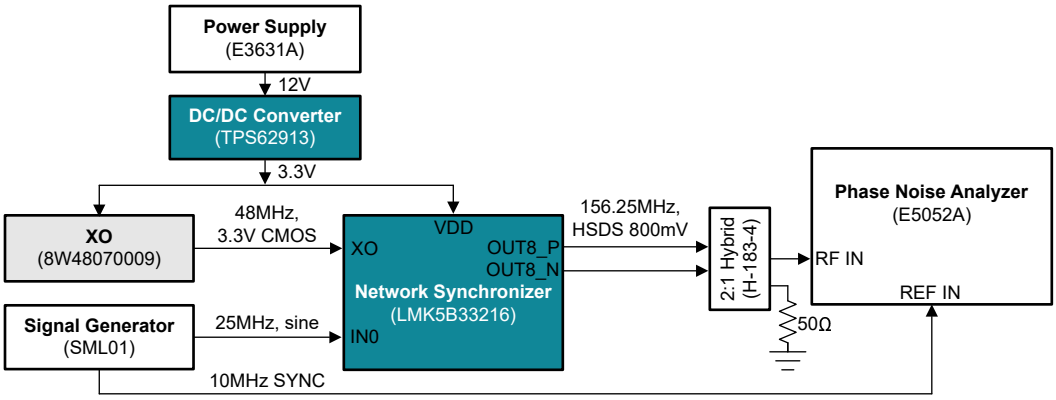
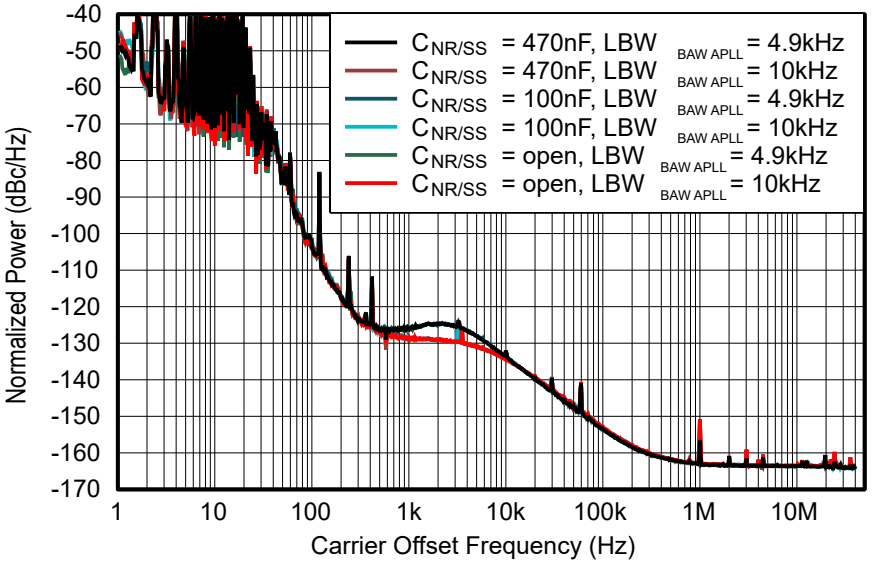


Figure 6-7. LMK5B33216 Test Setup, XO With TPS62913 Supply

Low-noise PLL outputs can be achieved regardless of the supply filter or loop bandwidth setting by using the LMK5B33216 to power the XO. Figure 6-8 shows the LMK5B33216 phase noise when powered by the LMK5B33216 and Figure 6-9 provides the test setup. The results show the negligible impact on PLL output jitter (between 12kHz and 20MHz offsets) when using a poor supply filter.



$C_{NR/SS}$ [nF]	$LBW_{BAW\ APLL}$ [kHz]	RMS Jitter (typ) Across 12kHz to 20MHz [fs]
470	4.9	51
470	10	52
100	4.9	51
100	10	52
0 (open)	4.9	51
0 (open)	10	52

Figure 6-8. LMK5B33216 Phase Noise, $C_{NR/SS}$ Varied, XO With LMK5B33216 Supply

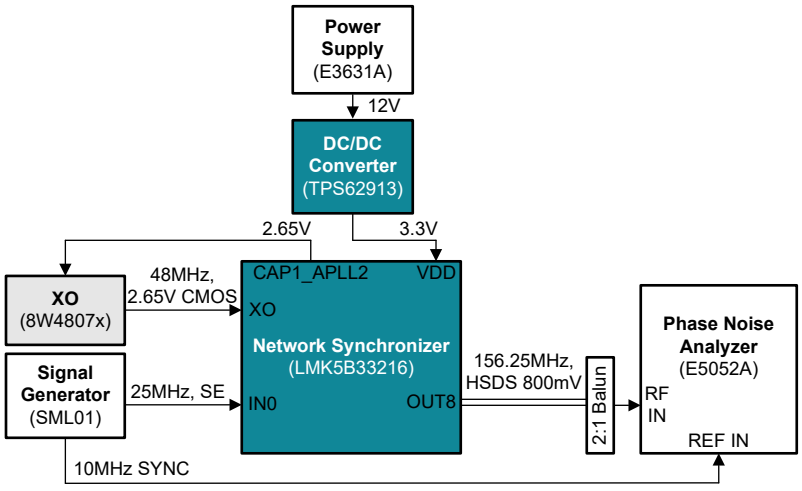


Figure 6-9. LMK5B33216 Test Setup, XO With LMK5B33216 Supply

7 Conclusion

The XO supply noise plays a major role in PLL clocking designs. The XO PSNR, XO supply filter, and the APLL LBW, strongly affect the PLL output phase noise. XOs with an integrated LDO, such as CDC6C or LMK6C, are highly recommended when a noisy XO supply cannot be avoided. PLLs with an integrated BAW VCO, such as the LMK5B33216, can be used with a narrow LBW to mitigate the XO noise impact. For seamless designs, use the LMK5B33216 to power the external XO and generate low jitter outputs regardless of the XO PSNR, supply filter, and APLL LBW.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025