User's Guide

LMK1C1104 Low-Additive, Phase-Noise LVCMOS Clock Buffer Evaluation Board

ABSTRACT

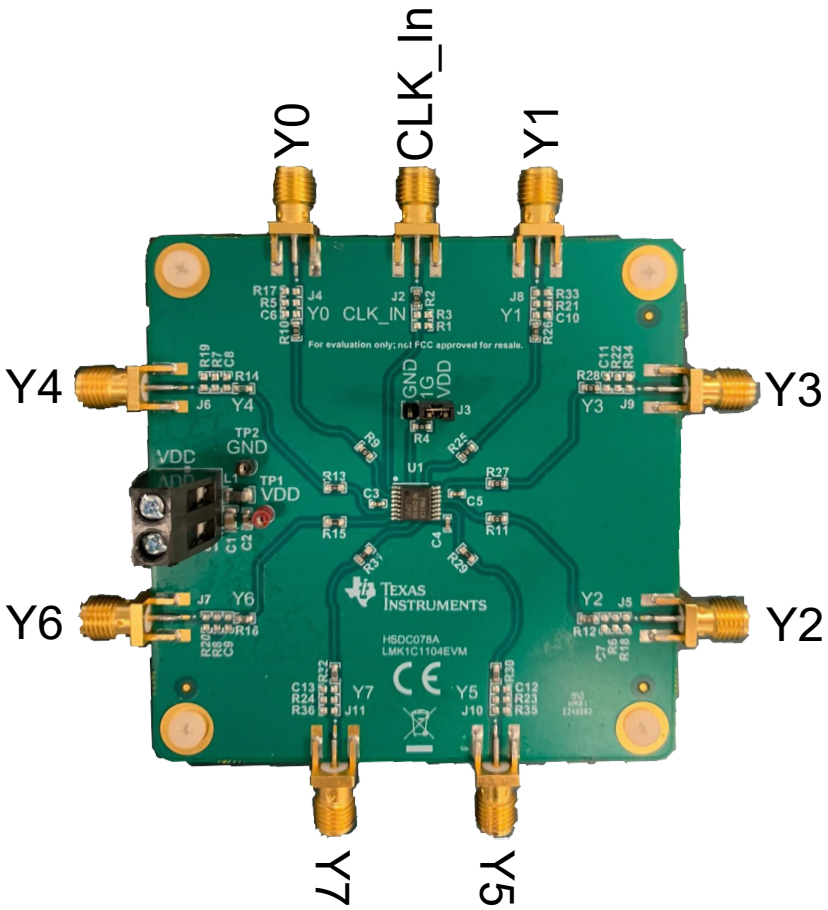

Figure 1-1. LMK1C1104EVM

The LMK1C1104 is a high-performance, low additive jitter LVCMOS clock buffer with one LVCMOS input, four LVCMOS outputs, and a global output enable pin.

This evaluation module (EVM) is designed to demonstrate the electrical performance of the LMK1C1104. Throughout this document, the acronym EVM and the phrases evaluation module and evaluation board are synonymous with the LMK1C1104EVM. Figure 8-1 illustrates the LMK1C1104EVM.

The LMK1C1104EVM is equipped with 50-Ω SMA connectors and impedance-controlled 50-Ω microstrip transmission lines for best performance.

Table of Contents

Trademarks

1 Features

- Easy-to-use evaluation board to fan out up to four LVCMOS clocks with low phase noise/jitter
- Output enable pin configurable through jumper
- Board powered from a single 3.3-V / 2.5-V / 1.8-V supply
- Clock output traces are length matched

2 Signal Path and Control Circuitry

The LMK1C1104EVM supports single-ended inputs up to 250 MHz. For more information about the LMK1C1104, see the LMK1C1104 product data sheet available for download from the TI Web site (www.ti.com).

3 Getting Started

The LMK1C1104EVM has self-explanatory labeling and uses similar naming conventions as the LMK1C1104 product data sheet. In this user's guide, all words in **boldface** reflect the actual labeling on the EVM.

4 Power-Supply Connections

Connect the power-supply source and ground to the terminal block labeled **J1** as shown in Figure 4-1. Alternatively, connect the power-supply source to **TP1**, and connect the ground of the power-supply **TP2**. Decoupling capacitors and a ferrite bead isolate the EVM power from the LMK1C1104 device power pins.

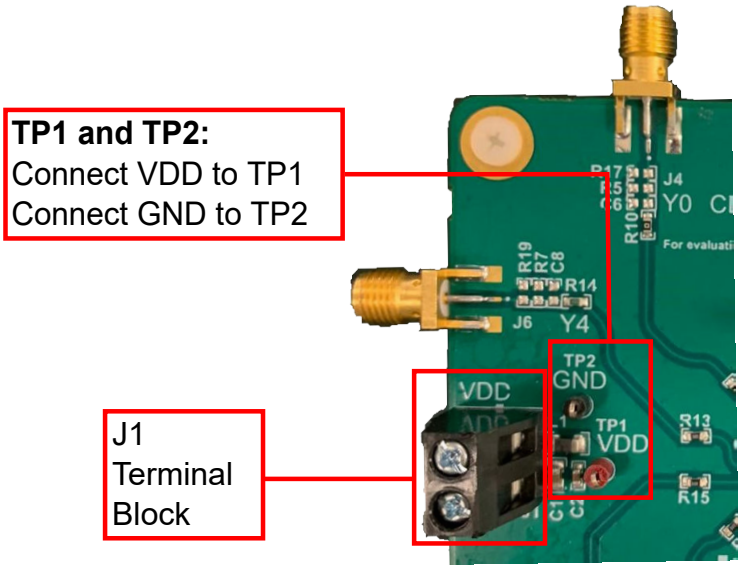

Figure 4-1. Power Supply Connection Locations

The LMK1C1104EVM operates from a single 3.3-V / 2.5-V / 1.8-V supply.

5 Enabling/Disabling the Outputs

The enable pin, 1G, of the LMK1C1104 can be controlled using jumper **J3**. Pull 1G to VDD by shunting pins 2 and 3 of J3 to enable the outputs as shown in Figure 5-1. Leave 1G floating or pull to GND to disable the outputs.

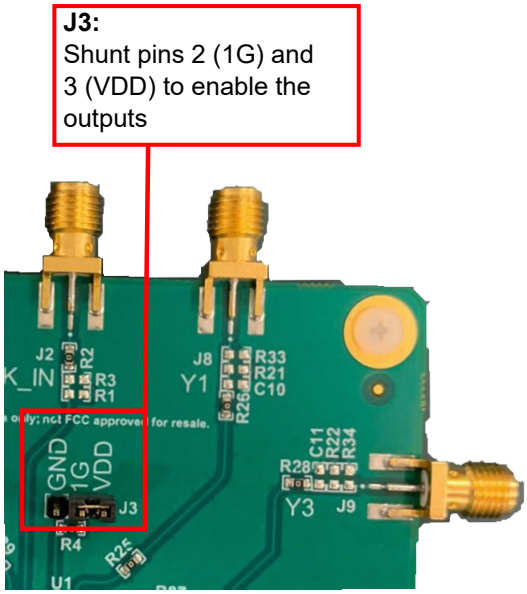

Figure 5-1. J3 Jumper Location

By default, a shunt is placed on pins 2 and 3 to enable the outputs.

6 Output Clock

The LMK1C1104 fans out four LVCMOS outputs. The outputs can be loaded using the pullup and pulldown footprints. No resistor has been soldered in those footprints.

The EVM board supports up to eight clock outputs for pin-compatible TSSOP packaged devices in the industry standard footprint. The LMK1C1104 uses four of the 8 outputs shown in Figure 1-1. These outputs are Y0, Y1, Y2, and Y3.

7 Bill of Materials

7.1 REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation we are notifying you that this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are:

Table 7-1. REACH SVHC

COMPONENT MANUFACTURER	COMPONENT TYPE	COMPONENT PART NUMBER	SVHC SUBSTANCE	SVHC CAS (WHEN AVAILABLE)
Molex	5.08 Pitch Eurostyle Vertical Fixed Mount PCB Terminal Block, 2 Circuits	039544-3002	Lead	7439-92-1

Table 7-2. Bill of Materials

DESIGNATOR	QTY	VALUE	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1	1	10uF	0805	C0805C106K8PACTU	Kemet
C2	1	1uF	0603	C0603X105J8RAC7867	Kemet
C3, C4, C5	3	0.1uF	0402	C0402C104K8RACAUTO	Kemet
H1, H2, H3, H4	4	4-40/0.25"	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4	0.5"	Standoff	1902C	Keystone
J1	1	Terminal Block	TH	039544-3002	Molex
J2, J4, J5, J8, J9	5	CON-SMA-EDGE-S	RF SMA EDGE	CON-SMA-EDGE-S	RF Solutions Ltd.
J3	1	1x3	0.1 in.	PBC03SAAN	Sullins Connector Solutions
L1	1	50Ω	1206	BLM31SN500SZ1L	MuRata
R2, R4, R9, R10, R11, R12, R25, R26, R27, R28	10	0Ω	0603	RC0603JR-070RL	Yageo
SH1	1	1x2	Shunt	SNT-100-BK-G	Samtec
TP1	1	Red Test Point	TH	5000	Keystone
TP2	1	Black Test Point	TH	5001	Keystone
U1	1	LMK1C1104	8-TSSOP	LMK1C1104PW	Texas Instruments
C6, C7, C10, C11	4	5pF	0603	GRM1885C2A5R0CA01D	MuRata
R1, R3, R5, R6, R17, R18, R21, R22, R33, R34	10	100Ω	0603	CRCW0603100RFKEA	Vishay-Dale

8 Schematic

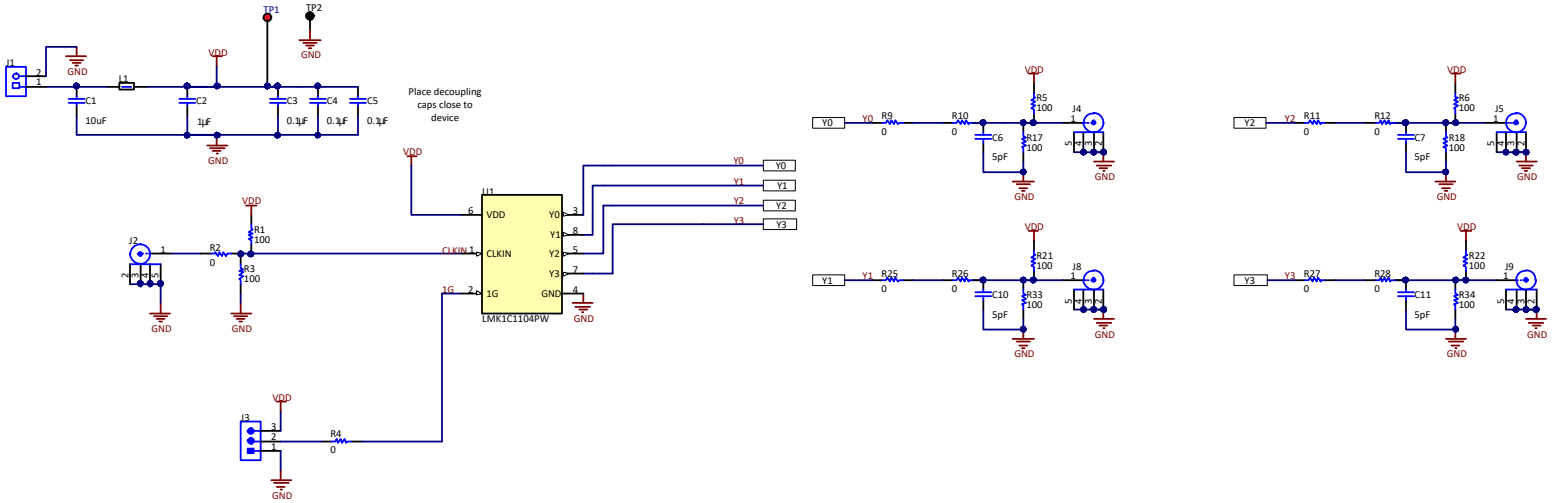

Figure 8-1. LMK1C1104 Schematic

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Removed 1.5-V supply option	2
• Added Figure 4-1	3
• Added Figure 5-1	3
• Added content to the *Output Clock* section	4
• Changed Table 7-2	4
• Changed Figure 8-1	5

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