Application Note

Precautions for LM636XX-Q1: Regarding a Failure Analysis in PFM Mode

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ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAG45)

LM636XX-Q1 is widely used in automotive applications such as automotive cabin, ADAS and body. This application note is intended to help users understand EOS (Electrical Overstress) failure cases in common applications. It details how to identify the root cause of chip failure through step-by-step analysis, and how to validate failure analysis conclusions through laboratory testing and mass production design validation. Ultimately, this drives chip design optimization to accommodate more application scenarios, refines chip design, and helps users develop more stable systems.

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1 Profile

LM636XX-Q1, a widely used Tier 1 Buck product in TI automotive system, supports 3.5V-36V input voltages. It accommodates voltage fluctuations from automotive 12V batteries during load dump conditions, withstanding up to 42V (WSON package). Featuring a low quiescent current of 23μA and supporting spread spectrum function, all current-rated products within the same series are pin-compatible (LM63610-Q1/LM63615-Q1/LM63625-Q1/LM63635-Q1). In the automotive cabin, external amplifier audio, ADAS and body modules are illustrated in following Figure 1-1 smart cabin architecture block diagram:

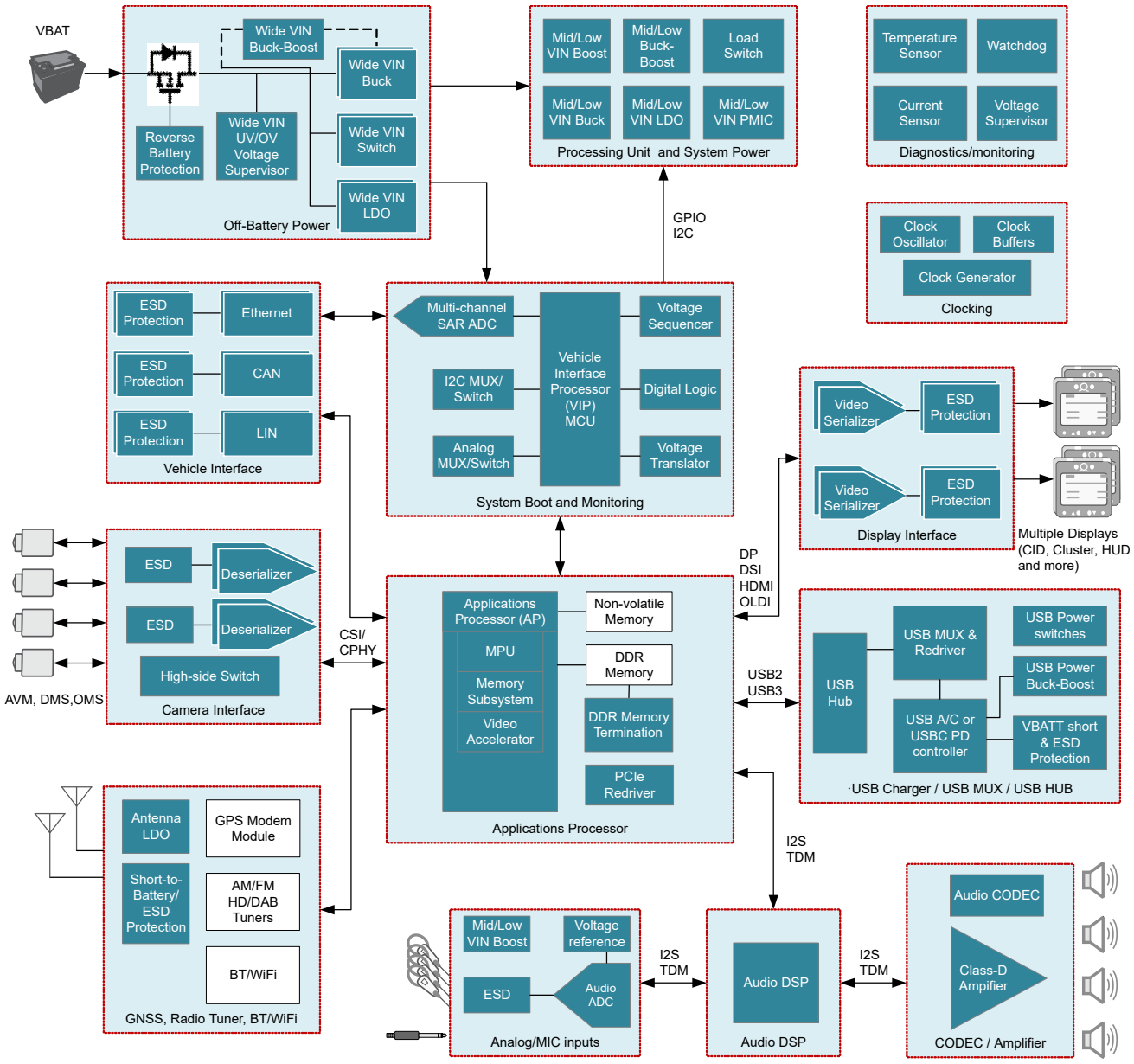

Figure 1-1. Digital smart cabin systems

The power module in the cabin carries the power supply of the entire system. The power chip inevitably suffers from various failures, and it is important to optimize the system design or chip design to find the root cause of each failure.

2 Generation of the reverse current

Reverse current is a common phenomenon for Buck topologies. When significant reverse current scenarios exist during operation, there is a risk of MOSFET failure. This failure, commonly referred to as EOS failure or Electrical Overstress, refers to the damage incurred when a chip endures voltage or current exceeding its tolerance limits. Such damage is typically triggered by overloads lasting from several microseconds to several seconds. For a failure analysis (FA, Failure Analysis) of a chip, the reported conclusion of FA for most cases may be EOS, but EOS is the result of silicon characterization, not the root cause of the problem. Numerous factors may precipitate EOS, including unreasonable application scenarios, schematic diagram/Layout design flaws, issues stemming from chip robustness, failures caused by abnormal power supply or load conditions, or a combination of multiple problems. This section examines a real-world failure case to elucidate the failure analysis process. The primary culprit of the failure in this case is reverse current. First we need to understand what the reverse current is. When the load current decreases, the inductor current can drop below zero. If the lower transistor MOSFET fails to switch off promptly, the output voltage will exceed the switch node voltage, causing current to flow back through the inductor from the output terminal, thereby generating negative current. There are several main conditions on the formation of reverse current:

- Higher output voltage, or smaller input-output voltage differential;
- Excessive output capacitance;
- The input voltage drops out faster than the output;
- Other loads draw high currents, resulting in lower input voltages;
- Prolonged operation in PFM mode.

3 EOS failure case

Application scenario: LM63635-Q1, Vin= BAT(6-16V), Vout=8V, Iout<1.5A, FSW=2100K, Auto Mode

The failure case presented in this chapter originates from an automotive smart cabin application, where the load is a POC (Power over Coax) load such as an automotive 360 surround view/dashcam. These represent short-duration high-load scenarios, though the majority of operational conditions involve light-load mode (PFM). The power supply is shown in Figure 3-1:

Figure 3-1. POC application block diagram

First, a visual comparison between intact and failed chips is presented below Figure 3-2:

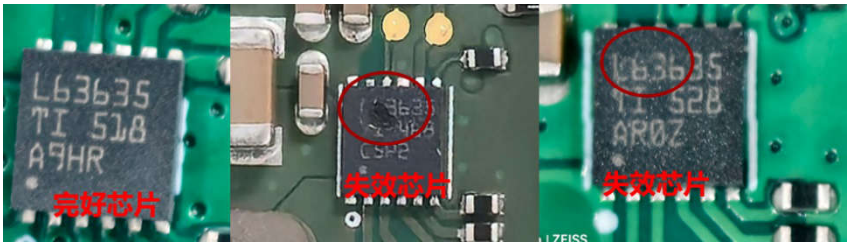

Figure 3-2. Failed chip appearance comparison

From the failure appearance, we can see that the failure of EOS occurs in the same part of the chip. 8D is reported as follows Figure 3-3. The post-failure analysis of the decapsulated chip reveals strikingly similar failure patterns: failures are concentrated at PIN1 (SW) Short to GND, PIN3 (VCC) Short to GND, PIN12 (VIN) OPEN, with a minor occurrence at PIN2 (BOOT) Short to GND. Concurrently, the visible damage on the failed chips indicates the failure originates from VIN bonding wire fusing.

- **External Package Examination:**

  External visual inspection with 50x magnification showed blown package in area of pin 12 (VIN).

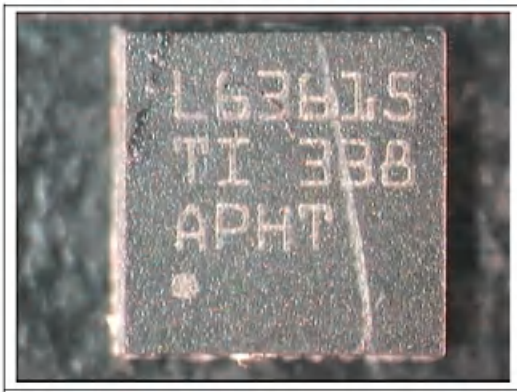

Figure 1. Unit 1. Top view

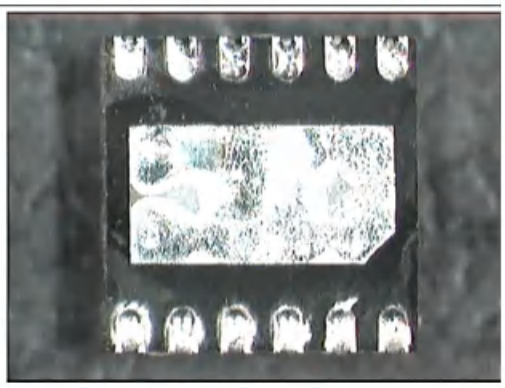

Figure 2. Unit 1. Bottom view

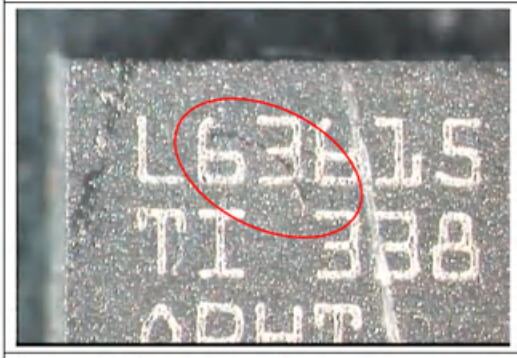

Figure 3. Unit 1. Blown package in area of pin 12

X-ray analysis evidenced melted bond wires of pin 12 (VIN)

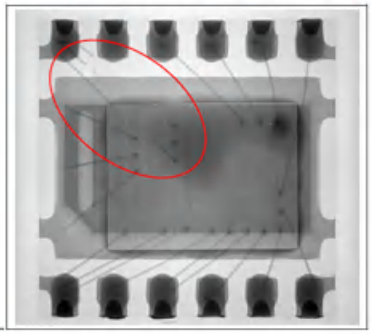

Figure 3-3. Decapsulation analysis in 8D report

The design schematic diagram for this case fully follows the reference application design of the data sheet as shown in Figure 3-4. Considering the application scenario and failure manifestations, analysis suggests possible cross-conduction between the upper and lower transistors. Multiple causes could trigger cross-conduction, for example, control logic failure caused by VCC noise may lead to the simultaneous conduction of the high-side and low-side MOSFET, while reverse current leads to stress damage. Only a direct connection between the two transistors would cause a substantial current in the Bonding wire, leading to a fusing.

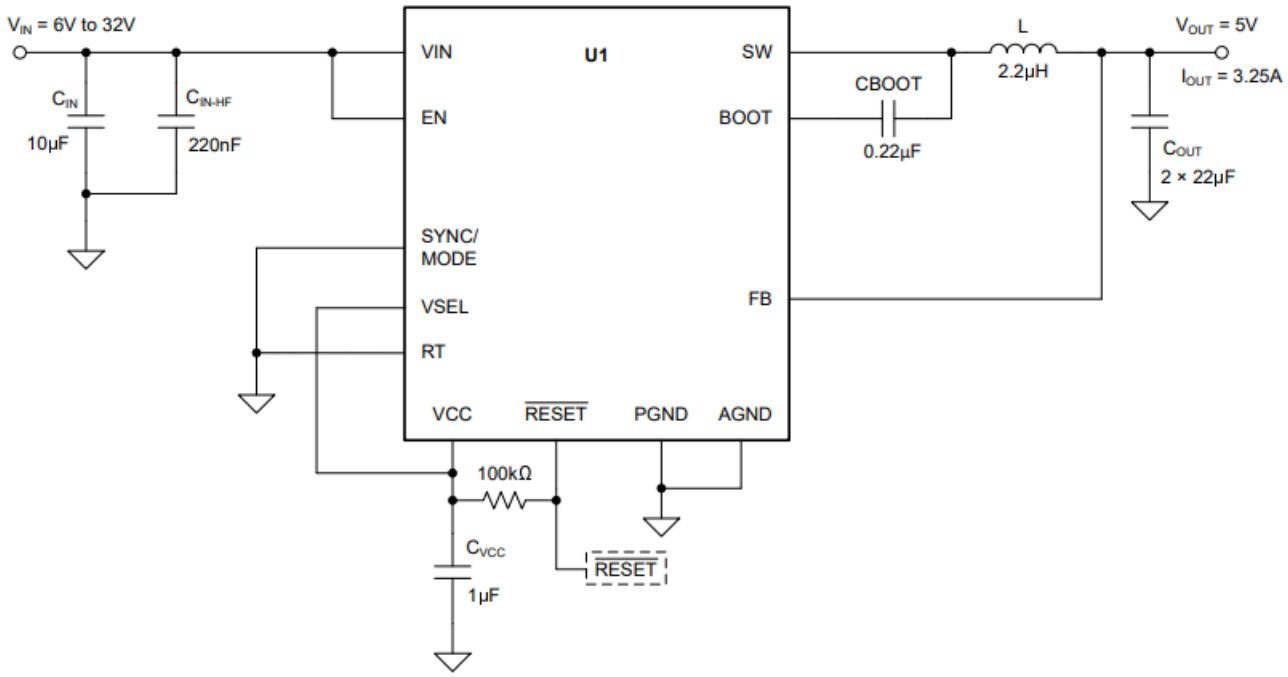

图 8-1. 示例应用电路 V_{IN} = 12V、V_{OUT} = 5V、I_{OUT} = 3.25A、f_{SW} = 2.1MHz

Figure 3-4. LM636XX-Q1 reference design

4 Potential cause

VCC is especially important for the logic work of the chip, and the irrational design of VCC can introduce noise. Any noise can affect the logic error of the control, thereby creating a risk of cross-conduction. VCC acts as the charge capacitance for CBOOT, and CBOOT acts as the bias voltage for the upper transistor driver in the half-bridge. This plays a vital role in the control logic.

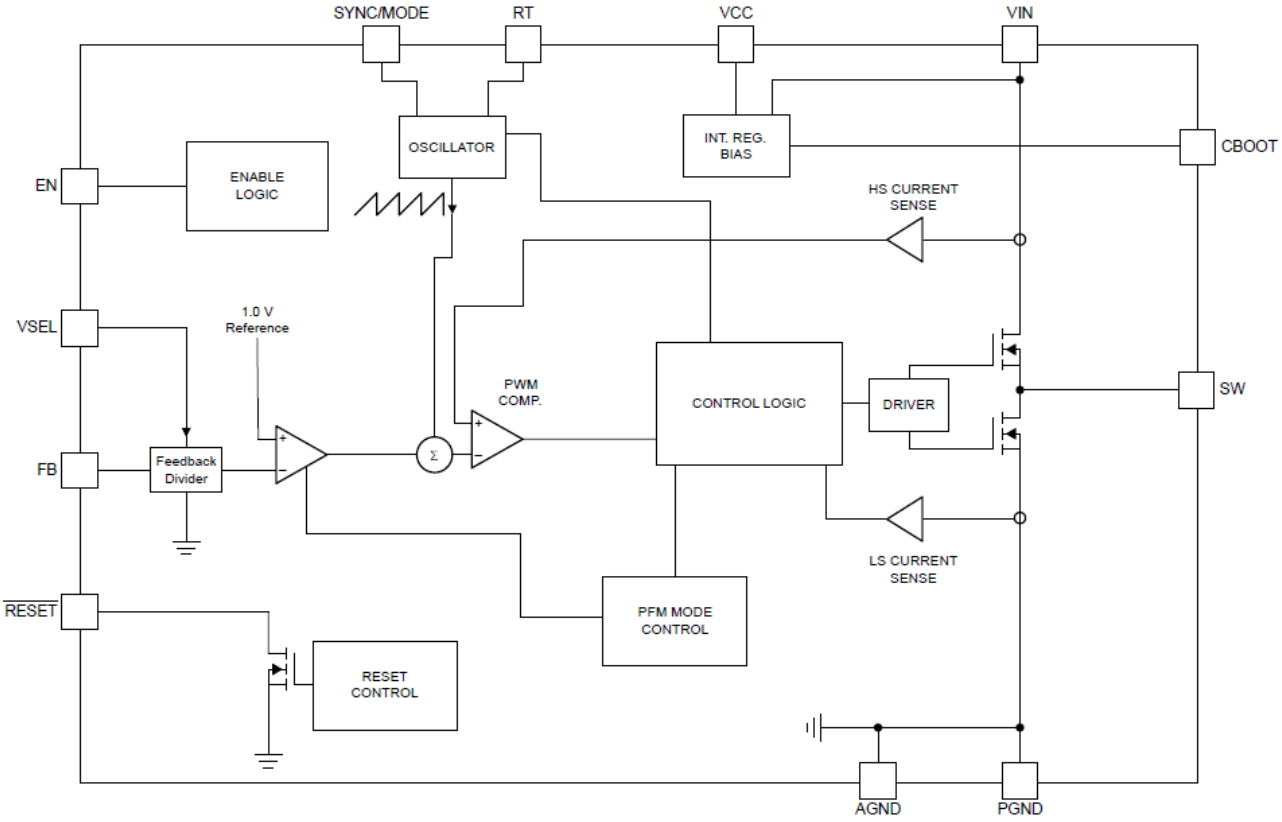

Figure 4-1. LM63635-Q1 function block diagram

It can be seen from Figure 4-1 that VCC is taken from the VIN linear buck, and any noise from VIN can be conducted to VCC. As shown in Figure 4-2, TI recommends avoiding any external circuitry connected to VCC while adding a 1uF high-quality capacitor for decoupling and filtering. Refer to LM63635-Q1EVM for guidance, using X7R MLCC capacitor.

8.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1µF, 16V ceramic capacitor connected from VCC to PGND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the $\overline{\text{RESET}}$ function and as a logic supply for the various control inputs of the device. A value of 100kΩ is a good choice for the $\overline{\text{RESET}}$ flag pullup resistor. The nominal output voltage on VCC is 5V.

Figure 4-2. LM63635-Q1 data sheet VCC design recommendations

For layout design, TI recommends placing a VCC bypass capacitor close to the VCC pin. This capacitor must be placed as close to the device as possible with short and wide traces to VCC and PGND pins. It is not recommended for thermal dissipation in this area.

Following a rigorous review of the schematic diagram and layout design by TI's product line for this case, the design is found to fully comply with the schematic diagram and layout specifications. This essentially rules

out control logic anomalies arising from an unreasonable VCC design. Consequently, the failure will now be analyzed from the perspective of reverse current.

5 EVM test

Given the low failure rate in this case, capturing abnormal waveforms during failure events proved impossible. Instead, EVM test is employed to detect potential reverse currents for verification, with test conditions precisely replicating the case scenario.

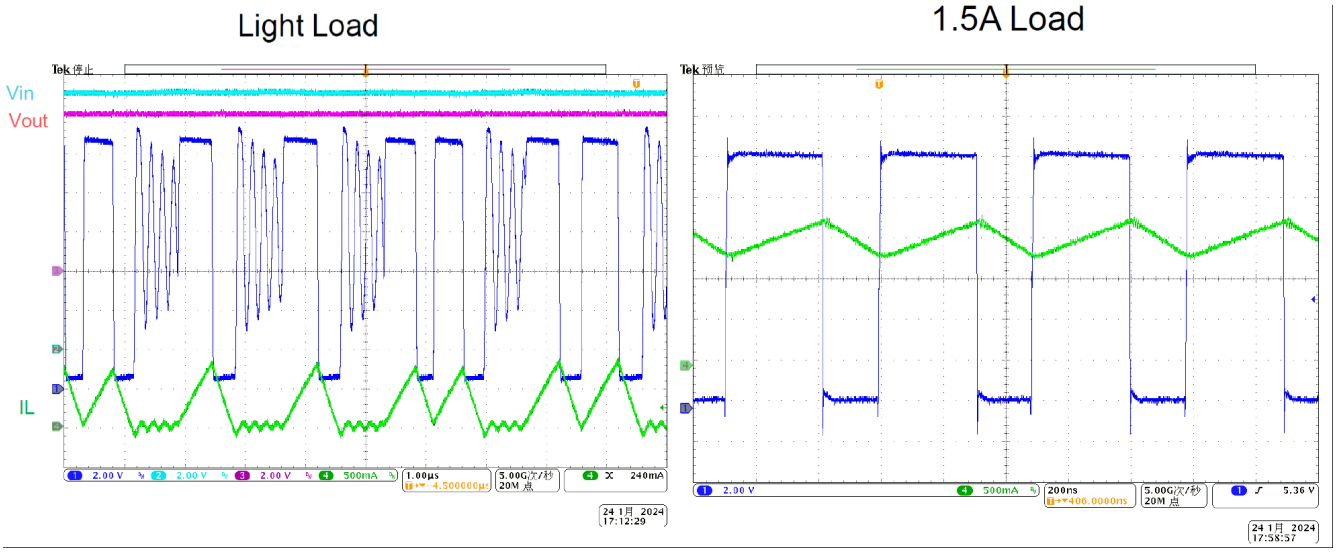

Figure 5-1. Normal operation waveform

As can be seen above Figure 5-1, a distinct frequency reduction occurs under light load conditions. This mechanism conserves switching losses by lowering the switching frequency during light load operation. The chip functions normally without any abnormal waveforms detected. Subsequently, to simulate conditions conducive to reverse current generation, specifically rapid input voltage de-energisation coupled with slow output voltage decay, the following waveforms are captured Figure 5-2:

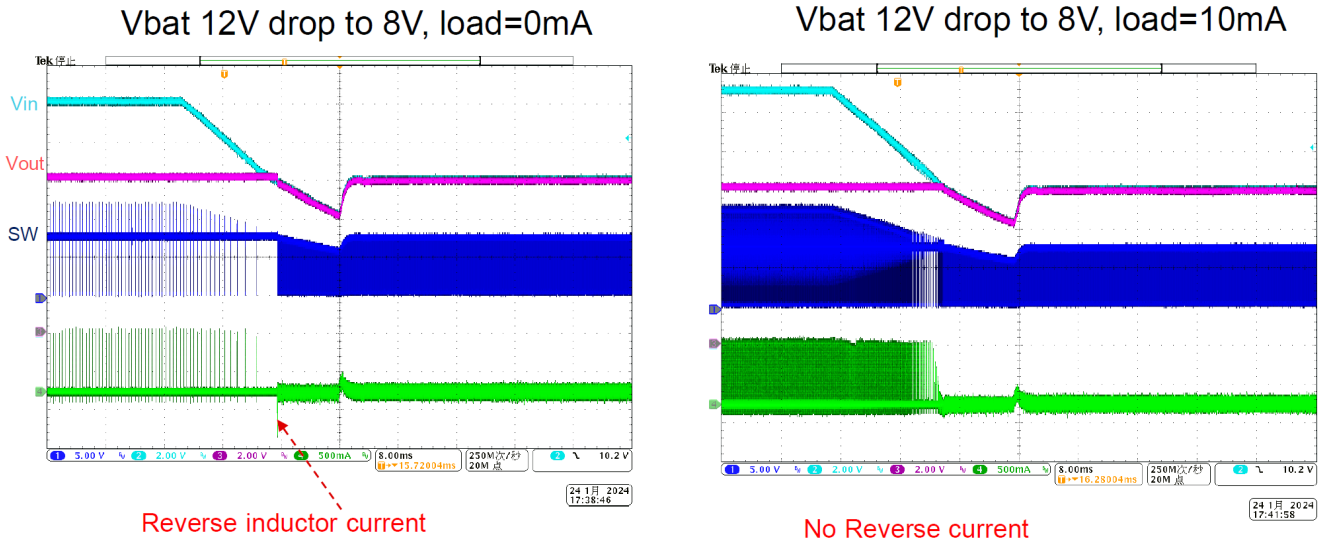

Figure 5-2. No-load versus loaded test waveforms

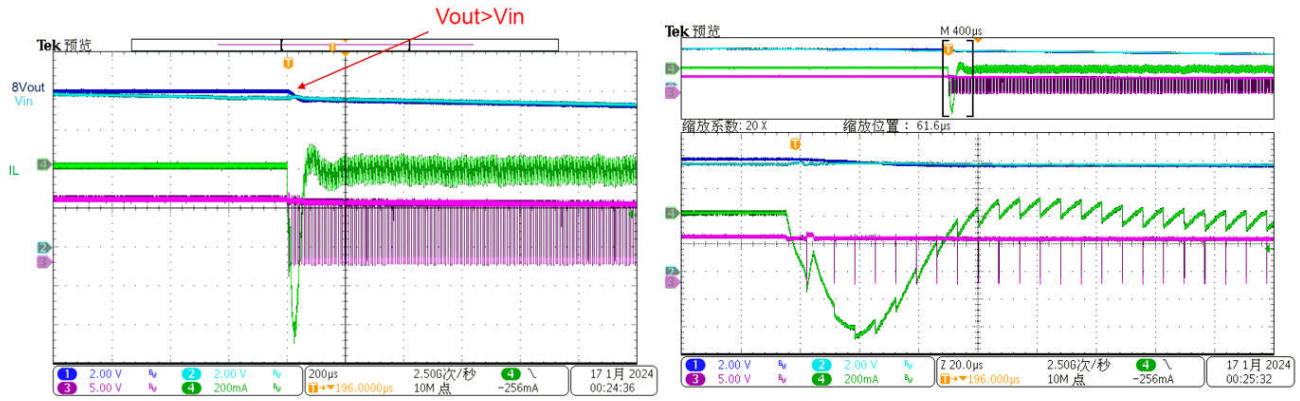

Figure 5-3. Amplify waveform

It can be seen from Figure 5-2 and Figure 5-3 test waveform results that under near-no-load conditions, the input voltage rapidly drops. While the output voltage is sustained by the large capacitance, a distinct transient reverse current is visible across the inductor. This transient current poses a risk of breakdown to the lower transistor MOSFET.

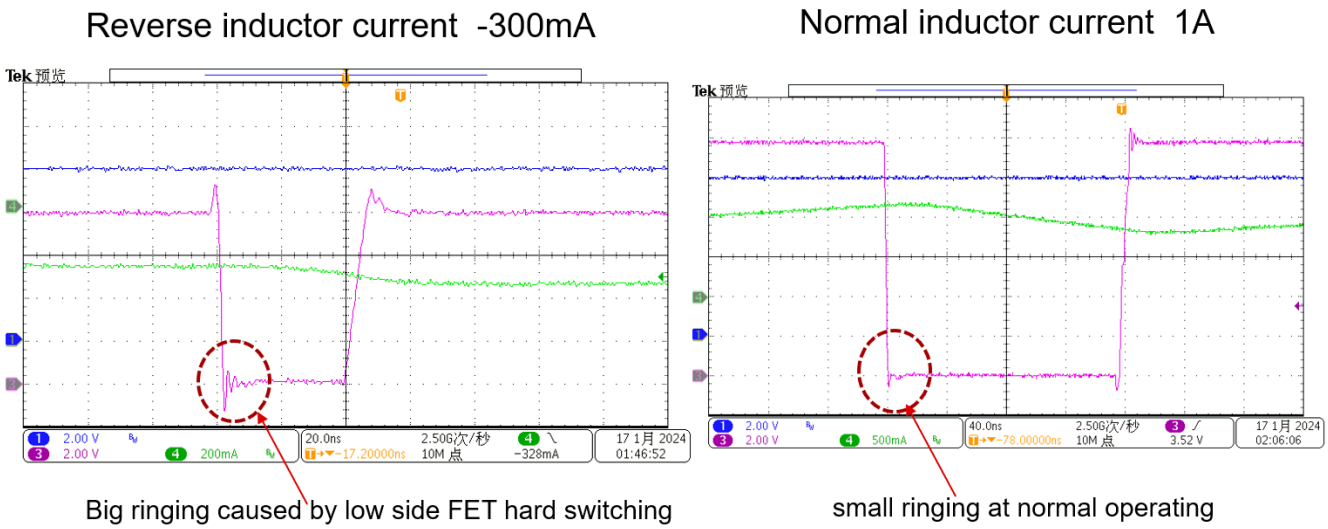

Figure 5-4. Lower transistor waveform

-300mA reverse current, coupled with ns level switching speed, generates substantial di/dt. This results in significant voltage formation at both sides of the lower transistor, posing a considerable risk of breakdown to the lower transistor MOSFET. However, due to individual variations in chip performance, stress tolerance differs among lower transistor MOSFET. Consequently, chips falling within the normal distribution of production margins may prove unable to withstand this immense stress and fail.

As an example, use the measured reverse current of -300mA (di=300mA), and considering LM636X5-Q1 as a converter product. Taking MOSFET (SQ7414AEN) used in LM25141 EVM as a reference, with rise time max dt=14ns, and based on the empirical value for parasitic inductance in Buck topologies typically ranging at 1-5nH, calculations are performed using the midpoint value L=3nH:

U=(di/dt)*L ≈ 64.3V. The chip's VDS withstand voltage is 60V, exceeding the stress tolerance of MOS, so this reverse current is at risk of damaging MOS. In practical applications, both the parasitic inductance and the rapid di/dt exert significant influence on the reverse voltage induced by the reverse current. This requires careful consideration in the design.

6 Reverse current generation and failure process

In the above text, the above tests conducted through the EVM find that there is indeed a large reverse current in the current application. While the chip on EVM is not damaged, large sample sizes can significantly increase the risk of breakdown due to reverse current. This chapter details how reverse current causes instantaneous failure during the switching process of a buck converter, along with the complete failure sequence.

(1) Q1 turn-on and dead-time phase

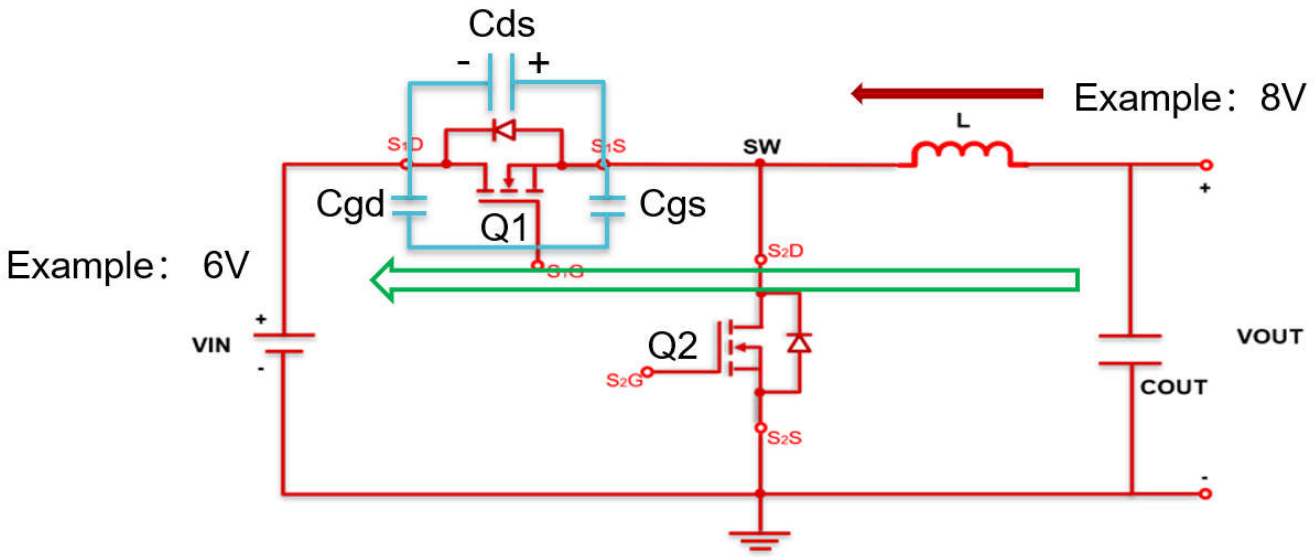

Figure 6-1. Q1 turn-on and dead-time phase

At power down or when the input falls below the output, the reverse current path is VOUT-> SW-> Q1 body diode-> VIN. During this phase, Cds is charged.

- When the upper transistor Q1 turns on, the lower transistor Q2 turns off, Cds is charged and the reverse current flows to VIN;
- When the upper transistor Q1 turns off, the lower transistor Q2 turns on and a reverse current flows from the lower transistor into GND for discharging.
- During the dead time, reverse current flows towards VIN via the body diode of upper transistor Q1, whilst Cds is simultaneously charged.

(2) Phase at which Q1 turns off and Q2 turns on

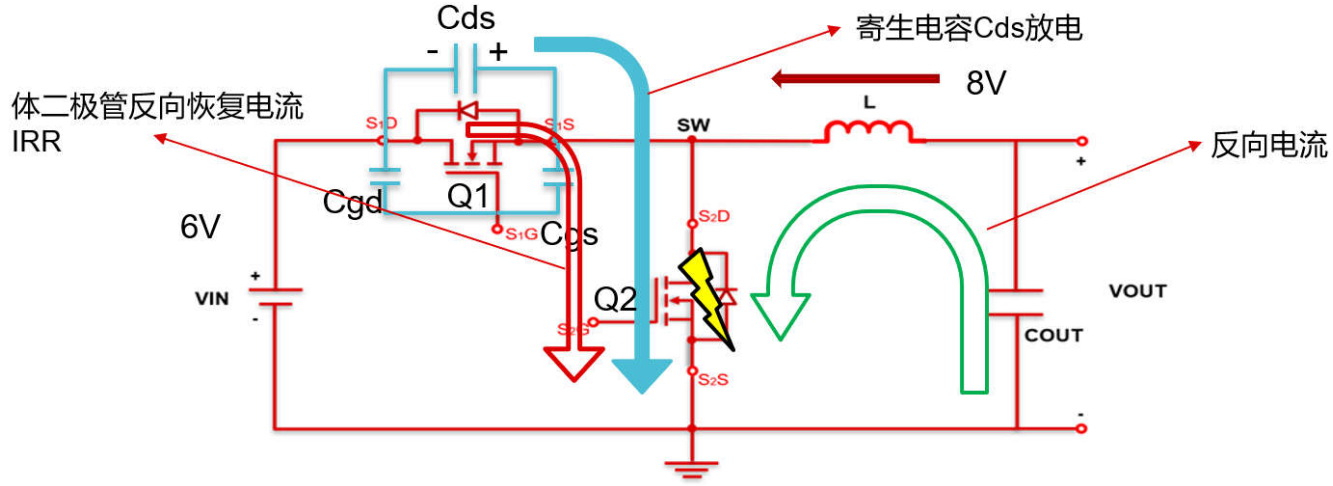

Figure 6-2. Phase at which Q1 turns off and Q2 turns on

When upper transistor Q1 turns off and lower transistor Q2 turns on:

- At this point, in addition to the reverse current of the output;
- Cds charged during Q1 turn-on phase and dead-time phase simultaneously discharges through the lower transistor;
- Reverse recovery current from the body diode conducting during dead time is also discharged by the lower transistor conduction.

Generally, the turn-on time of the lower transistor is at **ns** level. Consequently, calculations indicate that even with reverse currents of merely several hundred mA, **di/dt** variation becomes substantial enough to reach levels capable of damaging the lower transistor MOSFET.

(3) Failure process analysis

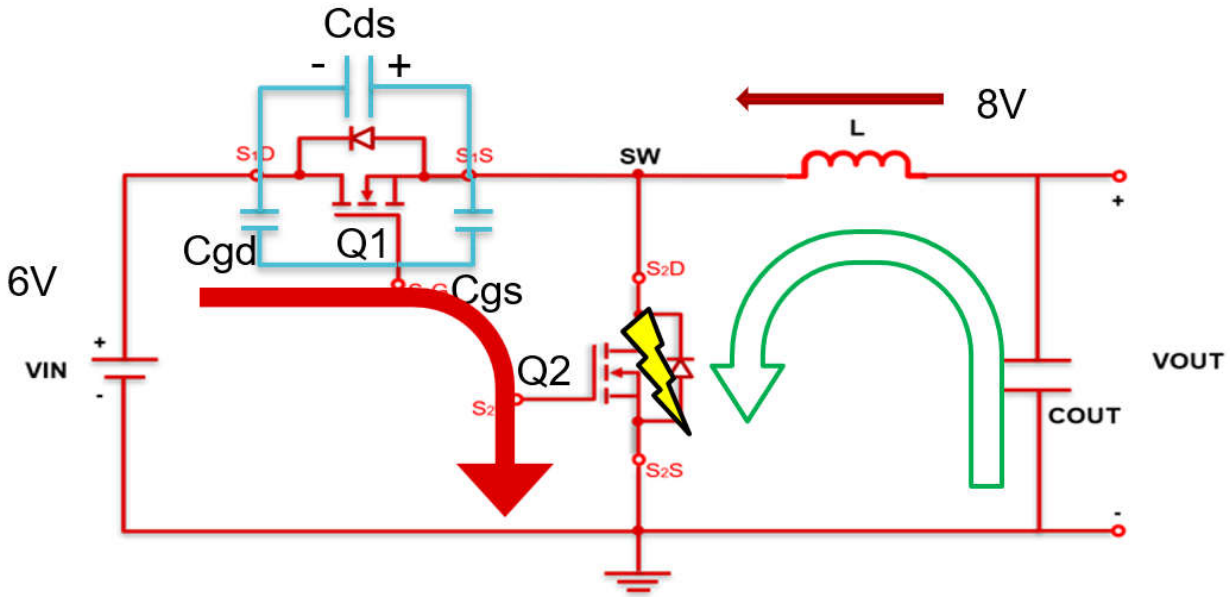

Figure 6-3. Lower transistor failure

- **PIN12:** Due to substantial di/dt, the lower transistor MOSFET fails, manifesting as a short circuit. Following the rapid connection of VOUT to GND, the output drops sharply. At this point, the upper transistor conducts, causing VIN to be directly shorted to GND. The resulting massive short-circuit current directly burns through VIN bonding wire on DIE, resulting in the failure symptom where VIN is displayed as OPEN.
- **PIN3:** VCC is an internal LDO PIN directly sourcing power from VIN to buck for internal logic supply. A VIN short-circuit device's immense current breaks down the internal LDO, causing VCC short-circuit.
- **PIN1:** SW exhibits failure as a short to GND due to the lower transistor short-circuit.

Additionally, some failures manifest as BOOT PIN short-circuits. This can be explained by the substantial di/dt simultaneously creating Figure 6-4 a significant potential difference across the BOOT capacitor. When this potential difference exceeds the breakdown voltage of BOOT capacitor, it forms a short-circuit loop with VCC breakdown.

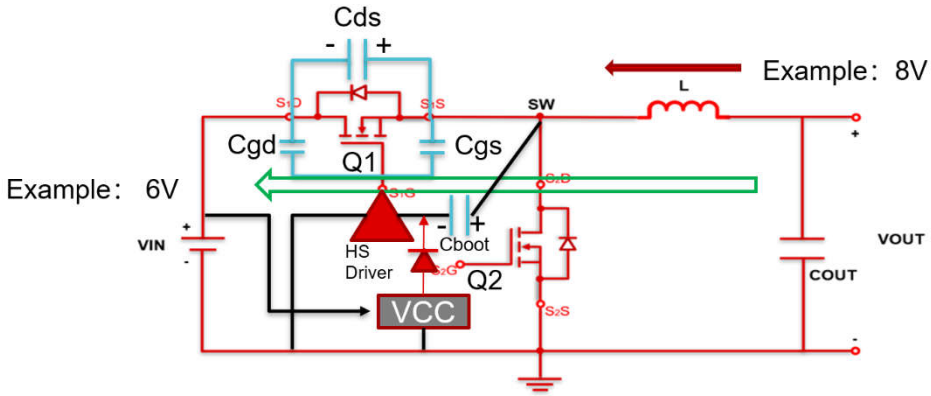

Figure 6-4. BOOT failure

(4) Other issues

Depending on the failure process of the reverse current, the following questions may arise:

- Why does the failure case only appear in PFM mode?

AUTO Mode (PFM Mode): Under light load, the chip reduces switching frequency to minimize switching and conduction losses, thereby lowering power consumption.

FPWM Mode: The chip maintains a constant switching frequency set by RT throughout operation, and it is currently designed to be 2.1MHz.

The charge accumulation in Cds during Q1 conduction is determined by the charging duration. This charging time of Cds comprises Q1 conduction and dead time, with the latter being fixed. Consequently, the primary influencing factor is Q1's conduction time. Therefore, under light load conditions, the frequency is lower, resulting in a shorter discharge time for Q2 when it turns on. If the discharge time for the reverse recovery current of the Cds and diode is too short, it will generate a substantial di/dt within a short period.

In summary, when the chip operates under light load conditions, a lower switching frequency results in a longer cycle time. Ton duration becomes longer compared to lower frequencies, meaning the upper transistor remains switched on for a longer period. This prolongs the charging time of the parasitic capacitances Cds and Cboot, leading to a greater current surge when the lower transistor switches on.

- Why is it prone to appearing in the design of POC?

The same power board in this case also utilizes 2pcs of LM63635-Q1 devices, though their outputs are set to 3.9V/3.3V, without any failure issues observed. For POC power supply applications, outputs are often set to 8V. Automotive batteries typically operate within a 9-16V range, with some requiring 6-16V. When the automotive battery voltage is inherently low, reverse current is more readily induced on the 3.3V/3.9V/5V power rails during power-down. In the current case, the camera load is relatively light. Compared to 3.9V load on the other LM63635-Q1 on the board, it is more prone to entering PFM Mode, thereby further increasing the probability of reverse current breakdown.

7 Data validation

Since SYNC/MODE was not designed with a pull-down in this case, it is impossible to directly modify it to a pull-up to VCC to switch to FPWM mode. This prevents the chip from staying in PFM mode for extended periods, which poses a risk of reverse current. Therefore, a compromise solution must be adopted by adding a dummy load at the output, as shown in Figure 7-1.

The design of the dummy load allows the chip to be as free as possible from operating in lower frequency PFM mode, but the dummy load continues to introduce losses and significantly affects efficiency. Moreover, owing to variations between individual chips and differences in current detection accuracy among different chips, it is not entirely possible to prevent chips from operating at frequencies exceeding 400kHz; operation at lower frequencies may still occur.

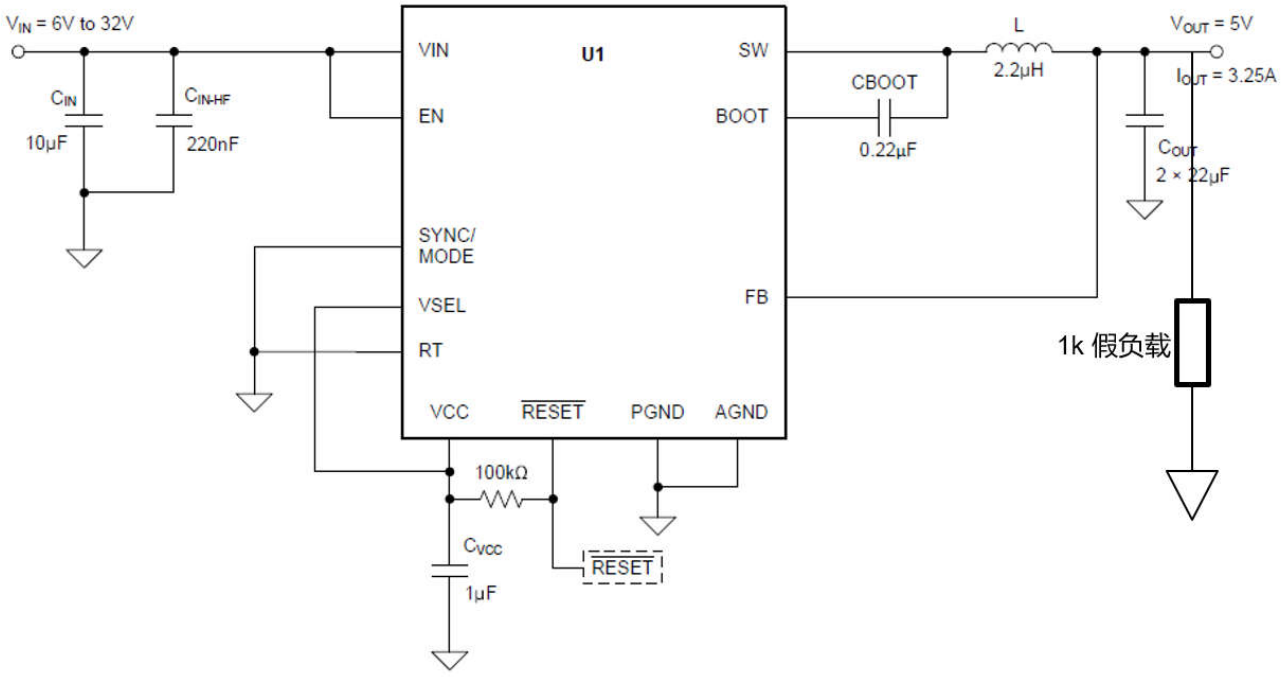

图 8-1. 示例应用电路 V_{IN} = 12V、V_{OUT} = 5V、I_{OUT} = 3.25A、f_{SW} = 2.1MHz

Figure 7-1. Add dummy load

Subsequent ongoing validation of failure data within this scenario yields the following comparison:

Failure rate without importing dummy load (mass production for 2 years): 622/72089 * 1000000=8628ppm

Failure rate when importing dummy load (within half a year of importing): 3/7640 * 1000000 = 392ppm

Concurrently, TI's extensive shipment and application survey data indicates that products operating in FPWM mode exhibit significantly lower failure rate than that in AUTO mode. Therefore, it can be concluded that the EOS failure in this case originates from reverse current inducing stress damage to the lower transistor MOSFET, subsequently causing conduction during the next switching operation.

8 Design recommendations

Through theoretical analysis, validation of EVM, validation of customer applications, and extensive data support, we have identified the root cause of this issue. For currently known potentially risky application scenarios, the following design recommendations are provided:

1. The peripheral of VCC is not connected to any external circuit. It uses a high quality (X7R) 1uF capacitor, with layout as close as possible to Pin design;
2. For applications requiring outputs exceeding 5V, when designing the schematic diagram, endeavor to employ FPWM mode or simultaneously reserve VCC pull-up or pull-down AGND designs on SYNC/MODE pin, selecting either with a 0Ω resistor;
3. To assist customers in mitigating risks encountered during POC application design, TI has implemented the optimized design modifications for LM636x5-Q1 product. For specific details regarding the modifications and affected production batches, please contact the relevant TI support team.

9 Summary

As one of the most widely used Tier 1 BUCK products in the world today, LM636XX-Q1 offers excellent performance and excellent cost-performance, providing automotive users with a superior experience. Concurrently, TI has implemented numerous optimizations to address inherent potential risks within BUCK topology, continuously refining the design to ensure product reliability. In addition to this, this article delves into the root causes of an EOS failure case study, driving chip optimization updates to accommodate broader application scenarios and enhance robustness of the chip.

10 References:

1. Data sheet "LM63635-Q1 3.5V to 36V, 3.25A, Automotive Buck Converter"
2. User Guide "LM63635EVM EVM User's Guide"
3. Application Report "Methods to Eliminate Damage Caused by Reverse Current in Synchronous Buck Converters"
4. Application Note "Design Considerations for Bootstrap Resistor in Buck Converters"
5. Application Report "AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines"

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