User's Guide

AM62L (AM62L32, AM62L31) Processor Family Schematic, Design Guidelines, Design Checklist and Review Checklist

ABSTRACT

The user's guide for AM62L (AM62L32, AM62L31) processor family includes custom board, schematic design guidelines, processor peripherals circuit implementation recommendations, and schematic review checklist for custom board designers using any of the processor from the processor family. The user's guide includes information related to processor power, external clocks, GPIO configurations, processor peripherals supported and interfacing the processor peripherals to attached (external) devices. Schematic review checklist (included at the end of each section), provides a comprehensive list of review points for the peripheral described in the specific section. The recommendation for custom board designers is to review the custom board schematic design implementation using the provided review checklist (points) and verify the recommendations or guidelines in the checklist have been implemented (followed).

Additionally, links (including product page on TI.com) have been provided for processor product pages, processor related collaterals, FAQs related to processor and processor peripherals published on E2E, and commonly referenced documents during custom board design. The recommendation for the custom board designers is to refer to the added links during custom board design to minimize design errors, optimize the design efforts, possibly reduce board build iterations and optimize the project timeline.

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1 Introduction

1.1 Guidelines for Usage of the User's Guide

The user's guide AM62Lx (AM62L32, AM62L31) processor family specific, *Schematic Design Guidelines and Schematic Review Checklist* includes schematic design guidelines that can be used by custom board designers during the custom board schematic design phase. Schematic review checklist is included at the end of each section and can be used by custom board designers to review the custom board schematic once the design is complete and before start of the layout.

1.1.1 Custom Board Schematics Design Guidelines - References Used in the User's Guide

The user's guide includes schematic design guidelines and schematic review checklist that can be used by custom board designers during custom board schematics design for the selected processor and the peripherals implemented (on-board or carrier (or add-on)) including memory (DDR4, LPDDR4, eMMC, OSPI, QSPI, SD card), power, communication interfaces, IOs and other circuit sections.

In the user's guide, reference to *Processor* implies the selected AM62Lx processor OPN and references to the *Attached devices* implies the external (on-board or carrier (or add-on)) peripherals that are interfaced to the processor (based on the target end equipment being designed and the application use case).

1.1.2 Processor Family Specific User's Guide

The user's guide covers AM62Lx (AM62L32, AM62L31) processors (GPNs). Each of the processor GPN can have multiple OPNs. The user's guide includes schematic design guidelines and schematic review checklist that can be used during custom board design. Processor family specific user's guide provides processor focused guidelines and checklist makes it easy to use for custom board designers when designing the board for a specific processor family. The user's guide is simpler and is easy to use for the chosen processor and processor family (Example: AM62Lx in this case).

1.1.3 Schematic Design Guidelines

The user's guide provides schematic design guidelines that can be used during custom board schematic design phase to implement the circuit connections between the processor and peripherals supported by the selected processor. Links to relevant FAQs have been added (as part of the guideline in each section) in addition to the design guidelines. FAQs (links added) provide additional information on a specific peripheral or interface topic including description and details on the implementation/use case and learning from customer interactions.

The recommendation is for custom board designers to follow the schematic design guidelines to minimize design errors that can affect board functionality, performance and to optimize the custom board design/build/test efforts.

1.1.4 Schematic Review Checklist

Schematic review checklist that can be used by custom board designers to review the custom board schematic design covering specific peripherals that have been described at the end of each section, sub section of the user's guide. The general recommendations, processor power and processor peripherals sections, sub sections described in the user's guide includes the checklist at the end. The schematic review checklist is categorized as *General*, *Schematic Review*, and *Additional*. Custom board designers can use the schematic review checklist to perform self-review of the custom board schematic design. Self-review minimizes possible schematics errors that can result in functional or performance related concerns and also reduce the review efforts during formal reviews (internal or external). Schematic review optimizes (reduces) the efforts required during custom board bring-up or performance testing resulting in increased board design quality and adherence to the planned timeline.

For information on available checklists and file formats, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x (ALV) / AM335x Design Recommendations / Custom board hardware design - Schematics review checklists

1.1.4.1 Common Checklist for Use With All Schematic Design Guidelines and Schematics Review Sections

1. Reviewed above section, including FAQ links and relevant application notes on TI.com.
2. Reviewed pin attributes and signal description sections in the processor-specific data sheet.
3. Reviewed timing and switching characteristics section, and any additional information available in the processor-specific data sheet.

1.1.4.1.1 Custom Board Schematic Design Implementation Checklist Sub-Sections Description

The schematic implementation review checklist includes 3 sub-sections:

General:

The general section lists (summarizes) the circuit implementations in bullets that are required (expected) to support the functionality for the peripheral section described above the checklist section (design guidelines section). The section also include care about to be considered when the section is interfaced or connected to another section to implement the required peripheral or module functionality (may not require (need) circuit implementation). The recommendation is to review and update the list of implementation checks provided as part of the schematic review before board build.

Schematic Review:

The schematic review section lists (summarizes) the circuit implementations in bullets that are required (expected) to be added by the custom board designers for implementing the circuit section to support the required functionality including the values, connections and other implementations to be followed for implementing the peripheral or module. The recommendation is to compare for the custom board schematic design implementation with the schematic checklist to make sure the implementation follows the design guidelines before the start of the layout.

Additional:

The additional section lists (details) the implementation and use case description in bullets that can be used by custom board designers along with the schematic review section to understand the circuit implementation rationale (need to implement) before considering optimizing the circuit design.

1.1.5 FAQ Reference for User's Guide Usage During Schematic Self-review

The below FAQ includes guidelines for custom board designers to perform a self-review using the available processor-specific collaterals,including schematic design checklist and General Guidelines Excel and Custom board schematic review checklist with figures Excel:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62D-Q1 / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Custom Board Schematics Self Review

1.2 AM62Lx Processor Family List of Processors

The user's guide applies to all the processor listed below. All relevant documents for the selected processor are available on the product pages on TI.com. The recommendation is to follow the product page link listed below to view the relevant product page.

See the *Ordering and Quality* section for information on the OPNs on the following product page:

- *AM62L*

1.3 Updates to Schematics Design Guidelines and Schematics Review Checklist

As part of efforts for continuous improvement of the collaterals, there can be changes or addition of sections to the *Schematics Design Guidelines and Schematics Review Checklist* user's guide with respect to the current revision published on TI.com (based on customer feedback, learnings, addition/enhancement of sections, errors or improvements) that are updated during the next document revision.

The below FAQ lists the changes customer board designers are required to follow during custom board schematic design (before the release of the revised user's guide on TI.com):

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Custom board hardware design - Updates to Hardware Design Considerations and Schematic Design Guidelines collaterals

The recommendation is to review the FAQ for possible updates frequently during all phases of the custom board design.

2 Related Collaterals and FAQs

Refer below FAQ. The FAQ includes the collaterals to be referenced and recommended steps to be followed during custom board design:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP - Collaterals for reference during different phases of custom board design, self-review and bring-up

2.1 Links to Commonly Referenced Collaterals During Custom Board Schematic Design

A number of documents relevant to the selected processor (family) are available on the processor-specific product page on TI.com. The recommendation for custom board designers is to read the relevant collateral (listed in the below FAQ) before starting the custom board design.

The following FAQ summarizes some of the key collaterals that can be referred, when starting the custom board design:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design – Collaterals to Get started

2.2 Hardware Design Considerations for Custom Board Design User's Guide

During the custom board design phase, the recommendation is to read, review and follow the applicable recommendations in the processor-specific *Hardware Design Considerations for Custom Board Design* user's guide linked below:

Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family

3 Processor-Specific Information

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

3.1 AM62Lx Processor Family Peripherals and IOs Change Summary (With Respect to AM62x Processor Family)

Below are the processor implementations to consider (note) during the AM62Lx-based custom board designs or changes to consider (note) when migrating from the AM62x processor based design to the AM62Lx processor based design:

1. Supports 2× Arm Cortex-A53 up to 1.25GHz
2. MCU Domain (MCU cores) not supported
3. GPU is not supported
4. The core supply voltage is fixed to 0.75V
5. VDDR_CORE has been internally connected to VDD_CORE
6. Reset inputs (x2) and reset status output (x1) numbers have been optimized
7. Implementation of 1.8V only IOs in addition to dual-voltage 1.8V/3.3V IOs. The IO supply for IO groups rails have been named accordingly. 1.8V only (VDDS0, VDDS1, VDDS_RTC and VDDS_WKUP) and dual-voltage 1.8V/3.3V (VDDSHVx [x = 0:4])
8. Buffer Type 1P8-LVCMOS and RTC-LVCMOS supported (have been implemented, refer Pin Attributes table) and Electrical Characteristics is added
9. Some of the processor peripherals including CPSW3G0 (3-port Gigabit Ethernet switch) and OSPI0 support 1.8V IO levels only
10. Non Muxed interface (connection of address bus and data bus separately) using GPMC0 interface is not supported
11. Camera Serial Interface (CSI-2) is not supported
12. Display interfaces supported includes MIPI DSI (x4 lanes DPHY) or DPI (24-bit RGB LVCMOS) (Any one of the display interfaces is actively supported and supported display is required to be selected during boot)
13. DDRSS addressing range for DDR4 and LPDDR4 is reduced (supports single rank only) and some of the DDRSS signals used for DDR4 interface have not been pinned out. The DDRSS does not support DDR0_ALERT_n, DDR0_PAR, DDR0_CKE1, DDR0_CS1_n, DDR0_ODT1 signals (pins).
14. OSPI0 interface supports connecting to x2 devices (OSPI0 module can be interface to 2 attached devices)
15. I2C interface instances including open-drain output type IO buffer I2C interface have been optimized
16. Pin connectivity requirements for I2C interface with open-drain output type IO buffer I2C buffers has been updated. A pullup is required only when the IO is used.
17. IOSETs (grouping of signal that are routed to multiple pins for timing closure) have been implemented for multiple peripherals (see the processor-specific data sheet)
18. Integrated LDO to power dual-voltage IO supply for IO group VDDSHV3 has been added to support generating switched 3.3V/1.8V MMC1 SD card interface IO supply to support UHS-I SD card.
19. Integrated x1 12-bit Analog-to-Digital Converter (ADC0), Up to 2MSPS (refer to the ADC Electrical Characteristics section of the processor-specific data sheet), x4 analog inputs (time-multiplexed)
20. Configuring the ADC inputs (ADC0_AIN0-3) as digital inputs is not supported
21. Programmable Real-Time Unit Subystem (PRUSS) is not supported

22. Support for multiple boot mode configuration approaches - Reduced pin count - Using only 4 of the bootstrap pins BOOTMODE [15:12], Boot from eFuse configured using the reduced pin count configuration and Full pin count - Using all 16 of the bootstrap pins BOOTMODE [15:0]
23. Ethernet boot is not supported
24. RTC only or RTC + IO + DDR (RTC + DDR) Self-refresh low-power modes are supported (Partial IO for CAN/GPIO/UART wakeup are not supported)
25. EXT_WAKEUP0 and EXT_WAKEUP1 function (pins) are added for External Wakeup Inputs
26. One (x1) VTM temperature sensor is supported (Temp Sensor 0: DDR/A53)
27. PMIC_LPM_EN0 has a special output cell that turns on a weak pullup as soon as power is applied. The weak internal pullup turns off at the same time the output is driven high on the rising edge of RTC_PORz input. (An external pull was recommended for the AM62x family of processors because the PMIC_LPM_EN0 IO was turned off while reset was asserted and the PMIC can never turn on without the external pullup resistor).
28. Voltage monitor input, fixed 0.45V (+/-3%) threshold VMON_VSYS functionality (pin) is not supported
29. Voltage monitor input for 3.3V processor VMON_3P3_SOC and Voltage monitor input for 1.8V processor power supply VMON_1P8_SOC are not supported
30. Available in a smaller 11.9mm ×11.9mm, 0.5mm VCA, 373-pin FCCSP BGA package (ANB)

For more information, refer below document:

AM625x/AM623x and AM62Lx Hardware Migration Guide

3.1.1 Silicon Revision

Refer *Device Naming Convention* section of the processor-specific data sheet for the available processor revisions. Refer *AM62Lx Sitara Processors* data sheet for the supported device features and *AM62Lx Sitara Processor-specific Silicon Errata* for information on the supported functions for specific silicon revisions.

3.2 Selection of Processor OPN (Orderable Part Number)

Selection of the processor OPN (based on the required features) is a critical and important phase during custom board design. To get an overview of the processor family (AM62L (AM62L32, AM62L31)) architecture and for selecting the required processor OPN (processor used on the custom board) based on the required functionalities and features, package (ANB) and speed grade, see the *Functional Block Diagram*, *Device Comparison*, *Device Naming Convention*, *Device Speed Grades* and *Packaging Information* sections of the processor-specific data sheet.

The recommendation is to update the schematics with the selected processor OPN.

For information on the supported (available) packages for AM62Lx processor family, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A / AM62D-Q1 / AM62P / AM62L Custom board hardware design - Available Device Packages

3.3 EVM Schematic Version and Revision Referenced

PROC181E1-1a_SCH_With_Design_Updates..Notes_V1.0.pdf version of the schematics has been referenced for all the illustrations in the user's guide. The illustration include design notes that can be referenced during custom board design.

3.4 Processor-specific Data Sheet Use Case and Version Referenced for User's Guide Edits

Processor-specific data sheet includes:

1. Pin attributes (ball number, pin to muxed function mapping).
2. Signal descriptions.
3. Pin connectivity requirements.
4. Electrical characteristics, timing and switching characteristics, and timing diagrams for the applicable processor peripherals.
5. Recommended operating conditions for the processor supply rails.
6. Sequencing for the processor supply rails (Power-up and Power-down).
7. Maximum operating conditions and Recommended operating condition.

8. Detailed Description of the processor internal structure.
9. Applications, Implementation, and Layout.
10. Device and Documentation Support including Device Nomenclature (Device Naming Convention), Tools and Software.
11. Revision History.
12. Mechanical, Packaging, and Orderable Information.

Processor-specific data sheet with revision number referenced (during user's guide edits):

SPRSPA1A – MARCH 2025 – REVISED SEPTEMBER 2025 (AM62Lx Sitara Processors data sheet)

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Current Data sheet revision, updates, revision backup and usage notes

3.5 Peripheral Instance Naming Convention - Data Sheet and TRM

For naming of peripherals and available number of peripheral instances, the processor-specific TRM tends to be *generic* and the processor-specific data sheet is *specific* (includes the number of supported instances). The recommendation is to always refer to the processor-specific data sheet for the supported peripherals and peripheral instances.

A suffix number is assigned to the peripheral name, in the processor-specific data sheet signal naming, even when there is a single peripheral instance. The suffix starts with *0*.

For the common platform Ethernet switch 3-port gigabit (CPSW3G0) port names, port 0 is the internal (communications port programming interface (CPPI) host) port of the switch.

3.6 Processor Peripherals and IOs Connection When Not Used (Unused)

During the custom board design, some of the processor peripherals are not be used (unused). Processor peripherals (including peripherals that have a dedicated function) have specific connectivity requirements when not used. Refer to the *Pin Connectivity Requirements* section of processor-specific data sheet for connecting the peripherals when not used. The connectivity requirements section includes recommendations for connecting the supply rails and the interface signals.

Processor GPIOs (muxed with peripherals, SDIO or LVCMOS buffer type or 1P8-LVCMOS Buffer Type) that support configuration of alternate functions (muxed), can be left unconnected when not used (in case there are no connectivity requirements specified). The pad configurations for the peripherals and IOs can be the reset state.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Data sheet Pin Attributes and Pin connectivity related queries

3.7 Ordering and Quality Information for AM62Lx Processor Family

For information related to ordering and quality for the selected processor, see the link below:

AM62L Ordering and quality

3.8 Checklist for Selection of Required Processor GPN (Generic Part Number) and OPN (Ordering Part Number)

General

During the custom board schematic design process, review and verify the following information, collaterals and data sheet sections to select the required processor OPN:

1. Availability of commonly used memory interfaces, high-speed communication, on-board synchronous and asynchronous communication interfaces and display interfaces.
2. On-board debug and diagnostics support (JTAG, UART, OBSCLK[1:0] and CLKOUT0).
3. Number of supply rails required, recommended operating conditions for supply rails, power-up and power-down sequence for core, memory interface, analog and IO supplies.
4. Electrical characteristics and timing information for the selected peripherals.
5. Availability of application notes, peripherals interface circuit implementation recommendations or examples, and layout guidelines.
6. Silicon errata related to processor functioning, boot modes (supported and care about, workarounds for the configured boot mode) and the peripherals of interest.
7. Availability of EVM for evaluation and design files for reference and/or reuse.

4 Processor Power Architecture

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

For an overview of TI power management portfolio, see the TI *Power management* page.

WEBENCH® circuit designer tool provides a visual interface that can be used to create customized power architecture.

4.1 Generating Processor-Specific and Peripherals (Attached Device) Supply Rails

The required supply rails for the selected processor and attached devices can be generated using integrated (using PMIC, discrete DC/DCs, discrete LDOs) or discrete (using DC/DCs, discrete LDOs) power architecture.

PMIC (integrated power architecture) are designed for a specific processor or processor family. Use of PMIC simplifies power architecture (power supply rails) design. The PMIC generates the commonly required (used) processor and the attached device supplies. The PMIC internally manages power-up sequencing, power-down sequencing, supply slew rate control, optional residual voltage (voltage decay) detection and meets the processor-specific power (PDN) requirements. Additional discrete DC/DCs and discrete LDOs can used to generate the other on-board supplies (based on the use case) required based on the use case.

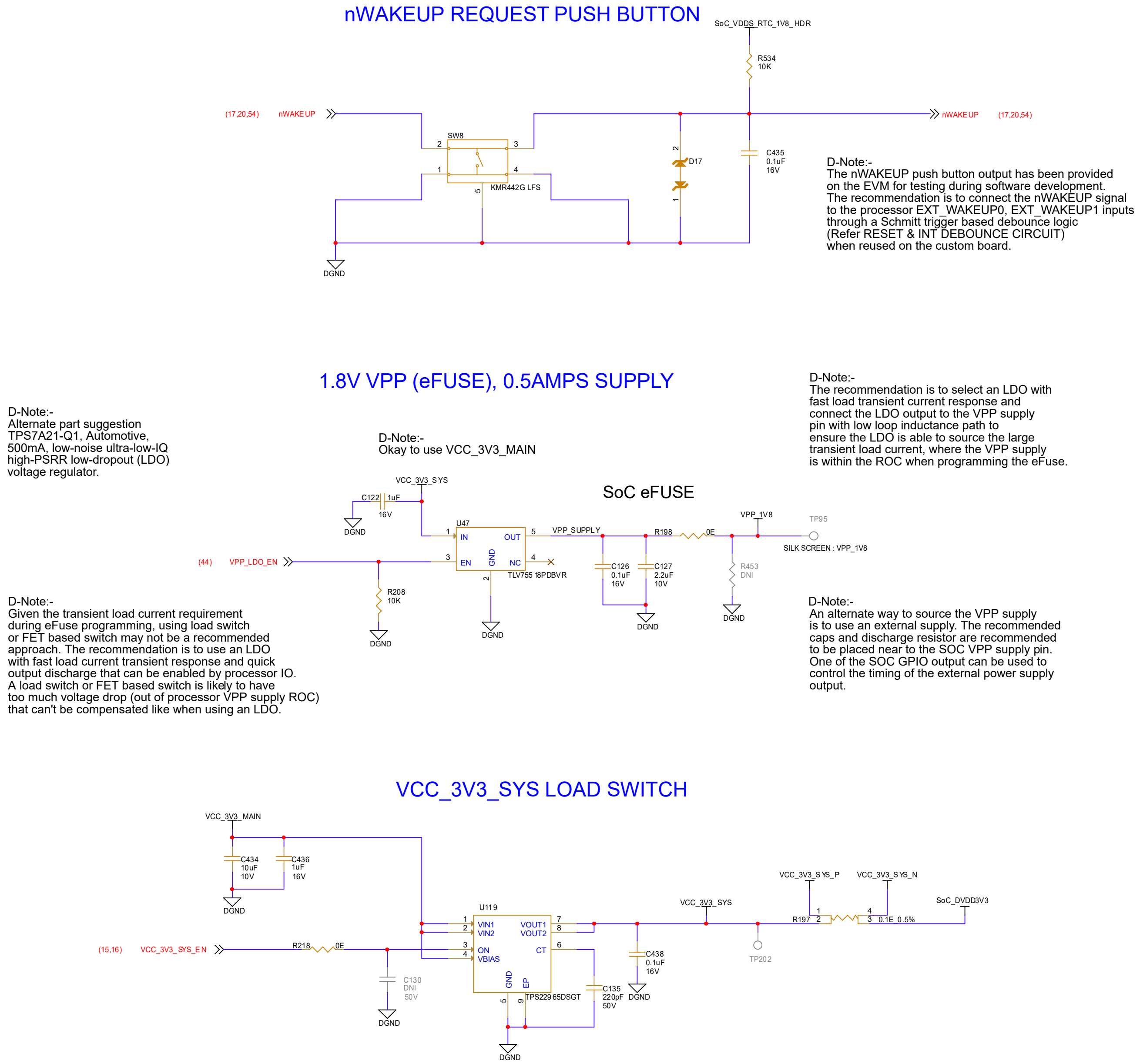
Use of discrete power architecture provides flexibility in selection of power devices and power architecture design. The design efforts can increase since the custom board designers are responsible for selection of discrete DC/DCs and LDOs that sources the required load current, DC/DCs and LDOs that can be adjusted or configured to generate the required supply voltages, DC/DCs and LDOs that can support the required load current transient, controls, supply slew rate and supports configuring the required supply sequencing.

Processor power supply rails have slew rate requirements specified. The recommendation is to follow the *Power Supply Slew Rate Requirement* section of processor-specific data sheet for the supply rails (generated or switched).

The family of power converters (DC/DCs and LDOs) products and related collaterals that can be used for implementing the on-board supplies using PMIC or discrete power architecture are summarized in the below sections:

4.1.1 AM62Lx Processor Family Power Architecture

Figure 4-1 includes load switch U119 for sequencing VCC_3V3_SYS (SOC IO supply) that is controlled by PMIC GPIO and a shunt (for current measurement or isolation) placed close to the load switch output. Capacitor provision to control the output supply slew rate to meet the processor slew rate requirements specified in the processor-specific data sheet is included.



nWAKEUP REQUEST PUSH BUTTON

D-Note:-
The nWAKEUP push button output has been provided on the EVM for testing during software development.
The recommendation is to connect the nWAKEUP signal to the processor EXT_WAKEUP0, EXT_WAKEUP1 inputs through a Schmitt trigger based debounce logic (Refer RESET & INT DEBOUNCE CIRCUIT) when reused on the custom board.

1.8V VPP (eFUSE), 0.5AMPS SUPPLY

D-Note:-
Alternate part suggestion
TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator.

D-Note:-
Okay to use VCC_3V3_MAIN

D-Note:-
The recommendation is to select an LDO with fast load transient current response and connect the LDO output to the VPP supply pin with low loop inductance path to ensure the LDO is able to source the large transient load current, where the VPP supply is within the ROC when programming the eFuse.

D-Note:-
Given the transient load current requirement during eFuse programming, using load switch or FET based switch may not be a recommended approach. The recommendation is to use an LDO with fast load current transient response and quick output discharge that can be enabled by processor IO.
A load switch or FET based switch is likely to have too much voltage drop (out of processor VPP supply ROC) that can't be compensated like when using an LDO.

D-Note:-
An alternate way to source the VPP supply is to use an external supply. The recommended caps and discharge resistor are recommended to be placed near to the SOC VPP supply pin.
One of the SOC GPIO output can be used to control the timing of the external power supply output.

VCC_3V3_SYS LOAD SWITCH

Figure 4-1. Load Switch for Processor IO Supply Sequencing

4.1.1.1 Power Management IC (PMIC) Based Power Architecture

Refer to the EVM schematics for the supported or tested PMIC based power architecture. The TPS65214x PMIC family supports RTC + IO + DDR low-power mode.

For custom board design using DDR4, there can be a change in the PMIC NVM configuration, supply rails generated by the PMIC and power architecture to support low power mode. Refer to the available documentation on AM62L processor product page and TPS65214 PMIC product page on TI.com or use E2E when designing custom board with DDR4.

Refer to *AM62L Power Supply Implementation* application note on processor product page for description of AM62L power architecture implementation for different application use cases and low-power modes.

For more information, see the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design – Queries regarding power architecture including PMIC

For information related to residual voltage and detection, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Residual Voltage, Detection and supply decay

4.1.1.1.1 PMIC Based Power Architecture Checklist for TPS65214x

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Selection of PMIC (OPN) based on the input supply and the required output voltages (core voltage, IO voltage and DDRSS voltage configuration)
3. PMIC checklist for addition of required input and output capacitors including values, feedback connection, and pin connections
4. Voltage rating of the selected capacitors considering voltage derating
5. Connection of the PMIC buck output feedback (after the output bulk capacitor)
6. Configuration of the recommended PMIC control and IO signals
7. Connection of the required control signals for processor IO supply sequencing (load switch)
8. Processor I2C interface instance used to interface with the PMIC
9. Processor to PMIC, and PMIC to processor IO interface connections
10. Connection of PMIC power good signal to processor PORz (through discrete buffer or directly, pullup (adjust resistor value based on the measured slew))
11. Connection of PMIC IO output to processor RTC_PORz when RTC + IO + DDR low power mode is implemented
12. Naming of the supply rails (indicating configured output voltage level)
13. Provision for isolating the PMIC output voltages for current measure or testing
14. Net name matches (same name) for processor and attached devices IO supplies
15. Connection of interrupt, MODE/RESET, and EN/PB/VSENSE signals and connection of the required pulls for the PMIC IOs

Schematic Review

Follow the below list for the custom schematic design:

1. Configuration of the PMIC output to match the processor and attached devices IO supply operating voltages as per the custom board requirements
2. The custom board PMIC implementation with the EVM schematic implementation for capacitors quantity, size and values, IOs connection
3. Connection of the PMIC buck output feedback (tie the feedback after the output bulk capacitors)
4. PMIC nRSTOUT0 slew (pullup value) when connected directly to processor PORz input (recommend using a discrete push-pull output type buffer)
5. Connection of the required control signals for processor IO supply sequencing (load switch EN for processor and attached device IO supply voltage and provision for load switch output voltage slew rate control using external capacitor)
6. Voltage rating of the selected capacitors considering derating (> twice the worst-case applied voltage is a commonly used guideline)
7. Matching of the PMIC output voltage level with the supply requirements for the processor and attached devices (based on the OPN)
8. Processor I2C instance used to interface to PMIC (Follow EVM or review the required I2C instance based on the use case)
9. Configuration of discrete DC/DC outputs and LDOs used along with the PMIC to generate additional supply rails
10. External LDO implementation for generating VPP supply (eFuse programming), LDO output enable (EN) control, addition of bulk and decoupling capacitors considering load current transient and provision for isolation resistor for testing the VPP supply output enable timing

Additional

1. In case custom board design power architecture is based on TI PMIC, the recommendation is to obtain a detailed review of the implementation done with the PMIC team (business unit or product line).
2. A 0Ω resistor or jumper is recommended at the output of the PMIC and discrete DC/DC, LDO for isolation or current measurement for the initial board build. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection for connecting TPs to 0Ω resistor or jumper.
3. The recommendation is to connect the feedback for the PMIC buck output after the bulk capacitor. The recommendation is to connect the feedback to make sure the removal of the 0Ω resistor does not affect the PMIC operation (connect on the PMIC side of the resistor).
4. The recommendation is to show the PMIC input bulk capacitors for buck (DC/DC) inputs and VSYS separately and near to each of the pin for ease of placement and routing.
5. The recommendation is to review and follow the FAQs related to residual voltage.
6. In case a non-TI PMIC is used, the recommendation for custom board designers is to review and follow the relevant processor collaterals including the processor-specific data sheet and *Maximum Current Ratings* application note. The recommendation is to review the *Recommended Operating Conditions*, *Supply Slew Rate Requirements*, *PORz Timing Requirements*, *Power-Up Sequencing and Power-Down Sequencing* sections of the processor-specific data sheet and confirm the selected PMIC based power architecture supports the above requirements and residual voltage (RV) check.

4.1.1.1.2 Additional References

For information, see the following section in the processor-specific data sheet.

- Device Connection and Layout Fundamentals
- Power Supply
- Power Supply Designs

4.1.1.2 Discrete Power Devices (DC/DC, LDO) Based Power Architecture

To generate the processor and the attached devices supply rails a Discrete power architecture can be considered.

The power architecture can be based on discrete DC-DC converters and LDOs.

For information related to available or recommended discrete power architecture, see the processor-specific (*AM62L*) product page on TI.com.

Processor-specific product page provides the updated information on the available power architecture.

Refer to the EVM schematics for implementing the RTC supplies using LDOs and generating the main 3.3V supply using DC/DC converter.

When a custom (TI or Non-TI) discrete power architecture is implemented, take note of the supplies sizing (current rating), supplies sequencing, supplies slew rate control and PORz input L->H delay (hold time) (for oscillator start-up and stabilization) requirements after all the supplies ramp. The recommendation is to verify the above listed requirements as per the processor-specific data sheet are followed.

During supply rail power-down (power off), the recommendation is for the PORz input to reach a valid logic low level before the supplies begin to ramp down. The discrete power architecture is recommended to be designed to be able to turn off all supply rails and monitor the power rails decay to less than 300mV before initiating a new power-up sequence anytime any of the supply rail drops below the minimum value defined in *Recommended Operating Conditions*.

PORz input is recommended (required) to be held low (active) during power-up until all the processor supplies ramp and are valid (stable) plus minimum delay of 9.5ms (mentioned as 9500000ns in processor-specific data sheet) for internal oscillator to start-up and stabilize (when using external crystal plus internal oscillator, see the processor-specific data sheet) or PORz input is held low (active) until all the processor supplies ramp and are valid and external oscillator clock output is stable (when using external LVCMOS digital clock source (oscillator)) plus minimum delay of 1.2µs (mentioned as 1200ns in processor-specific data sheet) (see the processor-specific data sheet).

The recommendation is to consider the *Maximum Current Ratings* application note for supply sizing.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Discrete power Architecture

4.1.1.2.1 Discrete DC/DCs

The recommendation is to consider discrete DC/DC such as the TPS63070 or LM5141 or similar switching power devices.

For an overview of the available discrete DC/DC (Buck) switching devices, see the *AC/DC & DC/DC converters (integrated FET)* page.

Additionally, refer the following document and video library:

Quick Reference Guide To TI Buck Switching DC/DC Application Note

Power Supply Design training resources - Video library

4.1.1.2.2 Discrete LDOs

The recommendation is to consider discrete LDO devices such as TPS74501 and TLV75518 or similar LDOs.

For an overview of the available discrete LDOs, see the TI *Linear and low-dropout (LDO) regulators* page.

Additionally, refer below application notes:

Low Dropout Regulators Quick Reference Guide

Linear Regulator Design Guide For LDOs

A Topical Index of TI LDO Application Notes

4.1.1.2.3 Discrete Power Devices (DC/DC, LDO) Based Power Architecture Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. The configured output voltage level and the current sizing (rating) for the supply rails.
3. Output voltage feedback connection and feedback resistor divider tolerance.
4. Selected discrete DC/DC supports active discharge.
5. Discrete DC/DC output slew rate meets the processor requirements.
6. Sequencing of the supply rails as per the processor requirements.
7. PORz input (DC/DC PG output) slew rate.
8. Voltage rating of the selected capacitors considering derating.
9. Implementation of SD card interface IO supply supporting UHS-I SD card.
10. Implementation of VPP (eFuse programming) supply.
11. Naming of the supply rails.
12. Matching of the Discrete DC/DC or Discrete LDO voltage levels.
13. Net name matches (same name) for processor and attached devices IO supplies.

Schematic Review

Follow the list below for the custom schematic design:

1. The resistor divider value including tolerance connected to the feedback to generate the required output supply voltage matches with the calculated value for discrete DC/DC or LDO.
2. DC/DC or LDO outputs current sizing.
3. Discrete DC/DC or LDO PG outputs have the required pullup and connects to other DC/DC or LDO EN for supply sequencing.
4. DC/DC or LDO outputs slew rate matches the processor slew rate requirements.

5. PORz input (DC/DC PG output) slew rate (connect through discrete push-pull output type buffer) and L to H delay (PORz input low hold time for clock start-up and stabilization) implementation after all the processor supplies ramp.
6. PORz input low hold time after supplies ramp, in case the DC/DC PG output connects directly to the processor PORz input.
7. Implementation of VPP (eFuse programming) supply including capacitors to support load current transients and output enable (EN).
8. Implementation of LDO for SD card interface IO supply for supporting UHS-I SD card.
9. Naming of the supply rails (indicate configured output voltage).
10. Matching of the Discrete DC/DC or Discrete LDO voltage levels with the supply requirements for the processor and attached devices.
11. Voltage rating of the selected capacitors considering derating (> twice the worst-case applied voltage is a commonly used guideline).
12. Discrete power device selection including output supply voltage rails (operating voltage/amplitude) and current rating, active discharge, provision to enable, slew rate control, residual voltage detection (Allow to power-up only when the supply voltages are < 300mV after power-down).

Additional

1. In case custom board design power architecture is based on TI power, the recommendation is to obtain a detailed review of the implementation with the relevant business unit or product line.
2. A 0Ω resistor or jumper is recommended at the output of the discrete DC/DC, LDO for isolation or current measurement for the initial board build. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection for connecting TPs to 0Ω resistor or jumper.
3. The recommendation is to add a zener at the output of discrete DC/DC or discrete LDO when adjustable output type discrete DC/DC or discrete LDO are used.

4.2 Processor Power Rails Supply Control, Sequencing and Supply Overload Protection

4.2.1 Load Switch (Processor Supply Rail Power Switching)

Load switches are used to switch and sequence the processor and attached devices supply rails. Load switches are used to control (turn on and off) power to a specific peripheral or sub-system referenced to (powered by) the same input supply rail, instead of using multiple discrete DC/DCs or LDOs to generate the supply. In some applications, there is a recommended power-up and power-down sequence that is recommended to be followed. Load switches simplifies the implementation of power sequencing to meet the power-up and power-down sequence timing requirements. The load switch enable can controlled by the PMIC or discrete DC/DC PG output to meet the processor power sequencing requirements.

Consider load switches such as TPS22965, TPS22918, TPS22902, and TPS22946.

For an overview of the available load switch families, see the TI *load switches* page.

4.2.1.1 Load Switch (Processor Supply Rail Power Switching) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Load switch current sizing
3. Connection and sequencing of the load switch enable
4. Output voltage slew rate control configuration
5. Addition of capacitors at the output as per the load switch data sheet recommendations
6. Voltage rating of the selected capacitors considering derating

Schematic review

Follow the below list for the custom schematic design:

1. Input and output capacitor values, ratio as per the data sheet and capacitor voltage rating.
2. Output voltage slew rate is configured (capacitor value selection) as per the processor IO supply slew rate requirements.

4.2.2 eFuse IC (Power Switching and Protection)

On the custom board design, an eFuse can be used at the supply input for protection. eFuse power switching and protection ICs are integrated power path protection devices that are used to limit circuit current and voltages to a safe level during fault conditions. eFuses offer a number of benefits to the design and include protection features that are often difficult to implement with discrete components. For an overview of the available eFuse families, see the TI *eFuses and hot swap controllers* page.

5 General Recommendations

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

The below sections include general recommendations that are recommended to be followed before the start of the custom design. The section also includes general recommendations while using the EVM collaterals as reference (including schematics) and during design of custom board schematics.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on processor core, VDD_CORE, VDDR_CORE, VPP and other core supplies

5.1 Processor Performance Evaluation Module (EVM)

Processor (hardware) performance evaluation modules and platforms (EVMs) are not reference designs. The modules and platforms do not represent proper or complete board or end equipment function implementation. In some cases, the EVMs are partially or completely designed and released for fabrication before the processor design is complete. The time line is such that the hardware platform is available when the first silicon is available. New (additional) processor requirements come up during processor bring-up and bench validation. All the new requirements may not be accounted for in the EVM (hardware evaluation platform). Therefore, TI expects custom board designers to carefully review and follow all requirements defined in the processor-specific data sheet, silicon errata, hardware design considerations user's guide, schematic design guidelines and TRM when designing custom boards.

Processor (hardware) performance evaluation platforms are not designed to be comprehensive of any custom board or end equipment specific requirements, such as EMI or EMC (Electro Magnetic Interference, Electro Magnetic Compatibility tests including radiated susceptibility, radiated emissions, ESD), noise susceptibility, thermal management, and so forth.

For design update notes that custom board designers can refer along with the EVM schematics, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics updates for Design Update Note

5.1.1 Evaluation Module (Starter Kit) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. The EVM schematic revision referenced includes D-Notes, R-Notes, and CAD Notes

5.2 Processor-Specific EVM Versus Data Sheet

During the design phase of custom board design, in case any discrepancy is seen between the processor-specific EVM and processor-specific data sheet during processor evaluation or custom board design, the recommendation is to follow the processor-specific data sheet. Despite the best efforts by the EVM designer, the EVM schematic can have errors that still function but are not completely aligned with the processor-specific data sheet specifications.

5.2.1 Notes About Component Selection

Note

Component values, package size and voltage rating in the EVM schematics are being provided as starting point for the custom board designer and are not always optimized. The recommendation for custom board designer is to validate if the values, size and voltage rating are appropriate for the specific custom board implementation and make the required updates.

The recommendation is to review the EVM BOM with respect to the custom board design requirements and optimize the components based on the processor-specific data sheet recommendations, application requirements, custom board design methodology being followed and available (company specific or generic) design or component selection guidelines.

The recommendation is to perform design calculations for the circuit implementation, perform board level tests and measurements, conduct internal design reviews before finalizing the components (value, package, voltage ratings and power ratings).

5.2.1.1 Series Resistor

Provision for a series resistor (0Ω) on the processor IOs interfaces is recommended based on the use case. The values for the series resistor used in the EVM schematics can be used as a starting point for custom board designs. The recommendation for custom board designers is to verify the values on the custom board and adjust accordingly (step function that occurs on the pin is not near the mid-supply). Simulation as required is recommended to finalize the values.

5.2.1.2 Parallel Pull Resistor

Note

There is no firm rule or requirement for external pull unless the pull requirements are defined in an industry standard. Industry standard definition for pulls is the main reason we can make firm recommendations for external pulls on the eMMC and SD card signals. For the other peripherals, the recommendation is for customers to evaluate the function of the attached devices connected to every processor signal on the custom board and apply appropriate technical/engineering judgment to determine the need to have external pulls that prevent any input from floating when attached device input buffer is turned on. The recommendations provided in the design guide are generic and customer is expected to review the design requirements and the availability of pulls internal to the attached device before implementing. Be sure to not provide an external pull in contention with an internal pull. Example: An example is adding an external pull that is in contention with the internal pull (internal to the attached device), such that the contention creates a mid-supply potential on the signal (input).

The recommendation is to provide provision for parallel pulls to the processor IOs that has a trace connected and not being driven actively or for the IOs connected to the attached device inputs that can float (to prevent the attached device inputs from floating until the host software configures the IO). Parallel pull polarity and pull value depends on the specific peripheral connectivity recommendations, recommendations for improved processor performance and reliability, and relevant interface or interface standards requirements. The recommendations for pullups are provided.

Pull values used in processor-specific EVM can be used as a starting point and custom board designer can select the appropriate pull values based on the recommendations for the processor and attached device, or specific board design requirements.10kΩ or 47kΩ (choice of pullup allowed to standardize the component selection and BOM) pull value is recommended for IOs or interfaces that do not have specific recommendations. The pull value can be chosen based on the board design to optimize the use of components or reduce current or improve noise performance.

When a trace is connected to the processor pin (IO pads) and the IO is not being actively driven (floating), a parallel pull 47kΩ is recommended. Processor IO buffers are (TX (Output) and RX (Input) are off during reset and after reset, and internal pulls (pullup and pulldown)) are turned off during reset and after reset. The IOs are in a high impedance state, effectively behaving as an antenna that can pick up noise. Without a parallel pull, the IOs are in high impedance state. High impedance makes noise to couple energy easily on the floating signal trace and develop a potential that can exceed the IO recommended operating condition. The potential creates an electrical over-stress (EOS) on the IO. Electrostatic discharge (ESD) protection circuits internal to the processor were designed to only protect the device from ESD during handling before being installed on a PCB.

5.2.1.3 Drive Strength or Slew Configuration

For information related to drive strength (Dual-voltage IOs, For LVCMOS Buffer Type Only) or slew rate (Fixed-voltage IOs, For 1P8-LVCMOS Buffer Type Only) configuration supported, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Drive Strength Configuration for dual-voltage LVCMOS and SDIO IO buffers and fixed 1.8V 1P8-LVCMOS, buffers

5.2.1.4 Processor-specific Data Sheet Recommendations

Custom board designers are responsible for implementing the required or recommended circuits to make sure the custom board design follows the processor-specific data sheet pin connectivity requirements. Example: Requirements for I2C Open-Drain Electrical Characteristics - Input Slew Rate limit requirements when pulled to 3.3V supply.

In case processor-specific data sheet recommendations are not available, the recommendation is to follow the schematic design guidelines or to follow the EVM schematic implementation as a starting point.

5.2.1.5 Processor IOs Protection - Provision for External ESD Protection Devices

An external ESD protection is recommended for the processor IOs that are connected directly to external inputs or connected to external connector. Internal ESD protection were not designed to handle the board level ESD requirements. For an overview of the ESD protection devices, see the TI *ESD protection* page.

5.2.1.6 Peripheral Clock Outputs Series Resistor

Series resistor (22Ω) on the clock outputs are recommended to be added near to the processor clock output (for MCSPI, MCASP) pins since the clock is also being used for retiming. The series resistor additionally supports possible reflection control (signal distortion).

For MMC0, MMC1, MMC2, OSPI0, GPMC0 interfaces, an unbonded pad is used (internal) for retiming (loopback). We do not use the same clock that is sent across the PCB to the attached device for our capture clock. We branch the output clock into two paths inside the device, where the clock is sent to two separate IO cells. One IO cell is connected to a package ball, which is used to source a clock to the attached device. The other IO cell is unbounded (not connected to any package ball). The clock used as the receive capture clock is sent out through the unbonded IO cell and looped back into the device before being used as the capture clock. This is done to make sure the clock has the same delay that is inserted on the clock going out to the attached device and the same delay that is inserted on the data coming back in from the attached device. The unbonded IO cell pad never experiences the voltage step that is produced on the source end of a PCB signal trace. A low value series resistor (0Ω to start) is recommended (provisioned) for control of possible signal reflections (improve signal integrity).

5.2.1.7 Peripheral Clock Outputs Pulldown Resistor

A pulldown is recommended on peripherals clock outputs (eMMC, SDIO, SD card, OSPI0, MCSPI, MCASP, GPMC0) connected to the attached device near to the clock input of the attached device. Optionally capacitor (8 to10pF) can be provisioned and configured as no populate. The capacitor can be mounted in case issues related to board level signal integrity is observed. The recommendation is to connect the capacitor to the attached device clock input with shortest stub.

5.2.1.8 Component Selection Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Selection of resistors value, tolerance, size and wattage.
3. Some specific resistors have ±1% tolerance requirements (refer to the processor or attached device data sheet, SK schematics, or EVMs).
4. Standard tolerance resistors can be used for other use cases, Example: pullup, pulldown, LED current limit, attached device address configuration or series resistor.
5. The recommendation is to compare the pull values implementation on the custom board with the EVM schematic.
6. Voltage rating of the capacitors used includes derating (for non-polarized capacitors, > x2 the worst case applied voltage is a commonly used guideline).
7. DC bias effect (use 10V or more) and capacitor tolerance (10%) considered while choosing the voltage rating of capacitors (to be within the recommended value) for CAP_VDDS_xxx
8. Discrete components package selection (application and use case dependent, considering voltage ratings, tolerance, aging and temperature range).
9. Selection of compatible attached devices (DDR4, LPDDR4, eMMC, OSPI, QSPI, SD card, EPHYs).
10. Selection of required memory size (DDR4, LPDDR4) and providing provision for expanding the memory as required.
11. Reviewed the FAQs related to passive components value, tolerance and voltage rating.

As a starting point for information on key components used on the EVMs and SKs, component values and tolerances, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key devices (components) list

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

5.2.2 Additional Information Regarding EVM Design (Schematic, Board) and Reuse

5.2.2.1 Updated EVM Schematic With Design, Review and CAD Notes Added

During custom board design, as part of the custom board design process, the custom board designers can (tend to) reuse the EVM design (CAD files) and make the required edits. Alternatively, custom board designers can reuse the common circuit implementations (sections), including processor, memory, power and high-speed communication interfaces. Since the EVM design is expected to have additional functions, custom board designers tend to optimize the EVM schematic design as per the custom board requirements. While optimizing the EVM schematics, errors can be introduced into the custom board design that can affect functionality, performance or reliability of the custom board. When optimizing the EVM schematics, custom board designers can have queries related to the EVM circuit implementation. Common design and optimization errors across multiple custom board designs were observed during the schematics review and during custom board debugs. Based on the customer queries, customer inputs, internal suggestions, and data sheet pin connectivity recommendations, comprehensive Design Notes (D-Note), Review Notes (R-Note) and CAD Notes (CAD-Note) have been added near each section of the EVM schematic for custom board designers to review and follow (implement the recommendations to minimize board design errors).

The available downloadable design documents are listed in the below FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - Design notes and Review notes for Reuse of EVM TMDS62LEVM Schematics

The product overview document is currently in works. Review the above FAQ or the recommendation is to check on TI.com frequently for availability.

5.2.2.2 EVM Design Files Reuse for Custom Board Design

Based on the design approach being followed during the custom board design and project timeline, the EVM design files can be used as a starting point to make the required updates (changes as per the custom board requirements). The recommendation is to review the EVM schematic design before implementation. The recommendation is to review the component selection for size, tolerance and voltage rating as per the custom board functional and performance requirements.

The following FAQ includes the PDF schematic and additional information related to EVM:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - Reusing TI EVM design files

5.2.2.2.1 Modular Schematic Sections

The number of pages in the EVM schematics has been increased. Each page now has specific section for easy review and reuse. The pages have been arranged in the order of priority of usage. A commonly used section of the EVM schematics are listed in the starting pages of the schematics. Sections that enhance the performance or are optional for custom board design have been listed below the commonly used schematic sections.

5.2.2.2.2 EVM Design Files Reuse for Custom board Design - Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Latest version of the selected or required EVM design files (collaterals) are being referenced.
3. D-Notes and R-Notes added close to the schematic sections have been reviewed and considered.
4. Reconfiguring the DNI properties for components whose DNI properties have been reset (custom board design implementation circuit components mounting option properties are reset (DNI configuration is reset, all components are shown as populate) when the EVM design files are saved as a different project or the schematic pages or circuit sections are rearranged).
5. Changes in circuit connections (connection missing) including off-page connections when the schematics design is translated to an alternate CAD tool.

5.2.2.3 EVM Schematic Pages Sequencing (Based on Functions, Reuse) and EVM Board Layout

For the EVM schematics revisions that are currently being released or in works (to be released in the future), TI is arranging (sequencing) the schematics pages in a modular format for ease of reuse. The schematic pages flow starts with required pages including processor power supplies generation, processor supplies and peripheral connections, attached devices circuit implementation. Optional debug and monitoring sections are added after the required pages. The arrangement helps custom board designers to delete the schematic sections that are not used during the custom board design.

The EVM board design implementation is a flat architecture with the processor and the attached devices integrated on the same board. Custom board designers can follow the EVM implementation when designing flat architecture custom board. In case the customer board architecture is SOM (System on Module) and Carrier board, the board layout approach (signal routing requirements), recommendations can change. The recommendation is for customer to verify the below guidelines and also follow general SOM design and layout guidelines to address board level signal integrity concerns:

1. Signal connections (high speed, differential signals) between the SOM and the Carrier board (including polarity)
2. Selection of high speed connector (lower contact resistance and inductance) that does not affect the board functionality or performance when high speed signals transition between the boards

3. Provision for adequate number of ground pads between signals on the connectors are provided to shield the signals to optimize board performance (minimize concerns related to signal integrity)
4. The recommended or required terminations for memory and other high speed or low speed peripherals have been provided
5. Fail-safe operation requirements between SOM and the Carrier board signals have been addressed
6. Completeness of the circuit implementation connected across SOM and Carrier board
7. IO level compatibility between the SOM and Carrier board signals
8. Any of the processor IOs or attached device IOs interfaced to the processor that can float has provision for parallel pull and the polarity has been verified
9. The required simulations have been performed before start of board build (SOM and Carrier)

For additional input on high-speed design including SOM based design, refer below FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

5.3 Processor-Specific SDK

In case the custom board design is for a new platform or updates being made for a platform, the recommendation is to use the latest Version/ Revision of the software development tools on TI.com.

Refer below link to download the required SDK version:

AM62L-PROCESSOR-SDK

1. ***AM62L-FREERTOS-SDK:*** FreeRTOS SDK for AM62L family of devices
2. ***AM62L-LINUX-SDK:*** Linux SDK for AM62L family of devices

Refer to *AM62LX Software Build Sheet* (Build Sheet of supported features for AM62Lx processor family).

In case an older Version/Revision is being used, the recommendation is to verify the compatibility using the release notes or reach out to TI (through E2E).

5.4 General Design Recommendations (to Know) Before Starting the Custom Board Design

5.4.1 Processor Documentation

During the custom board design phase, the recommendation is to refer/use the latest version of the collaterals/ documentation, examples include the processor-specific data sheet, silicon errata, TRM, and other commonly referenced board design collaterals. Review the processor-specific product page on TI.com at frequent interval and look for latest available document revision or addition of new documents.

Tips for documentation search: Search the documentation for words such as: *recommended*, *require*, *do not*, *note*, *pin connectivity*, and so forth. Important criteria for the processor typically contain one or more words.

Tips to get updated information: On a TI.com processor product page, there is a ***Notifications* button**. Registering at the button enables automatic notification of processor documentation changes.

The latest revision of the processor-specific data sheet or other collaterals are available on TI.com. The recommendation is to archive the older revision internally for future use.

5.4.2 Processor Pin Attributes (Pinout) Verification

Verify the following attributes for the processor pins used in the custom board design:

- Processor pin number labeling and naming (pin number associated with the processor symbol section) corresponds to the correct pin numbers listed in the *Pin Attributes* section of the processor-specific data sheet. The recommendation is to maintain the processor-specific data sheet names internal to the symbol and change the function (net) names as per the application use case.
- Supply voltages that are connected to the processor power pins follow the *Recommended Operating Conditions*.
- All processor pins (grouped into functions and having separate symbol block) including reserved pins are included in the schematics to minimize tool related and functional errors.

- For a number of processor IOs TX (Output) and RX (Input) buffers are off and internal pulls (pullup and pulldown) are turned off during reset and after reset. External pulls (10kΩ or 47kΩ) are recommended to hold attached device input in a valid state until software initializes the IOs when trace is connected and IOs are not being actively driven. When a TP is connected to the processor IO, a parallel pull (10kΩ or 47kΩ) is recommended. When adding pull is not feasible, the recommendation is to route the traces away from high frequency signals.
- For improved custom board performance, consider provisioning for external measurement of processor supply rails (voltage), current draw for the supply rails and on-board temperature measurement at hot spots.

For queries related to processor-specific data sheet pin attributes, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to SOC data sheet Pin Attributes Excel format

5.4.3 Device Comparison, IOSET and Voltage Conflict

Availability of features listed in the comparison table are a function of IO pins configuration and required peripheral functions. The peripheral functions internally implemented are multiplexed to a limited number of pins. The recommendation is to use *SysConfig-PinMux* tool to assign the required signal functions to pins. The SysConfig-PinMux tool provides a better understanding of limitations associated with pin multiplexing.

Processor peripherals are timing closed using the IOs grouped as IOSETs. IOSETs are grouping of signals specific to an interface that are timing closed as a set. Any interface that has IOSETs is recommended to select all interface signals from the same IOSET. Some interface signals can be shared over multiple IOSETs. The valid combinations of pins for an IOSET supporting a specific peripheral are detailed in the *SysConfig-PinMux* tool.

Voltage Conflict:

Signals are grouped by functional IO domain, not by power domain. There is a possibility to encounter voltage conflict warnings with some peripheral IO configuration. The warning is to highlight difference between the preferred voltage and the configured voltage for IOs so custom board designer can take necessary action in case there is a real voltage conflict. The warning is most useful when grouping GPIO signals from different voltage domains since the current tool configuration only allows one preferred voltage per peripheral. Any peripheral that includes IOs (pins) with different voltages levels, a warning is shown. The warning is shown because the preferred voltage is a different level than the IO (pin) voltage (Example: Preferred voltage is 3.3V while the pin voltage is 1.8V). The warning can be suppressed as long as 1.8V is the intended voltage for selected IOs (pins). The indication of conflict is not a hardware issue or a tool bug, but a notification that the preferred voltage is different than IO (pin) voltage configured. The warning are there simply to highlight the conflict between preferred operating voltage and selected (configured) operating voltage. A long as you understand the reason for the conflict, the warnings can be suppressed.

For information on voltage conflict and IOSET, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to SysConfig-PinMux IOSET and Voltage Conflict

5.4.4 RSVD0 Reserved Pin (Signal)

Pin named RSVD0 is Reserved. The recommendation is to leave the RSVD0 pin unconnected (do not connect any PCB trace or test point (TP)) as recommended in the processor-specific data sheet.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L (AM62L32 , AM62L31): Custom board hardware design – Connection recommendations for RSVD or RSDV0 pins

5.4.5 Note on PADCONFIG Registers

A number of the processor IOs (LVCMOS or SDIO buffer type) support multiplexing of multiple (different) functions on the same pin. The required IO function can be chosen from the supported multiple functions. The list of functions available for each IO (pad) is listed in the *SIGNAL NAME* column in the *Pin Attributes* table of the processor-specific data sheet.

The required function is configured using the MUXMODE field of the relevant (associated) pad configuration register. The PADCFG_CTRL0_CFG0_PADCONFIG0 to PADCFG_CTRL0_CFG0_PADCONFIG146 registers support (can be used) the signal multiplexing of the IOs in the processor MAIN domain.

The *Description in the Pad Configuration Register Bits* table in *Pad Configuration Register Functional Description* subsection of the *Pad Configuration Registers* section of the processor-specific TRM summarizes the *Bit Field* description, supported configurations and the *Reset Values* for the PADCONFIG registers. The recommendation is to review and follow the notes listed at the end of the table while configuring the PADCONFIG registers. The recommendation is to not (never) set the RXACTIVE bit without a valid logic input being sourced to the pin that is associated with the respective PADCONFIG register. A floating input can damage the processor IO or affect the reliability of the processor. ST_EN bit is set by default. The recommendation is to verify the ST_EN bit and set the bit to 1 in case the bit value has been reset to 0. The recommendation is to not modify the default value of the bit. A summary of all the PADCONFIG registers default configuration is listed in the *Pad Configuration PADCONFIG Registers* table in the *Pad Configuration PADCONFIG Registers* subsection of *Pad Configuration Registers* section of the processor-specific TRM.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on PADCONFIG bits and PADCONFIG registers default values summary

5.4.6 Processor IO (Signal) Isolation for Fail-Safe Operation

The recommendation is to power the processor IO supply for IO group and the attached device (or FPGA or MCU or Processor) IO supply to the same power source to make sure there are no violations related to fail-safe operation. In case the processor and the attached devices or an additional processor are connected to (powered by) different power sources, signal isolation is recommended since many of the processor IOs are not fail-safe. The recommendation is to connect the signals through a FET bus switch circuit designed to isolate the two devices anytime the IO power is not valid for the device connected as input. The FET bus switch and control logic are recommended to be powered from an always-on power supply and only enabled by an AND function of power good signals from multiple (different) power sources.

5.4.7 Pin Connectivity Requirements and Reference to Processor-Specific EVM

The *Signal Description* and *Pin Connectivity Requirements* sections of processor-specific data sheet includes connection recommendations for peripherals, IOs and pins (functions) specific to processor family.

The processor-specific EVM can be referenced when the processor-specific data sheet does not include specific connection requirements.

5.4.8 Custom Board High-Speed Interface Design Guidelines

For recommendations on USB2.0 signals connection and routing, see the *High-Speed Interface Layout Guidelines*. The recommendation is to include appropriate constraints or notes related to the routing requirements to be followed during the custom board design.

For USB interface, adding common-mode is an option to improve the custom board USB interface noise immunity performance when the custom board is expected to operate in harsh industrial environments. Adding common-mode choke can reduce the signal amplitude and degrade USB interface performance (speed, data throughput, communication errors). The recommendation is to add provision to bypass the common-mode choke using 0Ω resistors. The recommendation is to add provision for external ESD protection for the USB interface and USB supply based on the application requirement.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

5.4.9 Recommendations for LVCMOS (GPIO) Output Current Source or Current Sink

The DC current output sourced by the processor IO configured as output needs to remain less than the maximum I_{OH} and I_{OL} values defined to achieve the V_{OL} maximum and V_{OH} minimum values defined in the *Electrical Characteristics* table. The output currents defined in the processor-specific data sheet shall not be used as limits for steady-state currents. The data sheet output current limits are only expected to be reached when charging or discharging signal capacitance to transition a signal from low to high or from high to low. Once the signal reaches a valid logic state, the steady-state current is expected to be much lower than the data sheet current limit values. The outputs can tolerate some level of steady-state current as required to over-drive typical pull resistors, but we do not expect large steady-state current like what is needed to drive an LED or similar load continuously. The recommendation is to use an external FET or transistor switch controlled by processor IO to drive LEDs or similar loads that can draw continuous current.

5.4.10 Connection of Slow Ramp Signal (Input) or Capacitor Load (Large Value at the IO Output) to Processor IOs

LVCMOS (SDIO) inputs have slew rate requirements specified (as part of the electrical specifications). Connecting slow ramp input (signal) directly to the LVCMOS (SDIO) inputs is not recommended. There can be long-term reliability issues (concerns) associate with the input buffer if the applied input (signal) spends more time in the voltage region between V_{IHSS} and V_{ILSS}. The transition time allowed (recommended) is <1000ns. The slew rate has frequency dependency. A maximum slew of 1000ns is recommended when the signals toggle rate is not high (non-frequency dependent limit). When IO is operating at 1.8V (as an example), the non-frequency dependent limit of 1.8E+6V/s becomes the larger value when the signal toggle rate is < 100kHz. The frequency dependent limit of 18fV/s (f = toggle frequency of the input signal in Hz) becomes the larger value when the signal toggle rates is >100kHz. When a slow ramp input is applied (when the input is at mid-supply), shoot-through current can flow from VDD through the partially turned on P-channel transistor and the partially turned on N-channel transistor to VSS. Accumulated exposure to slow ramp input results in IO performance, board performance or processor reliability concerns.

Connecting a large capacitor directly at the LVCMOS (SDIO) outputs is not recommended. LVCMOS (SDIO) output buffers are not designed to drive large capacitive loads. When LVCMOS (SDIO) type IOs are configured as output and a capacitor is connected at the output, the recommendation is to follow the processor-specific data sheet recommendations for the allowed capacitor value or add series resistor to limit the IO current draw. The recommendation is to perform simulations to finalize the capacitor value.

5.4.11 Queries Related to Processor and Processor Peripherals Design During Custom Board Design

During the custom board design, there can be questions (queries) related to processor and processor peripherals. The recommendation is to start an E2E query for queries related to processor and processor peripherals, for the device experts to support. The recommendation is to include queries related to a specific section of the design or peripheral or specific topic in an E2E query to minimize assignment and response delay.

5.4.12 General Design Recommendations (to Know) Before Starting the Custom Board Design Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Latest version of the selected EVM design collaterals are being referenced.
3. Relevant collaterals on TI.com are being referred to minimize errors (design efforts) during custom board design.
4. Processor schematics symbol used on custom board schematic follows the ball name, pin numbers as per the processor-specific data sheet Attributes section are followed.
5. IOSET grouping recommendations for specific peripherals are being followed (follow SYSCONFIG IOSET grouping)
6. The required IO functions and required PADCONFIG configurations have been considered.
7. Buffering of the processor IOs (outputs, based on the use case) - to drive higher load.
8. Fail-safe operation for processor IOs are considered.

9. Output capacitor load requirements, connected vs allowed verified through simulation or required analysis done
10. The recommendation is to frequently check the product page on TI.com for the latest documents revision (for the documents of interest).
11. The recommendation is to use E2E (to seek clarification rather than making assumptions).

5.4.13 Attached Devices Recommendations

TI does not make attached devices recommendations for custom board design.

The recommendation is to refer the *DDR Electrical Characteristics* section of the processor-specific data sheet for selection of DDR4 or LPDDR4 memory.

The MMCSD host controller and PHY associated with the MMC0 are designed to be compliant with the standard, as described in the processor-specific data sheet (and TRM). The recommendation is to refer the *MMC0 - eMMC/SD/SDIO Interface* section of the processor-specific data sheet when selecting the eMMC.

During the custom board design, as a starting point for information on key devices (components) used on the EVMs and SKs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key devices (components) list

6 Processor-Specific Recommendations for Power, Clock, Reset, Boot and Debug

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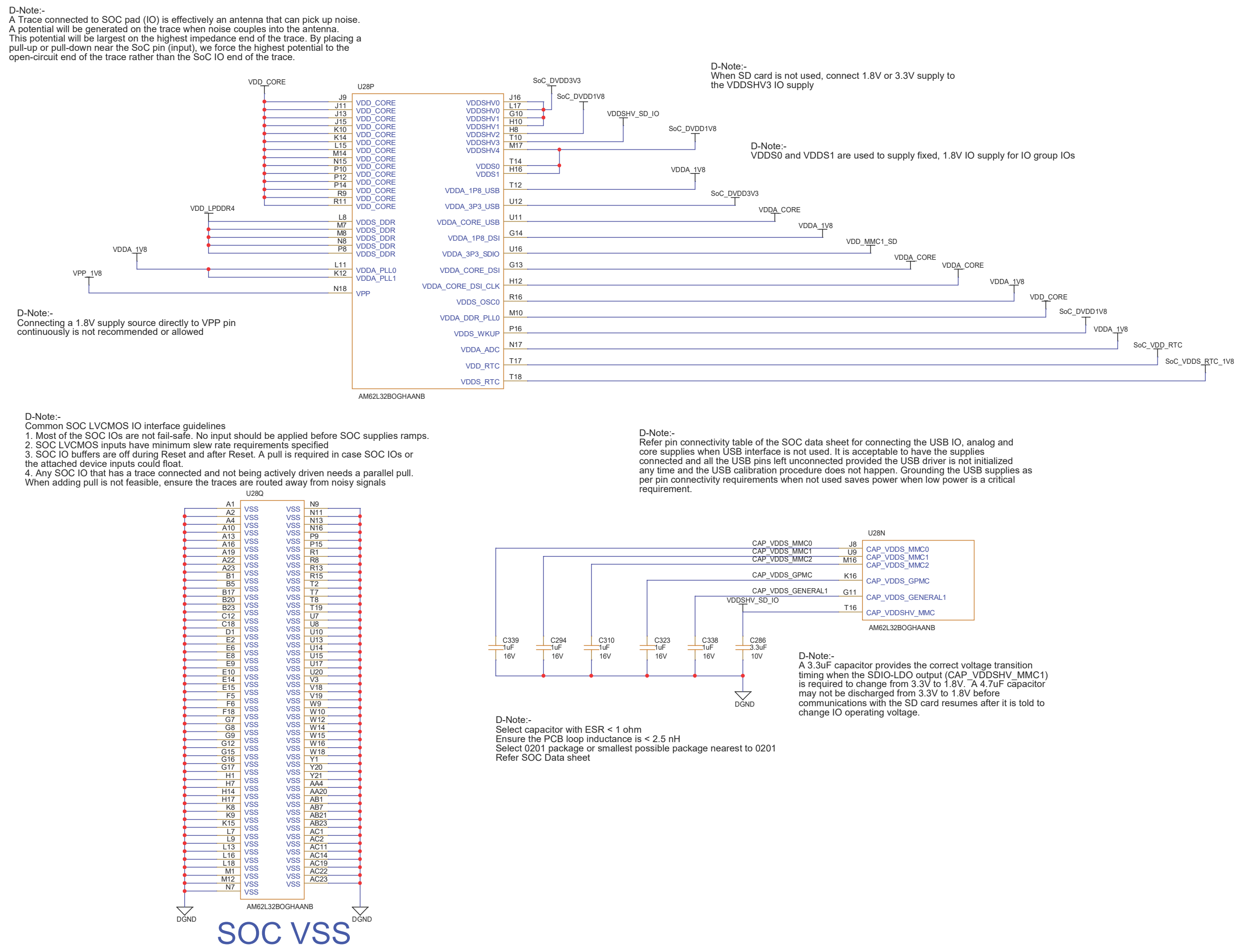
Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

6.1 Common (Processor Start-Up) Connections

6.1.1 Power Supply

Figure 6-1 includes connection of supply rails for the processor core supply and peripheral core supplies, DDR PHY IO supply, peripheral analog supplies, Fixed-voltage supply for processor IO group, Dual-voltage IO supply for IO group, RTC core supply and Fixed-voltage supply for LFOSC0 and RTC IO group.



D-Note:-
A Trace connected to SOC pad (IO) is effectively an antenna that can pick up noise.
A potential will be generated on the trace when noise couples into the antenna.
This potential will be largest on the highest impedance end of the trace. By placing a pull-up or pull-down near the SoC pin (input), we force the highest potential to the open-circuit end of the trace rather than the SoC IO end of the trace.

D-Note:-
When SD card is not used, connect 1.8V or 3.3V supply to the VDDSHV3 IO supply

D-Note:-
VDDS0 and VDDS1 are used to supply fixed, 1.8V IO supply for IO group IOs

D-Note:-
Connecting a 1.8V supply source directly to VPP pin continuously is not recommended or allowed

D-Note:-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before SOC supplies ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset and after Reset. A pull is required in case SOC IOs or the attached device inputs could float.
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note:-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note:-
A 3.3uF capacitor provides the correct voltage transition timing when the SDIO-LDO output (CAP_VDDSHV_MMC1) is required to change from 3.3V to 1.8V. A 4.7uF capacitor may not be discharged from 3.3V to 1.8V before communications with the SD card resumes after it is told to change IO operating voltage.

D-Note:-
Select capacitor with ESR < 1 ohm
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package nearest to 0201
Refer SOC Data sheet

Figure 6-1. Power Supply Rails

When selecting or designing the processor power architecture, the recommendation is to consider the below listed guidelines:

- The current (power) requirement for each of the supply rail varies based on the interfaces used and the operating environment.
- The current draw of processor supply rails is estimated using the *Power Estimation Tool (PET)* for a specific use case.
- In case the supply rail powers the other on-board attached (peripheral) devices, include the maximum current draw of the attached devices for sizing the supply rail.
- For power supply sizing the recommendation is to consider the maximum current for the processor supply rails. For information on the maximum current rating for different supply rails, the recommendation is to frequently check processor (AM62L) product page.
- The recommendation is to verify the output current ratings of the selected power architecture (including PMIC, discrete DC/DCs and discrete LDOs) meet the maximum current ratings of the selected processor and attached devices. The recommendation is to add additional margins for design or manufacturing variances.
- The recommendation is to verify if the power supply sequence (power-up and power-down) and supplies slew rate follows the processor-specific data sheet. For the recommended power sequencing requirements, refer to the *Power Supply Sequencing* section of processor-specific data sheet.

For more information about processor *Recommended Operating Conditions (ROC)*, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – SOC ROC Recommended Operating Condition

Below are some guidelines to consider when selecting or designing the processor power architecture:

1. Supply rails are configured to the required operating voltage level and the supply outputs are within the processor ROC.
2. Power architecture follows the power-up and power-down sequence as specified in the processor-specific data sheet.
3. Power architecture meets the slew rate requirements specified for the supply rails in the processor-specific data sheet.
4. All the power supplies ramp-up and are stable before the PORz input is released (deasserted).
5. The delay between the processor power supplies ramp up and the PORz input high follows the processor-specific data sheet recommendations (9.5ms min).
6. The recommendation is to make sure the supplies are enabled only when the supply voltages ramp-down below 300mV (no residual voltage) during cold reset.
7. All the supply rails decay below 300mV (There is no time or decay voltage tolerance associated with the requirement) before any of the power rail is allowed to ramp up after a power cycle.
8. PORz input slew is minimum to avoid internal reset circuit glitch (the recommendation is to connect the PORz input through discrete push-pull output type buffer with minimum slew).

For information on residual voltage and detection, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Residual Voltage, Detection and supply decay

Note

Read the note at the start of *Pin Connectivity Requirements* section of the processor-specific data sheet for connecting the supply rails and processor signals named RSVD0.

The recommendation is to verify the processor power pin mapping and connection of the recommended supplies including the voltage level. Follow the below FAQ to verify the pin mapping:

[FAQ] AM625 / AM623 / AM625-Q1 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Custom board hardware design - Processor pin mapping and SK board connections (Supply rail, Capacitors and ferrites).

6.1.1.1 Core and Peripherals Supplies

For proper operation, the recommendation is to connect all power supply pins (balls) with the supply voltages recommended in the *Recommended Operating Conditions* section of the processor-specific data sheet. Power supply pins that have specific connectivity requirements are listed in the *Pin Connectivity Requirements* section of the processor-specific data sheet.

The processor family supports connecting fixed 0.75V supply to VDD_CORE and peripheral core supply rails. Processor core supply VDD_CORE and peripheral core supplies VDDA_CORE_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 are recommended to be powered from the same power source. The recommendation is to configure the supply source to fixed 0.75V operation (specified nominal operating voltage as per the *Recommended Operating Conditions* (ROC)). Custom board designers are expected to take care that the voltage differential between VDD_CORE and VDDA_CORE_USB is within ±1%.

The recommendation is to always connect the VDDS_OSC0 supply.

The processor family supports multiple analog supply pins VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_ADC, VDDA_1P8_DSI, VDDA_1P8_USB that provides power supply to sensitive analog circuitry. Filtered (ferrite) power supplies are recommended for the analog supplies.

Connecting VDDA_3P3_USB to a 3.3V analog supply for supporting USB2.0 interface is recommended.

For more information, see the *Recommended Operating Conditions* and *Power Supply Sequencing* sections of the processor-specific data sheet.

6.1.1.1.1 Power Supply Ramp (Slew Rate) Requirement and Dynamic Voltage Scaling

The recommendation is to allow for controlled supply ramp (follow supply slew requirements) for all the processor power supplies. For more information, see the *Power Supply Slew Rate Requirements* section of the processor-specific data sheet.

The processor (family) does not support dynamic voltage scaling (change) for processor core, peripherals core and peripheral analog supplies.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Dynamic Voltage Scaling for SOC core (VDD_CORE), Peripheral Core and Analog supplies

6.1.1.1.2 Additional Information

For information on processor power-sequencing requirements, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Processor power-sequencing requirements for power-up and power-down

The FAQ is generic and can also be used for AM62Lx processor family.

For information on processor power supply rails filtering using ferrite, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails

The FAQ is generic and can also be used for AM62Lx processor family.

6.1.1.1.3 Processor Core and Peripheral Core Power Supply Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of processor core VDD_CORE and peripheral core VDDA_CORE_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 supply (fixed, 0.75V only)
3. ROC, slew rate as per processor-specific data sheet and voltage sequence requirements for processor core and peripheral core supply rails.
4. Addition of the required bulk and decoupling capacitors, and peripheral core supply filters.
5. Connection of peripheral core supply pins when specific peripherals are not used.
6. Connection of peripherals core supplies VDDA_CORE_DSI, VDDA_CORE_DSI_CLK (DSITX0) when peripheral is not used but boundary scan function is required.

Schematic Review

Follow the below list for the custom schematic design:

1. The recommendation is to compare the implementation of the bulk and decoupling capacitors for the supply rails with EVM schematic implementation or refer PDN application note
2. A fixed and recommended supply voltage of 0.75V is applied to the processor core VDD_CORE and peripheral core VDDA_CORE_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 supply rails
3. The supply rail operating voltage connected to processor core and peripheral core supplies follows the ROC
4. The recommendation is to connect supply rail VDDA_3P3_USB to a 3.3V supply for supporting USB 2.0 interface. The recommendation is to connect 3.3V supply voltage to VDDA_3P3_SDIO (same as output of SD card power control power switch that can be reset) integrated LDO input.
5. Ferrite filters are provided for peripheral core supplies (DSI, USB)
6. Connection of core supply when specific peripherals are not used as per pin connectivity requirements

7. Connection of core supply (VDDA_CORE_DSI, VDDA_CORE_DSI_CLK for DSITX0), when peripheral is not used but the boundary scan function is required, follow data sheet pin connectivity requirements

Additional

1. The recommendation is to add a 0Ω resistor or jumper for isolation or current measurement at the PMIC DC/DC or LDO output for the core supply. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection to connect the TPs. Choose the resistor package based on the supply rail current and the resistor current carrying capacity.
2. Dynamic voltage scaling (DVS) of core supplies is not supported (not recommended or allowed).
3. Changing the core voltage after the device is released from reset is not allowed. When the core supply is turned off, the recommendation is to ramp down all the power supply rails as per the power-down sequence and wait until all supply rails decay below 300mV before turning on power.
4. When USB driver is not initialized and the USB calibration procedure does not happen, connecting the supplies and leaving all of the USB pins for USB0, USB1, or both is acceptable. Grounding the USB supplies per pin connectivity requirements when both USB interfaces are not used reduces power when low power is a critical requirement.

6.1.1.1.4 Peripheral Analog Power Supply Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of recommended supply voltages to peripheral analog power supply rails VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_ADC, VDDA_1P8_DSI, VDDA_1P8_USB.
3. Connection of 3.3V USB analog supply VDDA_3P3_USB.
4. Processor supply ROC, slew rate as per processor-specific data sheet and voltage sequence requirements for peripheral analog supply rails.
5. Addition of the required bulk and decoupling capacitors, and peripheral analog supply filters
6. Connection of peripheral analog supply pins when specific peripherals are not used.
7. Connection of peripheral analog supply (for DSITX0), when specific peripherals are not used but boundary scan function is required.

Schematic Review

Follow the below list for the custom schematic design:

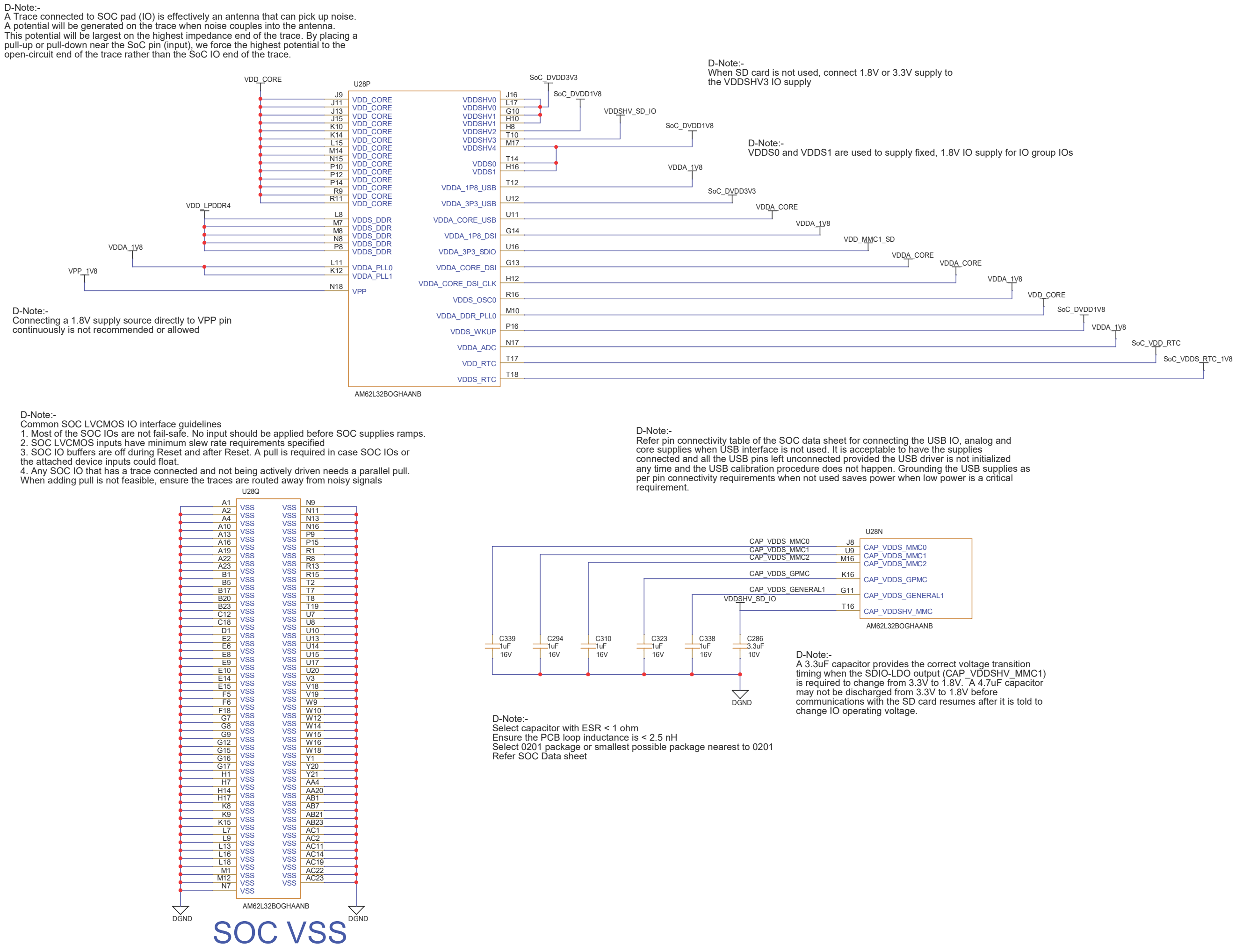
1. The recommendation is to compare the implementation of bulk and decoupling capacitor for the supply rails with EVM schematic implementation.
2. The supply rail operating voltage connected to peripheral supplies follows the ROC.
3. Recommended supply voltage 1.8V is connected to the peripheral analog power supply rails VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_ADC, VDDA_1P8_DSI, VDDA_1P8_USB.
4. The recommendation is to connect supply rail VDDA_3P3_USB to a 3.3V analog supply for supporting USB2.0 interface. The recommendation is to connect 3.3V to VDDA_3P3_SDIO (switched, same as output of SD card power control power switch) as integrated LDO input.
5. Slew rate of the analog supply rails follows the data sheet requirements.
6. Filters (ferrite) are provided for peripheral analog supplies (DSI, PLL, USB (1.8V), WKUP_OSC0), as per the EVM schematic implementation.
7. Connection of peripheral analog supply when specific peripherals are not used as per pin connectivity requirements.
8. Connection of peripheral analog supply (VDDA_1P8_DSI for DSITX0), when specific peripherals is not used but boundary scan function is required as per pin connectivity requirements. Ferrites and bulk capacitors are optional.

Additional

1. The recommendation is to add a 0Ω resistor or jumper for isolation or current measurement at the PMIC DC/DC or LDO output for the analog supply. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection to connect the TPs. Choose the resistor package based on the supply rail current and the resistor current carrying capacity.
2. Dynamic voltage scaling (DVS) of analog supplies is not supported (not recommended or allowed).
3. When USB driver is not initialized and the USB calibration procedure does not happen, connecting the supplies and leaving all of the USB pins for USB0, USB1, or both is acceptable. Grounding the USB supplies per pin connectivity requirements when both USB interfaces are not used saves power.

6.1.1.2 IO Supply for IO Groups

Figure 6-2 includes connection of external capacitors to SDIO_LDO (3.3uF) and General1, GPMC, MMC0, MMC1, MMC2 IO group (1uF).



D-Note:-
A Trace connected to SOC pad (IO) is effectively an antenna that can pick up noise.
A potential will be generated on the trace when noise couples into the antenna.
This potential will be largest on the highest impedance end of the trace. By placing a pull-up or pull-down near the SoC pin (input), we force the highest potential to the open-circuit end of the trace rather than the SoC IO end of the trace.

D-Note:-
When SD card is not used, connect 1.8V or 3.3V supply to the VDDSHV3 IO supply

D-Note:-
VDDS0 and VDDS1 are used to supply fixed, 1.8V IO supply for IO group IOs

D-Note:-
Connecting a 1.8V supply source directly to VPP pin continuously is not recommended or allowed

D-Note:-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before SOC supplies ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset and after Reset. A pull is required in case SOC IOs or the attached device inputs could float.
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note:-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note:-
A 3.3uF capacitor provides the correct voltage transition timing when the SDIO-LDO output (CAP_VDDSHV_MMC1) is required to change from 3.3V to 1.8V. A 4.7uF capacitor may not be discharged from 3.3V to 1.8V before communications with the SD card resumes after it is told to change IO operating voltage.

D-Note:-
Select capacitor with ESR < 1 ohm
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package nearest to 0201
Refer SOC Data sheet

Figure 6-2. External Capacitor CAP_VDDS_xxx for IO Group Connection

The below FAQ includes recommendations on CAP_VDDS_xxx capacitor value, and the effect of the capacitor assembly (mounted or shorted):

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to CAP_VDDSx CAP_VDDS

The processor family supports dual-voltage 1.8V/3.3V IO supply for IO groups and fixed-voltage 1.8V IO supply for IO groups supply rails for IOs.

The dual-voltage 1.8V/3.3V IO supply for IO groups are of two types and includes fixed 1.8V/3.3V IO supply for IO groups and dynamically switched 1.8V/3.3V IO supply for IO groups.

6.1.1.2.1 Dual-voltage 1.8V/3.3V IO Supply for IO Group

The processor family supports x5 (five) dual-voltage IO supply for IO group (VDDSHVx [x = 0:4]). Each IO supply for IO group is connected (referenced) to a fixed set of IOs. Each IO supply for IO group can be connected to fixed (VDDSHV2, VDDSHV3 and VDDSHV4 supports dynamic supply switching) 3.3V or 1.8V supply independently. The IO supply for IO group defines a common operating voltage for the entire set (fixed set) of IOs.

Processor pads (pins) designated as CAP_VDDS_xxx [total 5 pins], and CAP_VDDSHV_MMC connects the external capacitor to the internal IO supply for IO group supply when the IO supply for IO groups is connected to 3.3V supply (optional when IO supply for IO group is connected to 1.8V).

A 1µF (± 10% tolerance, voltage rating of 10V or above connected across CAP_VDDS_xxx pins and VSS, see the processor-specific data sheet) capacitor is recommended. For CAP_VDDS_xxx pins, the capacitor value is recommended to be within 0.8-1.5µF considering DC bias, tolerance, frequency and aging. When IO supply for IO groups are connected to 3.3V, the steady state DC output VDDSHVx/2, is the voltage to be considered for choosing the capacitor voltage rating considering the DC bias effect. A 3.3µF (recommended tolerance is ± 10%, voltage rating of 10V or above connected across CAP_VDDSHV_MMC and VSS). The capacitor value is recommended to be within 3.3µF ± 20% considering DC bias, tolerance, frequency and aging. See the processor-specific data sheet.

To minimize PCB loop inductance, place the capacitors on the back side of the PCB in the array of the BGA. The choice of capacitor voltage rating influences capacitor package (size) selection.

The recommendation is to select capacitor with ESR < 1Ω, keep the trace loop inductance < 2.5nH.

6.1.1.2.1.1 Dual-voltage IO Supply for IO Group Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. A valid fixed supply source is connected to (VDDSHV0, VDDSHV1) all the dual-voltage IO supply for IO groups as per the ROC of the processor-specific data sheet
3. A valid supply (that can be dynamically switched) source is connected to (VDDSHV2, VDDSHV3,VDDSHV4) all the dynamically switched dual-voltage IO supply for IO groups as per the ROC of the processor-specific data sheet
4. Slew rate requirements for IO supply rails for IO groups as per processor-specific data sheet are followed
5. Connection of recommended external capacitor to CAP_VDDS_xxx pin for IO supply for IO group (tolerance, voltage ratings - refer EVM schematics, connected across CAP_VDDS_xxx pin and VSS) when IO supply is 3.3V or 1.8V.
6. Connection of recommended external capacitor to CAP_VDDSHV_MMC for IO supply for SD card IO supply (tolerance, voltage ratings - refer EVM schematics, connected across CAP_VDDSHV_MMC pin and VSS)
7. Power sequence recommendations as per the processor-specific data sheet are followed

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the recommended capacitor to CAP_VDDS_xxx pins and VSS when IO supply for IO group is connected to 3.3V supply (optional when 1.8V supply is connected)
2. Voltage rating and tolerance of the selected capacitor for the capacitance value to be in the range 0.8 to 1.5µF including tolerance, aging, temperature drift and effect of DC bias
3. CAP_VDDS_xxx capacitor package (use the smallest possible (0201 or greater package possible which is closest to 0201) package to minimize loop inductance)
4. All IO supply rails for IO groups have a valid supply irrespective of the use of the IOs

5. Supply rails connected follow the ROC
6. Each CAP_VDDS_xxx pin requires a separate 1µF capacitor connected with respect to VSS (ground)
7. Select CAP_VDDS_xxx capacitor with < 1Ω ESR, keep the trace loop inductance < 2.5nH
8. The required bulk and decoupling capacitors are connected to IO supply for IO groups (follow EVM schematics)

Additional

1. For all supply rails, the recommendation is to use a 0Ω resistor or jumper for isolation or current measurement at the output of the supply rails. Choose the package of the resistor based on the supply rail current and the resistor current carrying capacitor.
2. When any of the VDDSHVx power rails are sourced from the 3.3V supply, all IOs referenced to the VDDSHVx are required to operate at 3.3V IO level. If a VDDSHVx power rail is sourced from a 1.8V supply, all IOs referenced to the VDDSHVx are required to operate at 1.8V IO level.
3. Some interfaces span over multiple VDDSHVx. When using any of the interfaces, all VDDSHVx domains supporting a specific interface are required to share the same voltage source.
4. Most processor IOs are not fail-safe. Applying input voltage to the IOs while the corresponding VDDSHVx supply is off is not recommended or allowed.
5. Verify all IO pins on each VDDSHVx only connects to a single voltage level.
6. Follow the processor-specific EVM for implementation of ferrites and capacitors.
7. Leaving VDDSHVx rail unconnected is not recommended. Connect the power pins to either 1.8V or 3.3V, depending on the use case and the ROC.

6.1.1.2.2 Fixed-voltage 1.8V IO Supply for (Peripheral) IO Groups

The processor family supports 3 Fixed-voltage 1.8V IO supply for IO groups supplies (VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC) where each domain provides power supply to a fixed set of IOs.

These are 1P8-LVCMOS buffer type. The custom board designers are responsible for interfacing the IOs referenced to fixed-voltage 1.8V IO supply for IO groups to attached devices with 1.8V IO levels.

6.1.1.2.2.1 Fixed-voltage 1.8V IO Supply for (Peripheral) IO Groups Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Connection of Fixed-voltage supply for general IO (VDDS0, VDDS1), WKUP and RTC IO group
3. ROC, voltage sequence as per processor-specific data sheet and slew rate requirements for processor fixed voltage supply for IO groups
4. Addition of the required bulk and decoupling capacitors for fixed voltage supply IO groups

Schematic Review

Follow the below list for the custom schematic design:

1. All IO supply rails for IO groups have a valid supply connected, irrespective of the use of the IOs
2. Supply rails connected follow the processor ROC
3. Supply levels of the IOs matches VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC fixed voltage supply for IO groups
4. Slew rate requirements are followed as per the processor requirements
5. Power sequence recommendations as per the processor-specific data sheet are followed

Additional

1. All IOs referenced to the VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC are required to operate at 1.8V IO level
2. A number of processor IOs are not fail-safe. Applying input voltage to the IOs while the corresponding VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC supplies are off is not recommended or allowed.

3. The recommendation is to verify all IO pins on each VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC only connects to 1.8V voltage level.
4. The recommendation is to follow the processor-specific EVM for implementation for adding ferrites and capacitors
5. Leaving VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC rails unconnected is not recommended. The recommendation is to connect the power pins to 1.8V.

6.1.1.2.3 Additional Information

A number of processor IOs are not fail-safe. For information on available fail-safe IOs, see the processor-specific data sheet. The recommendation is to connect the IO supply of attached devices to the same power source connected to the respective processor IO supply for IO group (VDDSHVx or VDDSx or VDDS_WKUP or VDDS_RTC) to make sure the custom board design never applies potential to any of the processor IOs that is not powered. Applying external input to the IOs that are not fail-safe when IO supply for IO groups supply is not available can affect the processor functionality, performance and reliability.

For more information on power-sequencing requirements between the processor and attached devices including signal isolation for fail-safe operation, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices (Fail-safe)

The FAQ is generic and can also be used for the AM62Lx processor family.

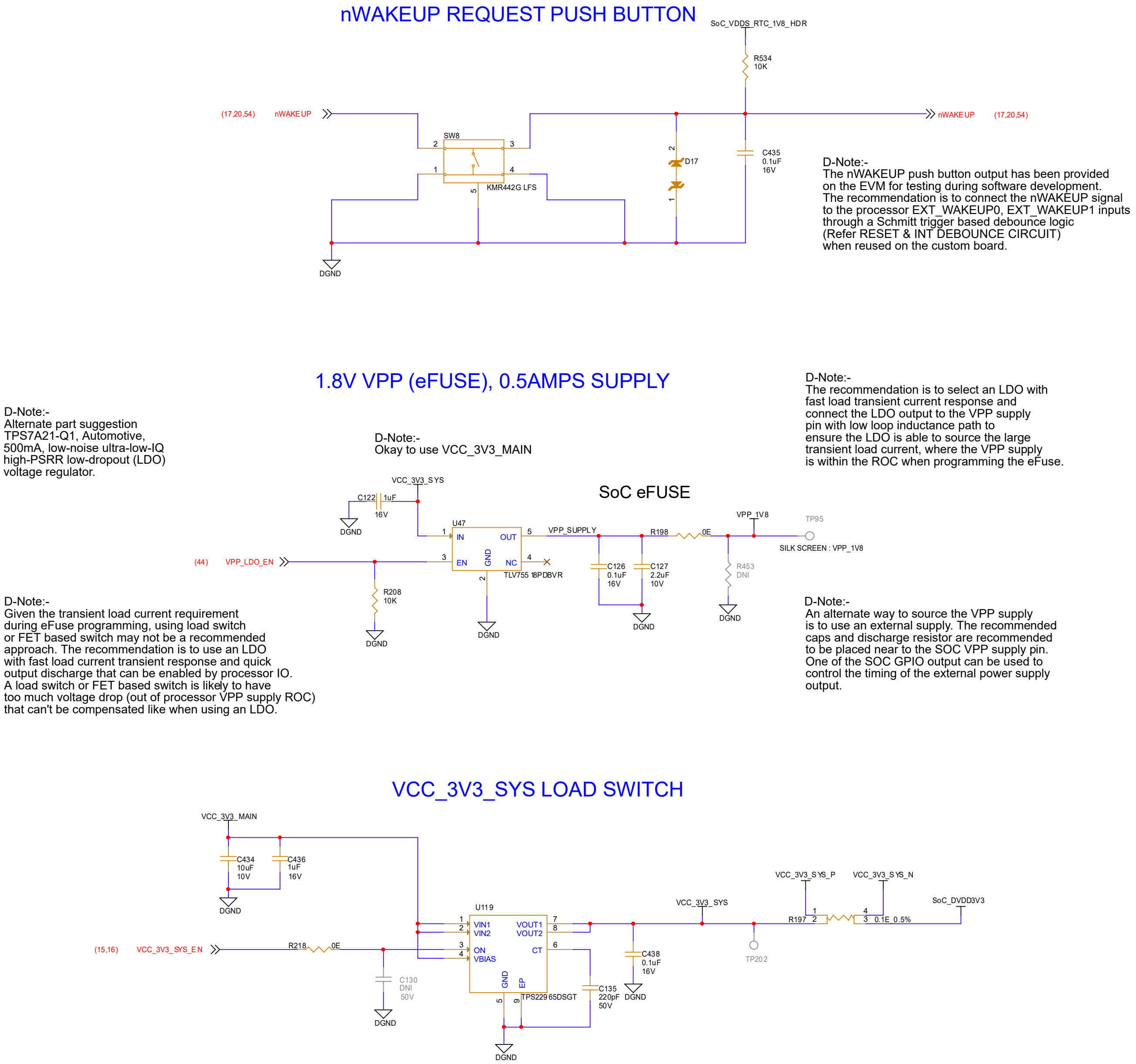
Note

The recommendation is to verify that a valid supply voltage for the VDDSHVx or VDDSx or VDDS_WKUP is present before applying input to the associated processor IOs or peripherals.

The recommendation is to connect the VDDSHVx supplies and associated CAP_VDDS_xxx (when IO supply connected is 3.3V, optional for 1.8V) capacitor irrespective of the usage of the processor IOs or peripherals.

6.1.1.3 Supply for VPP (eFuse ROM Programming)

Figure 6-3 includes VPP_1V8 supply generation LDO U47, VPP_LDO_EN signal (IO) with a pulldown (LDO is expected to be disabled normally), bulk + decoupling capacitor at the LDO output to support transient load current and 0R at the LDO output to isolate the VPP supply pin for testing the LDO output voltage value, timing.



nWAKEUP REQUEST PUSH BUTTON

D-Note:-
The nWAKEUP push button output has been provided on the EVM for testing during software development.
The recommendation is to connect the nWAKEUP signal to the processor EXT_WAKEUP0, EXT_WAKEUP1 inputs through a Schmitt trigger based debounce logic (Refer RESET & INT DEBOUNCE CIRCUIT) when reused on the custom board.

1.8V VPP (eFUSE), 0.5AMPS SUPPLY

D-Note:-
Alternate part suggestion
TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator.

D-Note:-
Okay to use VCC_3V3_MAIN

D-Note:-
The recommendation is to select an LDO with fast load transient current response and connect the LDO output to the VPP supply pin with low loop inductance path to ensure the LDO is able to source the large transient load current, where the VPP supply is within the ROC when programming the eFuse.

SoC eFUSE

D-Note:-
Given the transient load current requirement during eFuse programming, using load switch or FET based switch may not be a recommended approach. The recommendation is to use an LDO with fast load current transient response and quick output discharge that can be enabled by processor IO.
A load switch or FET based switch is likely to have too much voltage drop (out of processor VPP supply ROC) that can't be compensated like when using an LDO.

D-Note:-
An alternate way to source the VPP supply is to use an external supply. The recommended caps and discharge resistor are recommended to be placed near to the SOC VPP supply pin.
One of the SOC GPIO output can be used to control the timing of the external power supply output.

VCC_3V3_SYS LOAD SWITCH

Figure 6-3. eFuse LDO and EN Control

VPP (eFuse ROM programming) supply used for programming the processor eFuse is recommended to be sourced (powered) from a separate LDO that support the required (refer processor-specific data sheet) load current, load current transient and active (quick) output discharge. The LDO is recommended to be enabled only during eFuse programming. VPP operating voltage is required to be within the ROC range during eFuse programming. An LDO powered from a higher input voltage (2.5V or 3.3V) is recommended to compensate for the voltage drop through the series pass transistor and maintain the correct operating voltage during high load current transients. Local bulk capacitors are recommended near the processor VPP pin to support the LDO transient response.

Powering VPP supply rail from a supply rail with a variation outside the ROC (±5%), or using a Load switch or FET based switch can be a concern due to high load current transients and the requirement for the VPP supply rail be within the processor supply ROC. Load switch or FET based switch topology does not account for the voltage drop going through the load switch. The load switch can be an option if the custom board designer uses power source with smaller variation (compared to ROC), such that the supply variation combined with the voltage drop through the load switch never exceeds the VPP recommended operating range. As an alternate approach, an external supply for programming the eFuse can be used. The supply requirements are similar to the on-board LDO and the recommendation is to time the external supply EN (enable) using one of the processor IO. When external VPP supply is used, the recommendation is to provision for the bulk and decoupling capacitor on the processor board near to VPP supply pin.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application

The FAQ is generic and can also be used for AM62Lx processor family.

AM625 / AM623 / AM625-Q1 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Custom board hardware design – Queries regarding VPP eFuse programming current waveform

6.1.1.3.1 Supply for VPP Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Implementation approach of VPP supply (LDO (recommended) or Load Switch/FET based switch (Not allowed))
3. Supply within the Recommended operating conditions for the load (current) transient during OTP eFuse programming
4. Provision for isolation of VPP supply connected to processor for testing
5. Control of VPP supply generation LDO output (LDO EN)
6. Recommended bulk and filter capacitors to support current transient and optimize discharge time
7. Connection recommendations when external supply is used as VPP supply
8. External VPP supply timing control
9. External VPP supply sequencing
10. Connecting the VPP supply to a continuous 1.8V supply rail is not recommended or allowed or a supported option.

Schematic Review

Follow the list below for the custom schematic design:

1. Recommended bulk and filter capacitors are provided (follow EVM schematic implementation).
2. Processor supply rail connected to the VPP supply (for eFuse programming) follows the processor ROC.
3. Implementation of on-board supply or provision to connect external supply with the bulk and decoupling capacitors added on the processor board.
4. A fixed output LDO or PMIC output (maximum current of 400mA) is recommended (use of FET based switch or Load switch is not recommended or allowed).
5. Choose on-board LDO that with nominal voltage of 1.8V and supports a minimum current of 400mA, has good load current transient response, and quick output discharge (active discharge) capability. Follow the LDO specs used on the EVM schematics.
6. When an adjustable LDO is used, the recommendation is to verify the output voltage configuration, output voltage accuracy, output voltage slew and use of output over voltage protection (zener).
7. Processor IO is used to control the EN of the LDO and the recommended pull is provided.
8. The recommendation is to verify if EN pull holds the LDO in off-state during and after power cycling.
9. When external supply is connected, the recommendation is to add bulk and decoupling capacitor provision on the processor board near to the processor VPP pin and provided a TP to connect the external supply.
10. External VPP supply (when used) follows the recommended power sequence and slew rate requirements as per the processor-specific data sheet.

Additional

1. The recommendation is to always provide provision on the processor board to connect VPP supply (on-board or external supply).
2. The recommendation is to connect LDO output to the processor VPP pin with a low loop inductance path to source the high load current transients, where the supply on the VPP pin never drops below the minimum operating voltage.
3. Series resistor or jumper is provided to isolate the processor VPP supply from the LDO output for testing the timing or LDO output. The resistor package is expected to be rated for current > 400mA.
4. When an adjustable output LDO is used, consider adding an external zener based over voltage protection at the LDO output and provide provision to isolate the LDO output connected VPP supply pin to test the LDO output.
5. Due to the load current transient requirement during eFuse programming, using load switch or FET based switch is not recommended. A load switch or FET based switch is likely to have higher voltage drop that is not compensated.
6. In case the use case requires use of load switch or FET based switch, the recommendation is to characterize the board performance by measuring the voltage on the processor VPP pin during programming and verify that VPP supply never drops below the ROC minimum value. Several variables in the path of VPP supply can cause the supply to be out of the ROC and are required to be characterized before implementing. Check if the load switch or FET based switch violates the maximum VPP supply slew rate requirement defined in the processor-specific data sheet.
7. The recommendation is to leave the processor VPP supply pin floating (Hi-Z) or connect to ground during power-up sequences, power-down sequences, and normal device operation.

6.1.1.4 Supply Connection for Configuring Low-Power Modes

Refer to *AM62L Power Supply Implementation* application note on processor product page for description of AM62L power architecture implementation for different application use cases and low-power modes.

Refer below FAQ for information related to RTC and Low-Power modes implementation:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design - Queries related to Real-Time Clock (RTC) timer module RTC, Supported Low-Power Modes and Hardware implementation, and EXT_WAKEUP0..1 inputs

The low-power modes supported by the processor family are listed below:

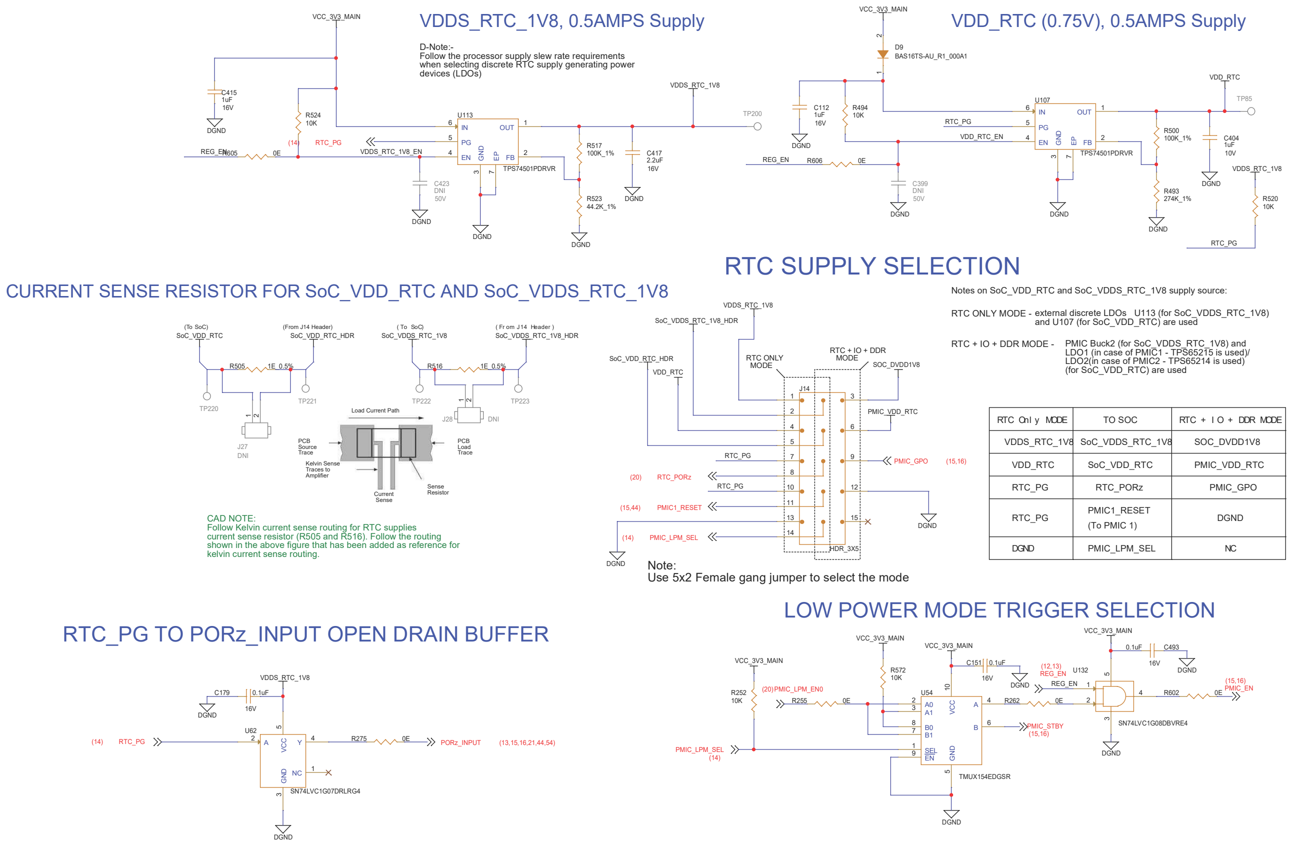
6.1.1.4.1 External Wakeup Inputs (EXT_WAKEUP0 and EXT_WAKEUP1)

EXT_WAKEUP0 and EXT_WAKEUP1 signals are the External Wakeup Inputs.

For connecting the EXT_WAKEUP0 and EXT_WAKEUP1 inputs, see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

6.1.1.4.2 RTC Only Low-power Mode

Figure 6-4 includes discrete LDO for generation of VDD_RTC and VDDS_RTC to support RTC only low power mode. Shunts R505 and R516 are provided to measure the RTC low power mode current or for isolation.



D-Note:-
Follow the processor supply slew rate requirements when selecting discrete RTC supply generating power devices (LDOs)

CAD NOTE:
Follow Kelvin current sense routing for RTC supplies current sense resistor (R505 and R516). Follow the routing shown in the above figure that has been added as reference for kelvin current sense routing.

Notes on SoC_VDD_RTC and SoC_VDDS_RTC_1V8 supply source:

RTC ONLY MODE - external discrete LDOs U113 (for SoC_VDDS_RTC_1V8) and U107 (for SoC_VDD_RTC) are used

RTC + IO + DDR MODE - PMIC Buck2 (for SoC_VDDS_RTC_1V8) and LDO1 (in case of PMIC1 - TPS65215 is used)/ LDO2(in case of PMIC2 - TPS65214 is used) (for SoC_VDD_RTC) are used

RTC Only MODE	TO SOC	RTC + IO + DDR MODE
VDDS_RTC_1V8	SoC_VDDS_RTC_1V8	SOC_DVDD1V8
VDD_RTC	SoC_VDD_RTC	PMIC_VDD_RTC
RTC_PG	RTC_PORz	PMIC_GPO
RTC_PG	PMIC1_RESET (To PMIC 1)	DGND
DGND	PMIC_LPM_SEL	NC

Note:
Use 5x2 Female gang jumper to select the mode

Figure 6-4. RTC-only LowPower Mode Supply

Refer EVM schematics for implementation of RTC only low-mode power architecture using discrete supplies.

Refer the power sequence diagram (*RTC Only Low-Power Mode Sequencing*) in the processor-specific data sheet for implementing the RTC only low-power mode.

6.1.1.4.2.1 RTC Only Mode Used

An always ON supply is recommended to be connected to VDDS_RTC (1.8V) and VDD_RTC (0.75V). VDDS_RTC and VDD_RTC needs to be available, ramp up and be stable before RTC_PORz is released. There is no supply sequencing requirement between VDDS_RTC and VDD_RTC.

The only firm sequencing requirement for the AM62Lx processor is VDD_RTC up before and down after VDD_CORE.

A valid clock source as per the processor-specific data sheet recommendations need to be connected to LFOSC0_XI and LFOSC0_XO (crystal) or LFOSC0_XI (LVCMOS).

6.1.1.4.2.1.1 RTC_PORz Delay When RTC Only Mode is Used

VDD_RTC and VDDS_RTC power rails are required to be valid before RTC_PORz goes high. There is no specific delay requirement and so the PG (power good) output of the supply source (VDD_RTC and VDDS_RTC) can be connected as RTC_PORz input.

6.1.1.4.2.1.2 EVM Implementation of RTC Only Mode Power Supply Architecture

VDD_RTC is expected to ramp up before VDD_CORE supply and ramp down after VDD_CORE supply. A diode can be used at the input of the discrete LDO used to generate VDD_RTC. Without the diode the VDD_RTC power rail can decay at the same time or before VDD_CORE when there is a uncontrolled power down, where the system power supply is turned off or disconnected from the board.

The VDD_RTC power domain does not draw much power, so the input capacitors on the VDD_RTC LDO holds the VDD_RTC rail valid for a longer time when the supply is isolated from the input power supply using a diode.

6.1.1.4.2.2 Low-Power Mode not Used (RTC Only or RTC + IO + DDR)

For custom board designs, where any of the low-power modes (RTC only or RTC + IO + DDR) are not used, VDD_RTC can be connected to the same 0.75V supply source that is connected to VDD_CORE. VDDS_RTC can be connected to the same 1.8V power supply source connected to VDDS_OSC0.

RTC_PORz can be connected to the same reset source that is connected to PORz.

6.1.1.4.2.2.1 32kHz LFOSC0 Clock When RTC Mode is not Used

The low-frequency oscillator is optional (not required to be connected) when none of the low-power modes are being (RTC) used. Follow the connection recommendation in the processor-specific data sheet when LFOSC0 is not used.

6.1.1.4.2.3 RTC Only Low-power Mode Checklist

General

Review and verify the following for the custom schematic design:
1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Connection of always ON (discrete, LDO) supplies for VDD_RTC and VDDS_RTC
3. Connection of the combined PG output of VDD_RTC and VDDS_RTC supplies to RTC_PORz input
4. VDD_RTC and VDDS_RTC, supply slew
5. Addition of 22pF glitch filter near to RTC_PORz input
6. Slew of the discrete LDOs PG output connected to RTC_PORz input
7. Sequencing of the VDD_RTC supply with respect to VDD_CORE

Schematic Review

Follow the below list for the custom schematic design:
1. Use of always ON discrete LDO supplies for VDD_RTC and VDDS_RTC
2. Supply outputs are within the ROC as per the processor-specific data sheet
3. VDD_RTC supply ramps before VDD_CORE
4. VDD_RTC and VDDS_RTC supply slew rate follows the data sheet specifications
5. Discrete LDOs of PG outputs for VDD_RTC and VDDS_RTC connected together
6. Connection of PG output of discrete LDOs to RTC_PORz input

Additional
1. Note the use of diode at the input of discrete LDO input to sequence the VDD_RTC supply

6.1.1.4.3 RTC + IO + DDR Self-refresh Low-power Mode

6.1.1.4.3.1 RTC + IO + DDR Low-Power Mode Used

Refer the power sequence diagram (*RTC + IO + DDR Low-Power Mode Sequencing*) in the processor-specific data sheet for implementing the RTC + IO + DDR low-power mode.

When TI PMIC based power architecture is implemented, there is a change in the NVM configuration and the supply rails generated by the PMIC for LPDDR4 or DDR4.

Refer EVM schematics for power architecture using PMIC and discrete logic to implement RTC + IO + DDR functionality for LPDDR4.

6.1.1.4.3.2 Low-Power Mode not Used (RTC Only or RTC + IO + DDR)

For custom board designs, where any of the low-power modes (RTC only or RTC + IO + DDR) are not used, VDD_RTC can be connected to the same 0.75V supply source that is connected to VDD_CORE. VDDS_RTC can be connected to the same 1.8V power supply source connected to VDDS_OSC0.

RTC_PORz can be connected to the same reset source that is connected to PORz.

6.1.1.4.3.3 RTC + IO + DDR Self-refresh Low-power Mode Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Selection of the PMIC version (OPN) based on use of LPDDR4 or DDR4 memory
3. Connection of VDD_RTC and VDDS_RTC supplies (using PMIC output or discrete LDOs or DC/DC based on the PMIC version (OPN) selected)
4. Connection of the power good outputs from PMIC (IO used for RTC_PORz depends on the PMIC version (OPN)) to processor PORz, RTC_PORz
5. Connection of processor PMIC_LPM_EN0 signal to PMIC
6. Discrete LDO PG output slew follow processor slew requirements

Schematic Review

Follow the below list for the custom schematic design:

1. Use of discrete LDOs for VDD_RTC and VDDS_RTC based on the PMIC version
2. VDD_RTC and VDDS_RTC supply slew rate follows the data sheet requirements when discrete LDOs are used
3. Discrete LDOs PG outputs for VDD_RTC and VDDS_RTC connected together
4. Connection of RTC_PORz input from the PMIC output or the discrete LDOs PG output
5. Discrete LDOs PG output slew follows processor-specific requirements
6. Supply output is within the ROC as per the processor-specific data sheet
7. VDD_RTC supply ramps before VDD_CORE
8. Connection of processor PMIC_LPM_EN0 to PMIC STBY input

6.1.1.4.4 DeepSleep, Standby

Implemented using software. Refer processor-specific TRM or refer to the processor-specific (AM62L) product page on TI.com for available application notes.

6.1.1.5 Additional Information

Placement of 0Ω resistor (shunt) or a jumper in line with the core supply and other supply rails are recommended for initial board builds. 0Ω resistor (shunt) or jumper can be used during board bring-up and debug to isolate the supply or for current measurement. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connections for connecting the TP to the resistor or jumper.

Shunt resistor connected to INA (instrumentation amplifier) following kelvin sense connection are used to measure the supply rails current in EVM.

The recommendation is to verify the effect of adding 0Ω resistor (shunt) provision on the custom board performance (voltage drop in cases shunt (resistor) value in milliohm (mΩ) is used for measurement).

6.1.2 Capacitors for Supply Rails

6.1.2.1 AM62Lx Processor Family

The recommendation is to verify that the required number of decoupling and bulk capacitors including value are provided for all power supply rails, including dual-voltage and fixed-voltage IO supply for IO group supply rails.

The recommendation is to place the decoupling capacitors close to the processor supply pins. Larger bulk capacitors can be placed further away.

The recommendation is to use Low-ESL capacitors and the recommendation is to connect the capacitors with the shortest possible traces to keep the loop inductance minimal. For more information, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

As a starting point the recommendation is to follow the EVM schematic implementation, for bulk and decoupling capacitors. Performing simulation (PDN analysis) is recommended to optimize the use of capacitors. For filtered (ferrite) power supplies implementation, follow the processor-specific EVM. Additionally, follow the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

6.1.2.2 Additional Information

When any of the processor peripheral instances (DDR Subsystem (DDRSS0), DSI0 and USB2.0 (USB0 and USB1)) are not used, the supplies (peripheral core, analog) associated with the peripherals have specific connectivity requirements. For more information, see the *Pin Connectivity Requirements* section of the processor-specific data sheet. Power supply filter (ferrite) and capacitors (bulk) are optional.

6.1.2.3 Capacitors for Supply Rails Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Addition of the required number of bulk and decoupling (high frequency) capacitors and ferrite filters
3. Package and value used for the capacitors
4. Voltage rating of the capacitors used considering derating (> twice the worst-case applied voltage is a commonly used guideline)

Schematic Review

Follow the below list for the custom schematic design:

1. All processor power rails use bulk and high frequency decoupling capacitors. The critical power domains that require the focused attentions are the low voltage, high current domains (VDD_CORE).
2. As a starting point, the recommendation is to follow the validated EVM, or PDN application note. When there is difference between the EVM and PDN, the recommendation is to follow the PDN. When information is not available in the PDN, follow the EVM implementation.
3. The recommendation is to use Low-ESL capacitors connected with short traces to minimize the PCB trace loop inductance.
4. The recommendation is to verify each of the power rail pins has a decoupling capacitor and each of the supply rail group has a bulk capacitor.
5. Voltage rating of the capacitors used (> twice the worst-case applied voltage is a commonly used guideline).

Additional

1. In case difference is observed between the EVM and the PDN application note on the capacitor number recommendation and value, the recommendation is to consider the recommendations in the PDN application note
2. While optimizing the capacitors, the recommendation is to perform static and dynamic PDN analysis to verify that the Reff, Cap LL, and Impedance targets are met
3. In some situations, the EVM uses 3-terminal capacitors, due to low inductance packaging. Make sure the 3-terminal capacitors connections are not implemented as an in-line or filter component
4. The recommendation is to show the connections of the capacitor near to the relevant pin for ease of placement and routing

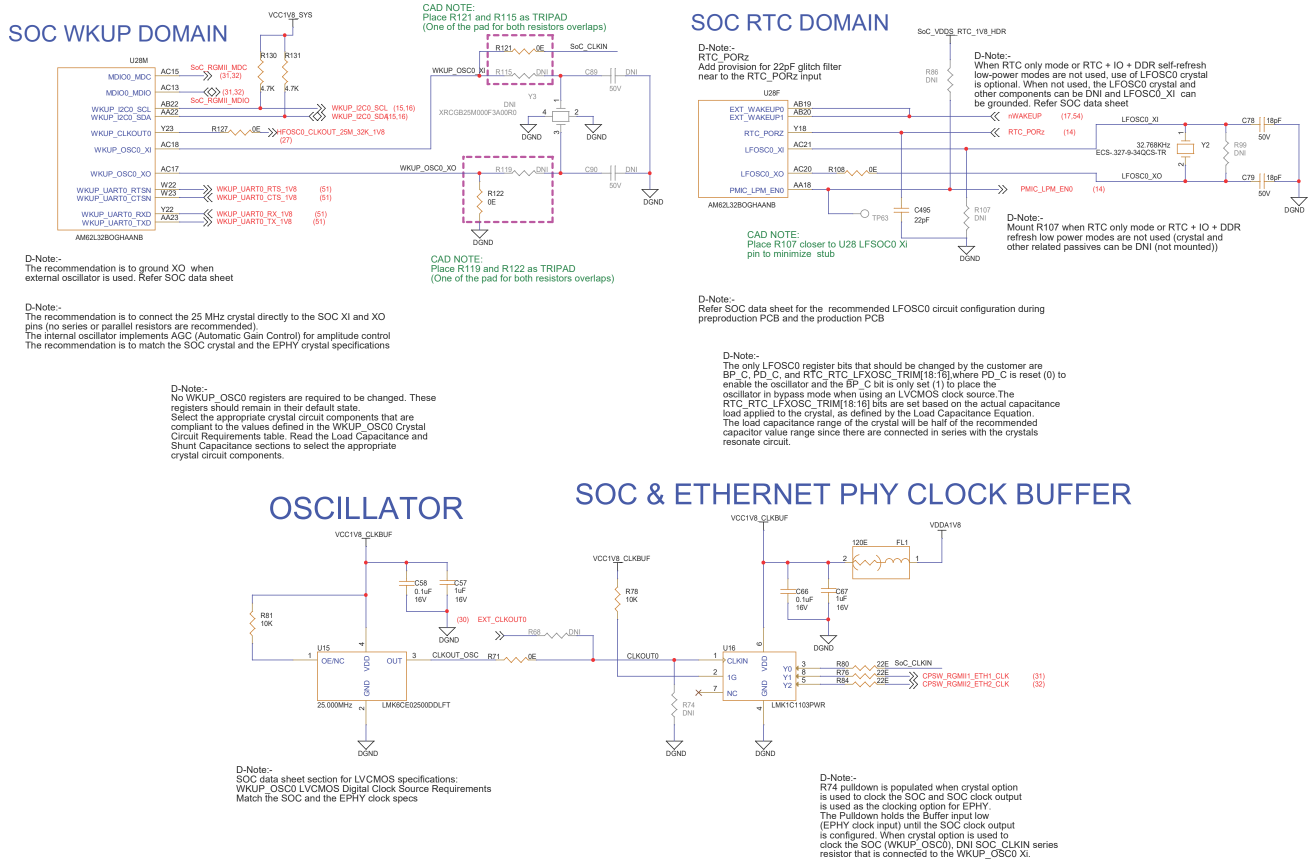
6.1.3 Processor Clocks (Inputs / Outputs)

6.1.3.1 Clock Inputs

6.1.3.1.1 WKUP_OSC0 (High Frequency) Clock (Internal Oscillator) or LVCMOS Digital Clock (External Oscillator)

Figure 6-5 includes WKUP_OSC0 clocking options including Crystal + Internal Oscillator and LVCMOS external oscillator. U15 is the external oscillator (Low Jitter, High-Performance BAW Oscillator) and U16 is the LVCMOS Clock Buffer (single input, 3 output) and the outputs of the clock buffer is connected to the processor and x2 EPHYs. External oscillator and low jitter buffer are populated when external clock input is used as the clocking option (currently implemented).

The load capacitors for the crystal and the crystal are included in the design (schematic) but is not populated. The clock source can be reconfigured to crystal based on the use case.



CAD NOTE:
Place R121 and R115 as TRIPAD
(One of the pad for both resistors overlaps)

CAD NOTE:
Place R119 and R122 as TRIPAD
(One of the pad for both resistors overlaps)

D-Note:-
The recommendation is to ground XO when external oscillator is used. Refer SOC data sheet

D-Note:-
The recommendation is to connect the 25 MHz crystal directly to the SOC XI and XO pins (no series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control
The recommendation is to match the SOC crystal and the EPHY crystal specifications

D-Note:-
No WKUP_OSC0 registers are required to be changed. These registers should remain in their default state.
Select the appropriate crystal circuit components that are compliant to the values defined in the WKUP_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

D-Note:-
RTC_PORz
Add provision for 22pF glitch filter near to the RTC_PORz input

D-Note:-
When RTC only mode or RTC + IO + DDR self-refresh low-power modes are not used, use of LFOSC0 crystal is optional. When not used, the LFOSC0 crystal and other components can be DNI and LFOSC0_XI can be grounded. Refer SOC data sheet

CAD NOTE:
Place R107 closer to U28 LFSOC0 Xi pin to minimize stub

D-Note:-
Mount R107 when RTC only mode or RTC + IO + DDR refresh low power modes are not used (crystal and other related passives can be DNI (not mounted))

D-Note:-
Refer SOC data sheet for the recommended LFOSC0 circuit configuration during preproduction PCB and the production PCB

D-Note:-
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and RTC_RTC_LFXOSC_TRIM[18:16],where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source.The RTC_RTC_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation.
The load capacitance range of the crystal will be half of the recommended capacitor value range since there are connected in series with the crystals resonate circuit.

D-Note:-
SOC data sheet section for LVCMOS specifications:
WKUP_OSC0 LVCMOS Digital Clock Source Requirements
Match the SOC and the EPHY clock specs

D-Note:-
R74 pulldown is populated when crystal option is used to clock the SOC and SOC clock output is used as the clocking option for EPHY.
The Pulldown holds the Buffer input low (EPHY clock input) until the SOC clock output is configured. When crystal option is used to clock the SOC (WKUP_OSC0), DNI SOC_CLKIN series resistor that is connected to the WKUP_OSC0 Xi.

Figure 6-5. WKUP_OSC0 Clock Connections

WKUP_OSC0 25MHz (mandatory) reference clock is required for the processor to operate. The clock is used internally to generate a number of clocks that are required for the processor to operate. The other clock inputs depends on specific end equipment or board functionality implemented. Clocking option supported includes external crystal + internal oscillator or external 1.8V LVCMOS square-wave digital clock source. Spread spectrum clocking (clock input) is not a supported clock option.

In case 25MHz external crystal connected to the internal high frequency oscillator (WKUP_HFOSC0) is the clock source for the internal processor operation, the recommendation is to place the discrete load capacitors used to implement the oscillator circuit close to the WKUP_OSC0_XI and WKUP_OSC0_XO pins. When crystal based oscillator is implemented, the recommendation is to follow the *WKUP_OSC0 Crystal Circuit Requirements* table of the processor-specific data sheet for choosing the load capacitors. The load capacitor capacitance value includes the PCB capacitance. The recommendation is to refer to *Clock Routing Guidelines, Oscillator Routing* section of the processor-specific data sheet for placement and routing of the crystal and load capacitors.

A 1.8V LVCMOS clock source can be used as processor clock source. When clock output from the external oscillator is connected to the XI input (through a series resistor), the recommendation is to ground XO as per the recommendations in the processor-specific data sheet. The inverter shown in the (figure *1.8V LVCMOS-Compatible Clock Input* in the processor-specific data sheet) was meant to represent an LVCMOS output, where the LVCMOS output can be the oscillator output buffer, or the LVCMOS output from some clock distribution device. There is no requirement to invert the clock source.

Refer to processor-specific data sheet. for WKUP_OSC0 LVCMOS Digital Clock Source Requirements. For more information on LVCMOS clock source including clock source requirements, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1/ AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding LVCMOS Digital Clock Source for, MCU_OSC0 (WKUP_OSC) or WKUP_LFOSC0 (LFOSC0)

Internal AC coupling capacitors have been implemented on both XI and XO signal paths that connect to an internal comparator that creates a square wave. A DC steady-state condition on the XI pin relative to the XO pin allows the comparator to generate glitches on the internal clock tree of the device and cause the clock circuit to do unpredictable operations. Connecting a DC input to XI is not recommended or allowed.

For information on clock selection and clock specifications, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding Crystal selection and clock specifications

For information on crystal Start-up Time, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L Custom board hardware design – Queries regarding crystal (MCU_OSC0 (WKUP_OSC0)) Start-up Time

Note

MCU_OSC0 (High frequency oscillator) for AM62x is WKUP_OSC0 for AM62Lx.

Note

25MHz is the only crystal frequency currently supported. See the processor-specific data sheet for information on the supported crystal frequency and recommended crystal parameters.

The processor-specific data sheet includes specification for selecting the 25MHz crystal and *WKUP_OSC0 LVCMOS Digital Clock Source Requirements*.

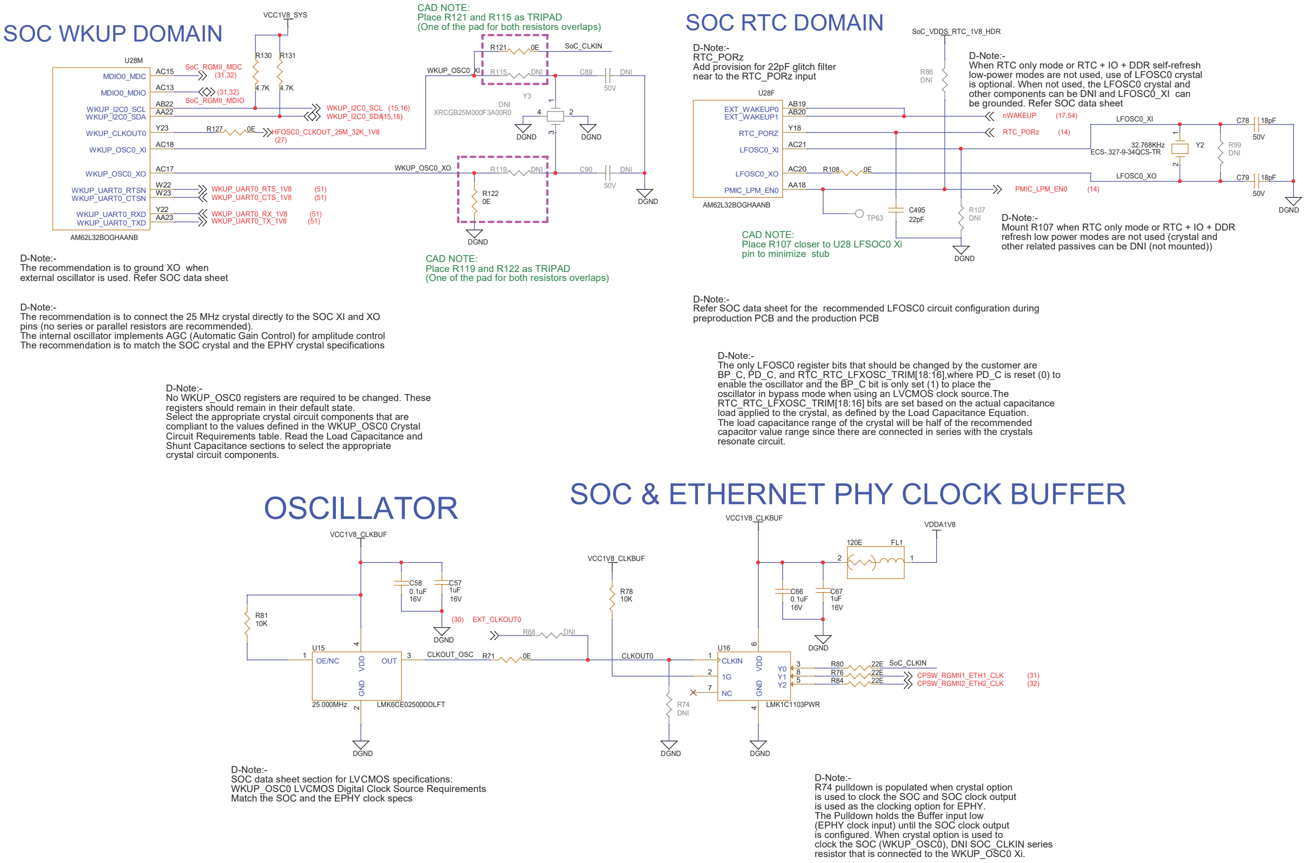
When an external clock (LVCMOS) oscillator is used as the clock source for the processor and the EPHYs, a single oscillator can be used or separate (individual) oscillators can be used. When a single oscillator is used, the clock output is recommended to be buffered before connecting to processor and EPHYs.

Single output buffer (individual ICs) for processor and EPHYs or dual or multiple output buffer (single IC) with a single input for processor and EPHYs, can be used to connect the clock output from the oscillator to the processor and the EPHYs.

For specific use case (requirement for some of the industrial applications using Time Sensitive Networking (TSN)), two or more output (based on number of EPHYs used) buffer with a single input is recommended for the processor and the EPHYs.

6.1.3.1.2 LFOSC0 (Low Frequency) Clock (Internal Oscillator) or LVCMOS Digital Clock (External Oscillator)

Figure 6-6 includes crystal + load cap + series resistor + parallel resistor for LFOSC0 (32.768KHz) clock source. Provision to ground Xi using 0R is provided to configure the LFOSC0 when not used as per processor-specific data sheet.



CAD NOTE:
Place R121 and R115 as TRIPAD
(One of the pad for both resistors overlaps)

D-Note:-
The recommendation is to ground XO when external oscillator is used. Refer SOC data sheet

CAD NOTE:
Place R119 and R122 as TRIPAD
(One of the pad for both resistors overlaps)

D-Note:-
The recommendation is to connect the 25 MHz crystal directly to the SOC XI and XO pins (no series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control
The recommendation is to match the SOC crystal and the EPHY crystal specifications

D-Note:-
No WKUP_OSC0 registers are required to be changed. These registers should remain in their default state.
Select the appropriate crystal circuit components that are compliant to the values defined in the WKUP_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

D-Note:-
RTC_PORz
Add provision for 22pF glitch filter near to the RTC_PORz input

D-Note:-
When RTC only mode or RTC + IO + DDR self-refresh low-power modes are not used, use of LFOSC0 crystal is optional. When not used, the LFOSC0 crystal and other components can be DNI and LFOSC0_XI can be grounded. Refer SOC data sheet

CAD NOTE:
Place R107 closer to U28 LFSOC0 Xi pin to minimize stub

D-Note:-
Mount R107 when RTC only mode or RTC + IO + DDR refresh low power modes are not used (crystal and other related passives can be DNI (not mounted))

D-Note:-
Refer SOC data sheet for the recommended LFOSC0 circuit configuration during preproduction PCB and the production PCB

D-Note:-
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and RTC_RTC_LFXOSC_TRIM[18:16],where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source.The RTC_RTC_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation.
The load capacitance range of the crystal will be half of the recommended capacitor value range since there are connected in series with the crystals resonate circuit.

D-Note:-
SOC data sheet section for LVCMOS specifications:
WKUP_OSC0 LVCMOS Digital Clock Source Requirements
Match the SOC and the EPHY clock specs

D-Note:-
R74 pulldown is populated when crystal option is used to clock the SOC and SOC clock output is used as the clocking option for EPHY.
The Pulldown holds the Buffer input low (EPHY clock input) until the SOC clock output is configured. When crystal option is used to clock the SOC (WKUP_OSC0), DNI SOC_CLKIN series resistor that is connected to the WKUP_OSC0 Xi.

Figure 6-6. LFOSC0 Clock Connections

A low frequency (32.768kHz) LFOSC0 is supported by the processor family. Based on the use case, a 32.768kHz external crystal + internal oscillator can be used as the clock source or an external 1.8V LVCMOS square-wave digital clock source can be used.

LFOSC0 has specific use cases (RTC only mode or RTC + IO + DDR low-power mode) and can be optional based on the custom design implementation. When LFOSC0 is not used, the recommendation is to connect the LFOSC0_XI to VSS and leave the LFOSC0_XO unconnected. For more information on connecting the unused LFOSC0, see the LFOSC0 Not Used section of the processor-specific data sheet.

For more information, see the following FAQs:

[FAQ] AM62L (AM62L32, AM62L31): Custom Board Hardware design - LFOSC usage in the processor

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1/ AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding LVCMOS Digital Clock Source for, MCU_OSC0 (WKUP_OSC) or WKUP_LFOSC0 (LFOSC0)

The recommendation is to place the discrete components used to implement the external crystal based oscillator close to the LFOSC0_XI and LFOSC0_XO pins. For the crystal, the load capacitance selected is recommended to be in the range specified in the *LFOSC0 Crystal Electrical Characteristics* table of the processor-specific data sheet. There is no requirement to add the PCB capacitance to the load capacitance.

The figure *LFOSC0 Crystal Implementation* in the processor-specific data sheet shows the recommended crystal circuit. TI recommends that preproduction printed-circuit board (PCB) designs include the two optional resistors Rbias and Rd in case these are required for proper oscillator operation when combined with production crystal circuit components. In a number of use cases, DNI or delete Rbias and Rd is a 0Ω resistor. The resistors option can be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCB.

Note

WKUP_LFOSC0 (low frequency (32.768kHz) oscillator) for AM62x is LFOSC0 for AM62Lx.

6.1.3.1.3 EXT_REFCLK1 (External Clock Input to MAIN Domain)

EXT_REFCLK1 input is routed to clock multiplexers as a selectable clock source to the Timer modules (DMTIMER/WDT), DMTIMER in Security Subsystem (SMS), MCAN, and CPTS (Time Stamping Module). The EXT_REFCLK1 is an option when an end equipment/ application requires a specific clock frequency to be fed to the timer modules. An example application is time synchronization. When EXT_REFCLK1 is used as a clock source, depending on the availability of external clock, a pulldown (10kΩ) is recommended near to the processor clock input pin.

6.1.3.1.4 Clock Input Checklist - WKUP_OSC0

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Configuration of processor clock input source, crystal + internal oscillator or external oscillator (use any one option on the board for optimizing the placement and routing)
3. Selection of crystal frequency (25MHz) and crystal load as per process-specific data sheet
4. Selection of WKUP_OSC0 external crystal load capacitor including PCB capacitance of ~4pF
5. Processor clock pins connection recommendations when crystal + internal oscillator or external oscillator is used
6. Connection of XO when external oscillator output is connected to XI
7. Connection of bulk and decoupling capacitors for external oscillator supply pin and connection of oscillator EN pin

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of 25MHz WKUP_OSC0 clock is mandatory.
2. Selection of External crystal or External clock oscillator as per the data sheet requirements.
3. Verify the crystal, crystal frequency and crystal load capacitor selected follows processor-specific data sheet recommendations.
4. 25MHz is the clock input frequency currently supported. Refer processor-specific data sheet for supported clock input frequencies.
5. Direct connection of crystal (without series or parallel resistor) and connection of the crystal load capacitance circuit (WKUP_OSC0) as per processor-specific data sheet.
6. External crystal load capacitor is recommended to be x2 of the crystal load, including PCB capacitance (~4pF).
7. The recommendation is to select crystal load value such that a standard value capacitor can be selected for the load capacitor.
8. The recommendation is to retain the HFOSC0 registers in the default state.
9. When external oscillator is used, the recommendation is to add decoupling capacitor and a bulk capacitor near to the oscillator supply pin and series resistor on the clock output pin.
10. The recommendation is to connect XO to VSS when external oscillator (LVCMOS clock) output is connected to XI.
11. Addition of series resistor (22Ω) on the clock output pin close to the oscillator.

Additional

1. Refer to the *Applications, Implementation, and Layout* section of the processor-specific data sheet for clock routing guidelines.
2. The recommendation is to connect the 25MHz (performance has been validated only with 25MHz frequency) crystal directly to the processor XI and XO pins, no series or parallel resistors are recommended. The internal oscillator implements Automatic Gain Control (AGC) for amplitude control.

3. Processor-specific data sheet shows that WKUP_OSC0 does not start until the core voltage ramps because there are some cases where the oscillator does not start until VDD_CORE ramps. In most of the use cases, the oscillator starts when VDDS_OSC0 supply ramps (although the oscillator starting when VDDS_OSC0 ramps is not always the case). The oscillator start-up diagram in the processor-specific data sheet shows the maximum start-up time, which includes the case where the delay is based on VDD_CORE being valid.
4. A DC steady-state condition is not allowed on WKUP_OSC0_XI because WKUP_OSC0_XI is internally AC coupled to a comparator that can enter an unknown state.
5. The LVCMOS clock sourcing the WKUP_OSC0_XI input is required to have monotonic transitions and shall be connected to WKUP_OSC0_XI with a point-to-point connection, via a series resistor placed near the clock source. The series termination resistor value shall match the clock source output impedance to the transmission line impedance. For example, a 20Ω is used when clock source has 30Ω output impedance and the PCB signal trace has 50Ω characteristic impedance. The series resistor allows the reflection that returns from the far end of the unterminated transmission line to be completely absorbed such that it does not introduce any non-monotonic events.
6. The recommendation is to minimize the PCB trace length connecting the external clock source to WKUP_OSC0_XI. Smaller trace length minimizes probability of external noise sources coupling to the clock signal. Reduced capacitive loading improves rise/fall times of the clock signal which reduces the probability of jitter being introduced (to the clock source or the custom board).
7. The recommendation is to verify the crystal selection with the crystal supplies or manufacturer.

6.1.3.1.5 Clock Input Checklist - LFOSC0

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Selection of LFOSC0 clock source - external crystal + internal oscillator or external oscillator. (use any one option on the board for optimizing the placement and routing)
3. Selection of LFOSC0 external crystal frequency
4. Selection of crystal load capacitors and value
5. Connection of series and parallel resistors for crystal-based oscillator circuit implementation
6. Connection of series and parallel resistors to the crystal base oscillator circuit.
7. Selection of external oscillator and connection of capacitor and series resistor
8. Connection of XO when external oscillator output is connected to XI
9. Connection of XI pin when the LFOSC0 is not used (XI is grounded, XO Unconnected)
10. Connection of bulk and decoupling capacitors for external oscillator supply pin and connection of oscillator EN pin

Schematic Review

Follow the below for the custom schematic design:

1. LFOSC0 clock input frequency supported is 32.768kHz.
2. Connections of the clock circuit (LFOSC0), as per the processor-specific data sheet recommendations.
3. Selection of crystal load and load capacitance value (follow the processor-specific data sheet), with the load capacitance being x2 of the crystal load (PCB capacitance is not included).
4. When external oscillator is used, the recommendation is to add decoupling capacitor and a bulk capacitor near to the oscillator supply pin and series resistor on the clock output pin.
5. Connection of XO when external oscillator is used (XO is connected to ground).
6. Connection of the XI input when the LFOSC0 is not used (XI is connected to ground, XO is left unconnected).
7. Connection of series and parallel resistors for initial prototype (preproduction) and production boards (can be removed) as per processor-specific data sheet requirements.

Additional

1. Crystal load capacitance versus LFOSC0 registers. The only LFOSC0 register bits custom board designers change are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the *Load Capacitance Equation*.
2. Refer to the processor-specific data sheet for the recommended circuit configuration (passives) during preproduction PCB and the production PCB.
3. LFOSC0 has limited use cases, the recommendation is to provide provision to ground the XI input when the clock option is not used.

6.1.3.2 Clock Outputs

Processor IOs (pins) named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for the attached devices (External peripherals - Example: EPHY).

WKUP_CLKOUT0 is driven low after reset for the AM62L family of processors.

The recommendation is to connect the clock as point-to-point connection. When CLKOUT0 and WKUP_CLKOUT0 are used to source more than x1 attached devices, buffering the CLKOUT0 and WKUP_CLKOUT0 is recommended.

The CLKOUT0 and WKUP_CLKOUT0 clock outputs performance is not defined in the processor-specific data sheet since there are a number of boards or end equipment specific dependencies that can impact the clock performance. The recommendation is to check the performance on the actual board (clock output meets board or end equipment specific requirements).

6.1.3.2.1 Clock Output Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Configuration of CLKOUT0 and WKUP_CLKOUT0 clock outputs
3. Connection of clock output to single or multiple loads (attached devices)
4. Provision for series resistor near to the clock output pin and pulldown near to the attached device

Schematic Review

Follow the list below for the custom schematic design:

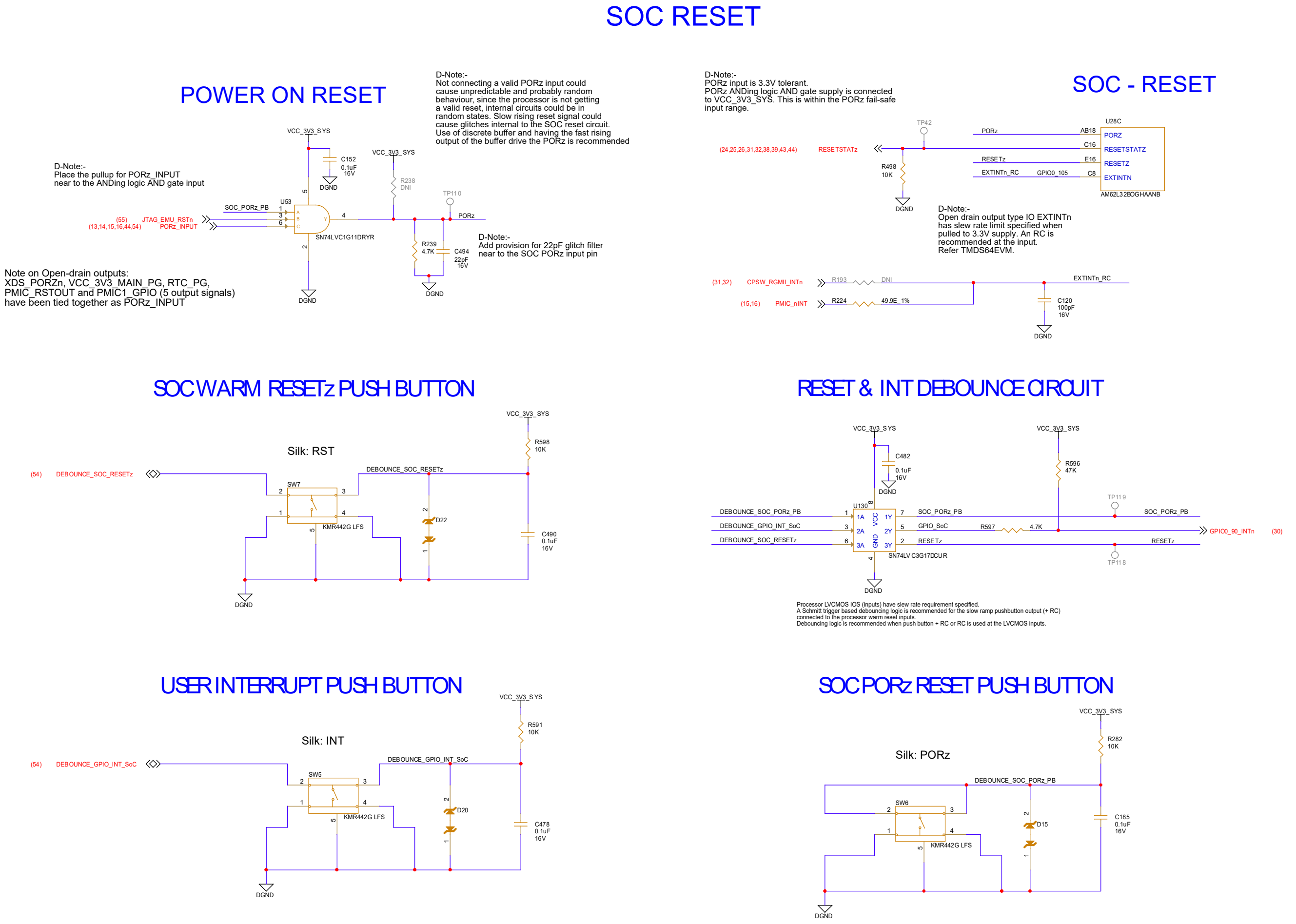
1. WKUP_CLKOUT0 can be configured as buffered output of XO. Add a TP for testing.
2. Series resistor 0Ω provision is provided for control of possible signal reflection.
3. Connection of clock output to single or multiple loads. When connected to multiple loads (inputs), each of attached device inputs are recommended to be connected to a buffered output.
4. Pulls are provided near to the attached device clock input that can float (to prevent the attached device inputs from floating until host software configures the clock output).

Additional

1. EXT_REFCLK1 can be configured as CLKOUT0. The recommendation is to connect clock signal as point-to-point, without any branches. When connecting CLKOUT0 to multiple clock inputs, the recommendation is to use a buffer (with one input and multiple outputs or individual buffers (based on the application use case)).
2. The CLKOUT0 and WKUP_CLKOUT0 clock outputs performance is not defined in the processor-specific data sheet since there are a number of boards or end equipment specific dependencies that can impact the clock performance.

6.1.4 Processor Reset

Figure 6-7 includes PORz (cold reset input) generated using a push-pull output type ANDing logic (U53) with a pulldown and a glitch filter added near to the PORz_Input pin. Provision to reset the processor manually through push button (Warm or Cold reset) connected to the processor through debouncing logic (U130) has been added.



D-Note:-
Not connecting a valid PORz input could cause unpredictable and probably random behaviour, since the processor is not getting a valid reset, internal circuits could be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use of discrete buffer and having the fast rising output of the buffer drive the PORz is recommended

D-Note:-
Place the pullup for PORz_INPUT near to the ANDing logic AND gate input

D-Note:-
Add provision for 22pF glitch filter near to the SOC PORz input pin

Note on Open-drain outputs:
XDS_PORZn, VCC_3V3_MAIN_PG, RTC_PG, PMIC_RSTOUT and PMIC1_GPIO (5 output signals) have been tied together as PORz_INPUT

D-Note:-
PORz input is 3.3V tolerant.
PORz ANDing logic AND gate supply is connected to VCC_3V3_SYS. This is within the PORz fail-safe input range.

D-Note:-
Open drain output type IO EXTINTn has slew rate limit specified when pulled to 3.3V supply. An RC is recommended at the input.
Refer TMDS64EVM.

Processor LVCMOS IOS (inputs) have slew rate requirement specified.
A Schmitt trigger based debouncing logic is recommended for the slow ramp pushbutton output (+ RC) connected to the processor warm reset inputs.
Debouncing logic is recommended when push button + RC or RC is used at the LVCMOS inputs.

Figure 6-7. SOC_Cold_Warm_RESET_Debounce_Logic

See the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design - Processor Reset inputs, Reset Status Output and Connection recommendations

6.1.4.1 External Reset Inputs

PORz is the external WKUP domain cold reset input to the processor. The recommendation is to hold the PORz pulled low during the supply ramp and oscillator start-up. Follow the recommended PORz timing in the *Power-Up Sequencing* diagram of the processor-specific data sheet.

For the PORz (3.3V tolerant, fail-safe input), applying a 3.3V input is an acceptable. The input thresholds are a function of the 1.8V IO supply voltage (VDDS_OSC0).

When PMIC based power architecture is used, the recommendation is to connect the open-drain output type reset signal (nRSTOUT0) from PMIC to the processor through push-pull output type logic gate or discrete buffer (with fast rise time) as PORz input (rather than connecting a slow rising open-drain output that can glitch the internal reset circuit). In case nRSTOUT0 is directly used (connected), the recommendation is to adjust the pullup to minimize the slew (<100ns).

The recommendation is to always connect a valid input to PORz. Not connecting a valid input to PORz input is not an allowed use case. In case PORz input is not connected, the processor may not complete the reset sequence during power-up and can cause unpredictable or random behavior. When the processor internal circuit does not go through a valid reset, internal circuits can be in random (undefined) states.

The recommendation is to provide provision to connect a 22pF filter (glitch) filter at the PORz input.

The capacitor value and mounting of the capacitor is use-case dependent. The recommendation is to choose the capacitor value such that the capacitor used does not cause the LVCMOS input to violate the slew rate requirements or cause reset to glitch internally.

Warm reset input (RESETz, LVCMOS IO) has input slew rate requirements specified. Connecting a capacitor (slow ramp) directly at the input is not recommended. A Schmitt trigger-based debouncing logic (circuit) is recommended. For implementing the debouncing logic, follow the processor-specific EVM schematic. When push-button is connected to control RESETz warm reset input, the recommendation is to add provision for external ESD protection.

See the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31): Custom Board Hardware design - PORz and RTC_PORz slew rate

6.1.4.2 Reset Status Output

RESETSTATz is the MAIN domain warm reset status output. When reset status output RESETSTATz is used to drive the attached device reset inputs (/reset), a pulldown (10kΩ) is recommended for reset status output to assert the reset (hold the attached devices in reset) to the attached devices during power-up and reset.

Note

An external pulldown connected at the output of reset status output holds the attached devices reset input low, in use cases where none of the attached devices has internal pullup. In case where any of the attached device has an internal pullup enabled, the reset signal is pulled to a mid-supply. The recommendation is to verify specific use-case before connecting the reset status output.

MAIN domain warm reset status output RESETSTATz can be used to reset on-board memories or peripherals that support external reset input functionality (eMMC, OSPI, or EPHY) or SD card power switch EN. The RESETSTATz can be used to latch the hardware strap configurations during reset (Example: latching the Ethernet PHY strap configurations or the boot mode configurations).

In case the reset status output is not used, the recommendation is to connect the reset status output to a test point for testing or future enhancements. Optionally a pulldown (10kΩ) can be provided and can be populated when used.

6.1.4.3 Additional Information

The BOOTMODE[15:00] (depending on the *Boot Mode Pin Mapping Option*) inputs that are used to configure the processor boot mode is recommended to be held in a known state to select the appropriate boot mode configuration as defined in the processor-specific TRM, until the boot mode configuration is latched during the rising edge of the RESETSTATz.

6.1.4.4 Processor Reset Input Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of reset inputs (cold and warm reset)
3. PORz input connection and L->H delay after all the processor supplies ramp (ramp-up and ramp-down)
4. PORz H->L delay after processor supplies ramp down (low before supplies ramp down)
5. PORz input IO level and fail-safe capability

6. Reset (Cold, Warm) input follows the slew rate requirements (Fail-Safe Reset (FS RESET) Electrical Characteristics) as per the processor-specific data sheet
7. Addition of pulldown and glitch filter at the input of PORz
8. PORz input state during processor supplies ramp
9. PORz input slew rate when open-drain output type reset signal (nRSTOUT0) from PMIC or discrete DC/DC or discrete LDO is connected as PORz input
10. Connection of external input to warm reset input RESETz (IO level)
11. RESETz slew rate when push button input is connected
12. Addition of glitch filter at the input of RESETz
13. Connection of warm reset input when not used

Schematic Review

Follow the below list for the custom schematic design:

1. A valid input that goes high after all the supplies ramp plus the required delay for clock start-up
2. PORz input is held low during power supply ramp-up or ramp-down.
3. PORz input deassertion hold time (9.5ms (9500000ns) minimum) after all processor supplies ramps is provided as per the processor-specific data sheet requirement.
4. Cold and warm reset input slew rate requirements have been considered and required push-pull output type discrete buffers are added. Slow slew can glitch the reset internally.
5. Slew rate when open-drain output type reset signal (nRSTOUT0) from PMIC or discrete DC/DC or discrete LDO is connected directly to the reset input. Lesser slew is better (<100ns). The recommendation is to connect reset input through fast rise time discrete push-pull output type buffer.
6. PORz input is 3.3V tolerant and fail-safe. The threshold follows the 1.8V IO level (VDDS_OSC0)
7. Provision for a pulldown 10K and a glitch filter (capacitor) is provided at the PORz reset input (add 22pF (place holder) capacitor provision)
8. IO level of warm reset input RESETz follows the VDDSHV1 supply (Fixed 1.8V or 3.3V)
9. Connection of push button for warm reset input through debouncing logic (Schmitt trigger buffer output).
10. The recommendation is to connect the warm reset input when not used as per pin connectivity requirements (a pullup is recommended)

Additional

1. PORz input has internal hysteresis enabled and slew rate requirement specified. When connecting PMIC_POWERGOOD (open-drain output type signal) to PORz input is the only available option, adjust the pullup to optimize the rise time (< 100ns).
2. The processor is required to restart (release reset) only after all the supply voltages ramp down below 300mV during power-down (There is no time or tolerance associated with the ramp down requirement. Each power rail is recommended to decay below 300mV before any power rail is allowed to ramp up).
3. Not connecting a valid PORz input can cause unpredictable and random behavior, since processor does not get a valid reset input and the internal circuits are in random states. Slow ramp reset input causes internal processor reset circuit to glitch.
4. LVCMOS RESETz input has slew rate requirements specified. A schmitt trigger based debouncing logic (circuit) is recommended for the slow ramp push button output signal connected to the processor warm reset input RESETz. Schmitt trigger based debouncing logic (circuit) is recommended when using an RC as reset input.
5. Provision for external ESD protection for manual (push button) reset input is recommended to be added near to the reset signal.
6. Fail-safe operation when connected to external reset input for warm reset. Applying an external input before the processor supply ramps can cause voltage feed and affects the board performance.
7. The recommendation is to follow the reset requirements including slew rate and PORz input hold time after supplies ramp when a non-TI power architecture is considered.

6.1.4.5 Processor Reset Status Output Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection and addition of pulldown for RESETSTATz status output.
3. IO level compatibility between the processor reset status output and attached device reset input.
4. Capacitor (load) connection at the output of reset status output.
5. Reset status output connection when not used.
6. External ESD protection for the reset status output when connected to carrier board or external connector.

Schematic Review

Follow the below list for the custom schematic design:

1. RESETSTATz is used as input to latch the processor boot mode configuration or attached device strap configuration during processor cold reset.
2. RESETSTATz is used to reset the attached devices when the processor undergoes any type of global reset (cold or warm).
3. RESETSTATz has pulldown provision to hold the attached devices in reset during supply ramp near to the processor pin.
4. Connection of capacitor directly on the reset output or near to the reset input of the attached device (capacitor > 22pF). Perform simulation as required.
5. IO level compatibility between the processor reset status output and attached device reset input (can cause residual voltage affecting custom board performance).
6. Provision for TP provided when reset status output is not used.
7. Processor reset output IO level and the attached device input IO levels are recommended to be matched to avoid voltage leakage.

6.1.5 Configuration of Boot Modes (for Processor)

Figure 6-8 includes bootmode configuration switches for Reduced pincount (15-12) bootmode configuration and Full pincount bootmode(15-0) configuration.

Refer to the EVM schematic for implementation of bootmode using external buffers. A 4-bit buffer has been used for Reduced pincount bootmode configuration.

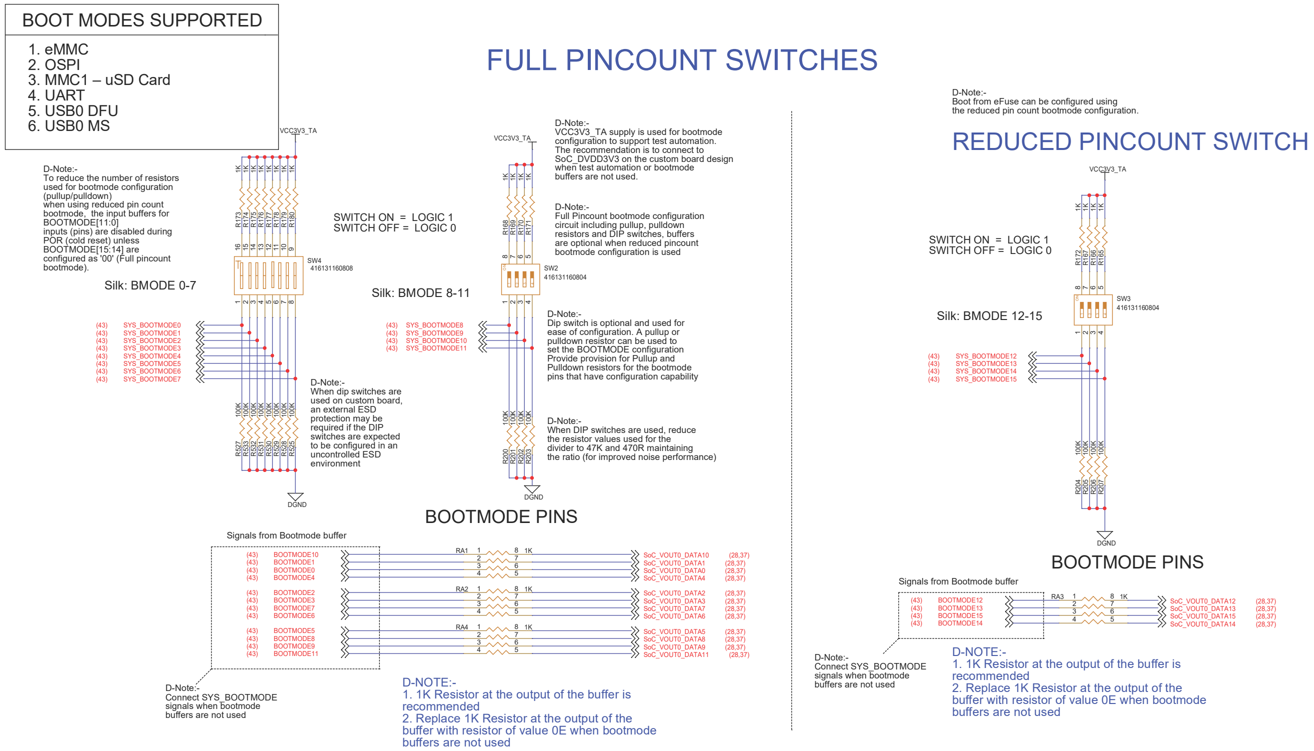


Figure 6-8. Boot Mode Configuration Switch

The processor family supports two BOOTMODE input connection (pin mapping) options, as described below:

1. Reduced pincount - using only four of the bootstrap pins BOOTMODE[15:12]
2. Full pincount - using all 16 of the bootstrap pins BOOTMODE[15:0]

For supported boot mode configurations, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62Ax / AM62Px / AM62D-Q1 / AM62L - Supported bootmode configurations

The reduced pincount boot mode mapping offers the advantage of requiring less bootstrap pins which can translate to fewer pullup or pulldown components required. The reduced pincount boot mode comes at the cost of making fewer boot mode options pin selectable.

However, two of the boot mode configuration options that are selectable from the *BOOTMODE Pin Mapping (Reduced)* table can be used (customized boot) to configure any of the full 16-bit bootmode configuration options by programming required boot mode configuration value into the eFuse. The eFuse values are also protected using SECDED error correcting encoding scheme; 22 eFuse bits are used to encode the 16-bit boot mode value.

To reduce the number of pullup or pulldown resistors required to configure the processor boot mode, the input buffers for BOOTMODE[11:0] inputs (pins) are disabled during POR unless BOOTMODE[15:14] are configured as '00'. Disabling the buffers minimizes power consumption due to floating of the boot mode input pins in case reduced pincount boot mode option is used.

Internal pulls (pullup or pulldown) are not enabled for the processor boot mode inputs (depends on reduced or full pincount boot configuration, BOOTMODE[15:12] for reduced pincount, BOOTMODE[15:00] for full pincount) during cold reset. The recommendation is to connect external pulls (10kΩ or 47kΩ) (pullup or pulldown) to configure the required boot mode (depends on reduced or full pincount boot configuration). The recommendation is to not leave any of the boot mode inputs unconnected (depends on reduced or full pincount boot configuration) including reserved pins.

In use case where dip switches are used to configure the required boot modes, the recommendation is to use resistor divider value of 1kΩ or 2kΩ (pullup, based on 1.8V or 3.3V supply) and 47kΩ (pulldown) for improved noise performance.

When the boot mode is configured using only resistors (without using dip switches), a standard resistor (same value can be used for pullup and pulldown) value can be used. As an example a 10kΩ or 47kΩ can be used since either pullup or pulldown is recommended to be populated. The recommendation is to provide provision to connect pullup or pulldown to all boot mode pins including pins that are reserved or not used.

The recommendation is to connect pullup or pulldown to boot mode pins marked as *Reserved* or not used.

The recommendation is to add provision for pullup and pulldown for the boot mode inputs (pins) that have configuration capability for testing/debug (including provision for USB0 DFU, UART0 boot mode configuration), design flexibility, and future enhancement. The recommendation is to populate either pullup or pulldown for each boot mode pins. Connecting boot mode pins directly to ground or IO supply rail is not recommended or allowed since IOs have alternate function that can be configured after boot and can be unintentionally configured as output by the software.

Boot mode inputs (pins) are not fail-safe. The recommendation is to not apply any external inputs before the processor IO supply ramps. When connecting boot mode using pullups/pulldowns without the use of boot mode buffer the recommendation is to connect the IO supply that is connected to the IO supply for IO group referenced by the processor IOs. When using boot mode buffers the recommendation is to connect the IO supply that connects the processor IOs to the B-port supply pin of buffers (processor side). When external inputs from carrier board are connected to configure the boot mode inputs, the inputs are recommended to be driven after the processor supply ramps and are required to be stable before the PORz input is pulled high.

Based on the application requirement, a buffer that is driven only when reset (PORz) is asserted (low) is used to present the boot configuration to the processor.

A series resistor (1kΩ) is recommended at the output of the buffer (to limit the output current in case the boot mode pins are configured as an output before the buffer OE is deasserted). For more information, see the processor-specific EVM for implementation.

6.1.5.1 Processor Boot Mode Inputs Isolation Buffers Use Case and Optimization

In the EVM, the boot mode inputs BOOTMODE[15:12], BOOTMODE[11:00] are asserted through x1 8-bit and x2 4-bit isolation buffers. The buffers make sure that the SYSBOOT pulls (pullup and/or pulldown) (boot mode configuration resistors) control the IO level of the signals when the boot mode inputs are latched (during RESETSTATz rising edge). The boot mode configuration resistors are isolated from other connected peripherals (since boot mode input pins have alternate functions) so that the other connected peripherals do not conflict with the intended boot mode configuration (IO levels).

The buffers are enabled when RESETSTATz is low. Once RESETSTATz is deasserted (goes high), the buffer outputs are in Hi-Z state.

For optimizing the custom board design (including BOM), the boot mode buffers can be optimized or deleted (use case dependent, custom board designer to verify). The recommendation is to select the pull resistors value, so that the resistors do not affect the operation of the attach devices.

6.1.5.2 Boot Mode Configuration

For configuring the required processor boot mode, refer to the *ROM Code Boot Modes* table in the *Initialization* chapter of the processor-specific TRM.

6.1.5.2.1 Notes for USB Boot Mode

USB0 interface supports DFU (Device Firmware Upgrade) boot. When the USB0 is configured for DFU boot, permanent 3.3V supply (direct or using divider) is not recommended to be connected to the USB0_VBUS input. Connecting a permanent supply equivalent to the USB0_VBUS divider input is not allowed. Connecting supply without the *USB VBUS Detect Voltage Divider / Clamp Circuit* violates fail-safe operation.

A 5V supply from the host (switched) connected through the USB interface connector is recommended to be connected to USB0_VBUS input through resistor divider, as per the processor-specific data sheet recommendations. Zener diode can be removed and the two resistors (16.5kΩ and 3.48kΩ) can be combined into a single 20kΩ resistor for the *USB VBUS Detect Voltage Divider / Clamp Circuit* if the custom board design does not apply a VBUS potential > 5.5V, and on-board supply is connected.

6.1.5.3 Notes on SD Card Boot SDCD Input Connection

Note the connection recommendation for SDCD pin on the processor side to support SD card boot in the *Boot Modes*, SD card boot section of the processor-specific TRM.

6.1.5.4 Notes on OSPI Boot OSPI Interface Chip Select Connection

Note the connection recommendation for OSPI chip select pin selection and connection on the processor side to support *Boot with OSPI Controller* section of the processor-specific TRM.

6.1.5.5 Boot Mode Implementation Approaches

For implementing the boot mode, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation with isolation buffers used

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation without isolation buffers

6.1.5.6 Additional Information

When external inputs are connected to configure the boot mode inputs, the boot mode configuration inputs are recommended to be stable before the processor PORz (cold reset) is released (L->H).

When using Ethernet boot and Reduced Gigabit Media Independent Interface (RGMII) interface, the recommendation is to use an EPHY that supports RGMII_ID on the EPHY RDx data path and disables RGMII_ID on the TDx data path (processor implements fixed RGMII_ID on the TDx clock signal with respect to the data signals). Processor ROM does not enable or disable RGMII_ID mode for the attached EPHY. RGMII_ID is set using pin strapping for the EPHY.

The recommendation is to select an EPHY, with capability to set the RGMII_ID through pin strap. Refer the processor-specific EVM for implementation using TI EPHY.

6.1.5.7 Configuration of Boot Modes (for Processor) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Bootmode configuration approach (Reduced or full pin count)
3. Does provision for bootmode configuration include eFuse usage
4. Connection approach of processor boot mode inputs (using buffers or connected directly)
5. Boot mode configuration (using dip switches and resistor divider or only resistors)
6. Boot mode input state during latching of the bootmode configuration
7. Connection of SDCD pin to support SD card boot as per SD card bootmode section of the processor-specific TRM
8. Connection of the recommended chip select pin to attached OSPI/QSPI memory device to support boot as per Boot with OSPI Controller section of the processor-specific TRM
9. Boot mode inputs connection recommendation when used for alternate functions
10. Fail-safe capability of boot mode inputs

Schematic Review

Follow the below list for the custom schematic design:

1. Boot mode configuration inputs are connected to the processor using resistor, switch + resistor divider, and buffers as per the EVM implementation.

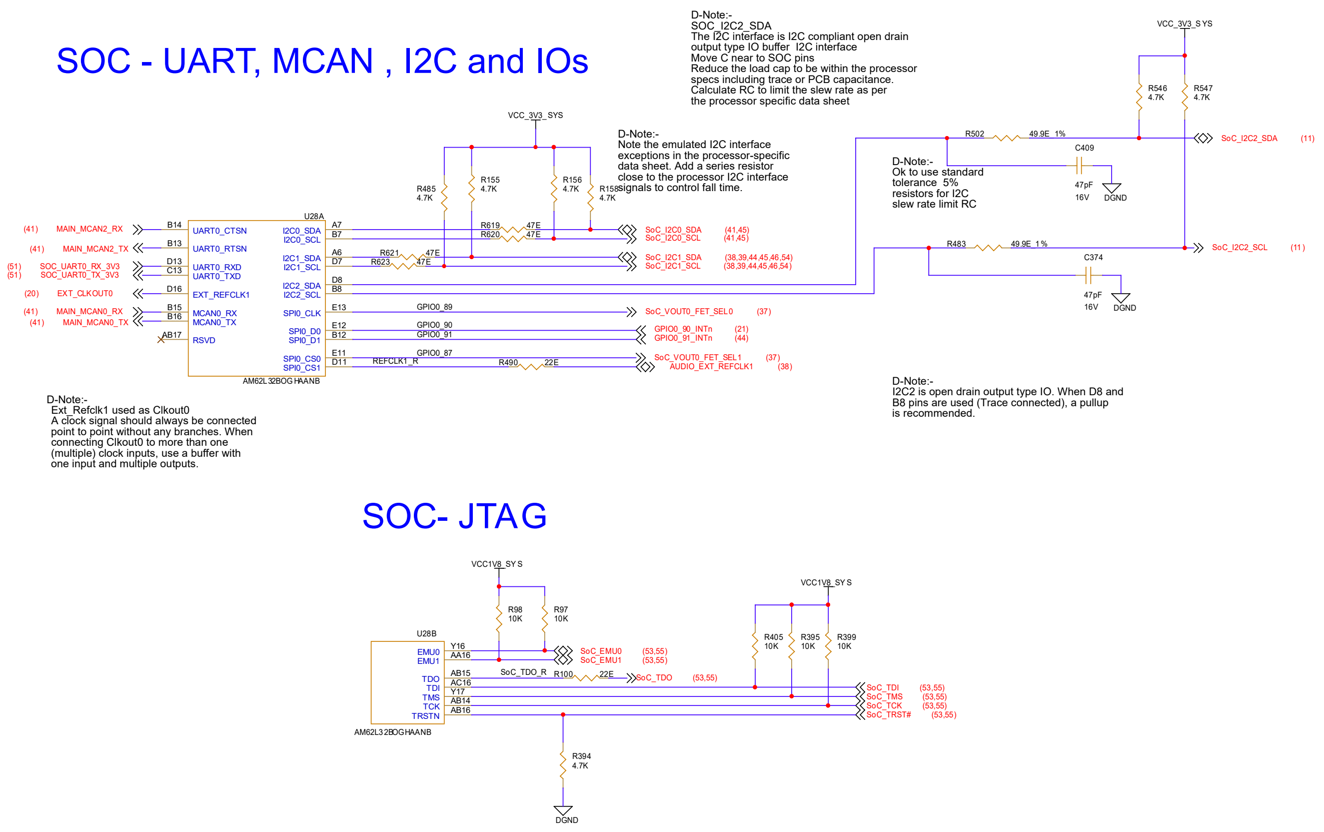
2. Series resistor 1kΩ is used at the output of the buffer when boot mode is implemented with buffers or driven by external control signals.
3. The recommendation is to verify the boot mode input configuration setting follows the processor-specific TRM recommendations for PLL clock input, primary boot and secondary boot.
4. Boot mode inputs IO compatibility (1.8V or 3.3V referenced to (powered by) VDDSHV0)
5. The recommendation is to use 1kΩ and 47kΩ value resistors when dip switches are used to configure the boot.
6. When dip switches are not used a standard 10kΩ resistor can be used for pullup and pulldown to configure the boot mode. The recommendation is to populate either pullup or pulldown to configure the required boot mode. Resistor divider is optional when dip switches are not used
7. All boot mode configuration input pins have external pulls or a circuit to drive the required boot mode input during processor cold reset (Leaving any of the boot mode inputs unconnected is not recommended or allowed)
8. External boot mode inputs applied are recommended to be stable before the processor cold reset input (PORz) is released (0->1)
9. The recommendation is to connect boot mode input signals to alternate functions through 0Ω for isolation or testing of the boot mode functionality
10. Boot mode inputs are not fail-safe (no external boot mode input is recommended to be applied before the processor supplies ramp)

Additional

1. Processor BOOTMODE input pins do not have internal pullup or pulldown enabled during reset (when the boot mode input configuration is being latched).
2. For initial (early or first prototype) designs, the recommendation is to connect external PU/PD resistors for the boot mode inputs (pins). See processor-specific TRM for information on the boot modes supported.
3. Boot mode inputs are latched when RESETSTATz goes high. If the boot mode inputs are reconfigured for alternate function during operation, boot mode inputs are required to be released/set back to the required configuration to select the boot mode whenever the processor is reset (cold reset). Boot mode configuration is a concern if signal is driven from external peripheral.
4. Connecting the boot mode inputs directly to IO supply or VSS is not recommended. Shorting of multiple boot mode inputs together and connecting to a common resistor is not recommended. (Custom board designs can have firmware configuration issues, where the LVCMOS IOs that are intended to be inputs are unexpectedly configured as outputs, driving a logic high signal instead of remaining in high-impedance state).
5. The recommendation is to add external ESD protection for boot mode inputs, in case the boot mode switches are configured in an uncontrolled environment.
6. Boot mode inputs are not fail-safe. Applying external inputs before the processor IO supplies ramp is not recommended or allowed. Applying external input signal to the processor boot mode inputs before processor supply ramps can cause voltage feed and can affect the custom board functionality.
7. Boot mode input buffers are optional and are provided on the EVM to support test automation.
8. When using buffers or logic gates to configure the boot mode inputs, the recommendation is to verify the device used supports OE (output enable capability).

6.2 Custom Board Debug Using JTAG and EMU

Figure 6-9 includes the JTAG interface connections and the recommended pull (pullup or pulldown) placed near to the processor JTAG interface pins as per the processor pin connectivity requirements section of the processor-specific data sheet.



SOC - UART, MCAN , I2C and IOs

D-Note:-
SOC_I2C2_SDA
The I2C interface is I2C compliant open drain
output type IO buffer I2C interface
Move C near to SOC pins
Reduce the load cap to be within the processor
specs including trace or PCB capacitance.
Calculate RC to limit the slew rate as per
the processor specific data sheet

D-Note:-
Note the emulated I2C interface
exceptions in the processor-specific
data sheet. Add a series resistor
close to the processor I2C interface
signals to control fall time.

D-Note:-
Ok to use standard
tolerance 5%
resistors for I2C
slew rate limit RC

D-Note:-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected
point to point without any branches. When
connecting Clkout0 to more than one
(multiple) clock inputs, use a buffer with
one input and multiple outputs.

D-Note:-
I2C2 is open drain output type IO. When D8 and
B8 pins are used (Trace connected), a pullup
is recommended.

SOC- JTAG

Figure 6-9. JTAG Pulls Connection

6.2.1 JTAG Interface and EMU Signals When Used

When JTAG interface is implemented, the recommendation is to use the TI recommended, defined and supported 20-pin connector (rather then the 10-pin ARM connector). The 10-pin JTAG connector does not include the TRSTn signal or the EMU0, EMU1 signals. The recommendation is to connect the JTAG (TDI, TCK, TMS and TRSTn) and EMU (EMU0 and EMU1) signals as per the *Pin Connectivity Requirements* section of the processor-specific data sheet. The recommendation is to place the pullups (10kΩ) and pulldown (4.7kΩ) near to the processor JTAG interface pins. Providing provision for low pass filter, implemented with a 100Ω series resistor and 0.1µF shunt capacitor on the processor side of the 100Ω resistor is recommended.

The recommendation is to add external ESD protection for all JTAG interface and EMU0 and EMU1 signals close to the external interface connector. EMU0 and EMU1 signals support boot sequence and debug after cold reset (PORz input high). Pullup for TDO is optional and depends on the selected debugger. Optionally, the recommendation is to connect a series resistor (0Ω) on the TDO (close to processor) signal for matching JTAG tool buffer impedance.

For additional information, refer to the *On-Chip Debug* chapter of the processor-specific TRM.

For more information, see the below FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Custom board hardware design – JTAG

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – JTAG Pulldown/Pullup

The FAQ is generic and can also be used for AM62Lx processor family.

6.2.2 JTAG Interface and EMU Signals Connection When Not Used

For connecting the JTAG interface signals and EMU signals when JTAG interface is not used, refer to the *Pin Connectivity Requirements* section of the processor-specific data sheet.

During custom board design, the recommendation is to provision for a minimal JTAG interface signals including EMU0, EMU1 connected to test points or a header footprint to support debugging early prototype. JTAG interface related components can be a DNI in the production version of the board. The recommendation is to provide provision to populate recommended pulls as per the *Pin Connectivity Requirements* section, and provide provision for external ESD protection near to the JTAG connector or TPs.

6.2.3 Additional Information

Buffering of clock and JTAG interface signals are recommended whenever the JTAG interface connects to more than one attached device. Buffering of clock is recommended even for single device implementations. For implementation, see the processor-specific EVM.

When trace interface is used, the recommendation is to connect TRC_DATAn signals to the emulation connector. All TRC_DATAn signals are pin-MUXed with other signals. The recommendation is to use either trace functionality or a GPMC interface. Short and skew matched connections (board trace) for TRC_DATAn signals are used for trace functionality. The trace signals are referenced to (powered by) VDDSHV0, and can be at a different supply voltage from the other JTAG signals. For additional recommendations on TRC/EMU design and layout, see the *Emulation and Trace Headers Technical Reference Manual*. A summary is available in the *XDS Target Connection Guide*.

When boundary scan is used, the recommendation is to connect EMU0 and EMU1 pins to the JTAG connector.

For implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual*.

6.2.4 Custom Board Debug Using JTAG and EMU Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of JTAG interface signals including EMU0, EMU1 signals to external interface connector or TPs
3. Connection of recommended pulls for JTAG interface signals as per processor pin connectivity requirements
4. Provision for low pass filter, implemented with a 100 ohm series resistor and 0.1uF filter (shunt) capacitor on the processor side of the 100 ohm resistor
5. JTAG interface signals IO level compatibility
6. Fail-safe operation of the JTAG interface signals
7. Provision for external ESD protection

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of JTAG interface signals and EMU0, EMU1 signals to the JTAG interface connector
2. Connection of supply voltage to the JTAG connector including filter capacitor (the recommendation is to connect the voltage source that connects to VDDS0)
3. Connection of the recommended pullup and pulldown as per the pin connectivity requirements near to the processor JTAG interface pins
4. Pullup (10kΩ) and pulldown (4.7kΩ) values used (recommend following the EVM implementation)
5. JTAG interface signals IO compatibility (IO supply referenced to (powered by) VDDS0)
6. Fail-safe operation of the JTAG interface signals. No JTAG input signals are available (applied) when the processor power supplies are off

Additional

1. The recommendation is to include (implement) at least a minimal JTAG signals on the custom board designs, connected to test points or header for debugging early prototypes. The minimum recommended

JTAG signals are TCK, TMS, TDI, TDO, TRSTn and EMU0, EMU1. If required, the recommendation is to delete JTAG routes and component footprints (except the pulldown on TRSTn and the pullups on TMS and TCK) in the production version of the board.

2. When trace is implemented, the TRC_DATAn signals are recommended to be connected to the emulation connector. All TRC_DATAn signals are pin-muxed with other signals. If the trace connections are implemented, the recommendation is to not use other muxed functions. The recommendation is to use short and slew matched traces (routes) for TRC_DATAn signals. Trace signals are referenced to (powered by) a different power domain and can be operating at a different voltage compared to JTAG signals.
3. The recommendation is to add provision for external ESD protection. The external ESD protection can be populated when JTAG interface is used.
4. The recommendation is to verify fail-safe operation when using JTAG interface. Applying an external input signal to the processor JTAG inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.

7 Processor Peripherals Power, Interface and Connections

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

Note

There is no firm rule or requirement for external pull unless the pull requirements are defined in an industry standard. Industry standard definition for pulls is the main reason we can make firm recommendations for external pulls on the eMMC and SD card signals. For the other peripherals, the recommendation is for customers to evaluate the function of the attached devices connected to every processor signal on the custom board and apply the appropriate technical/engineering judgment to determine the need to have external pulls that prevent any input from floating when attached device inputs buffer is turned on. The recommendations provided in the design guide are generic and customer is expected to review the design requirements and the availability of pulls internal to the attached device before implementing. Be sure to not provide an external pull in contention with an internal pull. Example: An example is adding an external pull that is in contention with the internal pull (internal to the attached device), such that the contention creates a mid-supply potential on the signal (input).

7.1 Supported Processor Cores

The recommendation is to refer to *Features* section of the processor-specific data sheet for the supported Processor Cores. The *Device Comparison* section of the processor-specific data sheet can be referenced for the selection of the Arm Cortex-A53 Microprocessor Subsystem cores.

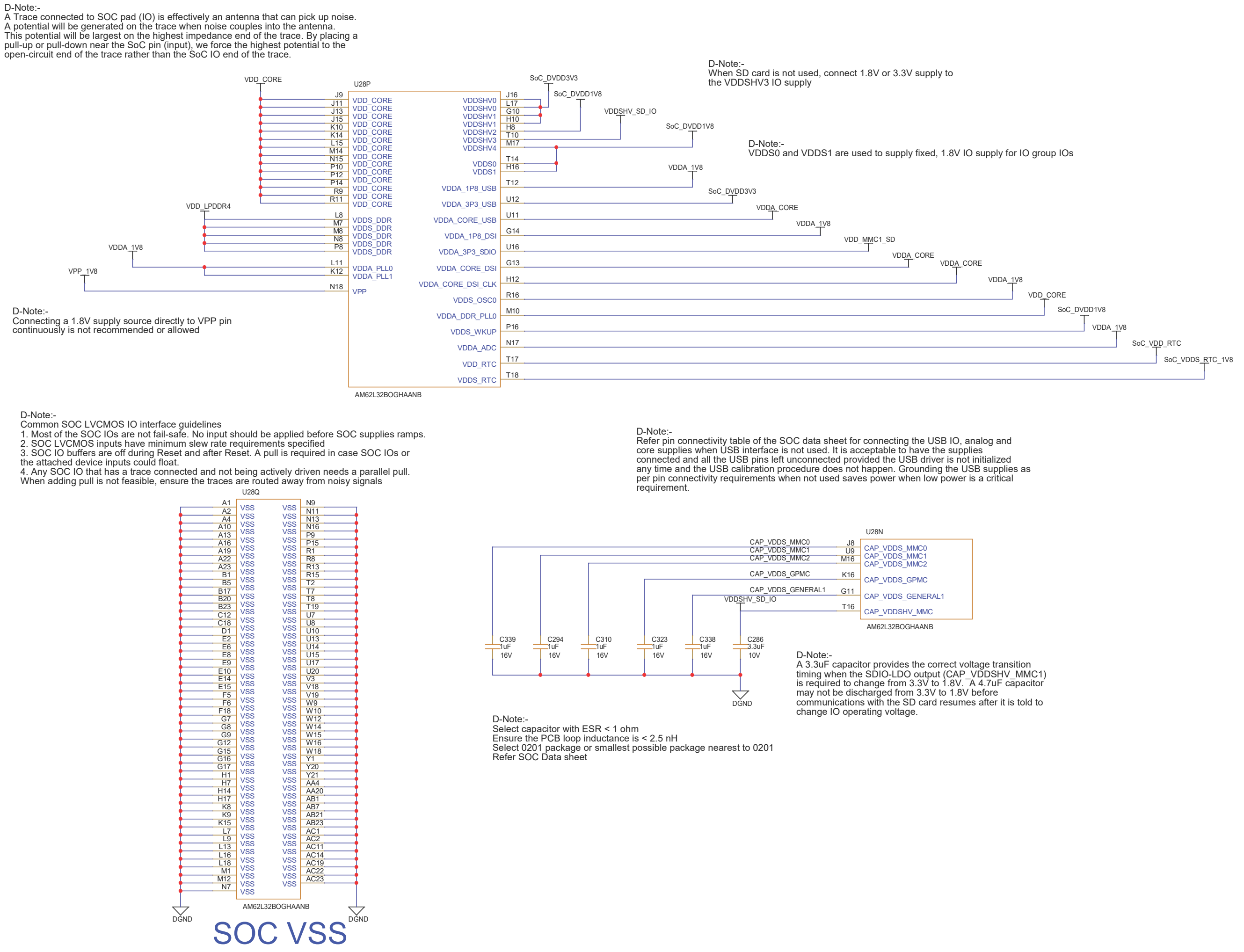
The *Operating Performance Points OPP* section of the processor-specific data sheet can be reference for definition of the required device grade and device operating performance points.

Refer below FAQ for additional details:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on processor core, PLL, VDD_CORE, VDDR_CORE, VPP and other core supplies

7.2 Supply Connections for IO Supply for IO Groups

Figure 7-1 includes connection of supply for processor fixed-voltage IO supply for IO group VDDS0, VDDS1 and Dual-voltage IO supply for IO group VDDSHV0, VDDSHV1, dynamically switched Dual-voltage IO supply for IO group VDDSHV2, VDDSHV3, VDDSHV4, and Fixed-voltage supply for LFOSC0 and RTC IO group.



D-Note:-
A Trace connected to SOC pad (IO) is effectively an antenna that can pick up noise.
A potential will be generated on the trace when noise couples into the antenna.
This potential will be largest on the highest impedance end of the trace. By placing a pull-up or pull-down near the SoC pin (input), we force the highest potential to the open-circuit end of the trace rather than the SoC IO end of the trace.

D-Note:-
When SD card is not used, connect 1.8V or 3.3V supply to the VDDSHV3 IO supply

D-Note:-
VDDS0 and VDDS1 are used to supply fixed, 1.8V IO supply for IO group IOs

D-Note:-
Connecting a 1.8V supply source directly to VPP pin continuously is not recommended or allowed

D-Note:-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before SOC supplies ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset and after Reset. A pull is required in case SOC IOs or the attached device inputs could float.
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note:-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note:-
A 3.3uF capacitor provides the correct voltage transition timing when the SDIO-LDO output (CAP_VDDSHV_MMC1) is required to change from 3.3V to 1.8V. A 4.7uF capacitor may not be discharged from 3.3V to 1.8V before communications with the SD card resumes after it is told to change IO operating voltage.

D-Note:-
Select capacitor with ESR < 1 ohm
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package nearest to 0201
Refer SOC Data sheet

Figure 7-1. IO Supply for IO Group Connection

The processor family supports fixed 1.8V IOs and 1.8V/3.3V fixed or dynamically switched IOs. The recommendation is to verify the IO level compatibility with the attached device. The recommendation is to power the processor IO supply for IO group and the attached device IO supply from the same power source. The custom board designer is expected to make sure the design never applies a potential that is greater than the values defined in the *Absolute Maximum Ratings* table of processor-specific data sheet.

7.2.1 VDDSHVx Dual-voltage IO Supplies and Fixed-voltage Supplies for IO Groups

Each of the dual-voltage IO supply for IO group (VDDSHVx [x = 0:4]) provides supply to a fixed set of IOs (peripherals). The recommendation is to connect either 3.3V/1.8V supply voltage to each of the dual-voltage IO supply for IO group (VDDSHV0, VDDSHV1) or dynamically switched 3.3V/1.8V supply voltage to each of the dual-voltage IO supply for IO group (VDDSHV2, VDDSHV3, VDDSHV4).

VDDSHV2, VDDSHV3, and VDDSHV4 IO supply for IO groups referenced to MMC0, MMC1 and MMC2 signal groups have been designed to support power-up, power-down, or dynamic supply voltage change (switching) without dependency on other processor supply rails. The dynamic voltage switching capability allows UHS-I SD card support.

The IO supply requirements depends on the IO buffer type (LVCMOS, SDIO) and the peripherals being connected.

Based on the selected memory type (DDR4 or LPDDR4), the recommendation is to connect DDR PHY IO supply as per the ROC.

7.2.2 VDDSx Fixed 1.8V Supply

Each of the fixed-voltage IO supply for IO group (VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC) provides power supply to a fixed set of IOs (peripherals). A fixed 1.8V supply voltage is connected to fixed-voltage IO supply for IO groups (VDDS0, VDDS1, VDDS_WKUP, VDDS_RTC).

Fixed-voltage IO supply for IO group are implemented using 1P8-LVCMOS IO buffer.

The recommendation is to design the power architecture to make sure the supply voltage outside of the ROC is not applied momentarily or continuously.

7.2.3 Supply Connections for IO Supply for IO Groups Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Standards referenced in the electrical characteristics including recommended operating conditions and any additional available information
3. IO buffer type implemented and the supported supply configuration (1P8-LVCMOS, LVCMOS fixed 1.8V or 3.3V) or SDIO dynamic voltage (1.8V or 3.3V) switching)
4. Connection of valid supply to all the dual-voltage IO supply for IO groups (VDDSHVx) and fixed-voltage IO supply for IO groups (VDDSx or VDDS_WKUP)
5. Sequencing of the processor IO supplies
6. Connection of processor DDRSS PHY IO supply based on the selected memory
7. IOs pullup supply voltage connection (same as the IO supply for IO group supply)

Schematic Review

Follow the below list for the custom schematic design:

1. IO groups supported included LVCMOS, 1P8-LVCMOS, SDIO and I2C OD type IO buffers
2. IO supply source used follows the ROC as per processor-specific data sheet.
3. IO supply sequencing follows the processor-specific data sheet.
4. IO buffer type LVCMOS supports fixed (1.8V or 3.3V) or SDIO type dynamic voltage switching (1.8V or 3.3V).
5. Attached device IO supply and the IO supply for IO group (dual-voltage or fixed-voltage) referenced by the processor interface signals are connected to the same supply source.
6. External pullups are connected to the same supply rail or source that is connected to the processor VDDSHVx or VDDSx or VDDS_WKUP or VDDS_RTC supply pins and attached device IO supply.
7. Connecting the 3.3V supply that is connected to the PMIC input, directly to the processor dual-voltage IO supply for IO groups VDDSHVx is not recommended since the IO supply will be available for an undefined time in case the PMIC does not start-up and generate other processor supply rails.

Additional

1. Note the power sequencing requirements based on the IO supply for IO groups voltage level used
2. Dynamic voltage switching are supported by specific dual-voltage IO supply for IO groups (VDDSHV2, VDDSHV3, and VDDSHV4)
3. Dynamic voltage switching of the dual-voltage IO supply for IO group referenced to (connected) LVCMOS IO buffers (IOs) are not supported or allowed.

7.3 Memory Interface (DDRSS (DDR4/LPDDR4), MMCSD (eMMC/SD/SDIO), OSPI/QSPI and GPMC)

7.3.1 DDR Subsystem (DDRSS)

The processor family supports x1 instance of DDR sub system DDRSS0 and supports interfacing to 16-bit SDRAM.

The DDRSS interface supports DDR4 or LPDDR4 memory interface. Choice of DDR4 or LPDDR4 memory is application or customer dependent as there are differences in latency and burst lengths in each of the memory type.

For additional information, refer below application note:

Sitara AM62Lx Benchmarks

Refer *DDR Electrical Characteristics* section of the processor-specific data sheet for information related to DDRSS compatibility with JEDEC standards. Refer note below from the processor-specific data sheet:

Note

The DDRSS interface is compatible with DDR4 devices that are JESD79-4B standard-compliant, and LPDDR4 devices that are JESD209-4B standard-compliant.

For the supported memory size for DDR4 and LPDDR4, refer to the processor-specific data sheet. There can be change in the supported memory size, DDRSS interface pin outs compared to the other processor family and the recommendation is to review the supported memory size and recommended connections when designing custom board schematics.

Refer to *AM62L Power Supply Implementation* application note on processor product page for description of AM62L power architecture implementation when LPDDR4 or DDR4 is used.

See the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV) Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDRSS : DDR4 / LPDDR4 MEMORY Interface

[FAQ] AM625: DDR4/ LPDDR4 performance difference

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.3.1.1 DDR4 SDRAM (Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

7.3.1.1.1 AM62Lx Processor Family

For implementation guidelines and routing topologies, see the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

For implementation reference follow below:

TMDS64EVM: AM64x evaluation module for Sitara processors

SK-AM62B-P1: AM62x Starter Kit EVM with PMIC

7.3.1.1.1.1 Memory Interface Configuration

The allowed memory configurations are x1 (single), 16-bit or x2 (two), 8-bit.

x1 (single), 8-bit memory configuration is not an allowed or valid configuration.

The recommendation is to verify the connection of DDRSS signals Bank Groups (DDR0_BG0, DDR0_BG1) based on the selected memory size, and Chip Select (DDR0_CS0_n) based on memory selection (Single-Rank). Refer *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

7.3.1.1.1.2 Routing Topology and Connection of Memory Terminations

When x1 (single) memory (DDR4) device (x1 (single), 16-bit) is used, the recommendation is to follow point-to-point topology (connections).

Summary of point-to-point topology implementation:

- For differential clock DDR0_CK0, DDR0_CK0_n, AC termination x2 R in series (value = Zo − Single-ended impedance) and a filter capacitor 0.01µF or value recommended by the memory manufacturer connected to the center of two resistors and DDR PHY IO supply VDDS_DDR is recommended.
- VREFCA (VDDS_DDR/2) is the reference voltage used for control, command, and address inputs to the memory (DDR4) devices. When VTT terminations and VTT termination LDO is not used, VREFCA is derived from VDDS_DDR using a resistor divider (two resistors (1kΩ, ±1%, recommended value) connected across VDDS_DDR and VSS) with a filter capacitor (0.1µF, recommended value) connected in parallel to the resistors. An additional decoupling capacitor is recommended near to the VREFCA pin (close to memory (DDR4) device).
- External VTT terminations for address and control signals are optional.

When VTT terminations are used for the address and control signals for use case where x1 DDR4 memory device is used, the recommendation is to use a Sink or Source DDR Termination Regulator (LDO) to generate the required VTT supply.

When x2 (two) memory (DDR4) devices (x2 (two), 8-bit) are used, the recommendation is to follow Fly-by topology (connections).

Summary of Fly-by topology implementation:

- External VTT terminations for address, control, and clock signals are recommended.
- Sink or Source DDR Termination Regulator (LDO) is recommended to generate the VTT supply.
- The Sink or Source DDR Termination Regulator (LDO) is used to generate the reference voltage VREFCA (VDDS_DDR/2).
- The recommendation is to add decoupling capacitors for the reference voltage.

7.3.1.1.1.3 Resistors for DDRSS Control and Calibration

A pulldown (10kΩ) is recommended for DDR0_RESET0_n (DDR_RESET#) close to memory (DDR4) device. Adding a filter capacitor (47pF or similar) across the pulldown resistor is optional.

The recommendation is to connect the recommended (follow processor-specific data sheet or EVM schematics) resistors for DDR0_CAL0 (IO Pad Calibration Resistor, close to processor cal pin) and ZQn (Memory Device Calibration reference resistor, n = 0-1, close to memory (DDR4) device).

The recommendation is to connect pulldown for TEN (test enabled). The recommendation is to add an optional pulldown provision DDR0_CKE0 signal (DDR_CKE net) and mark as DNI (no populate).

7.3.1.1.1.4 Capacitors for the Power Supply Rails

The recommendation is to verify adequate bulk and decoupling capacitors have been provided for the processor DDRSS supply rails and memory (DDR4) device supply rails.

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

7.3.1.1.1.5 Data Bit or Byte Swapping

During custom board design, in case bit swapping is required, bit swaps within a data byte, and swapping across bytes is allowed with some restrictions. Address and control bit swapping is not supported. Do not swap the DM and DQS bits with any other signals.

For more information, see the *Bit Swapping* section of *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

The recommendation is to update the schematics with the bit swapping changes including notes for future reference or reuse.

7.3.1.1.1.6 Unsupported DDRSS Interface Pins

The DDRSS does not support DDR0_ALERT_n, DDR0_PAR, DDR0_CKE1, DDR0_CS1_n, DDR0_ODT1 signals (pins). Refer to the memory data sheet or application notes for connecting the pins or verify with the memory supplier.

7.3.1.1.1.7 DDR4 Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Selection of Memory (JESD79-4B standard-compliant), supported memory configuration and number of memory devices connected
3. Connection of address, clock, control and data signals
4. Connection and routing topology followed based on number of memory devices (x1 or x2) connected
5. Maximum supported memory size and connection of DDRSS signals based on the selected memory size
6. Differential clock termination implementation, connection and value of the VTT resistors and filter capacitors used
7. DDR reference voltage generation resistor divider
8. VTT Termination for address and control signals when x2 memory devices are used
9. Connection of DDRSS RESETn signal to DDR_RESETn memory reset input
10. Connection of ODT signal from DDRSS to memory device (external pull is optional)
11. Connection of processor DDR0_CAL0 and attached memory device TEN, ZQn and Alert_n (including value and tolerance) pins.
12. Swapping of Data Bit or Data Byte
13. Addition of required bulk and high frequency capacitors, and value.
14. Connection of pins (Example: DDR0_PAR) on the memory side that is not supported by the processor DDRSS.

Schematic Review

Follow the below list for the custom schematic design:

1. x1 16-bit memory device and x2 8-bit memory devices are the supported memory configuration.
2. The recommendation is to compare the bulk and decoupling capacitors used and values with EVM schematic implementation.
3. Supply rails connected to the processor DDRSS peripheral supply rail and the attached memory device IO follow the processor and attached memory device ROC.
4. Connection of address, clock, control and data signals, as per the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.
5. Routing topology followed based on number of memory devices connected ((data bus topology is always point-to-point), (for address and control, x1 16-bit, point-to- point and x2 8-bit Fly-by (daisy chain)).
6. Connection of signals based on the selected memory size (CS0, BG0, BG1, refer *AM62x, AM62Lx DDR Board Design and Layout Guidelines*).
7. Differential clock termination using x2 resistors and filter capacitor. Value of the VTT resistors and filter capacitors used. (Refer EVM schematics).
8. DDR reference voltage resistor divider value and tolerance. Resistor divider connection (1kΩ, ±1%) for DDR reference DDR_VREFCA generation. The recommendation is to place a decoupling capacitor 0.1μF across the resistors and near to the memory pin.
9. Connection of VTT Terminations for address and control signals when x2 memory devices are used (optional for x1 memory device) including VTT resistors and capacitors (x1 capacitor for every x2 VTT resistors) quantity and value (The recommendation is to follow TMDS64EVM). VTT termination supply LDO implementation.
10. Connection of DDRSS RESETn signal to DDR_RESETn memory reset input (to hold the signal low during power-on initialization). The recommendation is to add a pulldown (10kΩ) for DDRSS RESETn signal and placed near the memory device reset input pin.
11. Connection of TEN (1kΩ pulldown) signal.
12. ZQ0, ZQ1, Memory device IO calibration resistor (240Ω, ±1%) connection across ZQ and VSS.
13. DDR0_CAL0, DDRSS IO pad calibration resistor (240Ω, ±1%) connected across DDR0_CAL0 and VSS.
14. Connection of ODT signal from DDRSS to memory device (external pull is optional).

15. Follow *AM62x, AM62Lx DDR Board Design and Layout Guidelines* when data bits and data groups are swapped.

Additional

1. The recommendation is to refer TMDS64EVM for implementing VTT terminations for DDR4 address and control signals and VTT supply (LDO).
2. The recommendation is to add layout notes on the schematic (the recommendation is to follow the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*).
3. The recommendation is to follow the *Pin Connectivity Requirements* section of the processor-specific data sheet for connecting unused DDRSS interface signals.
4. Connection of required DDRSS signals to the memory device for expansion.
5. The DDRSS does not support DDR0_ALERT_n, DDR0_PAR, DDR0_CKE1, DDR0_CS1_n, DDR0_ODT1 signals (pins). Refer to the memory data sheet or application notes for connecting the pins or verify the connection recommendations with the memory supplier.

7.3.1.1.1.8 DDR4 VTT Termination Implementation Schematic Reference

When x2 (two) memory (DDR4) devices (x2 8-bit) are used, each device is connected to each data byte of the DDRSS. The address signals or control signals are connected in Fly-by topology with VTT terminations connected near to the memory device placed far from the processor DDRSS.

For implementing VTT terminations, follow *TMDS64EVM (AM64x evaluation module for Sitara processors)*.

The recommendation is to perform board-level simulations as part of the design.

7.3.1.2 LPDDR4 SDRAM (Low-Power Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

Figure 7-2 includes processor DDRSS configured for LPDDR4 memory interface and interfaced to LPDDR4 memory U29 including the LPDDR4_RESET_N (LPDDR4 memory reset input) and decoupling capacitors.

Refer to SK-AM62B-P1 and TMDS64EVM in case the processor DDRSS is required to be interfaced to DDR4 memory.

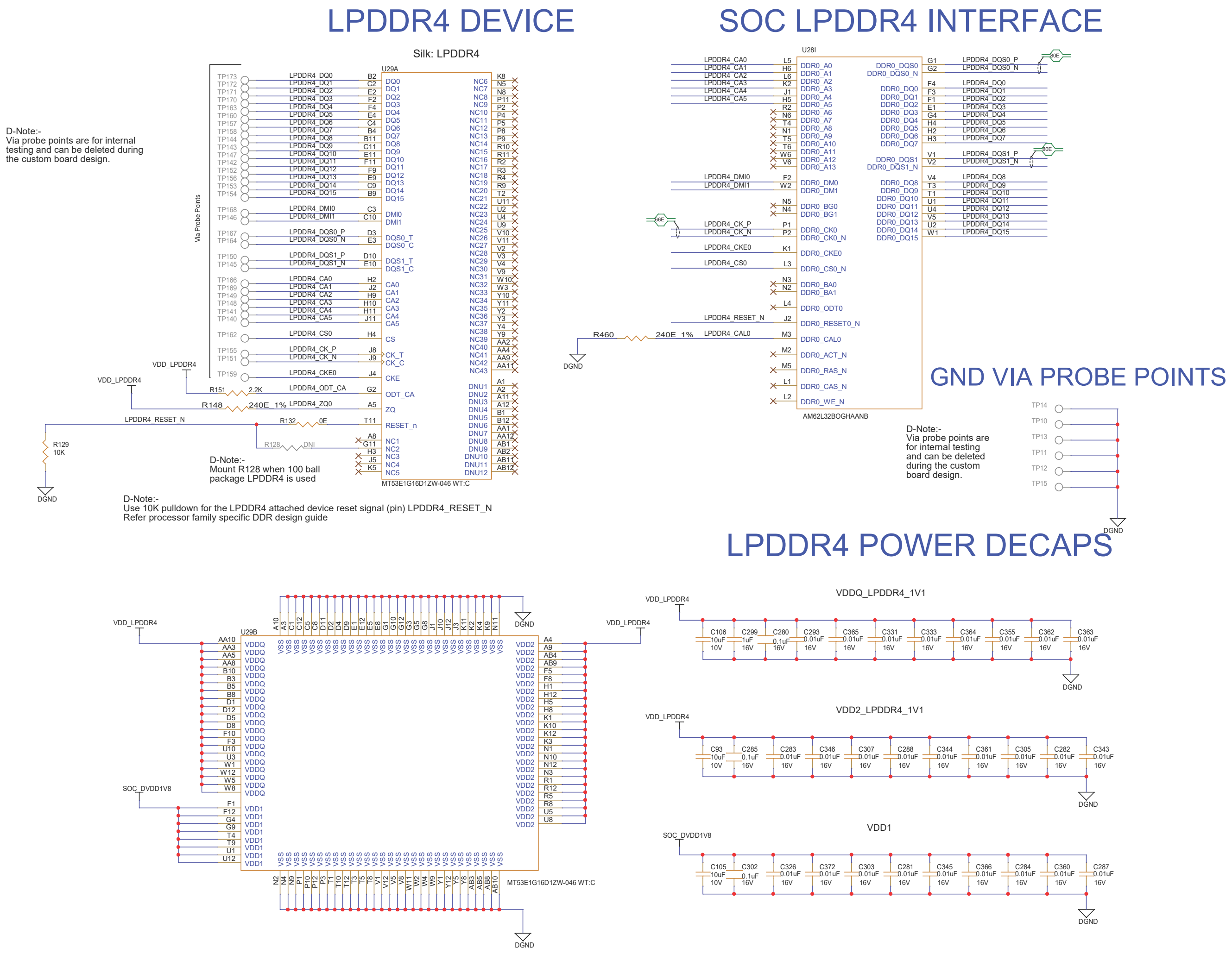


Figure 7-2. DDRSS LPDDR4 Interface

7.3.1.2.1 AM62Lx Processor Family

For implementation guidelines and routing topology, see the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

The controller supports DDR4 or LPDDR4 interface . The LPDDR4 address interface is 6-bit wide and is connected to the first 6-bits of the processor DDR_A port. When using LPDDR4, the extra address signals (used for DDR4) are not used and can be left unconnected. Refer to the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* when designing the DDR portion of custom board.

7.3.1.2.1.1 Memory Interface Configuration

The allowed memory configuration is x1 (single), 16-bit.

7.3.1.2.1.2 Routing Topology and Connection of Memory Terminations

The recommendation is to follow point-to-point topology for clock (CK), address, control (ADDR_CTRL) and data signals.

VTT termination does not apply for LPDDR4 memory type. Memory terminations that are required for address and control signals are supported (handled) internally (on-die).

7.3.1.2.1.3 Resistors for DDRSS Control and Calibration

A pulldown (10kΩ) is recommended for DDR0_RESET0_n (LPDDR4_RESET_N) close to memory (LPDDR4) device. Adding a filter capacitor (47pF or similar) across the pulldown resistor is optional.

The recommendation is to connect the recommended (follow processor-specific data sheet or EVM schematics) resistors for DDR0_CAL0 (IO Pad Calibration Resistor, close to processor cal pin), ODT_CA_A (2.2kΩ used on EVM, DDRSS On-Die Termination for Chip Select, close to memory (LPDDR4) device) and ZQ (Memory Device Calibration reference resistor, close to memory (LPDDR4) device).

7.3.1.2.1.4 Capacitors for the Power Supply Rails

The recommendation is to verify adequate bulk and decoupling capacitors have been provided for the processor DDRSS supply rails and memory (LPDDR4) device supply rails.

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

7.3.1.2.1.5 Data Bit or Byte Swapping

During custom board design, in case bit swapping is required, bit swaps within a data byte, and swapping across bytes is allowed. Address and control bit swapping is not supported.

For more information, see the *Byte and Bit Swapping* section of *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

The recommendation is to update the schematics with the bit swapping changes including notes for future reference or reuse.

7.3.1.2.1.6 LPDDR4 Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Selection of Memory (JESD209-4B standard-compliant), supported memory configuration, memory size and number of memory devices connected (x1 allowed)
3. Supply rails connected to the processor DDRSS peripheral supply rail and the attached memory device IO
4. Connection of address, clock, control and data signals
5. Connection of DDRSS RESETn signal to LPDDR4_RESET_N memory reset input
6. Connection of chip select CSn0 to the attached memory device
7. ODT configuration pullup connection, DDRSS CAL0 and Memory device ZQn resistor connections including value and tolerance
8. Swapping of Data Bit or Data Byte
9. Addition of required bulk and high frequency capacitors, and value
10. The recommendation is to add layout notes on the schematic (the recommendation is to follow the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*)

Schematic Review

Follow the below list for the custom schematic design:

1. x1 16-bit is the only supported memory configuration.
2. The recommendation is to compare the bulk and decoupling capacitors used and values with relevant EVM schematic implementation.
3. Supply rails connected to the processor DDRSS peripheral supply and the attached memory device IO follow the processor and attached memory device ROC.
4. Connection of address, clock, control and data signals. For LPDDR4 memory interface, x16 is the only supported data bus width. For connecting the DDRSS to 16-bit memory device - refer *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

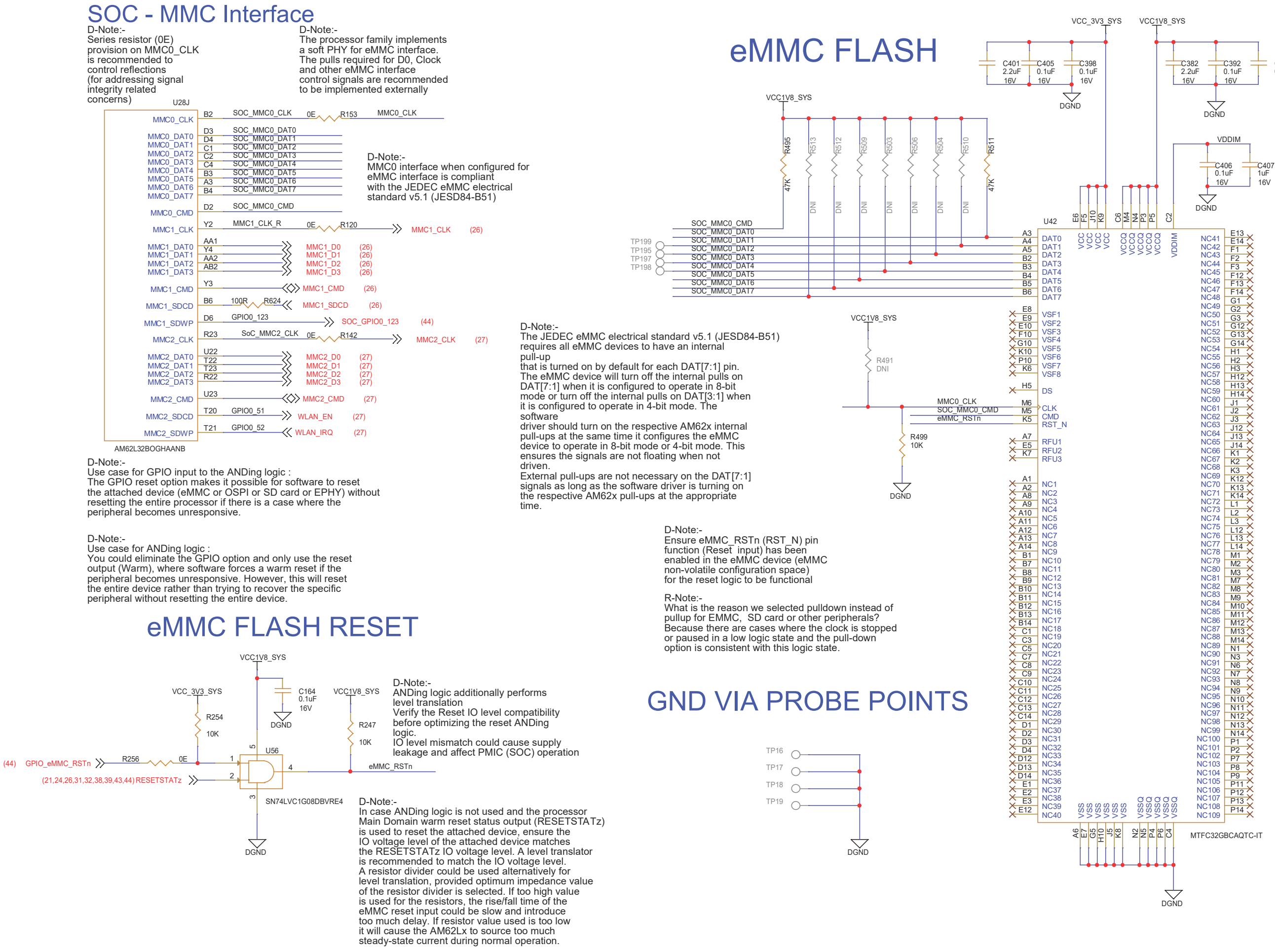
5. Connection of DDRSS RESETn signal directly to LPDDR4_RESET_N memory reset input (to hold the signal low during power-on initialization). The recommendation is to add a pulldown (10kΩ) for DDRSS RESETn signal and place close to the memory device reset input pin.
6. Connection of chip select CSn0 to the attached memory device. Follow *AM62x, AM62Lx DDR Board Design and Layout Guidelines* based on selected memory
7. Memory device ODT pulled up through a resistor (2.2kΩ used on EVM, the recommendation is to not connect DDRSS signals and follow the EVM schematics).
8. DDR0_CAL0, DDRSS IO pad calibration resistor (240Ω, ±1%) connected across DDR0_CAL0 and VSS.
9. ZQ0 Memory device IO calibration resistor (240Ω, ±1%) connected across ZQ and VDD_LPDDR4.
10. Data Bit or Byte Swapping. Follow *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

7.3.2 Multi-Media Card/Secure Digital (MMCSD)

The processor family supports x3 (three) Multi-Media Card/Secure Digital (MMC/SD/SDIO) (8b(4b) + 4b + 4b).

7.3.2.1 MMC0 - eMMC (Embedded Multi-Media Card) Interface

Figure 7-3 includes processor MMC0 interface configured for eMMC interface and connected to eMMC memory U42. The required pullups for data0 and CMD signals, series resistor (placed near to processor clock output) and pulldown for clock input (placed neat to memory device input) and the eMMC reset logic using ANDing logic are included. D1-D7 pullups are supported internal to the Memory device and processor and hence the external pullup is configured as DNI.



D-Note:-
Series resistor (0E) provision on MMC0_CLK is recommended to control reflections (for addressing signal integrity related concerns)

D-Note:-
The processor family implements a soft PHY for eMMC interface. The pulls required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally

D-Note:-
MMC0 interface when configured for eMMC interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

D-Note:-
Use case for GPIO input to the ANDing logic :
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note:-
Use case for ANDing logic :
You could eliminate the GPIO option and only use the reset output (Warm), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

D-Note:-
The JEDEC eMMC electrical standard v5.1 (JESD84-B51) requires all eMMC devices to have an internal pull-up that is turned on by default for each DAT[7:1] pin. The eMMC device will turn off the internal pulls on DAT[7:1] when it is configured to operate in 8-bit mode or turn off the internal pulls on DAT[3:1] when it is configured to operate in 4-bit mode. The software driver should turn on the respective AM62x internal pull-ups at the same time it configures the eMMC device to operate in 8-bit mode or 4-bit mode. This ensures the signals are not floating when not driven.
External pull-ups are not necessary on the DAT[7:1] signals as long as the software driver is turning on the respective AM62x pull-ups at the appropriate time.

D-Note:-
Ensure eMMC_RSTn (RST_N) pin function (Reset input) has been enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

R-Note:-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

D-Note:-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect PMIC (SOC) operation

D-Note:-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.
A resistor divider could be used alternatively for level translation, provided optimum impedance value of the resistor divider is selected. If too high value is used for the resistors, the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If resistor value used is too low it will cause the AM62Lx to source too much steady-state current during normal operation.

Figure 7-3. MMC0 eMMC Interface

7.3.2.1.1 AM62Lx Processor Family

The processor family supports x1 peripheral instance MMC0 that can be configured for eMMC/SD/SDIO interface. MMC0 is recommended for eMMC interface since **MMC0 has been timing closed for eMMC interface**. MMC0 supports 8-bit eMMC (embedded Multi-Media Card) interface. For supported speeds, see the *MMC0 - eMMC/SD/SDIO Interface* section of processor-specific data sheet, refer EVM for implementation. When not used for eMMC interface, the MMC0 signals can be used for on-board SDIO interface or as IOs or other supported muxed functions. Interfacing MMC0 port for SD card is not recommended.

For more information on eMMC memory interface, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface

[FAQ] AM62A7: MMC0 Pull Resistor Requirements

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

For more information, see the *MMC0 - eMMC/SD/SDIO Interface* section of the processor-specific data sheet.

7.3.2.1.1.1 IO Power Supply

The processor IOs used for the MMC0 (eMMC) interface are referenced to (powered by) VDDSHV2 supply rail (Dual-voltage IO supply for MMC0 IO group).

VDDSHV2 is designed to support power-up, power-down, or dynamic voltage switching independent of other power rails, allowing the operating voltage to change from 3.3V to 1.8V.

The recommendation is to connect VDDSHV2 and the IO supply rail of the attached device to the same supply source.

VDD (CORE voltage) of the attached device can be powered from (by) an independent (different power supply source) supply source.

7.3.2.1.1.2 eMMC Interface Signals Connection

The recommendation is to make the following connections:

- The recommendation is to add a series resistor (0Ω) for MMC0_CLK signal close to processor clock output pin (The series resistor is recommended for control of possible signal reflections, which can cause false clock transitions). The recommendation is to use 0Ω initially and adjust to match the PCB trace impedance.
- An external pulldown (10kΩ) (close to attached eMMC device clock input pin) is recommended for MMC0_CLK near to the attached device clock input pin to hold the clock in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) until the host configures the signal as clock.
- The recommendation is to connect external pullup (47kΩ) for MMC0_DAT0 and MMC0_CMD signals (close to eMMC device) to prevent the attached device inputs from floating until driven by the host.
  - Pullup resistors are optional (delete, DNI) for MMC0_DAT[7:1] signals since the attached eMMC device (for eMMC device that are compliant to eMMC JEDEC standard JESD84-B51) is required (expected) to turn on internal pullups for the MMC0_DAT[7:1] signals until the host changes the bus width to 4-bit or 8-bit mode. The host is expected to enable its internal pullups and the eMMC device is expected to turn off its internal pullups on MMC0_DAT[3:1] when changing to 4-bit mode. The host is expected to enable its internal pullups and the eMMC device is expected to turn off its internal pullups or MMC0_DAT[7:1] when changing to 8-bit mode.
- The recommendation is to connect a pulldown with test point (optional) for DS signal (close to the eMMC device).

7.3.2.1.1.3 eMMC (Attached Device) Reset

Note

Make sure eMMC_RSTn (RST_N) pin function (Reset input) has been enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional.

The recommendation is to implement the attached device (eMMC memory) reset using a 2-input ANDing logic since the ANDing logic provides flexibility to be able to reset the attached device in all processor reset condition including local reset (in use cases where the attached device becomes non-responsive and needs to be reset without a power cycle). Processor GPIO is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (connected) to reset the EPHY (attached device), the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. In case the resistor divider value is too high the rise/fall time of the processor IO connected to eMMC reset input can be slow and introduce delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

7.3.2.1.1.4 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant EVM implementation) bulk and decoupling capacitors have been provided for VDDSHV4 supply rail and the attached device (CORE and IO supplies).

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

7.3.2.1.1.5 MMC0 (eMMC) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and implements a soft eMMC PHY.
3. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
4. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of D0-D7 (data) of processor to D0-D7 of attached device or similar connections)
5. Connection of pullups for DAT0 and CMD signals. Pullup value used vs allowed for pullup resistor value to be within the standards requirements.
6. Series resistor provision for MMC0_CLK and placement.
7. Pulldown implementation for MMC0_CLK, placement and value.
8. Processor IO supply for IO group (VDDSHV2) and the attached eMMC device IO supply power source connection.
9. Implementation of attached device reset logic to support boot mode configuration.
10. Implementation of attached device reset logic in case boot from the attached memory device is not required (using RESETSTATz)
11. Reset signal IO level compatibility between processor and attached device.
12. Addition of required bulk and high frequency capacitors, and value.

Schematic Review

Follow the below list for the custom schematic design:

1. Required bulk and decoupling capacitors are provided for processor and attached device IO supply rails. The recommendation is to compare with the SK schematic (SK-AM62P-LP) implementation as a starting point.
2. The recommendation is to compare the eMMC memory interface with EVM schematic implementation for provisioning of parallel pulls, series resistors, and the resistor values.
3. IO supply for IO group VDDSHV2 (fixed, 1.8V or 3.3V) and the attached eMMC device IO supply is powered from the same power source and follow the ROC.
4. The recommendation is to connect external pullup (47kΩ) for the MMC0_DAT0 and MMC0_CMD signals close to eMMC device. Provision for external pullups is optional for MMC0_DAT[7:1]. (The eMMC device (as long as the eMMC device is compliant to the eMMC JEDEC standard) has the pullups enabled for data signals MMC0_DAT[7:1]. The eMMC device turns off the MMC0_DAT[3:1] pullups when entering 4-bit mode and MMC0_DAT[7:1] pullups when entering 8-bit mode. The eMMC host software turns on the respective MMC0_DAT[7:1] pullups when the software changes the mode).
5. The recommendation is to provision for a series resistor (0Ω) on MMC0_CLK and placed close to the processor clock output pin. The series resistor has been provisioned for control of possible signal reflections, which can cause false clock transitions.
6. The recommendation is to add a pulldown (10kΩ) to the eMMC attached device clock signal near to the attached device clock input (since there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with the logic state).
7. In case eMMC boot mode configuration is required, 2-input ANDing logic can be used for implementing eMMC attached device reset. Processor GPIO is connected as one of the inputs to the AND gate with provision for pullup near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).
8. Alternatively, warm reset status output RESETSTATz can be connected directly to reset the attached device. In case RESETSTATz is used, the recommendation is to match IO level between the processor reset status output and the attached device reset input. The recommendation is to verify IO level matching implementation (level shifter or resistor) follow the design recommendations.
9. In case eMMC memory is not used for boot, the attached eMMC device reset input can be controlled by using only the processor GPIO. The recommendation is to pulldown the reset input of the eMMC memory device.

Additional

1. ANDing logic additionally performs IO level translation. The recommendation is to verify the reset input IO level compatibility while optimizing the reset ANDing logic. IO level mismatch can cause residual voltage and affect board performance.
2. An external pullup on CMD and DAT0 is recommended as per the eMMC JEDEC standard and also to make sure the attached eMMC memory device inputs does not float until the software initializes the processor IOs associated with MMC0 interface. External pulls are recommended because the IOs associated with MMC0 are implemented with standard dual-voltage LVCMOS IO cells with the capability of multiplexing additional signal functions to the respective device pins. MMC0 interface IO buffers are off during reset and after reset.
3. The recommendation is to verify eMMC memory device reset eMMC_RSTn is enabled (eMMC non-volatile configuration space) for the external reset logic to be functional. The GPIO reset option is used to reset the attached eMMC device without resetting entire processor if there is a case where the peripheral becomes unresponsive. Only warm reset status output can be used to reset the attached eMMC device. Software forces a warm reset when the peripheral becomes unresponsive. However, using warm reset status output resets the entire processor, rather than trying to recover the specific peripheral without resetting the entire processor. When RESETSTATz is used to reset the attached device, the recommendation is to verify the IO level of RESETSTATz matches the attached device IO levels.
4. A level translator is recommended to match the processor IO output level with the attached device reset input level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. If the resistor divider resistance value is too high, then the rise or fall time of the

eMMC reset input can be slow and introduce delay. If the resistor divider resistance value is too low, then the processor sources too much steady-state current during normal operation.

5. Adding a capacitor at the reset input of eMMC attached device is not recommended when RESETSTATz or processor IO is connected directly. A stand-alone reset connection using RC to reset the eMMC memory device is not recommended.

7.3.2.1.2 Additional Information on eMMC PHY

The recommendation is to refer to the notes in the *Signal Descriptions* section, *MMC, MAIN Domain* sub-section of the processor-specific data sheet.

Note

There are implementation difference in the eMMC Controller and eMMC PHY IPs used in different processor families. The recommendation is to follow the processor-specific recommendations for the eMMC interface including recommended pullup configuration and value when migrating to a different Sitara processor family. The recommendation is to review the processor-specific data sheet, TRM, relevant SK or EVM and following the connection recommendations for the processor and attached device.

Processor-specific EVM implementation can be followed as a starting point reference.

7.3.2.1.3 MMC0 – SD (Secure Digital) Card Interface

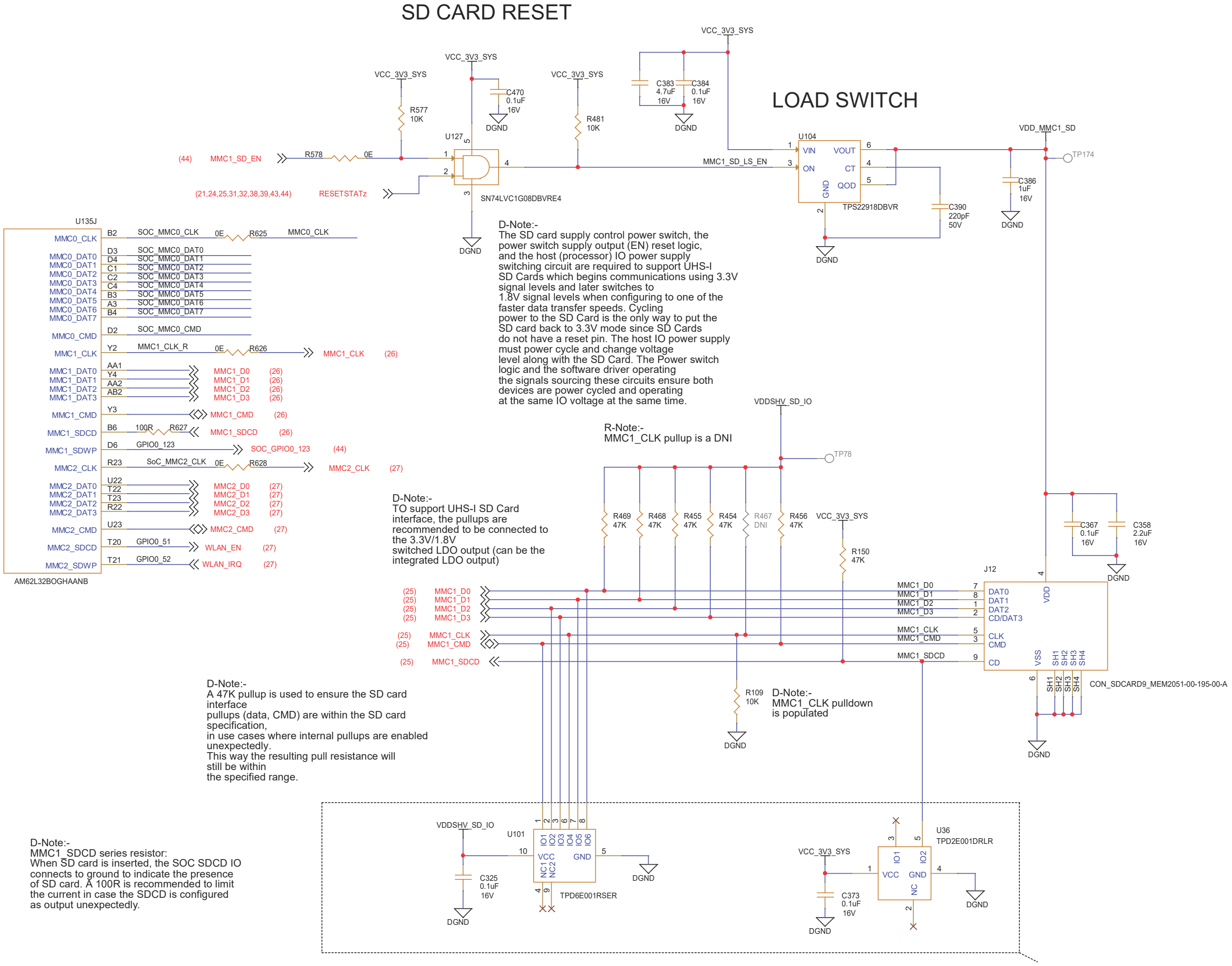
MMC0 peripheral instance has been timing closed for eMMC interface and eMMC interface has been implemented on the MMC0 interface in the EVM (schematics). CD (Card Detect) and WP (Write Protect) functionality (pins) are not supported on the MMC0 interface to implement SD card interface.

When eMMC interface is not used, the recommendation is to configure MMC0 port for other muxed functions supported (or SDIO embedded interface). The recommendation is to always confirm the software support provided (use E2E) before implementing embedded SDIO interface.

Interfacing SD card to MMC0 port is not recommended. The recommendation is to configure MMC1 port for SD card interface.

7.3.2.2 MMC1/MMC2 – SD (Secure Digital) Card Interface

Figure 7-4 includes MMC1 interface configured for SD Card Interface (recommended) connected to SD card connector J2. The implementation supports UHS-I SD card and includes series resistor (placed near to processor clock output pin) and pulldown for SD card clock input (placed near to the SD card socket clock input pin) , 47K pullups for SD card D0-D3 data and SD card CMD signals referenced to VDDSHV_SD_IO (3.3V/1.8V, switched IO supply), R150 pullup (47K for 3.3V (10K for 1.8V) or common 10K) connected to SDCD pin of MMC1 interface. Load switch U104 has been provided for resetting the SD card supply (for UHS-I SD card). ANDing Logic to reset the SD card power switch EN is included.



D-Note:-
The SD card supply control power switch, the power switch supply output (EN) reset logic, and the host (processor) IO power supply switching circuit are required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later switches to 1.8V signal levels when configuring to one of the faster data transfer speeds. Cycling power to the SD Card is the only way to put the SD card back to 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power cycle and change voltage level along with the SD Card. The Power switch logic and the software driver operating the signals sourcing these circuits ensure both devices are power cycled and operating at the same IO voltage at the same time.

R-Note:-
MMC1_CLK pullup is a DNI

D-Note:-
TO support UHS-I SD Card interface, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output (can be the integrated LDO output)

D-Note:-
A 47K pullup is used to ensure the SD card interface pullups (data, CMD) are within the SD card specification, in use cases where internal pullups are enabled unexpectedly.
This way the resulting pull resistance will still be within the specified range.

D-Note:-
MMC1_CLK pulldown is populated

D-Note:-
MMC1_SDCD series resistor:
When SD card is inserted, the SOC SDCD IO connects to ground to indicate the presence of SD card. A 100R is recommended to limit the current in case the SDCD is configured as output unexpectedly.

Figure 7-4. MMC1 SD Card Interface

The processor family supports x2 peripheral instances MMC1, MMC2 that can be configured for SD card interface. MMC1, MMC2 interface supports 4-bit SD card interface including support for UHS-I SD card. The recommendation is to use **MMC1 for SD card interface (based on the custom board design requirements)**. MMC1 is recommended for implementing SD card interface since MMC1 supports SD card boot mode, MMC1 IOs are connected to the IO supply for IO group that support SD card functionality. When MMC2 interface is used to implement SD card interface, the signals (SDCD and SDWP) are required to be multiplexed to the IOs connected to VDDSHV1.

For more information, refer to the *MMC1/MMC2 - SD/SDIO Interface* section of the processor-specific data sheet.

7.3.2.2.1 IO Power Supply

MMC1 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV3 supply rail (Dual-voltage IO supply for MMC1 IO group). VDDSHV3 is designed to support power-up, power-down, or dynamic voltage switching independently of other power rails, allowing the operating voltage to change from 3.3V to 1.8V as the transfer speed is increased.

VDDSHV3 supply is recommended to start with 3.3V and allow changing to 1.8V when software is expected (required) to change the IO supply voltage (to support UHS-I SD card).

The recommendation is to use separate supply sources (discrete LDO or PMIC) that can be switched independently for VDDSHV3 supply rail when configured for SD card interface.

The processor family supports an integrated LDO (SDIO_LDO) to power dual-voltage IO supply for MMC1 IO group VDDSHV3 to support IO voltage level switching when UHS-I SD Card interface support is implemented. The output of the SD card power control power switch described in the reset section below is connected as input to the SDIO_LDO (VDDA_3P3_SDIO pin). The output of SDIO_LDO is 3.3V during and after reset and allows switching to 1.8V when host software is ready to change the SD card speed to UHS-I speed (1.8V supply voltage). The output of the SDIO_LDO is controlled by the V1P8_SIGNAL_ENA bit and defaults to 3.3V output.

Make sure the recommended capacitor is connected to CAP_VDDSHV_MMC pin (output of integrated LDO).

MMC1 SD Card Detect (CD) and Write Protect (WP) signals are referenced to (powered by) VDDSHV1 supply rail (IO supply for GENERAL1 IO group). The recommendation is to connect the pullups (10kΩ) for MMC1_SDCD, MMC1_SDWP to the same supply rail connected to VDDSHV1 (fixed supply).

SD Card Detect (CD) input to the processor connects directly to ground when the SD card is inserted. A series resistor (100Ω) is recommended to limit the current in case the IO is configured as output due to programming error.

MMC2 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV4 supply rail (Dual-voltage IO supply for MMC2 IO group). VDDSHV4 is designed to support power-up, power-down, or dynamic voltage switching independently of other power rails, allowing the operating voltage to change from 3.3V to 1.8V as the transfer speed is increased.

VDDSHV4 supply is recommended to start with 3.3V and allow changing to 1.8V when software is expected (required) to change the IO supply voltage (to support UHS-I SD card).

The recommendation is to use separate supply sources (discrete LDO or PMIC) that can be switched independently for VDDSHV4 supply rail when configured for SD card interface.

MMC2 SD Card Detect (CD) and Write Protect (WP) signals are referenced to (powered by) VDDSHV4 (Dual-voltage IO supply for MMC2 IO group) supply rail or VDDSHV1 supply rail (Dual-voltage IO supply for General1 IO group). The selection of IOs referenced to (powered by) dual-voltage IO supply for IO group VDDSHV1 or VDDSHV4 is use case dependent. The recommendation is to add external pullups (10kΩ) for MMC2_SDCD and MMC2_SDWP (optional) signals can be connected to VDDSHV4 or VDDSHV1 supply rail (depending on the pins (IOs) selected) (close to attached device).

Note

When integrated LDO (SDIO_LDO) is not used to power VDDSHV3, see the *Pin Connectivity Requirements* section of the processor-specific data sheet to terminate the VDDA_3P3_SDIO and CAP_VDDSHV_MMC pins.

7.3.2.2.2 Signals Connection

The recommendation is to note the change in mapping of the dual-voltage IO supply for IO groups and make the connections as below when MMC1 and MMC2 interface signals are used to implement SD card interface:

Note

IO supply for IO group VDDSHV0 for AM62x corresponds to VDDSHV1 for AM62Lx

IO supply for IO group VDDSHV5 for AM62x corresponds to VDDSHV3 for AM62Lx

IO supply for IO group VDDSHV6 for AM62x corresponds to VDDSHV4 for AM62Lx

7.3.2.2.2.1 MMC1 Signals Used for SD Card Interface (Recommended)

- The recommendation is to add a series resistor (0Ω) for MMC1_CLK (close to processor clock output pins for control of possible signal reflections). A pulldown (10kΩ) is recommended for MMC1_CLK near to the attached device input to hold the clock in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) until the host configures the signal as clock.

- The recommendations is to add external pullup (47kΩ) for the SD card data signals (MMC1_DAT[3:0]) and CMD signal (MMC1_CMD) to prevent the attached device inputs from floating until the host software drives the interface signals. The recommendation is to connect the SD card interface signals pullup to dual-voltage IO supply for IO group (MMC1 = VDDSHV3) supply rail. 47kΩ pullup is recommended for data and command signals to meet the SD card specification (in case internal pullups are unexpectedly enabled the resulting pullup (47kΩ parallel to the internal pullup) value is still within the resistance range specified in the relevant standards).
- The recommendation is to add external pullup (10kΩ) for the MMC1_SDCD and MMC1_SDWP signals connected to the VDDSHV1 supply rail (close to attached device (SD card socket)).
- SD Card Detect (SDCD) input to the processor connects directly to ground when the SD card is inserted. A series resistor (100Ω) to limit the current in case the IO is programmed as output unexpectedly is recommended.

7.3.2.2.2.2 MMC2 Signals Used for SD Card Interface

- The recommendation is to add a series resistor (0Ω) for MMC2_CLK (close to processor clock output pins for control of possible signal reflections). A pulldown (10kΩ) is recommended for MMC2_CLK near to the attached device input to hold the clock in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) until the host configures the signal as clock.
- The recommendations is to add external pullup (47kΩ) for the SD card data signals (MMC2_DAT[3:0]) and CMD signal (MMC2_CMD) to prevent the attached device inputs from floating until the host software drives the interface signals. The recommendation is to connect the SD card interface signals pullup to dual-voltage IO supply for IO group (MMC2 = VDDSHV4) supply rail. 47kΩ pullup is recommended for data and command signals to meet the SD card specification (in case internal pullups are unexpectedly enabled the resulting pullup (47kΩ parallel to the internal pullup) value is still within the resistance range specified in the relevant standards).
- For supporting SD card interface, the recommendation is to use MMC2_SDCD and MMC2_SDWP signals referenced (power) to VDDSHV1. The recommendation is to connect the external pullup (10kΩ) for the MMC2_SDCD and MMC2_SDWP signals to the same supply rail that is connected to VDDSHV1 supply rail (close to attached device (SD card socket)).
- SD Card Detect (SDCD) input to the processor connects directly to ground when the SD card is inserted. A series resistor (100Ω) to limit the current in case the IO is programmed as output unexpectedly is recommended.

7.3.2.2.2.3 Additional Information

See the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design –SD card Interface

[FAQ] AM62L (AM62L32 , AM62L31) Why is MMC1 powered by two different voltage supplies, VDDSHV1 and VDDSHV3 ?

[FAQ] AM62A7-Q1: how to connect the pin net VDDSHV4, VDDSHV5, and VDDSHV6 if SD card is not used

[FAQ] AM6442: AM6442 MMC1

FAQ] AM625: MMC interface

The FAQs are generic and can also be used for the AM62Lx processor family.

7.3.2.2.3 SD Card Power Supply Switch EN Reset Logic

The recommendation is to provide provision for a software-enabled (controlled) power switch (load switch) that sources the power supply (VDD) to the SD card. A fixed 3.3V supply (processor IO supply) is connected as the input to the power switch.

Use of power switch allows power cycling of the SD card supply (since resetting the power switch is the only way to reset the SD card) and resetting the SD card to the default state when UHS-I SD card is used.

The recommendation is to implement the SD card power switch enable and reset logic using a 2-input ANDing logic since the ANDing logic provides flexibility to be able to reset the attached device in all processor reset condition including local reset (in use cases where the attached device becomes non-responsive and needs to be reset without a power cycle). Processor GPIO is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support SD card boot) near to the ANDing logic AND gate and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

The external power switch sourcing the SD card power supply is recommended to default to ON (powered state) to support SD card boot.

For implementation, see the processor-specific EVM.

7.3.2.2.4 External ESD Protection for the SD Card Interface Signals

External ESD protection is recommended for the SD card interface signals (data, clock, and control signals). Internal ESD protection is not designed to handle the board or end equipment level ESD requirements.

7.3.2.2.5 Capacitors for the Dual-voltage IO Supply for IO Groups Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant EVM implementation) bulk and decoupling capacitors have been provided for VDDSHV1, VDDSHV3 and VDDSHV4 supply rails and attached devices.

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

> **Note**
>
> The recommendation is to follow the processor-specific connection recommendations for data and control signals. The recommendation is to place the series resistor for the clock close to processor clock output pin for control possible signal reflections.

7.3.2.2.6 SD Card Interface (MMC1) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Verify the MMC port used for SD card interface. The recommendation is to use MMC1 for SD card interface.
3. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
4. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of D0-D3 (data) of processor to D0-D3 of attached device or similar connections)
5. Implementation of series resistor and pulldown for MMC1_CLK
6. MMC1 CMD and DAT [3:0] signals interface connection including addition of recommended pulls, Pull values used for the data, command and clock signals
7. IO supply for IO group supply connection
8. Connection of MMC1 SDCD and SDWP signals including the connection of power supply (IO supply for IO group) and external pullup, pullup value.
9. Circuit implementation to support UHS-I card including IO supply voltage switching LDO (integrated LDO or external LDO) and SD card power control power switch
10. Integrated LDO input supply connection (Output of SD card power switch)
11. Supply rail connected to the SD card power switch input
12. Implementation of SD Card Power supply, power switch EN Reset logic to support boot
13. Supply voltage referenced to SD card data and CMD interface signals (VDDSHV3) and SDCD, SDWP (VDDSHV1)
14. ESD protection provision for the SD card interface signals
15. Addition of required bulk and high frequency capacitors, and value.

Schematic Review

Follow the below list for the custom schematic design:

1. The MMC1 CLK, CMD, and DAT[3:0] signals interfaces are implemented using SDIO buffers referenced to (powered by) dual-voltage IO supply for IO group VDDSHV3 (SDIO buffer type IOs support dynamic voltage switching 3.3V or 1.8V to support UHS-I SD card).
2. Required bulk and decoupling capacitors are provided for the supply rails. The recommendation is to follow the processor-specific EVM implementation for bulk and decoupling capacitors when recommendations are not available.
3. Supply rails connected to processor dual-voltage IO supply for IO groups VDDSHVx (VDDSHV3 and VDDSHV1) follow the ROC.
4. 47kΩ pullup is recommended for data and command signals to meet the SD card specification (in case internal pullups are unexpectedly enabled the resulting pullup (47kΩ parallel to the internal pullup) value is still within the resistance range specified in the relevant standards).
5. Series resistor (0Ω) for MMC1_CLK is placed close to processor clock output pin for control of possible signal reflections (which can cause false clock transitions). A pulldown (10kΩ) is placed near to the attached device clock input.
6. MMC1 SDCD and SDWP signals are implemented using LVCMOS buffers referenced to (powered by) IO supply for IO group VDDSHV1 through a 10kΩ , which operate at a fixed 1.8V or 3.3V.
7. The recommendation is to add a series resistor 100Ω on the SDCD pin since the processor IO connects directly to the ground when the SD card is inserted.
8. Verify the integrated LDO configuration and input, output connection.
9. To support UHS-I SD card, while the IO voltage for SD card interface can be 1.8V or 3.3V, the SD card VDD supply is a fixed 3.3V supply (switched 3.3V_SYS, processor IO supply 3.3V)
10. The recommendation is to provide provision for a software-enabled (controlled) power switch (load switch) that sources the power supply (VDD) to the SD card. A fixed 3.3V supply (processor IO supply) is connected as the input to the power switch. The output of the power switch is connected to VDDA_3P3_SDIO (SDIO 3.3V analog supply, input to the internal SDIO LDO).
11. The recommendation is to implement the SD card power switch enable and reset logic using a 2-input ANDing logic since the ANDing logic provides flexibility to be able to reset the attached device in all processor reset condition including local reset (in use cases where the attached device becomes non-responsive and needs to be reset without a power cycle). Processor GPIO is connected as one of the inputs to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support SD card boot) near to the ANDing logic AND gate and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is MAIN domain warm reset status output (RESETSTATz). The external power switch sourcing the SD card power supply is recommended to default to ON (powered state) to support SD card boot.

Additional

1. The recommendation is to connect the SD card interface to MMC1 interface since MMC1 supports boot. The logic state of the MMC1_SDCD and MMC1_SDWP inputs to the host must not change when a UHS-I SD card changes the IO operating voltage. Maintaining a valid logic state is not possible if the signals propagate through an input buffer of a dual-voltage SDIO cell that changes voltage. The signal functions are assigned to IOs that do not change voltage dynamically. Signals only connect to switches in the SD card connector, so there is no reason for the signals to change voltage when the SD card signals change operating voltage. The MMC1_SDCD and MMC1_SDWP signals are required to connect to the SD card connector switches and pull high with external pull resistors connected to the VDDSHV1. The other MMC1 SD card interface signals (DAT[3:0], CMD) are required to have the pullups connected to VDDSHV3 source that dynamically switches the voltage.
2. An SD card power switch (with the power switch supply EN pin reset logic) and the host IO power supply circuit is required to support UHS-I SD cards which begins communication using 3.3V IO level and later change to 1.8V IO level when changing to one of the faster data transfer speeds. Cycling power to the SD card is the only way to cycle back into 3.3V mode since SD cards do not have a reset pin. The host IO power supply must power off and on and change voltage at the same time as the SD card. The circuits and the software driver operating the signals sourcing the circuits verifies that both devices are off, or on and operating at the same IO voltage at the same time.

3. UHS-I SD card support implementation and integrated LDO use case: There is no requirement for VDDA_3P3_SDIO power rail to ramp along with the other 3.3V power rails. There is no issue with VDDA_3P3_SDIO being off until after reset is released. The SDIO_LDO only controls the operating voltage of the AM62Lx VDDSHV3 IOs it does not control the operating voltage of the SD card. The SD card features a SDIO_LDO equivalent circuit that changes its IO operating voltage from 3.3V to 1.8V via a command, but the only way to change the SD card IO operating voltage back to 3.3V is to cycle power (reset). The AND gate and load switch applies power to the AM62Lx SDIO_LDO and the SD card (after reset) and the ROM code provides enough delay to verify the SD card is ready.

   During processor boot, the ROM code checks the status of the card detect input (SDCD). The input is recommended to be low to indicate SD card is inserted (detected).

   For implementing SD card interface using MMC2 interface signals, for the data, CMD, clock signals MMC1 connection can be followed. The IO supply for IO group referenced by the MMC2 signals is VDDSHV4. The MMC2_SDCD and MMC2_SDWP signals can also be referenced to VDDSHV4. Connecting a UHS-I SD card to MMC2 requires MMC2_SDCD and MMC2_SDWP to be connected to a fixed supply voltage. The signal functions are recommended to be implemented using alternate pin option (IOSET) that uses an LVCMOS IO type referenced to fixed voltage source VDDSHV1.

7.3.2.3 MMC1/MMC2 SDIO (Embedded) Interface

Figure 7-5 includes MMC2 interface configured for SDIO interface connected to an M.2 interface connector. Pullups for DAT0-DAT3 and CMD, series resistor (placed near to the processor clock output pin) and pulldown (placed near to the attached device) for clock input are included. SDIO interface operates on a fixed voltage - 3.3V or 1.8V.

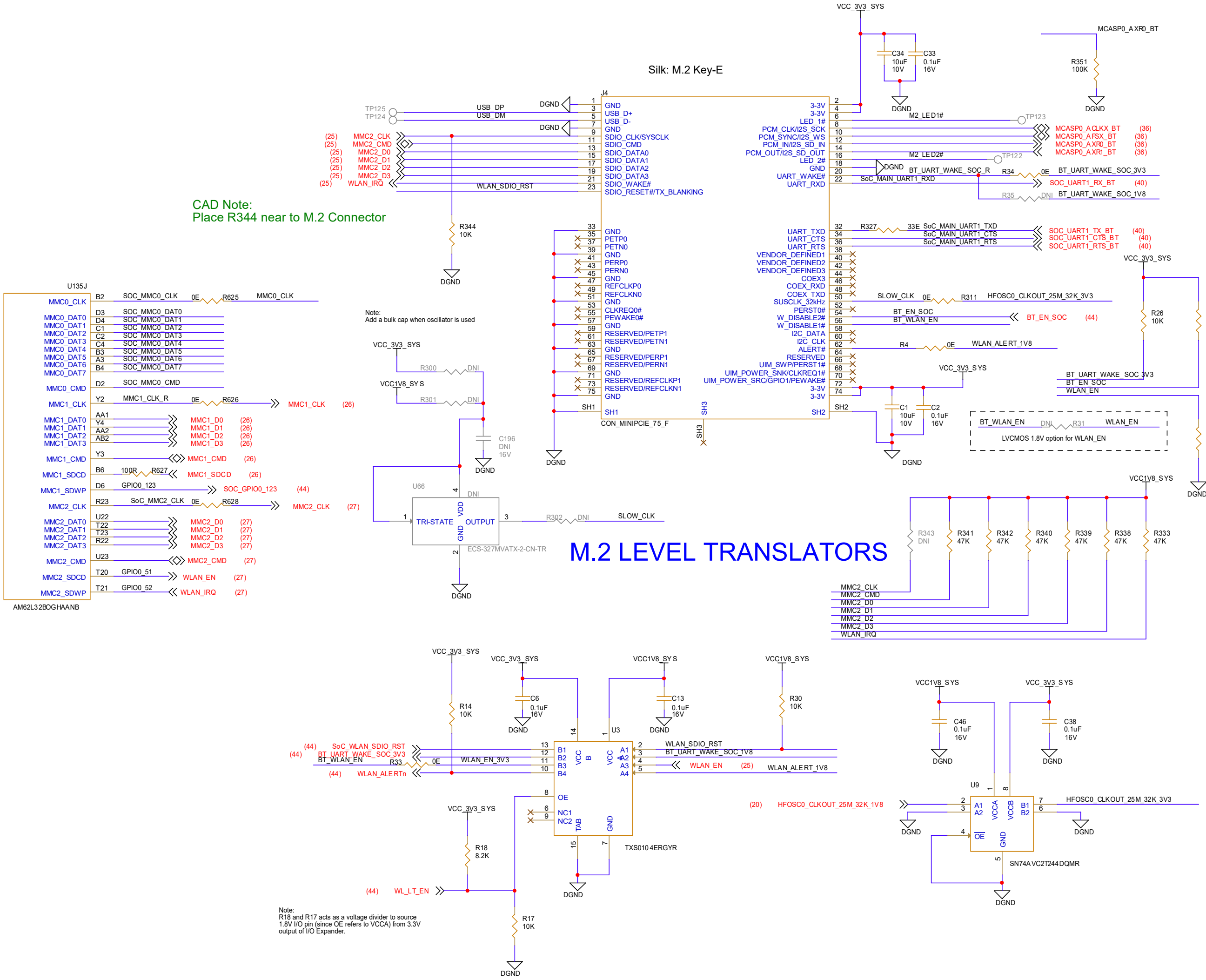


Figure 7-5. M.2 Interface Implementation using SDIO Interface

The processor family supports x2 peripheral instances MMC1, MMC2 that can be configured for SDIO interface. **The recommendations is to use MMC2 interface for on-board fixed voltage embedded SDIO devices use case such as Wi-Fi or Bluetooth transceivers since MMC2 interface has been tested for SDIO interface on the EVM. MMC1 can be used for SDIO as required. Since the SDIO interface has not been tested on MMC1, customer is expected to check the availability of software support and perform the required performance tests on the custom board design.**

A fixed IO supply is used for embedded SDIO interface and simplifies the power architecture. The signals used includes data, command, clock and reset. Connecting SDCD and SDWP signals are optional and can be use case dependent.

There are no specific guidelines about implementation of pulls for embedded SDIO (providing or not providing pulls internal to the interfaced device). Custom board designer implementing an embedded SDIO device is responsible to determine the supported pulls on the SDIO device and apply appropriate external pulls on the custom board design. The processor IOs buffers (for a number of IOs) are off during reset and after reset and are not enabled until the board has booted and the software configures. To prevent floating inputs, the recommendation is to use external pulls on the signals connected to the inputs of attached devices that can float.

For more information, refer to the *MMC1/MMC2 - SD/SDIO Interface* section of the processor-specific data sheet.

Additionally, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – SDIO (embedded) interface

7.3.2.3.1 IO Power Supply

MMC1 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV3 supply rail (Dual-voltage IO supply for MMC1 IO group). MMC1 SD Card Detect (CD) and Write Protect (WP) signals (optional) are referenced to (powered by) VDDSHV1 supply rail (Dual-voltage IO supply for General1 IO group). The recommendation is to connect the pullups (10kΩ) for MMC1_SDCD, MMC1_SDWP for the SDIO interface to the same supply rail VDDSHV1.

MMC2 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV4 supply rail (Dual-voltage IO supply for MMC2 IO group). MMC2 SD Card Detect (CD) and Write Protect (WP) signals (optional) are referenced to (powered by) VDDSHV4 (Dual-voltage IO supply for MMC2 IO group) supply rail or VDDSHV1 supply rail (Dual-voltage IO supply for General1 IO group). The pullups (10kΩ) for MMC2_SDCD, MMC2_SDWP for the SDIO interface can be connected to VDDSHV4 or VDDSHV1 supply rail.

7.3.2.3.2 Signals Connection

Note

The recommendation is to follow the below general recommendations in case there are no pulls recommended. The custom board designer is responsible to review the pulls supported by the attached device and make sure no reverse polarity pulls are externally added.

The recommendation is to make the following connections for MMC1 interface:

- The recommendation is to connect a series resistor (0Ω) for MMC1_CLK (close to processor clock output pin for control of possible signal reflections) and external pulldown (10kΩ) for MMC1_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
- The recommendation is to add external pullups (47kΩ) for the data lines (MMC1_DAT[3:0]) and CMD signal (MMC1_CMD) connected to the respective dual-voltage IO supply for IO group (MMC1 = VDDSHV3) supply rail (close to attached device).
- The recommendation is to add external pullups (10kΩ) for MMC1_SDCD and MMC1_SDWP (optional) signals connected to the VDDSHV1 supply rail (close to attached device).

The recommendation is to make the following connections for MMC2 interface:

- The recommendation is to connect a series resistor (0Ω) for MMC2_CLK (close to processor clock output pin for control of possible signal reflections) and external pulldown (10kΩ) for MMC2_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
- The recommendation is to add external pullups (47kΩ) for the data lines (MMC2_DAT[3:0]) and CMD signal (MMC2_CMD) connected to the respective dual-voltage IO supply for IO group (MMC2 = VDDSHV4) supply rail (close to attached device).
- The recommendation is to add external pullups (10kΩ) for MMC2_SDCD and MMC2_SDWP (optional) signals connected to VDDSHV4 or VDDSHV1 supply rail (depending on the pins (IOs) selected) (close to attached device).

7.3.2.3.3 SDIO (MMC2 Recommended, Embedded) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. There are no specific guidelines about implementation of pulls (CLK, DATA, CMD, SDCD, SDWP) for embedded SDIO (providing or not providing pulls internal to the interfaced device). Custom board designers

implementing an embedded SDIO device are responsible for determining the supported pulls on the SDIO device and apply appropriate external pulls on the custom board design.
3. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
4. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of D0-D3 (data) of processor to D0-D3 of attached device or similar connections)
5. Implementation of series resistor and pulldown for MMC2_CLK
6. Implementation of pullups for MMC2 CMD, and DAT [3:0] signals
7. Dual-voltage IO supply for IO group supply connection (fixed voltage connected)
8. Implementation of MMC2 SDCD and SDWP signals connection
9. Implementation of attached device reset logic
10. Addition of required bulk and high frequency capacitors, and value.

Schematic Review

Follow the list below for the custom schematic design:

1. The MMC2 CLK, CMD, and DAT[3:0] signals interfaces are implemented using SDIO buffers referenced to (powered by) dual-voltage IO supply for IO group VDDSHV4 (SDIO buffer type IOs support dynamic voltage switching 3.3V or 1.8V to support UHS-I SD card).
2. Required bulk and decoupling capacitors are provided for the supply rails. The recommendation is to follow the processor-specific EVM implementation for bulk and decoupling capacitors when recommendations are not available.
3. For embedded SDIO application, the recommendation is to power dual-voltage IO supply for IO group from the same fixed 1.8V or 3.3V power source that is used to power the IOs of the attached device (Example: Wi-Fi module).
4. MMC2 SDCD and SDWP signals are implemented using LVCMOS buffers referenced to (powered by) dual-voltage IO supply for IO group VDDSHV4 or VDDSHV1 (IOSET configuration), which operate at fixed 1.8V or 3.3V. For SDIO use case VDDSHV4 can be used since the IO supply is not switched. Use of SDCD and SDWP is use case dependent and there are no specific recommendations.
5. Series resistor (0Ω) for MMC2_CLK is placed close to processor clock output pin for control of possible signal reflections (which can cause false clock transitions). A pulldown (10kΩ) is placed for MMC2_CLK near to the attached device clock input to hold the clock input in a low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state). The recommendation is to verify processor or attached device internal pulls are not configured when external pulls are used.
6. Pull values used for the data, command and clock signals. The recommendation is to follow the attached device recommendations or compare the implementation with the EVM schematic implementation. When no recommendations are available for SDIO pulls, as good design practice, a 47kΩ pullup is recommended for the pullup value (to be within the SD card specification when internal pulls are enabled unexpectedly). With 47kΩ, the resulting pull resistance (47kΩ external pullup in parallel to the internal pulldown) value is still within the resistance range specified in the relevant standards. The recommendation is to verify processor or attached device internal pulls are not configured when external pulls are used.
7. Supply rails connected to processor dual-voltage IO supply for IO group VDDSHVx (VDDSHV4 when used for SDIO or VDDSHV1 when IO set is configured) and attached device IO supply follow the ROC.
8. When processor IO is used to implement the attached device reset, a pulldown is recommended to hold the attached device in reset condition until the host initializes the SDIO interface.

Additional

1. The recommendation is to verify if the required external ESD protections have been provided for the interface signals in case the signals are connected over an add-on card.
2. When using MMC1 for embedded SDIO interface, software changes are required since the EVM only implements the SDIO interface on MMC2. Custom board designers are responsible for testing the performance.

3. Processor IO buffers (for MMCx signals) are off during reset and after reset. The IO buffers are not enabled until the board has booted and the software configures the IOs. To prevent floating of processor IOs or the attached device inputs being driven by the processor IOs the recommendation is to add external pulls on the signals connected to the inputs of attached devices.

7.3.2.4 Additional Information

The recommendation is to refer to the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the processor-specific data sheet.

7.3.3 Octal Serial Peripheral Interface (OSPI) or Quad Serial Peripheral Interface (QSPI)

Figure 7-6 includes processor OSPI0 interface connected to x2 attached devices. One of the attached device U34 is configured for OSPI supporting DQS and the other attached device is configured for QSPI (TAP mode).

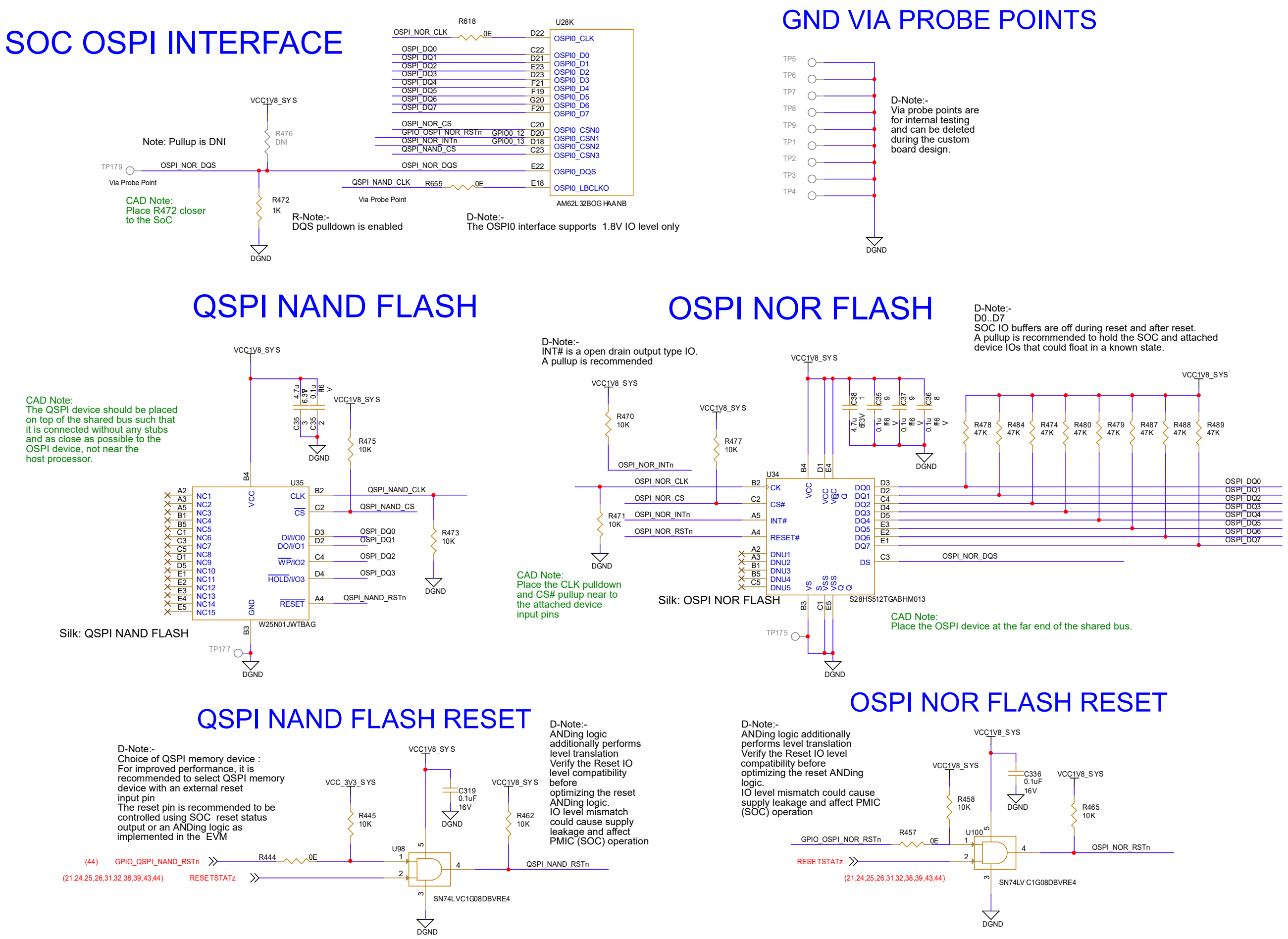
The pullups are placed near to the flash configured for OSPI flash to ensure the memory IOs does not float. OSPI flash is place away from the processor compared to the QSPI flash. The attached device reset logic implemented individually for x2 memory devices is also included.

Note

OSPI0 interface supports a fixed 1.8V IO interface. The recommendation is to verify the IO level compatibility with the attached device. The recommendation is to connect the processor Fixed-voltage supply for GENERAL0_1 IO group (VDDS1, includes OSPI0 IO group) and the attached device IO supply to the same power source. The custom board designer is expected to ensure the design never applies a potential that is greater than the values defined in the ROC during normal operation and *Absolute Maximum Ratings* table during testing or board-bring-up.

Note

Refer the linked section for implementing series resistors and parallel pulls: *Processor-Specific EVM Versus Data Sheet*.



Note: Pullup is DNI

CAD Note:
Place R472 closer
to the SoC

R-Note:-
DQS pulldown is enabled

D-Note:-
The OSPI0 interface supports 1.8V IO level only

D-Note:-
Via probe points are
for internal testing
and can be deleted
during the custom
board design.

CAD Note:
The QSPI device should be placed
on top of the shared bus such that
it is connected without any stubs
and as close as possible to the
OSPI device, not near the
host processor.

Silk: QSPI NAND FLASH

D-Note:-
INT# is a open drain output type IO.
A pullup is recommended

D-Note:-
D0..D7
SOC IO buffers are off during reset and after reset.
A pullup is recommended to hold the SOC and attached
device IOs that could float in a known state.

CAD Note:
Place the CLK pulldown
and CS# pullup near to
the attached device
input pins

Silk: OSPI NOR FLASH

CAD Note:
Place the OSPI device at the far end of the shared bus.

D-Note:-
Choice of QSPI memory device :
For improved performance, it is
recommended to select QSPI memory
device with an external reset
input pin
The reset pin is recommended to be
controlled using SOC reset status
output or an ANDing logic as
implemented in the EVM

D-Note:-
ANDing logic
additionally performs
level translation
Verify the Reset IO
level compatibility
before
optimizing the reset
ANDing logic.
IO level mismatch
could cause supply
leakage and affect
PMIC (SOC) operation

D-Note:-
ANDing logic additionally
performs level translation
Verify the Reset IO level
compatibility before
optimizing the reset ANDing
logic.
IO level mismatch could cause
supply leakage and affect PMIC
(SOC) operation

Figure 7-6. OSPI0 Interface with Clock

The processor family supports connecting x1 memory device (x1 Octal Serial Peripheral Interface (OSPI0) or Quad Serial Peripheral Interface (QSPI0)) or connecting up to x2 memory (Example: x1 OSPI + x1 QSPI) devices over the OSPI0 interface. The OSPI0 IOs are referenced to VDDS1 and support fixed 1.8V IO level.

The valid combinations are below:

- OSPI + OSPI (Faster - DQS)
- QSPI + OSPI (Faster - DQS)
- OSPI (Faster - DQS)
- QSPI (Faster - LBCLKO)

The recommendation is to verify the IO supply for IO group referenced by the IOs (fixed) of the OSPI0 peripheral and the IO voltage level of the attached devices are compatible. The recommendation is to connect the IO supply of the attached device and the IO supply for IO group referenced by the OSPI0 processor peripheral IOs are connected to the same supply source.

For more information, see the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the processor-specific data sheet or collaterals on TI.com.

For more information on OSPI or QSPI memory interface, see the following FAQs:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design – OSPI (OSPI0) interface implementation (on TMDS62LEVM) guidelines

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface

[FAQ] OSPI FAQ for Sitara/Jacinto devices

The FAQ is generic and can also be used for the AM62Lx processor family.

7.3.3.1 OSPI0 Interfaced to Single Device

The recommendation is to follow the AM62x or other processor family OSPI0 interface implementation when using x1 device.

7.3.3.1.1 IO Power Supply

The processor IOs used for the OSPI0 (OSPI or QSPI) interface are referenced to (powered by) VDDS1 supply rail (IO supply for OSPI0 IO group).

The recommendation is to connect VDDS1 and the IO supply rail of the attached device to the same supply source.

VDD (CORE voltage) of the attached device can be powered from (by) an independent (different power supply source) supply source.

7.3.3.1.2 Signals Connection

The recommendation is to make the following connections:

- The recommendation is to connect a series resistor (0Ω) for OSPI0_CLK (close to processor clock output pin for control of possible signal reflections) and external pulldown (10kΩ) for OSPI0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
- The recommendation is to provide provision for a series resistor (0Ω) for OSPI0_LBCLKO (close to processor clock output pin to be able to connect or disconnect the LBCLKO).
- The recommendation is to add provision for external pullup (10kΩ) for CS signal close to attached device input.
- The recommendation is to add provision for external pullup (10kΩ) for INT# output near to the processor IO input configured as interrupt input.
- The recommendation is to provide provision for external pullups (10kΩ or 47kΩ) for the data lines (DAT0:7) connected to the attached device inputs (signals) to prevent the attached device inputs from floating until driven by the host. The recommendation is to connect the pullup resistors to the same power supply that is used to source the VDDS1 supply rail.

7.3.3.1.3 OSPI/QSPI Device Reset

The recommendation is to implement the attached device reset (OSPI/QSPI memory) using a 2-input ANDing logic since the ANDing logic provides the flexibility to be able to reset the attached device in all processor reset condition including local reset (in use cases where the attached device becomes non-responsive and needs to be reset without a power cycle). Processor GPIO is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (connected, without ANDing logic) to reset the attached device, the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. In case the resistor divider value is too high the rise/fall time of the processor IO connected to OSPI/QSPI reset input can be slow and introduce delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

The recommendation is to choose memory device that supports external reset input pin in addition to the data, clock, and chip select inputs.

7.3.3.1.4 Loopback Clock

Refer *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the processor-specific data sheet. The section provides the PCB routing guidelines that is recommended to be followed when connecting OSPI, QSPI, or SPI memory devices.

The recommendation is to verify the loopback clock configuration. Different clock loopback configurations can be implemented using OSPI0_LBCLKO (OSPI0 Loopback Clock Output) and OSPI0_DQS (OSPI0 Data Strobe or Loopback Clock Input) signals. Refer the below diagrams in the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of processor-specific data sheet for information related to supported loopback configurations:

- OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback
- OSPI Connectivity Schematic for External Board Loopback
- OSPI Connectivity Schematic for DQS

External Board Level Loopback

Processor DQS (or Loopback Clock input) is used along with the DS data strobe output of the attached memory device

The recommendation is to connect the DS (in case DS (Read Data Strobe) pin is available on the attached device) pin of the attached device to the OSPI0_DQS pin of the processor. The recommendation is to leave the OSPI0_LBCLKO pin unconnected when not used.

The recommendation is to configure the external loopback in case DS pin is not available on the attached device (Example: QSPI).

The recommendation is to connect the OSPI0_LBCLKO output pin of the processor to the OSPI0_DQS input pin of the processor (take note of the length matching requirements).

When External Loopback is not used, the recommendation is to leave the OSPI0_LBCLKO and OSPI0_DQS pins unconnected.

Note

D0 and D1 pins of the processor OSPI0 interface is recommended to be connected to D0 and D1 pins of the OSPI/QSPI memory device to support legacy x1 commands. Swapping of the data bits is not allowed.

7.3.3.2 Interfaced to x2 Devices

The OPSI0 interface supports interfacing x2 attached devices.

Refer to the EVM for implementation. Refer to the processor-specific (AM62L) product page for addition of application notes related to OSPI0 interface.

7.3.3.3 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant EVM implementation) bulk and decoupling capacitors have been provided for VDDS1 supply rail and the attached device (CORE and IO supplies).

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

7.3.3.4 OSPI0 or QSPI0 Peripheral Interface Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Required memory interface configuration and recommended connections for OSPI or QSPI memory interface

3. Connection of attached device IO supply and the fixed-voltage IO supply for IO group referenced to (powered by) the OSPI0 interface signals (connected to the same supply source)
4. IO level compatibility (1.8V) between processor and attached device.
5. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
6. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of D0-D7 (data) of processor to D0-D7 of attached device or similar connections)
7. Provision for series resistor near to the processor clock output pin and pulldown for OSPI0_CLK signal near to the attached memory device
8. Provision for pullups including value for OSPI/QSPI data interface and CS signals
9. Implementation of attached device reset logic to support boot and connection of attached device reset input.
10. Clock loop back configuration based on the interface selected (OSPI/QSPI) and memory device used
11. Provision for series resistor added on the CS0 that supports boot
12. Connection of DQS input from memory (OSPI) and pulldown for the processor DQS input pin
13. Connection of LBCLKO from processor output (for QSPI) to DQS input and addition of pulldown near to processor DQS input pin
14. LBCLKO connection when not used
15. Connection recommendations to implement x1 or x2 attached device interface
16. Addition of required bulk and high frequency capacitors, and value.

Schematic Review

Follow the below list for the custom schematic design:

1. The recommendation is to compare the OSPI0 or QSPI0 memory interface connections with EVM schematic implementation for provisioning of parallel pulls, series resistors, and the resistor values.
2. The recommendation is to compare implementation of attached device reset logic with the EVM schematic implementation.
3. Series resistor (0Ω) provision for OSPI0_CLK (close to processor clock output pin for control of possible signal reflections) and external pulldown (10kΩ) for OSPI0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
4. Provision for pullups (10kΩ or 47kΩ) are provided for data and control signals that can float (to prevent the attached device inputs from floating until driven by the host). The recommendation is to verify the supply source connected to the pullups.
5. Connecting the OSPI0 interface to X1 (single) or X2 (multiple) attached devices. Follow the EVM or recommended guidelines when connecting the OSPI0 interface to multiple attached devices (more than 1 attached device)
6. IO level compatibility between processor and attached device. The attached device IO supply and the fixed-voltage IO supply for IO group VDDS1 referenced to (powered by) the OSPI0 interface signals are connected to the same supply source.
7. Supply rail connected to the fixed-voltage IO supply for IO group VDDS1 referenced to (powered by) OSPI0 peripheral and attached device IO supply follows the ROC.
8. Implementation of external loopback (based on the use case).
9. Connection of DQS from OSPI memory device and pulldown added for DQS input near to processor.
10. Connection of OSPI0_LBCLKO for QSPI memory device through 0Ω.
11. Pulling up the reset input to a high state during reset or supply ramp (is not recommended).
12. Implementation of reset logic when used for boot using a 2-input (RESETSTATz and processor IO) ANDing logic or using MAIN domain warm reset status output RESETSTATz.
13. When OSPI0 interface is not used for boot, the reset logic can be implemented using a processor IO. A pulldown is recommended near to the reset input.

Additional

1. The recommendation is to verify that the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the processor-specific data sheet is followed.

2. In case OSPI/QSPI boot mode is implemented, the recommendation is to verify the silicon errata, selected memory meets the boot criteria described in the processor-specific TRM (or verify with TI, recommend using E2E).

7.3.4 General-Purpose Memory Controller (GPMC)

The recommendation is to verify the number of GPMC IOs (signals pinned out) available and supported interface configuration in the processor-specific data sheet and the TRM.

Non Muxed-NOR interface is not supported due to the number of address lines pinned out. The description for GPMC0_A0-A6 is the IP functional description (not the pin function description).

7.3.4.1 IO Power Supply

The recommendation is to verify the IO supply for IO group that is referenced by the IOs (fixed or dual-voltage) of the connected processor peripheral and the IO voltage level of the attached device are compatible. The processor IOs used for GPMC interface are referenced to (powered by) VDDSHV0 supply rail (IO supply for GPMC IO group).

The recommendation is to connect VDDSHV0 and the IO supply rail of the attached device to the same supply source.

VDD (CORE voltage) of the attached device can be powered from (by) an independent (different power supply source) supply source.

7.3.4.2 GPMC Interface

The GPMC interface supports specific memory interface configurations. For supported memory interfaces, see the *Media and Data Storage* section in the *Features* chapter, *Device Comparison* table in the *Device Comparison* chapter and *GPMC0 Signal Descriptions* table in the *Terminal Configuration and Functions* chapter of processor-specific data sheet.

The recommendation is to verify the memory interface configuration used (vs supported) and number of attached devices connected to the GPMC interface.

The recommendation is to connect the GPMC interface to x1 (single) device when configured in synchronous mode. Using multiple attached devices (CSn) requires splitting the GPMC clock (and other interface signals) on-board, which can cause signal integrity concerns affecting performance.

A detailed timing analysis is recommended when interfacing multiple memory devices in asynchronous mode. When interfacing to multiple memory devices in asynchronous mode, the control signals are required to be routed to multiple devices. The split routing and loading (trace length and number of devices) can affect custom board performance.

7.3.4.3 Signals Connection

The recommendation is to connect a series resistor (0Ω) for GPMC0_CLK (close to processor clock output pin for control of possible signal reflections) and external pulldown (10kΩ) for GPMC0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).

The recommendation is to provision for external pullups (10kΩ) on GPMC0_CSn0-3 (depending on the configuration) to prevent the attached device inputs from floating until driven by the host.

The recommendation is to provision for external pulls (10kΩ or 47kΩ) for the GPMC address and data interface signals to prevent the attached device inputs from floating until driven by the host.

7.3.4.3.1 GPMC NAND

The active high ready and active low busy (R/B#) output from the NAND flash is open-drain output type signal and is connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). The recommendation is to provide the pullup (commonly used value 10kΩ) close to the attached device.

7.3.4.4 Memory (Attached Device) Reset

When using NAND flash or NOR flash, availability of reset input (pin) depends on the selected memory device. In case the reset pin is supported, the recommendation is to review the required reset configuration and connect the relevant external reset signal to the memory reset input pin including implementing 2-input ANDing logic since the ANDing logic provides flexibility to be able to reset the attached device in all processor reset condition including local reset (in use cases where the attached device becomes non-responsive and needs to be reset without a power cycle). Adding a pullup on the reset pin enables the memory during supply ramp and this is not recommended.

7.3.4.5 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant EVM implementation) bulk and decoupling capacitors have been provided for VDDSHV0 supply rail and the attached device (CORE and IO supplies).

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

7.3.4.6 GPMC Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. GPMC memory interface configuration (NAND or NOR flash), interface mode used - Async or Sync clock mode
3. Connection of GPMC memory NAND or NOR, address and data signals - multiplexed or non-multiplexed, synchronous or asynchronous, data bit width as per the processor-specific data sheet and TRM
4. Supported address and data range (IOs pinned out of the processor as per the processor-specific data sheet)
5. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
6. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of D0-D7 (or higher data) of processor to D0-D7 (or higher) of attached device or similar connections)
7. Connection of series resistor 0Ω near to the processor GPMC clock output pin and pulldown for GPMC0 clock input near to the attached device
8. Connection of required pulls for GPMC interface signals (signals that can float)
9. Connection of open-drain output type signal active high ready and active low busy (R/B#) outputs from the attached memory device (NAND flash)
10. Boot mode input signal connections when configured for alternate function (GPMC interface)
11. Attached device IO compatibility with the processor GPMC interface signals. The attached device IO supply and dual-voltage IO supply for IO group referenced to the GPMC interface signals are connected to the same supply source
12. GPMC interface timing required versus feasible and effect of layout on timing
13. When connecting multiple memory devices in Async mode, the recommendation is to perform timing analysis and load calculation
14. Addition of required bulk and high frequency capacitors, and value.

Schematic Review

Follow the below list for the custom schematic design:

1. GPMC interface configuration and recommended connections. Connection of GPMC memory NAND/ NOR, address and data signals - multiplexed or non-multiplexed, synchronous or asynchronous, data bit width as per the processor-specific TRM.

2. Supported address and data range (IOs pinned out for the processor as mentioned in the processor-specific data sheet).
3. IO level compatibility between processor and attached device. The attached device IO supply and IO supply for IO group referenced to (powered by) the GPMC interface signals are connected to the same supply source and follow ROC
4. The recommended pulls (47kΩ) are provided for the interface signals that can float (to prevent the attached device inputs from floating until driven by the host).
5. The recommendation is to provision for external pullups on GPMC0_CSn0-3 (depending on the configuration) to prevent the attached device inputs from floating until driven by the host.
6. Series resistor (0Ω) provision for GPMC0_CLK (close to processor clock output pin for control possible signal reflections) and external pulldown (10kΩ) for GPMC0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
7. Open-drain output type signal active high ready and active low busy (R/B#) outputs from the NAND flash are connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). The recommendation is to provide the pullup (commonly used value 10kΩ) close to the attached device.
8. Boot mode inputs configured for alternate function (GPMC interface) through a 0Ω to be able to isolate to check boot mode functionality.

7.4 External Communication Interface (Ethernet (CPSW3G0), USB2.0, UART and MCAN)

Note

Refer the linked section for implementing series resistors and parallel pulls: *Processor-Specific EVM Versus Data Sheet*.

7.4.1 Ethernet (MAC) Interface

Figure 7-7 includes CPSW3G (Ethernet) peripheral configured for RGMII interface and connected to Ethernet PHY U87 (DP83867, Gigabit). Series resistor for the MAC interface TDX and RDx signals and parallel pulls for configuring the EPHY parameters (pin strapping) are included. Reset logic to reset the EPHY (individually) using an ANDing logic is shown. The recommended bulk and decoupling capacitors for the EPHY supply rails are also included.

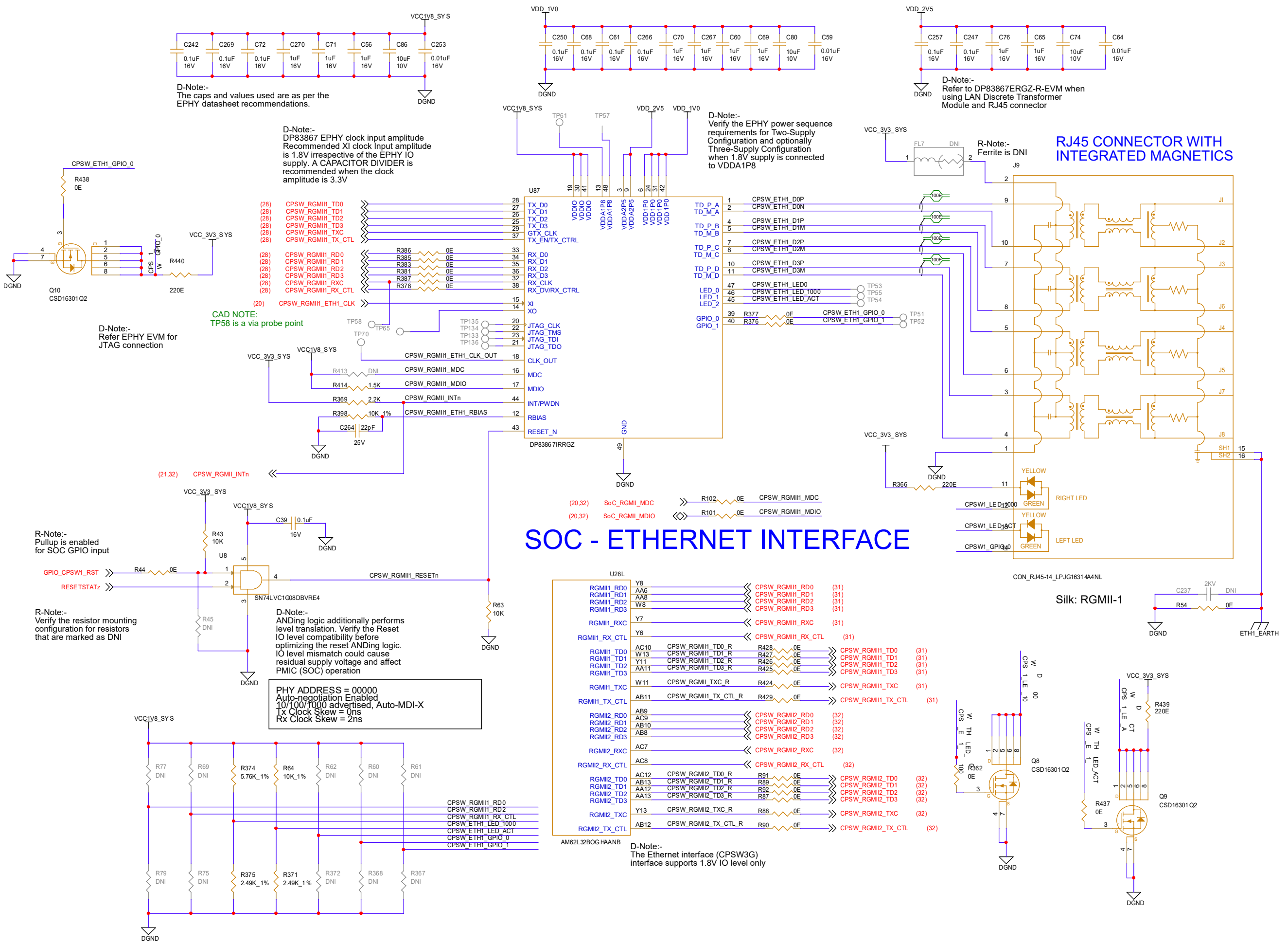


Figure 7-7. SOC MAC - EPHY RGMII Interface

The processor family supports x2 (two) independent Ethernet interface with individual MAC IDs (using CPSW3G0 peripheral). Each of the MAC interface supports RGMII or RMII interface.

For more information on the Ethernet interface, see the following FAQs:

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 and AM2434, AM2432, AM2431 (ALV, ALX) Custom board hardware design - Ethernet

The FAQ is generic and can also be used for AM62Lx processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RGMII interface and RGMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RMII interface and RMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Ethernet PHY RGMII synchronous clock

The FAQ is generic and can also be used for AM62Lx processor family.

7.4.1.1 Common Platform Ethernet Switch 3-port Gigabit (CPSW3G0)

Note

Ethernet interface supports a fixed 1.8V IO interface. The recommendation is to verify the IO level compatibility with the attached device (EPHY). The recommendation is to power the processor Fixed-voltage supply for GENERAL0 IO group (VDDS0, RGMII1 and RGMII2 interface IO groups) and the attached device IO supply from the same power source. The custom board designer is expected to ensure the design never applies a potential that is greater than the values defined in the ROC during normal operation and *Absolute Maximum Ratings* table during testing or board-bring-up.

The processor family supports x1 instance of CPSW3G0 Ethernet switch (with 2 external ports) that can be configured either as a 3-port switch (interfaces to 2 external Ethernet ports (port 1 and 2)) or dual independent MAC interface having individual MAC address.

CPSW3G0 supports RGMII (10/100/1000) or RMII (10/100) interface for each of the external Ethernet interface port. In RGMII interface, both TDx (data transmitted by processor) data path and RDx (data received by processor) data path are completely independent on each other, where each have own clock and data signals that perform source synchronous data transfers.

7.4.1.1.1 IO Power Supply

Processor MAC interface (CPSW3G0) signals (IOs, used for Ethernet interface with EPHYs) are referenced to (powered by) VDDS0 supply rail (IO supply for GENERAL0 IO group). The recommendation is to connect VDDS0 and the IO supply rail of the attached device (EPHYs) to the same supply source (1.8V).

VDD (CORE voltage) of the attached device (EPHYs) can be powered from (by) an independent (different power supply source) supply source.

7.4.1.1.2 MAC (Data, Control and Clock) Interface Signals Connection

Provisioning for series resistors (0Ω or 22Ω, adjust after testing) is recommended for the processor Ethernet MAC interface signals (For TDx signals, the recommendation is to place series resistor near to the processor MAC TDx interface pins). The recommendation is to use the smallest possible package (0402 or smaller) and place series resistors close to source. For the RDx signals internal impedance control (in case EPHY supports) option provided by EPHYs can be used. The recommendation is to provide provision for external series resistors (0Ω) on the RDx signals near to the EPHY pins in case space is not a constraint or EPHY does not support internal impedance control.

The interrupt output of the EPHYs can be connected to the processor EXTINTn (interrupt) pin. The recommendation is to connect a pullup (10kΩ) for the EXTINTn close to processor.

7.4.1.1.3 EPHY Reset

The recommendation is to implement the attached device (EPHY) reset using a 2-input ANDing logic since the ANDing logic provides the flexibility to be able to reset the attached device (EPHY) in all processor reset condition including local reset (in use cases where the attached device becomes non-responsive and needs to be reset without a power cycle). Processor GPIO (used to locally reset the EPHY) is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

When more than one (x2) EPHYs are used, the recommendation is to provide provision to reset the EPHYs individually.

A pullup or pulldown (10kΩ) at the output of the ANDing logic can be used based on the EPHY reset input polarity. The EPHY is required to be held in reset for a specified minimum time after the clock is valid.

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (connected) to reset the EPHY (attached device), the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. In case the resistor divider value is too high the rise/fall time of the processor IO connected to EPHY reset input can be slow and introduce delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

7.4.1.1.4 Ethernet PHY (and MAC) Operation and Media Independent Interface (MII) Clock

The recommendation is to match the clock specifications for the EPHYs and the processor.

7.4.1.1.4.1 Crystal Used as Clock Source for Processor and EPHYs

In case a crystal is used as the clock source for the EPHYs, the recommendation is to match crystal (clock) specifications with the processor clock specifications.

7.4.1.1.4.2 External Oscillator Used as Clock Source

An external (LVCMOS) oscillator can be used as the clock source for the processor (and the EPHYs). A x1 (single) oscillator or multiple oscillators (separate oscillator for each of the EPHYs and processor) can be used. When using x1 (single) oscillator, the recommendation is to buffer the oscillator clock output (use individual buffer for each attached device clock input) before connecting to the processor and EPHYs.

A single channel (with single input and single output) buffers, or single input with dual or multiple output buffer can be used to connect the clock output of the oscillator to the processor and EPHYs. A 1-input to n-output buffer ensures appropriate signal quality on each clock signal.

For a specific use case (requirement for some of the industrial applications using a Time Sensitive Networking (TSN)), single input and two or more output (based on number of EPHYs used) buffer is recommended for the processor and the EPHYs.

The recommendation is to verify that the XO of the EPHY is connected according to the recommended guidelines.

7.4.1.1.4.3 Processor Clock Output (CLKOUT0)

For optimizing the custom board design, the processor clock output (CLKOUT0) can be used as clock source (input) to the EPHYs. CLKOUT0 is buffered internally and is intended to be connected in a point-to-point clock topology. Buffering of the CKLOUT0 (individually) is recommended before connecting to the clock input of the attached devices (EPHYs). A series resistor (0Ω, adjust after testing) is recommended at the source end of the CLKOUT0 for control of possible signal reflections.

EPHY using RGMII interface requires a 25MHz clock input that is not synchronous to any other signals. 25MHz clock does not have any timing requirements, but is important the EPHYs does not receive any non-monotonic transitions on the clock input.

When EPHY is configured for RMII interface, clocking option depends on the EPHY configuration.

When EPHY is configured as a controller, many of the RMII EPHYs use a 25MHz input clock that is not synchronous to any other signals, the 25MHz clock signal does not have any timing requirements, but is important to make sure the EPHY does not receive any non-monotonic transitions on the clock input.

The RMII EPHY provides the 50MHz clock output to the MAC. For RMII use case, the 50MHz data transfer clock is delayed (hardware delay) to the MAC relative to the EPHY. The delay shifts clock to data timing relationship which can erode the timing margin. Eroded timing margin can be a concern for some designs if the delay is large.

When EPHY is configured as a device, the MAC and the EPHY uses a 50MHz common clock that is synchronous to both transmit and receive data. The 50MHz clock is defined in the RMII specification as a common data transfer clock signal that is used by both the MAC and the EPHY, where transitions are expected to arrive simultaneously at the MAC and EPHY device pins. The common clock provides better timing margin for both transmit and receive data transfers. Important requirement is that the MAC and EPHY do not receive any non-monotonic transitions on the clock inputs. To improve the clock signal integrity, the recommendation is to route the common clock signal through a single input, two-output phase aligned buffer. The recommendation is to use equal length signal traces that are half the length of the interface data signals for connecting the clock buffer outputs, where one of the buffered clock output connects to the processor MAC and the other buffered clock output connects to the EPHY clock input.

For RMII interface, the recommended configuration *RMII Interface Typical Application (External Clock Source)* is explained in the processor-specific TRM. When the *RMII Interface Typical Application (Internal Clock Source)* configuration is used, the recommendation is to validate performance on a board level. The recommendation is to provision for connecting an external clock for initial performance testing and comparison with internal clock.

The Ethernet performance (RGMII) is validated on the processor and the EPHY (used on the EVM board) with 25MHz clock frequency.

The CLKOUT0 can be used to source a 25MHz or a 50MHz clock to processor (MAC) and EPHY. The CLKOUT0 output is available after the software configures the clock output. The CLKOUT0 configuration is not recommended when support for Ethernet boot is required. CLKOUT0 connected as EPHY clock input is likely to glitch after the configuration is changed.

Processor clock outputs performance is not defined in the processor-specific data sheet since the clock performance can be influenced by a number of variables unique to each custom board design. The recommendation for custom board designer is to validate timing of all peripherals by using the actual PCB delays, minimum or maximum output delay characteristics, and minimum setup and hold requirements of each device to confirm there is enough timing margin.

7.4.1.1.5 Ethernet PHY Pin Strapping

Some of the TI EPHYs configure the outputs as inputs during reset and latch the EPHY configuration (pin strapping done through resistors) when the EPHY reset is released. Applying appropriate pullup or pulldown (as per EPHY recommendations) on strap inputs (IOs) is recommended (strap inputs also connects to processor IOs). TI EPHY used on the processor-specific EVM use a combination of pullup and pulldown allowing multiple configuration modes to be configured with each pin. During processor reset, the IO buffers and internal pullup or pulldown are OFF, and minimizes any concern of a mid-supply voltage being applied to the processor input buffer by the EPHY. The EPHY is required to be configured to normal state from reset state to drive a valid logic state before enabling any of the associated processor input buffers.

7.4.1.1.6 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type fail-safe IO buffer. The recommendation is to connect external pullup (10kΩ) when a PCB trace is connected and an external input is not being actively driven. Open-drain output type IO buffer has slew rate requirements specified when pulled up to 3.3V. An RC (delay) is recommended to limit the input slew rate. The capacitor is recommended to be placed near to the processor pin.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection

7.4.1.1.6.1 External Interrupt (EXTINTn) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Electrical characteristics (fail-safe and slew rate requirements when pulled to 3.3V)
3. Connection of pullup for EXTINTn IO
4. Connection of RC for EXTINTn IO when pulled to 3.3V including placement of C (near to the processor pin)

Schematic Review

Follow the below list for the custom schematic design:

1. Pullup value used. The recommendation is to compare with the EVM schematic implementation as a starting point.
2. Pullup referenced to (powered by) the processor VDDSHV1 (pullup connected to correct IO voltage level).
3. EXTINTn is an open-drain output type fail-safe IO buffer. An external pullup is recommended when a trace or external input is connected.

4. Open-drain output type IO buffer, EXTINTn has slew rate requirements specified when pulled to 3.3V supply. The recommendation is to add an RC at the input to limit the input slew rate. Refer TMDS64EVM.
5. RC value used for slew rate control. Refer TMDS64EVM. The recommendation is to connect capacitor near to the processor pin.

7.4.1.1.7 MAC (Media Access Controller) to MAC Interface

When implementing EPHY-less (MAC-to-MAC) connection between x2 processors, RGMII interface is recommended (check with TI if the MAC-to-MAC interface is officially supported on the selected processor family) since the clocks are source synchronous.

When MAC-to-MAC interface between x2 processors is implemented, the recommendation is to verify fail-safe operation, matching of clock specifications, and IO level compatibility.

7.4.1.1.8 MDIO (Management Data Input/Output) Interface

The processor IOs used for MDIO interface are referenced to (powered by) VDDS0 supply rail (IO supply for GENERAL0 IO group).

The recommendation is to connect an external pullup (2.2kΩ (Follow EPHY recommendations), close to the EPHY) for the MDIO0_MDIO (MDIO data) signal.

For the MDIO_MDC, the recommendation is to verify if the EPHY supports internal pull (pulldown).

7.4.1.1.9 Ethernet MDI (Medium Dependent Interface) Including Magnetics

In case the EPHY and MDI (copper or fiber) interface including the magnetics and the RJ45 connector are implemented on the processor board, the recommendation is to follow the EVM implementation for MDI interface connections, recommended magnetics (recommending using the magnetic used on the EVM or similar) and connection of RJ45 connector shield to circuit ground. Provision for external ESD protection is recommended.

7.4.1.1.10 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant EVM implementation) bulk and decoupling capacitors have been provided for VDDS0 supply rail and the attached device (CORE, ANALOG and IO supplies).

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

7.4.1.1.11 Ethernet Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Processor MAC to EPHY media independent interface MII configuration - RGMII or RMII.
3. IO level compatibility (1.8V) between processor and EPHY (attached device) MII (MAC) interface signals
4. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
5. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of TDx0-3(RDx0-3) data) of processor to TDx0-3(RDx0-3) of attached device or similar connections)
6. Connection of IO supply for IO group referenced to processor MAC interface signals and EPHY IO supply connected to the same supply source
7. Matching of processor and EPHY clock specifications.
8. Clock configuration used for processor MAC and EPHY for RMII interface (Master, Slave)
9. Implementation of EPHY reset logic.
10. Implementation of x2 EPHYs reset logic.
11. MDIO interface connection and EPHY address configuration.

12. External Pull on the MDIO interface MDC (clock signal) can be optional (EPHY may support internal pulldown; the recommendation is to verify the availability of pull in the EPHY data sheet)
13. Addition of series resistors for the MAC interface signals (TDx, RDx) placed near to the source for control of possible signal reflections
14. Interface configuration and connection for MAC-to-MAC interface (Processor to Processor)
15. Addition of required bulk and high frequency capacitors, and value.

Schematic Review

Follow the list below for the custom schematic design:

1. The recommendation is to compare the bulk and decoupling capacitors used for processor and the EPHYs supply rails with EVM schematic implementation (when TI EPHY is used).
2. The recommendation is to provision for a series resistors (0Ω or 22Ω, adjust after testing, on the TDx signals near to processor MAC TDx output pins) for control of possible signal reflections.
3. The recommendation is to verify the attached device IO supply and the IO supply for GENERAL0 IO group VDDS0 referenced by (powered by) the processor MAC interface signals are connected to the same supply source and follow the ROC.
4. MDIO interface connection including pullup (2.2kΩ (Follow EPHY recommendations)) for MDIO data signal added near to the EPHY. MDIO connection to multiple devices and the addition of pullup near each EPHY. When more than x1 EPHY are used, configuration of EPHY address for MDIO interface.
5. A crystal with internal oscillator or an external oscillator for each EPHYs or a common external oscillator with buffers (outputs are use case dependent) can be used.
6. The recommendation is to match the EPHYs and the processor clock specifications.
7. Clocking of EPHYs and processor MAC for RMII interface including addition of buffers (based on the EPHY configuration) and clock architecture (use of common Oscillator and Buffer with multiple outputs). In case processor clock output is connected to more than one input, each of the clock input is recommended to be the buffered output of the clock.
8. When MAC-to-MAC interface is used, the recommendation is to verify IO level compatibility, fail-safe operation (when x2 processor MACs are referenced to (powered by) different power sources) and matching of clock specifications.
9. The recommendation is to verify the EPHY reset implementation including ANDing logic, AND gate input pullup and EPHY reset input pull with the EVM implementation when TI EPHY is used. A 2-input ANDing logic can be used to implement the attached device (EPHY) reset. Processor GPIO (used to locally reset the EPHY) is connected as one of the input to the ANDing logic AND gate with provision for pullup (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).
10. When more than one (x2) EPHYs are used, the recommendation is to provide provision to reset the EPHYs individually.

Additional

1. The recommendation is to follow the steps below recommended when TI EPHY is used:
    - Obtain a review of the implementation done with the EPHY business unit or product line.
    - The recommendation is to verify recommended bulk and decoupling capacitors are added and the power sequence requirements are followed.
    - The recommendation is to verify RBIAS resistor value & tolerance, selection of the RJ45 connector, external ESD protection provision for MDI signals and connection of RJ45 connector shield to circuit ground
2. A single channel (with single input and single output) buffers, or single input with dual or multiple output buffer can be used to connect the clock output of the oscillator to the processor and EPHYs. For a specific use case (requirement for some of the industrial applications using a Time Sensitive Networking (TSN)), single input and two or more output (based on number of EPHYs used) buffer is recommended for the processor and the EPHYs.
3. When EPHY is configured as RMII peripheral, a single input (common clock input), two-output phase aligned buffer is recommended.

4. Consider adding 0Ω (optional and recommended when space is not a constraint) series resistors near to the attached device (EPHY) for the RDx signals.
5. In case Ethernet boot is considered, the recommendation is to review the silicon errata, verify the supported EPHY interface configurations, MAC interface port used versus recommended, and the recommended clock and interface connection.

7.4.2 Universal Serial Bus (USB2.0)

Figure 7-8 includes connection of processor USB0 and USB1 interfaces. USB1 interface has been configured for Host interface. Power switch with OC (U46) indication controlled by SOC, Common Mode filter on the USB data interface signals and the USB connector is included. Although VBUS divider is shown, VBUS divider is optional for HOST interface.

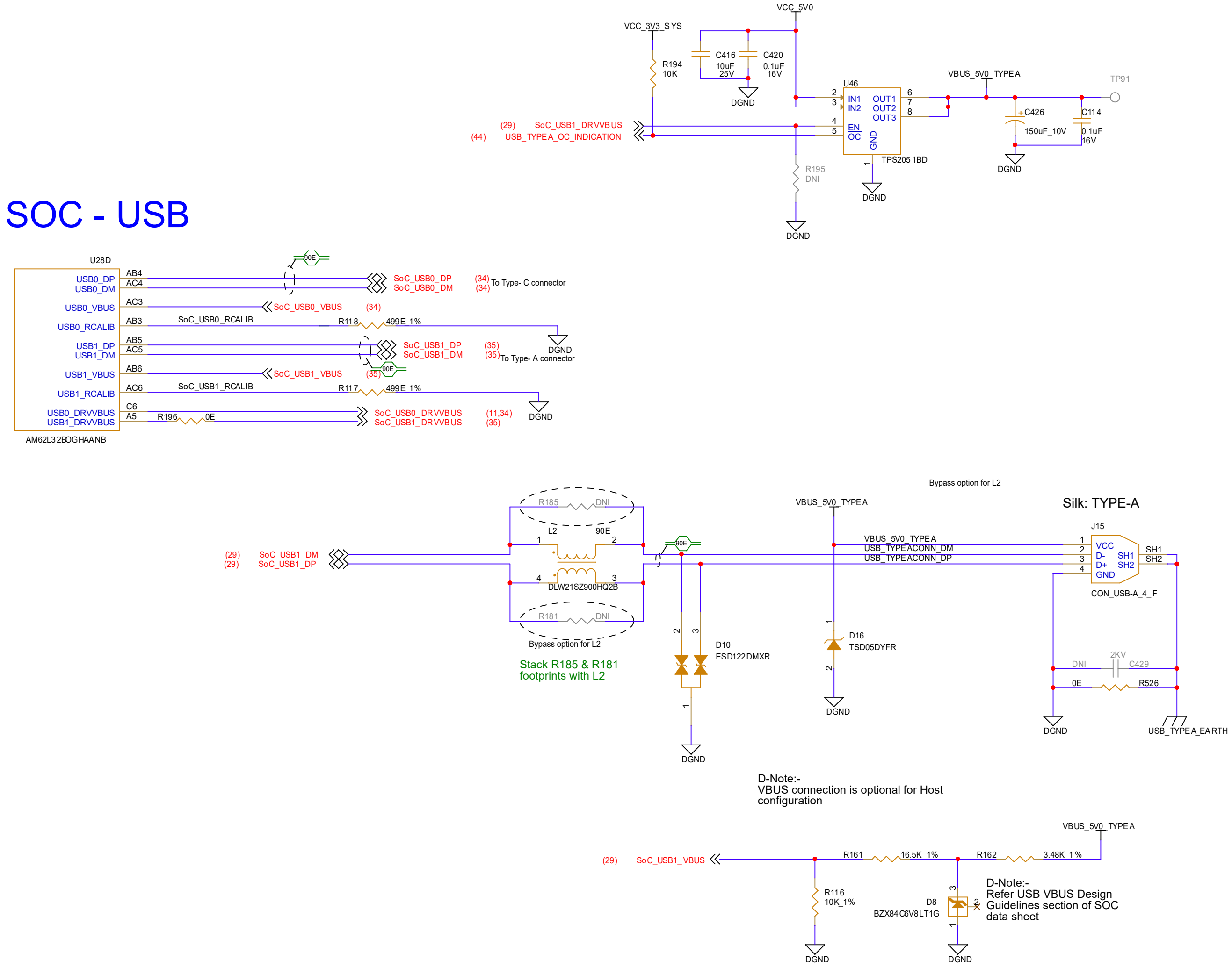


Figure 7-8. USC SOC Host Interface

The processor family supports x2 (two) instances of USB 2.0 interface ports. The USB interfaces (USB0, USB1 ports) can be configured as host or device or Dual-Role Device (DRD).

USBn_VBUS (n = 0-1) is recommended to be connected as per the *USB Design Guidelines* section of the processor-specific data sheet. The supply voltage range for the USBn_VBUS pins is defined in the *Recommended Operating Conditions* section of the processor-specific data sheet. The nominal input voltage applied is equal to the resistor divider output when VBUS supply voltage level is 5V.

USBn_ID functionality can be implemented using any of the processor GPIOs.

Note

USBn_VBUS are fail-safe inputs. The fail-safe input is valid only if the VBUS supply is connected through the recommended *USB VBUS Detect Voltage Divider / Clamp Circuit*.

7.4.2.1 USBn (n = 0-1) Interface When Used

The recommendation is to connect the USB supplies VDDA_CORE_USB (USB0 and USB1, core supply), VDDA_1P8_USB (USB0 and USB1, 1.8V analog supply), and VDDA_3P3_USB (USB0 and USB1, 3.3V analog supply) to the recommended power supply rails as per the processor-specific data sheet.

The recommendation is to connect USBn_DM (n = 0-1) and USBn_DP (n = 0-1) signals directly (without any series resistor or filter capacitor). The recommendation is to route USBn signals with traces that does not include any stubs or test points.

The recommendation is to connect a calibration resistor between USBn_RCALIB (n = 0-1) pin (close to processor RCALIB pin) and VSS. Refer to the processor-specific data sheet for recommended resistor value and tolerance.

7.4.2.1.1 USB Interface Configured as Host

The recommendation is to implement a USB power switch to control the VBUS supply to externally connected USB device. The power switch protects the on-board supply from overload (excess current draw).

The power switch output connects to the USB type A connector. The recommendation is to connect a capacitor (minimum value of 120μF) on the VBUS supply close to the connector.

The USBn_DRVVBUS (n = 0-1) signals (internal pulldown enabled during and after reset) can be used to enable the VBUS power switch. An external pullup near to the power switch enable (EN) pin is not recommended. External pulldown (10kΩ) is optional.

The recommendation is to use a USB power switch with OC (over current) indication, add a pullup (10kΩ or 47kΩ) and connect to the processor IO (input) to detect VBUS overload.

Connection of USBn_VBUS (VBUS supply input including Voltage Divider, Clamp) input is optional.

7.4.2.1.2 USB Interface Configured as Device

The VBUS power supply is sourced from an external host. USB standard recommends connecting < 10μF capacitor to the VBUS close to the USB Type-B connector.

The recommendation is to follow the *USB VBUS Design Guidelines* section of the processor-specific data sheet to divide the USB VBUS voltage (supply near the USB interface connector using resistor divider and zener diode protection) before connecting to USBn_VBUS input.

The zener diode protection (recommended) can be considered to be optional if custom board designer is absolutely sure that the board never sees a VBUS voltage > 5.5V (sourced on-board).

Connecting an on-board supply that is not switched (permanent) or connecting a permanent 3.3V supply with equivalent divider or connecting a permanent 1.65V directly to USBn_VBUS is not recommended or allowed. A switched supply that can be disconnected at the end of the session and switched back during the start of the next session is recommended.

7.4.2.1.3 USB Interface Configured as Dual-Role-Device

In case the custom board uses USB Micro-AB connector, the USBn_ID signal from the connector is recommended to be routed to any of the processor pin. The GPIO pin used can be specified in the board device tree file, including the pinmux setting of the GPIO pin.

Note

Full compliant USB On-The-Go (OTG) feature is not supported. The USB ID pin is not bonded out.

7.4.2.1.4 USB Type-C

In case the custom board design uses a USB Type-C connector, the USBn_ID signal connection is not a requirement. The DRD mode switching is controlled by the USB Type-C companion device.

DRP (Dual Role Port) requires a controller, primarily to switch power based on the negotiated role. In a Device Mode only, USB2.0 only, USB Type-C implementations where the device is not powered by the USB Type-C connector, no USB Type-C controller is required.

- The CC pins at the connector are required to be connected to ground independently using 5.1kΩ resistors.
- The USB DP and USB DM connector pins are shorted on the PCB (DM=B7:A7, DP=B6:A6). Shorting allows for USB2.0 connectivity regardless of cable orientation. The recommendation is to keep the resulting stubs short.

Refer to the *USB VBUS Design Guidelines* section of the processor-specific data sheet for more information on USBn_VBUS input scaling recommendations.

The AM62x SK USB0 interface design can be a reference for implementation of the USB Type-C interface.

See the following FAQ:

[FAQ] SK-AM62A-LP: Is USB OTG possible without PD controller?

The FAQ is generic and can also be used for AM62Lx processor family.

7.4.2.2 USBn (n = 0-1) Interface Connection When Not Used

When USB0 and USB1 interfaces are not used in the custom board design, the recommendation is to provide provision to connect the USB interface signals (for the supported USB boot configuration (USB0 - DFU)) on the USB0 interface and also add provision to connect the required processor USB supplies for the initial board builds.

When both USB0 and USB1 are not used or USB0 or USB1 is not used, the interface signals and the supplies have specific connectivity requirements.

For connecting the USB0 and USB1, interface signals and supply pins, see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

The recommendation is to connect the USB supplies (VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB) to VSS through separate 0Ω resistors.

In case USB0 or USB1 is planned to be used for future expansion, the recommendation is to connect the signals (USBn_DM, USBn_DP, USBn_RCALIB and USBn_VBUS) to a USB connector following the USB interface routing guidelines. The recommendation is to provide provision to connect the required supplies.

7.4.2.3 Additional Information

The recommendation is to connect USBn_DM and USBn_DP signals directly from the processor to the USB hub upstream port. The hub then distributes USBn signals to the downstream ports. As each hub has different implementation requirements, the recommendation is to follow the hub manufacturer recommendations.

For more information on USB2.0 interface, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – USB2.0 interface

The FAQ is generic and can also be used for the AM62Lx processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.4.2.4 USB Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Required USB interface configuration (Host or Device) and recommended connections.
3. Connection of USBn_VBUS pin. USB VBUS design guidelines followed based on the USB interface configuration.
4. Connection of USB supplies including filtering.
5. Connection of USB interface signals between processor and external USB interface connector.
6. Connection of recommended USBn calibration resistor, value and tolerance.
7. Implementation of USB VBUS supply control power switch when USB interface is configured as host.
8. Implementation of pull for USBn_DRVVBUS and USBn_ID functionality.
9. USB power switch, EN using USBn_DRVVBUS and connection of power switch OC output to processor IO.
10. Provision for recommended capacitors on the USB VBUS pin near to the USB connector.
11. Provision for external ESD protections for the USB interface
12. Connection of USB supplies, USB interface signals, calibration resistor and USBn_VBUS when USB interface is not used as per pin connectivity requirements
13. In case USB boot is implemented, the recommendation is to verify the silicon errata, supported interface configuration, USB port and the connections.
14. Provision for USB boot in case USB interface is not implemented
15. Fail-safe operation of USBn_VBUS and USB interface signals.

Schematic Review

Follow the list below for the custom schematic design:

1. The USB interface can be configured for Host (refer relevant EVM schematics) or device or DRD.
2. Direct connection of the USB signals from the processor to the USB connector. USB interface connection matches the required USB interface configuration (Host or Device). Compare the implementation with EVM schematic.
3. Any of the processor GPIO can be used to support DRD.
4. USBn_VBUS connection is optional for USB Host configuration.
5. The recommendation is to follow the processor-specific data sheet recommendations for VBUS voltage divider values and tolerance (±1%). Use of multiple resistors is allowed provided the total resistance value, tolerance and divider ratio is maintained over temperature and voltage. VBUS supply input protection (Zener protection and value) and VBUS capacitor values follow USB standards (refer EVM).
6. USBn_DRVVBUS has an internal pulldown enabled during and after reset. Connecting pullup drives the attached device to mid-supply.
7. Power switch enable connection (in case processor USBn_DRVVBUS is used, pullup is not recommended or allowed since the USBn_DRVVBUS has an internal pulldown enabled during reset and after reset).
8. Connection of power switch OC output to the processor IO and IO level compatibility (pullup connection).
9. Connection of power supplies (core, peripheral and IO). A filtered supply (ferrite and capacitors) is used for VDDA_CORE_USB and VDDA_1P8_USB. VDDA_3P3_USB can be connected to the 3V3_SYS voltage. Refer to specific and latest EVM for implementation as filter implementations are being continuously optimized.
10. Processor USB peripheral supply rails connected follow the ROC.
11. Connection of 499Ω ±1% resistor to USB0 and USB1 RCALIB pins.
12. Connecting 5V supply from the USB connector directly to the USBn_VBUS pin is not recommended or allowed. Changing the processor-specific data sheet recommended VBUS divider and zener value is not recommended or allowed. Fail-safe capability support for VBUS input is valid only when the recommended divider values as per processor-specific data sheet is implemented.
13. Connection of the recommended capacitor based on the USB configuration. Refer EVM schematics for implementation. For USB host, the recommendation is to connect a capacitor (minimum value of 120μF) on the VBUS supply close to the connector. For USB device, the VBUS power supply is sourced from an external host. USB standard recommends connecting < 10μF capacitor to the VBUS close to the USB Type-B connector.
14. The recommendation is to follow the pin connectivity requirements for connecting the USB core, peripheral and IO supplies when USB0 or USB1 is not used, and USB0 and USB1 are not used.

15. USBn_VBUS fail-safe capability is supported when the VBUS configuration as per the processor-specific data sheet is implemented.
16. USB interface signals fail-safe is valid when USB interface is connected to devices that is compliant to the USB specification.

Additional

1. In case Type-C USB interface is implemented using TI devices, the recommendation is to obtain a review of the implementation with the relevant business unit or product line.
2. The recommendation is to verify fail-safe operation of USB interfaces. Applying an external interface signal before processor supply ramps can cause voltage feed and can affect the custom board functions.
3. Common-mode chokes (CMC) can be used on the USB interface signals for EMI control. CMC can reduce the signal amplitude and degrade USB interface performance (speed, data throughput, communication errors). Provision to bypass the CMC using 0Ω resistors is recommended. When a CMC is used on the USB interface signals, the recommendation is to verify the connections including the polarity. Reversing the CMC connection polarity can short the USB interface data signals.
4. DNI external pullup and pulldown connected to USBn_DRVVBUS pin to implement wakeup from deep sleep functionality.
5. The recommendation is to consider marking of differential signals and the differential impedance value.
6. In case USB interfaces are not used, the recommendation is to provide provision for USB0 DFU boot interface for the initial boards.

7.4.3 Universal Asynchronous Receiver/Transmitter (UART)

Figure 7-9 include illustrations for connecting the processor UART signals to external transceiver including the signal connection direction and polarity. Pulls for the IOs that can float and series resistors for control of possible signal reflections are included.

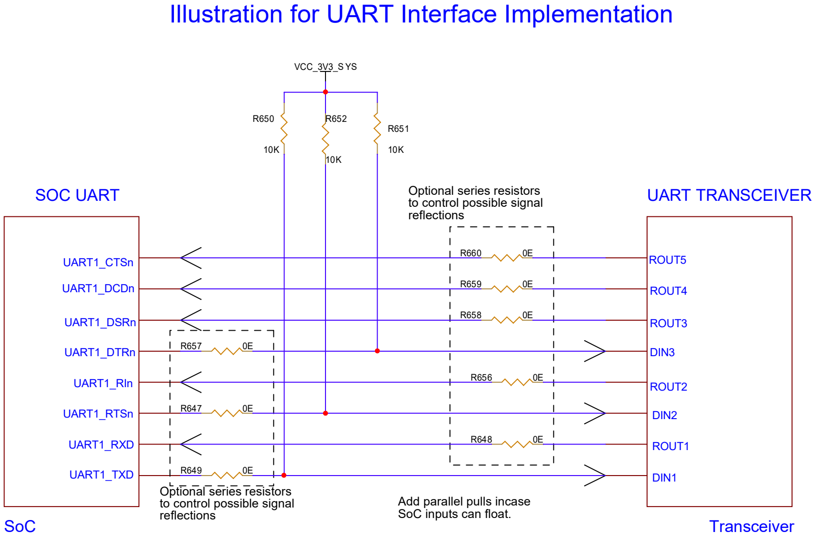


Figure 7-9. UART Interface Connections including Flow Control

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Note

The processor peripheral implements connecting the signal with same function on multiple pins.

The processor family supports x8 (eight) (x7 MAIN domain, x1 WKUP domain) instances of UART interface and supported functions include data transfer (TXD, RXD), Modem control functions (CTS, RTS) and extended modem control signals (DCD, RI, DTR, DSR - supported by MAIN domain UART1).

For the number of UART instances supported, see the processor-specific data sheet. The recommendation is to refer the *Signal Descriptions* section of the processor-specific data sheet for the supported functionalities for each of the UART instances.

The recommendation is to verify the application requirements for UART interfaces (external communication interface or debug) and functions (configuration, 2-wire or 4-wire with flow control).

When an external RS232 transceiver is used, the recommendation is to match the external interface signal IO level and the IO supply for IO group operating voltage level. The recommendation is to power the IO supply of the external transceiver and the processor IO supply for IO group VDDSHVx or VDDSx or VDDS_WKUP or VDDS_RTC from the same source. The recommendation is to verify fail-safe operation of the UART inputs and the voltage level connected to the external pull resistor.

The recommendation is to provision for series resistors (0Ω) on the interface signals, close to source, for isolation (debug) or control possible signal reflections.

Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pullup (10kΩ or 47kΩ) is recommended on the processor UART receive inputs (UARTn_RXD [n = 0-6] and WKUP_UART0_RXD) in case the processor IOs can float (to prevent the attached device inputs from floating until driven by the host). The recommendation is to verify the availability of pulls on the external interface signal and populate the pulls accordingly. A pullup (47kΩ) is recommended on the processor UART transmit signals (UARTn_TXD [n = 0-6] and WKUP_UART0_TXD) in case the processor or the attached device outputs can float.

One of the common error observed when UART interface is used is UART interface signals polarity being reversed. The recommendation is to connect the signals as below:

- TX to RX
- RX to TX

The recommendation is to verify the signal naming on the attached device side and make the required connections accordingly.

The recommendation is to verify the connections, IO level and matching of polarity when additional UART interface flow control signals are used.

When external UART interface signals are connected directly to the processor UART interface, the recommendation is to verify IO level compatibility and fail-safe operation. The recommendation is to provide provision for external ESD protection.

The recommendation is to provision for connecting UART boot (UART0) for early board builds for board bring-up and debug.

7.4.3.1 UART Interface Connection When Not Used

When UART interfaces are not implemented on the custom board design, the recommendation is to provide provision for connecting external UART interface signals for debug. The recommendation is to follow the below priority for provisioning the UART interface signals:

- UART0
- WKUP_UART0

The recommendation is to add TPs on the processor board for connecting external inputs. The recommendation is to provide parallel pulls (10kΩ or 47kΩ) for the IOs that can float (to prevent the attached device inputs from floating until driven by the host). Provision for adding external ESD protection is recommended and can be populated when the UART interface is used.

The UART interface signals are not fail-safe. No external inputs (UART interface signals) is recommended to be applied before the processor supplies ramp.

7.4.3.2 Universal Asynchronous Receiver/Transmitter (UART) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Connection of UART interface signals including polarity
3. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
4. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of TX->RX, Dout to Din or similar connections)
5. Verify the IO voltage level connected based on the buffer type implemented for the IOs used to configure the interface
6. Provision for series resistors for UART interface signals added near to the source for isolation or control of possible signal reflections.
7. Parallel pull provision added for the processor or attached device IOs that can float (data, direction control)
8. Required communication speed (Baud rate) versus supported speed (baud rates)
9. Required communication errors (%) versus calculated communication errors (%) due to internal clock divider mismatch.
10. Connection of processor IO supply for IO group and the attached device IO supply (connected to the same supply source)
11. Fail-safe operation of UART interface signals.
12. External ESD protection when the interface signals are connected directly to external inputs directly
13. Addition of required bulk and high frequency capacitors, and value

Schematic Review

Follow the below list for the custom schematic design:

1. Provision for series resistors (0Ω) near to source added for the interface signals to control of possible signal reflections or isolate for testing
2. Parallel pull (10kΩ or 47kΩ) provided for the interface signals that can float (to prevent the attached device inputs from floating until driven by the host)
3. Pullup referenced to (powered by) the processor VDDSHVx or VDDSx or VDDS_WKUP or VDDS_RTC for corresponding UART instance and signals matches
4. Interface signals (data, direction control) connections including signal polarity matching
5. Supply rails connected to the IO supply for IO group VDDSHVx or VDDSx or VDDS_WKUP or VDDS_RTC referenced to (powered by) UART peripherals and attached devices IO supply are connected to the same power source and follow the ROC
6. Provision for parallel pull added for any of the processor or attached device IOs that can float
7. UART interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps

Additional

1. The recommendation is to verify fail-safe operation when external interface signals are connected directly and are sourced from a different supply with respect to the processor dual-voltage IO supply for IO group.
2. Applying an external input signal to the processor UART inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.
3. The recommendation is to provision for external ESD protection for the interface signals when external inputs are connected directly.
4. In case UART interfaces are not used, the recommendation is to provide provision for connecting the UART0 or WKUP_UART0 for debug.

7.4.4 Modular Controller Area Network (MCAN) with Full CAN-FD Support

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Note

The processor peripherals (MCAN, MCSPI, MCASP, I2C) implements connecting the signal with same function on multiple pins and the signals are grouped as IOSET. The recommendation is to verify and use the correct IOSET (grouped signals) in the custom board design. Timing closure for the interface is based the IOSET.

The processor family supports x3 (three) (x3 MAIN domain) instances of Modular Controller Area Network (MCAN) with Full CAN-FD support.

The MCAN module supports both classic CAN and CAN-FD (CAN with Flexible Data-Rate) specifications.

The MCAN interface, interfaces to the attached device supporting MCAN interface through external MCAN transceiver.

In case an external transceiver is used, the recommendation is to match the external interface signal IO levels with the IO supply for IO group voltage level. The recommendation is to power the IO supply of the transceiver and the processor IO supply rail from the same source.

The recommendation is to provision for series resistors (0Ω) on the interface signals, close to source, for isolation (debug) or control possible signal reflections. Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pullup (47kΩ) is recommended on the processor MCAN transmit (receive) signals in case the processor or the attached device outputs can float.

The recommendation is to provide the recommended terminations for the MCAN transceiver external interface inputs.

7.4.4.1 Modular Controller Area Network Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Connection of MCAN interface signals including polarity
3. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
4. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of TX->RX, Dout to Din or similar connections)
5. Verify the IO voltage level connected based on the buffer type implemented for the IOs used to configure the interface
6. Provision for series resistors added for all the MCAN interface signals and placed near to the source for isolation or control of possible signal reflections (data).
7. Provision for parallel pull added for the processor or attached device inputs that can float
8. Connection of processor IO supply for IO group and attached device IO supply (connected to the same supply source)
9. Fail-safe operation of MCAN interface signals
10. Addition of required bulk and high frequency capacitors, and value

Schematic Review

Follow the below list for the custom schematic design:

1. Series resistor value used (0Ω) and the placement (near to source)
2. Parallel pull value (10kΩ) added for any of the processor or attached device IOs that can float (to prevent the attached device inputs from floating until driven by the host)

3. Pullup referenced to (powered by) the processor VDDSHVx for corresponding MCAN instance and pins matches
4. Supply rails connected to the dual-voltage IO supply for IO group VDDSHVx referenced to (powered by) MCAN peripherals and attached devices IO supply are connected to the same power source and follow the ROC
5. Provision for parallel pull added for any of the processor or attached device IOs that can float
6. MCAN interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps

Additional

1. Processor IOs are not fail-safe. No external input is recommended to be applied before the processor supply ramps. The recommendation is to verify fail-safe operation when connected to external interface signals. Applying an external input signal to the processor MCAN inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.
2. External ESD protection when the interface signals are connected directly to external inputs

7.5 On-board Synchronous Communication Interface (MCSPI, MCASP and I2C)

7.5.1 Multichannel Serial Peripheral Interface (MCSPI) and Audio Peripheral - Multichannel Audio Serial Port (MCASP)

Note

The processor peripherals (MCAN, MCSPI, MCASP, I2C) implements connecting the signal with same function on multiple pins and the signals are grouped as IOSET. The recommendation is to verify and use the correct IOSET (grouped signals) in the custom board design. Timing closure for the interface is based the IOSET.

Multichannel Serial Peripheral Interface (MCSPI):

Figure 7-10 includes illustration for MCSPI interface including series resistor placed near to the processor clock output pin and pulldown placed near to the attached device, pullup for /CS near to the attached device and optional pull for the data interface signals (IOs) that can float.

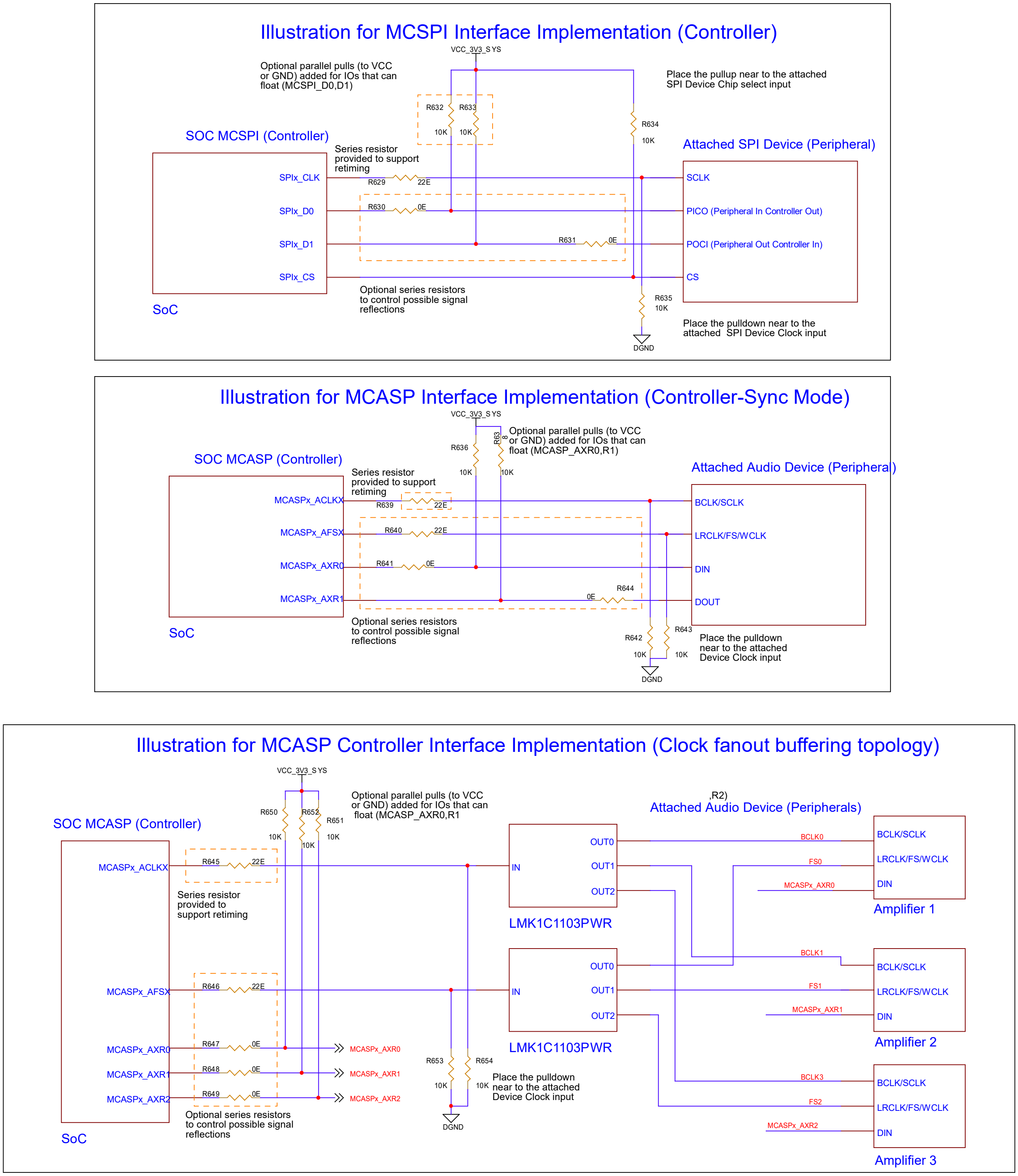


Figure 7-10. SPI Interface Illustration (Generic)

The processor family supports x4 (four) (x4 MAIN domain) instances of MCSPI. The MCSPI module is a multichannel transmit/receive, synchronous serial bus and can operate in controller mode or peripheral mode. In controller mode, the processor SPI interface sources the clock to the attached device. In peripheral mode, the attached device is required to source the SPI clock to processor.

A series resistor 22Ω is recommended (as a starting point) for the MCSPI clock output signals. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown (10kΩ) is recommended close to the attached device clock input pin. A pullup (10kΩ) is recommended for the chip select (CS) pin close to the attached device.

The MCSPI peripheral does not support boot. The OSPI0 interface supports SPI boot.

For the MCSPI interface SPIx_D0 and SPIx_D1 are the data lines. The data lines support programming the signals either to transmit data (transmission, output) or receive data (reception, input).

Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A parallel pull (10kΩ or 47kΩ) is recommended for the processor or attached device data lines that can float (to prevent the attached device inputs from floating until driven by the host).

The recommendation is to connect the SPI interface to x1 (single) memory device. When connecting to multiple memory devices, the recommendation is to follow high-speed design practices and perform simulations to make sure the layout is not going to generate non-monotonic clock transitions when the single clock source is connected to multiple SPI attached devices.

See the following FAQs:

[FAQ] SK-AM64B: MCSPI Integration Guide

[FAQ] AM6412: AM64x SPI D0 and D1 - MISO/MOSI

The FAQ is generic and can also be used for AM62Lx processor family.

Audio Peripheral - Multichannel Audio Serial Port (MCASP):

Figure 7-11 includes illustration for MCASP interface including the series resistor near to the processor clock output pin and pulldown near to the attached device, and optional pulls for the data interface signals (IOs) that can float.

The figure additionally illustrates buffering of bit clock and word clock when connected to multiple attached devices (speaker or amplifier).

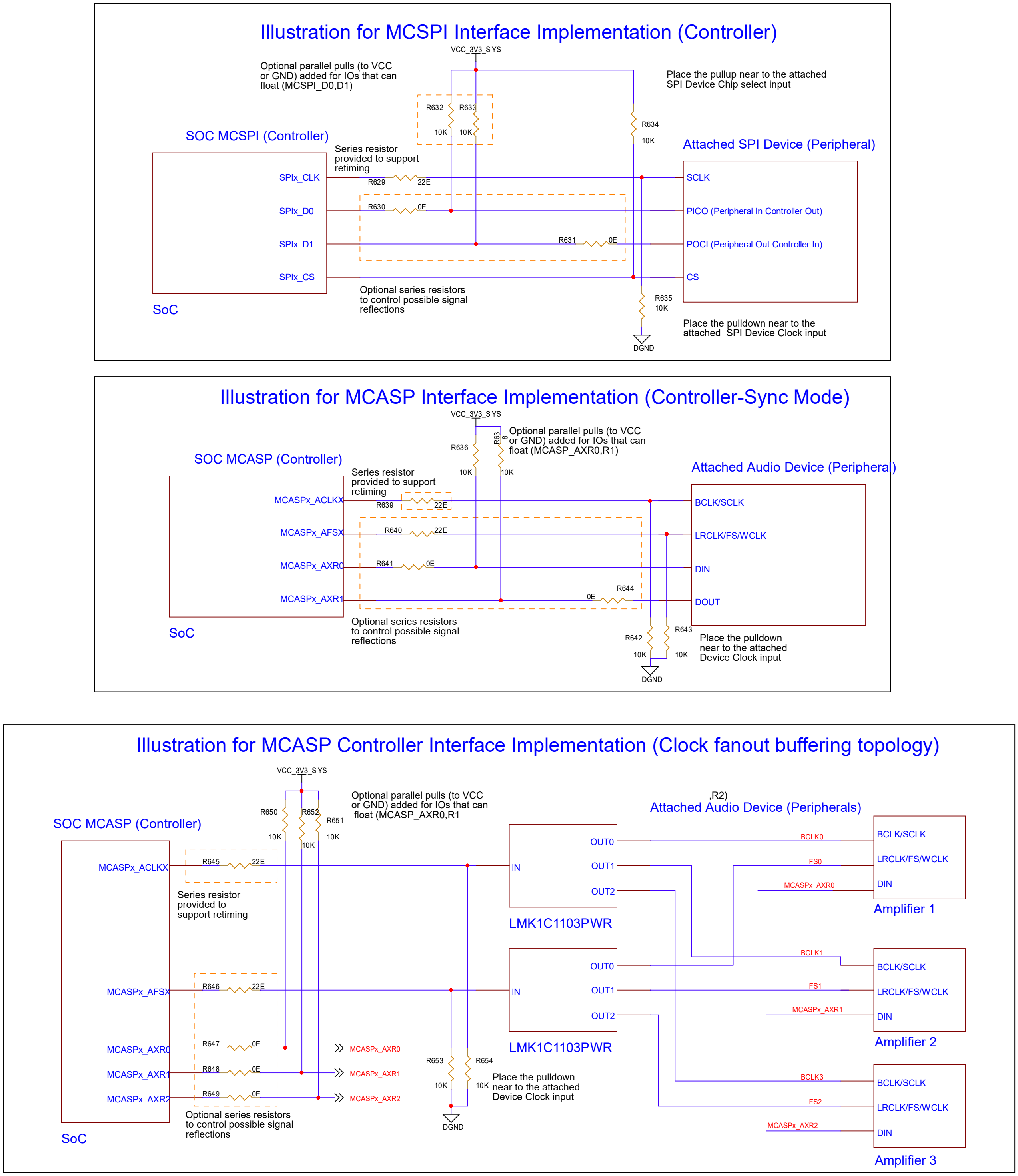


Figure 7-11. MCASPI Interface Illustration (Generic)

The processor family supports x3 (three) (x3 MAIN Domain) instances of Audio peripheral - Multichannel Audio Serial Port (MCASP). MCASP supports up to 4/6/16 Serial Data Pins (serializer) across x3 MCASP with Independent TX and RX Clocks. MCASP supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and similar formats. A series resistor 22Ω is recommended (as a starting point) for the MCASP clock output. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown (10kΩ) is recommended close to the attached device clock input pin.

Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A parallel pull (47kΩ) is recommended for the processor or attached device data lines that can float (to prevent the attached device inputs from floating until driven by the host).

The MCASP functions as a general-purpose audio serial port and are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L Design Recommendations / Custom board hardware design - Queries related to MCASP

7.5.1.1 Connection of MCSPI and MCASP Interface Signals

For the MCSPI interface, the recommendation is to provide series resistors (22Ω) for SPI clock output signals SPI0..3_CLK (MCSPI 0..3) close to processors clock output pin (processor MCSPI is configured as controller) since the clock output is used for retiming.

The recommendation is to provide provision for series resistor (0Ω or 22Ω) for receiver clock (Receive Bit Clock) output signals MCASP0..2_ACLKR and Receive Frame Sync signals MCASP0..2_AFSR (close to attached device). Provision for parallel pull is recommended for processor IOs that can float

For the data interface signals a parallel pull is recommended for processor or attached device IOs that can float. A series resistor provision near to the source for control of possible signal reflection is recommended.

The recommendation is to provide provision for series resistor (0Ω or 22Ω) for receiver clock (Receive Bit Clock) output signals MCASP0..2_ACLKR and Receive Frame Sync signals MCASP0..2_AFSR (close to attached device).

For the data interface signals a parallel pull is recommended for processor or attached device IOs that can float.

A series resistor provision near to the source for control of possible signal reflection is recommended.

The recommendation is to provide provision for series resistor (0Ω or 22Ω) for receiver clock (Receive Bit Clock) output signals MCASP0..2_ACLKR and Receive Frame Sync signals MCASP0..2_AFSR (close to attached device).

For a number of processor IOs (LVCMOS or SDIO), the IO buffers TX (Output) and RX (Input) are off and internal pulls (pullup and pulldown) are turned off during reset and after reset. The recommendation is to verify if external pullups (10kΩ) are provided for SPI Chip Select SPI0..3_CS0..3 (MCSPI 0..3) (close to attached device). The recommendation is to add pulls (10kΩ or 47kΩ) to the processor and the attached device signals (data interface - data in, data out) that can float (to hold the attached device inputs in a known state until driven by the host).

Two (x2) or more attached devices (common clock connection (BCLK, frame sync), different data signals connection, working simultaneously) are allowed to be connected to MCASP interface. The MCASP can be configured to have the transmit and receive sections operate synchronously to the transmit section clock and transmit frame sync signals. The BCLK and frame sync need to be the same for all target devices if using dedicated serializers, not an issue if using TDM. During custom board design, the potential of signal quality/ signal reflections (signal reflections caused by driving multiple inputs from a single MCASP clock output) is something to be considered. Buffering the BCLK and frame sync is one of the approach that can be followed.

Follow the below application note for connecting the MCASP signals:

McASP Design Guide - Tips, Tricks, and Practical Examples

7.5.1.2 MCSPI Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Timing and switching characteristics, and any additional information available.
3. Verify the IO voltage level connected based on the buffer type implemented for the IOs used to configure the interface
4. MCSPI Interface configuration and signal connections
5. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
6. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of TX->RX, Dout to Din or similar connections)
7. Series resistor 22R provision for processor MCSPI interface clock output signal placed near to the processor pin including value and placement
8. Connection of pulldown for clock output signal near to the attached device input
9. Optional series resistors provision for the MCSPI data interface signals placed near to the source
10. External SPI interface attached device Chip Select connection including pullup
11. Configuration of MCSPI data interface signals for DIN and DOUT functionality
12. Connection of parallel pulls for data interface signals (processor or attached device inputs, that can float)
13. Connection of IO supply for IO group and attached device IO supply (connected to the same supply source)
14. Interface performance and signal integrity related concerns when connected to >x1 attached devices
15. Fail-safe operation of interface signals
16. Addition of required bulk and high frequency capacitors, and value

Schematic Review

Follow the below list for the custom schematic design:

1. Interface configuration and recommended connections (including following the IOSET for configuring (grouping) the signals)
2. Series resistor 22Ω added to the clock output signal near to processor clock output pin (used for retiming)
3. Provision for series resistors added (0Ω) for the interface signals (to isolate for testing or for control possible signal reflections)
4. Pullup referenced to (powered by) the processor VDDSHVx or VDDSx for corresponding MCSPI instance and signals
5. Processor VDDSHVx or VDDSx and the attached device IO supply are sourced from the same supply
6. Supply rails connected to the IO supply for IO group VDDSHVx or VDDSx referenced to (powered by) MCSPI peripherals and attached devices IO supply follow the ROC
7. Pulldown (10kΩ) provision for MCSPI clock (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) for all IOs configured for MCSPI interfaces
8. Provide provision for external pullups for SPI Chip Select SPI0..3_CS0..3 (MCSPI 0..3) (close to attached device). The recommendation is to add pulls to the processor and the attached device signals (data interface - data in, data out) that can float (to prevent the attached device inputs from floating until driven by the host). Pullup values (10kΩ or 47kΩ) can be used.
9. Configuration of processor SPIx data bits D0 and D1 bits (data direction) matches the attached device and required pulls are added for signals that can float
10. Parallel pull added for the processor or attached IOs that can float
11. Interface performance (speed, data throughput, communication errors) and signal integrity related concerns have been analyzed (simulated) when connecting to multiple attached devices
12. MCSPI interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps

Additional

1. The recommendation is to verify fail-safe operation when processor IOs are directly connected to external interface signals or connector (through carrier board or add-on board). Applying an external input signal to the processor MCSPI inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.

2. External ESD protection when the interface signals are connected directly to external inputs.

7.5.1.3 MCASP Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Timing and switching characteristics, and any additional information available.
3. Verify the IO voltage level connected based on the buffer type implemented for the IOs used to configure the interface
4. MCASP interface configuration and signal connections.
5. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
6. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of TX->RX, Dout to Din or similar connections)
7. Series resistor provision for processor clock output signal placed near to the processor pin including value and placement
8. Connection of pulldown for clock output signal near to the attached device input
9. Optional series resistors provision for the MCASP interface signals placed near to the source.
10. Connection of parallel pulls for data interface signals (processor or attached device inputs, that can float)
11. Connection of IO supply for IO group and attached device IO supply (connected to the same supply source)
12. Interface performance (speed, data throughput, communication errors) and signal integrity related concerns.
13. Connection of MCASP signals when connected to multiple attached devices.
14. Clock output buffering when connected to multiple devices
15. Fail-safe operation of MCASP interface.
16. Addition of required bulk and high frequency capacitors, and value

Schematic Review

Follow the below list for the custom schematic design:

1. MCASP interface configuration and recommended connections (including following the IOSET for configuring (grouping) the signals)
2. Series resistor (22Ω) added to the clock output signal (transmit bit clock) near to the processor clock output pin (used for retiming) and provision for series resistor 0Ω or 22Ω for transmit frame sync signal near to the processor clock output pin for control of possible signal reflections
3. Provision for series resistors added (0Ω optional) for the interface signals (to isolate for testing or for control of possible signal reflections)
4. Pulldown (10kΩ) provision for the MCASP clock (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) for all IOs configured for MCASP interfaces
5. Supply rails connected to the IO supply for IO group VDDSHVx or VDDSx referenced to (powered by) MCASP peripherals and attached devices IO supply are sourced from the same supply and follow the ROC
6. Pullup referenced to (powered by) the processor VDDSHVx or VDDSx for corresponding MCASP instance and signals
7. Provide provision for external pullups for MCASP interface (Transmit or Receive) close to attached devices. The recommendation is to add pulls to the processor and the attached device signals (data interface - data in, data out) that can float (to prevent the attached device inputs from floating until driven by the host). Pullup values used (10kΩ or 47kΩ)
8. Interface performance (speed, data throughput, communication errors) and signal integrity related concerns have been analyzed (simulated) when connecting to multiple attached devices
9. Connection of MCASP signals when connected to multiple attached devices. Follow general design guidelines to minimize stubs
10. Parallel pull added for the processor or attached device IOs that can float

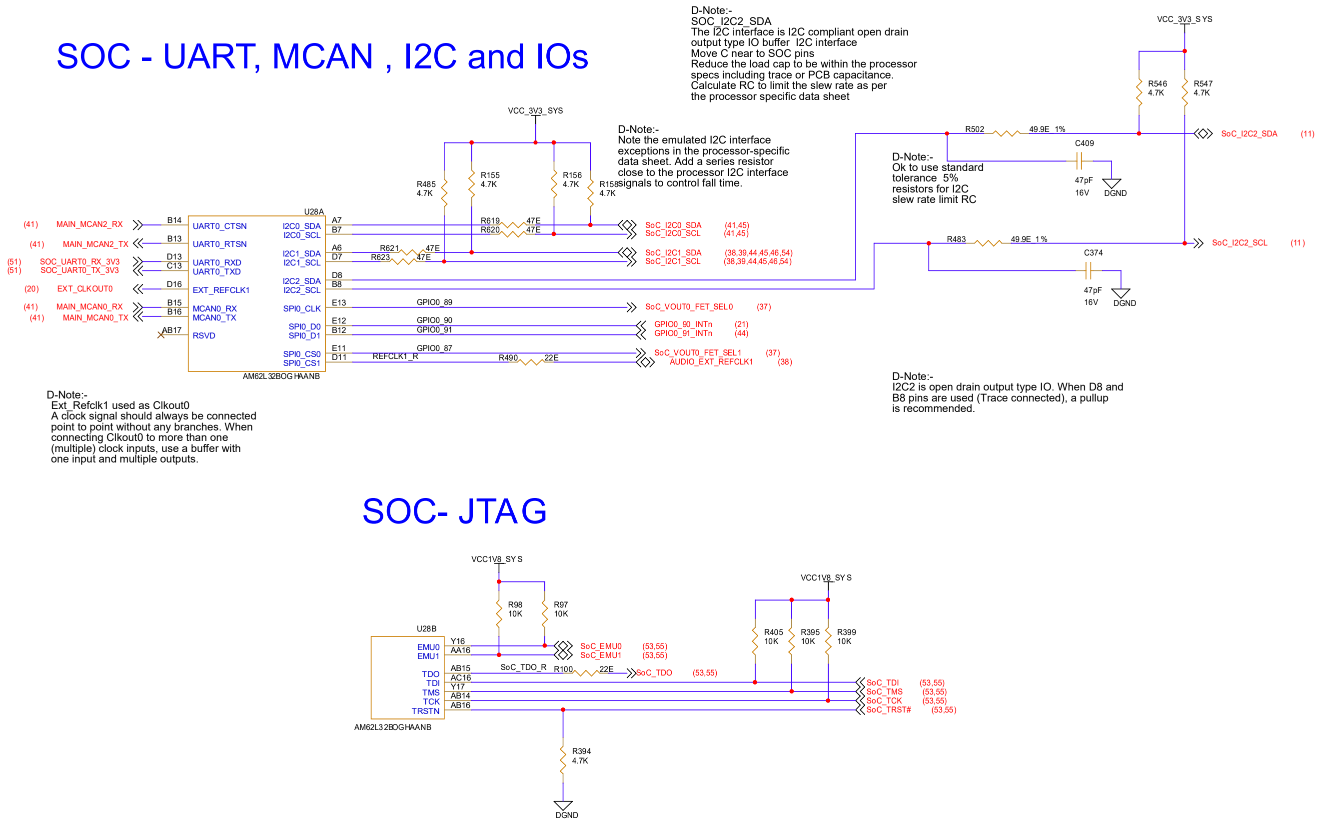
11. MCASP interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps

Additional

1. The recommendation is to verify fail-safe operation when connected to external signals. Applying an external input signal to the processor MCASP inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.
2. Connecting Two (x2) or more devices (common clock connection, different data signals connection, working simultaneously) to MCASP interface is supported. The recommendation is to follow good or recommended layout practices when routing the bit clock (transmit bit clock and receive bit clock). Perform simulations using IBIS model. The x2 devices (Example: Codec and amplifier) are recommended to be running with the same format (TDM/I2S/etc) and Codec and amplifier are recommended to be running with the same format (TDM/I2S/etc) and word size setup are synchronized with the bit clock and frame Sync.
3. External ESD protection when the interface signals are connected directly to external inputs.

7.5.2 Inter-Integrated Circuit (I2C)

Figure 7-12 includes I2C interface connections for open-drain output type buffer (I2C2) and emulated open-drain output type buffer (I2C0, I2C1) I2C interfaces. An RC is added for open-drain I2C interface when pulled to 3.3V for slew rate limit. A series resistor is added on the emulated open-drain I2C interface signals for control of fall time.



D-Note:-
SOC_I2C2_SDA
The I2C interface is I2C compliant open drain
output type IO buffer I2C interface
Move C near to SOC pins
Reduce the load cap to be within the processor
specs including trace or PCB capacitance.
Calculate RC to limit the slew rate as per
the processor specific data sheet

D-Note:-
Note the emulated I2C interface
exceptions in the processor-specific
data sheet. Add a series resistor
close to the processor I2C interface
signals to control fall time.

D-Note:-
Ok to use standard
tolerance 5%
resistors for I2C
slew rate limit RC

D-Note:-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected
point to point without any branches. When
connecting Clkout0 to more than one
(multiple) clock inputs, use a buffer with
one input and multiple outputs.

D-Note:-
I2C2 is open drain output type IO. When D8 and
B8 pins are used (Trace connected), a pullup
is recommended.

Figure 7-12. Open-Drain or Emulated Open-Drain

Note

The processor peripherals (MCAN, MCSPI, MCASP, I2C) implements connecting the signal with same function on multiple pins and the signals are grouped as IOSET. The recommendation is to verify and use the correct IOSET (grouped signals) in the custom board design. Timing closure for the interface is based the IOSET.

The processor family supports x5 (five) (x1 (single) I2C compliant, fail-safe open-drain output type IO buffer and x4 (four) LVCMOS buffer type IO based emulated) I2C interfaces. The supported I2C interfaces include x4 MAIN domain, x1 WKUP domain I2C interfaces.

The recommendation is to verify if the application requires an I2C interface that is fully compliant to I2C-bus specification. I2C2 (only when using processor pins with *I2C OD FS* buffer type. For example, B8, D8 for ANB package) are fail-safe, true open-drain output type buffers, and are fully compliant to the I2C specifications. Open-Drain output buffer type I2C interface can support HS-mode (up to 3.4Mbps) operations when the IO buffers (interface) are operating at 1.8V.

Note

For I2C interface with open-drain output type buffer (I2C2), an external pull is recommended, when the IOs are used (for I2C interface or configured for alternate function as an IO). I2C interface signals with open-drain output type buffer (I2C2) can be left open when not used (trace is not connected).

Pullups (4.7kΩ, adjust after testing) are recommended for LVCMOS IOs when configured for I2C functionality. The recommendation is to connect the pullups with the shortest possible stub.

When the open-drain output type buffer I2C interface is pulled to 3.3V supply, the IOs have slew rate requirements specified. An RC is recommended to limit the slew rate. For RC implementation (C near to processor pins), refer to the EVM schematic.

For more information, see the *Connection of Supply Rails to External Pullups* section.

In the case that additional I2C interfaces are required, use emulated open-drain output type I2C interfaces I2C0, I2C1, I2C3, WKUP_I2C0, and I2C2 (except when using the processor pins with *I2C OD FS* buffer type). Emulated open-drain output I2C interfaces are not fully compliant with the I2C specification, in particular falling edges are fast (< 2ns).

The recommendation is to verify the *Exceptions* in the *Timing and Switching Characteristics*, *I2C* section of the processor-specific data sheet. Take note of the exceptions for the emulated open-drain output type buffer I2C interface. Any attached device connected to emulated open-drain type buffer (LVCMOS) I2C interface needs to function properly with the faster fall time. Emulated open-drain output type buffer I2C interface supports 100kHz and 400kHz operation. Pullups are recommended when the IOs are configured for I2C interface. Connect the pullups with the shortest possible stub. The recommendation is to use series resistor (47Ω, adjust after testing) to control the fall time. The value depends on the custom board design and is recommended to be finalized during testing.

For more information, refer to the FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design – I2C interface

In case the plan is to use TI provided software, connect the recommended processor I2C interface to the PMIC, as WKUP_I2C0 is the interface used for PMIC control.

Note

Refer to the *Signal Description* section of the processor-specific data sheet. When I2C2 (supports I2C OD FS or LVCMOS buffer type) and I2C3 interfaces are used, refer to the note (can be multiplexed to more than one pin) in the *Timing and Switching Characteristics*, *Peripherals*, *I2C* section of the processor-specific data sheet.

Note

The recommendation is to verify the *Exceptions* in the *Timing and Switching Characteristics*, *I2C* section of the processor-specific data sheet during the custom board design. Take note of the exceptions for the emulated open-drain output type buffer I2C interface. **The recommendation is to add a series resistor (47Ω, adjust after testing) to control the fall time**.

7.5.2.1 I2C (Open-drain Output Type IO Buffer) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Timing and switching characteristics, and any additional information available.
3. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
4. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of Data, Clock or similar connections)
5. Open-Drain output buffer type I2C interface instance (I2C2, can be configured to use LVCMOS buffer type) supported and connection to multiple attached devices.
6. Open-Drain output buffer type I2C interface configuration, I2C interface pullup requirements and connection recommendations.
7. Slew rate requirements and connection of RC (C near to processor pin) for slew rate control when pulled to 3.3V supply.
8. Connection of attached device address inputs
9. Open-drain output type buffer I2C interface Fail-safe operation support
10. Addition of required bulk and high frequency capacitors, and value
11. Open-drain output type I2C interface connection recommendations when interface is not used.
12. Voltage connection of the pullup to support Hs-mode (up to 3.4Mbps is supported when pulled to 1.8V)

Schematic Review

Follow the below list for the custom schematic design:

1. I2C2 (only when using processor pins with "I2C OD FS" Buffer Type. Example: B8, D8 for ANB package) controllers have dedicated I2C compliant open-drain output type buffers.
2. A pullup is required only when the IO is used as I2C interface or IO interface. I2C interface signals can be left unconnected when IO is not used.
3. The recommendation is to verify the pullup values used for the I2C interface with the EVM schematic implementation or calculate the pullup value based on the load. A pullup (4.7kΩ, adjust after testing) is recommended for the I2C interfaces.
4. The I2C pullup supply voltage connected follows the steady-state maximum voltage specified for fail-safe IOs. The supply threshold depends on the supply voltage connected to IO supply for IO group.
5. RC for open-drain output type IO buffer for limiting the input slew rate when interface operates (pulled) at 3.3V. Capacitor connected near to the processor I2C interface pins when RC for input slew rate control is implemented. Verify the effect of RC on the I2C interface speed and adjust the RC as required.
6. Supply rails connected to the IO supply for IO group VDDSHVx or VDDSx referenced to (powered by) I2C peripherals and attached devices IO supply are sourced from the same supply and follow ROC.
7. Attached device address inputs connected to IO supply through a resistor (> 1kΩ).
8. Processor supports multiple I2C instances. The recommendation is to verify that there are no I2C address conflicts on any of the I2C interface. In case additional I2C interfaces are required, an I2C switch can be used.

Additional

1. The recommendation is to review the *Timing and switching characteristics*, *I2C Exceptions* section of the processor-specific data sheet during the design stage and include the required circuit.
2. The I2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I2C port.
3. The recommendation is to not place more than one set of pullup resistors on the I2C bus, the pullups can result in excessive loading and potential incorrect operation. Adjust the pullup value based on the bus speed configured.
4. The recommendation is to make sure IO supply for IO group powering the processor I2C IOs matches the supply voltage used for the pullup and the attached I2C devices IO supply. Connecting the pullups to proper supply level can prevent incorrect I2C interface operation.
5. I2C interfaces support clock stretching. The recommendation is to adjust the pullup in case the measured clock frequency does not match the configured frequency due to the bus loading or signal slew rate.

7.5.2.2 I2C (Emulated Open-drain Output Type IO) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Timing and switching characteristics, and any additional information available.
3. Verify the IO voltage level connected based on the buffer type implemented for the IOs used to configure the interface
4. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).
5. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of Data, Clock or similar connections)
6. Emulated open-drain output type I2C interface instances (I2C0, I2C1, I2C2 (in case selected pins support LVCMOS buffer type), I2C3, WKUP_I2C) Supported and connection to multiple attached devices.
7. Supported IO supply level for the I2C interfaces (1.8V/3.3V or fixed 1.8V) vs Connected Voltage level
8. Emulated open-drain output buffer type I2C interface pin configuration, I2C interface pullup recommendations and connections.
9. Connection of attached device address inputs.
10. Emulated open-drain output type I2C interface exceptions and connection recommendations (series resistor) for fall time control
11. Emulated open-drain output type I2C interface fail-safe operation
12. Addition of required bulk and high frequency capacitors, and value
13. Emulated open-drain output type I2C interface connection recommendations when interface is not used.

Schematic Review

Follow the below list for the custom schematic design:

1. I2C interface configuration and recommended connections (including grouping of the interface signals as per IOSET). I2C interface type and pullup requirements.
2. A pullup (4.7kΩ) is recommended when IO is configured as I2C interface.
3. The recommendation is to verify the pullup values used for the I2C interfaces with the EVM schematic implementation or calculate the pullup value based on the load. A pullup (4.7kΩ, adjust after testing) is recommended for the I2C interfaces.
4. Pullup referenced to (powered by) the processor VDDSHVx or VDDSx (I2C pullup connected to correct voltage).
5. When I2C interface is not used, these IOs can be configured for alternate functions and the pulls are dependent on the IO function.
6. Supply rails connected to the IO supply for IO group VDDSHVx or VDDSx referenced to (powered by) I2C peripherals and attached devices IO supply are sourced from the same supply and follow the ROC.

7. Processor supports multiple I2C instances. The recommendation is to verify that there are no I2C address conflicts on any of the I2C interface. In case additional I2C interfaces are required, an I2C switch can be used.
8. Attached device address pin connected to IO supply through a resistor (> 1kΩ).
9. Note the I2C exceptions in the *Timing and Switching Characteristics* section of the processor-specific data sheet for emulated open-drain output type I2C interface. Series resistor (47Ω, adjust after testing) is recommended near to the processor I2C interface signals to control fall time.

Additional

1. LVCMOS type IO buffer to emulate an open-drain output type IO are not fully compliant with the I2C specification, in particular falling edges are fast (< 2ns).
2. The recommendation is to review the *Timing and switching characteristics*, *I2C Exceptions* section of the processor-specific data sheet during the design stage.
3. The I2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I2C port.
4. The recommendation is to not place more than one set of pullup resistors on the I2C bus, the pullups can result in excessive loading and potential incorrect operation. Adjust the pullup value based on the bus speed configured.
5. The recommendation is to make sure IO supply for IO group powering the processor I2C IOs matches the supply voltage used for the pullup and the attached I2C devices IO supply. Connecting the pullups to proper supply level can prevent incorrect I2C interface operation.
6. I2C interfaces support clock stretching. The recommendation is to adjust the pullup in case the measured clock frequency does not match the configured frequency due to the bus loading or signal slew rate.
7. Fail-safe interface support (emulated open-drain output type IOs are not fail-safe, no external input is recommended to be applied recommended to be applied before the processor IO supply ramps). The recommendation is to verify fail-safe operation when connected to external interface signals. Applying an external input signal to the processor I2C inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.

7.6 User Interface (DPI, DSI), GPIO and Hardware Diagnostics

7.6.1 Display Subsystem (DSS)

Note

The processor family supports pinouts (pin attributes defined) for DPI and DSI interfaces. The processor (internal hardware) supports configuring (using) either MIPI DSI (x4 lanes D-PHY (DPHY)) or DPI (24-bit RGB LVCMOS) display (external). The selection of the processor display interface is required to be done at boot time.

For information related to DPI interface including mapping of the DPI interface signals and MIPI DSI interface, Refer to *Display Subsystem and Peripherals* section of processor-specific TRM.

7.6.1.1 Display Parallel Interface (DPI)

Refer to processor-specific data sheet and TRM for information related to supported data formats including BT656.

7.6.1.1.1 AM62Lx Processor Family

The processor family supports x1 24-bit per pixel, RGB/YUV422 modes, LVCMOS output, DPI (parallel) display interface instance.

For information related to Spread Spectrum Clocking support for DPI, refer *AM62x, AM62Ax, AM62Px, AM62Lx Spread-Spectrum Clocking* application note.

For more information on DPI, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB- display interface

The FAQ is generic and can also be used for AM62Lx processor family.

7.6.1.1.1.1 IO Power Supply

The processor DPI interface is powered by VDDSHV0 supply rail (IO supply for GPMC IO group).

7.6.1.1.1.2 Connection

Verifying display (RGB) connections.

DPI display interface support includes 12-, 16-, 18-, and 24-bit RGB active matrix displays. When connecting 16-bit data to an 18-bit panel (BGR565 to BGR666), the recommendations is to connect D0-D4 to B1-B5 of the LCD module input, D5-D10 to G0-G5 of the LCD module input, and D11-D15 to R1-R5 of the LCD module input connector. For the 18-bit interface, on the LCD module input side, the recommendations is to connect B0 to B5, R0 to R5, and R0 to R5.

7.6.1.1.1.3 DPI (Attached Device) Reset

The recommendation is to implement the attached device reset (LCD module) using a 2-input ANDing logic since the ANDing logic provides the flexibility to be able to reset the attached device in all processor reset condition including local reset (in use cases where the attached device becomes non-responsive and needs to be reset without a power cycle). Processor GPIO (used for LCD module local reset) is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (pullup enabled) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (connected) to reset the DPI (attached device), the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. In case the resistor divider value is too high the rise/fall time of the processor IO connected to DPI reset input can be slow and introduce delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

7.6.1.1.1.4 DPI Signals Connection

The recommendation is to provide provision for connecting a series resistor (0Ω) for VOUT0_PCLK (Pixel Clock Output) (close to processor clock output pin for control of possible signal reflections). In case space is not a constraint, the recommendation is to add series resistors (0Ω) for all other control and data signals near to the processor pins.

7.6.1.1.1.5 Capacitors for the Power Supply Rail

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant EVM implementation) bulk and decoupling capacitors have been provided for VDDSHV0 (supply rail referenced to (powered by) DPI interface signals) supply rail and the attached device.

The recommendation is to follow the processor-specific EVM implementation when recommendations are not available.

7.6.1.1.1.6 DPI (VOUT0) Peripheral Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Mapping and connection of the processor DPI signals to the attached device
3. Mapping of processor pin (ball number) to the required functionality (peripheral, signal name) on custom board (selected pin supports muxing (multiplex) the IO for the required function) and naming of the signal as per the processor data-sheet pin attributes signal name column (when using standard peripherals).

4. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of RGB signals (D0-D7), Clock, Control or similar connections)
5. Addition of series resistor for the processor pixel clock output signal near to processor pin
6. Addition of series resistor for DPI display interface control and data interface signals near to processor pins
7. Implementation of attached device reset logic
8. Provision for External ESD protection
9. Addition of required bulk and high frequency capacitors, and value for the attached device

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the interface signals including mapping of DPI pins of the processor with the attached device (RGB display) and display control signal.
2. Supply rails connected to the IO supply for IO group VDDSHV0 referenced to DPI peripheral and attached device IO supply follow the ROC.
3. The recommendation is to compare the decoupling capacitor of DPI IO supply with relevant EVM.
4. Connection of series resistor (0Ω) for the clock output signal near to the processor clock output pin PCLK (for control of possible signal reflections).
5. Series resistors for the display interface DPI control and data interface signals is optional. Adding the series resistors is recommended when space is not a constraint.
6. The recommendation is to implement the attached device (LCD module) reset using a 2-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup or pulldown (pullup enabled) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).
7. The recommendation is to provision for external ESD protection (based on the use case).

7.6.1.2 Display Serial Interface (DSI)

7.6.1.2.1 AM62Lx Processor Family

The processor family supports display interface with x4 (four) data lanes and x1 (single) clock lane.

Refer processor-specific data sheet for supported display resolution.

7.6.1.2.1.1 DSITX0 Peripheral Used

The processor DSITX0 interface is referenced to (powered by) VDDA_CORE_DSI and VDDA_CORE_DSI_CLK and DSITX0 1.8V analog supply VDDA_1P8_DSI..

The recommendation is to connect a parallel resistor between DSI0_TXRCALIB (close to processor) and VSS. Refer processor-specific data sheet for recommended resistor value and tolerance.

The recommendation is to follow the DPI0 attached device reset implementation in case the attached device is required to be reset.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.6.1.2.1.1.1 DSITX0 Peripheral Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of the DSITX0 interface signals to the attached device.
3. Matching of the polarity of the peripheral data interface signals between the processor and the attached device (Example Mapping of DSI0 clock, data or similar connections)

4. Connection of recommended external calibration resistor DSI0_TXRCALIB.
5. Connection of DSITX0 core, DSITX0 clock core, DSITX0 analog supplies
6. Addition of required bulk and high frequency capacitors, and value for the attached device
7. Implementation of attached device reset logic
8. Connection of DSITX0 interface signals when not used
9. Connection of the DSITX0 interface signals when partial lanes are not used
10. Connection of DSITX0 core, DSITX0 clock core, DSITX0 analog supplies when DSITX0 interface is not used and boundary scan is implemented
11. Connection of DSITX0 core, DSITX0 clock core, DSITX0 analog supplies when DSITX0 interface is not used and boundary scan is not implemented
12. Provision for external ESD protection

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the DSITX0 peripheral signals with attached devices including the polarity.
2. Connection of 499Ω ±1% to DSI0_TXRCALIB pin and ground.
3. Ferrite and capacitors used for DSITX0 analog and core supply, when DSITX0 peripheral is used. Follow EVM schematics.
4. Supply rails connected to the DSITX0 peripheral supply rail and attached device IO supply are sourced from the same supply follow the ROC.
5. Pin connectivity requirement followed when DSITX0 peripheral is not used and boundary scan functionality is required. IO calibration resistor can be DNI when DSITX0 interface is not used, but boundary scan functionality is required.
6. Pin connectivity requirement followed when DSITX0 peripheral is not used and boundary scan functionality is not required.

Additional

1. The recommendation is to provision for external ESD protection (based on the use case).
2. The recommendation is to include marking (optional) (100Ω) of differential signals and the differential impedance value.

7.6.1.2.1.2 DSITX0 Peripheral Connection When Not Used

DSITX0 peripheral when not used has specific connection requirements for interface signals and power supplies.

For connecting the DSITX0 peripheral signals, power supplies (core and analog), see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

When boundary scan function is used, DSITX0 supplies (VDDA_CORE_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_DSI) are recommended to be connected to the recommended supply rails. Decoupling capacitors on the supply pins are recommended. Bulk capacitors and ferrites are optional.

When boundary scan function is not used and DSITX0 interface is not used, the recommendations is to connect DSITX0 supplies (VDDA_CORE_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_DSI) to VSS through separate 0Ω resistors. Decoupling capacitors, bulk capacitors and ferrites are not recommended to be populated.

7.6.2 General Purpose Input/Output (GPIO)

Note

Read the note at the end of *Pin Connectivity Requirements* section of processor-specific data sheet for connecting processor IOs.

The processor family supports x1 general-purpose input/output GPIO module instances (GPIO0) in the MAIN domain and x1 GPIO module instance (WKUP_GPIO0) in Wakeup domain. The GPIO module supports signals (pins) that can be configured as either inputs or outputs. When configured as an output, software can write to internal registers to control the state driven on the output pins. When configured as an input, software can read the state of the input by reading the internal registers. In addition, the GPIO peripheral can generate host CPU interrupts and DMA synchronization events in different interrupt/event generation modes. The *Pin Attributes* and *Signal Descriptions* sections of the processor-specific data sheet provides information on the processor pins that can be configured as GPIOs (push-pull output type) supporting LVCMOS and SDIO IO buffer types. Other type of IOs supported by the processor are also described in the *Pin Attributes* section.

Refer below FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to GPIO

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Custom board hardware design – Queries related to LVCMOS input Hysteresis

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Data sheet Pin Attributes and Pin connectivity related queries

7.6.2.1 Availability of CLKOUT on Processor GPIO

Buffered output of WKUP_OSC0_XO can be configured on the WKUP_CLKOUT0.

7.6.2.2 GPIO Connection and Addition of External Buffer

The recommendation is to add a series resistor (with a value that is use case dependent and limits the current as per the processor-specific data sheet). When loads that draw (require) higher currents (above the processor-specific data sheet values) are connected to the processor GPIO, the recommendation is to buffer the processor IO before connecting to the load.

Common processor LVCMOS IO interface guidelines:

1. A number of the processor IOs are not fail-safe. No external input is recommended to be applied before the processor supply ramps
2. Processor LVCOMOS IOs have slew rate requirements specified, applying a slow ramp input or connecting a cap at the input is not recommended
3. Connecting a cap load >22pF at the LVCMOS IO output is not recommended. DNI the cap or perform simulations based on the use case.
4. Processor IO buffers (TX (output) and RX (input) and internal pulls (pullup and pulldown)) are turned off during Reset and after reset. A parallel pull is recommended near to the attached device being driven by the processor IO that can float (to prevent the attached device inputs from floating until driven by the host).
5. A parallel pull (47kΩ) is recommended for any processor IO (pad) that has a trace connected and not being drive actively). When adding parallel pull is not feasible, make sure the traces are routed away from noisy signals
6. Connecting processor IOs that can be configured for alternate function, directly to supply or ground is not allowed or recommended (including boot mode inputs). Custom board can have an configuration issue with the firmware and mis-configures these LVCMOS IOs that were intended to be inputs, to be outputs driven logic high instead.
7. Verify capacitor loading of the processor output (when any capacitor value >22pF (use case dependent, max value) is connected, recommendation is to simulate), slew rate of the input signal (LVCMOS input slew should be 1000ns or less)
8. The recommendation is to verify IO level compatibility between the processor IOs (inputs) and the attached device IOs (output)
9. Provide provision for external ESD protection when external IOs are connected directly to processor inputs
10. Make sure ST_EN bit in the PADCONFIG register is enabled for all the IOs
11. Make sure the pullup or pulldown value used for processor IOs are > 4.7kΩ
12. Make sure either pullup or pulldown is populated for processor IOs, When provision for pullup and pulldown is provided, place the resistors as tripad

7.6.2.3 Additional Information

Pins (or Pads) of unused IOs can be left unconnected, unless otherwise stated. A number of IOs have a *Pad Configuration Register* that provides configuration control over the capabilities of the IO (RXENABLE field in each conf_<module>_<pin> register). For more information, refer to the *Control Module* chapter of the processor-specific TRM. Software can disable the IO receive buffers (that is, RXENABLE=0) that are not used in the design, as part of early initialization. The recommendation is for the software to not unexpectedly enable the receiver of an IO (by setting the RXENABLE bit) when the associated pin is floating.

Note

For guidance on configuring unused pins (or peripherals), the recommendation is to refer to the *Pin Connectivity Requirements* section of the processor-specific data sheet.

Note

PADCONFIG register bit configuration - ST_EN:

The recommendation is to keep the ST_EN bit enabled in case the PADCONFIG register is modified by the software. The minimum *Input Slew Rate* parameter defined in each *Electrical Characteristics* table is associated with long-term reliability. The parameters are not a function of the ST_EN bit. The schmitt trigger function implemented in the input buffer only changes the output results of the input buffer, by filtering noise pulses that do not exceed the hysteresis. The schmitt trigger function does not change how the input buffer operates when a application applies a slew rate to the IO input that is slower than defined in the processor-specific data sheet.

Note

For guidance on configuring the IOs, refer to the *Pad Configuration Registers* section of the processor-specific TRM.

Note

Specific peripherals and GPIOs support debounce functionality. The recommendation is to review the notes related to debounce functionality for peripherals or GPIOs in the *Signal Descriptions* section of processor-specific data sheet.

For more information on connection of unused processor peripherals and IOs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC peripherals and IOs connection when not used

For information on connecting (used/unused) processor pins, and peripherals, see the following FAQ:

[FAQ] AM62x, AM62Ax, AM62D-Q1, AM62L, AM62Px, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals and add pullup or pulldown? (e.g. GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSx, ...)

Refer to the note at the end of *Connectivity Requirements* section of the processor-specific data sheet while using the processor GPIOs.

7.6.2.4 GPIO Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.

2. Connection of the supplies to IO pullup and IO supply for IO group (All IO pins referenced to (powered by) VDDSHVx, VDDSx, VDDS_WKUP, VDDS_RTC connect to same voltage level).Buffer type and supported voltage level (1.8V/3.3V or Fixed 1.8V)
3. Verify the IO voltage level connected based on the buffer type implemented for the IOs used to configure the interface
4. IO level compatibility with externally applied inputs.
5. Relevant PADCONFIG register configuration based on the required IO functionality
6. LVCMOS (SDIO) input slew rate as per processor-specific data sheet, connection of capacitor at the input or connection of capacitor at the output of processor IO.
7. Connection of processor IOs directly to supply or VSS
8. Connection of multiple IOs together directly
9. IO current sink or source follows the processor-specific data sheet recommendations.
10. One of the common use case for the IO interface is driving LEDs for indication. The recommendation for custom board designer is to review the LED source or sink current, effect on the processor IO voltage level, and adjust the current.
11. If continuous current draw is expected, the recommendation is to drive the LEDs using an external FET or Transistor based switch.
12. Fail-safe operation of LVCMOS (SDIO) IOs

Schematic Review

Follow the below list for the custom schematic design:

1. Each IO has an associated supply voltage used to power the IO cell (VDDSHVx, VDDSx or VDDS_WKUP or VDDS_RTC). VDDSx or VDDS_WKUP are recommended to be connected to 1.8V power source. In case VDDSHVx is sourced from 3.3V (1.8V) supply, all IO referenced to (powered by) VDDSHVx rails are recommended to be connected (operate) at 3.3V (1.8V) level.
2. The supply voltage for all pullups that are connected to processor IOs matches the voltage applied to the corresponding IO supply for IO group (VDDSHVx, VDDSx or VDDS_WKUP or VDDS_RTC). Pulling a signal to a different IO voltage can cause voltage leakage (residual voltage).
3. Supply rail connected to the GPIO group referenced to (powered by) the IO supply for IO group VDDSHVx, VDDSx, VDDS_WKUP, VDDS_RTC and the external inputs or GPIO pullup voltage level follow the ROC.
4. Directly connecting processor IOs to supply or VSS is not recommended or allowed, (including boot mode inputs). The custom board designer can have errors with the firmware and miss-configure the LVCMOS GPIOs that are intended as inputs, to be outputs driving logic high instead.
5. IO level compatibility for externally applied inputs from add-on or carrier board or external input is directly connected to the IOs through an external connector (provision for external ESD protection added).
6. External pulls are added for any of the processor (or attached device) IOs that can float (to prevent the attached device inputs from floating until driven by the host).
7. Input signal applied to the processor LVCMOS inputs follow the slew rate requirements as per processor-specific data sheet. Connecting a capacitor directly at the input can increase the signal slew and is not recommended.
8. Connection of capacitor load directly to the processor output for control or enabling of attached device is not allowed. Recommend simulation when capacitor load > 22pF (place holder) is used at the output of GPIO.
9. A number of processor IOs are not fail-safe. No external input voltage is allowed to be applied to the processor IOs before the IO supply for IO groups supply VDDSHVx, VDDS, VDDS_WKUP, VDDS_RTC ramps (excluding fail-safe IOs).
10. Shorting of multiple IOs together directly is not recommended. Connecting the IOs to supply or ground directly is not recommended.

Additional

1. Provision for external ESD protection for external input directly connected to the IOs.
2. Common processor LVCMOS IO interface guidelines, refer to *GPIO Connection and Addition of External Buffer* of user's guide. A number of processor IOs (LVCMOS, SDIO) are not fail-safe. No external input is recommended to be applied before the processor supply ramps.

3. Processor IOs have slew rate requirements specified. Applying a slow ramp input or connecting a capacitor directly at the input is not recommended.
4. Connecting a capacitor load > 22pF (place holder) at the output is not recommended. DNI capacitor or perform simulations (based on the use case).
5. Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pull is recommended for the attached device being driven by the processor IO that can float (to prevent the attached device inputs from floating until driven by the host).
6. A parallel pull (47kΩ) is recommended for any processor IO (pad) that has a trace connected and not being actively being driven. When adding a pull is not feasible, the recommendation is to route the traces away from noisy signals (Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pullup (47kΩ) is recommended near to the attached device, to hold the attached device inputs that can float in a known state).
7. Fail-safe operation when connected to external signals. Applying an external input signal to the processor GPIO inputs before processor supply ramps can causes voltage feed and affects the board performance.
8. External ESD protection provision is recommended when the IOs are connected directly to external interface signals.
9. Fail-safe IOs include PORz, I2C2 (only when using processor pins with I2C OD FS buffer type. For example, B8, D8 for ANB package), EXTINTn, and USBn_VBUS (n = 0-1), when the recommended VBUS voltage divider as per the processor-specific data sheet is used.

7.6.3 On-board Hardware Diagnostics

7.6.3.1 Internal Temperature Monitoring

The processor supports one VTM module, WKUP_VTM0 (supports single temperature sensor, temp0), which is located in the WKUP domain. The analog supply for sensor temp0 is provided by VDDA_PLL0 (PLL analog supply).

The VTM module supports voltage and thermal management by providing control of on-chip temperature sensor.

Temperature sensor is located at designated hotspot on the processor. The recommendation is to read the on-die temperature sensor in Linux and perform thermal management. See the *E2E thread*.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x (ALV, ALX) Custom board hardware design – Voltage and Thermal Manager (VTM)

7.6.3.1.1 Internal Temperature Monitoring Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Connection of the recommended supply to the temperature sensor temp0 supply pin
3. Addition of filter capacitor for temp0 sensor analog supply pin

7.7 Analog to Digital Converter (ADC)

The processor family supports x1 12-bit Analog-to-Digital Converter (ADC0), sampling rate up to 2MSPS, x4 (four) analog inputs (time-multiplexed).

For the allowed ADC0 input range and electrical characteristics, sampling rate see the *ADC Electrical Characteristics* section of processor-specific data sheet. ADC0_REFP and ADC0_REFN are directly connected to VDDA_ADC0 and VSS inside the processor.

7.7.1 ADC0 Connections When Used

The recommendation is to connect the ADC0 analog supply VDDA_ADC0 to the recommended power supply rail as per the processor-specific data sheet.

The recommendation is to follow the notes added at the end of the *Signal Descriptions, ADC, MAIN Domain* table of the processor-specific data sheet before using ADC0.

Note

ADC0 inputs are not fail-safe. Applying a voltage to any of the ADC0 inputs before the processor VDDA_ADC0 supply ramps is not recommended or allowed. The input applied (based on the input level) can cause residual voltage on the processor supply rail and can result in board start-up issues. Refer *Absolute Maximum Rating* table of processor-specific data sheet. In case supply rails that are available before the processor supply ramps are required to be monitored, the recommendation is to connected these inputs to ADC0 through a switch. The switch can be controlled by processor GPIO or power good signal from any of the supply source including PMIC.

7.7.2 ADC0 Connection When Not Used

When entire ADC0 is not used, there are specific connection requirements for the ADC0 inputs and ADC0 supply rail. When any of the ADC0 inputs are not used, there are specific connection requirements for the unused inputs.

For connecting the ADC0 inputs, analog supply pin, see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

When ADC0 is not used, the recommendation is to connect ADC0 inputs and processor analog supply pin to VSS through separate 0Ω resistors. The provision is for future expansion or enhancement and is optional.

7.7.3 ADC0 Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Selection of processor OPN supporting ADC functionality
3. Connection of ADC0 analog supply VDDA_ADC0 (ADC0_REFP and ADC0_REFN are directly connected to VDDA_ADC0 and VSS internally)
4. Connection of the analog inputs including input range and provision for filters
5. Filtering and decoupling capacitors for analog inputs and ADC0 supply
6. Connection of ADC0 inputs when partial or complete ADC0 is not used
7. Fail-safe operation of ADC inputs

Schematic Review

Follow the below list for the custom schematic design:

1. Review selection of processor part number that support ADC0 functionality
2. Connection of ADC0 analog supply as per processor-specific data sheet and follows the ROC. (ADC0_REFP and ADC0_REFN are directly connected to VDDA_ADC0 and VSS inside the processor)
3. The applied analog input voltage range is within the data sheet input voltage range specification
4. Connection of the required filters and decoupling capacitors (the recommendation is to follow the EVM implementation) for ADC0 supply and analog inputs
5. Refer to the pin connectivity requirements for connecting the ADC inputs when partial or complete ADC0 is not used

Additional

1. ADC0 inputs are not fail-safe. The recommendation is to not apply any input before the ADC0 supply ramps. When ADC0 inputs are available before the ADC0 supply ramps, connect the ADC0 inputs through a switch that is controlled by the processor supply or processor IO.

7.8 EVM Specific Circuit Implementation (Reuse)

In case some of the EVM implementation listed below are reused:

- DPI to HDMI
- AUDIO CODEC
- FT4232 UART TO USB BRIDGE
- XDS110 DEBUGGER
- CPSW3G RGMII or RMII – EPHY
- M.2 INTERFACE – SDIO
- CURRENT MONITORING DEVICES
- USB TYPE-C PD CONTROLLER AND POWER SUPPLY

The recommendation is to follow the below FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Guidelines for reuse of SK specific implementations listed below on custom board design

7.9 Performing Board Level Testing During Custom Board Bring-up

7.9.1 Processor Pin Configuration Using PinMux Tool

The recommendation is to verify the processor peripheral and IO configuration using the TI *SysConfig-PinMux* tool to take care valid IOSETs have been configured.

For more information, refer the following application note:

Accelerating Development with SysConfig using MCU+SDK

For more information, see the PinmuxConfigSummary.csv file provided by the SysConfig-PinMux tool.

7.9.2 Schematics Configurations

The recommendation is to verify the circuit options provided for alternate functionality or testing that are required to be DNI during normal functioning of the board (populating the components can affect or influence custom board performance) are marked as DNI in the custom board design and are not populated on the board before powering the board.

7.9.3 Connection of Supply Rails to External Pullups

Connecting processor IO pullup to a different IO supply rail/operating voltage (does not match the voltage level of IO supply for IO group referenced by the IO group) can cause voltage leakage on the IO rail and affect the custom board performance or processor reliability. Each signal has an associated IO supply for IO group (Example: VDDSHVx or VDDSx or VDDS_WKUP or VDDS_RTC). For more information, see the *Pin Attributes* table in the processor-specific data sheet.

For example, to pullup SPI0_CLK signal in GPIO MUX mode (GPIO0_0), connect the external pullup to supply rail connected to IO supply for IO group VDDS1.

7.9.4 Peripheral (Subsystem) Clock Outputs

For any of the processor peripheral that includes a clock output, the recommendation is to configure the RXACTIVE bit of the appropriate CTRLMMR_PADCONFIGx registers. The bit configuration is required for the clock output to work properly.

7.9.5 General Board Bring-up and Debug

Board bring-up tips before starting the board bring-up, includes verifying the following:

- The processor (selected OPN), attached devices and other components (passives) assembled on the custom board matches the design (custom board schematics and the custom board design requirements)
- Assembled boards have been inspected for mounting of components as per BOM (make sure component marked as DNI in the SK or EVM schematics or custom board schematics are not populated (installed)).

- The assembled boards have been inspected for assembly (soldering of the components and soldering workmanship)
- No external inputs are connected to the processor inputs before the custom board supply is connected and the processor supplies ramp and are stable

See the following FAQ:

[FAQ] Board bring up tips for Sitara devices (AM64x, AM243x, AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px)

7.9.5.1 Clock Output for Board Bring-Up, Test, or Debug

The following clock outputs are available on the processor for test and debug purposes only:

WKUP_SYSCLKOUT0

WKUP_PLL0_HSDIV0_CLKOUT (PER_SYSCLK0) is divided by 4 and connected to specific pins named WKUP_SYSCLKOUT0. The clock output is provided for test or debug purposes only.

SYSCLKOUT0

MAIN_PLL0_HSDIV0_CLKOUT (MAIN_SYSCLK0) is divided by 4 and connected to specific pins named SYSCLKOUT0. The clock output is provided for test and debug purposes only.

WKUP_OBSCLK0

The output can only be used as a functional clock source when WKUP_OBSCLK_OUTMUX is used to select the direct output from WKUP_HFOSC0.

The output can only be used for test and debug purposes when selecting any other clock source.

OBSCLKn [n = 0-1]

Observation clock outputs can only be used as a functional clock sources when OBSCLK0_CTRL is used to select the direct output from WKUP_HFOSC0.

The outputs can only be used for test and debug purposes when selecting any other clock source.

The recommendation is to provide TPs and parallel pulls (10kΩ or 47kΩ) when feasible for the processor pins designated OBSCLK0, OBSCLK1, WKUP_OBSCLK0, WKUP_SYSCLKOUT0 and SYSCLKOUT0.

In case the clock output pins are configured for alternate functions, the recommendation is to insert a TP on the trace and provide provision to isolated the signals from the attached device for test or debug.

7.9.5.2 Additional Information

The recommendation is to provide test point for PG outputs for testing or debug when not used.

For on-board attached devices (discrete DC/DC or LDO or Temperature sensor or Voltage monitors) that have an alert output, over-current indication output or PG (power good) output, the recommendation is to provide a pullup (10kΩ) and test point for testing or future enhancements (when not used).

7.9.5.3 General Board Bring-up and Debug Checklist

General

Review and verify the following for the custom board schematic design:

1. The recommendation is to add provision to isolate the IOs that can be used for debug from alternate functions
2. The recommendation is to add provision for connecting UART0 interfaces for debug during initial board build
3. The recommendation is to add provision for pulls for the UART interface signals that can float
4. The recommendation is to add provision for JTAG connector or Test points for JTAG interface signals
5. The recommendation is to place the pulls for the JTAG interface signals and EMU0, EMU1 as per pin connectivity requirements near to the processor JTAG interface pins
6. The recommendation is to add provision for external ESD protection for the UART and JTAG interface signals

Schematic Review

Follow the below list for the custom schematic design:

1. Provision to connect the debug UARTs have been provided (UART0, WKUP_UART0)
2. The required pullup, and series resistors are provided for the UART interface signals
3. External ESD protection provision added when external interface signals are directly connected to the processor UART signals

Additional

1. A number of processor IOs including UARTs are not fail-safe. The recommendation is to connect external inputs only after the processor supplies ramps
2. The recommendation is to disconnect the external interface signals in case the processor board is powered off

Refer below FAQ:

[FAQ] SK-AM62: Purpose Of Different UARTs

The FAQ is generic and can also be used for AM62Lx processor family.

8 Self-Review of Custom Board Schematic Design

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

After the required schematics updates are complete (following the user's guide, EVM or SK schematic implementation, hardware design considerations user's guide and other collaterals on TI.com), the next phase of the custom board design is to perform a self-review. The self-review can be done by following the review checklist provided (general, schematic review and additional) at the end of the detailed design guidelines description for each circuit or interface section of the user's guide. Example of schematic review checklist sections for self-review:

- *Processor Core and Peripheral Core Power Supply Checklist*
- *General Board Bring-up and Debug Checklist*

The schematic review checklist in also available in excel format. The checklist is multiple sheets segregated by:

- Readme page with links to all the schematics sections to review
- Table of content that summarizes all the circuit sections and Links to FAQs and other collaterals that can be used during custom board design
- IO supply connections and DDRSS interface (DDR4, LPDDR4
- Memory interface connections for MMC0, MMC1 and MMC2
- Memory interface connection for OSPI0 and GPMC
- Peripheral (high speed) interface connections for CPSW3G - Ethernet, USB0, USB1, UART and MCAN
- Peripheral (synchronous) interface connections for MCSPI, MCASP and I2C
- Peripheral (User interface) interface connections for CSI-2, DPI, DSI and GPIO interface
- Processor power connection including Processor and Processor peripheral core supplies, processor analog and IO supplies, eFuse programming supply
- Clock - inputs and outputs, Reset - input and outputs, RTC supplies
- Bootmode configurations
- General recommendations for external interface design
- Power architecture - PMIC or Discrete

The checklist includes figuere (illustrations) for each of the schematics sections with description labels for reference. The excel can be used to perform self-review and fill the review status and share or for documentation purpose.

The below FAQ lists the available collaterals and review steps that can be followed by custom board designer while performing a self-review of custom board schematics:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design - Custom board schematics self-review

Follow the below sections:

- AM62L32, AM62L31 Processor Family Schematic Design Checklist and General Guidelines and Schematic Review Checklist:
  - AM62L32_AM62L31_Schematic_Design_Checklist_General_Guidelines
  - Custom board schematic review checklist with figures - Recommended to use after reading the above Custom board schematic design guidelines

The below FAQ lists common errors observed (based on review of multiple customer schematics and reference to multiple collaterals). The recommendation is to read the list of errors and make the required updates to the custom board schematics:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - List of errors observed during customer schematics review

9 Custom Board Layout Notes (Added Near to the Schematic Sections) and General Guidelines

The recommendation is to consider adding the required or applicable design notes for the processor, attached devices and other on-board devices to reduce errors during custom board design. The recommendation is to add the required design notes for the processor memory (Example: USB2.0 interface, Ethernet interface, Display (DSITX0) interfaces including eMMC, OSPI, SD card, SDIO and other used processor peripherals including USB, MCSPI, MCASP). The recommendation is to include notes to include custom board boot mode configurations, placement of series and parallel resistors, placement of decoupling and bulk capacitors.

The recommendation is to mark all differential signals, critical signals that can affect performance and specify the target impedance (as required). See the following examples:

- The differential impedance for the USB2.0 data lines is expected to be within the specified tolerance for a nominal value of 90Ω.
- The differential impedance for the DSITX0 interface signals is expected to be within the specified tolerance for a nominal value of 100Ω.

See the following FAQs that includes board layout guideline to follow:

[FAQ] AM625: PCB Pattern Recommendations for Specific Peripherals

[FAQ] AM625: MMC0 PCB Connectivity Requirements

AM6442: PCB layout guidelines for MMCSD0(eMMC) and MMCSD1(SD card)

The FAQs are generic and can also be used for AM62Lx processor family.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

Refer below document for LVCMOS Board Design and Simulation Guidelines:

Board Design and Simulation Guidelines for High-Speed Parallel Interfaces

9.1 Layout Considerations

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. The recommendation is to make sure custom board design is compliant to the PCB trace delay requirements defined in the *Timing Conditions* tables found in the *Timing and Switching Characteristics* section of the processor-specific data sheet
3. The recommendation is to follow the relevant sections in the *Applications, Implementation, and Layout* section of the processor-specific data sheet
4. The recommendation is to follow general high-speed guidelines

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guideline

10 Custom Board Design Simulation

The baseline drive impedance and ODT settings for attached memory (DDR4 or LPDDR4) are derived from the signal integrity (SI) simulations performed on the EVM.

The recommendation is to perform simulation on the custom board design to finalize the values as the configuration values can be different compared to the EVM schematic implementation.

The below FAQs can be referenced when simulations are performed:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62L / AM62P / AM62P-Q1 / AM64x / AM243x Custom board hardware design – S-parameter and IBIS model of IO-buffer

[FAQ] Using DDR IBIS Models for AM64x, AM243x (ALV), AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px

To get an overview of the board extraction, board simulation, and analysis methodologies for high speed LPDDR4 interfaces, see the *LPDDR4 Board Design Simulations* chapter of the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* application note.

The drive strength can be adjusted using the *DDR Register Configuration Tool* on SysConfig.

For more information on configuring the DDRSS registers, see the following FAQ:

[FAQ] AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design – Processor DDR Subsystem and Device Register configuration

The FAQ is generic and can also be used for AM62Lx processor family.

For queries related to PDN power SI simulations, see the following FAQ:

[FAQ] AM62A3-Q1: AM62A3-Q1 PDN Power SI SIMULATION Questions

The FAQ is generic and can also be used for AM62Lx processor family.

10.1 DDR-MARGIN-FW

The DDR margin firmware and supporting scripts allow visualization and measurement of custom board margin in the DDR interface on board. The tools enable probe-less measurement of critical data signals to understand if the custom board design follows the recommended design guidelines of the interface.

DDR-MARGIN-FW - Firmware and scripts to measure system DDR margin

Check the device-specific (AM62L) product page on TI.com for availability.

For more information, see the following FAQ:

[FAQ] PROCESSOR-SDK-AM62X: Question about AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP DDR MARGIN TEST Tool

The FAQ is generic and can also be used for AM62Lx processor family.

11 Additional References

Additional references include FAQs and *Hardware Design Considerations for Custom Board Design* document for specific processor. Schematics for attached devices including PMIC and EPHY.

11.1 FAQ Covering AM64x, AM243x, AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62Lx Processor Families

The below FAQ summarizes key collaterals that can be referenced during custom board schematic design and custom board schematic review:

[FAQ] AM64x, AM243x (ALV, ALX), AM62x, AM62Ax, AM62Px, AM62D-Q1, AM62L Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

Note

While using the EVM PDF schematics with D-Notes and R-Notes for custom board schematics review, the recommendation is to view the FAQ links added on the schematics for additional information.

11.2 FAQs - Processor Product Family Wise and Sitara Processor Families

Based on TI sitara processor applications and systems team interactions with multiple custom board designers, queries from custom board designers and learnings from queries received from custom board designers and review of internal collaterals, FAQs have been created (related to (detailed explanation and example illustrations added) processor functioning, processor power and IO connections, processor peripherals and interfaces, processor evaluation SK or EVM, common errors observed during customer board design reviews, data sheet and pin attributes and commonly asked E2E queries) to support custom board designers during the custom board design phase. Refer the following list of FAQs is recommended during custom board design along with other available design collaterals including *Hardware Design Considerations for Custom Board Design* and *Schematic Design Guidelines and Schematic Review Checklist* on TI.com:

AM62Lx Processor Family:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and EVM

AM62Px Processor Family:

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

AM62Ax and AM62D-Q1 Processor Families:

[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

AM62x Processor Family:

[FAQ] AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

Sitara Processor Families:

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families

See the following FAQ that provides list of all the available FAQs including software related FAQs for sitara processor families:

[FAQ] AM6x: Latest FAQs on AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM24x, AM3x, AM4x Sitara devices

Note

The FAQs are being updated frequently. The recommendation is to review the FAQs of interest and the FAQ master list at regular intervals for availability of updated information.

11.3 Schematics Review (Self) and Schematic Review Request (Suppliers)

As part of the custom board design cycle, the recommendation is to perform a self review and team review of the design. External review with the silicon suppliers can be planned as required. Review supplier specific documentation for the process to be followed for schematic review request.

In case a schematics review request is required to be submitted to TI, the recommendation is to follow the below FAQ:

[FAQ] Sitara MPU Hardware Applications Support - Schematics review request

11.4 Processor Attached Devices Checklist

Ethernet PHY PCB Design Layout Checklist

Note

The recommendation is to verify availability of device-specific schematic review checklist on TI.com for the attached devices and verify the custom board schematic implementation using the available checklist.

12 User's Guide Content and Usage Summary

The user's guide includes schematic design guidelines that custom board designers can refer during the custom board schematic design. The user's guide also includes schematic review checklist for each of the peripheral sections that be used to review the custom board design. The recommendations provided in user's guide can be used by custom board designers to optimize the custom board design, minimize schematic errors, reduce custom board bring-up and debug time, and can possibly minimize future board re-spins.

13 References

13.1 AM62L

- Texas Instruments: *AM62Lx Sitara Processors*, Data Sheet
- Texas Instruments: *AM62L Sitara Processors*, Technical Reference Manual
- Texas Instruments: *AM62Lx Sitara Processors Silicon Errata*
- Texas Instruments: *EVM TMDS62LEVM*, product page
- Texas Instruments: *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family*, user's guide
- Texas Instruments: *AM62x, AM62Lx DDR Board Design and Layout Guidelines*, application note
- Texas Instruments: *AM62Lx Escape Routing for PCB Design*, application note
- Texas Instruments: *AM62L Maximum Current Ratings*, application note
- Texas Instruments: *AM62L Power Supply Implementation*, application note
- Texas Instruments: *AM62L Product Overview*, application note
- Texas Instruments: *Sitara AM62Lx Benchmarks*, application note
- Texas Instruments: *AM625x/AM623x and AM62Lx Hardware Migration Guide*, application note
- Texas Instruments: *Board Design and Simulation Guidelines for High-Speed Parallel Interfaces*, application note
- Texas Instruments: *xSPI Custom Flash Debug Guide for MCU+SDK*, application note
- Texas Instruments: *AM62x Audio System Design Guide*, application note
- Texas Instruments: *AM275x Audio System Design Guide*, application note

13.2 AM62P, AM62P-Q1

- Texas Instruments, *AM62Px Sitara Processors*, Data Sheet
- Texas Instruments, *AM62Px Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62Px Silicon Errata*
- Texas Instruments, *Starter Kit SK-AM62P-LP*, product page
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processors Family*, user's guide
- Texas Instruments, *AM62P Power Estimation Tool*, application note
- Texas Instruments, *PMIC for Powering AM62Px Devices*, application note
- Texas Instruments, *AM62Px Escape Routing for PCB Design*, application note
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*, application note
- Texas Instruments, *SK-AM62P-LP Design Package Folder and Files List*, product overview
- Texas Instruments, *Sitara AM62P Benchmarks*, application note
- Texas Instruments, *Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs*, application brief

13.3 AM62A7, AM62A3, AM62A7-Q1, AM62A3-Q1, AM62A1-Q1

- Texas Instruments, *AM62Ax Sitara Processors*, Data Sheet
- Texas Instruments, *AM62Ax Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62Ax Silicon Errata*
- Texas Instruments, *Starter Kit SK-AM62A-LP*, product page
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 and AM62D-Q1 Processor Families*, user's guide
- Texas Instruments, *AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 & AM62D-Q1 Processor Families Schematic Design Guidelines & Schematic Review Checklist*, user's guide

- Texas Instruments, *AM62Ax Maximum Current Ratings*, application note
- Texas Instruments, *AM62Ax Power Estimation Tool*, application note
- Texas Instruments, *PMIC Solution for AM62Ax*, product overview
- Texas Instruments, *PMIC for Powering AM62Px Devices*, product overview
- Texas Instruments, *AM62Ax/AM62Dx Escape Routing for PCB Design*, user's guide
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*, application note
- Texas Instruments, *SK-AM62A-LP Design Package Folder and Files List*, product overview
- Texas Instruments, *Sitara AM62Ax Benchmarks*, application note
- Texas Instruments, *Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs*, application brief

13.4 AM62D-Q1

- Texas Instruments, *AM62Dx Sitara Processors*, Data Sheet
- Texas Instruments, *AM62Dx Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62Dx Sitara Processors Silicon Errata, Silicon Revision 1.0*
- Texas Instruments, *AUDIO-AM62D-EVM*, product page
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 and AM62D-Q1 Processor Families*, user's guide
- Texas Instruments, *AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 & AM62D-Q1 Processor Families Schematic Design Guidelines & Schematic Review Checklist*, user's guide
- Texas Instruments, *PMIC Solution for AM62Ax*, product overview
- Texas Instruments, *PMIC for Powering AM62Px Devices*, product overview
- Texas Instruments, *AM62Ax/AM62Dx Escape Routing for PCB Design*, user's guide
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*, application note
- Texas Instruments, *Sitara AM62Dx Benchmarks*, application note
- Texas Instruments, *Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs*, application brief

13.5 AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP

- Texas Instruments, *AM62x Sitara Processors*, Data Sheet
- Texas Instruments, *AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*, Data Sheet
- Texas Instruments, *AM62x Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62x Silicon Errata*
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family*, user's guide
- Texas Instruments, *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* , user's guide
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- Texas Instruments, *Powering the AM62x With the TPS65219 PMIC*, application note
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- Texas Instruments, *AM62x SiP Escape Routing for PCB Design*, application note
- Texas Instruments, *AM62x, AM62Lx DDR Board Design and Layout Guidelines*, application note
- Texas Instruments, *PRU-ICSS Feature Comparison*, application note
- Texas Instruments, *How the AM625SIP Processor Accelerates Development by Integrating LPDDR4*, application brief

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- Texas Instruments, *SK-AM62B-P1 Design Package Content Overview*, product overview
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- Texas Instruments, *SK-AM62-SIP Design Package Folder and Files List*, product overview
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- Texas Instruments, *Sitara AM62x Benchmarks*, application note

13.6 Common for all Processor Families

- Texas Instruments, *AM623, AM625, AM625SIP, AM620-Q1, AM625-Q1, AM62A3, AM62A7, AM62A7-Q1, AM62D-Q1, AM62P-Q1 Schematic Design Guidelines and Review Checklist* application note
- Texas Instruments: *Accelerating Development with SysConfig using MCU+SDK*, application note
- Texas Instruments: *Board Design and Simulation Guidelines for High-Speed Parallel Interfaces*, application note
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- Texas Instruments, *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note
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- Texas Instruments, *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines* application note
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- Texas Instruments, *Emulation and Trace Headers Technical Reference Manual* user's guide
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- Texas Instruments, *Interface Circuits for TIA/EIA-644 (LVDS)* design consideration
- Texas Instruments, *General Hardware Design/BGA PCB Design/BGA Decoupling* application note
- Texas Instruments, *MSL Ratings and Reflow Profiles* application note
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- Texas Instruments, *Clocking Design Guide for KeyStone Devices* application note
- Texas Instruments, *Hardware Design Guide for KeyStone II Devices* application note
- Texas Instruments, *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design* design guide
- Texas Instruments, *Jacinto 7 DDRSS Register Configuration Tool* application note
- Texas Instruments, *Using IBIS Models for Timing Analysis* application note
- Texas Instruments: *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs* application note
- Texas Instruments, *McASP Design Guide - Tips, Tricks, and Practical Examples* application note
- Texas Instruments, *Driving Multiple Loads With a Single LVCMOS Oscillator* application note

13.7 Master List of Available FAQs - Processor Family Wise

A complete list of the FAQs are available that is recommended to quickly view the available list of FAQs for the selected processor or processor families.

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and EVM

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

13.8 Master List of Available FAQs - Sitara Processor Families

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families

13.9 FAQs Including Software Related

[FAQ] AM6x: Latest FAQs on AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM24x, AM3x, AM4x Sitara devices

13.10 FAQs for Attached Devices

[FAQ] DP83869-EP: Ethernet compliance Testing failure

[FAQ] TPS65219: Benefits of a PMIC vs discrete solution to power Sitara AM62x MPU

[FAQ] List of FAQs for TPS6594-Q1, TPS6593-Q1, LP8764-Q1 PMICs

14 Terminology

ADC	Analog-to-Digital Converter
BOM	Bill of Materials
CAN	Controller Area Network
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
DFU	Device Firmware Upgrade
DNI	Do Not Install
DPI	Display Parallel Interface
DRD	Dual-Role Device
E2E	Engineer to Engineer
ECC	Error-Correcting Code
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EOS	Electrical Over-Stress
ESD	Electrostatic discharge
ESL	Effective Series Inductance
ESR	Effective Series Resistance
FAQ	Frequently Asked Question
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HS-RTDX	High Speed Real Time Data eXchange
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
IEP	Industrial Ethernet Peripheral
JTAG	Joint Test Action Group
LDO	Low Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MAC	Media Access Controller
MCASP	Multichannel Audio Serial Ports
MCSPI	Multichannel Serial Peripheral Interface

MDI	Medium Dependent Interface
MDIO	Management Data Input/Output
MMC	Multi-Media Card
MMCSD	Multi-Media Card/Secure Digital
ODT	On-die Termination
OPN	Orderable Part Number
OSPI	Octal Serial Peripheral Interface
PCB	Printed Circuit Board
PDN	Power Distribution Network
PET	Power Estimation Tool
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROC	Processor-Specific Data Sheet Recommended Operating Condition
SD	Secure Digital
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TEN	Test Enable
TMS	Test Mode Select Input
TRC_DATAn	Trace Data n
TRM	Technical Reference Manual
TRSTn	Reset
UART	Universal Asynchronous Receiver/Transmitter
WKUP	Wake-up
XDS	eXtended Development System
ZQ	Memory Device Calibration reference resistor

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 31, 2025 to May 30, 2026 (from Revision * (March 2025) to Revision A (May 2026)) **Page**

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- Updated Processor Family Specific User's Guide section....................3
- Updated Custom Board Schematic Design Implementation Checklist Sub-Sections Description....................3
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