Technical Article

How SHP in Plastic Packaging Addresses 3 Key Space Application Design Challenges

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Electronics intended for space missions face unique conditions and challenges – specialized integrated circuit (IC) packaging can help mitigate some of those challenges. We at TI have historically developed devices for commercial (non-space) use first; only after verification in a plastic package did the engineering team start on the ceramic design. But ceramic packages are usually not drop-in compatible with plastic packages, which necessitates developing new test and characterization hardware and qualifying the ceramic package test solution for large-scale production. These efforts pose a problem for space hardware designers because they either have to wait for the creation of the ceramic-packaged device to start their prototype build, or start with the plastic-packaged IC for their prototype and redesign and refabricate the board when ceramic samples become available.

What Is SHP?

TI has developed a new device screening specification called space high grade in plastic (SHP) for space-qualified devices constructed in plastic packaging traditionally used in industrial applications. SHP includes both plastic substrate ball-grid array (BGA) and plastic-encapsulated packages. The SHP qualification level produces devices suitable for tough mission profiles typically served with ceramic Qualified Manufacturers List (QML) Class V devices.

The SHP level represents a reliability grade higher than TI's space-enhanced products in many parameters important to tough space missions. As listed in Table 1, the most important differences are higher single-event latch-up immunity, a higher total ionizing dose, the production burn-in and the life test per wafer lot.

Table 1. Comparing TI's SHP Qualification Category to Other Known or Drafted Standards

	Space-enhanced product	**SHP**	**QML-P**(1)	**QML-Y**(2)	**QML-V**
Specification owner	TI	TI	Defense Logistics Agency (DLA)/Joint Electron Device Engineering Council (JEDEC)	DLA/JEDEC	DLA/JEDEC
Packaging	Plastic substrate or encapsulated	Plastic substrate or encapsulated	Plastic encapsulated	Ceramic substrate (plastic substrate)(2)	Ceramic
Hermetic	No	No	No	No	Yes
Single controlled baseline	Yes	Yes	Yes	Yes	Yes
Bond wires(when used)	Gold	Gold	Gold	Gold	Aluminum
Is there pure tin?	No	No	No	No	No
Production burn-in	No	Yes	Yes	Yes	Yes
Outgassing tested per American Society of Testing and Materials (ASTM) E595	Yes	Yes	Yes	N/A(2)	N/A (no plastic)
Lot-level temperature cycle	Lot level	Group D	Group D	Group D	Group D

Table 1. Comparing TI's SHP Qualification Category to Other Known or Drafted Standards (continued)

	Space-enhanced product	SHP	QML-P(1)	QML-Y(2)	QML-V
Lot-level highly accelerated stress testing (HAST)	Yes	Group D	Group D	Group D	N/A
Multiple wafer lots per reel possible	No	No	No	No	No
Life test per wafer lot	No	Yes	Yes	Yes	Yes
The following items are required in the TI specs			The following items are not required in the QML specs		
TI Radiation (TID) Lot Acceptance (RLAT / RHA)	**All SEP and SHP have RLAT**		**TI parts of these classes are usually RHA via RLAT but does vary by product (all new parts will have RLAT going forward)**		
Single-Event Latchup (SEL) test (level could vary by product)	TI = 43 MeV	**TI products are normally 60MeV to 120 MeV at these screening levels**			
Radiation, Total Ionizing Dose (TID) (level could vary by product)	TI = 30krad to 50krad (RT, radiation tolerant)	**TI products are normally 50krad to 300krad at these screening levels** (RHA, radiation-hardness assured)			

(1) QML Class P: in JEDEC/DLA review in 2022
(2) QML Class Y: plastic substrate in DLA/JEDEC review in 2022. Outgassing would be added if plastic is allowed.

It is possible to mitigate design challenges by using plastic packaging with the same pinout and basic package used in space- and industrial-grade versions. In addition to reducing development time and resources, space application designers should consider the thermal efficiency, size and bandwidth benefits of plastic packages.

Design Challenge No. 1: Thermal Efficiency

Traditional hermetic ceramic package designs require placing the die in a cavity and welding a lid to the top of the cavity to provide a moisture-proof solution. This design leaves an airgap between the die and the metal lid that is difficult to bridge with a thermal epoxy. With flip-chip BGA SHP packaging, the metal lid connects to the back of the flip-chip die directly with thermal epoxy; there is no airgap to fill.

TI has seen an improvement in thermal efficiency from the die to the package, with the thermal resistance reducing from ~16 C/W in column-grid array ceramic packages to ~0.8 C/W in plastic BGA packages. By allowing the system around the chip to run hot and stay reliable, you expend less size, weight and cost in the system to dissipate heat by removing a fluid pump, additional heat-sink metal or other heat-removal systems.

Design Challenge No. 2: Size Constraints

The space industry calculates launch costs on size and weight, so a smaller, lighter solution is cheaper to launch into orbit. The total package size of flip-chip BGA packaging is smaller than the ceramic equivalent in all dimensions. Figure 1 shows a 15-mm-by-15-mm hermetic ceramic package, used for the QML-V ADC12DJ3200QML-SP, with a total height of >6 mm. The plastic BGA shown on the right is the package used for both the new ADC12DJ5200-SP and ADC12QJ1600-SP, which fit in a 10-mm-by-10-mm package with a total height of <2 mm. This significant size reduction means a smaller total solution, reducing the size and weight of the entire system or creating a ability to fit more analog-to-digital converters (ADCs) in the same area.

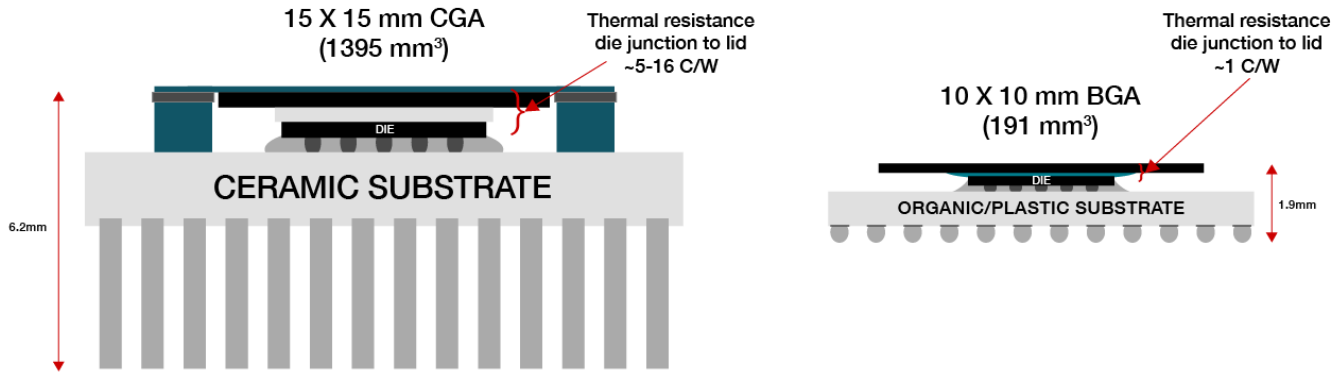

Figure 1. Comparing Hermetic-ceramic Packaging to Plastic Packaging

Figure 2 illustrates the improvements in package size of the 10-mm-by-10-mm-by-1.9-mm ADC12DJ5200-SP and ADC12QJ1600-SP (which share this package) to the prior generation 15-mm-by-15-mm-by-6.2-mm ceramic ADC12DJ3200QML-SP.

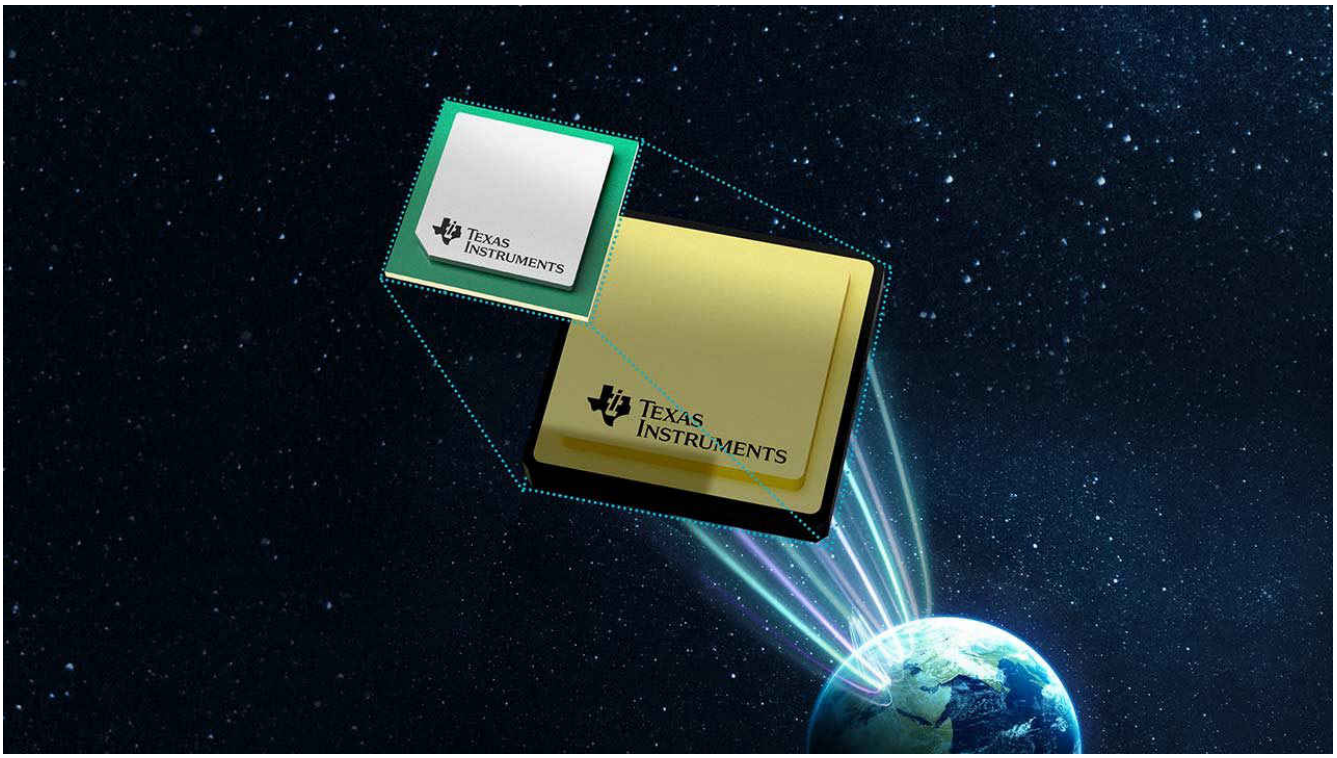

Figure 2. Comparing the Packaging Size across Generations of Space-grade ADCs

Design Challenge No. 3: Increasing Bandwidth

For high-frequency products in flip-chip packages, plastics provide superior electrical performance when compared to ceramic for these reasons:

- The relative permittivity of the organic substrates in plastic packages is about 3.7; for ceramic, it is 9.8. As a result, capacitive coupling between adjacent signal lines for plastic packages is over 2.5 times less, improving crosstalk and signal integrity.
- The lower permittivity enables the creation of 100-Ω differential lines and 50-Ω single-ended lines with smaller wire-to-wire spacings and smaller wire-to-ground spacings, enabling higher density-controlled impedance lines in plastic substrates compared to ceramic substrates.
- The lower capacitance plastic substrates improve the bandwidth and return loss of key analog signals.

Additionally, plastic substrates yield a higher bandwidth through the use of copper for signal lines and power planes, versus the tungsten used in ceramic substrates. Copper has over a third less electrical resistance compared to tungsten.

Conclusion

TI's SHP space-qualification level provides higher thermal efficiency, a smaller footprint and increased bandwidth compared to traditional ceramic packaging. The common package and pinout between the industrial- and space-grade versions enable you to get the newest technologies into your space hardware designs as soon as the commercial-grade device is sampling, because all prototyping work on the commercial product translates directly to a drop-in space-qualified SHP product when it's time to fly the system.

Additional Resources

- Learn about our other radiation-hardened and radiation-tolerant products at TI.com/space.
- Keep up to date with newly released space products with the "TI Space Products Guide."

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