Technical Article

What's Not in the Power MOSFET Data Sheet Part 2: Voltage-dependent Leakage Currents

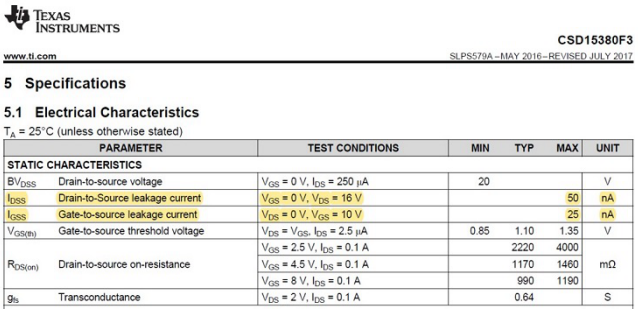
John Wallace1

In part 1 of this series, I reviewed power metal-oxide semiconductor field-effect transistor (MOSFET) data sheets and explained what's in the data sheet and more importantly, what's not, while specifically looking at the temperature dependence of some key MOSFET parameters. In part 2, I'll focus on voltage-dependent leakage currents – the drain-to-source leakage (I_{DSS}) and the gate-to-source leakage (I_{GSS}).

Why leakage currents? There are two fundamental reasons why leakage currents are important when selecting a power MOSFET for your application. First, in electronic systems, there is a green campaign to reduce wasted power, especially when the system is operating in standby mode. And second, in battery-operated systems low leakage helps maximize both battery life for primary cells and the run time between charges for secondary cells.

MOSFET Leakage Currents

As shown in Figure 1, the MOSFET data sheet for the CSD15380F3 specifies two leakage currents: I_{DSS} and I_{GSS}.



TEXAS INSTRUMENTS
www.ti.com
CSD15380F3
SLPS579A – MAY 2016 – REVISED JULY 2017

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	20			V
I_{DSS}	Drain-to-Source leakage current	V_{GS} = 0 V, V_{DS} = 16 V			50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 2.5 µA	0.85	1.10	1.35	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_{DS} = 0.1 A		2220	4000	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.1 A		1170	1460	
		V_{GS} = 8 V, I_{DS} = 0.1 A		990	1190	
g_{fs}	Transconductance	V_{DS} = 2 V, I_{DS} = 0.1 A		0.64		S

Figure 1. Leakage Current Specifications from the CSD15380F3 Data Sheet

The maximum leakage is specified at one voltage: I_{DSS} at 80% of BV_{DSS} (V_{GS} = 0 V) and I_{GSS} at the absolute maximum V_{GS} (V_{DS} = 0 V). I'm often asked how these parameters vary with voltage, and the answer depends not only on the applied voltage but also on the gate electrostatic discharge (ESD) structure, as detailed in the technical article, "What type of ESD protection does your MOSFET include?" As a refresher, the three types of ESD protection used in TI MOSFETs are none (lowest leakage), single-ended (lowest leakage) and back-to-back (highest leakage).

I_{GSS} Current

In this section, I'll present graphs showing I_{GSS} variation with voltage for several TI N- and P-channel NexFET™ power MOSFETs with the three types of gate ESD protection. These are typical curves for design guidance only and not a guarantee of performance. TI only guarantees leakage as specified in the MOSFET data sheet.

Figure 2 shows sweeps of I_{GSS} vs. V_{GS} for a 30-V N-channel FET (NFET) and a –20-V P-channel FET (PFET) that have no gate ESD protection. The leakage is relatively flat until V_{GS} gets close to its positive and negative absolute maximum limits.

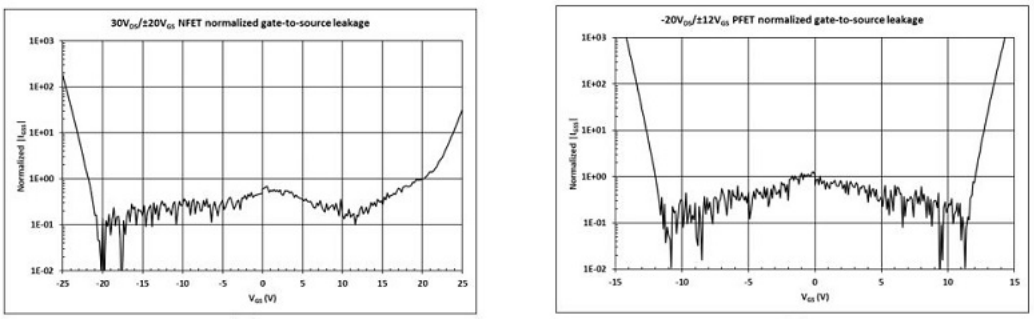


Figure 2. I_{GSS} Vs. v_{GS} With No ESD Protection: 30-v NFET (a); and –20-v PFET (b)

Figure 3 shows I_{GSS} for a 20-V N-channel FET and a –20-V P-channel FET with a single-ended gate ESD protection structure. The leakage current increases exponentially when the gate ESD diode becomes forward-biased. If this is likely to occur in an application, then you must use an external gate resistor to limit the current and prevent damage to the MOSFET.

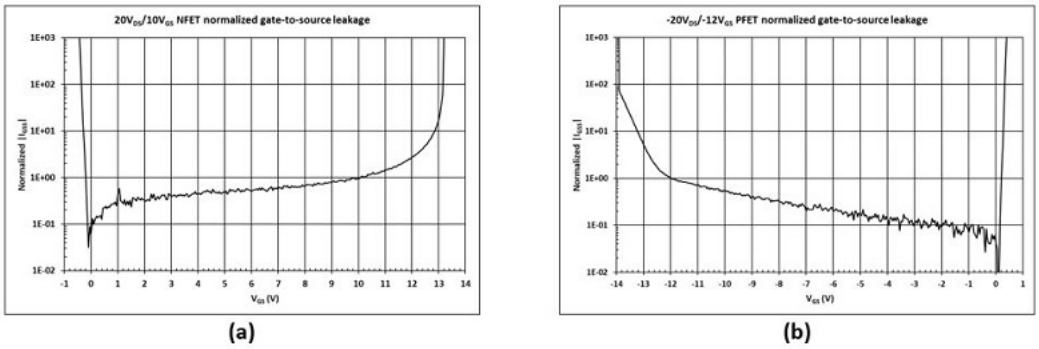


Figure 3. I_{GSS} vs. V_{GS} with single-ended ESD protection: 20-V NFET (a); and –20-V PFET (b)

The plots in Figure 4 display I_{GSS} for a 60-V NFET and a –8-V PFET with a back-to-back gate ESD protection structure. These devices display a symmetric leakage characteristic around V_{GS} = 0 V because of the back-to-back gate ESD diodes.

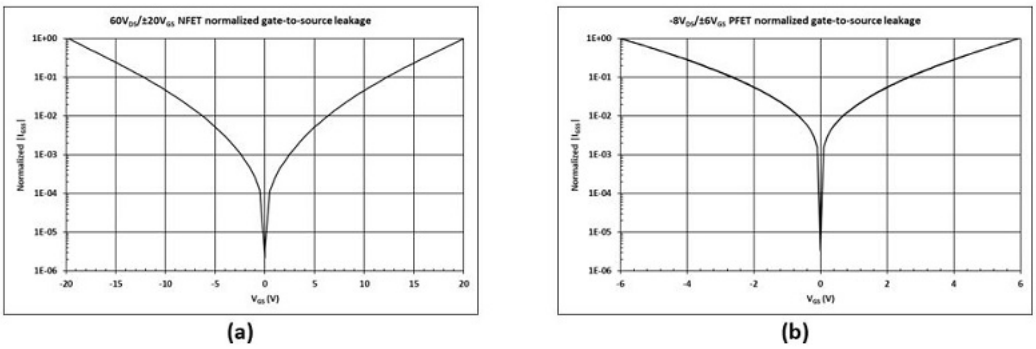


Figure 4. I_{GSS} vs. V_{GS} with back-to-back ESD protection: 60-V NFET (a); and –8-V PFET (b)

I_{DSS} Current

The other MOSFET leakage current, I_{DSS}, is from drain-to-source when the FET is off. The next several graphs show I_{DSS} vs. V_{DS} for TI NFETs and PFETs with the three types of ESD protection. These are typical curves for design guidance only and not a guarantee of performance. TI only guarantees leakage as specified in the MOSFET data sheet.

Figure 5 plots I_{DSS} for a 30-V NFET and a –20-V PFET with no ESD protection.

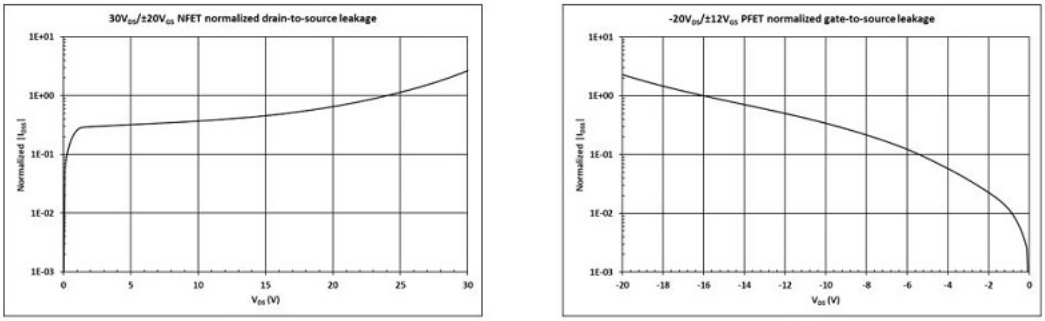


Figure 5. I_{DSS} Vs. v_{DS} With No ESD Protection: 30-v NFET (a); and –20-v PFET (b)

Figure 6 shows I_{DSS} for a 20-V N-channel MOSFET and a –20-V P-channel FET, with a single-ended gate ESD protection diode.

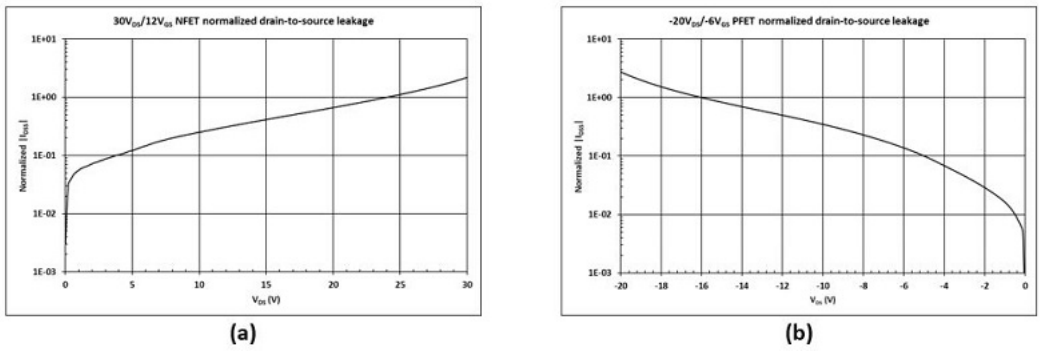


Figure 6. I_{DSS} Vs. v_{DS} With Single-ended ESD Protection: 20-v NFET (a); and –20-v PFET (b)

The plots in Figure 7 display I_{DSS} for a 12-V N-channel MOSFET and a –20-V P-channel MOSFET with the back-to-back gate ESD protection structure.

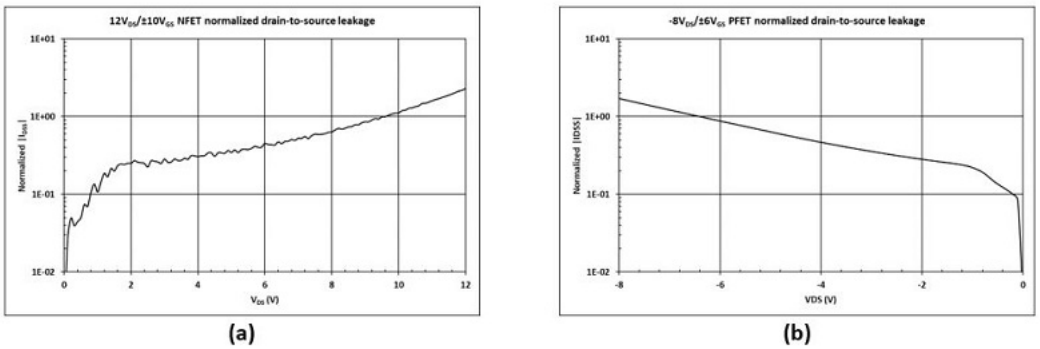


Figure 7. I_{DSS} Vs. v_{DS} With Back-to-back ESD Protection: 12-v NFET (a); and –20-v PFET (b)

Conclusion

I hope that the typical curves of I_{GSS} current and I_{GSS} vs. V_{GS}, and I_{DSS} current and I_{DSS} vs. V_{DS} will help you understand how MOSFET leakage currents vary with voltage. TI specifies and tests the maximum leakage currents at the conditions in the Electrical Characteristics data sheet. As a reminder, always use the data-sheet limits when designing with TI FETs, and if you don't see it in the data sheet, request it from your FET vendor.

Additional Resources

- Visit the TI MOSFET support and training center.
- Check out these technical articles
  - "What type of ESD protection does your MOSFET include?"
  - "What's not in the power MOSFET data sheet, part 1: temperature dependency"

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