Design Guide: TIDA-020079

Zone Reference Design

Description

This reference design demonstrates key functions of next-generation zone control modules including power distribution, load actuation, and in-vehicle networking. The design highlights functional safety compliant PMIC and microcontroller (MCU) design, redundant power supply management with ideal diode controllers, and smart eFuses for safe power distribution. The design also features various options for load actuation expected in zone control modules, such as high-side drivers, motor drivers, configurable drivers, and a Class-D audio amplifier. The zone reference design showcases a variety of communication protocols, such as Ethernet, CAN, and LIN and enables emerging trends in vehicle networking technology such as Ethernet AVB, 10BASE-T1S, and CAN FD light.

Resources

TIDA-020079	Design Folder
AM263P4-Q1, DP83TG721S-Q1	Product Folder
TPS653860-Q1, TPS2HCS10-Q1	Product Folder
DRV8245S-Q1, TIC12400-Q1	Product Folder

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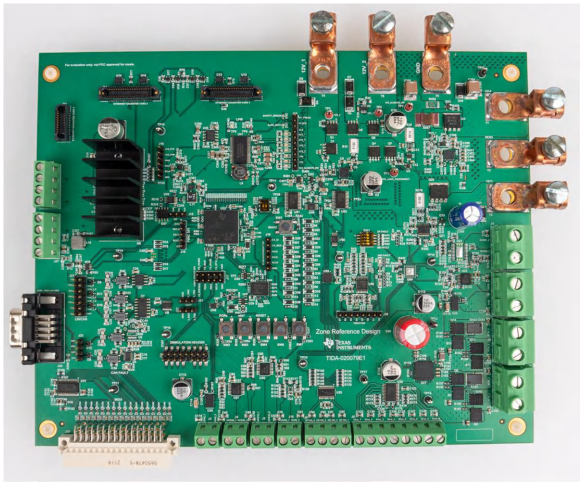
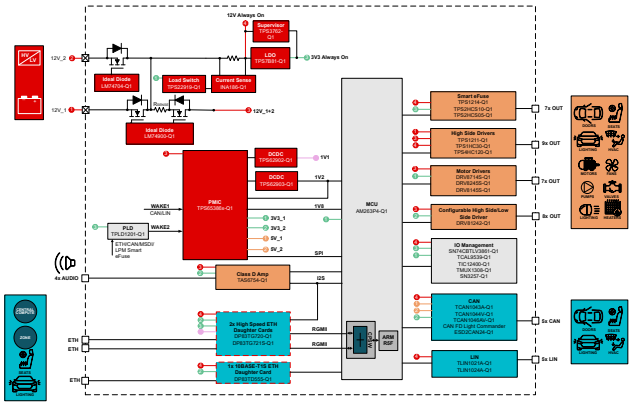
Features

- MCU with integrated Ethernet switch to optimize Ethernet ring topologies by implementing the following hardware protocols:
  - 802.1Qav, 802.1Qbv, 802.1cb (partial), 1588 TE, and 802.1Q ALE
- AVB Ethernet audio support with Ethernet PHY hardware time stamping and integrated media clock adjustment
- ASIL D-rated MCU and PMIC with system Limp Home Mode (LHM) capability
- Low-power mode with wake from Ethernet, CAN, LIN, smart eFuses, and MSDI off-board switch inputs
- Optimized microcontroller GPIO:
  - SPI daisy chain of smart eFuses and motor drivers
  - SPI and I2C IO expanders

Applications

- Zone control module





1 System Description

Automotive OEMs are moving towards a zone-based architecture where control modules are based on the location within the vehicle and software is centralized. This allows for over-the-air updates, easier collection of vehicle data, design and manufacturing cost savings, and new potential revenue streams. For more information, see *Software-Defined Vehicles Shift the Future of Automotive Electronics Into Gear* and *How a Zone Architecture Paves the Way to a Fully Software-Defined Vehicle* application briefs. This reference design showcases various subsystems within a zone control module, such as input power protection and distribution, load drivers, communication, and IO management.

This design features redundant 12V inputs that are ORed together with ideal diode controllers to create a 12V always-on rail and a second 12V rail for load disconnect. The 12V always-on rail is used to supply power to the PMIC, MCU, smart eFuse, CAN, LIN, ETH, and always-on 3.3V LDO. The 12V load disconnect rail supplies power to load drivers that do not require always-on operation such as high-side switches, motor drivers, and class D audio amplifiers. Additionally, this design showcases smart eFuses which feature configurable overcurrent protection and programmable fuse profiles to optimize the wire harness for any load profile with full protection.

This zone reference design showcases multiple types of load drivers that can be seen in typical zone control modules, including high-side drivers, motor drivers, and a configurable high-side or low-side driver to drive various actuators, such as motors, fans, pumps, valves, lighting, and heating elements. This design showcases high-side switches and controllers with high-accuracy current sensing and output diagnostics, such as overload and short-circuit protection, undervoltage lockout (UVLO) protection, thermal shutdown recovery, ground loss protection, and reverse battery protection. TI's motor drivers offer voltage monitoring and load diagnostics as well as protection against overcurrent and overtemperature. Additionally, this design features a Class-D audio amplifier to demonstrate zonal audio.

Various types of networking protocols can be used in zonal architecture, and this design provides versatility by offering 1000BASE-T1, 100BASE-T1, 10BASE-T1S, CAN FD, CAN FD Light, and LIN. The board has two connectors with RGMII and additional IO needed for high-speed Ethernet to enable Ethernet ring and Ethernet AVB support. The connectors allow daughter cards to be attached to enable testing of various PHYs. There is an additional daughter card connector for a 10BASE-T1S card. This design has three CAN FD transceivers supplying four ports with the option of 2 × UART over CAN. This design also features a CAN FD Light commander for a 5Mbps data rate. Lastly, this design features two LIN transceivers with a total of 5 ports.

Shifting to zone architecture increases the amount of load drivers on a single board, resulting in a need for more GPIO. This design uses I2C and SPI IO expanders and multiplexers to offer additional IO. The board also offers a 24-pin multiple switch detection interface (MSDI) for autonomous input and output monitoring when the MCU is powered down. Lastly, this board utilizes programmable logic devices to reduce the overall logic footprint by integrating logic functions into one package.

2 System Overview

2.1 Block Diagram

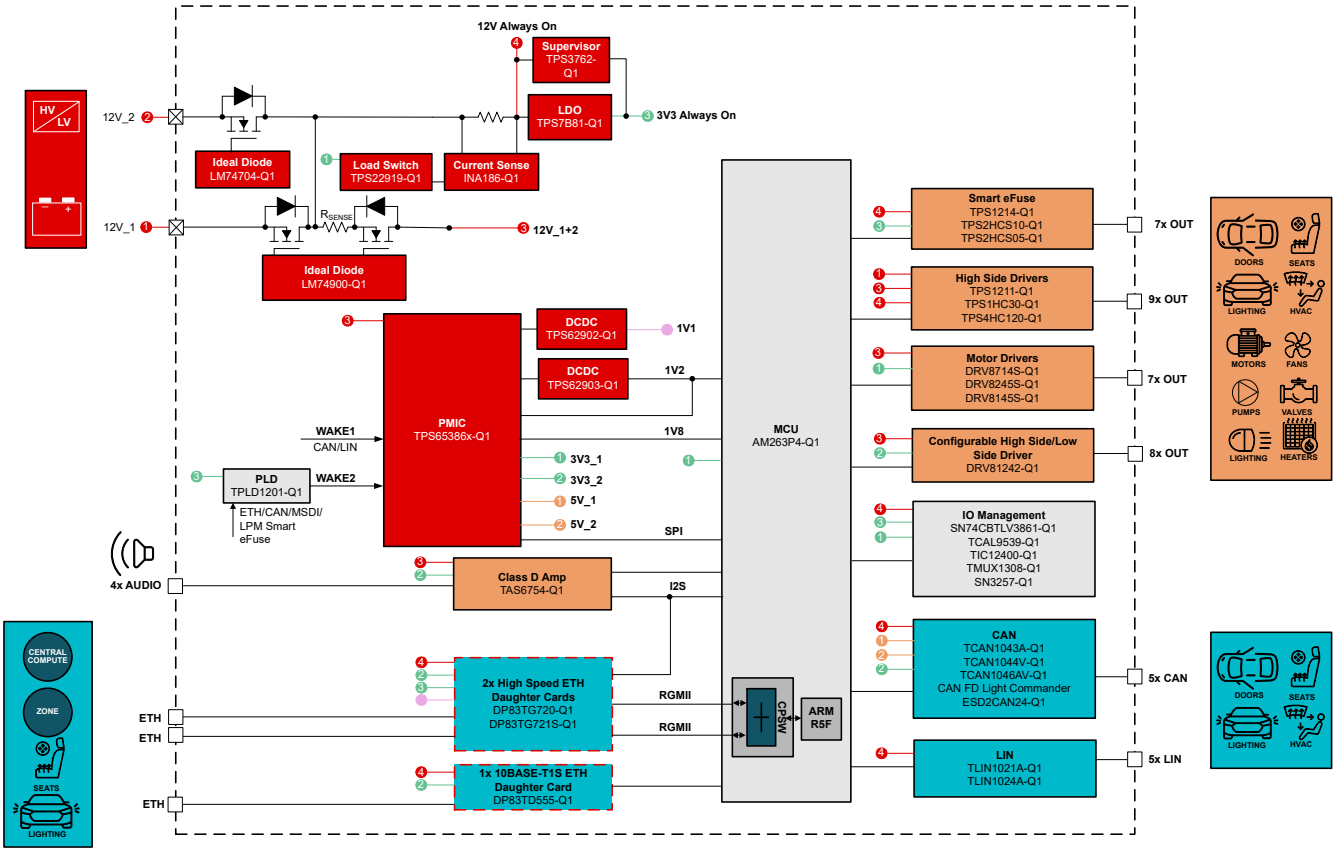


Figure 2-1. TIDA-020079 Block Diagram

2.2 Design Considerations

2.2.1 Redundant Input Supplies

This design features two ideal diode controllers for the redundant 12V inputs, the LM74704-Q1 and LM74900-Q1. The LM74704-Q1 drives an external N-channel MOSFET to regulate forward voltage drop and turns off the MOSFET when a reverse current event is detected. The LM74900-Q1 behaves similarly, but drives back-to-back N-channel MOSFETs to emulate an ideal diode rectifier and has integrated current sense. The first MOSFET provides reverse input protection and output voltage holdup, and the second MOSFET allows load disconnect in case of an overcurrent or overvoltage event. In this system, the drain of the N-channel MOSFET driven by LM74704-Q1 is connected to the drain of the first N-channel MOSFET driven by LM74900-Q1 to create a 12V always-on rail. The second MOSFET of LM74900-Q1 provides power to load drivers to allow for load disconnect in the case of overcurrent or overvoltage and to disconnect the supply during a low-power state to reduce quiescent current.

2.2.2 Ethernet Ring

The AM263P4-Q1 has an integrated 3-port gigabit Ethernet switch (common platform switch, CPSW) supporting 2 external ports to implement an Ethernet ring topology. The CPSW supports multiple features and protocols in hardware to off-load computing resources for redundant packet replication, ring termination, and packet forwarding.

2.2.3 Audio Video Bridging (AVB)

In addition to Ethernet ring topologies, the zone reference design supports Ethernet audio video bridging (AVB) protocol to play local audio through a combination of the AM263P4-Q1, DP83TG721S-Q1, and the local class-D amplifier. The AM263P4-Q1 supports Ethernet AVB protocol through a combination of hardware (integrated in the CPSW switch and the programmable real-time unit) and software to play local digital audio. The DP83TG721S-Q1 PHY implements IEEE1588v2, 802.1AS time synchronization and IEEE1722 media clock generation to adjust the local media clocks and output all necessary audio clocks including the serial clock (SCLK) and frame sync (FSYNC) clock to the AM263P4-Q1 and the Class-D amplifier.

The AM263P4-Q1 integrated CPSW Ethernet switch supports AVB protocols such as 802.1Qav, 802.1Qbv, and IEEE1588 time stamping. In addition, the programmable real-time unit is capable of supporting Inter-Integrated Circuit Sound (I2S) to transmit local digital audio data. The Ethernet AVB hardware bill of materials is simplified by implementing the DP83TG721S-Q1 Ethernet PHY to remove the need for an additional clock generator or phased-lock loop.

2.2.4 Low-Power Mode and Wake

Low-power mode reduces energy consumption by limiting or turning off non-essential functions to extend the range of a vehicle. This design demonstrates low-power mode by turning off nonessential load drivers connected to the output of LM74900-Q1 and only devices connected to the 12V and 3.3V always-on rails (that is, PMIC, smart eFuse, MSDI, CAN, LIN, ETH) receive power. The design allows for wake activation from Ethernet, CAN, LIN, smart eFuse, and MSDI. For the system to wake up, packets must be detected on the communication bus for Ethernet, CAN, and LIN, and the load current increases on the smart eFuses, or MSDI detects an off-board switch input. The TPS65386x-Q1 PMIC has two wake pins rated for up to 40V. Figure 2-2 shows the CAN and LIN INH pins tied together for a 12V wake signal going to WAKE1 and the TPLD1201-Q1 being used to aggregate the 3.3V wake signals going to WAKE2.

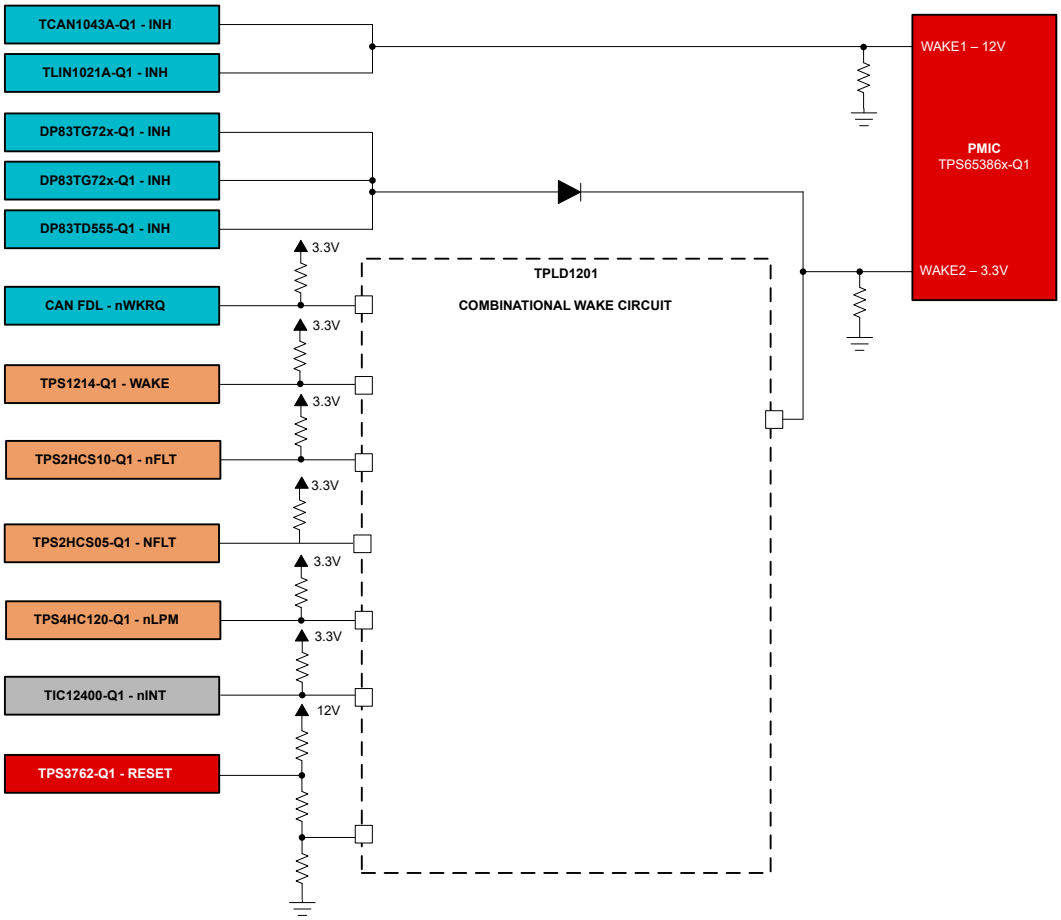


Figure 2-2. Wake Diagram

Figure 2-3 shows a closer look at the wake circuitry flashed into the TPLD1201-Q1. Most pins are active low during system sleep, so if a signal *low* is observed at any of the pins, wake 2 is asserted high, waking up the PMIC.

The TPSxHCSxx-Q1 family does require additional logic because the wake signal is only active for 100µs, which is shorter than the wake deglitch time of the PMIC. To overcome this challenge, the TPSxHCSxx-Q1 wake pins are latched for 3ms using D-flip-flops, enabling the PMIC to see the TPSxHCSxx-Q1 wake events.

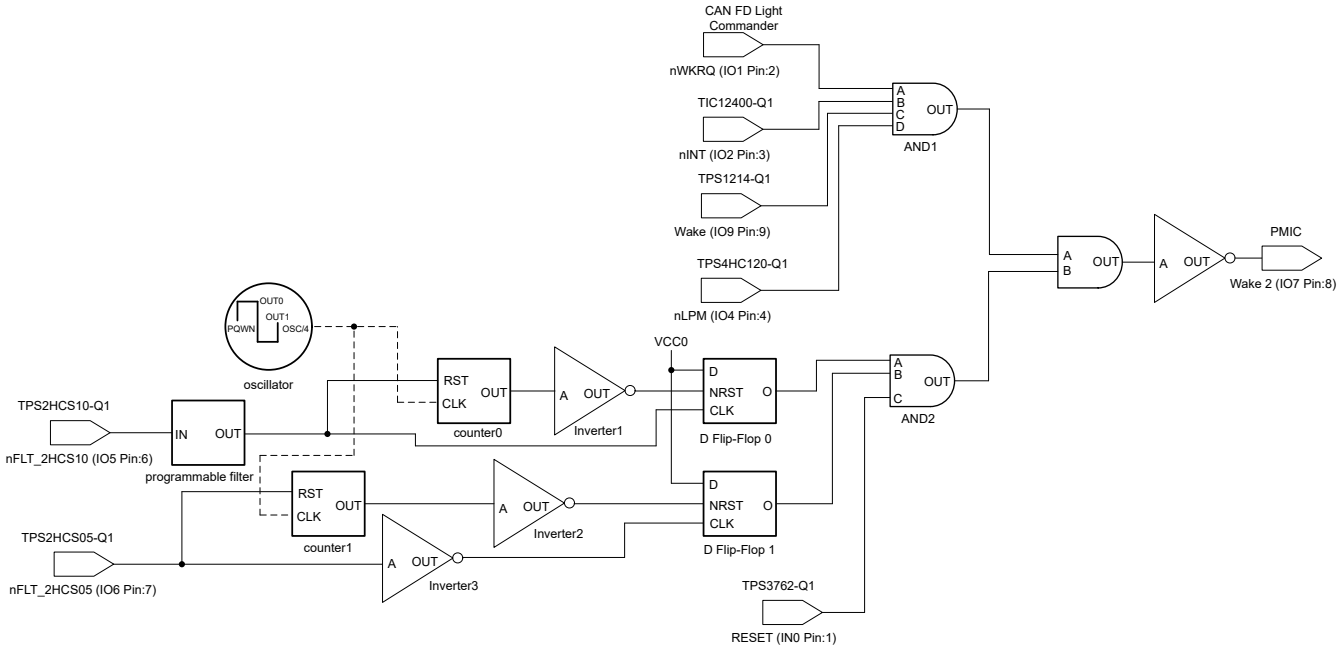


Figure 2-3. TPLD Wake Logic

2.2.5 Limp Home Mode

Limp home mode (LHM) is a safety feature in vehicles used to maintain essential functions when a critical fault is detected. This design uses the PMIC to detect a safety issue and place the system into LHM where the outputs are in the desired safe state. The PMIC has two SAFE_OUT outputs that can be configured for the desired safing condition. These outputs can connect to the LHI pin of the smart eFuse to tell the smart eFuse to enter LHM and enter the desired safe state (can be configured ON or OFF). Additionally, the smart eFuses can detect a SPI watchdog timeout error (that is, a SPI communication error) and if V_{DD} is lost, the device signals a fault as SPI is not supported without V_{DD}.

2.2.6 SPI Daisy Chain

This design demonstrates separate smart eFuse and motor drive SPI daisy chaining by using a single SPI port for multiple smart eFuses or motor drivers. These devices can be configured to allow for a single chip select pin to be shared across all devices in a chain, enabling control and diagnostic feedback using only 5 pins (4 SPI, 1 FAULT). SPI daisy-chaining creates system-level savings of GPIO and ADC pins. For more information, including test results, see the *Reducing System Bill of Materials and MCU Pin Requirements With SPI eFuse Switches* application brief.

2.2.7 Reset Aggregation

To perform a system reset, there are two switches located on the design. SW2 is for power-on reset (POR) and SW4 is for a warm reset of the MCU.

Figure 2-4 details the logic circuit that is used to determine which devices must be reset.

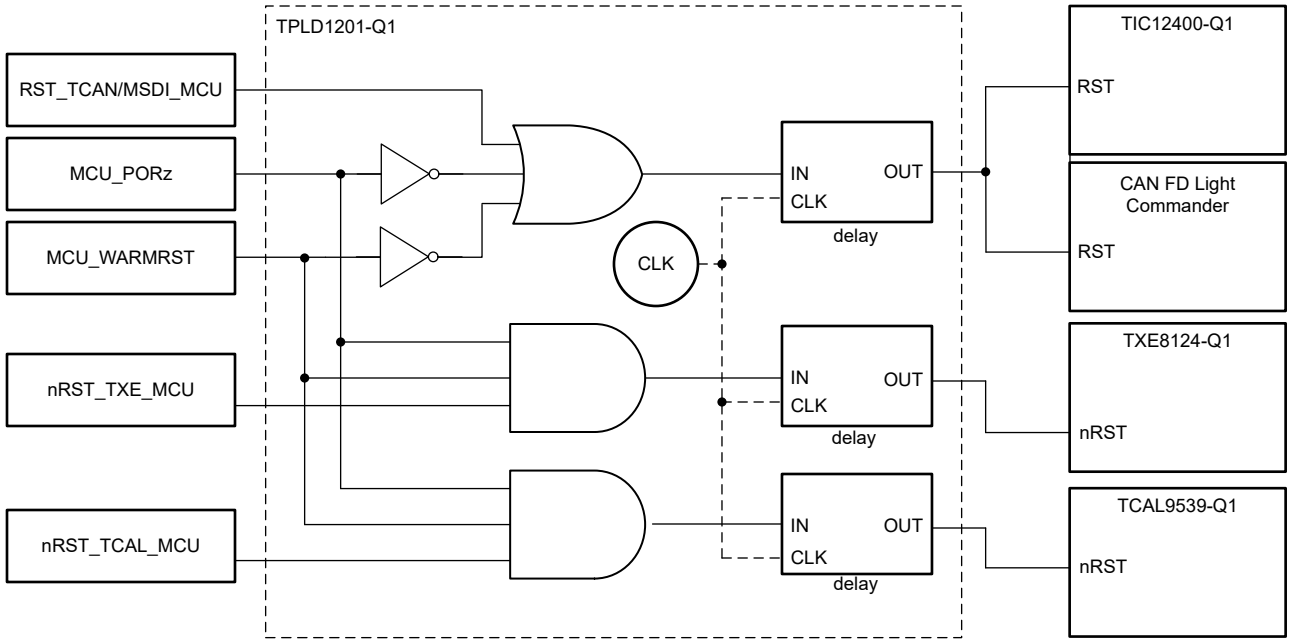


Figure 2-4. TPLD1201-Q1 Reset Circuit

2.3 Highlighted Products

2.3.1 AM263P4-Q1

The AM263P4-Q1 device is a quad-core Arm Cortex-R5F MCU for up to 400MHz with real-time control and expandable memory. The integrated Ethernet switch makes this MCU an excellent choice for Ethernet ring networking using MII, RMII, or RGMII. The AM263P4 is designed for the future of motor control with advanced analog sensing and digital actuation modules. This device also has a Hardware Security Manager (HSM) allowing for implementation of stringent security frameworks.

2.3.2 DP83TG721S-Q1

The DP83TG721S-Q1 is an automotive 1000BASE-T1 Ethernet PHY with TC-10, 802.1AS, advanced TSN, and AVB features. This device provides all physical layer functions needed to transmit and receive data with the flexibility to support RGMII and SGMII MAC interfaces. The DP83TG721S-Q1 supports OA TC10 low-power sleep with wake forwarding to reduce system power consumption when communication is not needed. This PHY integrates IEEE 1722 CRF decode to generate Media Clock, FSYNC, and SCLK for I2S and TDM8, making the device an excellent choice for AVB applications.

2.3.3 DP83TD555J-Q1

The DP83TD555J-Q1 is an IEEE802.3cg 10BASET1S and Open Alliance (OA) TC10, TC14 compliant Serial Peripheral Interface (SPI) MAC-PHY Ethernet transceiver. The device supports 10Mbps multi-drop or point-to-point half-duplex communication over unshielded twisted pair cables with extended common mode voltage tolerance. The device communicates to a host controller or switch using OA SPI. The DP83TD555J-Q1 integrates IEEE802.3 Media Access Controller (MAC) that enables microcontrollers with SPI to seamlessly connect to Ethernet networks using the 10BASE-T1S bus. The DP83TD555J-Q1 incorporates TC10 wake and sleep features to enable efficient system-level power consumption.

2.3.4 TPS653860-Q1

The TPS653860-Q1 is an automotive power management IC (PMIC) for safety-relevant applications for microcontrollers, sensors, transceivers, and peripherals. This device was developed with functional safety in mind, offering systematic capability and hardware integrity up to ASIL D. This PMIC is rated for 2.3V to 36V and 2.8A and has a synchronous buck-boost preregulator, four LDOs, and two additional protected LDOs for sensor or peripheral supplies.

2.3.5 TPS2HCS10-Q1

The TPS2HCS10-Q1 is an automotive, dual channel, 10mΩ smart high-side switch with I^2T wire protection, low I_Q mode, and SPI. This device supports an SPI-configurable capacitive charging mode for ECU loads in power distribution switch applications. This smart eFuse integrates a programmable fuse profile that turns off the switch under persistent overload conditions to reduce the overhead on the MCU.

2.3.6 TPS2HCS05-Q1

The TPS2HCS05-Q1 device is a dual-channel, smart high-side switch controlled through a serial peripheral interface (SPI) and is intended for power distribution and actuator drive applications. The device integrates robust protection to provide output wire and load protection against short circuit or overload conditions. The device features overcurrent protection configurable via SPI with sufficient flexibility to support loads that require large inrush currents and provide improved protection. The device also integrates a programmable fuse profile (current versus time) that turns off the switch under persistent overload condition. The two features together allow optimization of the wire harness for any load profile with full protection.

2.3.7 DRV8245S-Q1

The DRV8245S-Q1 is a SPI-controlled, fully integrated H-bridge driver for automotive applications. This device can be configured as a single full-bridge or two independent half-bridge drivers. The DRV8245S-Q1 integrates an N-channel H-bridge, chard pump regulator, high-side current sensing with regulation, current proportional output, and protection circuitry. The device has voltage monitoring, load diagnostics, and overcurrent and overtemperature protection.

2.3.8 TIC12400-Q1

The TIC12400-Q1 is an advanced Multiple Switch Detection Interface (MSDI) designed to detect external switch status in an automotive system. This device has an integrated 10-bit ADC to monitor multi-position analog switches and a comparator to monitor 24 digital switches independently of the MCU. The TIC12400-Q1 supports wake-up operation on all switch inputs to allow the MCU to shut down and can enter polling mode to periodically sample the input status for low-power-mode applications.

2.3.9 LM74900-Q1

The LM74900-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control with overcurrent and overvoltage protection. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) in case of overcurrent and overvoltage events using HGATE control.

2.3.10 LM74703-Q1

The LM74703-Q1 is an automotive AEC Q100 qualified ideal diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low-loss reverse polarity protection with a 20mV forward voltage drop.

2.3.11 INA186-Q1

The INA186-Q1 is an automotive, low-power, voltage output, current-sense amplifier (also called a current shunt monitor). This device is commonly used for monitoring systems directly connected to an automotive 12V battery. The INA186-Q1 can sense drops across shunts at common-mode voltages from –0.2V to +40V, independent of the supply voltage. In addition, the input pins have an absolute maximum voltage of 42V.

2.3.12 TPS7B81-Q1

The TPS7B81-Q1 is a low-dropout (LDO) linear regulator designed for up to 40V V_{IN} applications. With only a 2.7µA typical quiescent current at light load, the device is an optimum design for powering microcontrollers and controller area network and local interconnect network (CAN/LIN) transceivers in standby systems. The device features integrated short-circuit and overcurrent protection.

2.3.13 TPS3762-Q1

The TPS3762-Q1 is a 65V input voltage supervisor with 4µA IDD, 0.9% accuracy, fast detection time (5µs), and a Built-In Self-Test feature. This device can be connected directly to 12V, 24V automotive battery systems for continuous monitoring of overvoltage (OV) and undervoltage (UV) conditions; with the internal resistor divider, the TPS3762-Q1 offers the smallest total size. Wide hysteresis voltage options are available to ignore large voltage transients and prevent false reset signals.

2.3.14 TPS62903-Q1

The TPS62903-Q1 is a highly efficient, small, and flexible synchronous step-down DC/DC converter that is easy to use. A selectable switching frequency of 2.5MHz or 1.0MHz allows the use of small inductors and provides fast transient response. The device supports high VOUT accuracy of ± 1.5% across the entire operating temperature range and enhanced load transient performance with the DCS-Control topology. The wide 3V to 18V input voltage range supports a variety of nominal inputs, like 12V supply rails, single-cell or multicell Li-Ion, and 5V or 3.3V rails.

2.3.15 TPS62902-Q1

The TPS62902-Q1 is a highly efficient, small, and flexible synchronous step-down DC/DC converter that is easy to use. A selectable switching frequency of 2.5MHz or 1.0MHz allows the use of small inductors and provides fast transient response. The device supports high VOUT accuracy of ± 1.5% across the entire operating temperature range and enhanced load transient performance with the DCS-Control topology. The wide 3V to 18V input voltage range supports a variety of nominal inputs, like 12V supply rails, single-cell or multicell Li-Ion, and 5V or 3.3V rails.

2.3.16 TPS7B4256-Q1

The TPS7B4256-Q1 is a monolithic, integrated, low-dropout (LDO) voltage tracker. The device is available in 8-pin SOIC and HSOIC packages. The TPS7B4256-Q1 is designed to provide power supply to off-board sensors in an automotive environment. Because the risk of failure in cables that deliver off-board power is high, the device comes with integrated protection features against fault conditions such as short to battery, reverse polarity, output short to ground (current limit), and overtemperature (thermal shutdown). The device incorporates a back-to-back PMOS topology that eliminates the need for an external diode that is otherwise required to help protect against fault conditions that result in flow of reverse current. The device is designed to handle a 45V (absolute maximum) input voltage and survive the automotive load dump transient conditions.

2.3.17 TPS1211-Q1

The TPS1211-Q1 is a 45V, smart high-side driver with protection and diagnostics. The device has a strong 3.7A peak source (PU) and 4A peak sink (PD) gate driver that enables power switching using parallel FETs in high-current system designs. Use INP as the gate driver control input. The device has accurate current sensing (±2% at 30mV) output (IMON) enabling system designs for energy management. The device has integrated two-level overcurrent protection with FLT_I output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured. The device features remote overtemperature protection with FLT_T output. The TPS12111-Q1 integrates a pre-charge driver (G) with control input (INP_G). This features enables designs that must drive large capacitive loads. In shutdown mode (EN/UVLO < 0.3V), the controller draws a total shutdown current of 0.9µA (typical).

2.3.18 TPS1HC30-Q1

The TPS1HC30-Q1 device is a fully protected, high-side power switch with integrated NMOS power FET and charge pump, targeted for the intelligent control of the variable kinds of loads. Accurate current sense and programmable current limit features differentiate the device from the market.

2.3.19 TPS4HC120-Q1

The TPS4HC120-Q1 is an automotive quad-channel, smart high-side switch, with integrated NMOS power FET and charge pump, designed to meet the requirements of 12V automotive battery systems. The low RON (120mΩ) minimizes the device power dissipation when driving a wide range of output load current up to 2A when all four channels are enabled or 2.5A when only one channel is enabled. The device integrates protection features such as thermal shutdown, output clamp, and current limit. These features improve system robustness during fault events such as short circuit. The TPS4HC120- Q1 implements a selectable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The device offers 10 selectable current limit settings (0.25A to 5A) based on the external resistor used on the ILIM pin. The device also provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection, which enables better predictive maintenance.

2.3.20 TPS2HC08-Q1

The TPS2HC08-Q1 is a dual-channel, smart high-side switch, with integrated NMOS power FETs and charge pump, designed to meet the requirements of 12V automotive battery systems. The low R_{ON} (9.4mΩ) minimizes device power dissipation when driving a wide range of output load current up to 7.5A DC when both channels are enabled or 10A DC when only one channel is enabled. The device integrates protection features such as thermal shutdown, output clamp, and current limit. TPS2HC08-Q1 implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current

2.3.21 TPS1HC04-Q1

TPS1HC04-Q1 is a single-channel, smart high-side switch, with integrated NMOS power FET and charge pump, designed for 12V automotive battery systems. The low on-resistance (4.9mΩ) minimizes device power dissipation when driving a wide range of output load current up to 15A DC. The device integrates protection features such as thermal shutdown, output clamp, and current limit. TPS1HC04-Q1 implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The adjustable current limit can be adjusted from (15A to 45A) using an external resistor on the ILIM pin. The device offers both thermal-regulated current limiting for capacitive loads at start-up and non-regulated current limiting for motor inrush or bulb applications

2.3.22 DRV8714S-Q1

The DRV871x-Q1 family of devices are highly integrated, multichannel gate drivers intended for driving multiple motors or loads. The devices integrate either 4 (DRV8714-Q1) or 8 (DRV8718-Q1) half-bridge gate drivers, driver power supplies, current shunt amplifiers, and protection monitors reducing total system complexity, size, and cost. A smart gate drive architecture manages dead time to prevent shoot-through, controls slew rate to decrease electromagnetic interference (EMI), and optimizes propagation delay for enhanced performance. Input modes are provided for independent half-bridge or H-bridge control. Four PWM inputs can be multiplexed between the different drivers in combination with SPI control.

2.3.23 DRV8145S-Q1

The DRV814x-Q1 family of devices is a fully integrated half-bridge driver intended for a wide range of automotive applications. Designed in a BiCMOS high power process technology node, this monolithic family of devices in a power package offer excellent power handling and thermal capability while providing compact package size, ease of layout, EMI control, accurate current sense, robustness, and diagnostic capability. This family provides an identical pin function with scalable R_{ON} (current capability) to support different loads.

2.3.24 DRV81602-Q1

The DRV81602-Q1 is an 8-channel low and high-side driver with protection and diagnostics. The device is designed to control relays, LEDs, lamps and motors. A serial peripheral interface (SPI) with daisy chain is utilized for control and diagnosis of the loads and the device. Two input pins with mapping functionality allow direct control of the outputs. The device supports Limp Home for fail-safe activation. Integrated PWM generators enable driving LEDs, and bulb inrush mode enables driving loads with large capacitance. Clamp circuits on each output dissipates the energy during turning OFF inductive loads. The device supports various protection features such as undervoltage, overvoltage, short circuit and open load detection. A high level of integration with embedded protection and diagnostic features make the DRV81602-Q1 an excellent choice for automotive body and powertrain applications.

2.3.25 TPS1214-Q1

The TPS1214-Q1 is a low IQ smart high side driver with protection and diagnostics. It has two integrated gate drives with 0.5A source and 2A sink (GATE) and 100µA source and 0.39A sink (G). With LPM Low, the low power path is kept ON and the main FETs are turned OFF with I_Q of 20µA (typ). Auto load wakeup threshold adjusted using RBYPASS resistor placed across CS2+ and CS2–. IQ reduces to 1µA (typ) with EN/UVLO low. The device has accurate current sensing (±2%) output (IMON) with adjustable I2t based overcurrent and short circuit protection using an external RSNS resistor and FLT indication. Auto-retry and latch-off fault behavior can be configured. The device also has NTC based temperature sensing (TMP) and monitoring output (ITMPO) output for overtemperature detection of external FETs.

2.3.26 TCAN1043A-Q1

The TCAN1043A-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification. The device supports both classical CAN and CAN FD data rates up to 8 megabits per second (Mbps) (TCAN1043A-Q1) or 5Mbps (TCAN1043AT-Q1). The TCAN1043A-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system through the INH output pin. This allows a low-current sleep state in which power is gated to all system components except for the TCAN1043A-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN1043AQ1 initiates system start-up by driving INH high. The TCAN1043A-Q1 features an SWE timer that enables a safe transition to Sleep mode after 4 minutes ($t_{INACTIVE}$) of inactivity in Standby mode. Making sure the device is transitioned to low-power Sleep mode if the MCU fails to transition the device to Normal mode.

2.3.27 TCAN1044-Q1

The TCAN1044-Q1 is a high-speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification. The TCAN1044-Q1 transceiver supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps). The TCAN1044V-Q1 includes internal logic level translation with the VIO pin to allow for interfacing the transceiver I/O directly to 1.8V, 2.5V, 3.3V, or 5V logic levels. The transceiver supports a low-power standby mode and wake over CAN compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP). The TCAN1044-Q1 transceiver also includes protection and diagnostic features supporting thermal-shutdown (TSD), TXD dominant time-out (DTO), supply undervoltage detection, and bus fault protection up to ±58V.

2.3.28 TCAN1046V-Q1

The TCAN1046V-Q1 is a dual, high-speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification. The TCAN1046V-Q1 transceiver supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps). The TCAN1046V-Q1 includes internal logic level translation via the VIO terminal to allow for interfacing the transceiver IOs directly to 1.8V, 2.5V, 3.3V, or 5V logic IOs. The two CAN channels support independent mode control through the standby pins. This provides the ability to place each transceiver into the low-power state, standby mode, without impacting the state of the other CAN channel. While in standby mode the TCAN1046V-Q1 supports remote wake-up through the ISO 11898-2:2016 defined wake-up pattern (WUP). The TCAN1046V-Q1 transceivers also include many protection and diagnostic features including thermal shutdown (TSD), TXD dominant timeout (DTO), supply undervoltage detection, and bus fault protection up to ±58V.

2.3.29 SN3257-Q1

The SN3257-Q1 is an automotive grade complementary metal-oxide semiconductor (CMOS) switch that supports high speed signals with low propagation delay. The SN3257-Q1 offers a 2:1 (SPDT) switch configuration with 4-channels making the device and excellent choice for multilane protocols such as SPI and I2S. The device supports bidirectional analog and digital signals on the source (SxA, SxB) and drain (Dx) pins and can pass signals above supply up to VDD × 2, with a maximum input and output voltage of 5.5V. The SN3257-Q1 has an active low EN pin that is used to enable and disable all channels simultaneously. When the EN pin is LOW, one of the two switch paths is selected based on the state of SEL pin. Powered-off protection up to 3.6V on the signal path of the SN3257-Q1 provides isolation when the supply voltage is removed (VDD = 0V). Without this protection feature, switches can back-power the supply rail through an internal ESD diode and cause potential damage to the system. Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pin, protecting the device from potential damage. Both logic control inputs have 1.8V logic compatible thresholds, providing both TTL and CMOS logic compatibility. Integrated pulldown resistor on the logic pins removes external components to reduce system size and cost.

2.3.30 TLIN1021A-Q1

The TLIN1021A-Q1 is a local interconnect network (LIN) physical layer transceiver. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol, that supports automotive in vehicle networking. The TLIN1021A-Q1 transmitter supports data rates up to 20kbps. The transceiver controls the state of the LIN bus through the TXD pin and reports the state of the bus on the open-drain RXD output pin. The device has a current-limited wave-shaping driver to reduce electromagnetic emissions (EME). The TLIN1021A-Q1 is designed to support 12V applications with a wide input voltage operating range. The device supports low-power sleep mode, as well as wake-up from low-power mode through wake over LIN, the WAKE pin, or the EN pin. The device allows system-level reductions in battery current consumption, by selectively enabling the various power supplies that can be present on a node through the TLIN1021A-Q1 INH output pin.

2.3.31 TLIN1024A-Q1

The TLIN1024A-Q1 is a Quad Local Interconnect Network (LIN) physical layer transceiver with integrated wake-up and protection features, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4 standards. LIN is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20kbps. The TLIN1024A-Q1 is designed to support 12V applications with wider operating voltage and additional bus-fault protection. The TLIN1024A-Q1 receiver supports data rates up to 100kbps for faster in-line programming. The TLIN1024A-Q1 converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin. Ultra-low current consumption is possible using the sleep mode which allows wake-up via LIN bus or EN pin.

2.3.32 TAS6754-Q1

The TAS6754-Q1 is a four-channel digital-input Class D audio amplifier that implements 1L modulation only requiring one inductor per BTL channel reducing system size and cost by removing four inductors compared to a traditional design. Additionally, 1L modulation lowers switching losses compared to traditional Class-D modulation schemes. The TAS6754-Q1 integrates DC and AC Load Diagnostics to determine the status of the connected loads. During audio playback this status can be monitored through output current sense which is available for each channel and reports the measurement to a host processor through TDM with minimal delay. The device monitors the output load condition while playing audio through real-time load diagnostics independent of the host and audio input. The TAS6754-Q1 device features an additional low latency signal path for each channel, providing up to 70% faster signal processing at 48kHz which enables time-sensitive Active Noise Cancellation (ANC), Road Noise Cancellation (RNC) applications.

2.3.33 TMUX1308-Q1

The TMUX1308-Q1 is a general purpose complementary metal-oxide semiconductor (CMOS) multiplexer (MUX). The TMUX1308-Q1 is an 8:1, 1-channel (single-ended) MUX, while the TMUX1309-Q1 is a 4:1, 2-channel (differential) MUX. The devices support bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from GND to VDD.

2.3.34 TPLD1201-Q1

The TPLD1201-Q1 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks. TPLD provides a fully integrated, low-power approach to implement common system functions, such as timing delays, voltage monitors, system resets, power sequencers, I/O expanders, and more. This device features configurable I/O structures that extends compatibility within mixed-signal environments, reducing the number of discrete components required. System designers can create circuits and configure the macro-cells, I/O pins, and interconnections by temporarily emulating the non-volatile memory or by permanently programming the one-time programmable (OTP) through Inter-Connect Studio. The TPLD1201-Q1 is supported by a hardware and software ecosystem with application notes, reference designs, and design examples. Visit ti.com for more information and access to design tools.

2.3.35 SN74CBTLV3861-Q1

The SN74CBTLV3861 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as one 10-bit bus switch. When output enable (OE) is low, the 10-bit bus switch is on, and port A is connected to port B. When OE is high, the switch is open, and the high-impedance state exists between the two ports. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature makes sure that damaging current does not backflow through the device when powered down. The device has isolation during power off. To make sure the high-impedance state during power up or power down, tie OE to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

2.3.36 TXE8124-Q1

The TXE81XX-Q1 devices provide general purpose parallel input/output (I/O) expansion for the four wire Serial Peripheral Interface (SPI) protocol and is designed for 1.65V to 5.5V VCC operation. The device supports 10MHz from 3.3V to 5.5V and 5MHz from 1.65V to 5.5V. I/O expanders, such as the TXE81XX-Q1, provide a simple approach when additional I/Os are needed for switches, sensors, push-buttons, LEDs, and fans. The TXE81XX-Q1 devices have I/O ports, which include additional features designed to enhance the I/O performance in terms of speed, power consumption, and flexibility. The additional features are: enable/disable pullup and pulldown resistors, latchable inputs, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs, and a fail-safe register mode which is enabled by the FAIL-SAFE pin.

2.3.37 TCAL9539-Q1

The TCAL9539-Q1 device provides general purpose parallel input/output (I/O) expansion for the two-line bidirectional I2C bus (or SMBus) protocol and is designed for 1.08V to 3.6V VCC operation. The device supports 100kHz (Standard-mode), 400kHz (Fast-mode), and 1MHz (fast-mode-plus) I 2C clock frequencies. I/O expanders such as the TCAL9539-Q1 provide a simple approach when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and so on. The TCAL9539-Q1 has Agile I/O ports which include additional features designed to enhance the I/O performance in terms of speed, power consumption and EMI. The additional features are: programmable output drive strength, programmable pullup and pulldown resistors, latchable inputs, maskable interrupt, interrupt status register, and programmable open.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The following hardware is required to use the TIDA-020079:

- TIDA-020079 zone reference design
- 12V power supply
- XDS110ISO-EVM: used for programming the AM263P-Q1 MCU

3.2 Software Requirements

This design includes firmware for testing the different features. To view this firmware, request access to the *Secure resources* folder.

3.3 Test Setup

Figure 3-1 shows the typical setup for the TIDA-020079-Q1. A 12V power supply source must be provided to 12V_1 to completely power all components on the design. 12V_2 is used as a redundant power port.

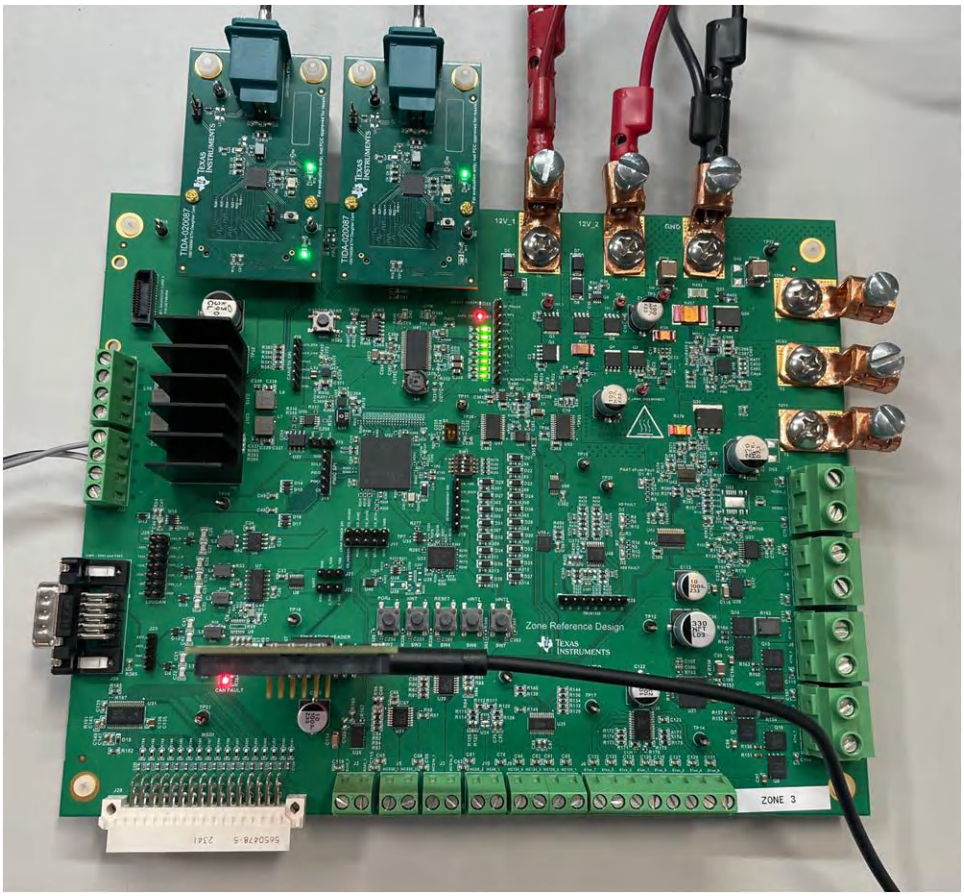


Figure 3-1. TIDA-020079 Board Setup

When using the XDS110-ISO EVM, the TIDA-020079 firmware can be loaded onto the AM263P-Q1. The TIDA-020079 firmware contains different tests for testing each feature set included in Figure 3-2.

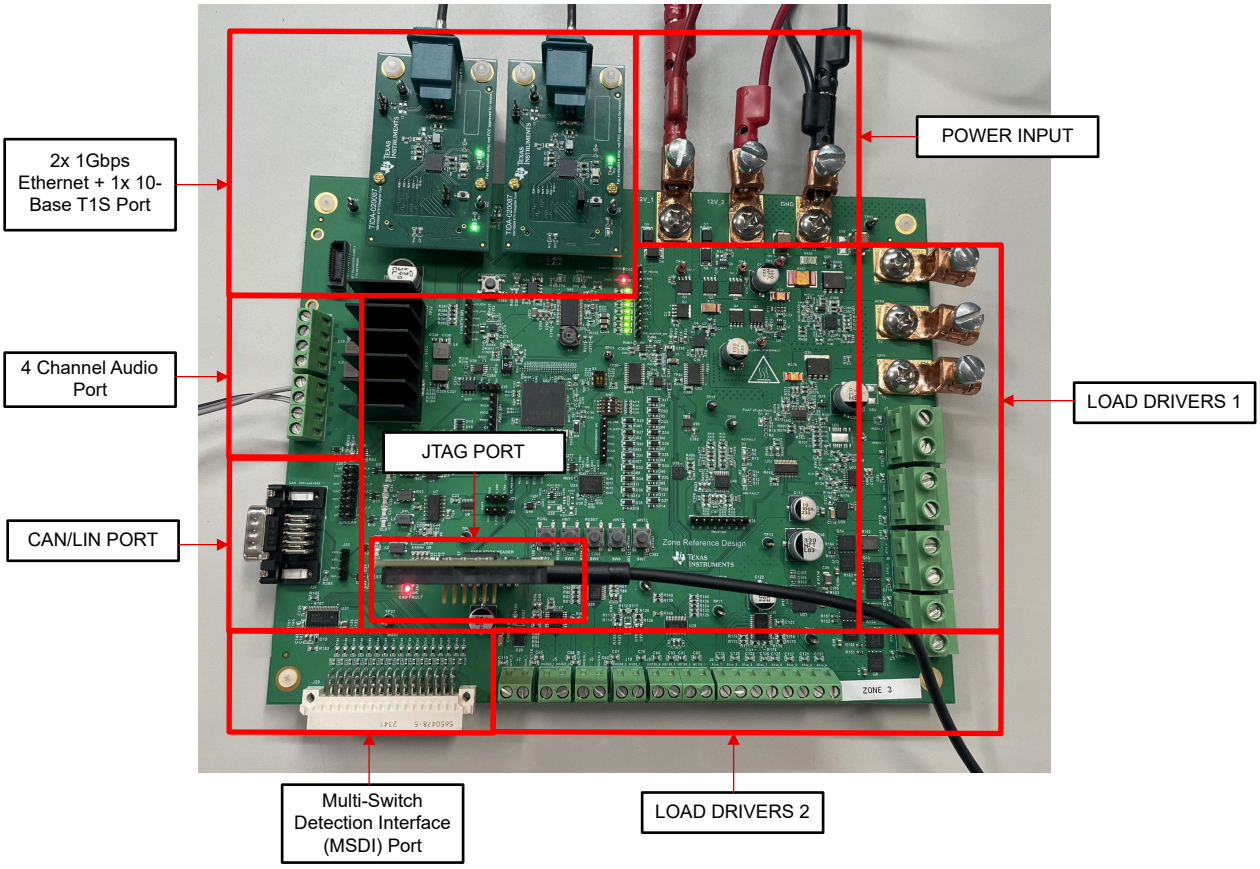


Figure 3-2. TIDA-020079 Feature Map

3.4 Test Results

3.4.1 Redundant Input Supply

This reference design features redundant input supplies, protected by ideal diode controllers.

This system operation is designed so that when the zone transitions to low power mode, only one of the 12V input supplies continues to deliver power to downstream loads, while the other is shut off. In this test, one 12V supply is shut off to simulate the loss of a power supply, while the second power supply is kept on. The 12V rails are monitored on an oscilloscope. Figure 3-3 shows that when supply one is shut off, the second supply continues to power the 12V rail for downstream loads without any interruption.

In a more comprehensive system, the module software must consider the load currents of all of the outputs to avoid overloading the remaining supply.

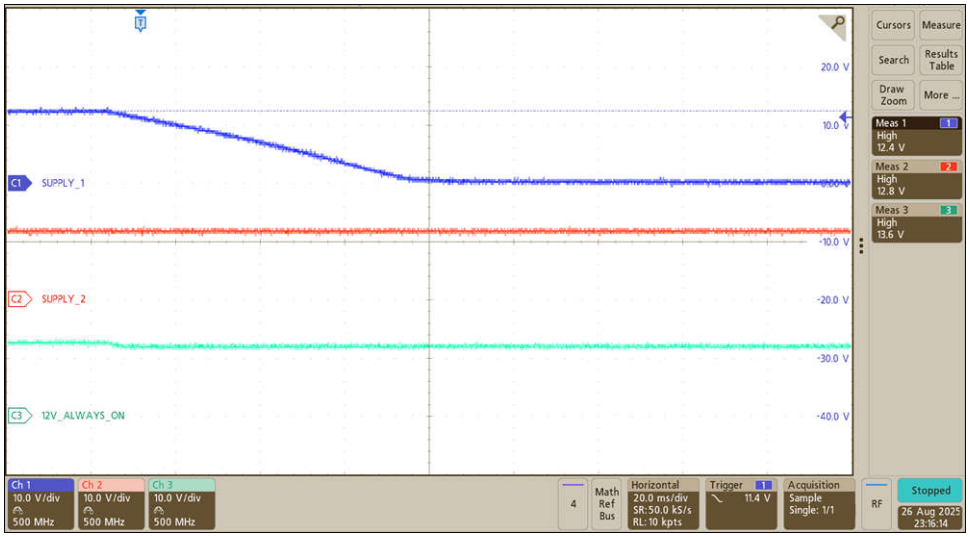


Figure 3-3. Redundant Supply Test

3.4.2 Power Sequence

This test covers how long the TIDA-020079 takes to fully wake up from OFF state. The 12V_always_on rail supplies power to the PMIC (TPS653860-Q1), always on LDO (TPS7B8133-Q1) and a 5V tracking LDO (TPS7B4256-Q1). The PMIC provides a 6V buck-boost output (6V0_BB) which then supplies a 1.2V buck converter (TPS62903-Q1) and a 1.1V buck converter (TPS62902-Q1). The 6V buck-boost output also supplies several PMIC LDOs including 3.3V LDO1 (3V3_1), 3.3V LDO2 (3V3_2), 5V LDO1 (5V0_1), 1.8V LDO (1V8), 5V LDO2 (5V0_2), and an unused 5V LDO (PLDO2_OUT).

The PMIC is configured by a one-time programmable (OTP) setting and with an SPI. For this design, the OTP is configured to power on 6V0_BB, 3V3_1, and to enable the 1.1V and 1.2V rails. 3V3_1 and 1.2V are needed to power on the MCU. When the MCU is on, the other PMIC rails are turned on with an SPI.

The power sequence test starts with the board completely powered off. When powered on, WAKE1 and WAKE2 are asserted on the PMIC, which transitions the PMIC from OFF state to Active state. The power rails shown in Figure 2-1 then power up starting with the 6V buck-boost pre-regulator.

The resulting wake sequence is split up into two scopeshots. Figure 3-4 shows the power rails enabled by default, either by the PMIC OTP settings or the 12V always-on domain. In Figure 3-5, all PMIC rails enabled by software (except A0 and A1) are shown, with timings based on the one-time programmable settings.

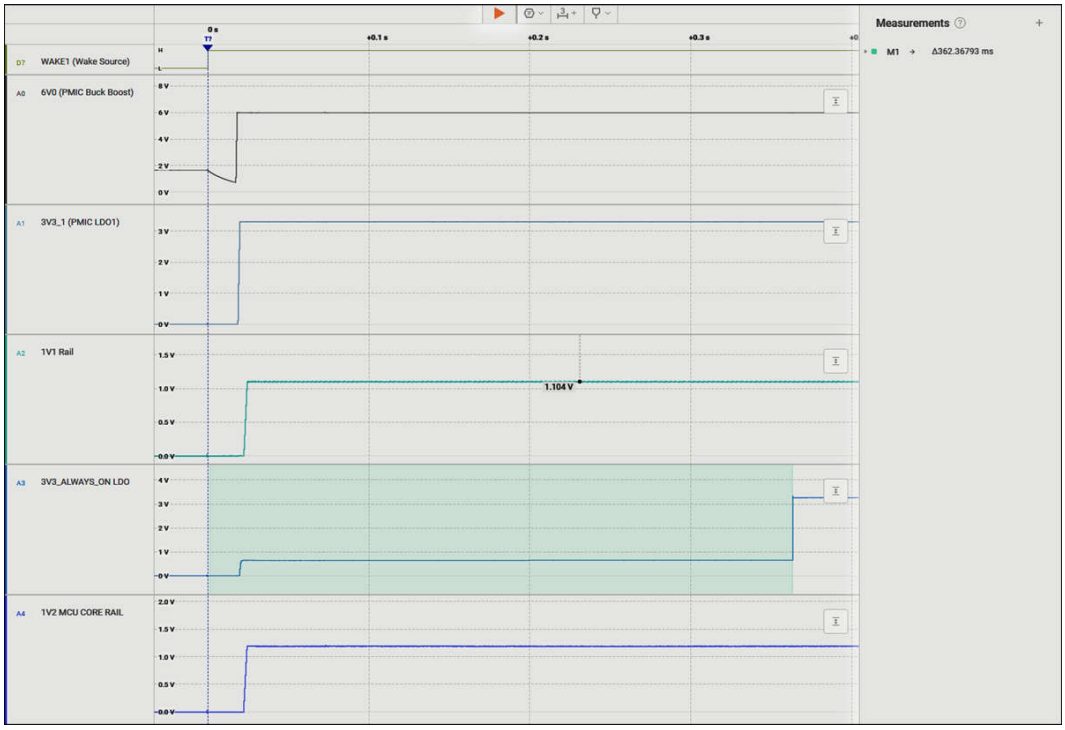


Figure 3-4. Power Sequence (Wake Start)

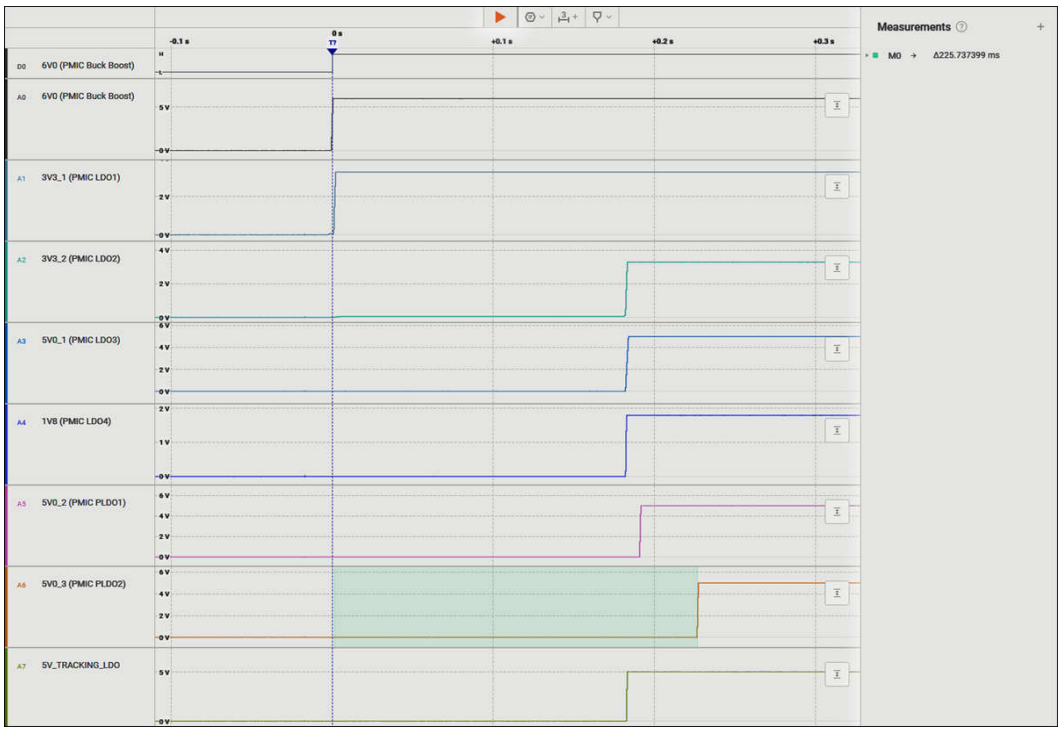


Figure 3-5. Power Sequence 2 (End of Wake Sequence)

As shown above, most of the PMIC rails go high at approximately the same time after 180ms. PLDO2 goes high at the 225ms mark because PLDO2 is the last rail enabled by software. PLDO2 is enabled after all of the MCU peripheral drivers are setup.

3.4.3 Reset Aggregation

To test the system reset circuit achieved using TPLD1201-Q1, some tests are performed by analyzing how different reset sources reset difference parts of the circuit. The main components considered for reset are the IO expanders and CAN FD Light Commander.Figure 2-4 shows the TPLD1201-Q1 reset circuit.

These tests consisted of pulling various signals high or low depending on whether a reset signal of a component operates active high or low. The TXE8124-Q1 and TCAL9539-Q1 operate active low and the TIC12400-Q1 is active high.

In the first test shown in Figure 3-6, NRST_TXE_MCU is pulled low by the MCU. As shown by the digital logic, only the TXE8124-Q1 resets after the appropriate delay set in the TPLD1201-Q1.

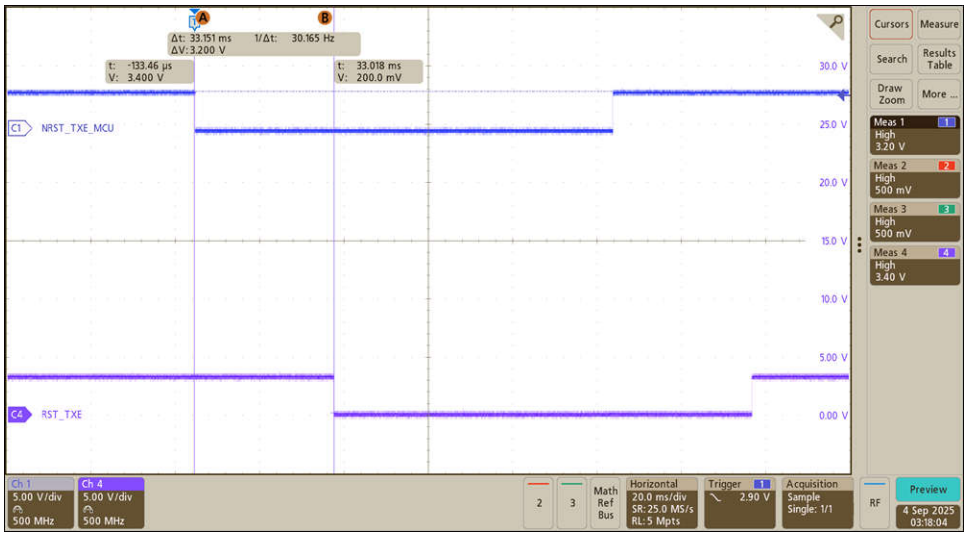


Figure 3-6. TXE Reset

In the second test detailed in Figure 3-7, PORZ is pulled low which triggers reset on the MCU and IO expanders. In this scope shot specifically, only TIC12400-Q1 is shown being reset.

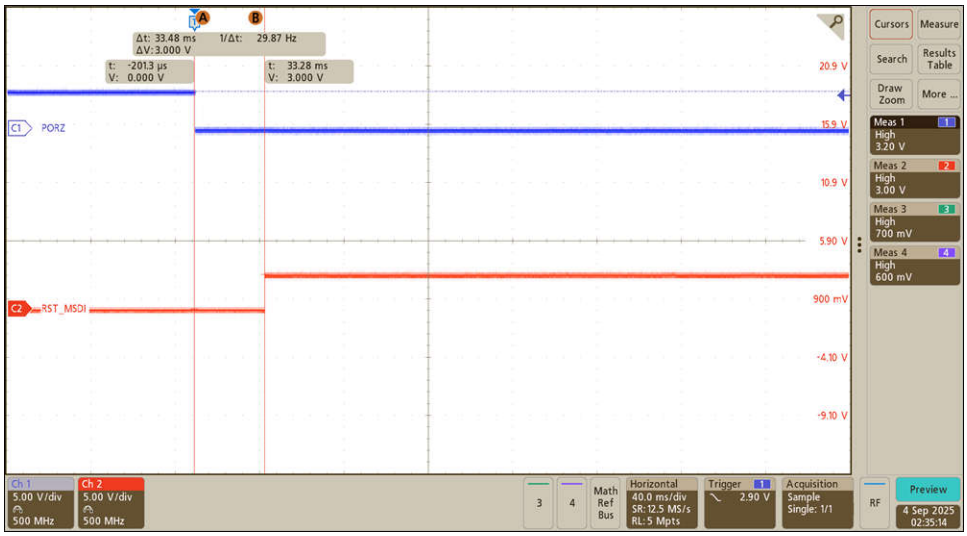


Figure 3-7. PORZ Reset

In the final test shown in Figure 3-8, a warm reset event is triggered on the MCU which pulls the WARMRST input low after a delay set in the TPLD1201-Q1. Although this similarly triggers reset on all components, resetting all IO Expanders to default states, a difference exists between PORZ and WARMRST. PORZ completely clears all register content and emulates the board state when the board recovers from loss of power. Conversely, WARMRST partially resets some registers on the MCU and resets all registers of the IO Expanders.

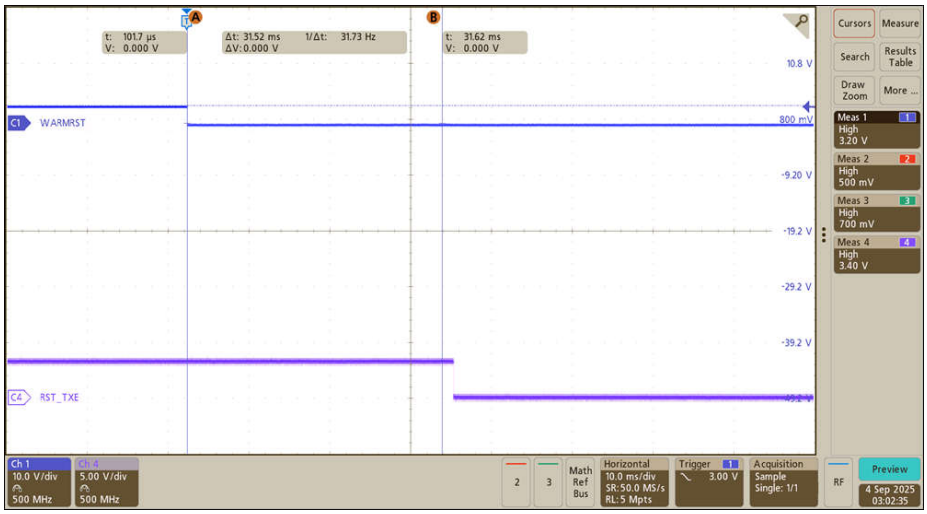


Figure 3-8. WARM RST

3.4.4 Low Power Mode Tests

Low power mode is crucial for conserving power during key-off or parked states especially for electric vehicles. The system stays in this low quiescent current state until a given event prompts the zone to wake up temporarily to respond either by supplying more power to ECUs, running a comprehensive software algorithm, or any response which requires full power. The following are typical events in a zone control module which prompt the system to transition to the main power state:

- CAN wakeup
- LIN wakeup
- Ethernet wakeup
- High-side switch, smart eFuse wakeup
- IO Expander wakeup
- Supervisor or system diagnostic wakeup

Although the AM263P-Q1 does not have a low power mode available, the system satisfies this requirement by shutting off the PMIC rails and all of the components powered by the 12V load disconnect rail to minimize Iq. This means the MCU is off in low power mode. Wake-up signals from certain components powered by the 12V and 3.3V always-on rails are monitored by a TPLD low power mode circuit to consider different wake-up events.

3.4.4.1 Low Power Mode Quiescent Current

Table 3-1 shows a summary of the total current consumption across the different always-on components in low power mode.

Table 3-1. Low Power Mode I_Q Distribution

DEVICE	SUBSYSTEM	COUNT ON BOARD	POWER RAIL	I_Q (µA)
LM74704-Q1	Power (ideal diode controller)	1	VBAT	80
TPS653860-Q1	Power (PMIC)	1	VBAT	45
TPS7B81-Q1	Power (3.3V always-on LDO)	1	VBAT	2.7
TCAN1043-Q1	CAN	1	VBAT	15
TLIN1021A-Q1	LIN	1	VBAT	9
DP83TG721-Q1	Ethernet	2	VSLEEP	16
TPS2HCSxx-Q1	Load Driver	2	VBAT	4.5
			VDD	14
TPS1214-Q1	Load Driver	1	VBAT	20
TPS4HC120-Q1	Load Driver	1	VBAT	20µA per channel (80µA with all channels)
TIC12400-Q1	IO Expansion	1	VBAT	7.5
			VDD	1.5
Total Expected				460.7µA

The measured low power mode current is 512.6µA. The measured value is slightly higher than the expected value due to additional passives and resistor dividers.

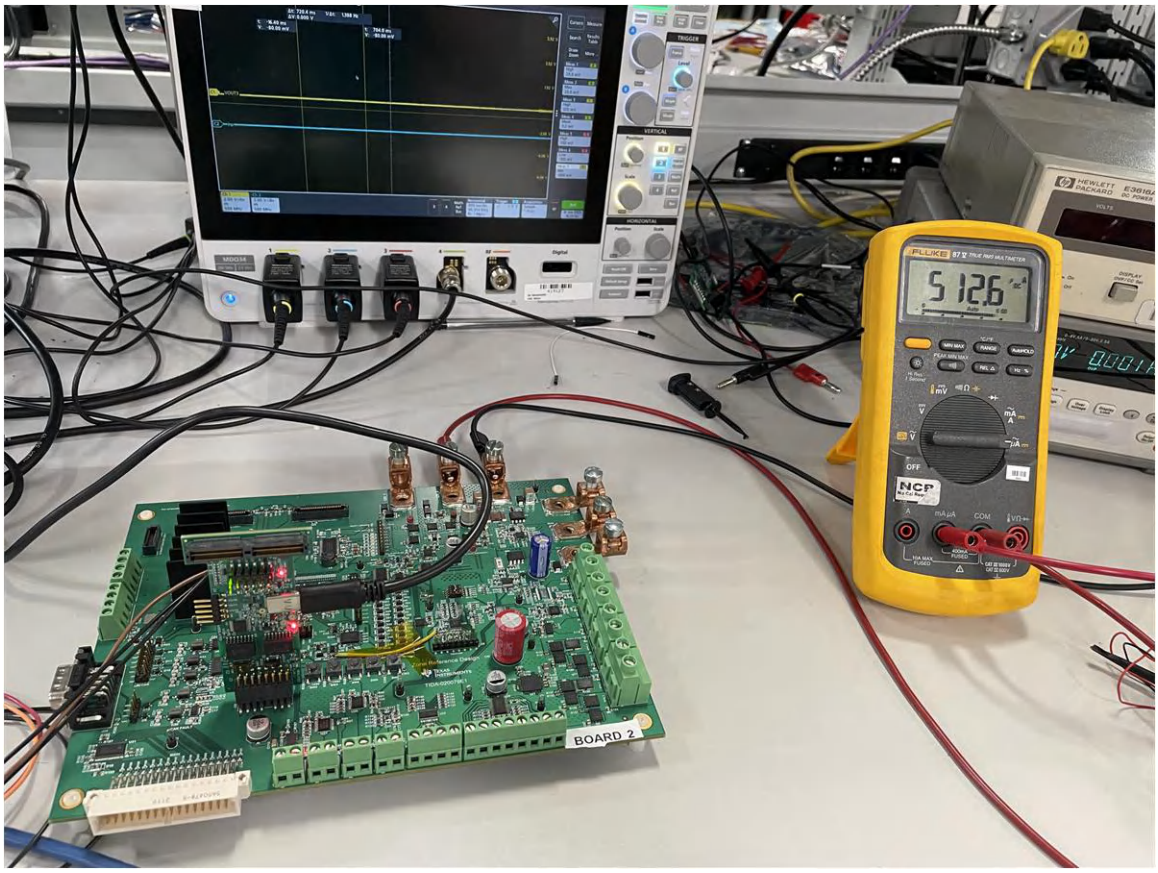


Figure 3-9. TIDA-020079 Low Power Mode Quiescent Current

3.4.4.2 Wake Measurement Results

This section details the system wake-up times measured for several different wake-up events included in Table 3-2. Note that these wake-up times are primarily influenced by the PMIC, which has two different settings for wake deglitch time. WAKE1 is configured for a deglitch time of 16ms, and WAKE2 is configured for a deglitch time of 2ms.

The wake time for all of these measurements is captured by measuring the time from wake source assertion to the PMIC buck-boost converter turning on.

Table 3-2. Wakeup Measurement Summary

DEVICE	WAKE SIGNAL	MINIMUM WAKE TIME (PMIC WAKE DEGLITCH TIME)	SYSTEM WAKE TIME
TCAN1043-Q1	Wake 1	16ms	18ms
TLIN1021-Q1	Wake 1	16ms	17.6ms
TPS1214-Q1	Wake 2	2ms	3.6ms
DP83TG721-Q1	Wake 2	2ms	About 3.6ms (Not tested)
TPSxHCSxx-Q1	Wake 2	2ms	3.637ms
TPS4HC120-Q1	Wake 2	2ms	3.561ms
TIC12400-Q1	Wake 2	2ms	About 3.6ms (Not tested)
TPS3762-Q1	Wake 2	2ms	About 3.6ms (Not tested)

3.4.4.3 CAN Wake

The first wake-up source test uses CAN wakeup. During low power mode, the CAN bus remains in a recessive state because all nodes operate in low power mode. An edge node can send a message to the TCAN1043-Q1 on the zone control module to start the wake-up sequence.

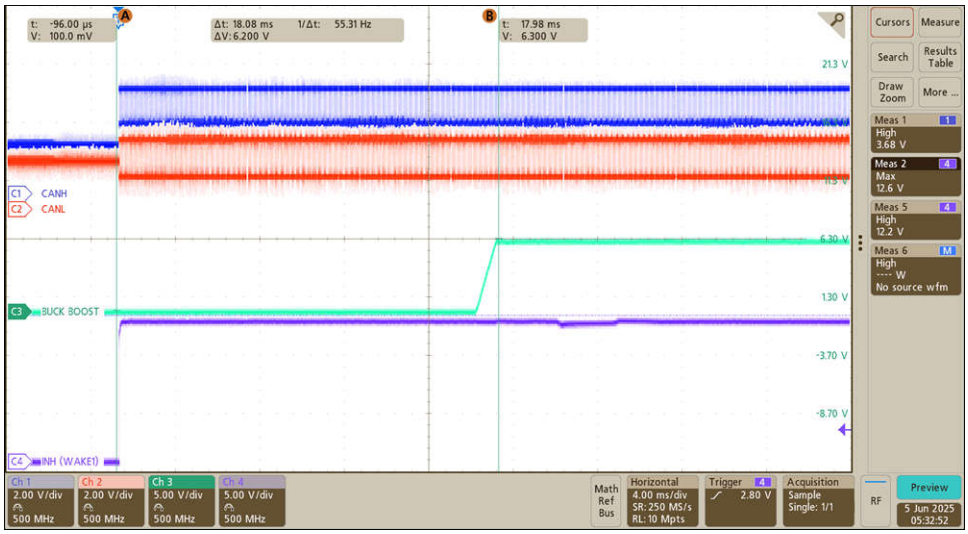


Figure 3-10. CAN Wakeup

3.4.4.4 LIN Wake

Figure 3-11 shows an example of a LIN wakeup using TLIN1021A-Q1. During low power mode, the LIN bus is kept in a recessive state (high); however, any connected LIN node can pull the LIN bus to a dominant state (low). The LIN bus is pulled low for 50µs to transition TLIN1021A-Q1 to active mode, which pulls Wake 1 high and wakes up the PMIC after about 18ms. In this case, all LIN nodes and zone control module are expected to be ready to communicate after 18ms.

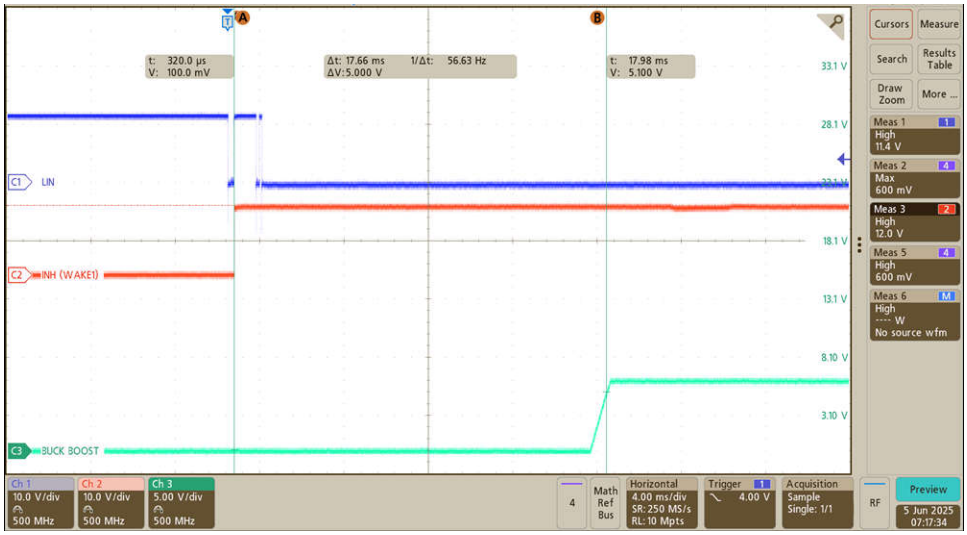


Figure 3-11. LIN Wakeup

3.4.4.5 High-Side Switch Controller Wake

The TPS1214-Q1 can automatically wake up the system when load current increases on the device output during low power mode. This load wake-up event connects the WAKE pin of the TPS1214-Q1 to a logic circuit built into a TPLD1201-Q1. When load current increases, the WAKE pin goes low, which triggers the TPLD circuit to pull the PMIC wake high and power up the MCU. During system wakeup, the TPS1214-Q1 automatically transitions from using the bypass path to the active path to support full load operation.

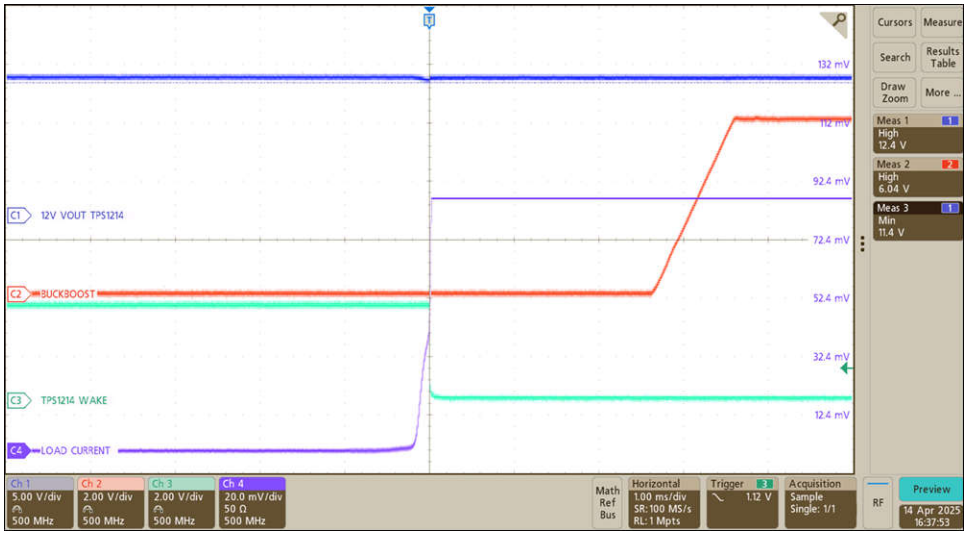


Figure 3-12. TPS1214-Q1 Automatic Load Wakeup

3.4.4.6 Smart eFuse Wake

The TPS2HCS10-Q1 can automatically wake up the MCU when load current increases on either device output during LPM. This load wake-up event connects the nFLT pin of the TPS2HCS10-Q1 to a logic circuit built into a TPLD1201-Q1. When load current increases, the nFLT pin goes low which triggers the TPLD circuit to pull the PMIC wake high. During system wakeup, the TPS2HCS10-Q1 automatically transitions from delivering current to the load from the bypass path to the active path, which supports full load operation.

The TPS2HCS10-Q1 requires additional logic within the TPLD1201-Q1 to wake up the MCU when compared to other load drivers. When the TPS2HCS10-Q1 sees load current increase at either output, the nFLT pin goes low for 100µs, thus the TPLD1201-Q1 output remains high for 100µs as well. However, the PMIC requires a minimum 2ms pulse on the WAKE pin to wake up due to the configured glitch time. To overcome this challenge,

additional logic within the TPLD1201-Q1 is added to capture the transition of the TPS2HCS10-Q1 nFLT pin on the falling edge from high to low by latching this value for 3ms.

By latching the TPLD1201-Q1 wake output high for well above the PMIC required pulse time, the system can now wake up with TPS2HCS10-Q1. Figure 3-13 shows the nFLT pin of the TPS2HCS10-Q1 transitioning high to low when the device sees an increase in output current, and the TPLD holds the output high for a time of 3ms to trigger the PMIC WAKE.

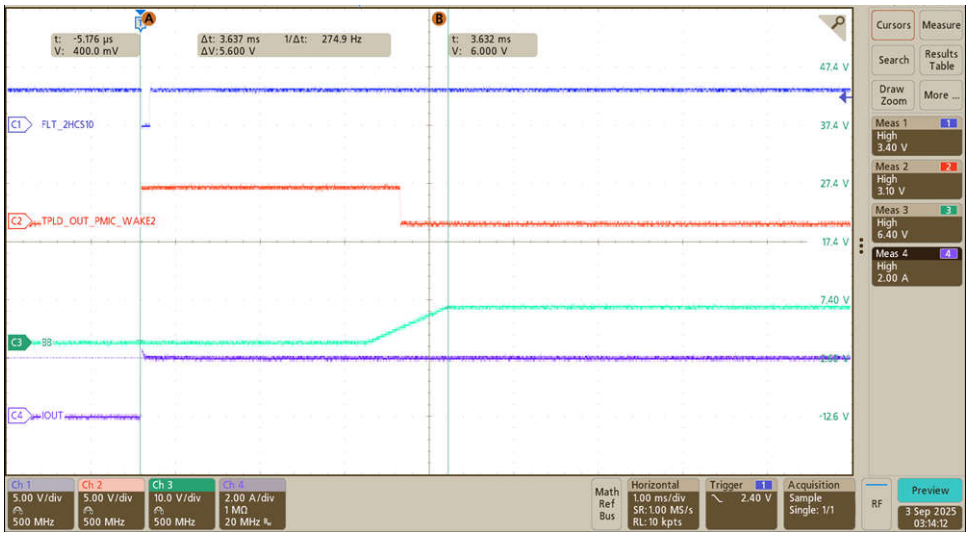


Figure 3-13. TPS2HCS10-Q1 Automatic Load Wakeup

3.4.4.7 High-Side Switch Wake

Simpler high-side switches can also wake up the system. The TPS4HC120-Q1 wakes up the system when load current increases on any of the four outputs during low power mode. This load wake-up event occurs by connecting the nLPM pin of the TPS4HC120-Q1 to a logic circuit built into a TPLD1201-Q1 when load current increases. When the nLPM pin goes low, this triggers the TPLD circuit to pull the PMIC wake high. During system wakeup, the TPS4HC120-Q1 outputs automatically transition from delivering current to the load from the bypass path to the active path, which supports full load operation.

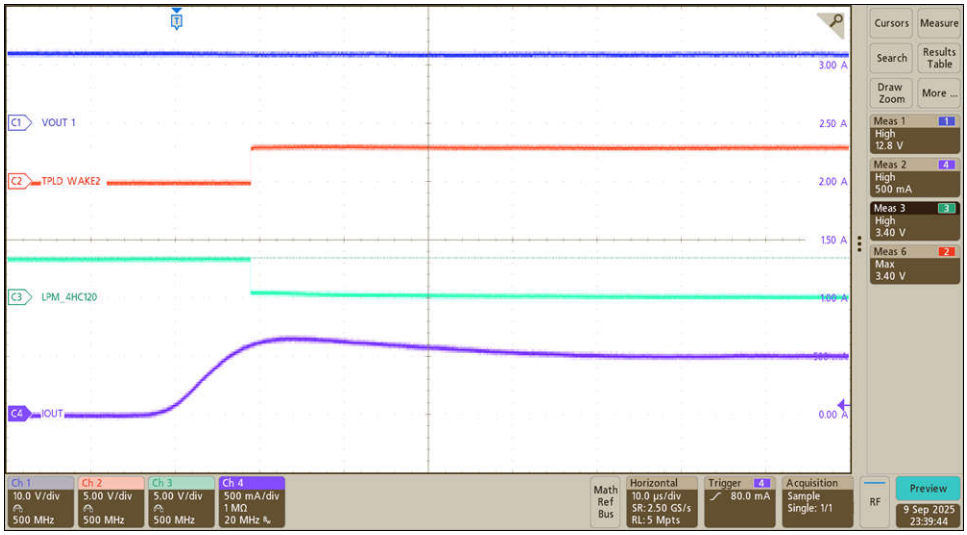


Figure 3-14. TPS4HC120-Q1 Automatic Load Wakeup

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-020079.

4.1.2 Layout

To download the layout, including layer plots, Gerber files, and assembly files, see the design files at TIDA-020079.

4.1.3 BOM

To download the bill of materials (BOM), see the design files at TIDA-020079.

4.2 Tools and Software

Tools

Code Composer Studio	Code Composer Studio™ integrated development environment (IDE)
SYSCONFIG	System Configuration Tool
TPLD-ICS	InterConnect Studio for TI Programmable logic devices

Software

To download the TIDA-20079 firmware, request access to the *Secure resources* folder.

AM263P4-Q1 SDK	AM263Px software development kit (SDK) for Sitara™ microcontrollers

4.3 Documentation Support

1. Texas Instruments, *Software-Defined Vehicles Shift the Future of Automotive Electronics Into Gear Marketing White Paper*
2. Texas Instruments, *How a Zone Architecture Paves the Way to a Fully Software-Defined Vehicle Marketing White Paper*
3. Texas Instruments, *Zone architecture, Ethernet drive vehicle of the future Technical Article*
4. Texas Instruments, *DP83TC812-Q1 TC10 System Timing Measurements Application Note*
5. Texas Instruments, *Zonal Architecture and MCU I/O Expansion Application Brief*
6. Texas Instruments, *Priority Power MUX Using Ideal Diodes in Automotive Zonal Modules Application Brief*
7. Texas Instruments, *Reducing System Bill of Materials and MCU Pin Requirements With SPI eFuse Switches Application Brief*
8. Texas Instruments, *AM263Px Sitara™ Microcontrollers with Optional Flash-in-Package Datasheet*
9. Texas Instruments, *DP83TG721x-Q1 1000BASE-T1 Automotive Ethernet PHY with Advanced TSN and AVB Datasheet*
10. Texas Instruments, *DP83TD555J-Q1 Automotive 10BASE-T1S Multidrop OA SPI MAC-PHY Ethernet Transceiver Datasheet*
11. Texas Instruments, *TPS653860/61-Q1 Power Management IC For Safety-Relevant Applications Datasheet*
12. Texas Instruments, *TPS1214-Q1 Low I_Q Automotive High Side Switch Controller With Low Power Mode, Load Wakeup, I^2t, and Diagnostics Datasheet*
13. Texas Instruments, *TPS2HCS10-Q1 11.3mΩ, Automotive Dual-Channel, SPI Controlled High-Side Switch With Integrated I2T Wire Protection and Low Power Mode Datasheet*
14. Texas Instruments, *TPS2HCS05-Q1 5mΩ , Automotive Dual-Channel , SPI Controlled High-Side Switch With Integrated I2T Wire Protection and Low Power Mode Datasheet*
15. Texas Instruments, *DRV8245-Q1 Automotive H-Bridge Driver with Integrated Current Sense and Diagnostics Datasheet*
16. Texas Instruments, *TIC12400-Q1 24-Input Multiple Switch Detection Interface (MSDI) With Integrated ADC and Adjustable Wetting Current for Automotive Systems Datasheet*

17. Texas Instruments, *LM749x0-Q1 Automotive Ideal Diode With Circuit Breaker, Undervoltage, and Overvoltage Protection With Fault Output Datasheet*
18. Texas Instruments, *LM74703-Q1, LM74704-Q1 Automotive Ideal Diode Controller With External FET Health Indication Datasheet*
19. Texas Instruments, *INA186-Q1 AEC-Q100, 40-V, Bidirectional, High-Precision Current Sense Amplifier With picoamp IB and ENABLE Datasheet*
20. Texas Instruments, *TPS7B81-Q1 Automotive, 150mA, Off-Battery, Ultra-Low I_Q (3µA), Low-Dropout Regulator Datasheet*
21. Texas Instruments, *TPS3762-Q1 Automotive 65V Window (OV & UV) Supervisor with Built-In Self-Test and Latch Datasheet*
22. Texas Instruments, *TPS62903-Q1 3-V to 18-V, 3-A, Automotive Low I_Q Buck Converter with +165°C T_J Datasheet*
23. Texas Instruments, *TPS62902-Q1 3-V to 18-V, 2-A, Automotive Low I_Q Buck Converter with +165°C T_J Datasheet*
24. Texas Instruments, *TPS7B4256-Q1Automotive, 70-mA, 40-V, Voltage-Tracking LDO With 6-mV Tracking Tolerance Datasheet*
25. Texas Instruments, *TPS1211-Q1 45V Automotive Smart High-Side Driver With Protection and Diagnostics Datasheet*
26. Texas Instruments, *TPS1HC30-Q1, 30-mΩ, 5-A, Single-Channel Automotive Smart High Side Switch Datasheet*
27. Texas Instruments, *TPS4HC120-Q1 120mΩ, 2A, Quad-Channel Automotive Smart High-Side Switch Datasheet*
28. Texas Instruments, *TPS2HC08-Q1 9.5mΩ Dual-Channel Automotive Smart High-Side Switch Datasheet*
29. Texas Instruments, *TPS1HC04-Q1 4.9mΩ Single-Channel Automotive Smart High-Side Switch Datasheet*
30. Texas Instruments, *DRV871x-Q1 Automotive Multichannel Smart Half-Bridge Gate Drivers With Wide Common Mode Inline Current Sense Amplifiers Datasheet*
31. Texas Instruments, *DRV8145-Q1 Automotive Half Bridge Driver with Integrated Current Sense and Diagnostics Datasheet*
32. Texas Instruments, *DRV81602-Q1 : 8-Channel, 40V, 700mΩ, Fully Protected, Configurable Low-side and High-side Driver for Automotive Relay, LED, Lighting and Motor Control Datasheet*
33. Texas Instruments, *TCAN1043A-Q1 Automotive Low-Power Fault Protected CAN FD Transceiver With Sleep Mode Datasheet*
34. Texas Instruments, *TCAN1044-Q1 Automotive Fault-Protected CAN FD Transceiver With 1.8V I/O Support Datasheet*
35. Texas Instruments, *TCAN1046V-Q1 Dual Automotive Fault-Protected CAN Transceiver Datasheet*
36. Texas Instruments, *SN3257-Q1 Automotive 5-V, Low Propagation Delay, 2:1 (SPDT),4-Channel Switch With 1.8 V Logic Datasheet*
37. Texas Instruments, *TLIN1021A-Q1 Fault-Protected LIN Transceiver with Inhibit and Wake Datasheet*
38. Texas Instruments, *TLIN1024A-Q1 Quad Local Interconnect Network (LIN) Transceiver with Dominant State Timeout Datasheet*
39. Texas Instruments, *TAS6754-Q1 1L Modulation, 2MHz Digital Input 4-Channel Automotive Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics Datasheet*
40. Texas Instruments, *TMUX13xx-Q1 Automotive 5-V, Bidirectional 8:1, 1-Channel and 4:1, 2-Channel Multiplexers with Injection Current Control Datasheet*
41. Texas Instruments, *TPLD1201-Q1 Automotive Programmable Logic Device with 8-GPIO Datasheet*
42. Texas Instruments, *SN74CBTLV3861-Q1 Low-Voltage 10-Bit FET Bus Switch Datasheet*
43. Texas Instruments, *TXE81XX-Q1 Automotive 16-Bit and 24-Bit SPI Bus I/O Expander with Interrupt Output, Reset Input, and I/O Configuration Registers Datasheet*
44. Texas Instruments, *TCAL9539-Q1 Automotive Low-Voltage 16-Bit I2C-Bus, SMBus I/O Expander with Interrupt Output, Reset, and Configuration Registers Datasheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (January 2026)	Page
• Added test setup and several test results for TIDA-020079	1

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