Design Guide: TIDA-010957

15kW, Bidirectional, Three-Phase Plus Neutral Flying Capacitor Based on GaN Reference Design

Description

This reference design provides a design template for implementing a three-level, three-phase plus neutral, Gallium Nitride (GaN) based flying capacitor power stage. The use of fast switching power devices allows switching at an equivalent frequency of 125kHz, reducing the size of magnetics for the filter and increasing the power density of the power stage. The multilevel topology allows the use of 650V rated power devices at higher DC bus voltages of up to 900V. The lower switching voltage stress across the transistors reduces the switching losses, resulting in an efficiency of 98.9% at full power.

Resources

TIDA-010957	Design Folder
LMG3522R030, UCC33421-Q1	Product Folder
TMCS1126, AMC0311D	Product Folder
AMC0381D, AMC0330R	Product Folder
ISOTMP35, TMS320F28P550SJ	Product Folder

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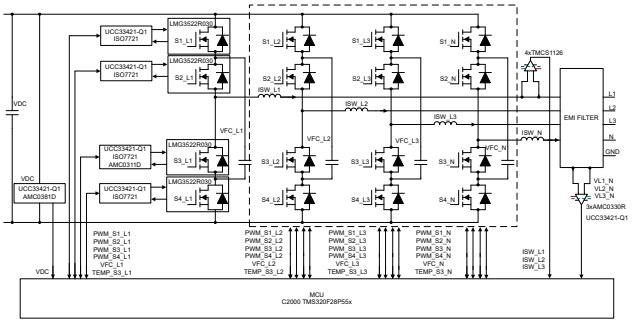
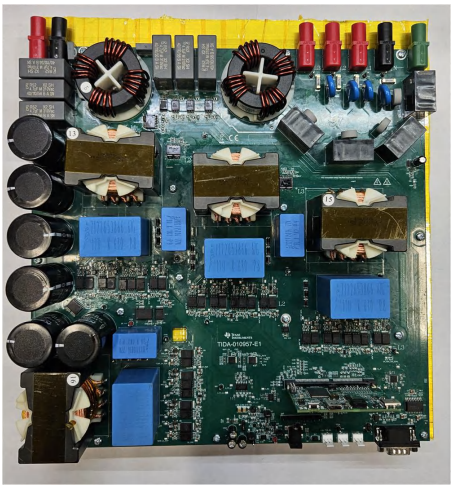
Features

- Power stage for three-phase plus neutral bidirectional DC/AC converter
- 650V rated switches in 900V system (due to three levels)
- High switching frequency of 125kHz and high efficiency design (98.9%)
- 21A_{RMS} per phase
- Control scheme that allows control of the unbalancing of three current phases

Applications

- String inverter
- Central inverter
- Onboard charger
- DC fast charging station
- Power conversion system (PCS)
- Uninterruptible power supply





1 System Description

Modern commercial scale solar inverters see advancement on multiple fronts, which lead to smaller, higher efficiency products in the market:

- Moving toward higher voltage solar arrays
- Reducing the size of onboard magnetics
- Inclusion of localized power storage requiring bidirectional power stages

By increasing the voltage to 1000V or 1500V DC from the PV string, the current can be reduced while maintaining the same power levels. The reduction in current reduces conduction losses and hence results in higher efficiency. However, high DC bus voltages limit the choice of power components, because higher withstand voltage is needed.

To compensate for the voltage stresses generated by high-voltage solar arrays, alternative topologies of solar inverters need to be taken in consideration[(1)]. In traditional half-bridge cells, each switching device needs to withstand the full DC bus voltage. By adding additional power components, the overall stress on the device can be significantly reduced when adopting multilevel converters. This reference design shows how to implement a three-level flying capacitor converter that limits the voltage stress on all the power components to only half the DC bus voltage, allowing use of more abundant and faster power components. This design also demonstrates the use of GaN devices in solar inverters which is not possible with other topologies due to the limitation of voltage withstand capability.

Additional power density is enabled by switching to a higher switching frequency in the power converters. As this design shows, a higher switching frequency reduces the overall size of the output filter stage.

Though multilevel flying capacitor topologies enable the use of lower voltage switching devices, the topologies come with certain limitations; the need to control in real time the flying capacitor at half the DC link voltage[(2)]. This design demonstrates how to address all 16 power devices in the power stage while controlling simultaneously:

- Three-currents
- DC link voltage
- The voltage of four flying capacitors

Another requirement that is becoming more prevalent for DC/AC power stages is the need for bidirectional power flow between the AC and the DC, and compensator of reactive power. This is important in storage-ready inverters where there can be a need for the power from the grid to be stored in local power storage system like a battery. The power conversion stage in an electronic energy storage system also has the same requirement. The flying capacitor power stage demonstrated in this design is inherently capable of bidirectional operation – only software is required for the stage to operate either as inverter or Power Factor Correction (PFC). Furthermore, the design has been proven to operate by injecting or draining reactive power from each phase.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETERS	SPECIFICATIONS	DETAILS
DC/AC Power Rating	15kVA	At 400V AC
AC Voltage	Three-Phase 400V AC	Maximum Voltage 480V AC
AC Current	21A	Overload 25A
DC Voltage	800V DC	From 650V DC to 900V DC
Switching Frequency	62.5kHz	Equivalent 125kHz
Peak Efficiency	98.9%	At 480V AC
Frequency	50Hz to 60Hz	
Heat Sink Temperature	Full Power up to 70°C	
Reference Design Dimensions	300mm × 300mm × 90mm	2.22kW/Liter

CAUTION

Do not leave the design powered when unattended.

WARNING

High voltage! *Accessible high voltages are present on the board.* Electric shock is possible. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

WARNING

Hot surface! Contact can cause burns. Do not touch!

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider the design as a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board*** . The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

2 System Overview

2.1 Block Diagram

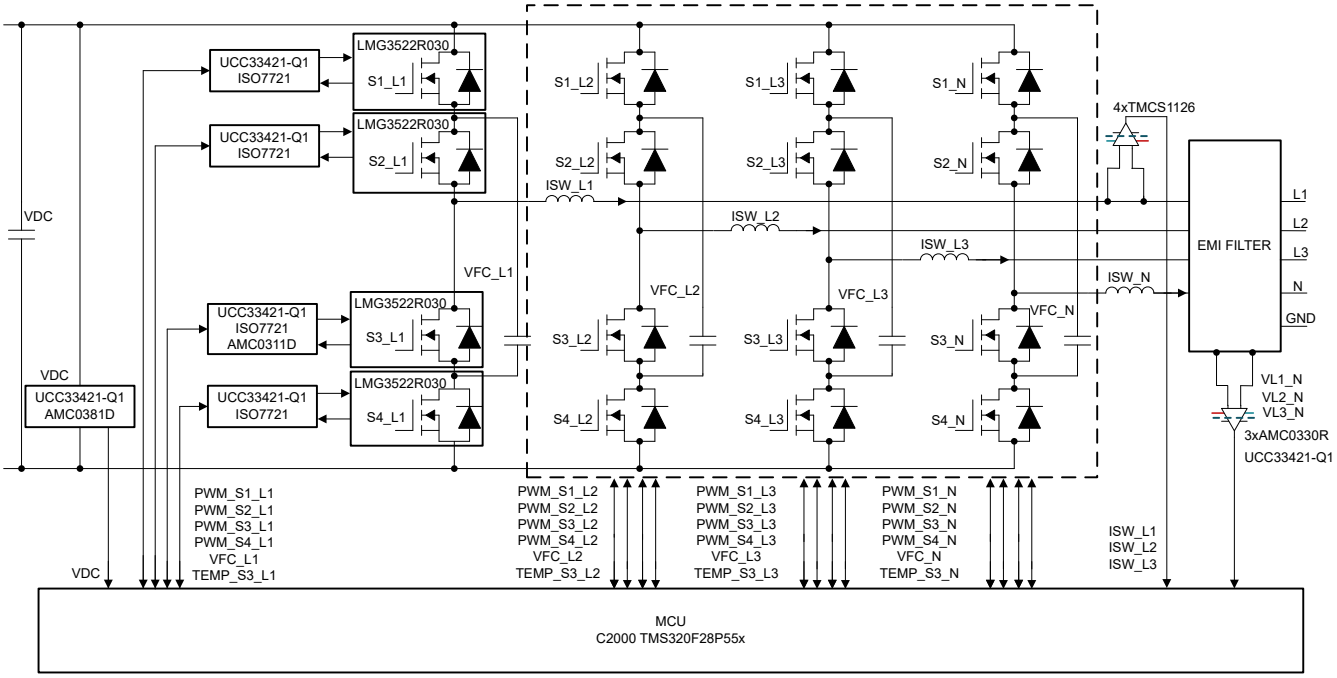


Figure 2-1. TIDA-010957 Block Diagram

This reference design is composed of the following boards:

- Main power board which is including all the power components
- A TMDSCNCD28P55X Control Card to support the DSP

The board does not include any auxiliary power supply able to convert the power from high voltage down to 12V. An external bias power supply is required to run the board.

2.2 Design Considerations

Figure 2-2 shows the basic architecture of the three-level three-phase converter reference design topology.

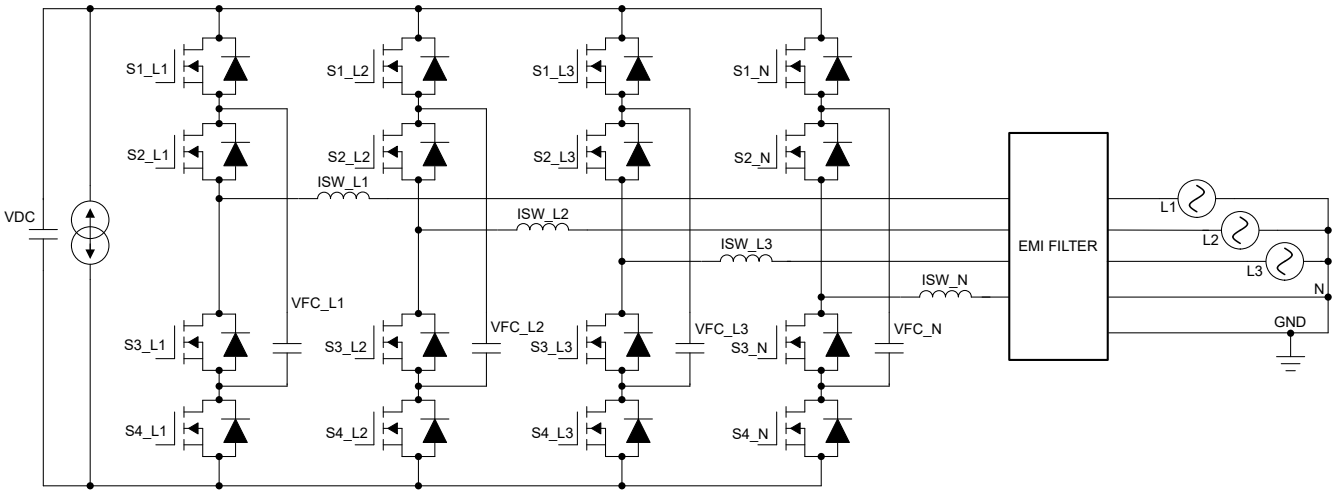


Figure 2-2. Flying Capacitor Converter Three-Phase Plus Neutral Architecture

Figure 2-2 shows that four flying capacitor switching cells are implemented for each terminal of the grid. Figure 2-3 shows a single leg can be separated out thus, simplifying the analysis of the topology.

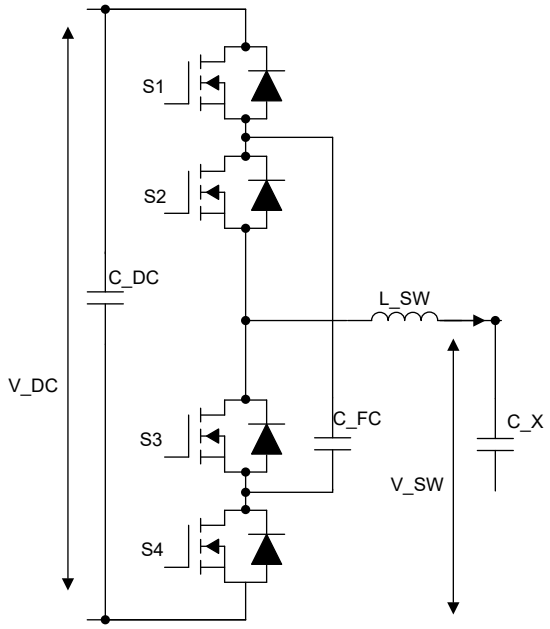


Figure 2-3. Flying Capacitor Single-Phase Leg

Four fundamental components are found in the main building block:

- S1, S2, S3, and S4 are four power FETs
- C_FC is the capacitor called flying capacitor
- L_SW is the switching node inductance
- C_DC is the DC link voltage capacitor

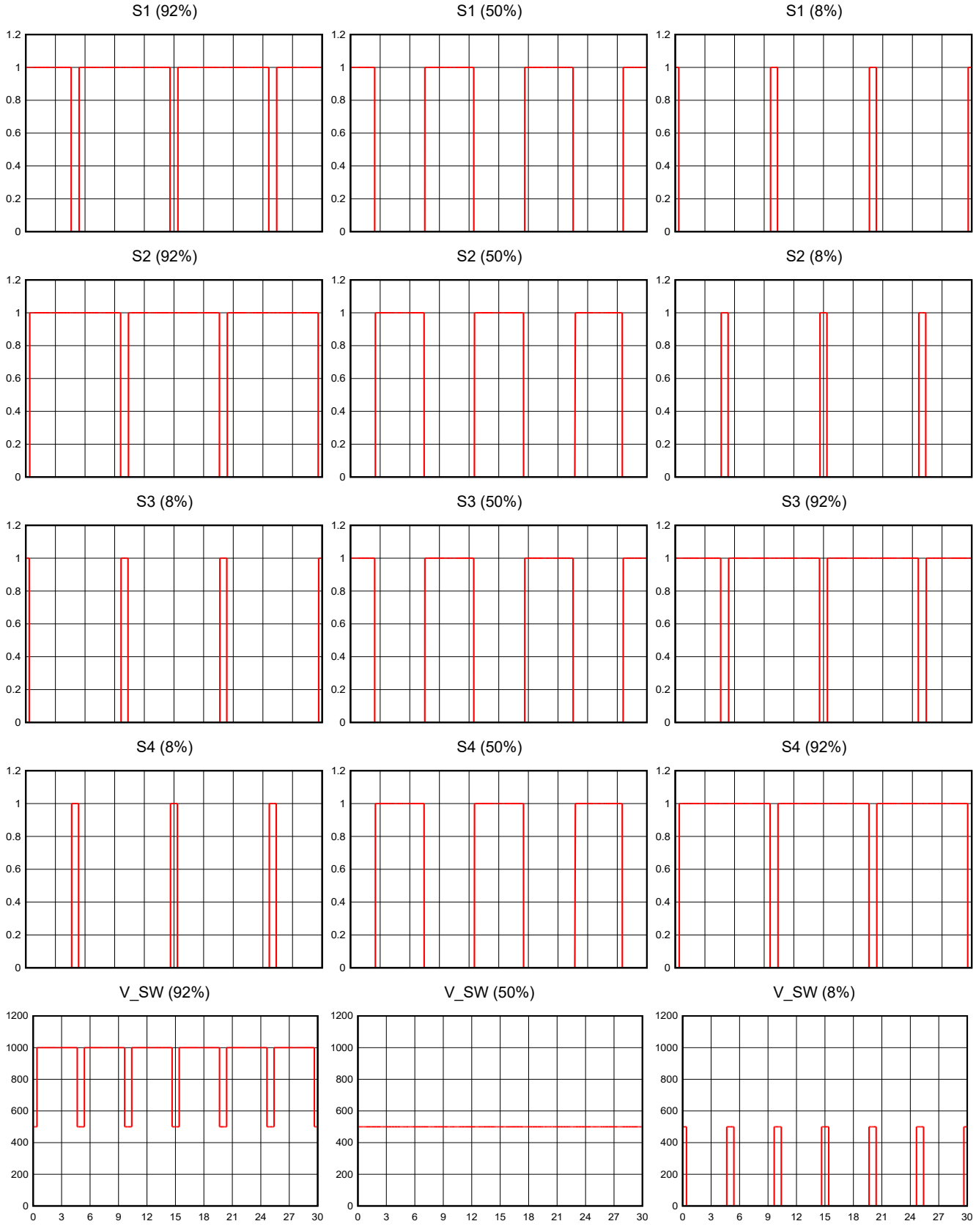
The components are described in the subsequent sections.

2.2.1 Switching Pattern of a 3-Level Flying Capacitor Switching Cell

As Figure 2-3 shows, there are four switches implemented for each phase (S1, S2, S3 and S4). In this topology, each FET is rated for half the DC link voltage. Though there are various switching schemes to control this power stage, a relatively simpler scheme is selected to reduce complexity. In this topology, all the transistors are switching at the nominal frequency f_{PWM} . Dead time, carrier and duty cycle needs to be defined for each FET:

- Switch pairs S1 and S4, and S2 and S3 are complementary to each other. Two pairs of dead times are required. If S1 and S4 are not complementary to each other there is risk of shorting C_{DC}, thus causing an important overcurrent plus overvoltage across S2 and S3. If S2 and S3 are not switching complementary to each other there is risk of shorting C_{FC}, thus causing an important overcurrent plus overvoltage across S1 and S4.
- S1 and S4 and S2 and S3 signals are 180 degrees phase-shifted to each other. This is achieved by phase shifting the carriers by 180 degrees. Because of this phase shifting, the inductor sees two times the switching frequency, thus making the inductor smaller.
- At first approximation the duty cycle applied to the two PWM pairs is going to be the same. The duty cycle can be calculated as a ratio between V_{SW} and V_{DC}.

Table 2-1. Gate-Drive PWM Signals and Switching Node Voltage When Having 1kV DC Bus Voltage



As Table 2-1 shows, three different operating points of the switching cell are investigated:

- Left column: when the duty cycle is higher than 50%, S1 and S2 are more time in the on-state than S3 and S4. When having 1000V DC link, the output switching voltage is switching between the levels 500V and 1000V.
- Right column: when the duty cycle is lower than 50%, S3 and S4 are more time in the on-state than S1 and S2. When having 1000V DC link, the output switching voltage is switching between the levels 0V and 500V.
- Central column: when the requested duty is equal to 50%, all the four switches are going to be ON 50% of the switching time. At first approximation, output switching node voltage is going to be fixed at 500V.

2.2.2 Power Switching Devices Selection and Cooling Approach

As described previously, the main switching device needs to support only half the full DC bus voltage. To support the 900V DC link voltage of this design, use at least 600V rated devices. The switches S1, S2, S3 and S4 are required to switch at high frequency; therefore, the devices must have good switching performances. To select the right power FET, conduction and switching losses need to be derived.

Conduction loss is mainly determined by the $R_{DS(on)}$ of the FETs. At any moment, there are always two devices conducting the main current at the same time. At first approximation, the total conduction loss of the single FET can be calculated as follows:

$$P_{COND} = \frac{R_{DS(on)} \times I_{SW}^2}{\sqrt{2}} \quad (1)$$

where

- I^2_{SW} represents the RMS current of the switching node

Switching loss is a function of the switching frequency and switching energy of each switching element; the switching energy being related to the device current and voltage at the switching transient. Using the switching energy curve in the datasheet, the total switching loss can be estimated. Note that the switching losses in all the operating modes are always the same, where with operating mode the text means PFC, inverter, capacitive compensator, and inductive compensator. The text indicates the importance of noticing that during the single half-cycle only two FETs are having switching losses.

2.2.3 Boost Inductor Selection

The boost inductor or the switching node inductor is used to filter out the voltage pulses generated by the switching cell. When selecting the right inductor three important parameters need to be considered:

- Peak-to-peak ripple current which drives losses of the inductor
- Application peak current which drives the saturation current of the core
- RMS current of the applications

In a three-level flying capacitor converter the peak-to-peak ripple current flowing through the boost inductor (L_{SW}) is calculated as follows:

$$D_{eff} = 2 \times D - \text{floor}(2 \times D) \quad (2)$$

$$\Delta I_{boost} = \frac{V_{DC} \times (D_{eff}(1 - D_{eff}))}{4 \times L_{sw} \times f_{sw}} \quad (3)$$

where

- V_{DC} is the DC link voltage
- D is the ratio between the switching node voltage and the DC link voltage
- L_{SW} is the switching node inductance
- f_{SW} is the switching frequency

The formula shows that the peak-to-peak current shows the maximum when the duty cycles are equal to 25% and 75%. In a sinusoidal applications as this reference design, considering as a worst case the 25% and the 75% duty cycle is recommended. Normally, working with an inductor peak-to-peak current of less than 40%

of the average maximum AC current is advisable. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI.

The saturation current of the inductor must be higher than the calculated peak inductor current. In this application, the peak current flowing into the inductor can be calculated as follows:

$$I_{peak} = \frac{\sqrt{2} \times S_N}{\sqrt{3} \times V_{LL}} + \frac{\Delta I_{boost}}{2} \quad (4)$$

Where the first part represents the peak average current of the application and each term is represented as:

- S_N is the apparent rated power of the converter
- V_{LL} is the line-to-line RMS voltage

2.2.4 Flying Capacitor Selection

C_{FC} is the flying capacitor implemented in the flying capacitor topology. When selecting the right capacitor, ripple voltage and RMS current needs to be calculated. The steady state peak-to-peak ripple voltage can be calculated as follows:

$$\Delta V_{FC} = \frac{(0.5 - ABS(D - 0.5)) \times I_{boost}}{C_{FC} \times f_{sw}} \quad (5)$$

where

- D is the voltage ratio between the input and the output
- F_{SW} is the switching frequency at which the two legs are switching
- I_{boost} is the switching node current
- C_{FC} is the flying capacitor capacitance value

The formula shows that when having a higher switching frequency, the capacitance can be decreased accordingly, thus making the capacitor smaller. When looking at the duty cycle dependency, the worst-case scenario happens when the duty cycle is equal to 50%. When selecting the right capacitance value, the worst-case duty cycle and inductor current need to be selected accordingly.

Calculate the flying capacitor current with Equation 6.

$$I_{FC,\,RMS} = \sqrt{2(0.5 - ABS(D - 0.5)) \times \left({I_{boost}}^2 + \frac{{\Delta I_{boost}}^2}{12} \right)} \quad (6)$$

where

- ΔI_{boost} represents the ripple peak to peak current

The formula shows that the worst-case scenario happens when the duty cycle is equal to zero.

2.2.5 Cx Capacitance Selection

Cx are the capacitors connected between line-to-line or line-to-neutral. The aim of these capacitors is to attenuate the differential mode noise injected from the DC/AC into the grid. The value of these capacitors is a trade-off between reactive power delivered to the grid and the differential mode attenuation. By default, the reactive power injected into the grid is equal to Equation 7.

$$Q = V_{LL}^2 \times C_x \times \omega \quad (7)$$

where

- Cx represents the equivalent capacitance connected between the line and the neutral
- ω is the grid electrical pulsation

Placing very high capacitance significantly reduces the injected noise, but leads to too much injected reactive power.

2.2.6 DC-Link Output Capacitance Selection

In three-phase applications, power ripple is present when the currents are unbalanced and can cause voltage ripple on the DC link. Use Equation 8 to calculate the peak-to-peak voltage ripple.

$$\Delta V = \frac{S_N}{3 \times 2 \times \pi \times f_e \times V_{DC} \times C_{DC}} \quad (8)$$

where

- C_{DC} is the total DC link capacitance
- f_e is the grid frequency

Equation 8 shows that S_N is divided into three because this value corresponds to the maximum power ripple. Based on the ripple voltage specification the right amount of electrolytic capacitance can be derived.

2.3 Highlighted Products

2.3.1 LMG3522R030 - 650V, 30mΩ GaN FET With Integrated Driver

The LMG3522R030 GaN FET with integrated driver and protections is targeting switch-mode power converters and enables designers to achieve new levels of power density and efficiency. The LMG3522R030 integrates a silicon driver that enables switching speed up to 150V/ns. TI integrated precision gate bias results in higher switching SOA compared to discrete silicon gate drivers. This integration, combined with TI low inductance package, delivers clean switching and minimal ringing in hard-switching power supply topologies. Adjustable gate drive strength allows control of the slew rate from 15V/ns to 150V/ns, which can be used to actively control EMI and optimize switching performance. Advanced power management features include digital temperature reporting and fault detection. The temperature of the GaN FET is reported through a variable duty cycle PWM output, which simplifies managing device loading. Faults reported include overtemperature, overcurrent, and UVLO monitoring.

2.3.2 TMDSCNCD28P55X - controlCARD Evaluation Module

TMDSCNCD28P55X is a low-cost evaluation and development board for TI's C2000™ MCU series of F28P55x devices. The device comes with a HSEC180 (180-pin high-speed edge connector) and, as a controlCARD, the device is an excellent choice for initial evaluation and prototyping. For evaluation of the TMDSCNCD28P55X, a 180-pin docking station TMDSHSECDOCK is required and can be purchased separately, or as a bundled kit.

2.3.2.1 Hardware Features

The TMDSCNCD28P55X hardware features follow:

- Isolated onboard XDS110 USB-to-JTAG debug probe enables real-time in-system programming and debugging
- Standard 180-pin controlCARD HSEC interface
- Analog I/O, digital I/O, and JTAG signals at card interface
- Hardware files are in C2000Ware at *boards\controlCARDs\TMDSCNCD28P55X*

2.3.2.2 Software Features

The TMDSCNCD28P55X software features include:

- TI Code Composer Studio IDE - integrated development environment for TI microcontrollers and embedded processors
- Software development kits (SDK)
- C2000Ware - low-level device drivers and examples
- MotorControl SDK - motor control system development for various three-phase motor control applications
- DigitalPower SDK - digital power system development for various AC-DC, DC-DC and DC-AC power supply applications

2.3.3 TMCS1126 - Precision 500kHz Hall-Effect Current Sensor With Reinforced Isolation

The TMCS1126 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 1.4% maximum sensitivity error over temperature and lifetime with no system level calibration, or less than 0.9% maximum sensitivity error including both lifetime and temperature drift with a one-time calibration at room temperature. AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated, on-chip, Hall-effect sensors. Core-less construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable current ranges up to ±120A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding $5kV_{RMS}$, coupled with a minimum of 8mm creepage and clearance, provides high levels of reliable lifetime reinforced working voltage. Integrated shielding enables excellent common-mode rejection and transient immunity. Fixed sensitivity allows the device to operate from a single 3V to 5.5V power supply, eliminating ratiometry errors and improving supply noise rejection. TI provides Grade B options at lower cost.

2.3.4 UCC33421-Q1 Ultra-Small, 1.5W, 5.0V, $5kV_{RMS}$ Isolation, DC/DC Module

The UCC33421-Q1 is an automotive qualified DC/DC power module with integrated transformer technology designed to provide 1.5W of isolated output power. The module can support an input voltage operation range of 4.5V to 5.5V and regulate 5.0V output voltage with a selectable headroom of 5.5V. The UCC33421-Q1 features a proprietary transformer architecture that achieves a $5kV_{RMS}$ isolation rating, while simultaneously supporting low EMI and excellent load regulation. The UCC33421-Q1 integrates protection features for increased system robustness such as enable pin with fault reporting mechanism, short circuit protection and thermal shutdown. The UCC33421-Q1 comes in a miniaturized, low-profile SSOP (5.85mm × 7.50mm) package with 2.65mm height and > 8.2mm clearance and creepage.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The Device under Test (DUT) in this design is set up and operated in several pieces:

- One TIDA-010957 board, heat sink (125631 Wakefield Thermal), and thermal interface material (T-Work8000)
- TMDSCNCD28P55X control card
- USB Type-C® cable USB isolator
- Power adapter with 12V output and 3A rating
- Laptop
- Oscilloscope, current, and voltage probes
- Thermal camera
- 18kVA bidirectional AC Grid Emulator (480VAC)
- 18kW bidirectional DC Emulator (1000VDC)

3.2 Test Setup

3.2.1 Testing TIDA-010957 Connected to the Grid With DC-Link

In this test condition, the system operates in closed-loop control mode. The control card TMDSCNCD28P55 executes the control. The MCU implements current control loops that synchronize with grid voltages from the AC source emulator. The PLL enables synchronization with the grid. Simultaneously, the voltage control loop generates the peak current reference for the three current loops. The peak current controls active power flow between DC and AC.

On the DC link, the bidirectional DC supply directly controls the drained or sourced current, allowing the user to control converter power. In this operating condition, efficiency versus power measurements occurred.

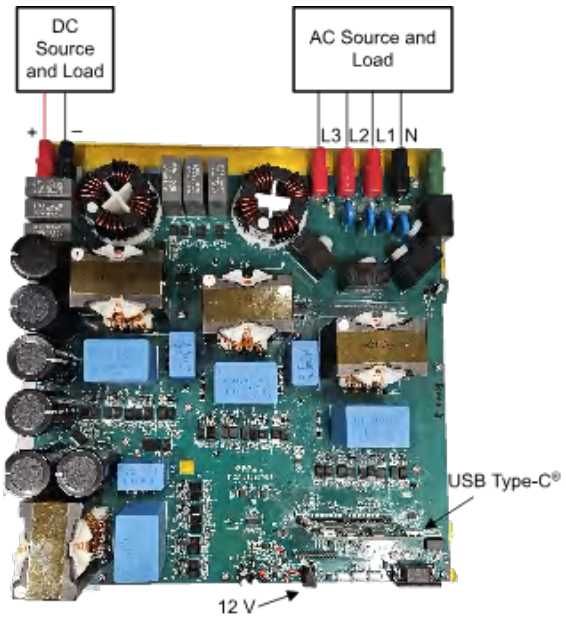


Figure 3-1. Connections for Testing the Reference Design Connected to the Grid

3.3 Test Results

3.3.1 Testing TIDA-010957 Connected to the Grid With DC-Link: Balanced Currents

To run this test, connect the board as Figure 3-1 shows.

3.3.1.1 Nominal Apparent Power

In these tests, nominal apparent power occurred when the DC link voltage reached 700VDC and the grid voltage reached 400VAC. The converter connects to the grid by controlling the three currents. The currents achieved full four-quadrant operation including: inverter, Power Factor Corrector (PFC), inductive compensator and capacitive compensator. The experimental results appear in Figure 3-2 through Figure 3-8. During the experiments, no significant zero crossing distortion appeared in the currents. The total harmonic distortion at nominal power remained below 3%. Furthermore, note that no significant current ripple enters the grid

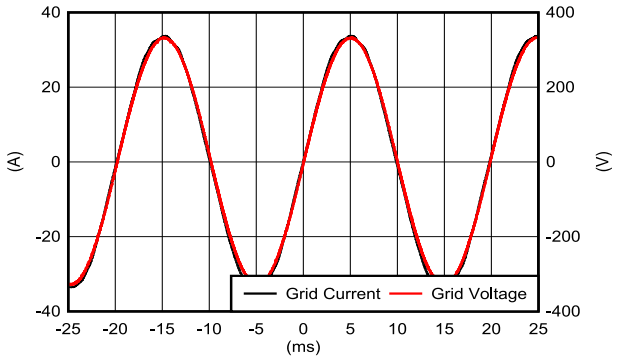


Figure 3-2. Experimental PFC Operation: Line Current and Line Voltage (Figure A)

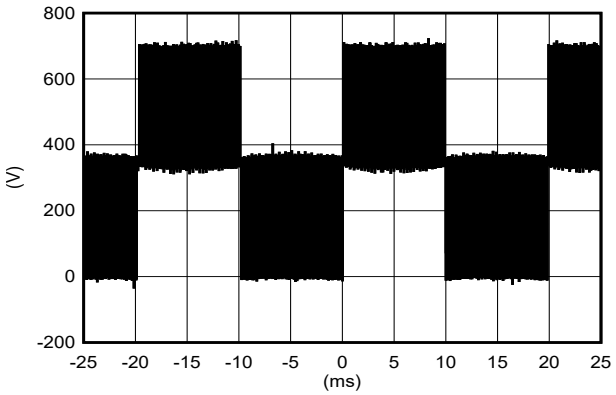


Figure 3-3. Experimental PFC Operation: Switching Node Voltage (Figure B)

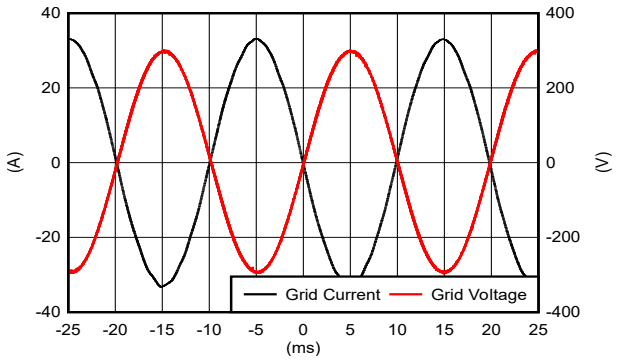


Figure 3-4. Experimental Inverter Operation: Line Current and Line Voltage (Figure A)

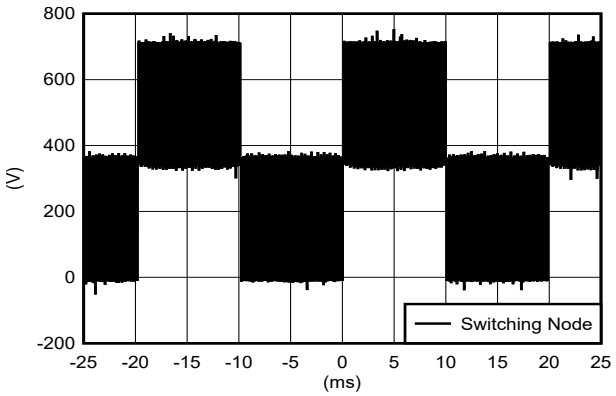


Figure 3-5. Experimental Inverter Operation: Switching Node Voltage (Figure B)

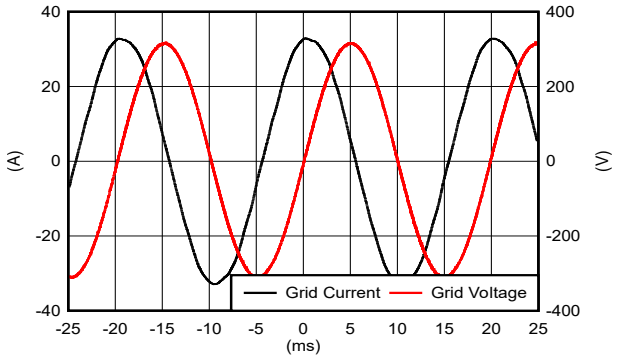


Figure 3-6. Experimental Inverter Plus Capacitive Compensation: Line Current and Line Voltage (Figure A)

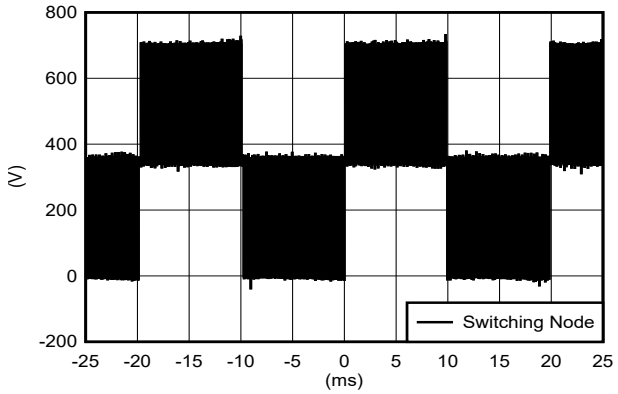


Figure 3-7. Experimental Inverter Plus Capacitive Compensation: Switching Node Voltage (Figure B)

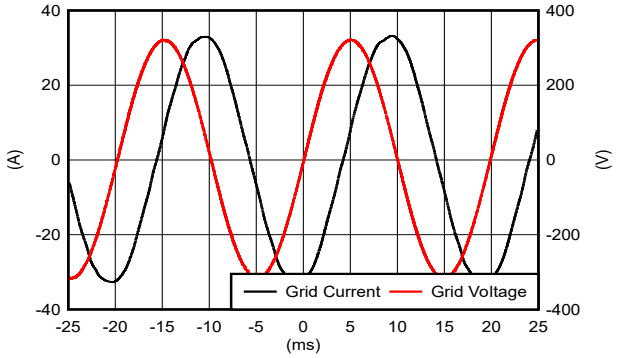


Figure 3-8. Experimental Inverter Plus Inductive Compensation: Line Current and Line Voltage (Figure A)

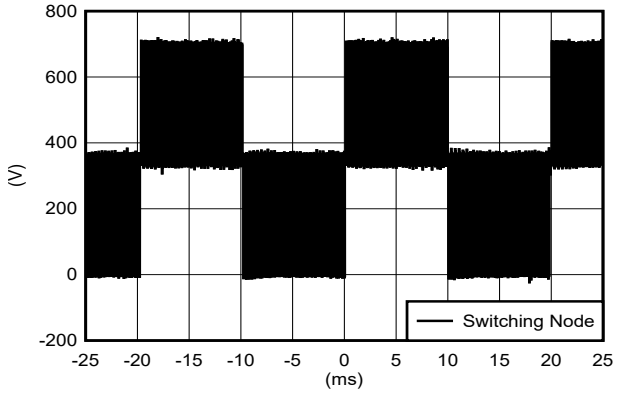


Figure 3-9. Experimental Inverter Plus Inductive Compensation: Switching Node Voltage (Figure B)

3.3.1.2 Efficiency vs Power vs DC-Link Voltage

Efficiencies for different powers and DC link voltages occurred at three different DC voltages: 700V, 800V, and 900V. When all measurements executed, the reactive power remained at zero. During these experiments, the MCU sampled GaN FET junction temperatures in real-time and recorded the highest temperatures.

3.3.1.2.1 Testing the Converter at 700VDC at 400VAC

Table 3-1 and Table 3-2 collect the efficiencies of the DC/AC at 400 VAC and 700 VDC, respectively, when operating as an inverter and a PFC. The results obtained from the power analyzer are taken from 1kW to 14.7kW. In most of the operating points, the power efficiency is higher than 98% by reaching a maximum of 98.81%.

Table 3-1. DC/AC at 700VDC and 400VAC Working as an Inverter

OUTPUT POWER INVERTER OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION	S3 JUNCTION TEMPERATURE RISE
1kW	95,89%	17,8%	7°C
2,42kW	97,99%	7,84%	7°C
3,98kW	98,54%	5,26%	11°C
5,54kW	98,75%	4,1%	14°C
7,03kW	98,80%	3,4%	18°C
8,61kW	98,81%	3%	20°C
10,2kW	98,76%	2,6%	24°C
11,67kW	98,68%	2,2%	32°C
13,28kW	98,59%	2,1%	38°C

Table 3-1. DC/AC at 700VDC and 400VAC Working as an Inverter (continued)

OUTPUT POWER INVERTER OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION	S3 JUNCTION TEMPERATURE RISE
14,72kW	98,52%	2%	46°C

Table 3-2. DC/AC at 700VDC and 400VAC Working as a PFC

OUTPUT POWER PFC OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION	S3 JUNCTION TEMPERATURE RISE
2kW	97,84%	9%	6°C
3,75kW	98,47%	5,6%	9,27°C
5,3kW	98,71%	4,2%	12,09°C
6,84kW	98,78%	3,5%	15°C
8,37kW	98,78%	3%	21°C
9,87kW	98,73%	2,6%	24°C
11,46kW	98,66%	2,32%	28,26°C
13,06kW	98,57%	2,1%	35,1°C
14,53kW	98,43%	2%	44°C

All the data summarized in Table 3-1 and Table 3-2 are collected and plotted as shown in Figure 3-10 through Figure 3-12. As Figure 3-10 shows a negligible decrement of 0.09% in the efficiency is observed when operating the DC/AC as a PFC with respect to the inverter operation, this is probably caused by the third-quadrant loss of the power FETs. In Figure 3-11, observe that the DC/AC converter shows a total harmonic distortion lower than 3% when the power is higher than half the nominal power. Figure 3-12 shows the worst-case junction temperature rise in the board. At full load, the temperature of the heat sink is around 60°C and the junction at 105°C. This demonstrated that even if the temperature of the system is high the efficiency number is quite impressive (98.52%).

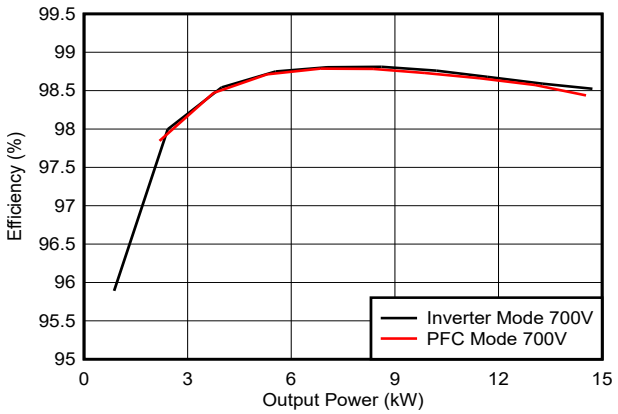


Figure 3-10. DC/AC Efficiency at 700VDC and 400VAC

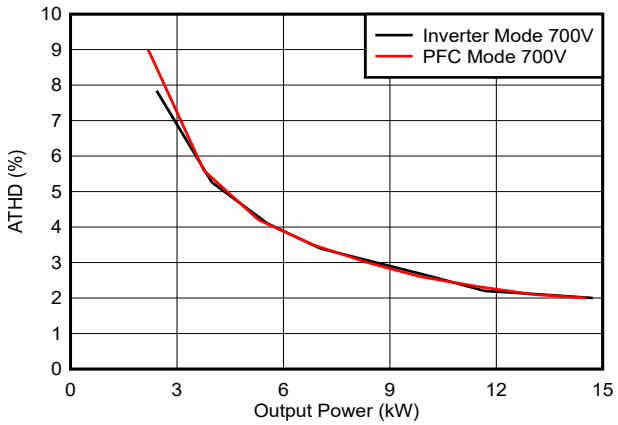


Figure 3-11. Total Harmonic Distortion for the DC/AC at 700VDC and 400VAC

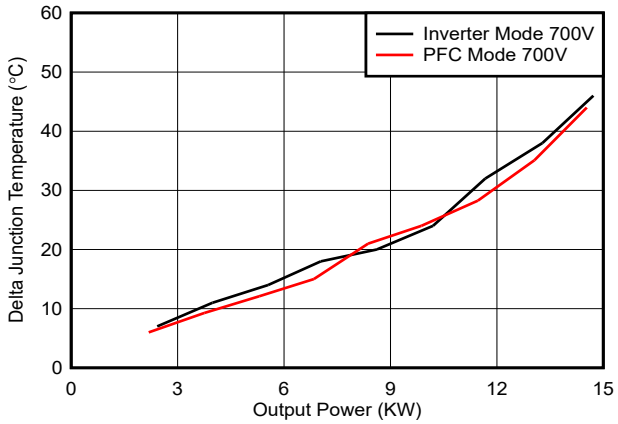


Figure 3-12. Junction Temperature Rise of the GaN S3 at 700VDC and 400VAC

3.3.1.2.2 Testing the Converter at 800VDC at 400VAC

Table 3-3 and Table 3-4 collect the efficiencies of the DC/AC at 400 VAC and 800 VDC, respectively, when operating as an inverter and a PFC. The results obtained from the power analyzer are taken from 1kW to 14.7kW. In most of the operating points, the power efficiency is higher than 98% by reaching a maximum of 98.63%.

Table 3-3. DC/AC at 800VDC and 400VAC Working as an Inverter

OUTPUT POWER INVERTER OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION	S3 JUNCTION TEMPERATURE RISE
1kW	93,98%	17,76%	6°C
2,3kW	97,35%	7,42%	5,84°C
3,83kW	98,1%	5,2%	10°C
5,40kW	98,45%	4%	13°C
6,89kW	98,58%	3,4%	19°C
8,46kW	98,63%	3%	22°C
10,05kW	98,62%	2,6%	25°C
11,66kW	98,57%	2,4%	35,3°C
13,2kW	98,48%	2,1%	41°C
14,74kW	98,37%	2%	49°C

Table 3-4. DC/AC at 800VDC and 400VAC Working as a PFC

OUTPUT POWER PFC OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION	S3 JUNCTION TEMPERATURE RISE
2kW	97,38%	7,3%	9,35°C
3,96kW	98,11%	5%	12°C
5,54kW	98,45%	3,7%	15°C
7,1kW	98,57%	3,2%	20°C
8,63kW	98,59%	2,7%	23°C
10,14kW	98,54%	2,3%	25°C
11,63kW	98,47%	2,2%	36°C
13,26kW	98,37%	2%	45°C
14,71kW	98,23%	1,7%	52°C

All the data summarized in Table 3-3 and Table 3-4 are collected and plotted as shown in Figure 3-13 through Figure 3-15. By comparing the converter operating at 700VDC (see Section 3.3.1.2.1), notice that there is a slight efficiency drop when operating at a higher DC link voltage. This is caused by the Coss losses. In Figure 3-14, observe that the DC/AC converter shows a total harmonic distortion lower than 3% when the power is

higher than half the nominal power. Figure 3-15 shows the worst-case junction temperature rise in the board. At full load, the temperature of the heat sink is around 60°C and the junction at 110°C. This demonstrated that even if the temperature of the system is high, the efficiency number is quite impressive (98.37%).

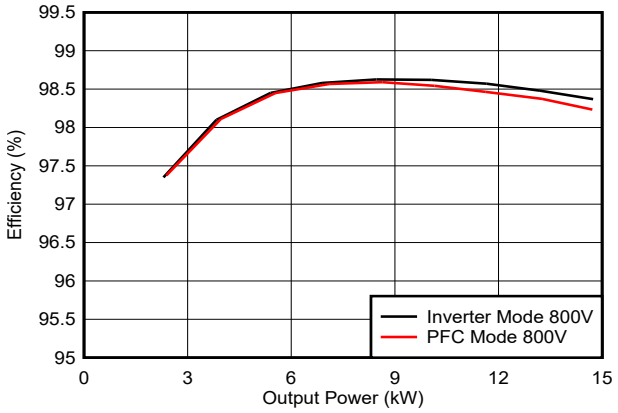


Figure 3-13. DC/AC Efficiency at 800VDC and 400VAC

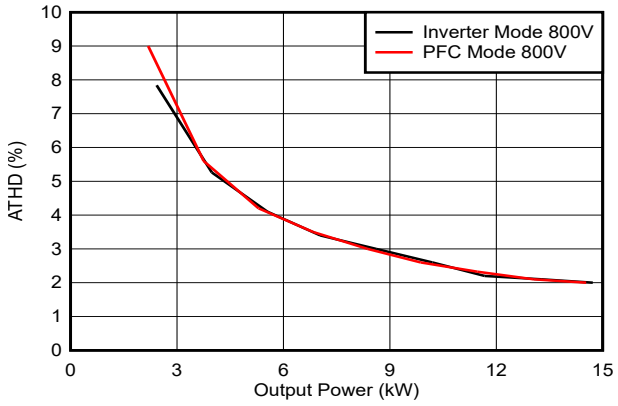


Figure 3-14. Total Harmonic Distortion for the DC/AC at 800VDC and 400VAC

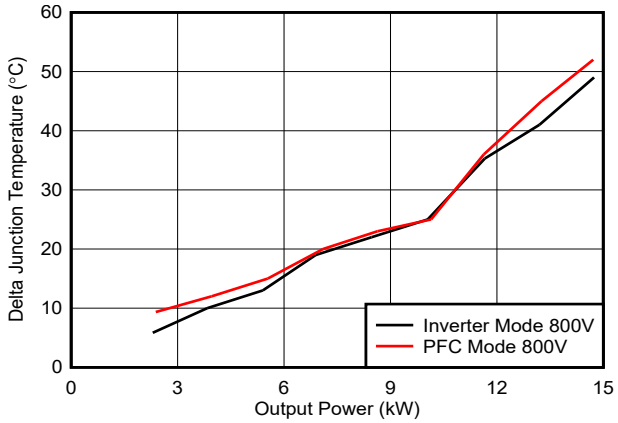


Figure 3-15. Junction Temperature Rise of the GaN S3 at 800VDC and 400VAC

3.3.1.2.3 Testing the Converter at 900VDC at 400VAC

Table 3-5 and Table 3-6 collect the efficiencies of the DC/AC at 400 VAC and 900 VDC, respectively, when operating as an inverter and a PFC. The results obtained from the power analyzer are taken from 1kW to 14.85kW. In most of the operating points, the power efficiency is higher than 98% by reaching a maximum of 98.42%.

Table 3-5. DC/AC at 900VDC and 400VAC Working as an Inverter

OUTPUT POWER INVERTER OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION	S3 JUNCTION TEMPERATURE RISE
1kW	90,98%	20%	5°C
2,17kW	96,7%	7%	9°C
3,75kW	97,63%	5%	11°C
5,33kW	98,12%	4%	16°C
6,84kW	98,33%	3,2%	18°C
8,42kW	98,41%	2,9%	23°C
9,96kW	98,42%	2,5%	28°C
11,58kW	98,38%	2,3%	33°C
13,21kW	98,31%	2,1%	39°C
14,85kW	98,21%	2%	47°C

Table 3-6. DC/AC at 900VDC and 400VAC Working as a PFC

OUTPUT POWER PFC OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION	S3 JUNCTION TEMPERATURE RISE
2kW	96,89%	6,4%	9°C
4,03kW	97,7%	4,7%	11°C
5,59kW	98,14%	3,6%	16°C
7,13kW	98,32%	3%	18°C
8,91kW	98,41%	2,7%	23°C
10,29kW	98,39%	2,5%	28°C
11,78kW	98,33%	2,2%	33°C
13,25kW	98,23%	2%	39°C
14,70kW	98,11%	1,7%	47°C

All the data summarized in Table 3-5 and Table 3-6 are collected and plotted as shown in Figure 3-16 through Figure 3-18. By comparing the converter operating at 700 VDC, notice that there is a slight efficiency drop when operating at a higher DC link voltage. This is caused by the Coss losses. In Figure 3-17, observe that the DC/AC converter shows a total harmonic distortion lower than 3% when the power is higher than half the nominal power. Figure 3-18 shows the worst-case junction temperature rise in the board. At full load, the temperature of the heat sink was around 60°C and the junction at 110°C. This demonstrated that even if the temperature of the system was high the efficiency number is impressive (98.21%).

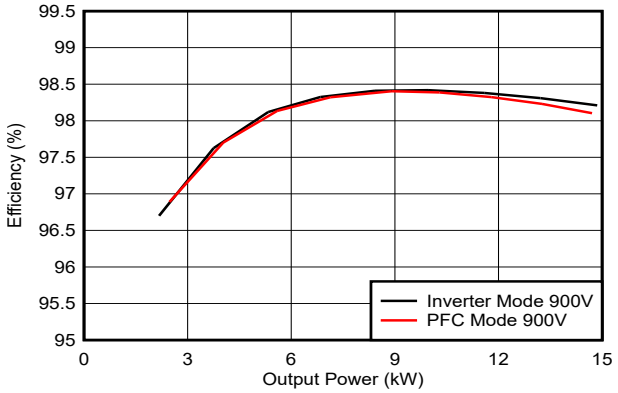


Figure 3-16. DC/AC Efficiency at 900VDC and 400VAC

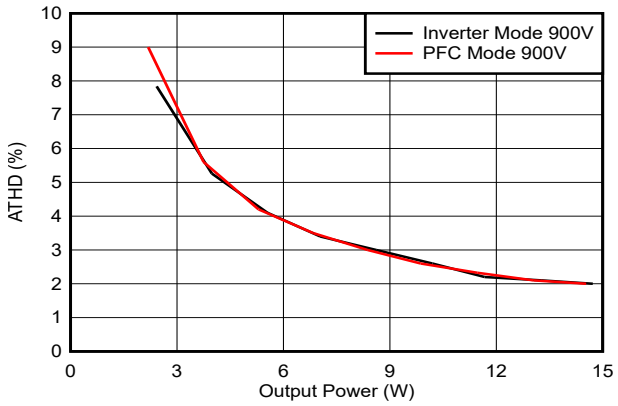


Figure 3-17. Total Harmonic Distortion for the DC/AC at 900VDC and 400VAC

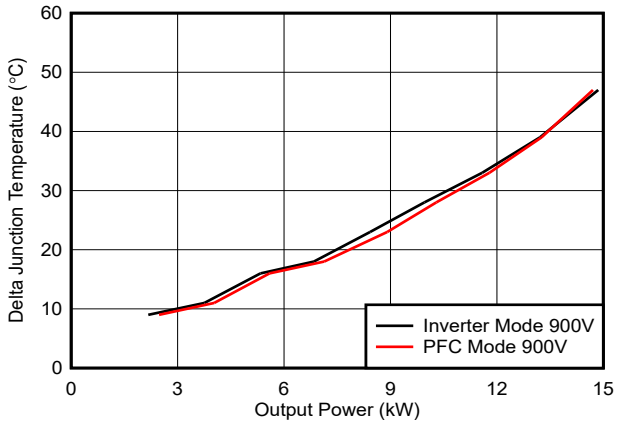


Figure 3-18. Junction Temperature Rise of the GaN S3 at 900VDC and 400VAC

3.3.1.2.4 Testing the Converter at 800VDC at 480VAC

Table 3-7 collects the efficiencies of the DC/AC at 480 VAC and 800 VDC when operating as a PFC. The results obtained from the power analyzer are taken from 3kW to 18kW. In most of the operating points, the power efficiency is higher than 98% by reaching a maximum of 98.89%. In this test condition, a higher power than 15kW is achieved because the grid input voltage is increased.

Table 3-7. DC/AC at 800VDC and 480VAC Working as a PFC

OUTPUT POWER PFC OPERATION	EFFICIENCY	TOTAL HARMONIC DISTORTION
3kW	97,97%	7,3%
4,69kW	98,56%	6,8%
6,55kW	98,78%	5,3%
8,42kW	98,87%	4,4%
10,3kW	98,89%	3,8%
12,21kW	98,87%	3,37%
14,13kW	98,82%	3%
16,06kW	98,75%	2,74%
18,00kW	98,66%	2,5%

All the data summarized in Table 3-7 are collected and plotted as shown in Figure 3-19 and Figure 3-20. By comparing the converter operating at 400VAC, notice that there is an important efficiency improvement. This is because at parity of input current, the power increases but the losses for the same current input are the same. In Figure 3-20 observe that the DC/AC converter shows a total harmonic distortion lower than 3% when the power is higher than 13kW. This is because the ratio between input and output voltage is closer to nominal.

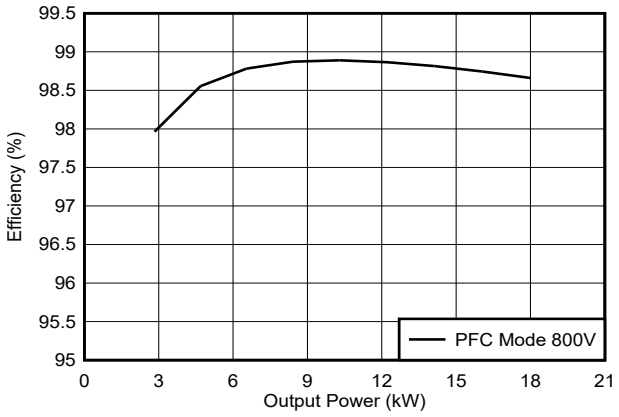


Figure 3-19. DC/AC Efficiency at 800VDC and 480VAC

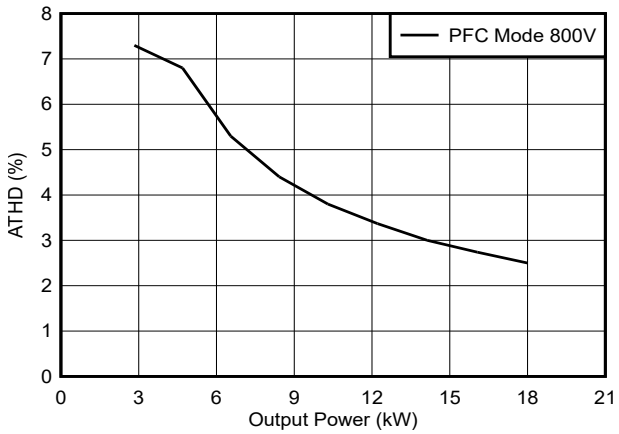


Figure 3-20. Total Harmonic Distortion for the DC/AC at 800VDC and 480VAC

3.3.2 Testing TIDA-010957 Tied to the Grid With DC-Link: Unbalance Currents

In this experiment, the converter operates with the DC/AC working as a PFC. The converter controls 700VDC. The grid draws power equal to 7kW. This experiment compares two conditions:

- 7kW balanced operation maintains equal RMS current in each phase (Figure 3-21)
- 7kW unbalanced operation decreases RMS current in phase L2 (Figure 3-23)

Figure 3-21 shows that in balanced operation, the three phases draw equal current amplitudes. Current L3 remains in phase with switching node voltage L3.

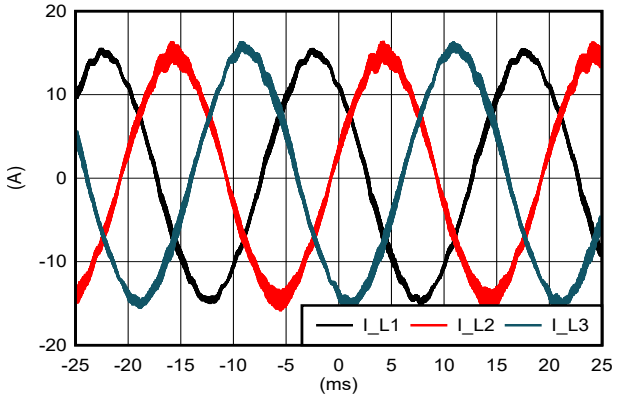


Figure 3-21. 7kW Balanced Currents (Figure A)

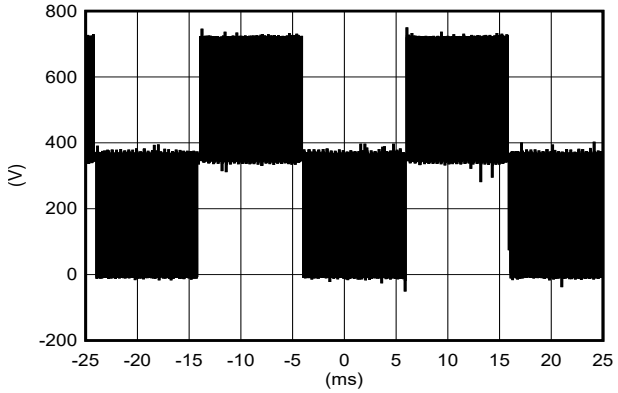


Figure 3-22. 7kW Switching Node Voltage (Figure B)

Conversely, when derating one phase power, currents on the other two phases increase as Figure 3-23 demonstrates. When current decreases in one phase, the other two phases must increase current to deliver the same power. Experimental results show that even during unbalanced operation, ripple current injected into the grid remains negligible. At this operating point, total harmonic distortion stays below 5%. The switching node voltage reveals a 100Hz harmonic generated by power ripple.

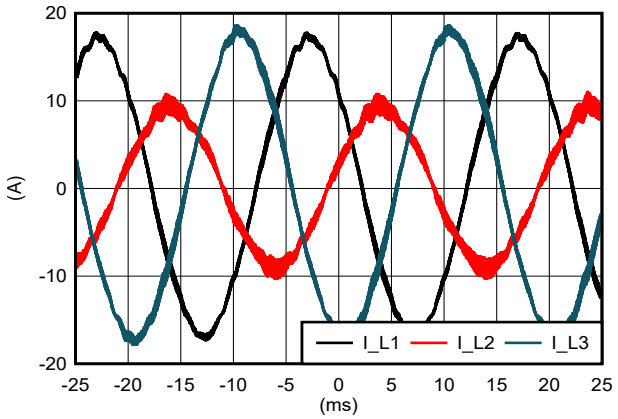


Figure 3-23. 7kW Unbalanced Currents (Figure A)

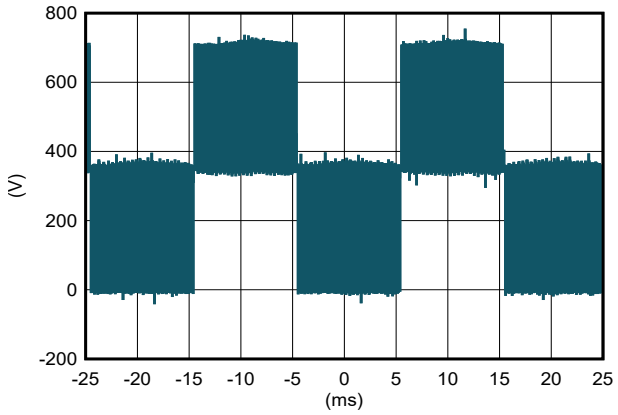


Figure 3-24. 7kW Switching Node Voltage (Figure B)

4 Design and Documentation Support

4.1 Design Files

To download the design files, see the design files at TIDA-010957.

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010957.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010957.

4.2 Documentation Support

1. Texas Instruments, *Comparison of AC/DC Power- Conversion Topologies for Three-Phase Industrial Systems Power Supply Design Seminar*
2. Texas Instruments, *Design Consideration of 3-Level Flying Capacitor Converters* (Future Application Note published together with the main reference design)

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

RICCARDO RUFFO received the Ph.D. degree in Electric, Electronics and Communication Engineering from Politecnico di Torino, Turin, Italy, in 2019. He is currently working at Texas Instruments Germany as System Engineer in the area of Solar Energy within Energy Infrastructure Team. His main work includes EV charging, inductive wireless power transfer, photovoltaic, renewable energy, and energy storage applications.

BOWEN LING is a system engineer at Texas Instruments, where he is working in the area of Solar Energy within the Energy Infrastructure team.

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