

J722S/AM67x/TDA4VEN/TDA4AEN Evaluation Module


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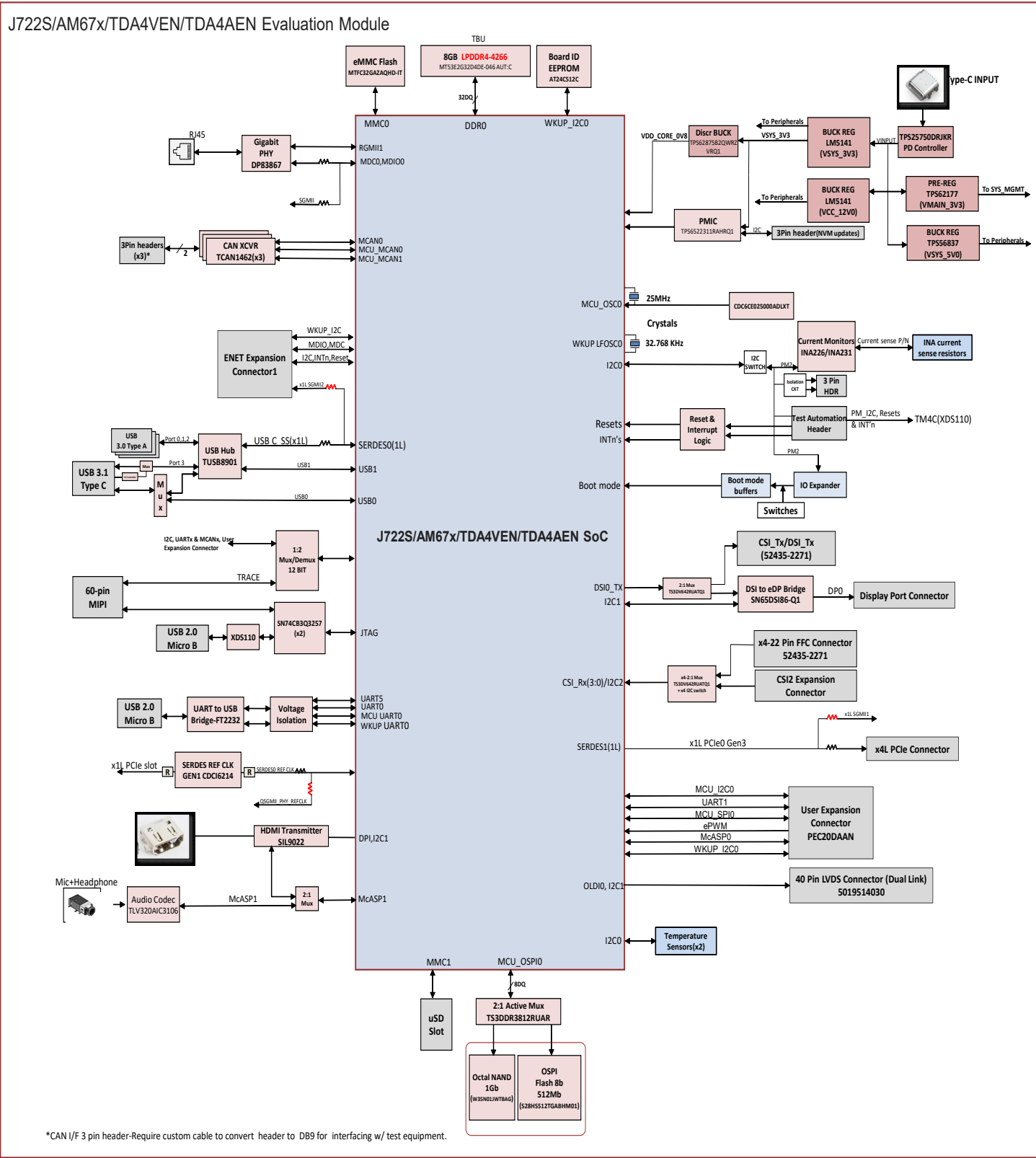
REVISION HISTORY #1

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	14 JUN 2023	Draft schematic	Mistral Design Team		
	0.2	26 JUN 2023	V0.11 Breakout schematic imported to core evm schematic			
	0.3	06 JULY 2023	Review comments updated			
	0.4	19 JULY 2023	Updated schematic to breakout V0.14			
	0.5	04 AUG 2023	Updated schematic to PDN 7G v0.16			
	0.6	05 SEPT 2023	Review comments updated			
	0.7	11 SEPT 2023	Board released to Fab	Mistral Design Team	TI	TI
	0.8	06 OCT 2023	Since LM61480Q5RPHRQ1 IC gives a default 5V0 output and does not need a resistor divider feedback. So,R443 is DNI'd and R448 is replaced with 0E. Feedback to VDD_RAM_0V85 supply is after the ferrite bead. There seems to be more noise in feedback. FL17 is replaced with 0E. Seeing 1.8V @ EN_TPS62177_ON signal which will enable the device even with jumper on J30. Replaced R775 with 0E in order to avoid voltage divide. Change in the compensation network values of 12V0 circuit. R438 is replaced with 10Kohm. To get default 100MHz clk from U10 LMK device, the enable should be either floating or pulled down. R58 is DNI'd to get default output. In order to source the 19.2MHz clock to DSI to eDP bridge external oscillator path is enabled by populating R410 and R412 DNI'd. Change in compensation values of 3V3 generation circuit to avoid initial power up issue. C241: 390pf, R385:7.5k, C240:3300pf I2C address text updated for U88 IO expander	Mistral Design Team	TI	TI
E2	0.9	15 Nov 2023	Replaced Compensation network for 12V0 and 3V3 values with new values suggested by TI Feedback VDDR supply is given before the FB Fix for TRACE DATA 13 U190 and U12 mux replaced with the mux which do not have internal pull down.			
	1.0	13 Dec 2023	LMK3H0102 devices are replaced with x2 NVM programmed parts. Resistor mount option changed for PCIe clock default to internal clock. Added support for RADAR(R-option or Mux for SPI on Expansion header) Added R-Option to connect MCU_OBSCLK and OBSCLK to test point.	Mistral Design Team	TI	TI
E3	1.1	11 JAN 2024	Added a open drain buffer to RGMII_INT# Signal Added 49.9E pull down resistors to SERDES REFCLK outputs. Pin VDD_MMC0 (W10) is connected to VDD_RAM_0v85 (non-filtered)			
	1.2	24 JAN 2024	Added 4x PMIC Resource Selection (RS[3:0]) bits to use diff PMIC power & GPIO resources and 5x 0E Rs to use diff interface signals on PMIC GPIO1,2 & 4 for supporting diff J722S/TDA4AEN/VEN PDN Schemes Updated RS[3:0] notes & fixed GPIO R-Muxes inadvertent REF DES changes back to existing R85 & R82 to enable net list generation. Changed power nets connected to VDD_MMC0 (BGA-W10) and input to PHY analog filters (FL23, 24 & 26) from VDD_RAM_0V85 to VDD_0V85 (new name) that is the output of 2:1 R-Mux which selects either VDD_RAM_0V85 or VDD_CORE as source for fixed 0.85V inputs per SoC operation & PDN diagrams. Changed following power net names to align with desired operation & PDN diagrams: From: VDD_IORET_0V75_xxx To: VDD_IORET_CORE_xxx TPS65224_EN PMIC_EN Added new 2:1 R-Mux (R6115 & R6114) to use VSYS_CAN_5V0 as input voltage to SD Card LDO (U191). This will remove the delayed ramp of VDD_SD_DV (LDO's Vo)) due to slow turn-on & ramp of VSYS_5V0.	Mistral Design Team	TI	TI
	1.3	02 FEB 2024	U57.4 Net name changed from USBC_PWR_EN to USBC_PWR_OUT_EN	Mistral Design Team	TI	TI

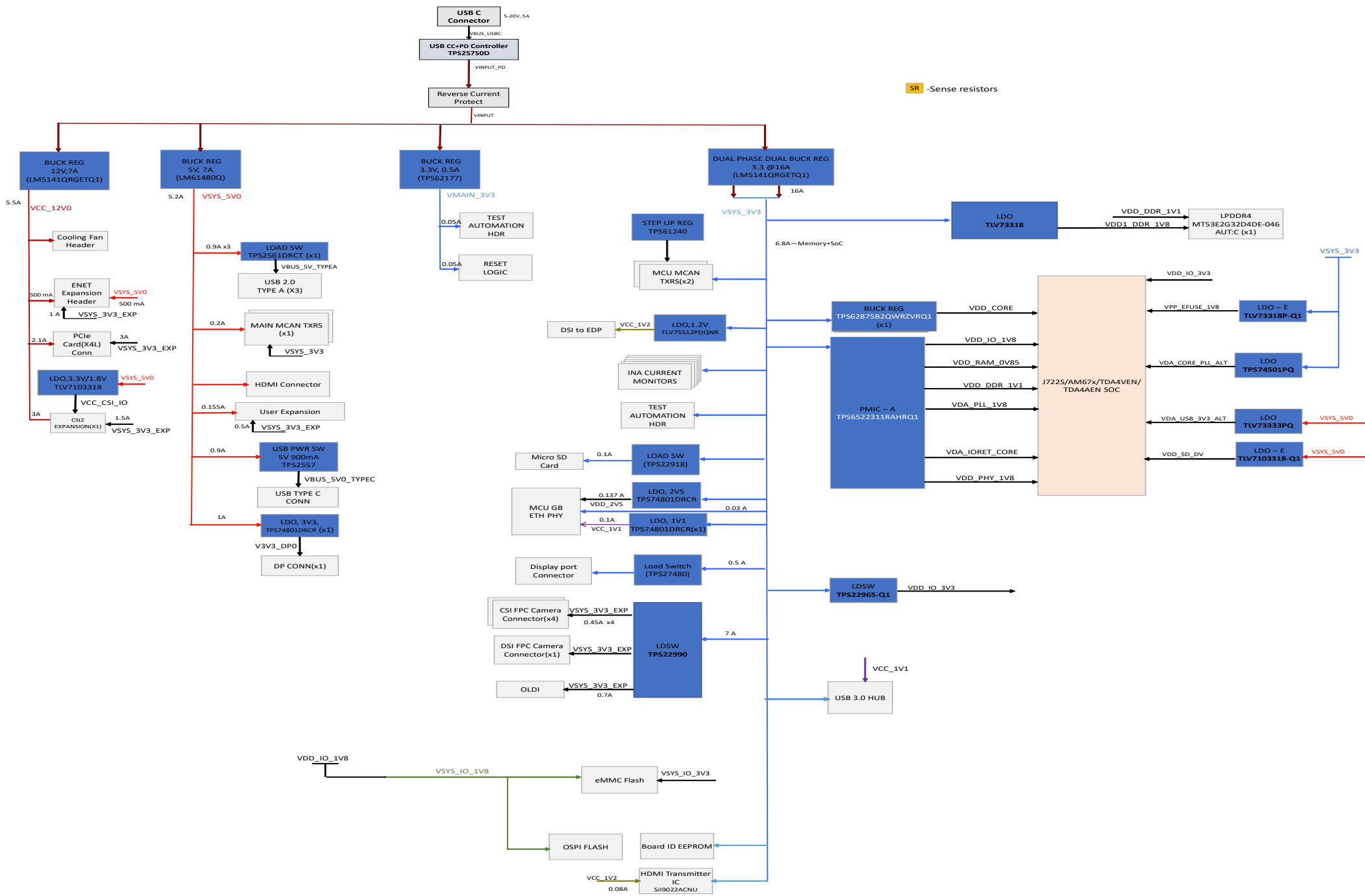
REVISION HISTORY #2

Project : J7 EVM			Title REVISION HISTORY#2			
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BLOCK DIAGRAM

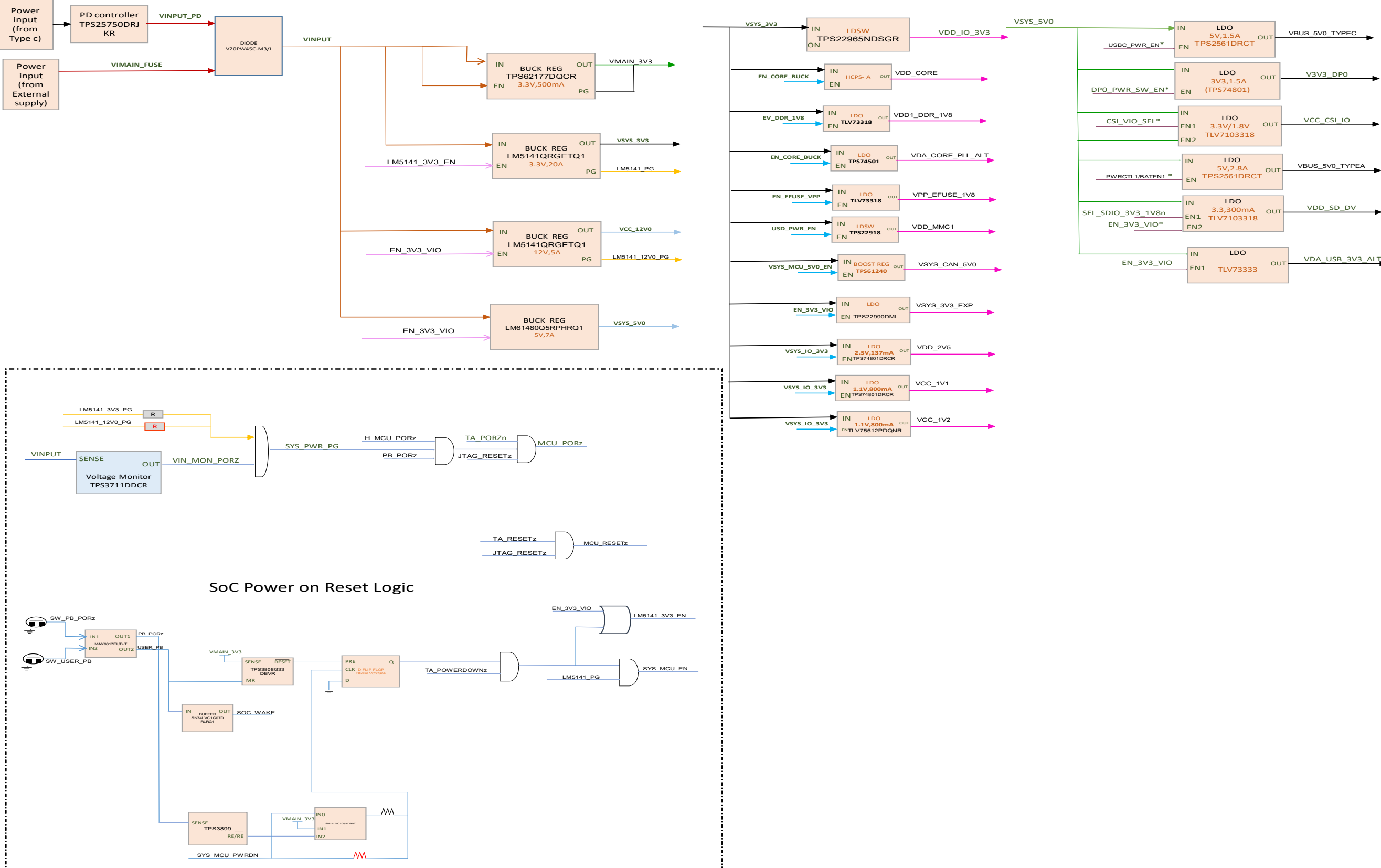


POWER FLOW DIAGRAM



POWER SEQUENCE

J722S TDA4VEN TDA4AEN AM67 Board Power Sequencing



Project

J7 EV



POWER SEQUENCE

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PDN

Legend:

Power Rails
PDN base
MCU Only/Island
Partial IO Retention (aka GPIO Ret)
DDR Retention (aka S2R)
End Product option
Peripheral loads (SW config'd after boot)

Control Signals:
General ctrl & logic
(Traffic = SW config'd after boot)
PDN base ctrl
Func Safety
GPIO Retention
DDR Retention (aka S2R)
End Product option
Peripheral comps

- Note items
- On-Chip "Pwr OK" Monitors (OV & UV)
- On-Chip "Pwr OK" Monitors (UV only)
- Provisioned In-Line Supply Filter
- High-lighted diagram changes

Burton PMIC-A, PN TP56522311-Q1 (3.5A bucks; 223 = ADC & 221 = No ADC; NVM ID = 11, NVM Rev = 0)
HCPS, Orchid PN TP56287582QWRZVRQ1 (PN ID = 5 for 20A max lo, Jacinto 7 PN = 82)

Features Supported (EVM Max Features):

- SoC's 4x A53s clock at 1.4GHz with SERDES operational per "EVM" use case (EVM UC combines FCD + CMS use cases)
- Functional Safety: ASIL-B capable system
- SDRAM: 1x EMIF with LPDDR4 (32Gb, 4x Die, 32b, 4000MTs, VIO = 1.1V)
- Flash: Octal SPI or NOR-Flash for boot & eMMC for mass storage
- Dual Voltage Signaling: Dual VIO (3.3/1.8V)
- Low power modes:
 - Partial IO Retention
 - Partial IO + DDR Retention

J722S EVM Burton PMIC + Orchid HCPS PDN-7G

(All SoC PN variants: TDA4AEN/VEN)
(Power Rail & GPIO Mapping Overview)

V0.22 10/10/2023 BMC 1. Updated Single Bit Dual Supply T-State buffer PN interfaced to PMIC's GPIO6 per SCH

V0.23 12/8/23 BMC 1. Added power mapping R-Muxes labels (PM#) to identify population options for alternative power maps supported by SoC
01/10/24 2. Updated Pwr-Mux (PM) resistor Ref Des #s to align with released vE1 assignments

7. End Product Options:

- Compliant high-speed UHS-I SD Card
- Best Effort USB 2.0 data eye (analog filter VDD_IO_3V3 to reduce noise for better eye)
- HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 ctrl signal)

Notes:

1) ASIL-B Functional Safety (FuSa) requires voltage monitoring (VMON) of all "safety critical" power rails (i.e. key SoC supplies) that could cause severe system failures. This classification depends on the end product use case & system resources a customer is using that can impact product safety. The PMIC & SoC have internal OV & UV monitoring for key SoC input supply voltages. The status is reported by each device's internal registers (i.e. SoC's Power OK (POK) status bits). PMIC & SoC VMON inputs (i.e. PMIC's VMONs, SoC's VMONs, JR_VEXTxxx) can be used to extend VMON to a few board level power rails (i.e. HCPS buck's VDD_CORE, load switch's VDD_IO_3V3). The following SoC & SDRAM supplies can be considered non-critical wrt FuSa & typically do not require direct OV/UV monitoring: VDDSHV (SD Card), VPP, VDDA_3P3_USB & VDD1_LPDDR4_1V8.

2) PDN default configuration supports 2x Retention (RET) Low Power modes: 1) Partial IO Only and 2) Partial IO + DDR; please note: DDR Ret alone is not supported by:

- Keeping key IO & DDR supplies energized (per power rail color coding: Partial IO RET & DDR RET) while all other SoC supplies are disabled
- Using the "Always ON" VSYS_3V3 pre-reg Vout to supply SoC's VDDSHV_CANUART that enables "CANUART IO signal toggling" to wake-up the system.
- Using controllable power resources (PMIC, Buck, LDO, Load Switch) that can be disabled per SoC power down seq to enter low pwr mode (reduced SoC power) and enabled per SoC power up seq to exit from low pwr mode and return to full active SoC operations.
- Using 1x I2C channel for SoC & PMIC communications that combines PMIC control & status with FuSa operations (i.e. servicing Watchdog Timer) that enables GPIO1 (= nRSTN2P function) connection to SoC's PMIC_LPM_EN signal that commands PMIC to enter (low) & exit (high) low power RET modes.
- Arming the PDN PFSM by SW I2C writes to set PMIC I2C_TRIGGER_# register bits that direct which RET mode to enter when PMIC_LPM_EN signal asserts as follows:

I2C TRIG_7	I2C TRIG_5	PDN State
0	0	SoC remains in Full Active state
0	1	Enters "IO/Partial IO Only RET" low pwr mode (same as J7xxx PDN-3x systems for SW compatibility)
1	0	SoC remains in Full Active state
1	1	Enters "IO/Partial IO + DDR RET" low pwr mode (same as J7xxx PDN-3x systems for SW compatibility)

3) PMIC's ENVPB/SENSE input pin has 3x diff selectable functions per data sheet. The VSENSE function was selected as NVM default setting to gain an "early warning" of input battery loss event so that a PMIC controlled power down seq can begin as soon as possible.

4) PMIC's GPIO6 supports 2x PDN operations:

- DISABLE_WDOG: PMIC latches logic level at GPIO6 pin at PMIC's W at Enable state just before beginning a start-up sequence.
 - High level at GPIO6 pin (SW I2C/MP-1 = closed/installed) directs PMIC to disable Watch-Dog Timer (setting WDOG_PWRHOLD bit to disable timer's long-window time-out).
 - Low level at GPIO6 pin (due to discrete load switch or LDO2 both having pull-down to Gnd whenever disabled) directs PMIC to enable Watch-Dog Timer (setting WDOG_PWRHOLD bit to enable timer's long-window time-out).
- During the W at Enable state, the VSYS_IO_1V8 supply will not be energized yet which will keep the Bi-Dir Voltage Translator output tri-stated. Thus connecting Rst to VSYS_3V3 (only energized supply) will set a high level logic on PMIC's GPIO6 pin.
- SAFETY_ERRORn: During power up seq, PMIC's PFSM sets GPIO6 = Error Signal Monitor (ESM) function to enable PMIC to capture SoC SAFETY_ERRORn pulses.
 - EVM's default configuration is to connect SoC's MCU_ERRORn signal to PMIC's GPIO6/ESM function.
 - An AND gate with inputs connected to SoC's MCU & MAIN_SAFETY_ERRORn signals enables logical combination of both error signals for PMIC's GPIO6/ESM function. The SoC's MAIN_ERRORn signal is an behind Trace & GPIC interfaces that the EVM must support. Therefore, an in-line sw switch typically isolates the MAIN_ERRORn net from the SoC and a Rst to VSYS_IO_3V3 is attached to enable the MCU_ERRORn signal to pass through the AND gate as default connection to PMIC's ESM function. If testing of a combined MCU & MAIN_ERRORn signal is desired, then reconfiguration of SoC's PMIMUX settings to output MAIN_ERRORn and EVM mux switch to connect with the AND gate input will be required.

5) PMIC GPIOs 1 & 2 are connected to SoC's PMIC_LPM_EN & TRIG_WDOG signals by default configuration. An alternative connection to a 2nd SoC I2C bus has been provisioned as a short-term option (if needed) until a single I2C bus that combines PMIC control & status with FuSa operations can become operational. No low power modes can be supported until this single I2C bus is supported since PMIC_LPM_EN must interface to GPIO1 to implement any low power modes.

6) PMIC ext voltage monitoring (VMON) are needed for VDD_CORE & VDD_IO_3V3 rails supplied from discrete power devices for FuSa ASIL-B. NVM settings provide:

- Differential voltage monitoring is needed for VDD_CORE since supply is < 1.0V. So PMIC's diff VMON feature using VMONL_P input pin & GPIO3 = VMONL_M function are needed
- Single-Ended VMON2 uses GPIO4 = VMON2 function for monitoring VDD_IO_3V3 since supply > 1.0V and a discrete load switch is used for loads > 165mA
 - PMIC's internal VMON of LDO2 Vout can be used and GPIO4 function can be reassigned (i.e. system GPIO, ADC_IN, etc.) by SW after boot if desired.

7) VDD_IO_3V3 power rail could be supplied by 2x different load switches based upon max load as follows:

- Discrete load switch for loads > 165mA
 - PMIC's LDO2 Vout (3.3V) will be used as the control signal for the discrete load switch.
 - PMIC's GPIO4 = VMON2 function is needed to provide OV/UV VMON coverage for FuSa ASIL-B on output side of discrete load switch.
- PMIC's LDO2 In Bypass mode for loads > 165mA (limits IR-drop to 1% (33mV) across bypass FET with a max 200mOhm Ron)
 - PMIC's internal VMON of LDO2 Vout can be used and GPIO4 function can be reassigned (i.e. system GPIO, ADC_IN, etc.) by SW after boot if desired.

8) PDN shows default option to supply SoC's VDDA_PLL from a filtered VDD_CORE rail and VDDA_OP05_xxx from a filtered VDD_RAM_OV05 rail. An option has been provisioned to supply either of these VDDA_xxx inputs from a discrete low noise LDO in case default power rails have any negative impact on PLL or DLL operations.

9) PDN shows default option to supply SoC's VDDA_3P3_USB from the digital VDD_IO_3V3 rail with in-line supply filter to reduce switching noise to give "reasonable" USB 2.0 data eye performance for product development tasks. An option has been provisioned to supply VDDA_3P3_USB from a low noise LDO derived from a VSYS_5V input to give optimal USB 2.0 data eye performance if needed. If USB 2.0/VF is not used, then the digital VDD_IO_3V3 rail can supply VDDA_3P3_USB directly without in-line analog filter.

10) PDN shows default option to supply SoC's VDDSHV5 from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed UHS-I SD card operation. Filtering digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but restricts data rates to standard 12Mb/s for 3.3V data signaling levels. If only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used. If SD card is not used, then digital VDD_IO_3V3 rail without supply filter can be used.

11) PDN shows default option to supply SoC's VPP from a 400mA rated LDO (i.e. PNs: TP5745-Q1 & TP5742L-Q1) with fast transient response, active pull-down on Vout and SoC GPIO signal for enable control. This configuration supports the capability for "in-the-field" Efuse programming updates to High Security (HS) SoCs. SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP and pre-programmed HS devices can leave the VPP input supply unconnected per DM since no Efuse programming is needed.

12) PDN shows default option to supply SoC's VDD_CANUART from an independent Buck via VDD_IJRET_OV75 rail to allow Partial IO Retention low power mode by disabling all but 2x SoC input supplies: VDD_CANUART & VDDSHV_CANUART. An option to supply all SoC low voltage core processing supplies (< 1.1V) from a common 0.85V VDD_CORE power rail to reduce PDN BOM cost has been provisioned for future testing if needed.

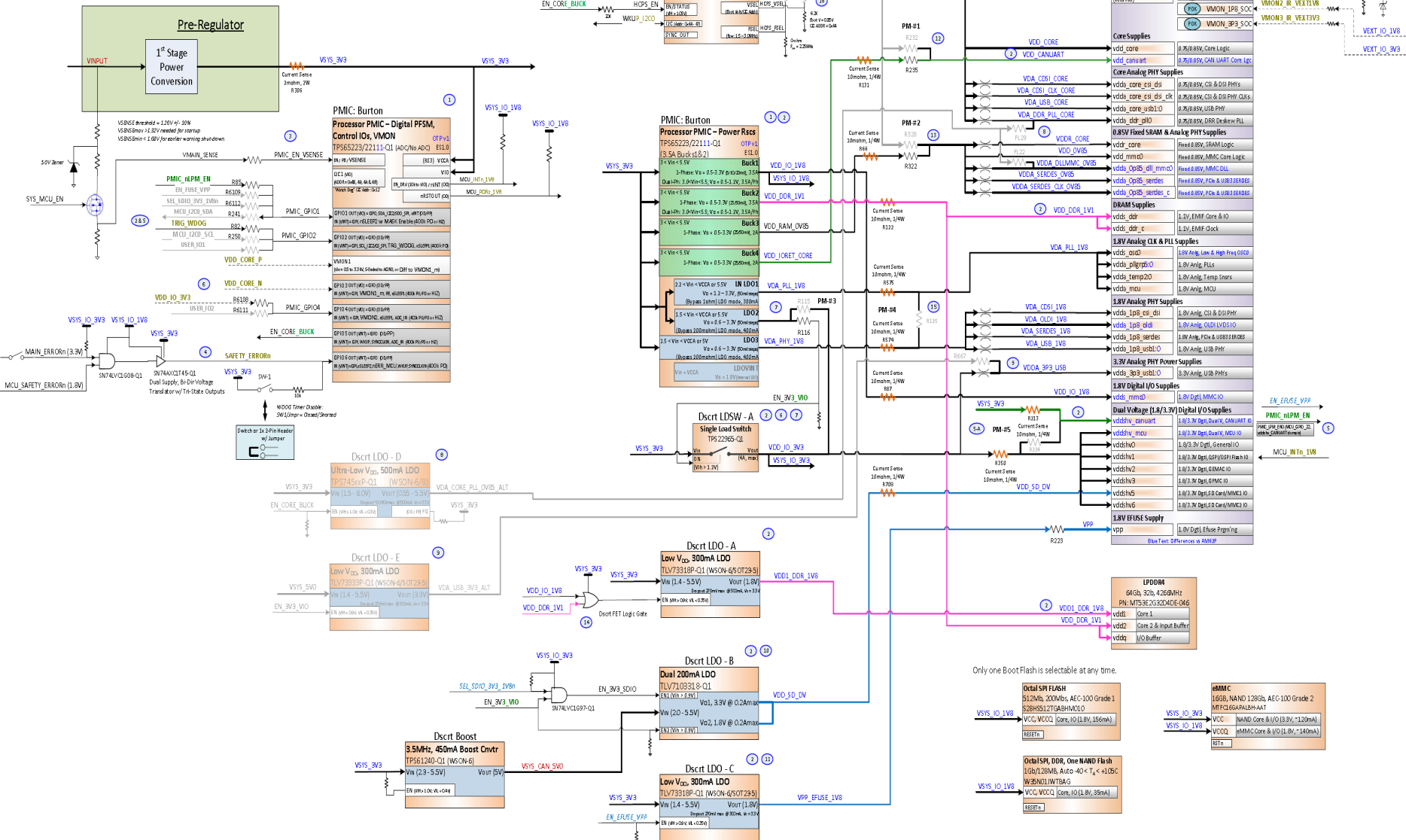
13) PDN shows default option to supply SoC's fixed 0.85V inputs (VDD_CORE, VDD_MMIO, VDDA_OP05_xxx) from an independent Buck via VDD_RAM_OV05 rail which allows VDD_CORE rail to operate at 0.75V for reduced power. An option to supply all SoC low voltage core processing supplies (< 1.1V) from a common 0.85V VDD_CORE power rail to reduce PDN BOM cost has been provisioned for future testing if needed.

14) An OR gate function is needed to keep the discrete LDO enabled that supplies 1.8V to LPDDR4 VDD1 (Internal bias voltage) during IO + DDR Ret low power mode. The OR gate must operate at Vthmin = 1.045V (1.1V - 5%) input signal using VSYS_3V3 supply since all other supplies will be disabled besides VSYS_3V3, VDD_DOR_LV1 & VDD1_LDR_1V8. The 2x typ single-gate (n listed below) do not meet the desired Vthmin = 1.045V: 1) Multi-Function Gate (SN74VLC1G97-Q1) has Vth 1.5 - 1.9V for 3.0V supply. 2) Single OR Gate (SN74VLC1G32-Q1) has Vth min 2V for 3 - 3.3V supply. Therefore, a discrete FET OR gate circuit that meets desired Vthmin = 1.045 has been used.

15) PDN shows default option to supply SoC's VDDA_OSC/PLL/TEMP/MCU & VDDA_1P8_CSDS/OLDI/SERDES/USB input supply groups from 2x independent PMIC LDOs via VDA_PLL_1V8 & VDA_PHY_1V8 power rails to avoid possible high-speed PHY switching transient impacts to OSC/PLL/TEMP/MCU supplies/SoC clocking. An option to supply all SoC 1.8V analog supplies from a common 1.8V PMIC LDO/power rail has been provisioned for future testing to min BOM cost & PCB area by enabling PDN/PMIC resource optimizations.

16) PDN shows default option to supply SoC's VDD_CORE from 1x discrete Orchid high-current buck (TP58726/45/6/2-Q1 with Max Currents 15A/20A/25A/30A). The VSEL input pin sets the boot voltage and I2C address assignments according to the VSEL state table connections to Vin or Gnd:

VSEL connection	Default output voltage	I2C device address	Drop compensation	Transient non-sys mode
VSEL GND to GND	0.85V	0x48	disabled	disabled
VSEL GND to GND	0.75V	0x45	disabled	disabled
VSEL GND to Vth	0.875V	0x46	disabled	disabled
VSEL with 4K to VIN	0.8V	0x47	disabled	disabled



Project :
J7 EVM

Title
PDN

Size
PROC170 002 EVM

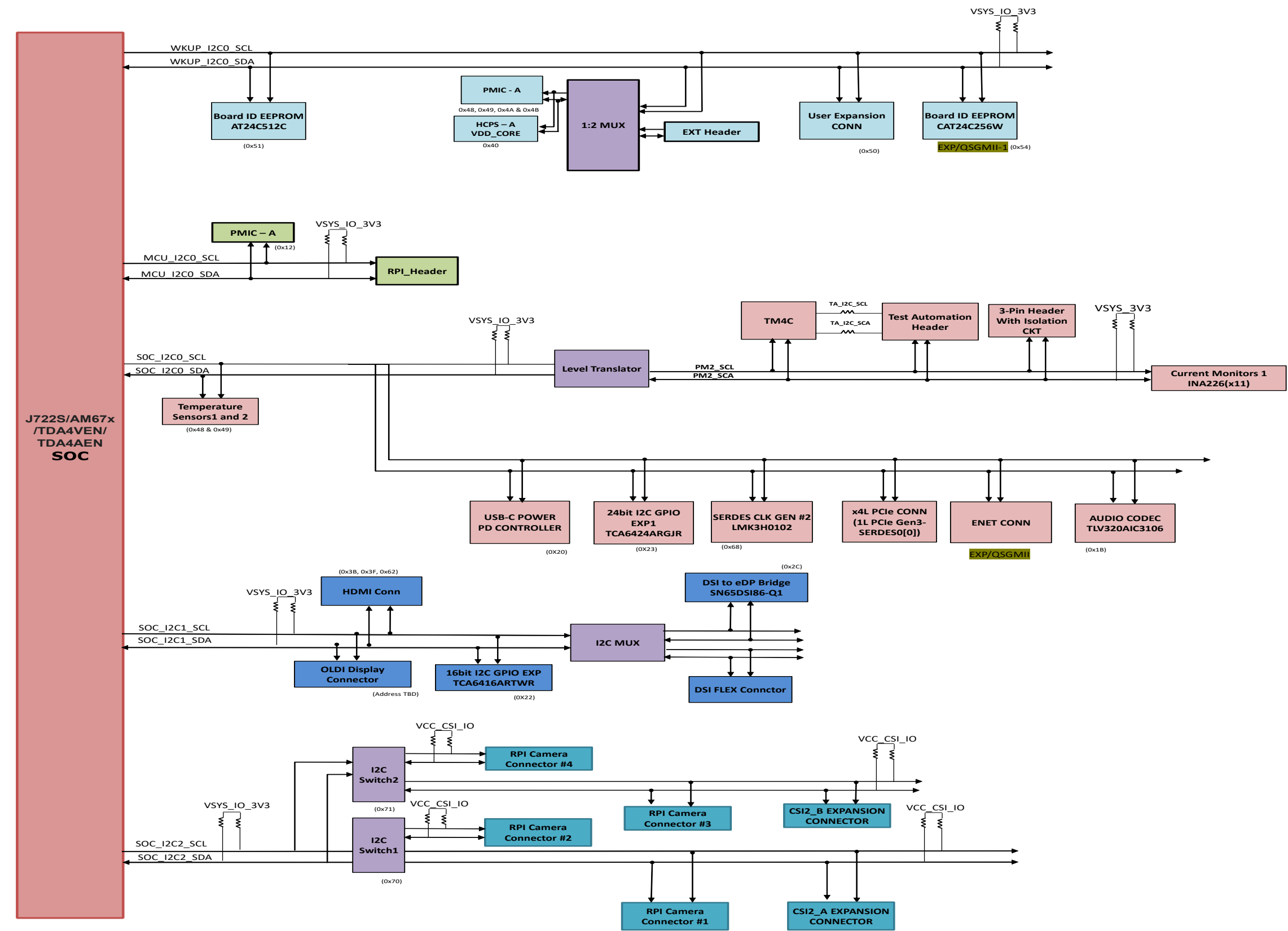
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I2C TREE



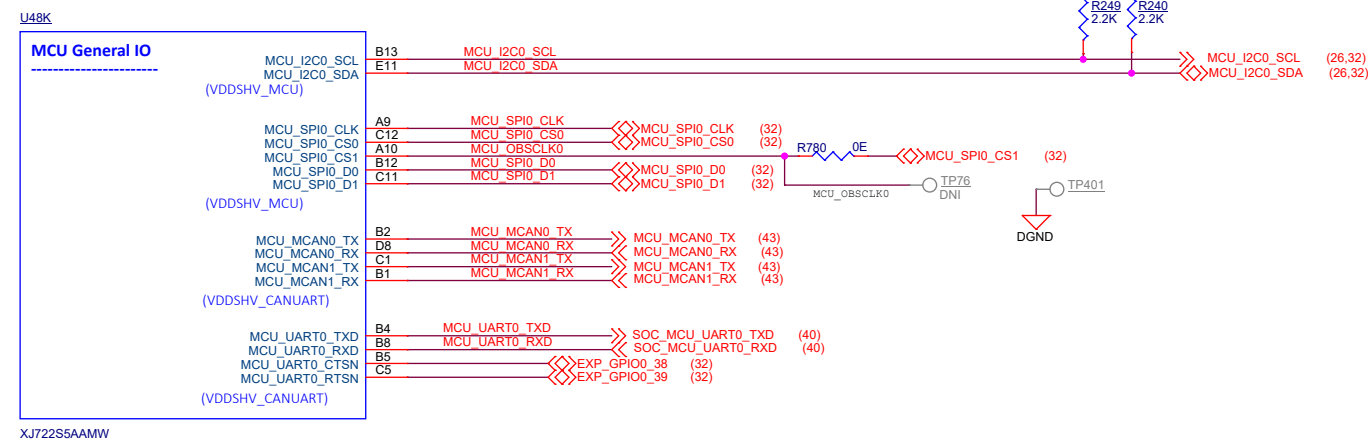
I2C TABLE

BOARD	DEVICE DESCRIPTION	PART#	ADDRESS	J722S TDA4VEN TDA4AEN AM67 PORT MAPPING
EVM	Board ID EEPROM	AT24C512C-MAHM-T	0X51	WKUP_I2C0
EXP/QSGMII -1	Board ID EEPROM	CAT24C256WI-GT3	0X54	
EXPANSION	User Expansion Connector	<connector interface>	0X50	
EVM	VDD_CORE REGULATOR	TPS62875	0X44	
EVM	PMIC	TPS65221-Q1	0x48,0x49, 0x4A, 0x4B	
EXPANSION	User Expansion Connector	<connector interface>		MCU_I2C0
EVM	PMIC	TPS65221-Q1	NA	
EXP/QSGMII -1	ENET	<connector interface>		SOC_I2C0
EVM	IO Expander 1	TCA6424ARGJR	0X23	
EVM	Temperature Sensors	TMP100NA/3K	0X48,0X49	
EVM	AUDIO CODEC	TLV320AIC3106IRGZT	0X1B	
EVM	Test automation	FH12A-40S		
EVM	x1LANE PCIe0	<connector interface>		
EVM	USB C PD Controller	TPS25750D	0X20	
EVM	INA226 device for VDD_CORE	INA226AIDGSR	0X40	
EVM	INA226 device for VDD_RAM_0V85	INA226AIDGSR	0X41	
EVM	INA226 device for VDA_PHY_1V8	INA226AIDGSR	0X42	
EVM	INA226 device for VDD_IOPRET_CORE	INA226AIDGSR	0X43	
EVM	INA226 device for VDD_SD_DV	INA226AIDGSR	0X44	
EVM	INA226 device for VDD_IO_1V8	INA226AIDGSR	0X45	
EVM	INA226 device for VSYS_3V3	INA226AIDGSR	0X46	
EVM	INA226 device for VDD_DDR_1V1	INA226AIDGSR	0X47	
EVM	INA226 device for VDD_IO_3V3	INA226AIDGSR	0X4C	
EVM	INA226 device for VDA_PLL_1V8	INA226AIDGSR	0X4D	
	INA226 device for VDD1_DDR_1V8	INA226AIDGSR	0X4E	
EVM	CLKGEN 2	LMK3H0102	0x68	
EVM	Bootmode Buffer	TCA6424ARGJR	0x22	TA_I2C_SCL
EVM	IO Expander	TCA6416ARTWR	0X20	SOC_I2C1
EVM	HDMI	SiI9022ACNU	0x3B, 0x3F, 0x62	
EVM	DSI Flex Connector	<connector interface>(Via Mux)		
EVM	DSI to eDP Bridge	SN65DSI86IPAPQ1(Via Mux)	0X2C	
EVM	OLDI	<connector interface>		
EVM	I2C switch	TCA9543APWR	0X70,0X71	SOC_I2C2(Via Mux)
EVM	CSI2_A Expansion Connector	QSH-020-01-L-D-DP-A-K(J1002)	From 0x70 Switch	CSIO_I2C2_SDA
EVM	FPC Camera Connector 1	CON_FLEX_22X1_52435(J1004)		
EVM	FPC Camera Connector 2	CON_FLEX_22X1_52435(J1005)		CSI1_I2C2_SDA
EVM	CSI2_B Expansion Connector	QSH-020-01-L-D-DP-A-K(J1003)	From 0x71 Switch	CSI2_I2C2_SDA
EVM	FPC Camera Connector 3	CON_FLEX_22X1_52435(J1006)		
EVM	FPC Camera Connector 4	CON_FLEX_22X1_52435(J1007)		CSI3_I2C2_SDA

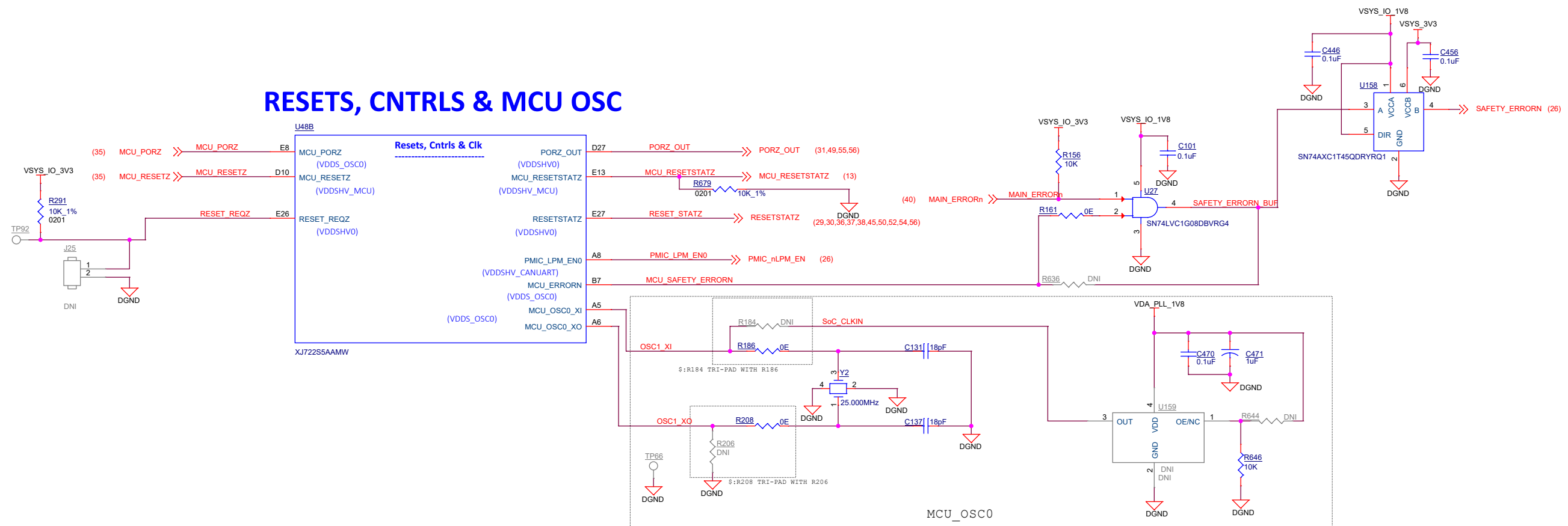
GPIO EXPANDER MAP/TABLE

	GPIO net name	Package Signal name	GPIO No	Input/Output	Default	State	Usage
SOC GPIO	SOC GPIO						
	MCU_INTn_1V8	OSPIO_CSN1	GPIO0_12	Input	PU	Active Low	PMIC Interrupt
	RGMII1_INT#	OSPIO_CSN2	GPIO0_13	Input	PU	Active low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
	OSPIO_INT#/ECC_FAIL	OSPIO_CSN3	GPIO0_14	Input	PU	Active Low	Interrupt from OSPI to SoC
	CSI2_EXP_A_GPIO0	GPMC0_CLK	GPIO0_31	IO	NA	NA	CSI2 Expansion Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO1	GPMC0_AD0	GPIO0_15	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO2	GPMC0_AD1	GPIO0_16	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO3	GPMC0_AD2	GPIO0_17	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO4	GPMC0_AD3	GPIO0_18	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO0	MMC2_CLK	GPIO0_69	IO	NA	NA	CSI2 Expansion Board Specific.
	CSI2_EXP_B_GPIO1	GPMC0_AD4	GPIO0_19	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO2	GPMC0_AD5	GPIO0_20	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO3	GPMC0_AD6	GPIO0_21	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO4	GPMC0_AD7	GPIO0_22	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	EXP_GPIO0_33	GPMC0_OEn_REn	GPIO0_33	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_36	GPMC0_BE1n	GPIO0_36	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_38	MCU_UART0_CTSn	MCU_GPIO0_7	IO	NA	NA	User Expansion Specific.
	EXP_GPIO0_39	MCU_UART0_RTSn	MCU_GPIO0_8	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_41	GPMC0_CSn0	GPIO0_41	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_42	GPMC0_CSn1	GPIO0_42	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	IOEXP1_INT#	MMC2_DAT1	GPIO0_67	Input	PU	Active low	Interrupt for IO Expander 1 ('0' - Interrupt, '1' - No interrupt)
	CSI2_EXP_RSTz	MMC2_DAT0	GPIO0_68	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	SEL_SDIO_3V3_1V8n	MMC2_CMD	GPIO0_70	Output	PU	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
	ENET1_EXP_INTB	MMC2_SDWP	GPIO0_72	Input	PU	Active low	ENET expansion 1 Interrupt signal
	EN_EFUSE_VPP	SPI0_D1	GPIO1_19	Output	PD	Active High	VPP_EFUSE LDO enable
	SYS_MCU_PWRDN	EXT_REFCLK1	GPIO1_30	Output	NA	Active low	SYS_MCU_PWRDN('1' - PWR ON, '0' - PWR OFF)
	TA_SOC_INT1z	EXTINTn	GPIO1_31	Input	PU	Active low	Test automation Interrupt to SOC
	SOC_GPIO1_49	MMC1_SDWP	GPIO1_49	Output	NA	Active High	User LED1 ('1' - LED ON, '0' - LED OFF)
	TA_SOC_INT2z/SOC_WAKE	WKUP_UART0_CTSn	MCU_GPIO0_11	Input	PU	Active low	Test automation Interrupt to SOC
	MCU_CAN_STB	WKUP_UART0_RTSn	MCU_GPIO0_12	Output	PU	Active High	Wake from IO retention mode
	TRIG_WDOG	WKUP_CLKOUT	MCU_GPIO0_23	Input	NA	Active Low	MCU CAN0 Standby
		MMC2_SDCD	GPIO0_71				Trigger WDOG to PMIC
							Open
I2C0/0X23	GPIO Expander - 1 Part # TCA6424ARGJR						
	TRC_MUX_SEL		P00	Output	PU	NA	Mux Select Line('0'- MCASP&User Expansion,'1'-TRC data)(Default to TRACE)
	OSPI/ONAND_MUX_SEL		P01	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPIO, '1' - OCTAL NAND)
	MCASP1_FET_SEL		P02	Output	PD	Active low	McASP1 FET SWITCH Select Line ('1' - Audio, '0' - HDMI)
	CTRL_PM_I2C_OE#		P03	Output	PU	Active High	I2c Switch Enable ('1' - Enable, '0' - Disable)
	CSI_VIO_SEL		P04	Output	DIP_SEL	Active High	LVC MOS IO Voltage Selection Enable Pin('0'- xxV, '1'- xxV)
	USB2_0_MUX_SEL		P05	Output	PD	Active low	Mux Select Line ('1'- D to 2D, '0'- D to 1D)
	CSI01_MUX_SEL_2		P06	Output	PD	Active low	CSI MUX select ('0'- D to A,'1'-D to B)
	CSI23_MUX_SEL_2		P07	Output	PD	Active low	CSI MUX select ('0'- D to A,'1'-D to B)
	LMK1_OE1		P10	Output	PU	Active low	Clock generator 1 Output 1 Enable
	LMK1_OE0		P11	Output	PU	Active low	Clock generator 1 Output 0 Enable
	LMK2_OE0		P12	Output	PU	Active low	Clock generator 2 Output 0 Enable
	LMK2_OE1		P13	Output	PU	Active low	Clock generator 2 Output 1 Enable
	GPIO_RGMII1_RST#		P14	Output	PU	Active low	Reset for RGMII ('1' - Enable, '0' - Disable)
	GPIO_AUD_RSTn		P15	Output	PU	Active low	Reset for Audio ('1' - Enable, '0' - Disable)
	GPIO_eMMC_RSTn		P16	Output	PU	Active low	Reset for Emmc ('1' - Enable, '0' - Disable)
	GPIO_uSD_PWR_EN		P17	Output	PU	Active High	Load switch ('1' - ON, '0' - OFF)
	USER_LED2		P20	Output	PD	Active low	User LED2 Enable ('1' - LED Off, '0' - LED On)
	MCAN0_STB		P21	Output	PU	Active High	MCAN0 Standby
	PCIe0_1L_RC_RSTz		P22	Output	PD	Active low	PCIe1 1-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	PCIe0_1L_PRSENT#		P23	Input	PU	Active High	PCIe0 1-Lane Hot Plug / Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	ENET1_EXP_SPARE2		P24	Input	NA	NA	Ethernet Expansion1 Spare2 ('0' - not defined, '1' - not defined)
	ENET1_EXP_PWRDN		P25	Output	PU	Active High	Ethernet Expansion1 PHY Powerdown ('0' - normal operation, '1' - device power down)
	ENET1_I2CMUX_SEL		P26	Output	PD	NA	Signal Mux Control ('0' - No Connect, '1' - I2C0)
	ENET1_EXP_RESETZ		P27	Output	PD	Active low	Ethernet Expansion1 Reset ('0' - device reset, '1' - normal operation)
I2C1/0X22	GPIO Expander - 2 Part # TCA6416ARTWR						
	DSI_Mux_SEL_2		P00	Output	PD	Active High	DSI Mux Select ('1'- DSI FPC Connector,'0'- DSI to EDP)
	GPIO_eDP_ENABLE		P01	Output	PD	Active High	eDP Bridge Enable
	DPO_PWR_SW_EN		P02	Output	PD	Active High	Enalbe for Display port LDO
	GPIO_OLDI_RSTn		P03	Output	PD	Active low	Reset for OLDI ('1' - Enable, '0' - Disable)
	GPIO_HDMI_RSTn		P04	Output	PD	Active low	HDMI Transmitter Reset Control GPIO
	HDMI_LS_OE		P05	Output	PD	NA	HDMI ESD Device
	PCIe0_1L_PERSTz		P06	Input	NA	NA	PCIe0 1-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	DSI_GPIO0		P10	IO	NA	NA	DSI flex Connector
	DSI_GPIO1		P11	IO	NA	NA	DSI flex Connector
	DSI_EDID		P12	Input	NA	Active low	Interrupt
	IO_eDP_IRQ		P13	Input	PU	NA	Interrupt signal from DSI to eDP bridge
	OLDI_INT#		P14	Input	PU	Active low	Interrupt from OLDI display
	HDMI_INTn		P15	Input	PU	Active low	Interrupt from HDMI display

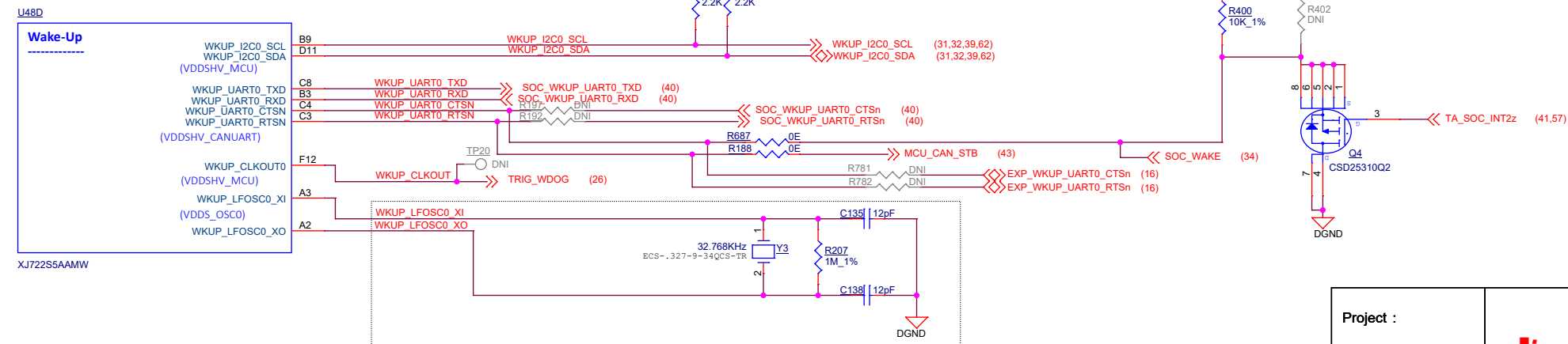
MCU GENERAL IO



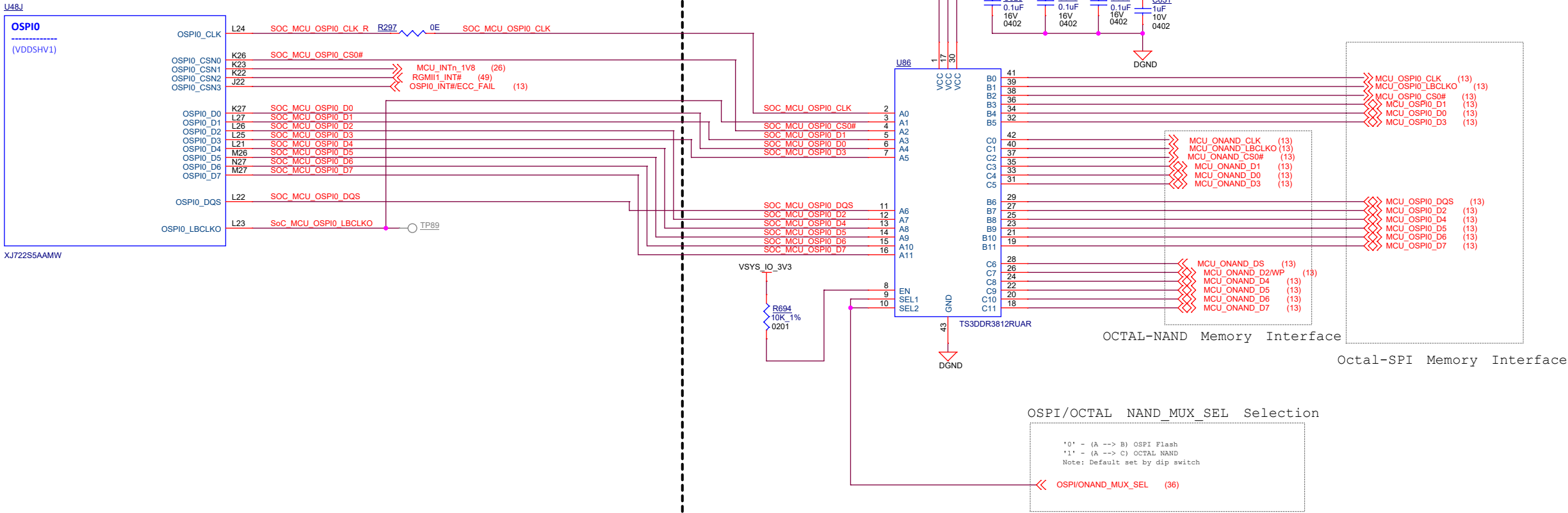
RESETS, CNTRLS & MCU OSC



WKUP RESETS, CNTRLS & OSC



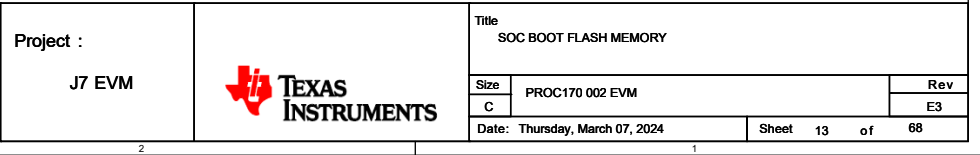
OSPI



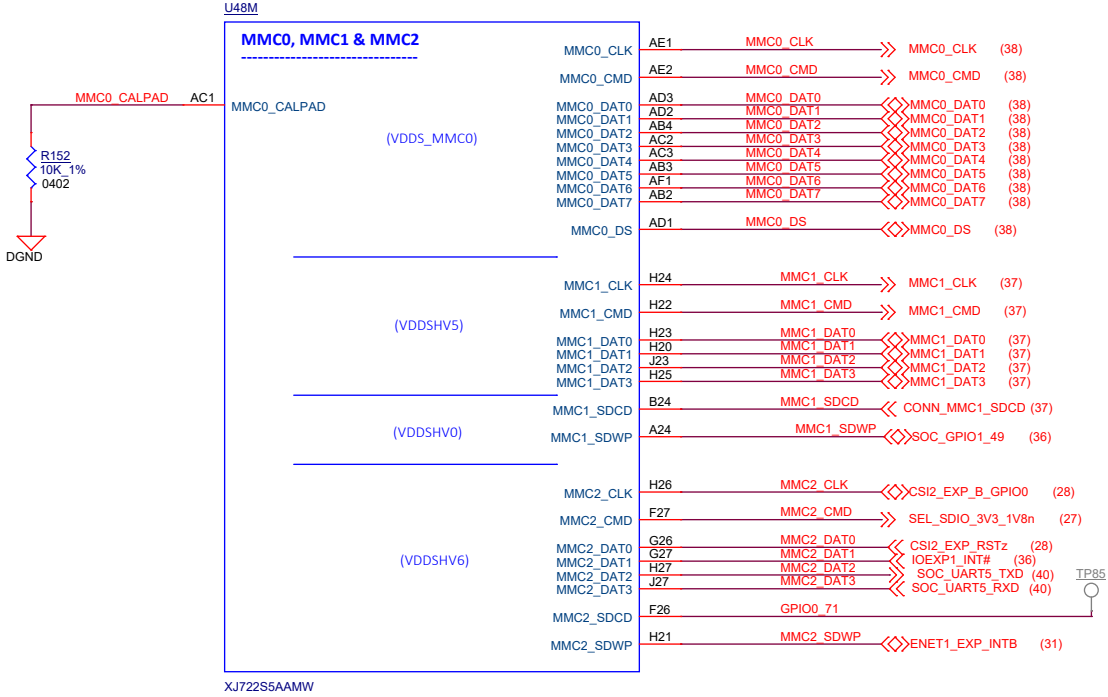
EVM development & evaluation test circuitry

(TI EVM Only)

2:1 Mux for OSPI/OCTAL NAND

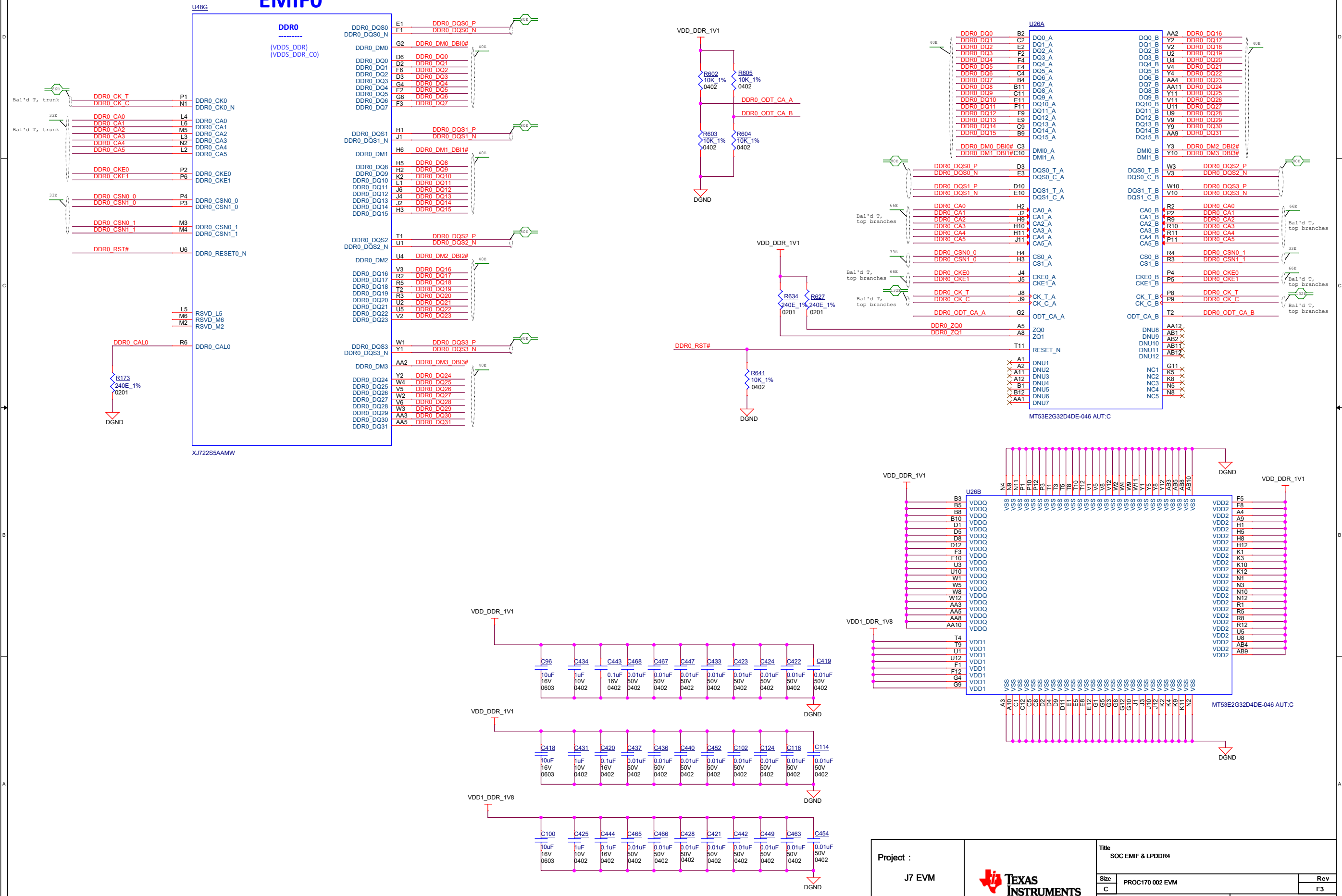


MMC 0, 1, 2



LPDDR4 MEMORY I/F

EMIF0



U48A

General IO

(VDDSHV0)

General IO

(VDDSHV0)

I2C0_SCL D23 I2C0_SCL

I2C0_SDA B22 I2C0_SDA

I2C1_SCL C24 I2C1_SCL

I2C1_SDA A22 I2C1_SDA

SPI0_CLK D20 SPI0_CLK

SPI0_CS0 B20 SPI0_CS0

SPI0_CS1 C20 SPI0_CS1

SPI0_D0 E19 SPI0_D0

SPI0_D1 E20 SPI0_D1

UART0_TXD F20 UART0_TXD

UART0_RXD F19 UART0_RXD

UART0_CTSN E22 UART0_CTSN

UART0_RTSN B21 UART0_RTSN

EXTINTN B23 EXTINTN

EXT_REFCLK1 A23 EXT_REFCLK1

MCAN0_TX D22 MCAN0_TX

MCAN0_RX C22 MCAN0_RX

MCASP0_ACLKR F24 MCASP0_ACLKR

MCASP0_AFSR C27 MCASP0_AFSR

MCASP0_AXR0 F23 MCASP0_AXR0

MCASP0_AXR1 B25 MCASP0_AXR1

MCASP0_AXR2 A26 MCASP0_AXR2

MCASP0_AXR3 A25 MCASP0_AXR3

MCASP0_ACLKX D25 MCASP0_ACLKX

MCASP0_AFSX C26 MCASP0_AFSX

SOC_I2C0_SCL (31,33,36,39,50,55,57,58)

SOC_I2C0_SDA (31,33,36,39,50,55,57,58)

I2C1_SCL

I2C1_SDA

SOC_I2C1_SCL (36,52,54)

SOC_I2C1_SDA (36,52,54)

EHRPWM1_A (32)

EHRPWM1_B (32)

ECAP0_IN_APWM_OUT (32)

EN_FUSE_VPP (27)

EXP_GPIO1_19 (16)

SOC_UART0_TXD (40)

SOC_UART0_RXD (40)

UART0_CTSN (40)

UART0_RTSN (40)

SYS_MCU_PWRDN (34)

MCAN0_TX (44)

MCAN0_RX (44)

UART1_TXD (32)

UART1_RXD (32)

MCASP0_AXR0 (32)

MCASP0_AXR1 (32)

MCASP0_AXR2 (32)

MCASP0_AXR3 (32)

MCASP0_ACLKX (32)

MCASP0_AFSX (32)

VSYS_IO_3V3

R690 10K

Q5 CSD25310Q2

DGND

TA_SOC_INT1z (41,57)

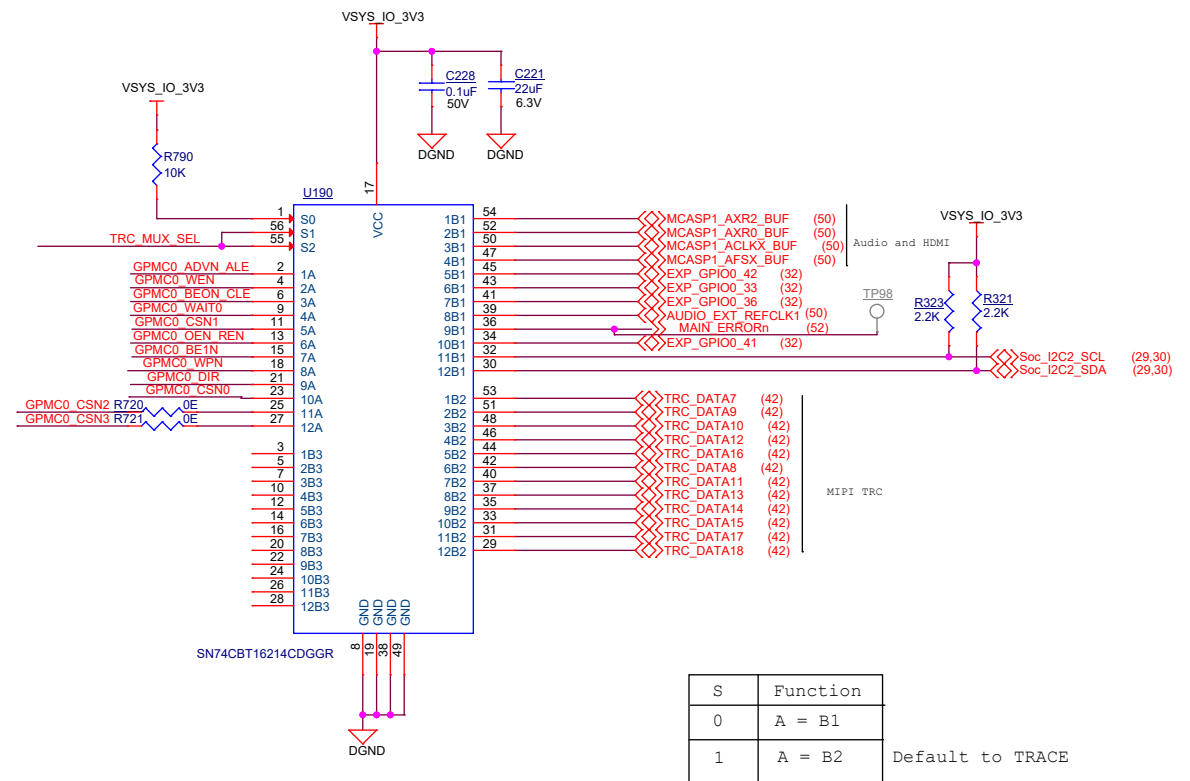
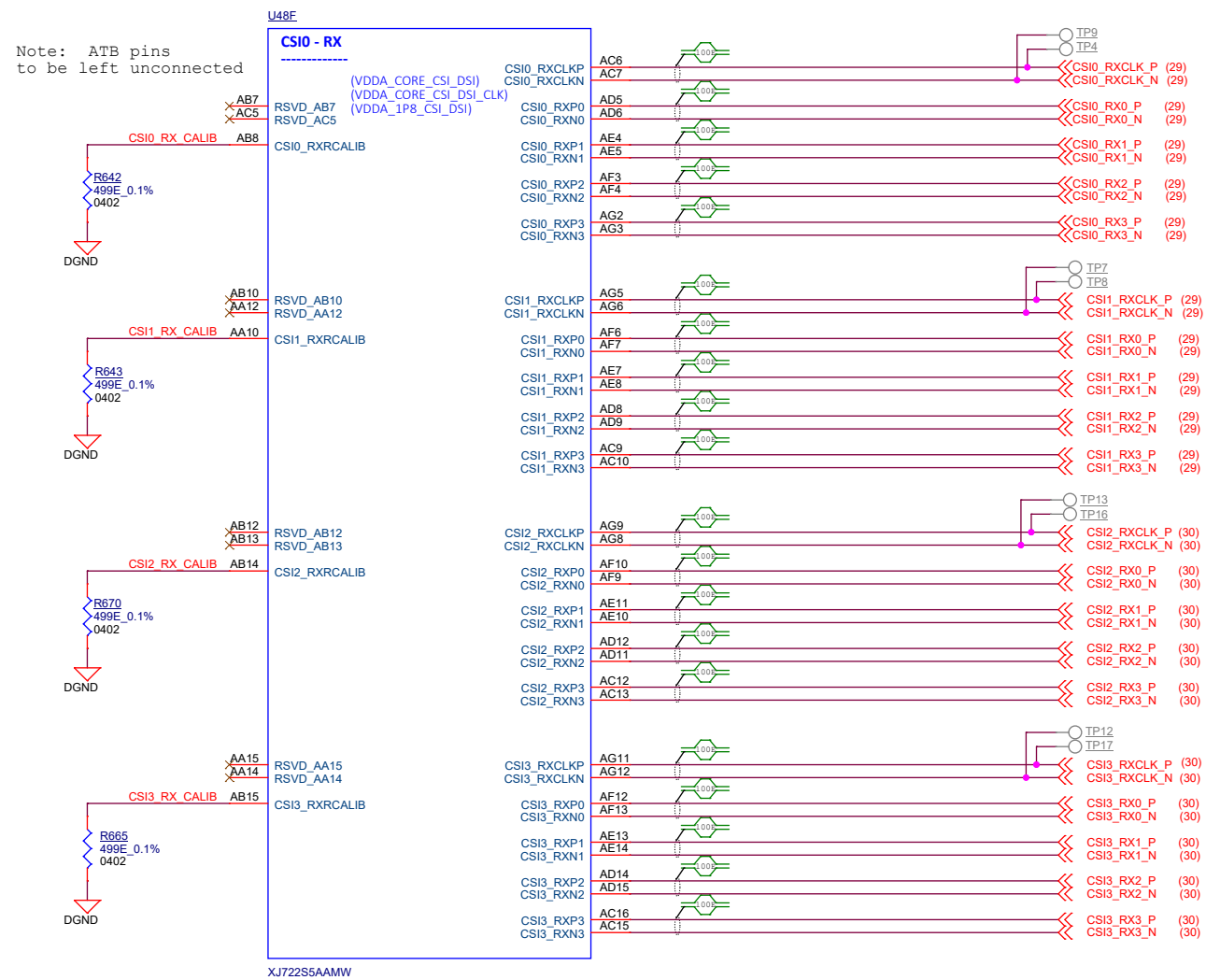
[illegible]

Figure 10: Pin connections for the ATmega328P microcontroller. The diagram shows the pin connections for the ATmega328P, including power pins (VCC, GND), reset pins (RESET), and various I/O pins (AD, GPMC, VOUT, OBSCLK, R784, UE). The pins are numbered 1 to 40, and the connections are color-coded: red for power, blue for reset, and green for I/O. The ATmega328P is shown in a 28-pin package, with pins 1 to 28 on the left and pins 29 to 40 on the right. The connections are as follows:

- Pin 1: VCC
- Pin 2: GND
- Pin 3: RESET
- Pin 4: AD0
- Pin 5: AD1
- Pin 6: AD2
- Pin 7: AD3
- Pin 8: AD4
- Pin 9: AD5
- Pin 10: AD6
- Pin 11: AD7
- Pin 12: AD8
- Pin 13: AD9
- Pin 14: AD10
- Pin 15: AD11
- Pin 16: AD12
- Pin 17: AD13
- Pin 18: AD14
- Pin 19: AD15
- Pin 20: AD16
- Pin 21: AD17
- Pin 22: AD18
- Pin 23: AD19
- Pin 24: AD20
- Pin 25: AD21
- Pin 26: AD22
- Pin 27: AD23
- Pin 28: AD24
- Pin 29: GND
- Pin 30: VCC
- Pin 31: RESET
- Pin 32: AD0
- Pin 33: AD1
- Pin 34: AD2
- Pin 35: AD3
- Pin 36: AD4
- Pin 37: AD5
- Pin 38: AD6
- Pin 39: AD7
- Pin 40: AD8

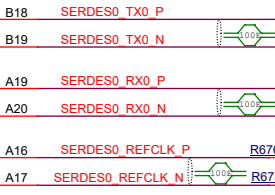
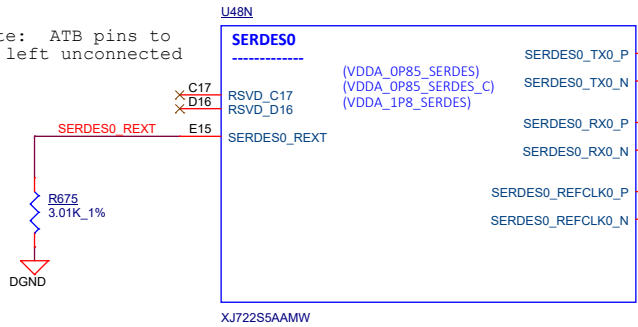
The diagram shows two test points, TP403 and TP402, connected to a common ground. TP403 is connected to a signal line labeled OBCLK0. TP402 is connected to a ground symbol labeled DGND.

CSI 0, 1, 2, 3



SERDES0

Note: ATB pins to be left unconnected



R63 DNI

R60 DNI

C153 DNI

C157 DNI

R269 DNI

R278 DNI

R796 DNI

R797 DNI

DGND

For External 156.25MHz Clk support:
DNI: R676, R678
Assemble: R64,R59,R63,R60

For SoC 156.25MHz Clk support:
DNI: R64,R59
Assemble: R676,R678,R63, R60

ENET EXPANSION

QSGMII1_PHY_REFCLK_P (31)

QSGMII1_PHY_REFCLK_N (31)

SGMII2_TX0_P (31)

SGMII2_TX0_N (31)

SGMII2_RX0_P (31)

SGMII2_RX0_N (31)

USB 3.0 HUB

USBC_SS_TX0_P (45)

USBC_SS_TX0_N (45)

USBC_SS_RX0_P (45)

USBC_SS_RX0_N (45)

CLKGEN_SERDES0_REFCLK_P (33)

CLKGEN_SERDES0_REFCLK_N (33)

ENET EXPANSION

SGMII1_TX0_P (31)

SGMII1_TX0_N (31)

SGMII1_RX0_P (31)

SGMII1_RX0_N (31)

PCIe x4L Connector

PCIE0_TX0_P (55)

PCIE0_TX0_N (55)

PCIE0_RX0_P (55)

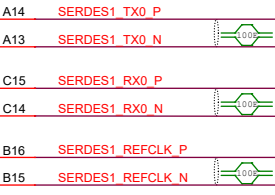
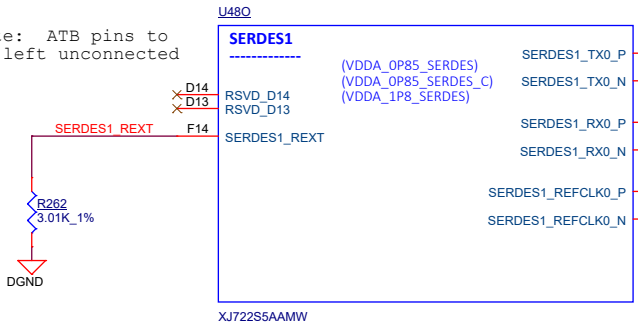
PCIE0_RX0_N (55)

SOC_SERDES1_REFCLK_P (55)

SOC_SERDES1_REFCLK_N (55)

SERDES1

Note: ATB pins to be left unconnected



R798
49.9E_1%

R799
49.9E_1%

DGND

Project :

J7 EVM



Title
SOC SERDES 0 & 1

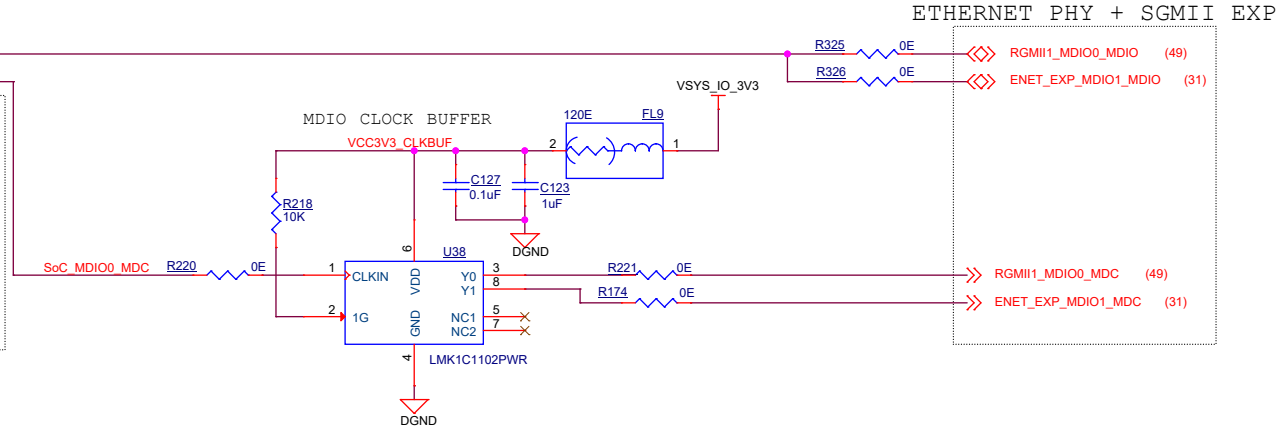
Size
C PROC170 002 EVM

Date: Thursday, March 07, 2024

Sheet 18 of 68

Rev
E3

U48L									
RGMII	MDIO0_MDIO	AD25	MCU MDIO0_MDIO						
	MDIO0_MDC	AC24	MCU MDIO0_MDC						
	RGMI1_RD0	AC25	MCU RGMI1_RD0						
	RGMI1_RD1	AD27	MCU RGMI1_RD1						
	RGMI1_RD2	AE24	MCU RGMI1_RD2						
	RGMI1_RD3	AE26	MCU RGMI1_RD3						
	RGMI1_RX_CTL	AD23	MCU RGMI1_RX_CTL						
	RGMI1_RXC	AE27	MCU RGMI1_RXC						
	RGMI1_TD0	AF27	MCU RGMI1_TD0						
	RGMI1_TD1	AE23	MCU RGMI1_TD1						
	RGMI1_TD2	AG25	MCU RGMI1_TD2						
	RGMI1_TD3	AF24	MCU RGMI1_TD3						
	RGMI1_TX_CTL	AF25	MCU RGMI1_TX_CTL						
	RGMI1_TXC	AG26	MCU RGMI1_TXC						



The schematic diagram illustrates the electrical connections for the USB Type-C and USB1 interfaces of the T3S0B221ARSER SoC. The diagram is divided into several functional blocks:

- USB HUB:** A dashed box representing the USB hub, with pins (45) USB1_HUB_DN4_D_P, (45) USB1_HUB_DN4_D_N, and (45,46) PWRCTL1/BATEN1.
- USB TYPE-C:** A dashed box representing the USB Type-C connector, with pins USB1_MUX_D_P (48), USB1_MUX_D_N (48), USB_TYPEC_DRVVBUS (48), and VBUS_5V0_TYPEC.
- USB1:** A dashed box representing the USB1 interface, with pins USB0_DP, USB0_DM, USB0_VBUS, USB0_DRVVBUS, USB_MUX_SEL, USB_MUX_OEn, and PWRCTL1/BATEN1.
- SoC Pins:** The T3S0B221ARSER SoC has pins U49 (1D+, 1D-, 2D+, 2D-, S, OE, GND) and U47 (1A, 1B2, 2A, 2B2, 3A, 3B2, 4A, 4B2, S, OE, GND).
- Connectors:** The USB0 connector has pins AA6 (USB0_DP) and AA7 (USB0_DM).

The connections are as follows:

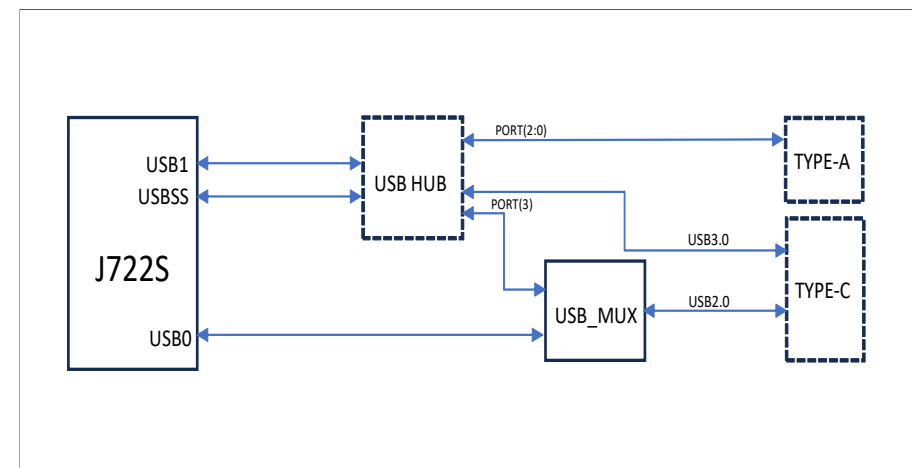
- USB Type-C to SoC (U49):**
 - USB1_MUX_D_P (48) to 1D+ (8)
 - USB1_MUX_D_N (48) to 1D- (7)
 - USB_TYPEC_DRVVBUS (48) to 2D+ (3)
 - VBUS_5V0_TYPEC to 2D- (4)
 - S (9) to S (5)
 - OE (6) to OE (6)
 - GND to GND (4)
- USB Type-C to USB1:**
 - USB1_MUX_D_P (48) to USB0_DP (AA6)
 - USB1_MUX_D_N (48) to USB0_DM (AA7)
 - USB_TYPEC_DRVVBUS (48) to USB0_DRVVBUS
 - VBUS_5V0_TYPEC to USB0_VBUS
- USB1 to SoC (U47):**
 - USB0_DP to 1A (1)
 - USB0_DM to 1B2 (2)
 - USB0_VBUS to 2A (7)
 - USB0_DRVVBUS to 2B2 (8)
 - USB_MUX_SEL to 3A (9)
 - USB_MUX_OEn to 3B2 (10)
 - PWRCTL1/BATEN1 to 4A (12)
 - S (1) to S (1)
 - OE (15) to OE (15)
 - GND to GND (4)
- Power and Grounding:**
 - VSYS_IO_3V3 to VCC (10) of U49 and VCC (16) of U47.
 - DGND to GND (4) of U49 and GND (4) of U47.
 - Capacitors C150 and C144 (0.1uF) are connected between VSYS_IO_3V3 and DGND.
 - Resistors R266 (10K) and R239 (10K 1% 0402) are connected between DGND and GND.

Note: Recommended V

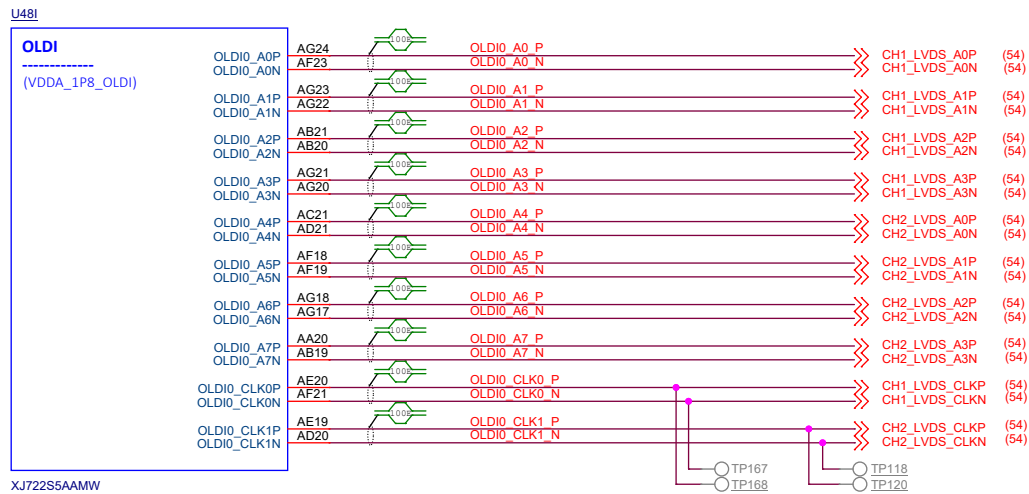
OEn	USB_MUX_SEL	U3184	U3185	
LOW	LOW	D=1D	A=B1	(default)
LOW	HIGH	D=2D	A=B2	
HIGH	X	Disconnect	Disconnect	

Note: Defaults to USB0 for Boot Support

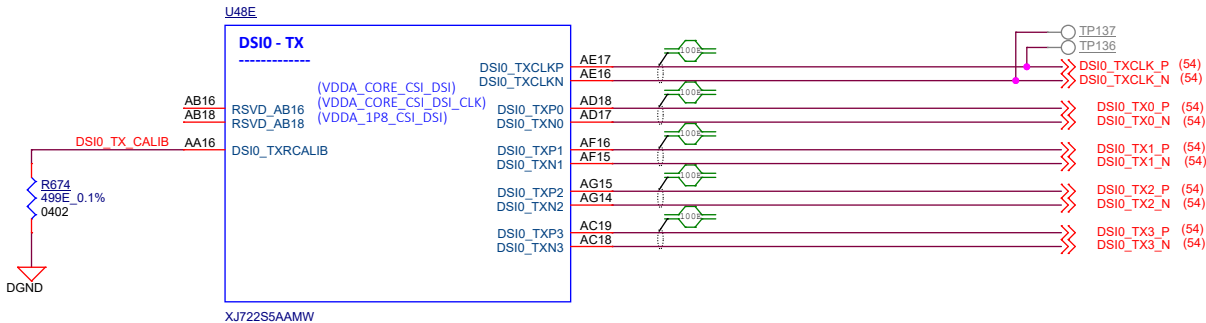
The schematic diagram illustrates the USB0 and USB1 connections for the XJ722S5AAMW module. The module's internal components, including the USB0 and USB1 controllers, are shown with their respective pins and internal connections. The USB0 controller is connected to the USB0_DP, USB0_DM, USB0_VBUS, and USB0_DRVVBUS pins. The USB1 controller is connected to the USB1_DP, USB1_DM, USB1_VBUS, and USB1_DRVVBUS pins. The PCIE0_CLKREQN pin is also shown. The diagram includes external components such as resistors R182, R275, R265, and R281, and a USB HUB. The USB HUB is connected to the USB0_DP, USB0_DM, USB1_DP, USB1_DM, USB_VBUS(45), and USB_HUB_DRVVBUS(45) pins. The diagram is labeled 'U48P' and 'XJ722S5AAMW'.



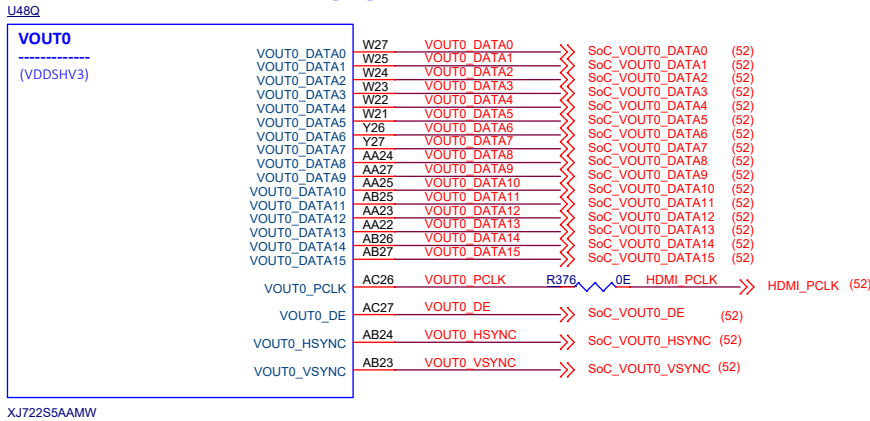
OLDI



DSI

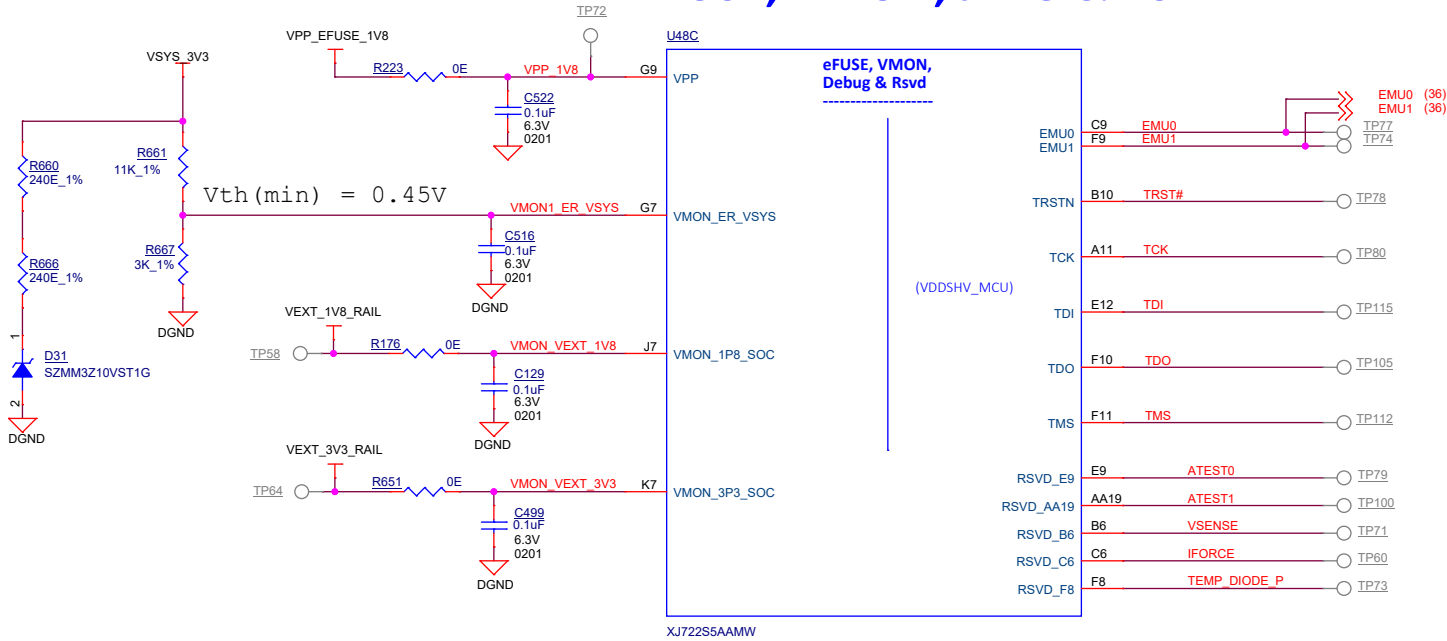


VOUT

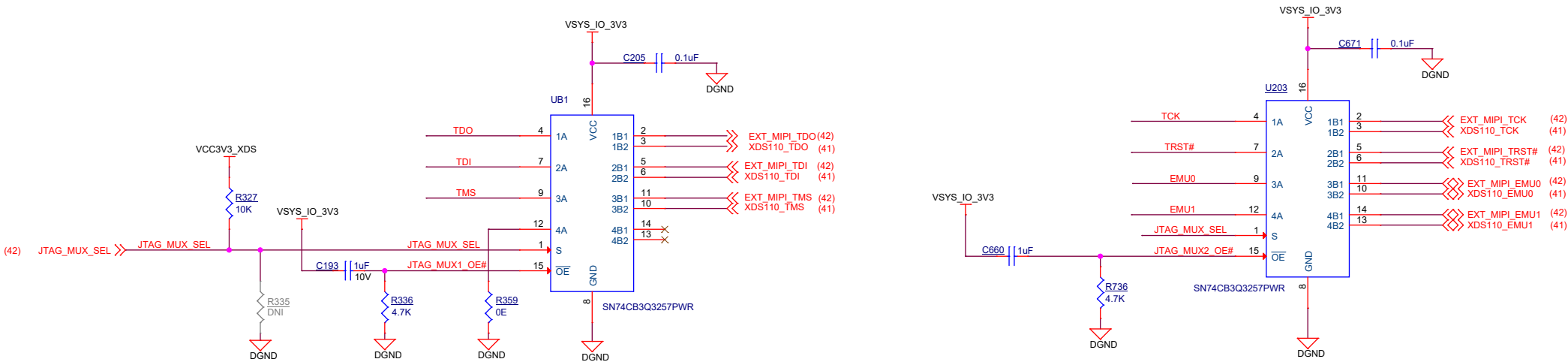


EFUSE, VMON, JTAG & RSVD

monitoring VSYS_3V3, to protect SoC from 1st stage power fault.



JTAG AND TRACE MUX



JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU] (default)
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]

ANALOG POWER 1

PDN shows default option to supply SoC's VDA_3P3_USB from the digital VDD_IO_3V3 rail with in-line supply filter to reduce switching noise to give reasonable USB 2.0 data eye performance for product development tasks.
An option has been provisioned to supply VDA_3P3_USB from a low noise LDO derived from a VDSYS_5V input to give optimal USB 2.0 data eye performance if needed.
If USB 2.0 I/F is not used, then the digital VDD_IO_3V3 rail can be supply VDA_3P3_USB directly

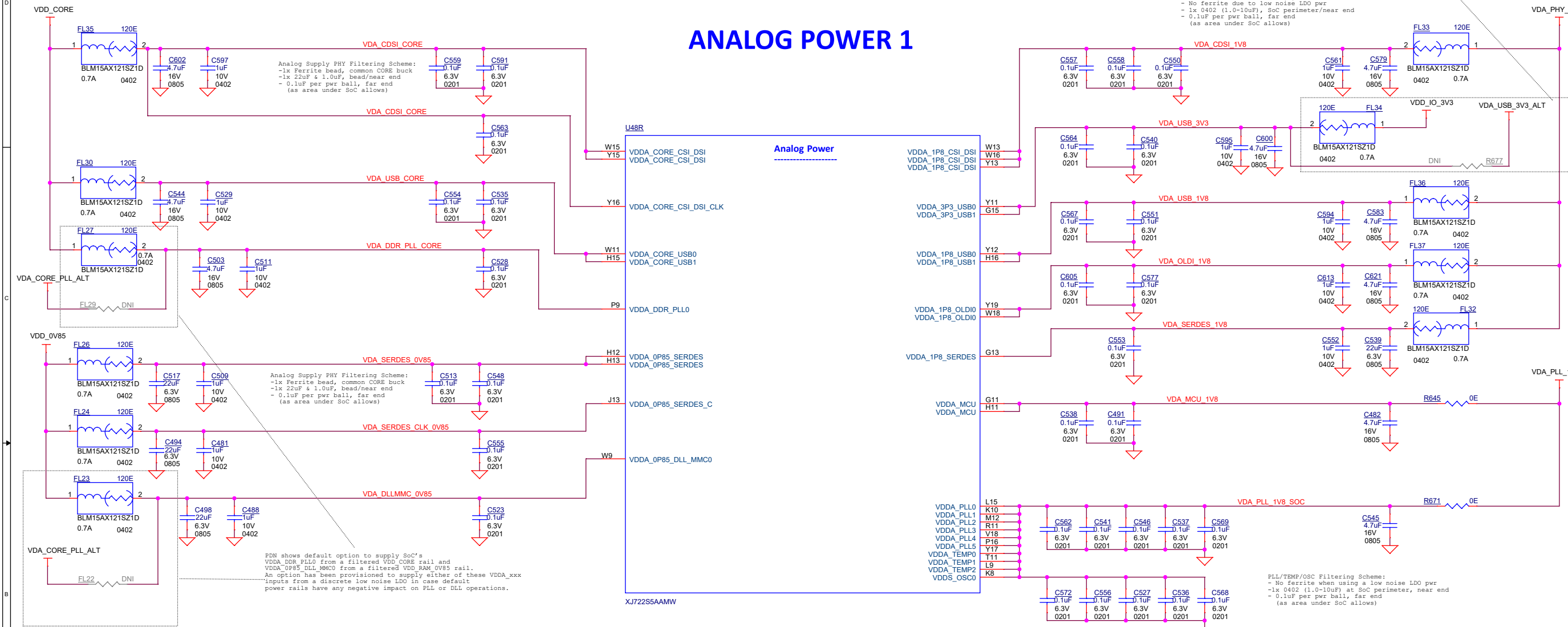
PLL/TEMP/OSC/USB2.0 Filtering Scheme:
- No ferrite due to low noise LDO pwr
- 1x 0402 (1.0-10uF), SoC perimeter/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

PLL/TEMP/OSC Filtering Scheme:
- No ferrite when using a low noise LDO pwr
- 1x 0402 (1.0-10uF) at SoC perimeter, near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

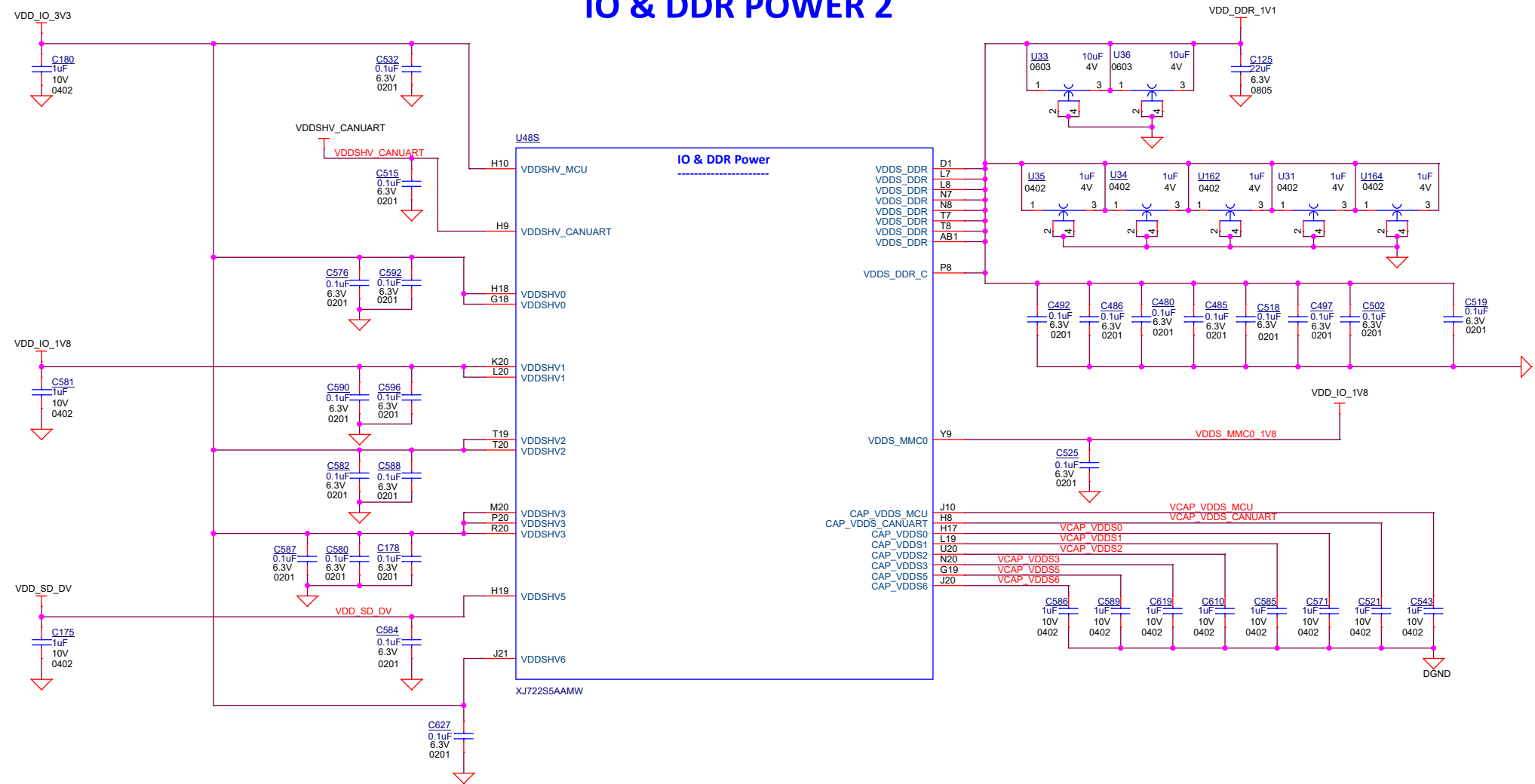
Analog Supply PHY Filtering Scheme:
- 1x Ferrite bead, common CORE buck
- 1x 22uF & 1.0uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

Analog Supply PHY Filtering Scheme:
- 1x Ferrite bead, common CORE buck
- 1x 22uF & 1.0uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

PDN shows default option to supply SoC's VDDA_DDR_PLL0 from a filtered VDD_CORE rail and VDDA_0P85_DLL_MMC0 from a filtered VDD_RAX_0V85 rail. An option has been provisioned to supply either of these VDDA_XXX inputs from a discrete low noise LDO in case default power rails have any negative impact on PLL or DLL operations.



IO & DDR POWER 2

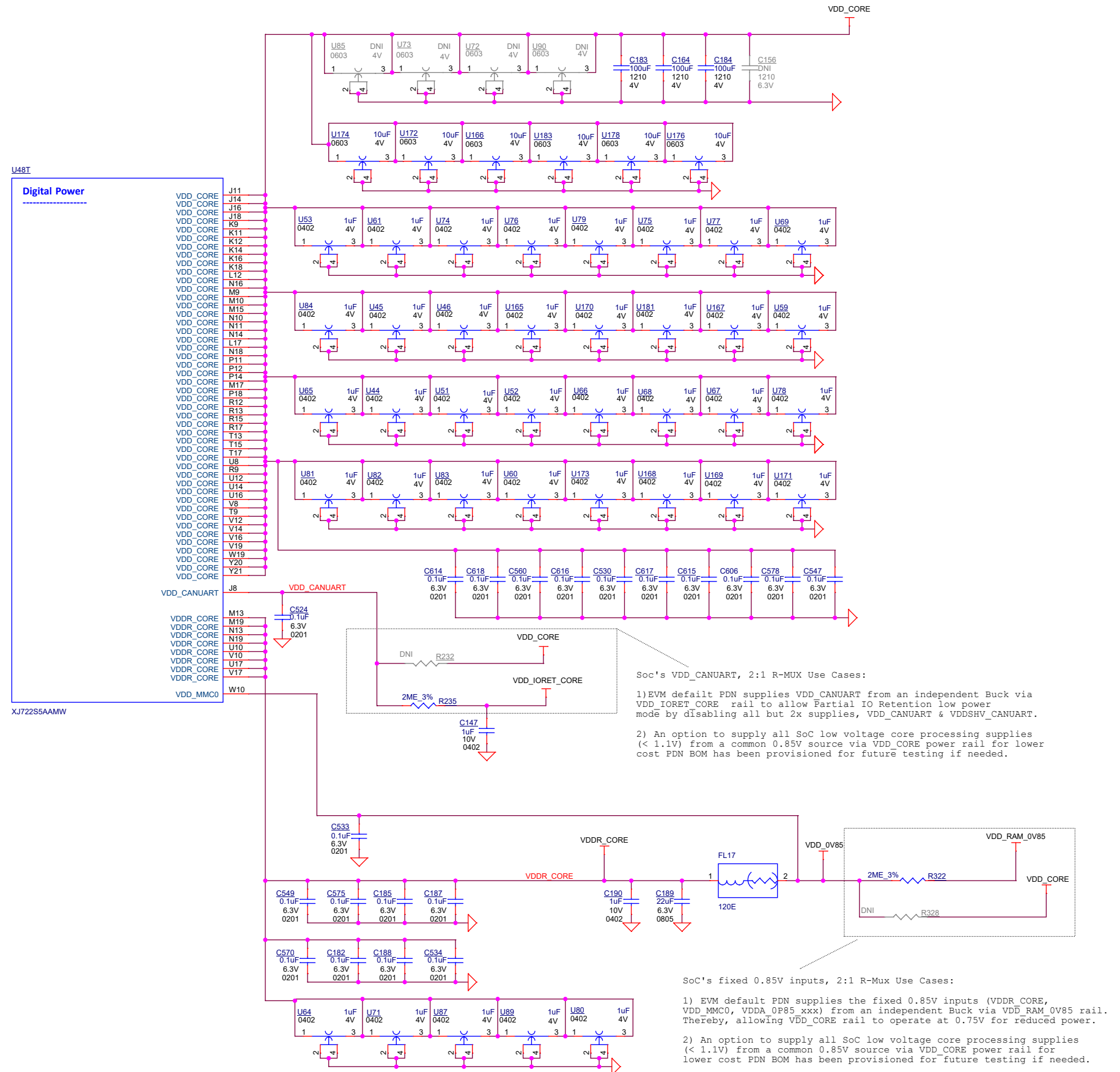


Note:

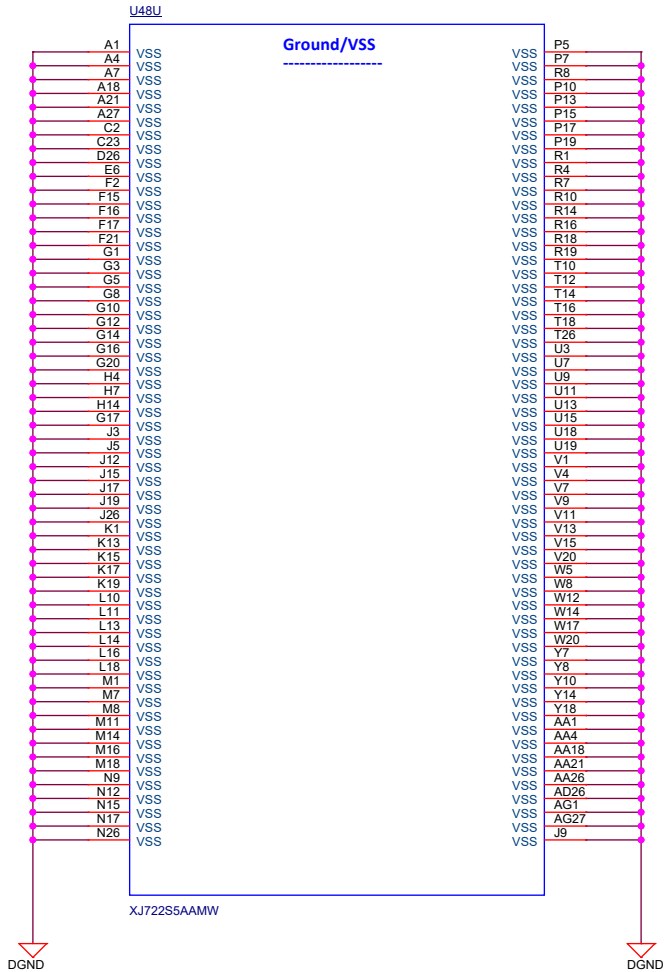
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

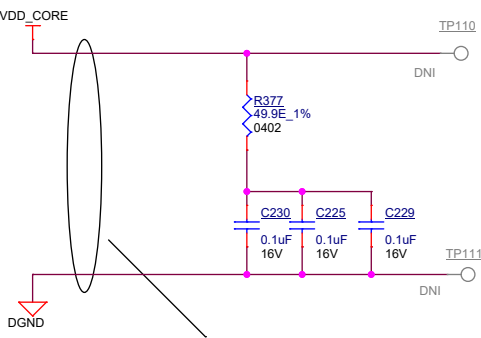
DIGITAL POWER 3



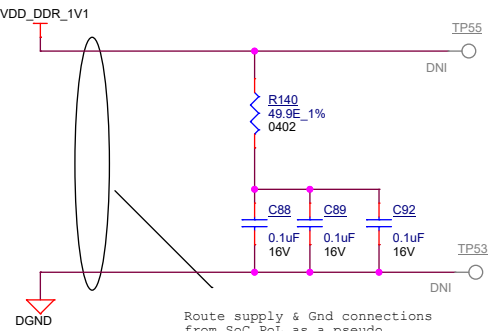
SOC GROUND



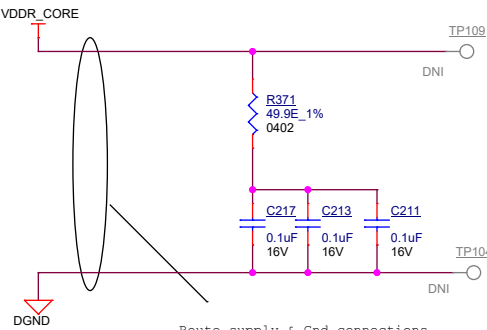
SoC Supply Noise Kelvin Sensing



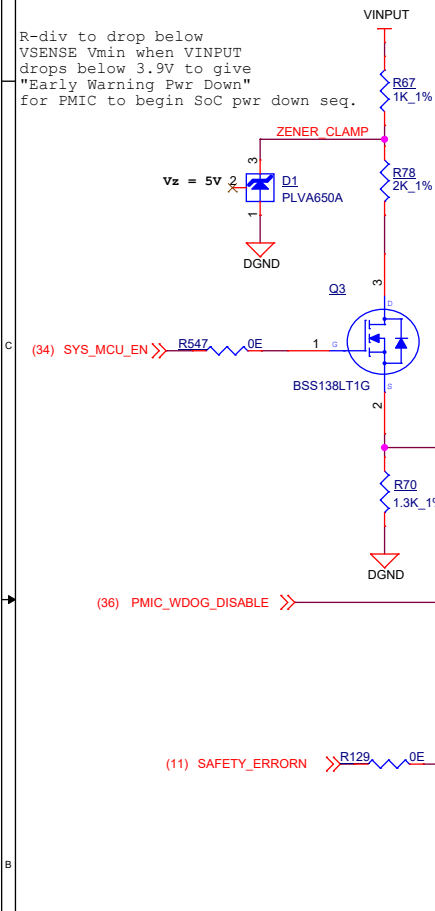
Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access



Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access



Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access

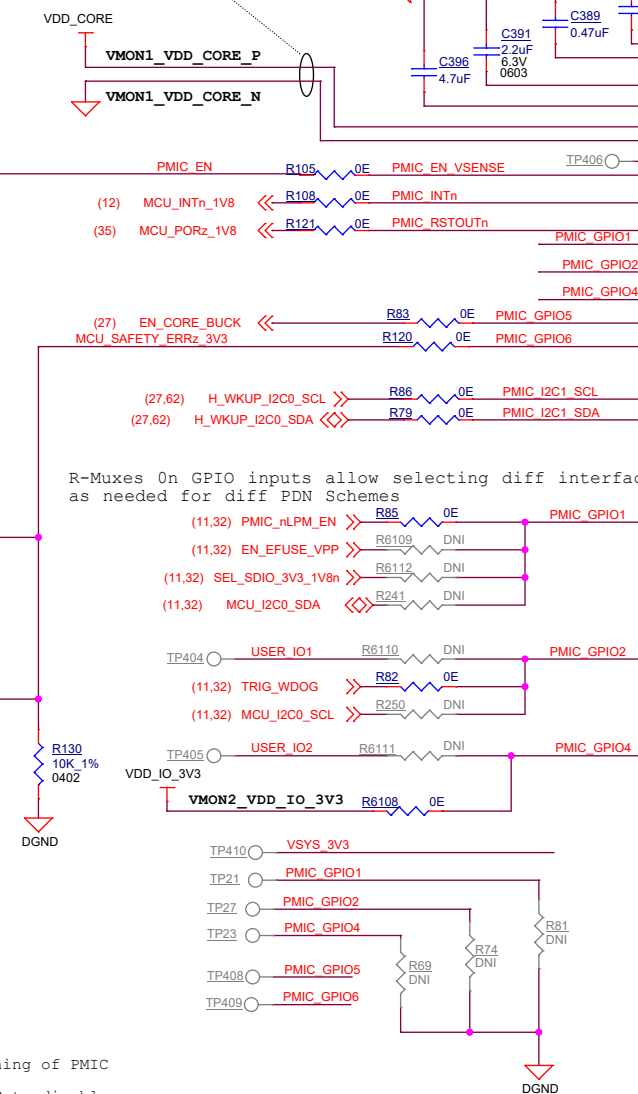


PMIC's GPIO6 supports 2x PDN functions:

- A) DISABLE_WDOG: PMIC reads logic level at GPIO6 pin at beginning of PMIC start-up sequence before NVN initialization.
 - a) High level at GPIO6 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_FWRHOLD bit to disable timer's long-window time-out).
 - b) Low level at GPIO6 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
- B) MCU SAFETY ERROR: After PMIC NVN initialization, GPIO6 function is set to Error Signal Monitor (ESM) function.

SWITCH (SW2 - 5)	Description
CLOSED	Disables WDog, high latched at Pwr-Up
OPEN (Default)	Enables WDog, low latched at Pwr-Up

```
Route VMON1 as pseudo
diff pair (VMON1_xxx_P/_N)
```



PMIC GPIO_1 & GPIO_2, 2:1 R-Mux Use Cases:

- 1) Install R85 to support SoC's Partial IO Ret low power mode that needs PMIC_nLPM_EN connected to GPIO1.

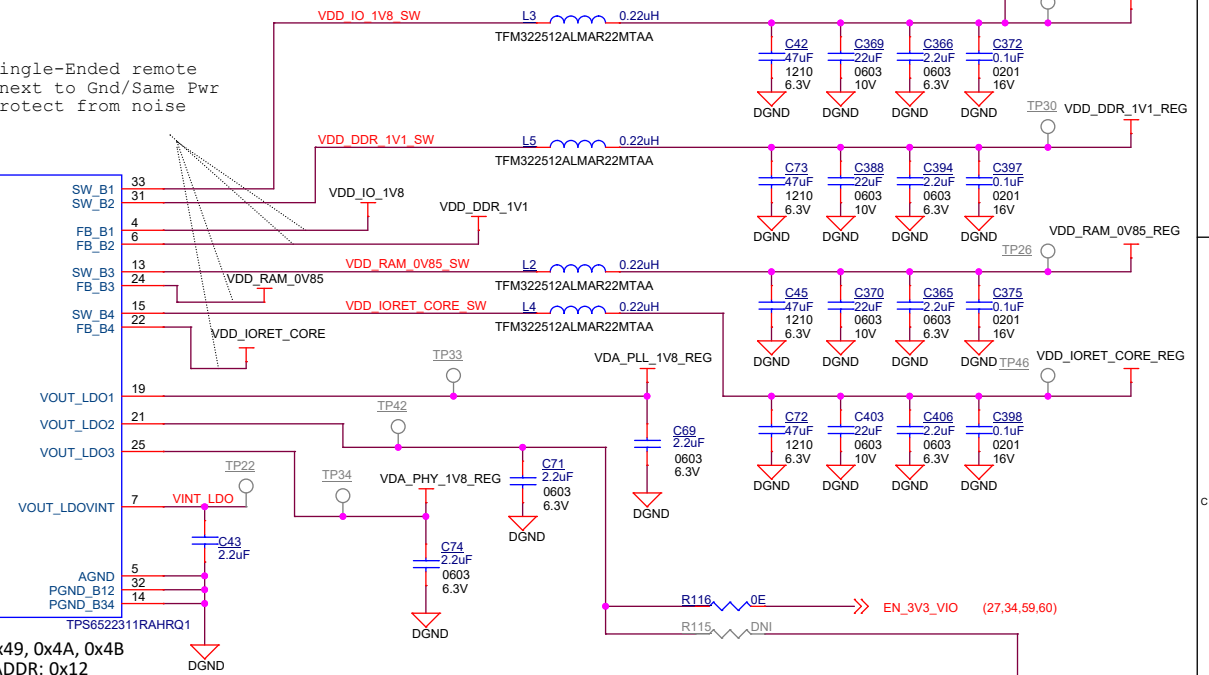
Install R82 to support alternative Trigger WDog timer mode of operation.

- 2) Install both R241 & 250 to use 2x independent I2C channels for PMIC settings & status and WDog timer in long window mode.

TI EVM default board & BOM supports Use Case #1

Note:
Previous J7xxx PDNs used a 2nd, indep I2C Ch
(MCU_I2C0_SCL/SDA) for WDOG operations.
Burton PMIC has limited GPIOs, so 1x I2C Ch
will be timed multiplexed (PMIC control/settings &
WDOG ops) in order to support low pwr modes.

Route all Single-Ended remote sense fdbk next to Gnd/Same Pwr guards to protect from noise coupling.



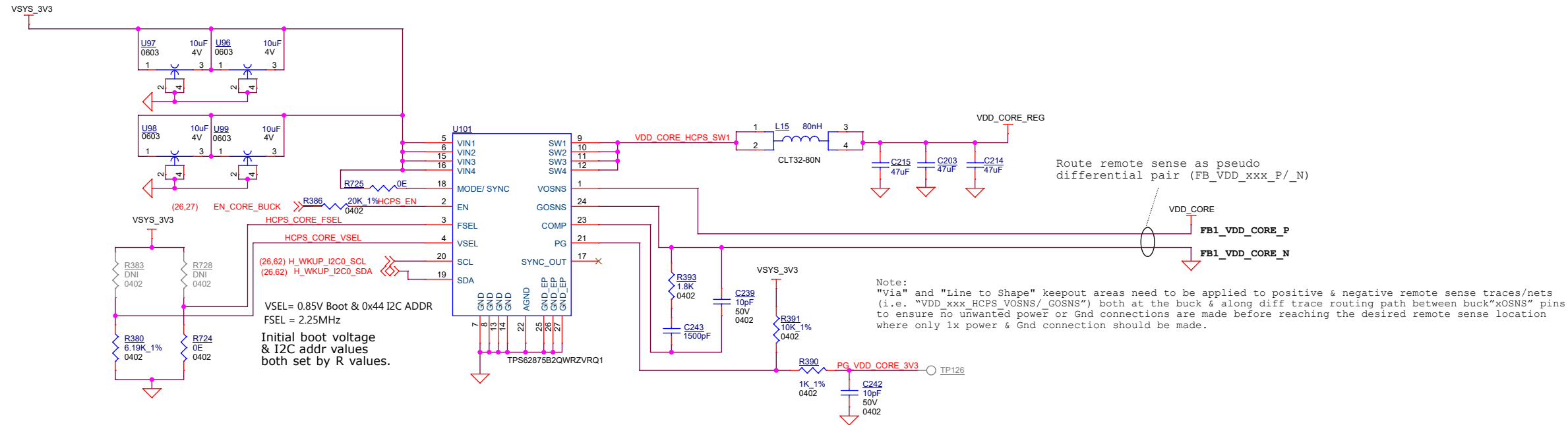
PMIC LDO2, 2:1 R-Mux Use Cases:

- 1) Install R116 to use LDO2 Vout as "EN_3V3_VIO" control signal on a discrete load switch to supply VDD_IO_3V3 loads > 165mA, SoC & all board peripheral components.
- 2) Install R115 to use LDO2 in FET Bypass/Load Switch mode to supply VDD_IO_3V3 loads < 165mA, SoC & all board peripheral components.

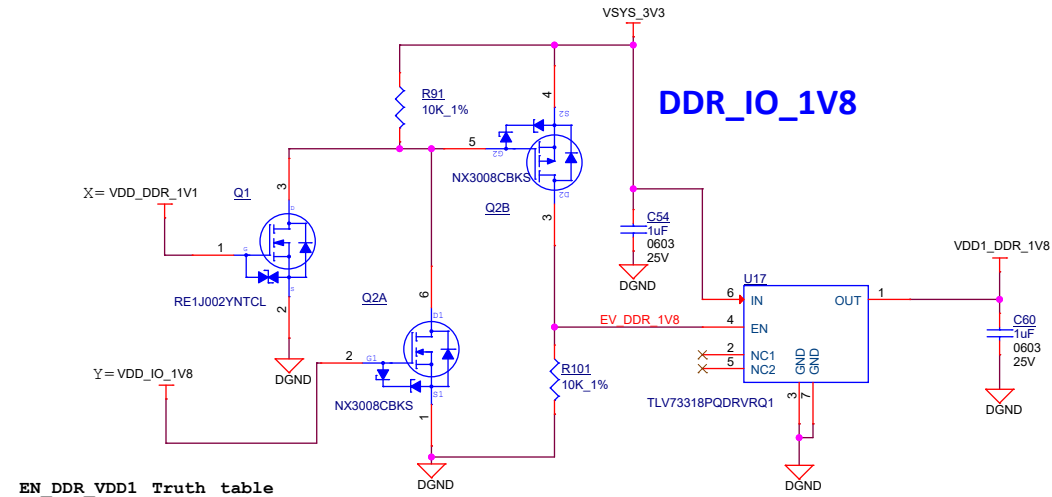
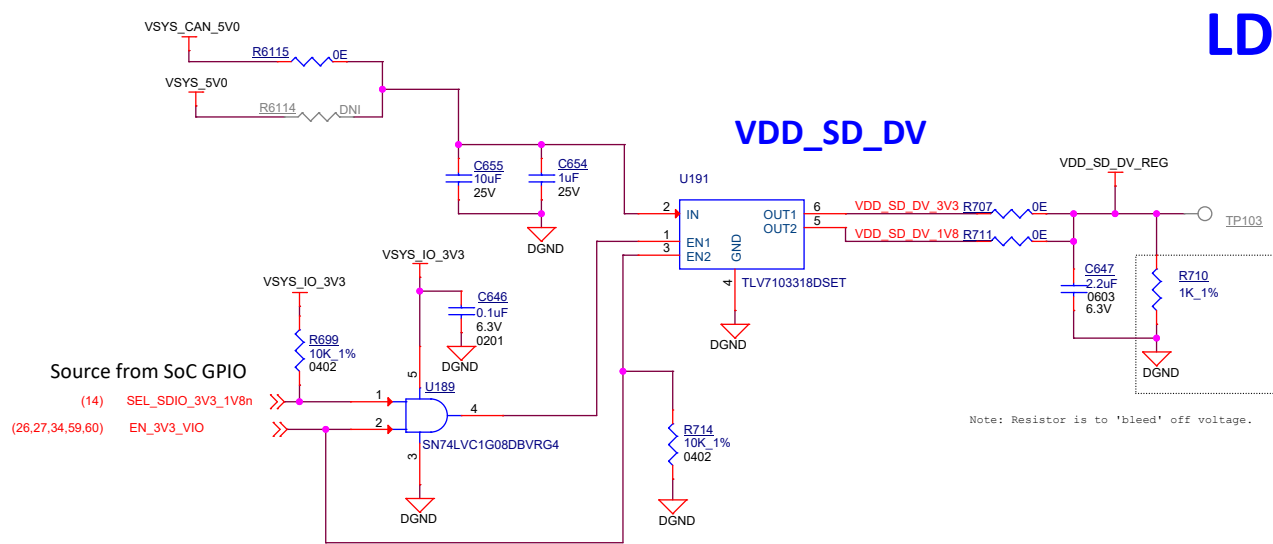
TI EVM default board & BOM is use case i#1.

[illegible]

VDD_CORE High-Current Power Stage (HCPS)

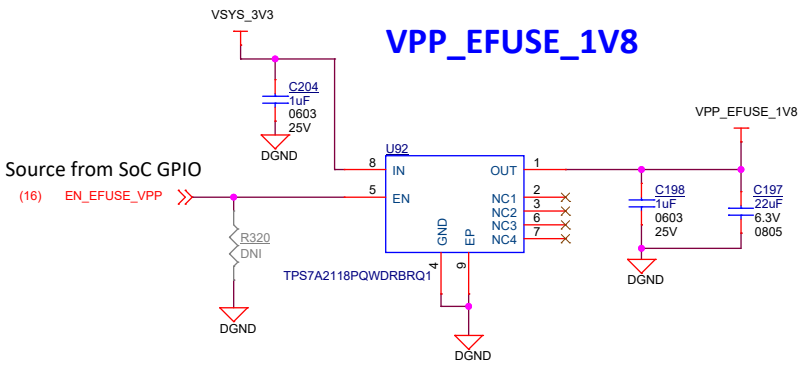
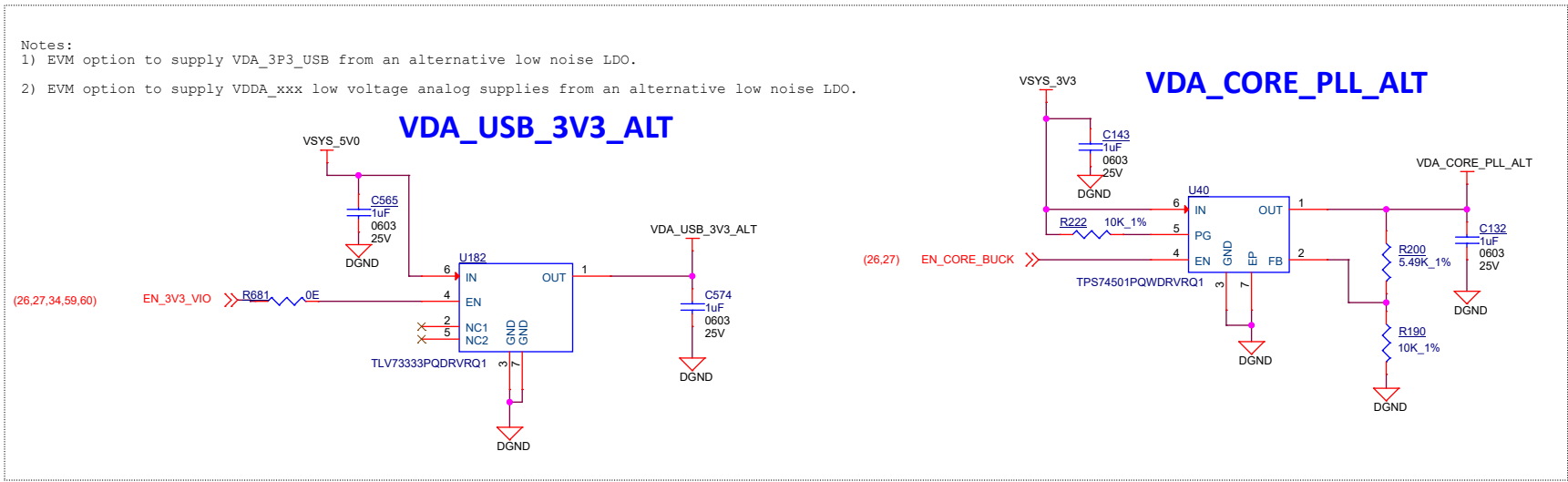


LDOs



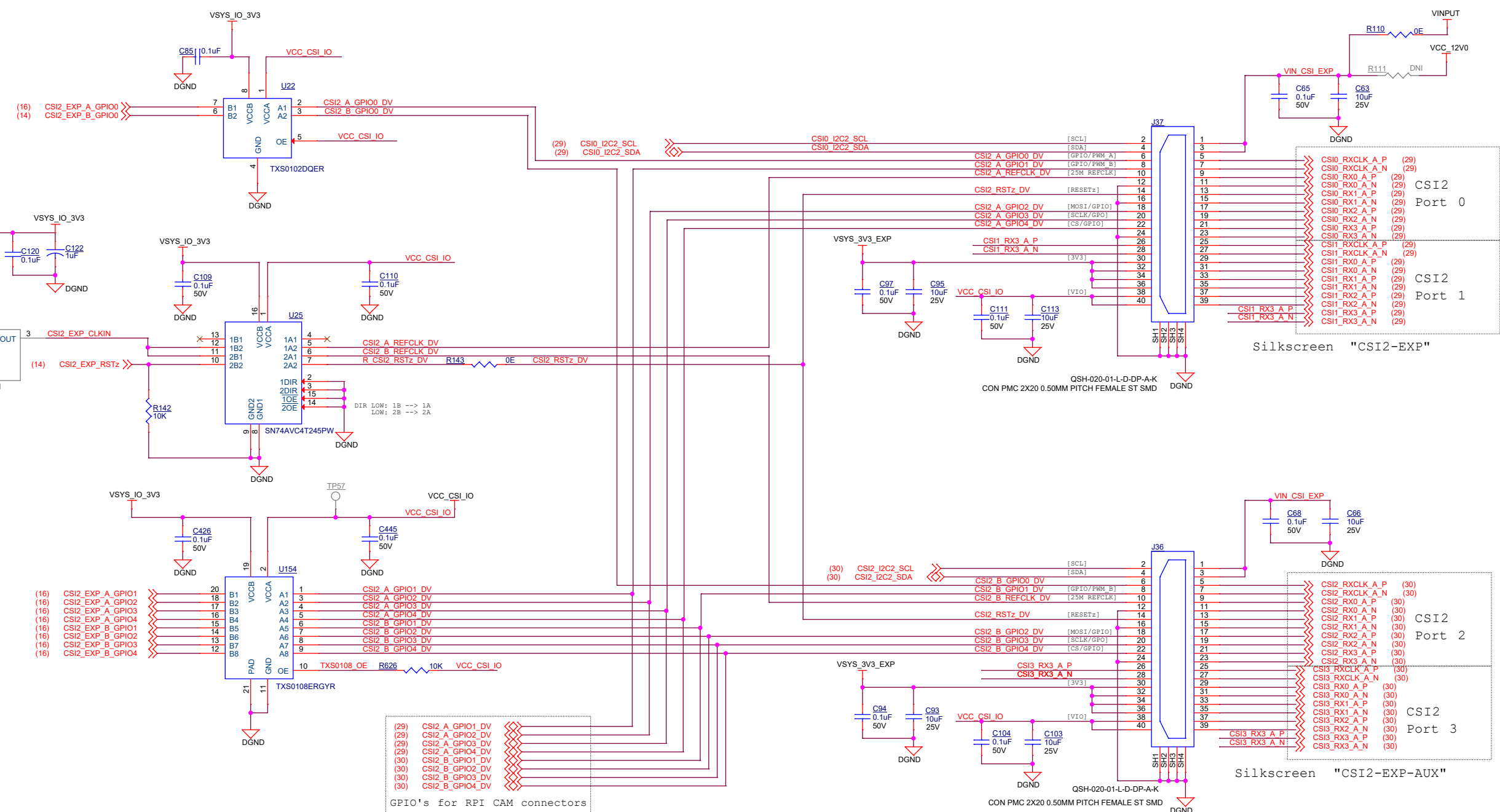
EN_DDR_VDD1 Truth table

Descrt	"OR" Gate Logic	EN_DDR_V8
X	Y	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1

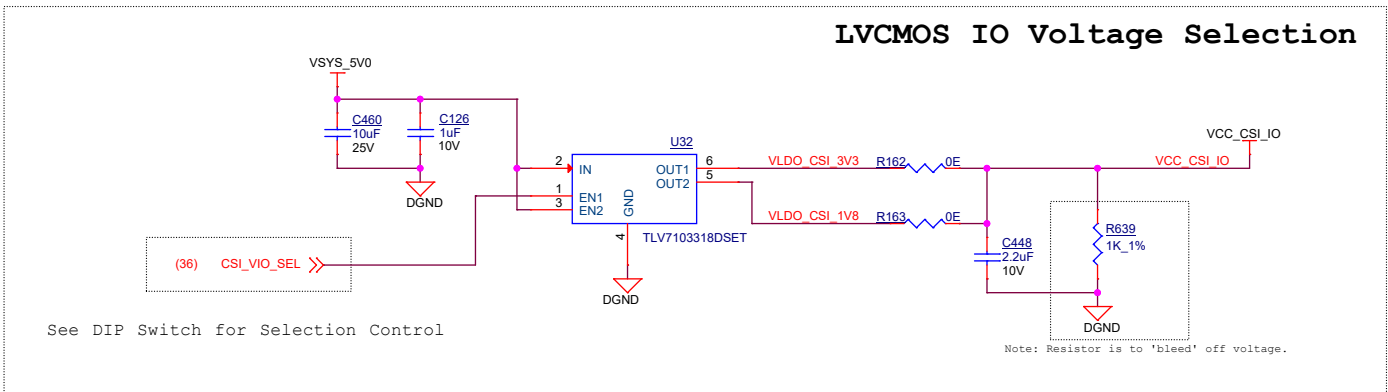


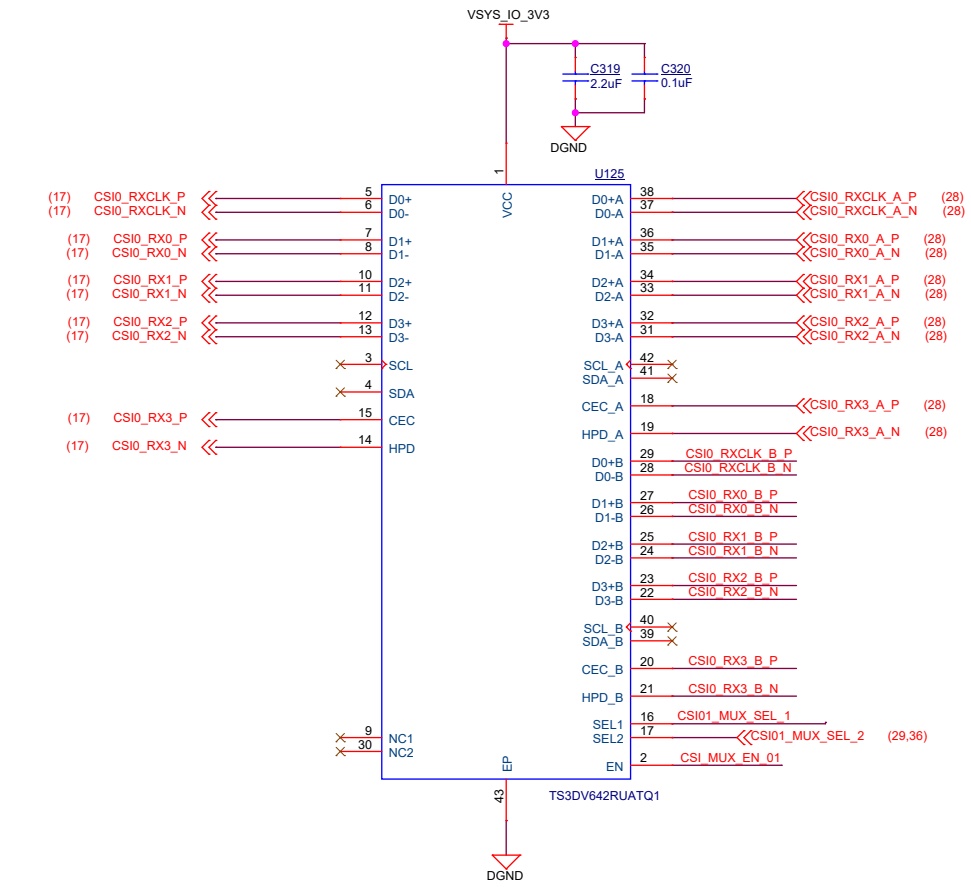
Level Translation for LVCMOS

CSI2 EXPANSION CONNECTORS



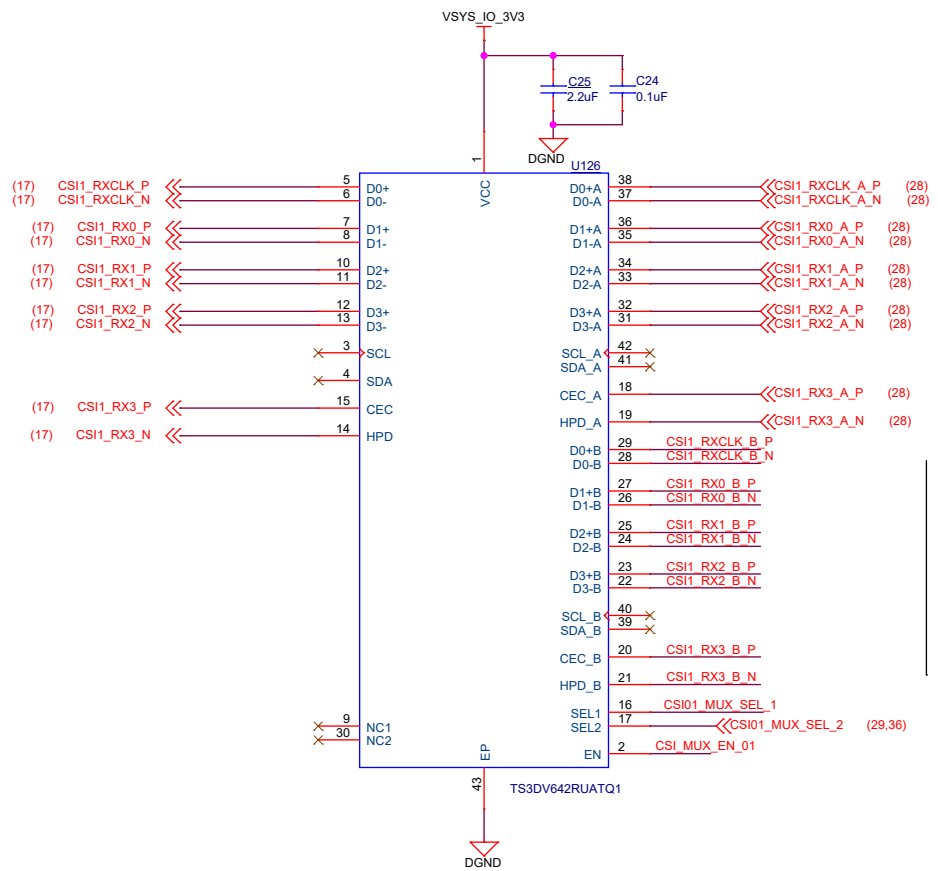
CSI2_EXP_A GPIO2, 4 are connected to SOC GPIO
and others are from IO expander





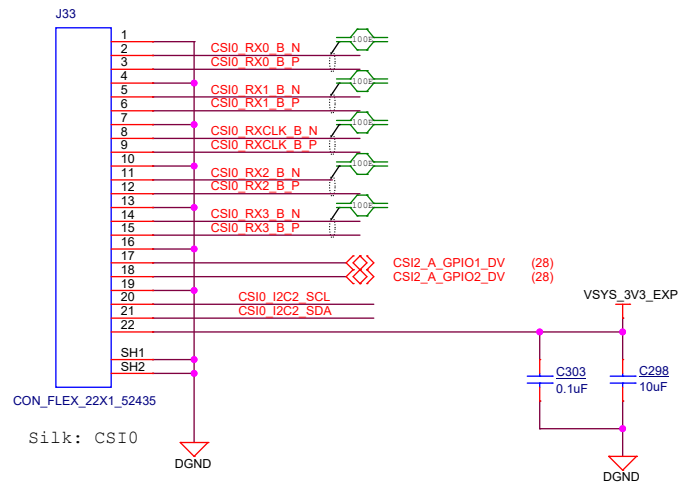
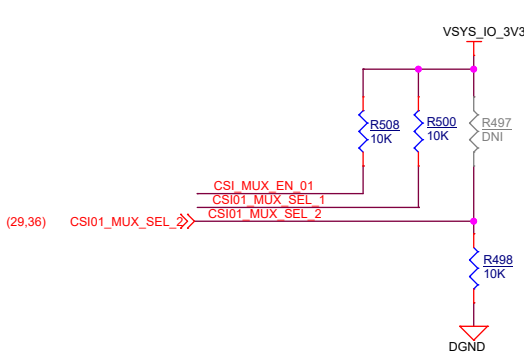
From CSI EXP Conn

From FPC Camera Conn

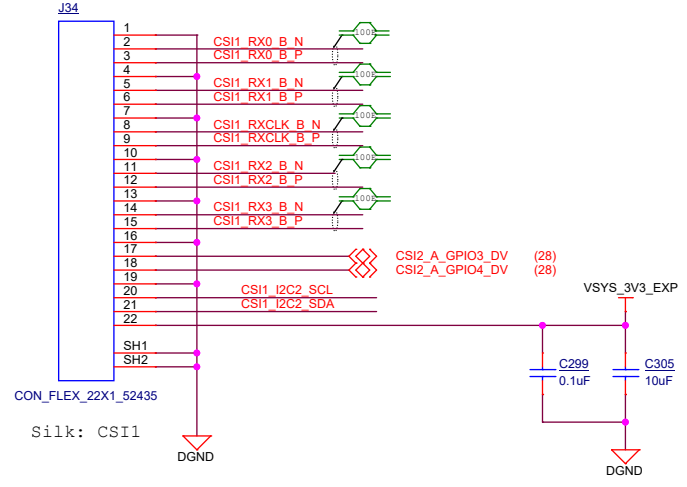


From CSI EXP Conn

From FPC Camera Conn

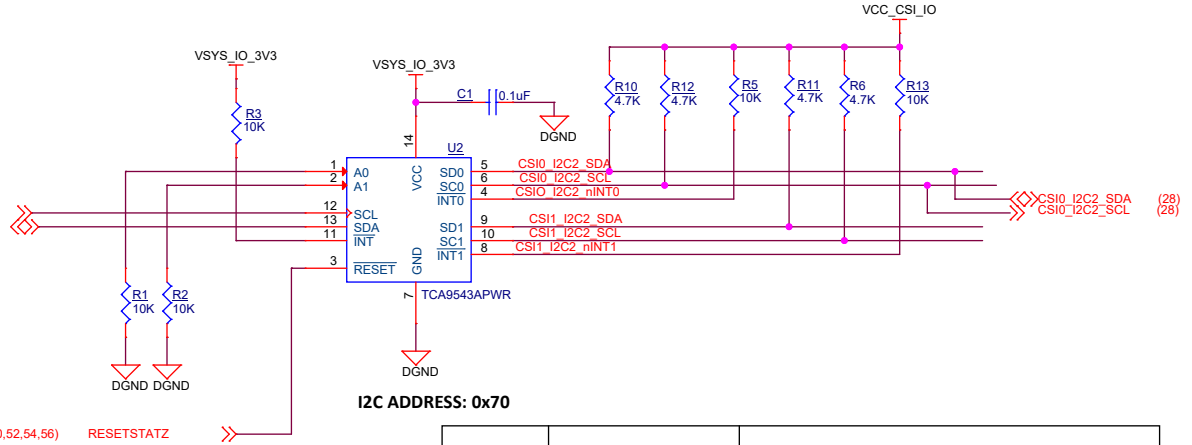


Silk: CSI0



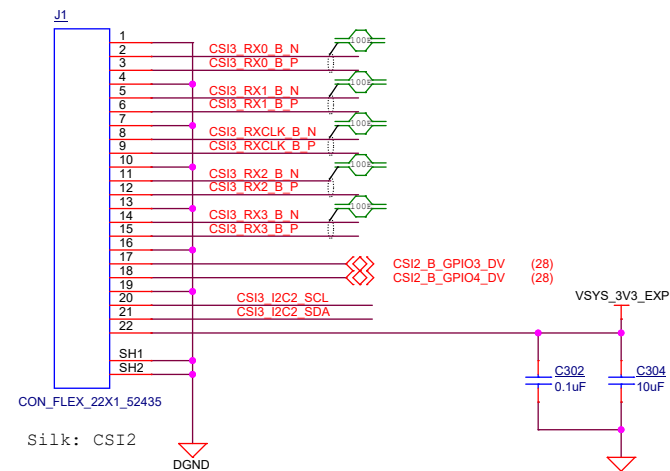
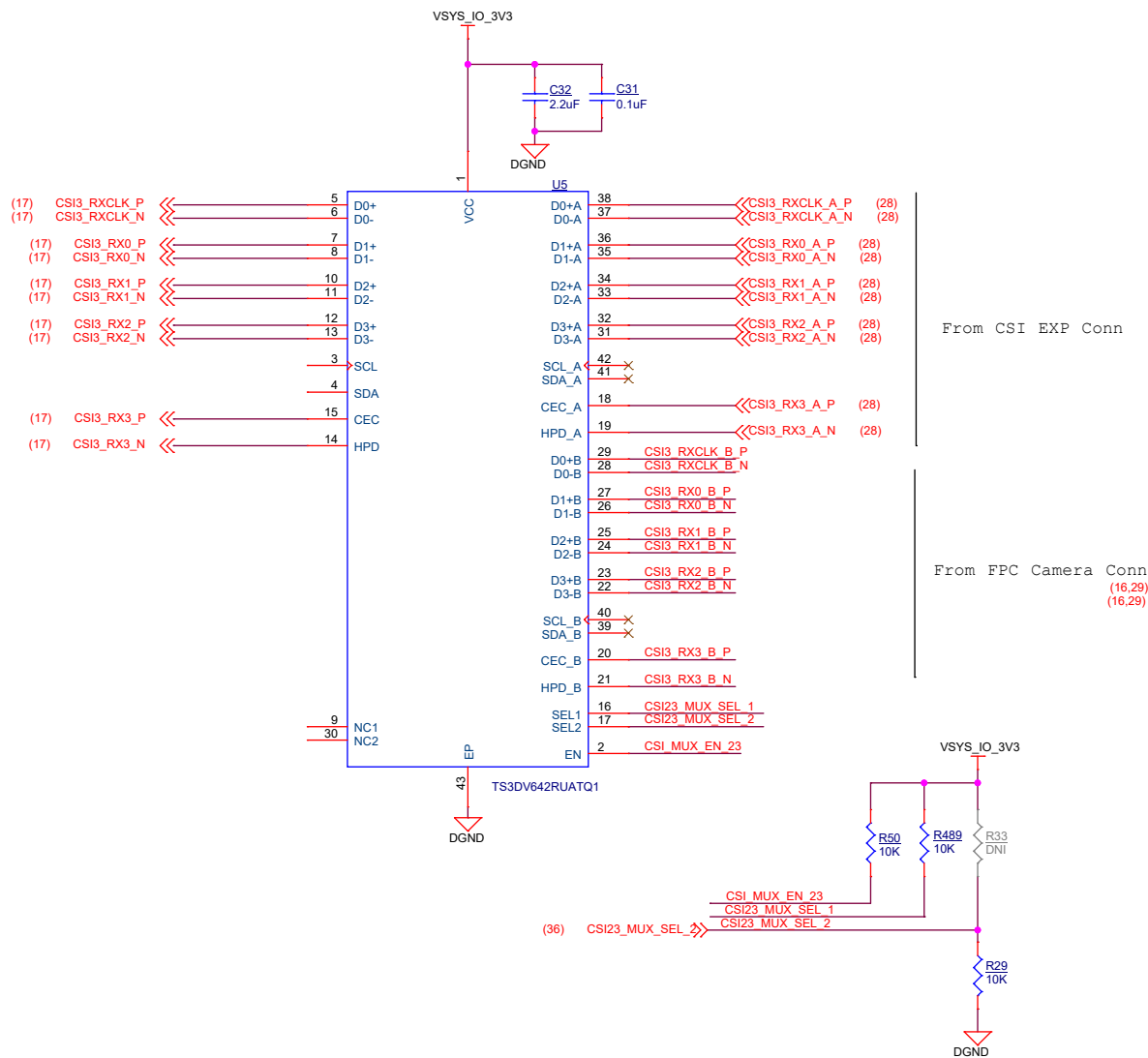
Silk: CSI1

I2C SWITCH FOR SoC_I2C2



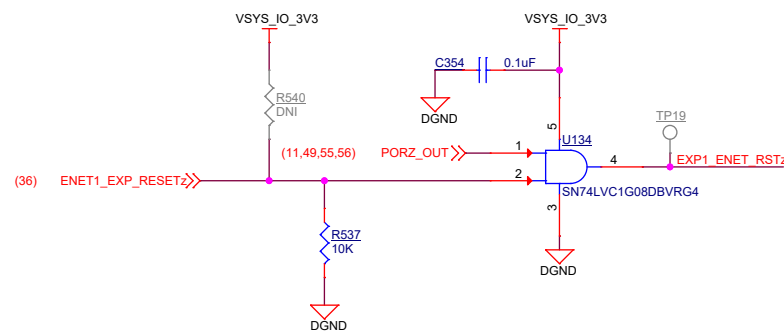
I2C ADDRESS: 0x70

EN	CSI01_MUX_SEL_2	FUNCTION
HIGH	LOW	INPUT<-- A Port [CSI2 Connector] (default)
HIGH	HIGH	INPUT<--B port [FPC Camera Connector]
LOW	X	Disconnect

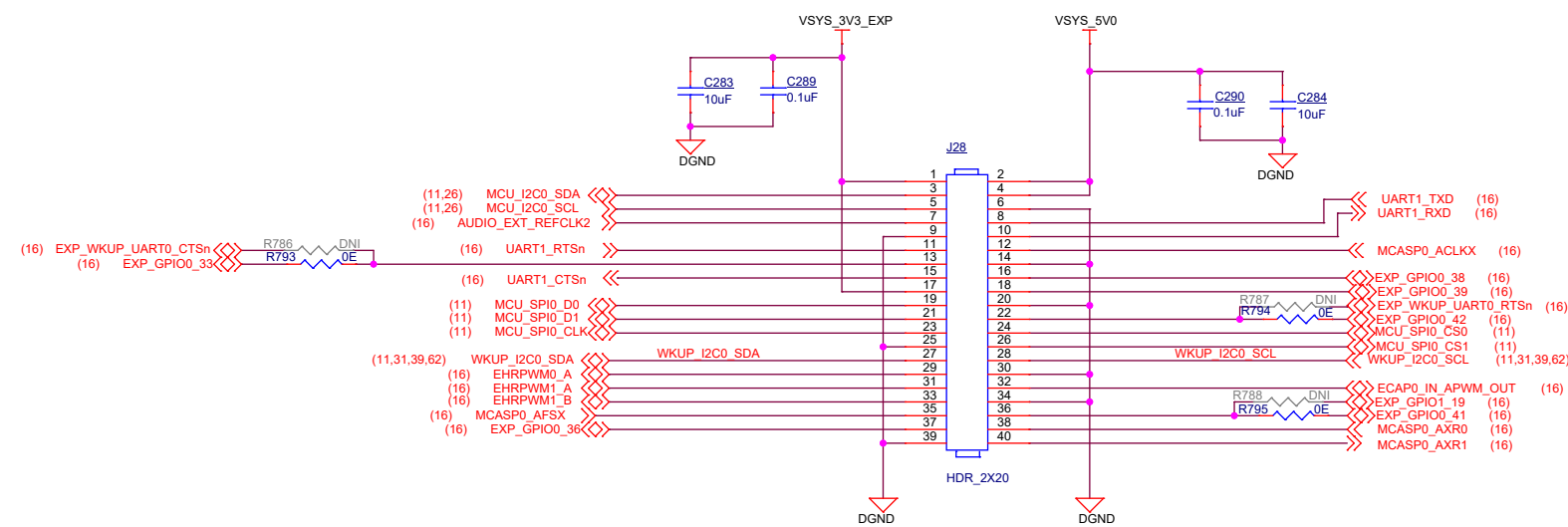
[illegible]

EN	CSI23_MUX_SEL_2	FUNCTION	
HIGH	LOW	INPUT<-- A Port [CSI2 Connector]	(default)
HIGH	HIGH	INPUT<--B port [FPC Camera Connector]	
LOW	X	Disconnect	

```
Silkscreen  "ENET-EXP-1"
```

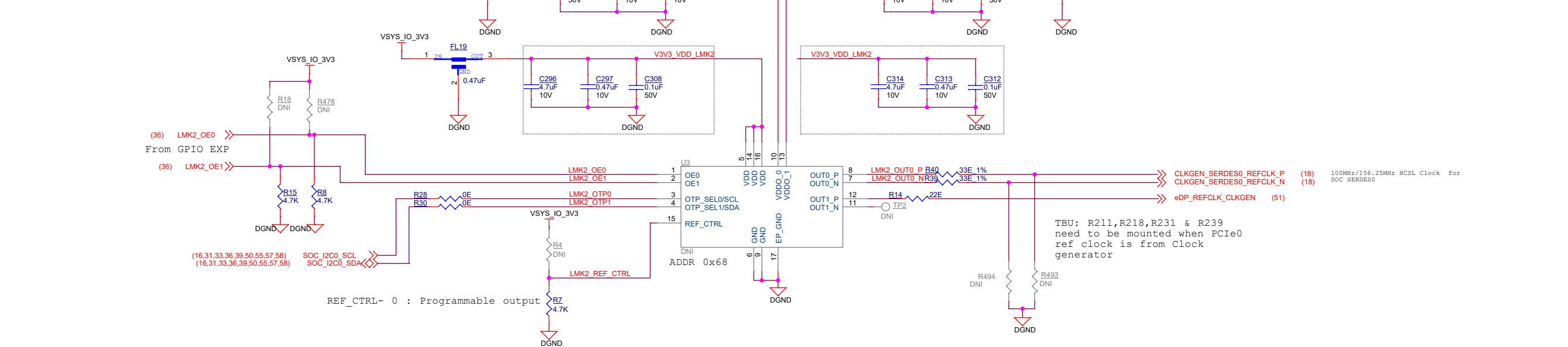


USER EXPANSION CONNECTOR

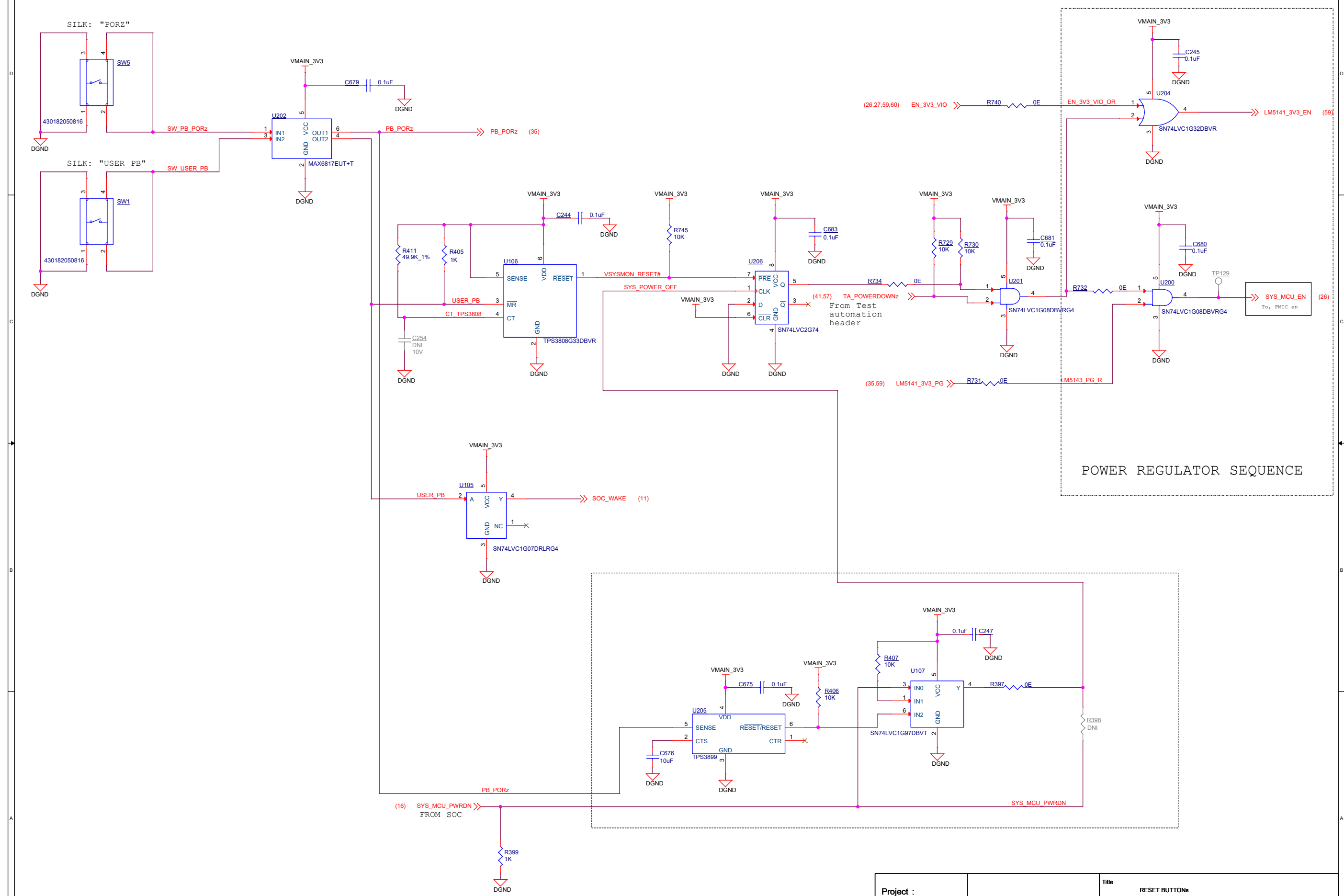


Silk Screen "40p EXP HDR"

SERDES CLOCK GENERATOR #2

[illegible]

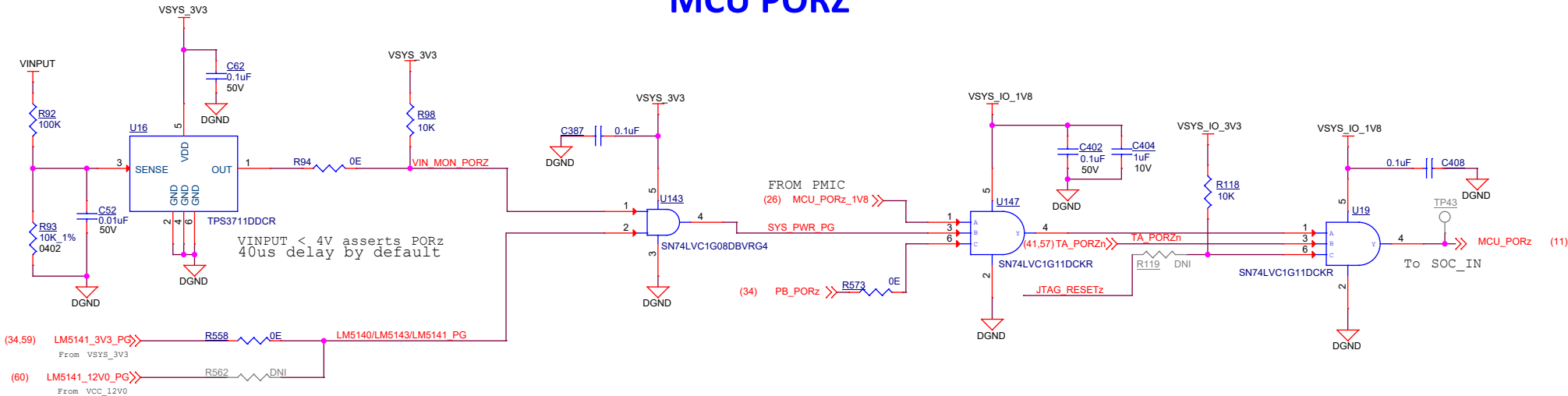
RESET BUTTONs



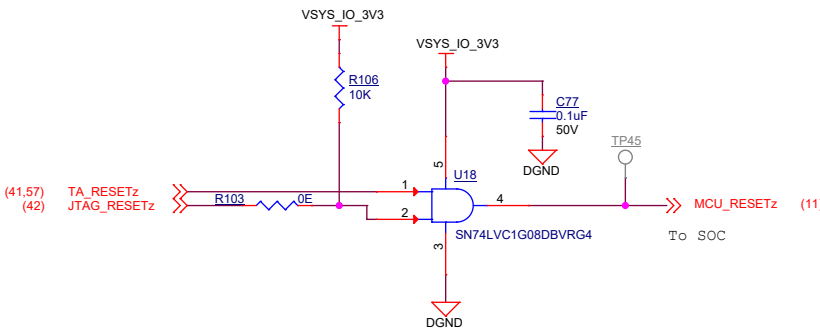
RESET INPUTS

Under Voltage Monitor (VINPUT)

MCU PORZ

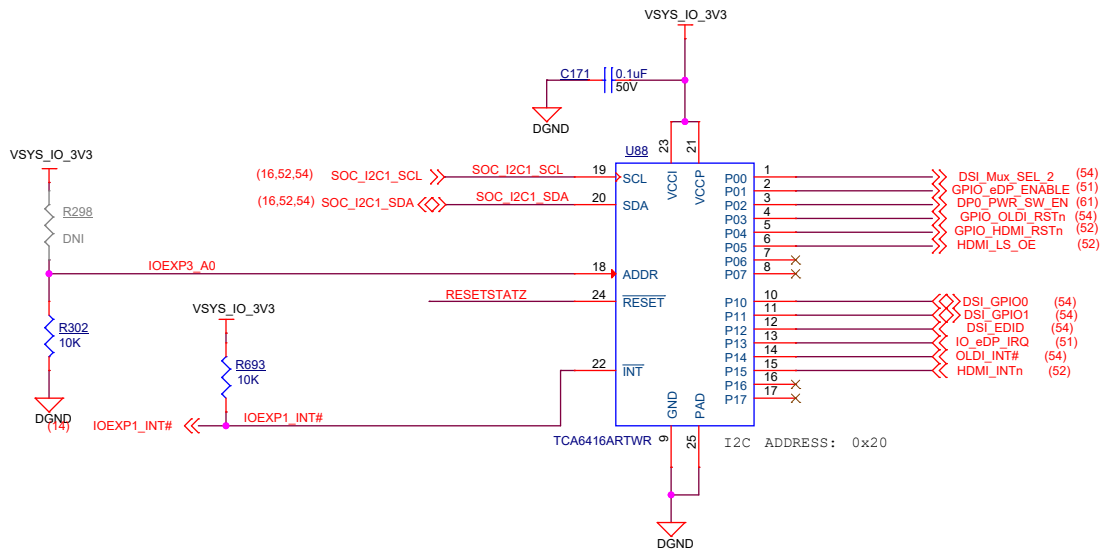
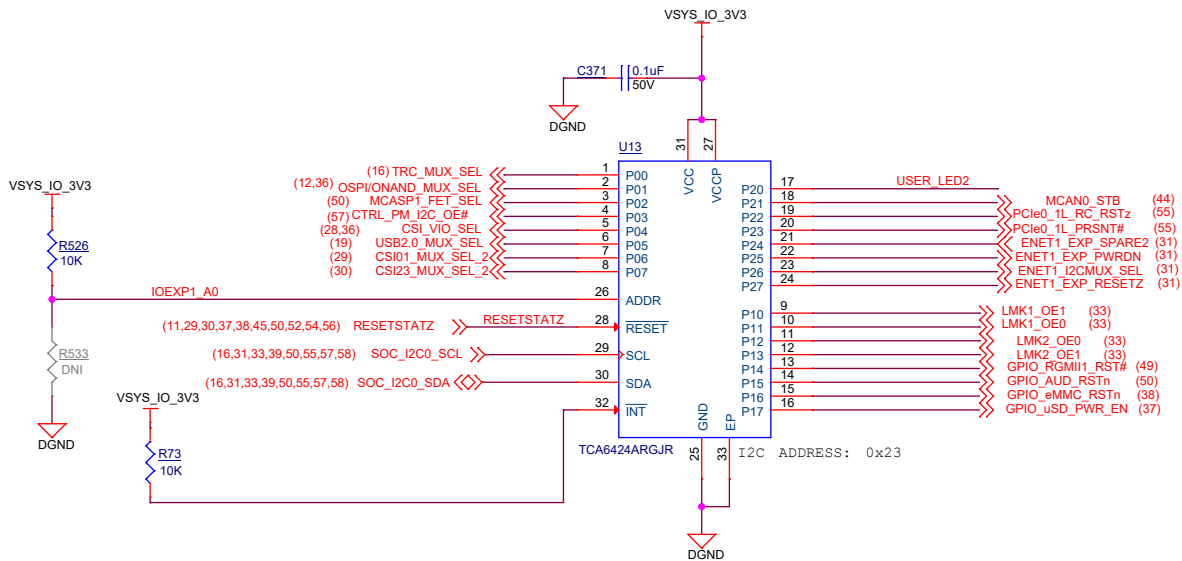


MCU_RESET



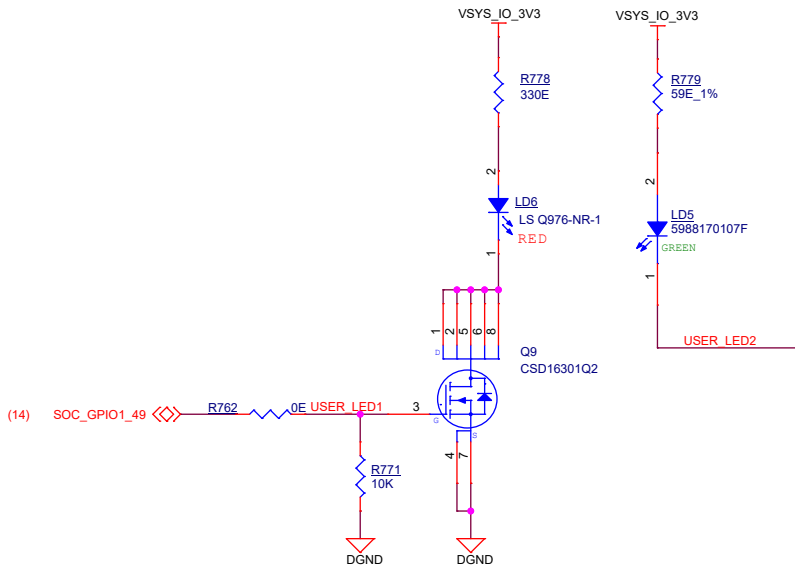
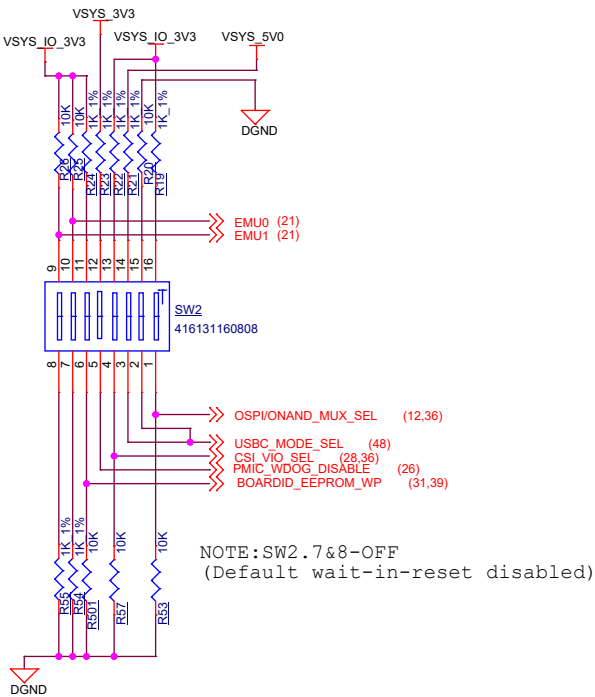
GPIO EXPANDERS

I2C GPIO EXPANDER1

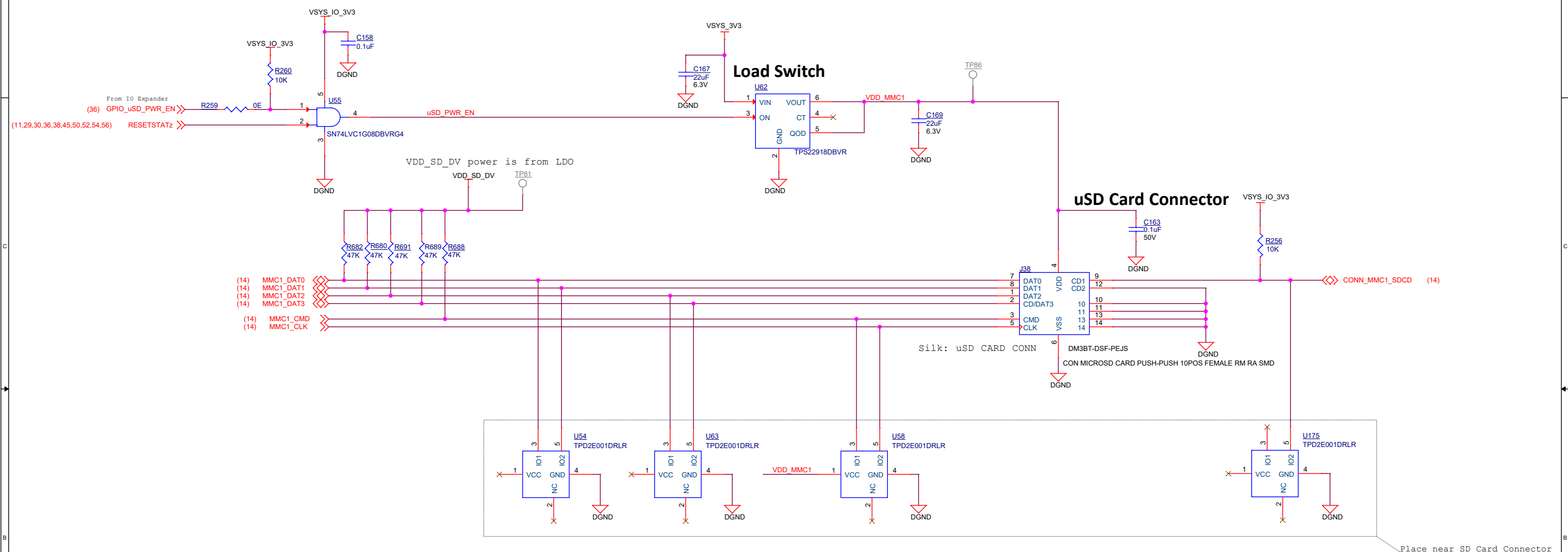


SWITCH (SW2.4)	Description
CLOSED	Disables WDog, high latched at Pwr-Up
OPEN (Default)	Enables WDog, low latched at Pwr-Up

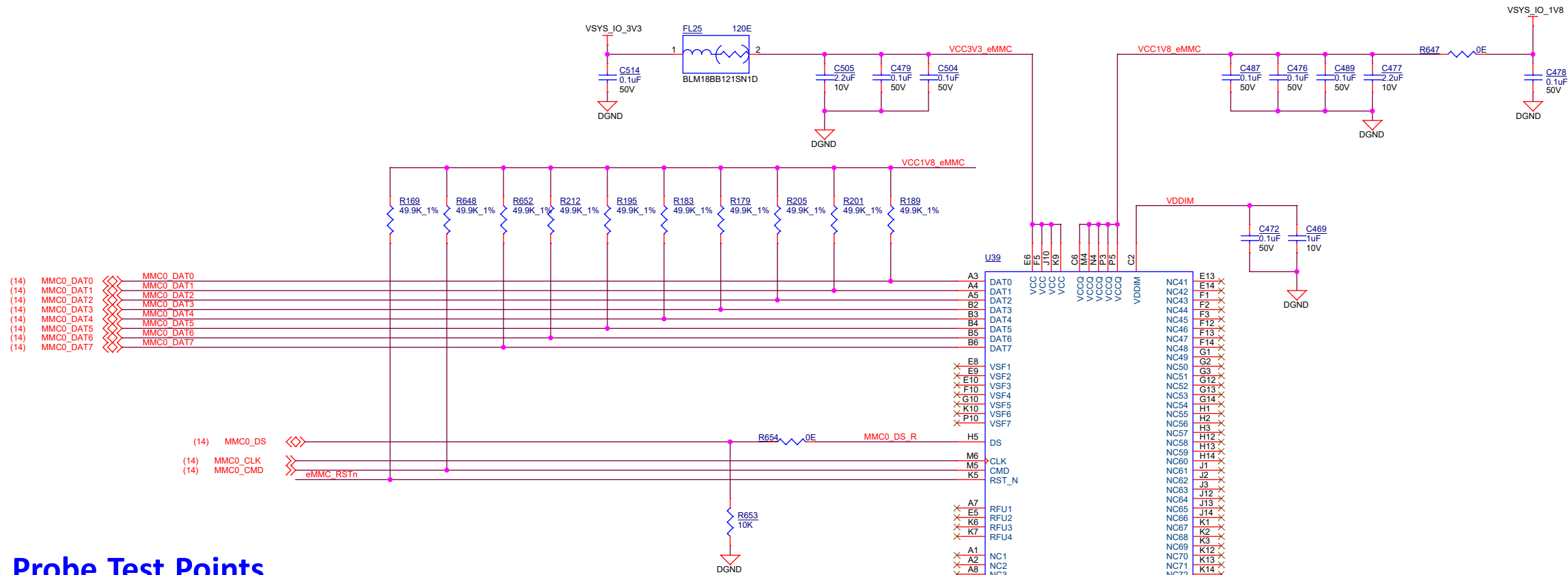
CONFIG DIP SWITCH



Micro SD CARD INTERFACE



eMMC FLASH

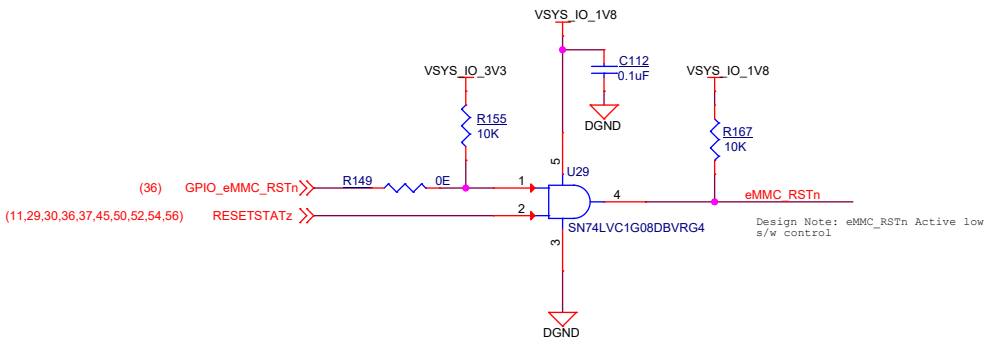


Via Probe Test Points

Place Near eMMC side

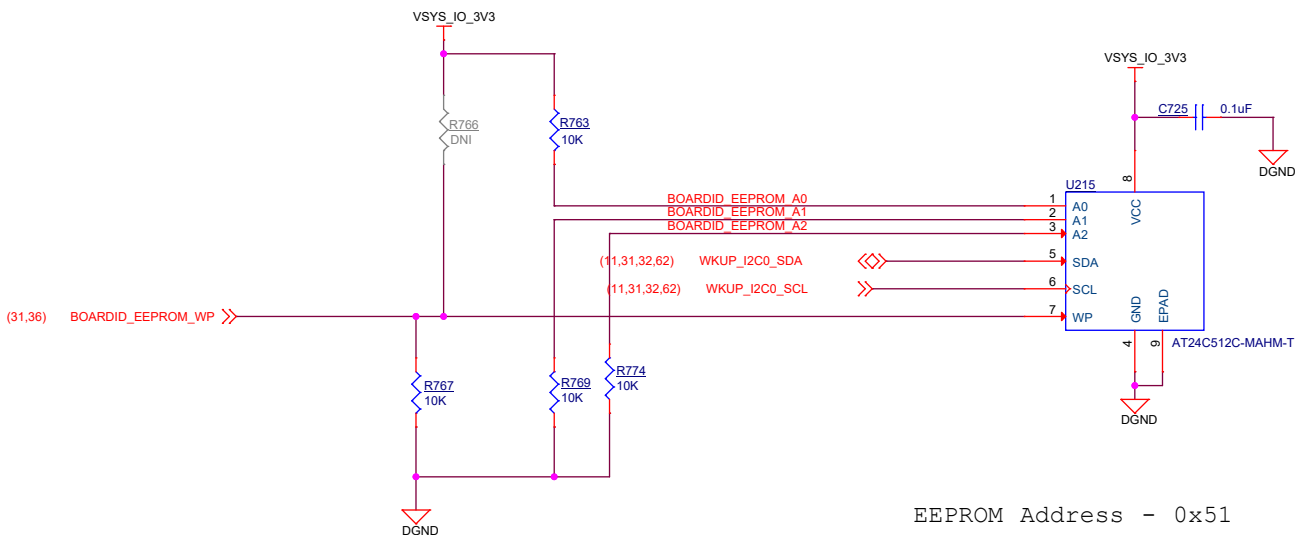
TP63	DNI	MMC0_DAT0
TP67	DNI	MMC0_DAT1
TP69	DNI	MMC0_DAT2
TP59	DNI	MMC0_DAT3
TP61	DNI	MMC0_DAT4
TP65	DNI	MMC0_DAT5
TP70	DNI	MMC0_DAT6
TP161	DNI	MMC0_DAT7
TP159	DNI	MMC0_DS_R
TP56	DNI	MMC0_CLK
TP160	DNI	MMC0_CMD

eMMC FLASH RESET

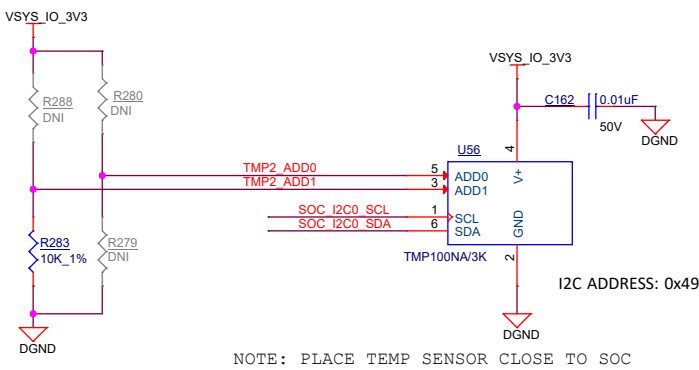
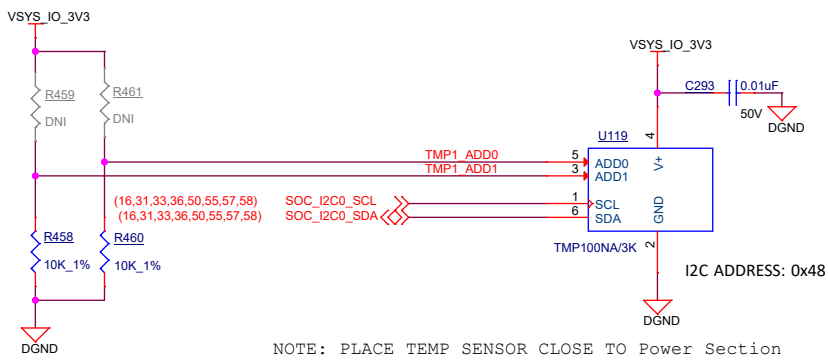


I2C for BOARD ID EEPROMs

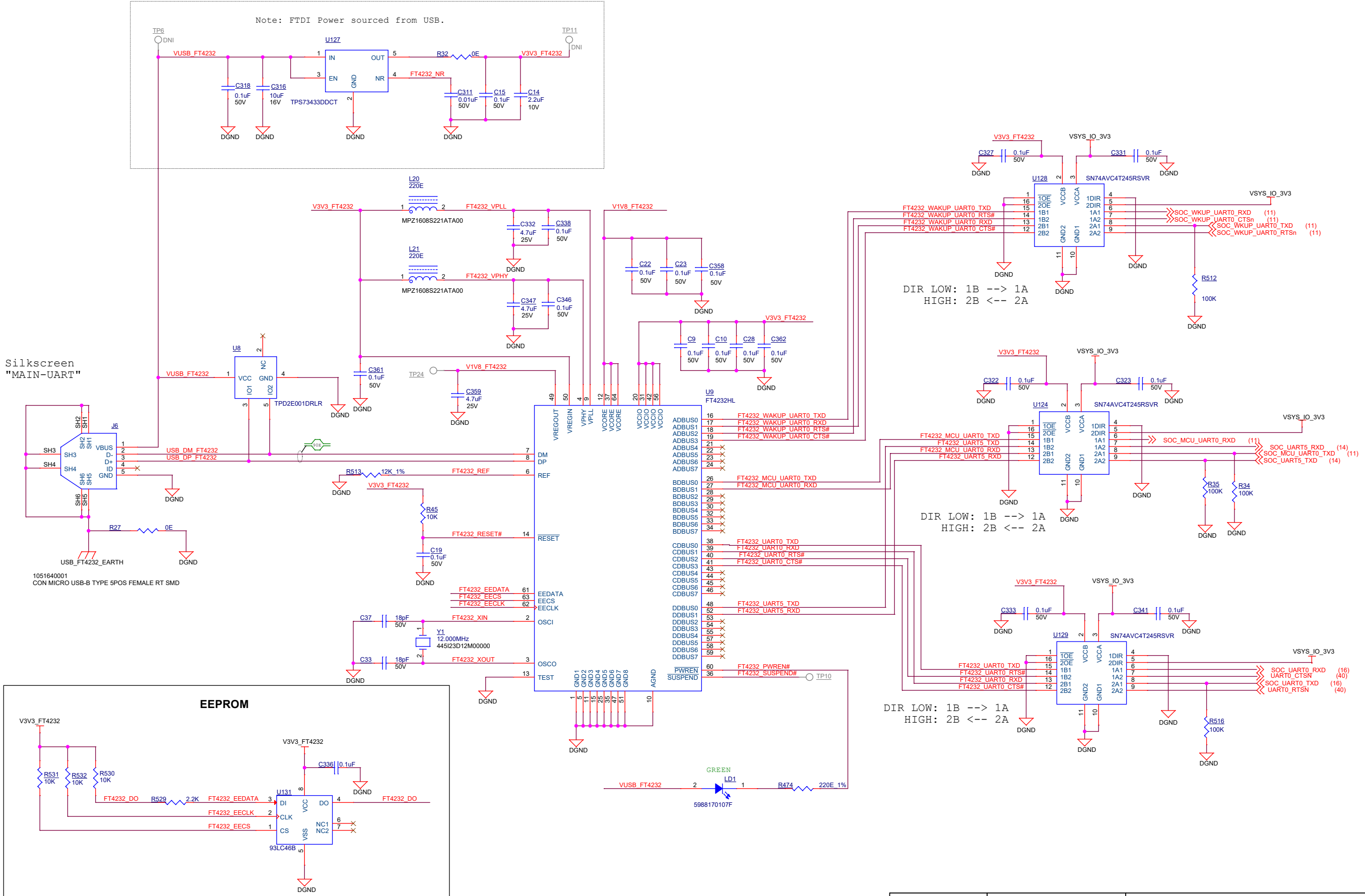
BOARD ID EEPROM



TEMPERATURE SENSORS
(TI EVM Only)



QUAD PORT FTDI



Note: FTDI EEPROM for storing manufacturing/configuration information.

XDS110 DEBUGGER

Silkscreen "XDS110"

1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD

(34,57) TA_POWERDOWNz<<
(35,57) TA_PORZn<<
(35,57) TA_RESETz<<
(16,57) TA_SOC_INT1z<<
(56,57) TA_BM_IOEXP_RSTn<<
(56,57) TA_BOOTMODE_CNTL#<<

SN74AVC87245PWR buffer is used to isolate test automation from xds110

Set the unique ID
of the debugger

Project :

J7 EVM



Title
XDS110 DEBUGGER

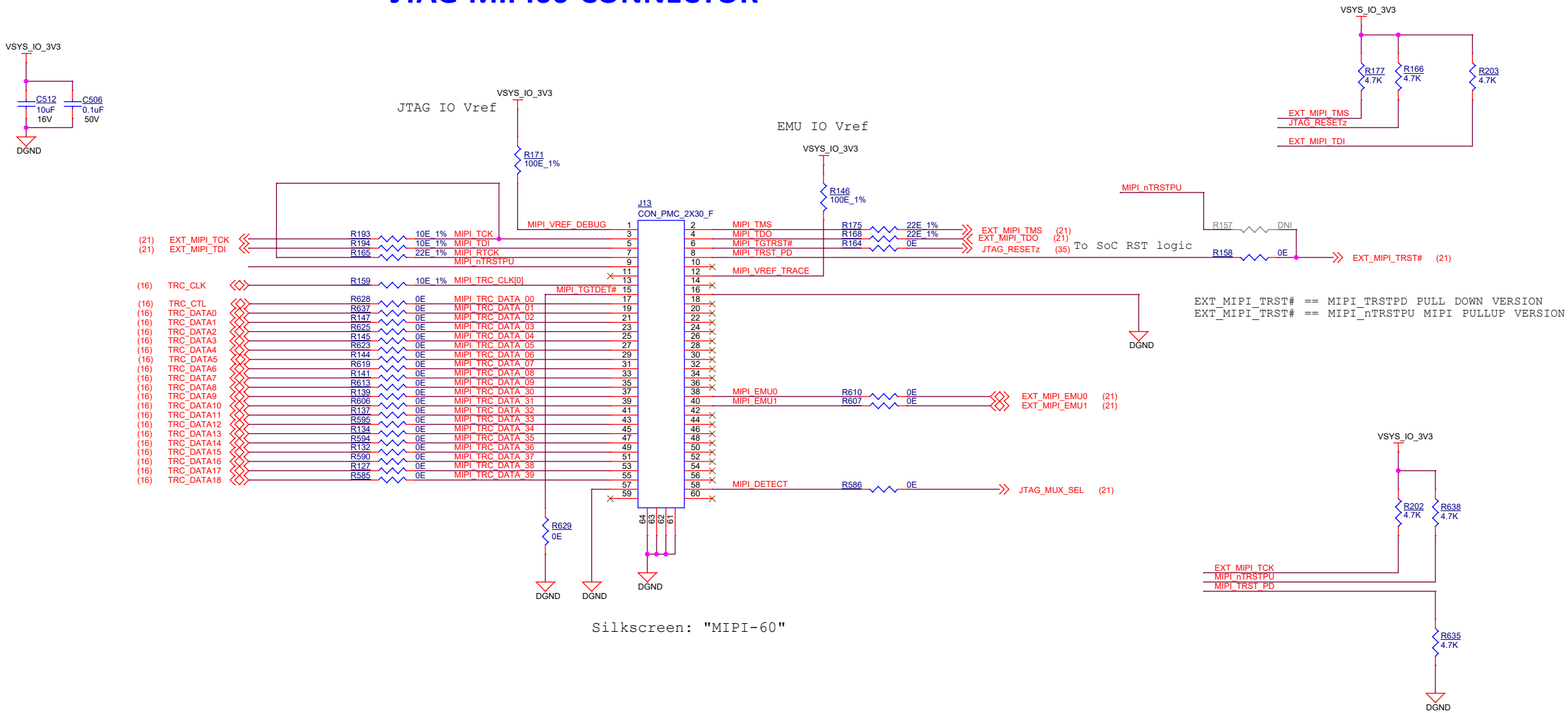
Size
C
PROC170 002 EVM

Date: Thursday, March 07, 2024

Rev
E3

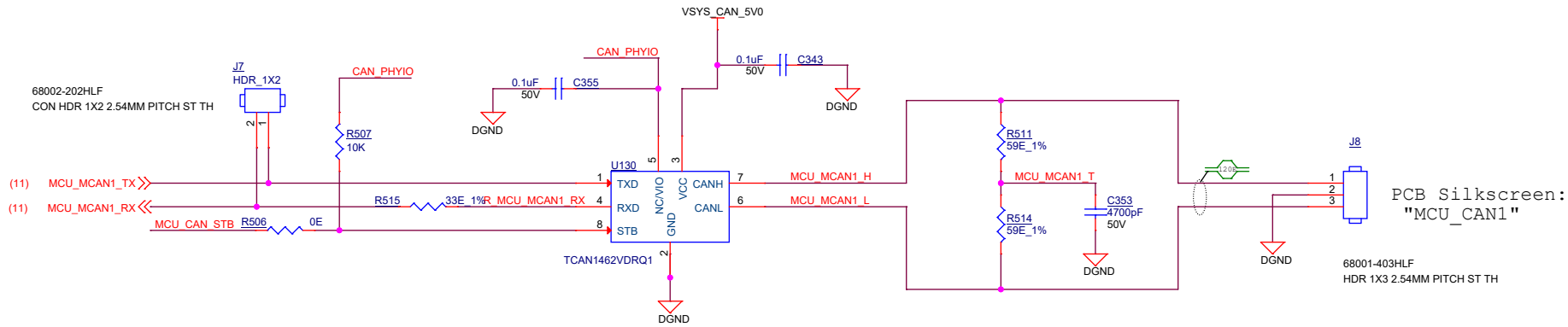
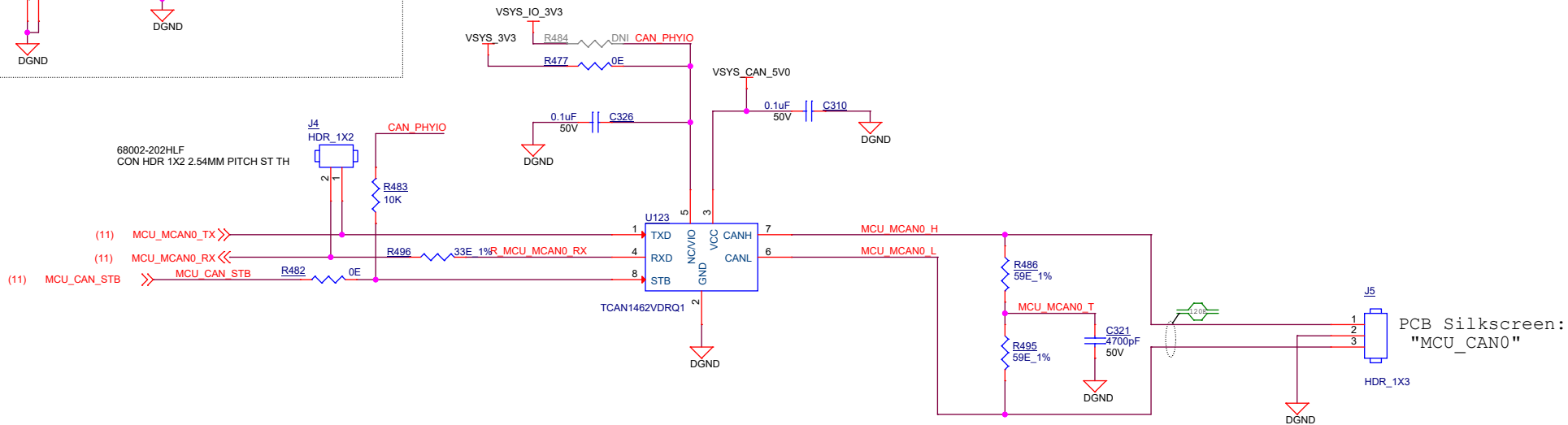
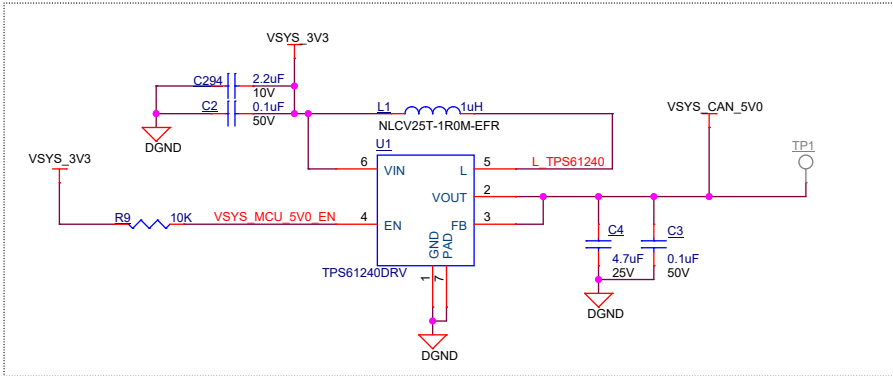
Sheet 41 of 68

JTAG MIPI60 CONNECTOR

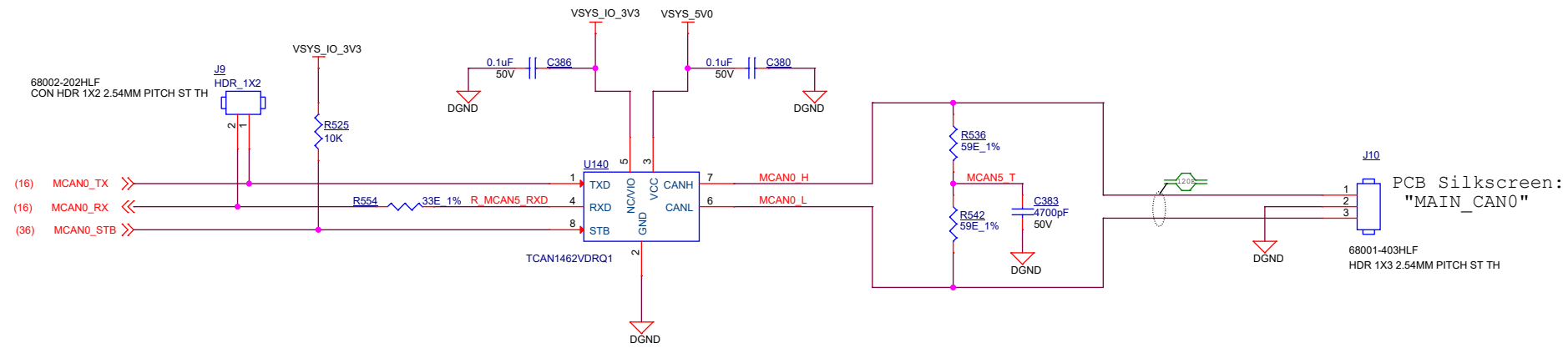


Silkscreen: "MIPI-60"

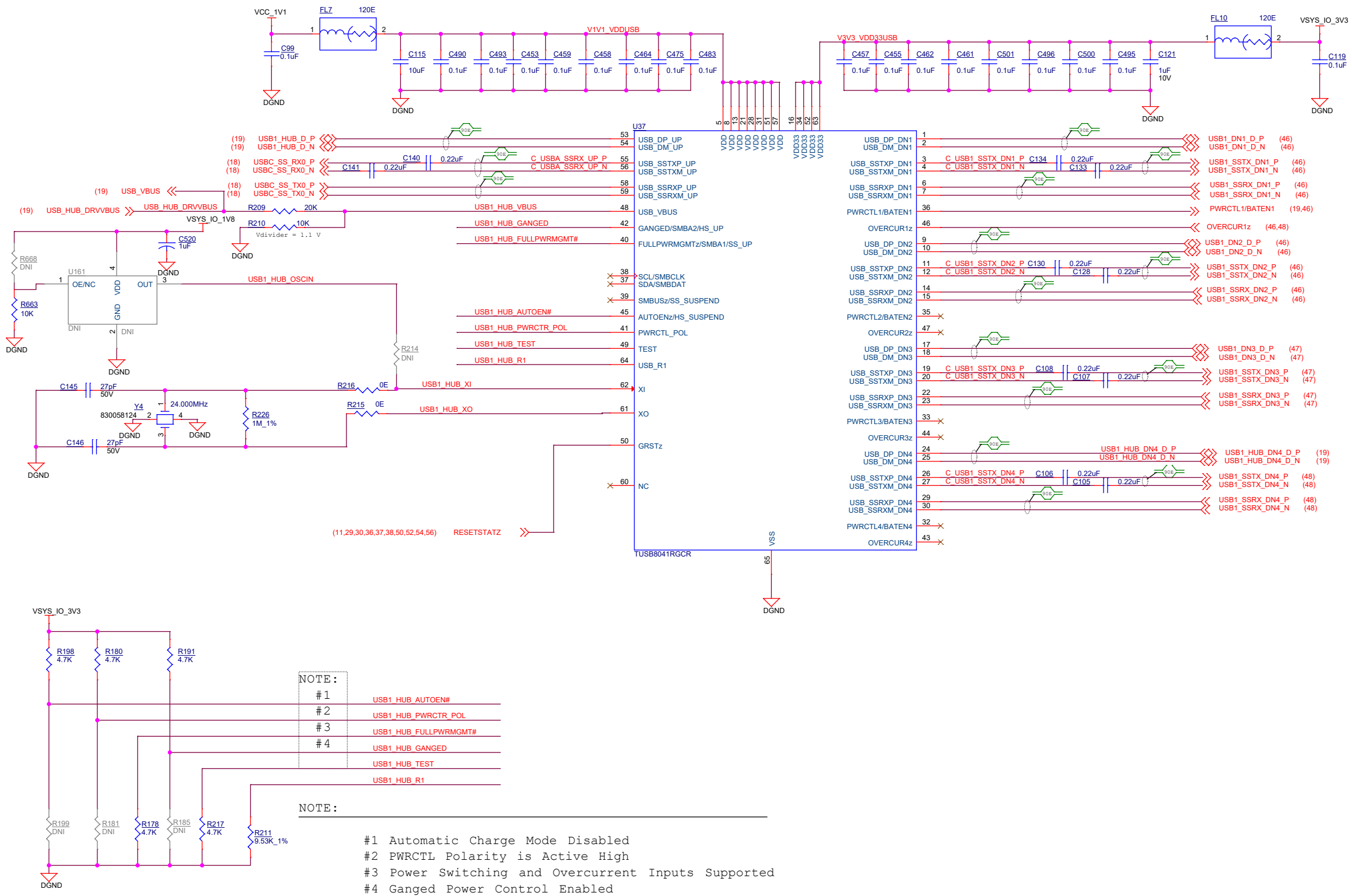
CAN TRANSCEIVERS #1-MCU DOMAIN



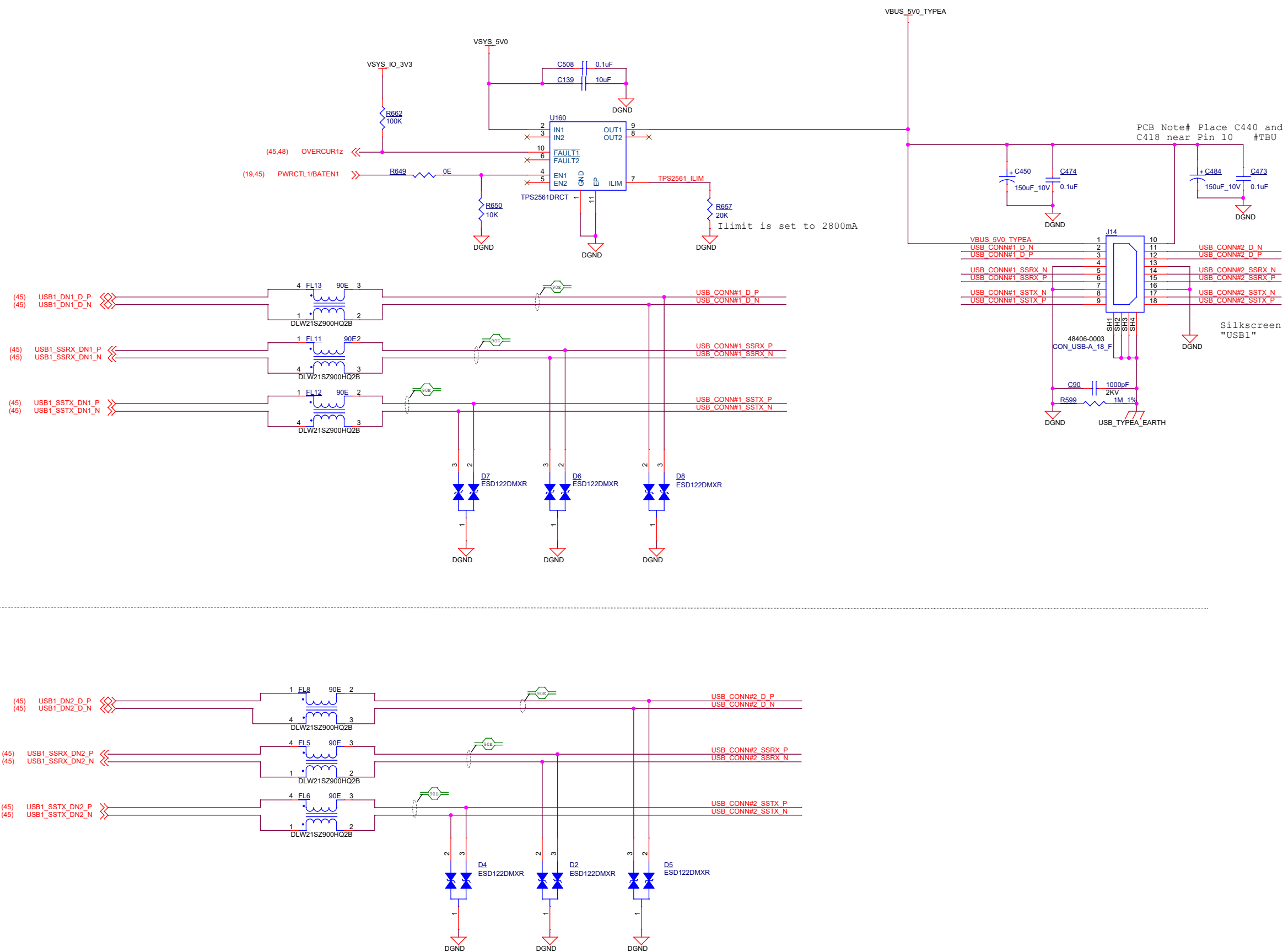
CAN TRANSCEIVERS #2-MAIN DOMAIN



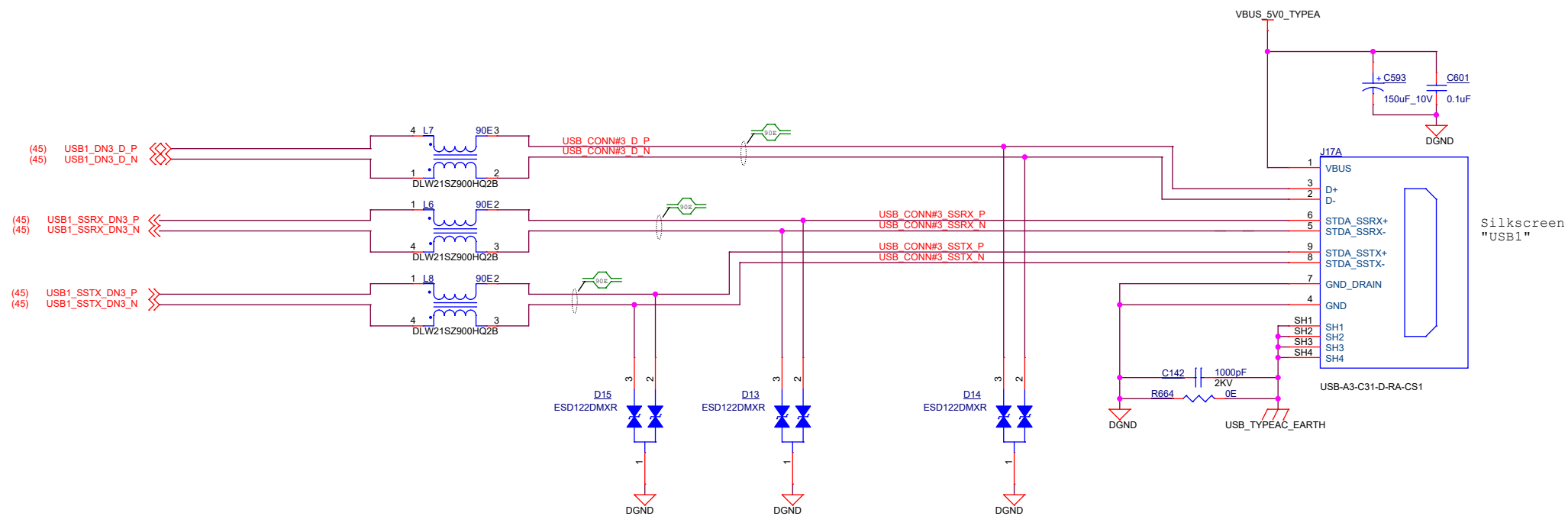
USB3.0 HUB



USB 3.0 TYPE-A CONNECTORS - 1

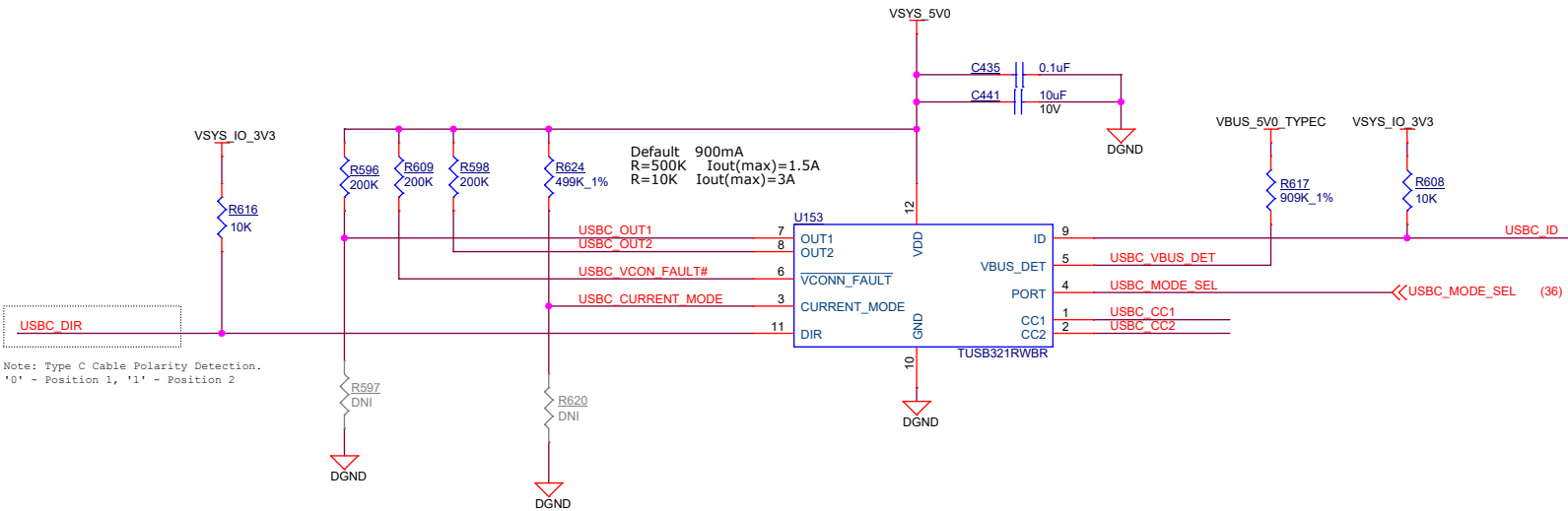


USB 3.0 TYPE-A CONNECTORS - 2

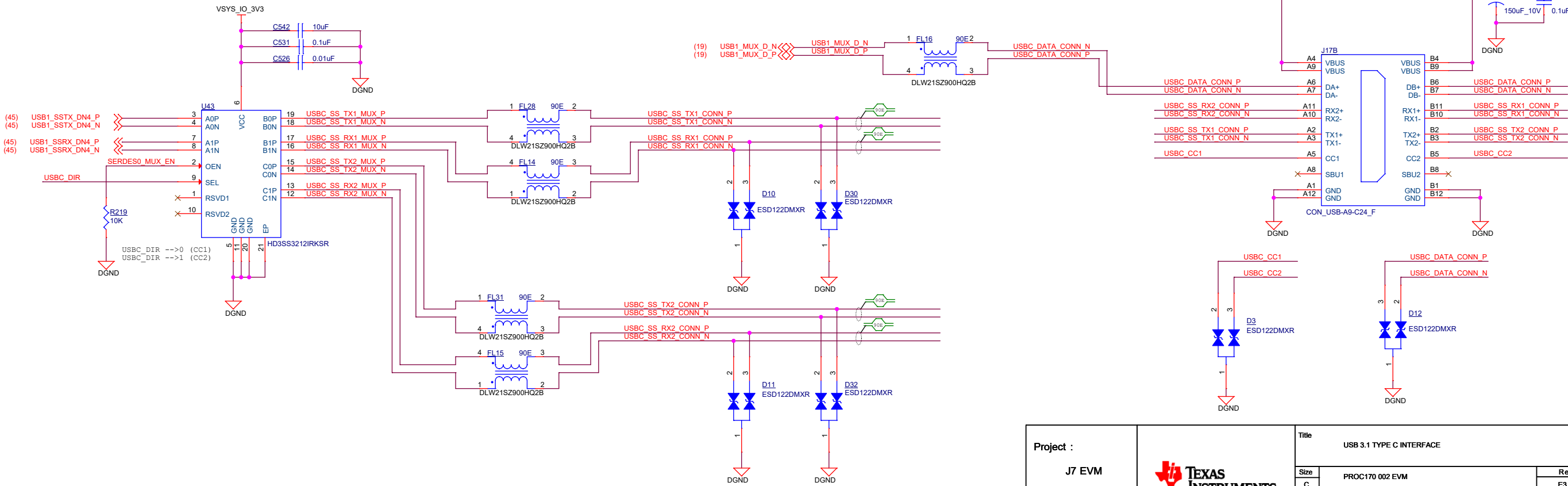
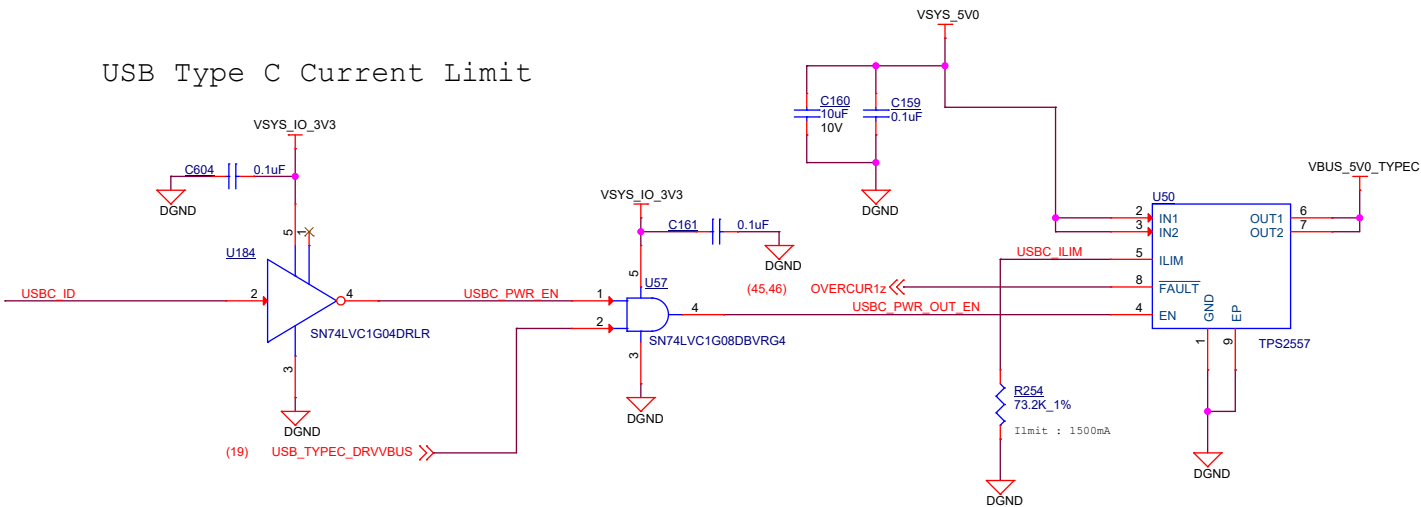


USB 3.0 TYPE C INTERFACE

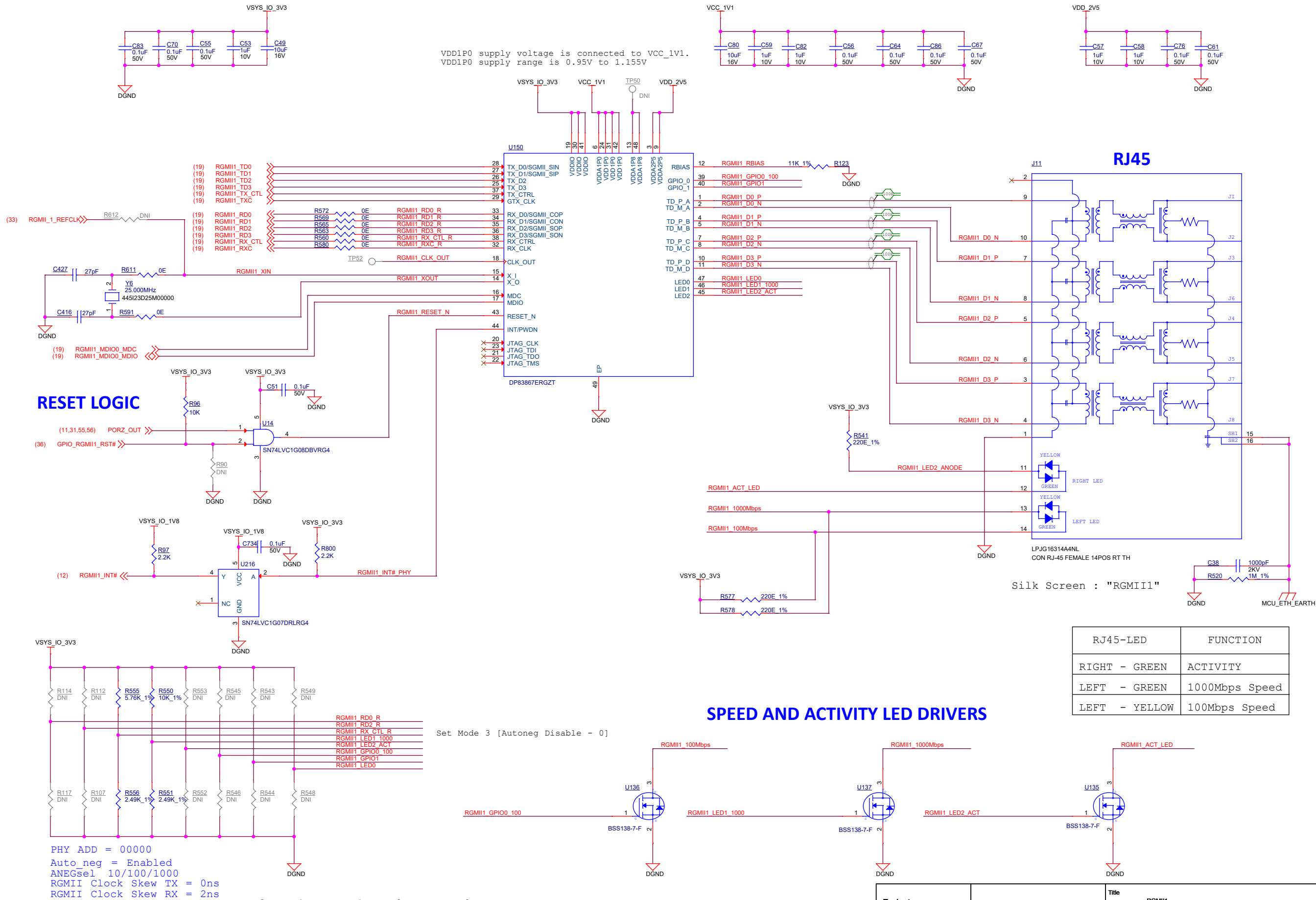
USBC_MODE_SEL	Selected USB C Mode
LOW	UFP
HIGH	DFP



USB Type C Current Limit

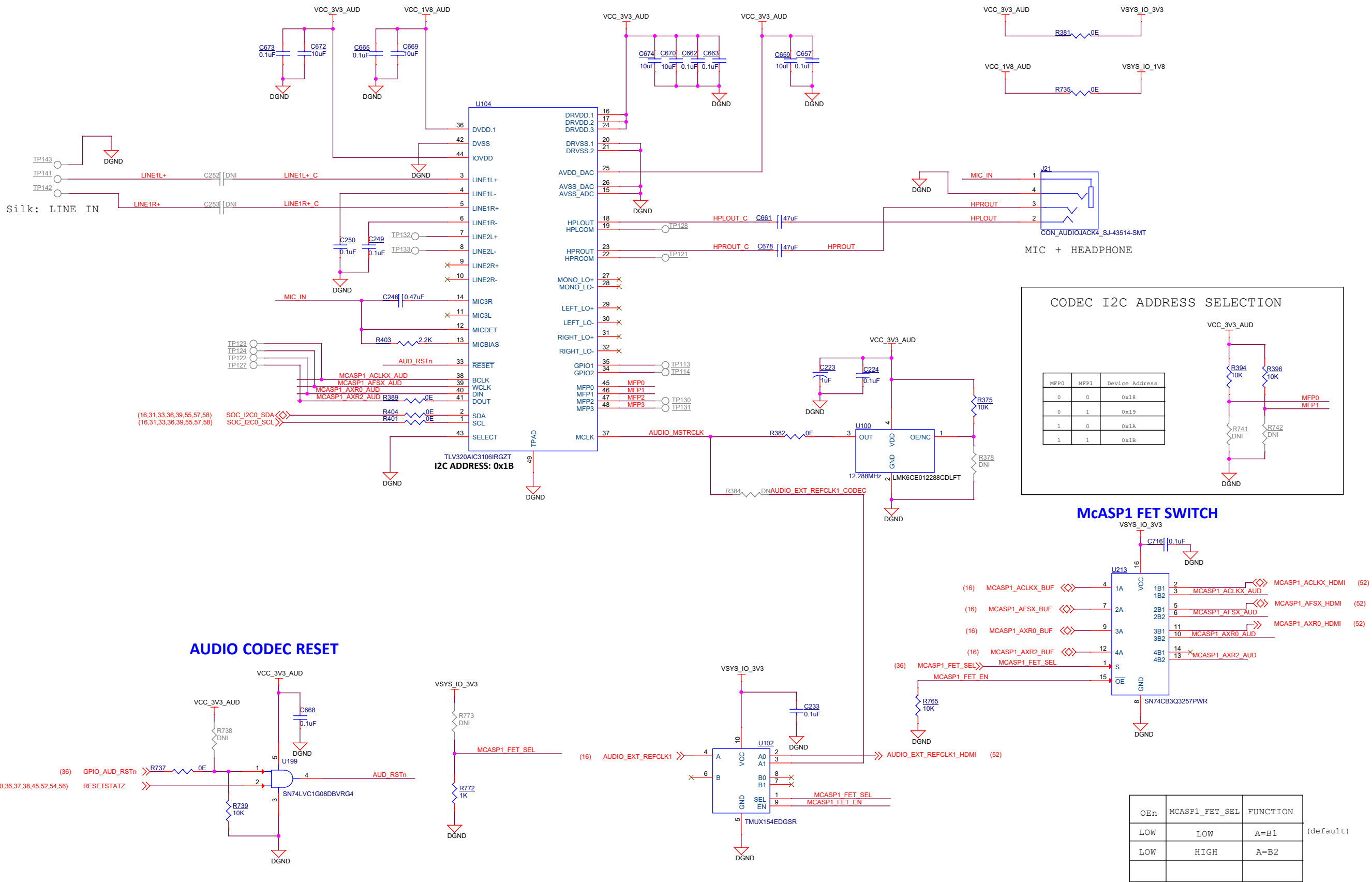


RGMII1

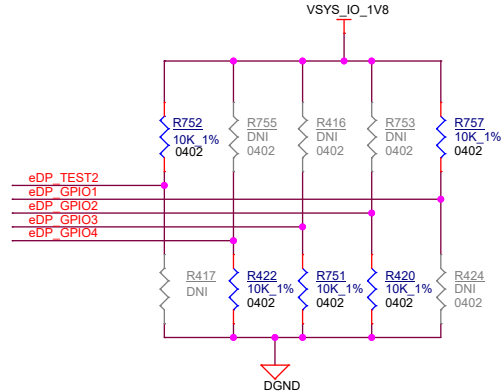
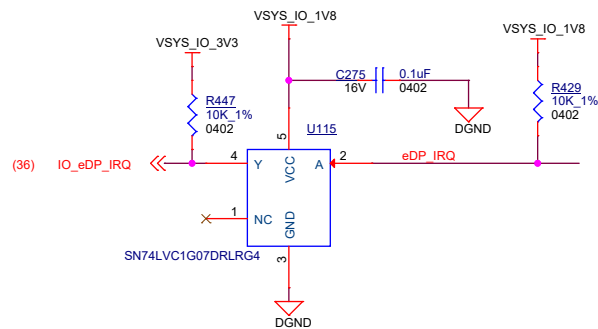
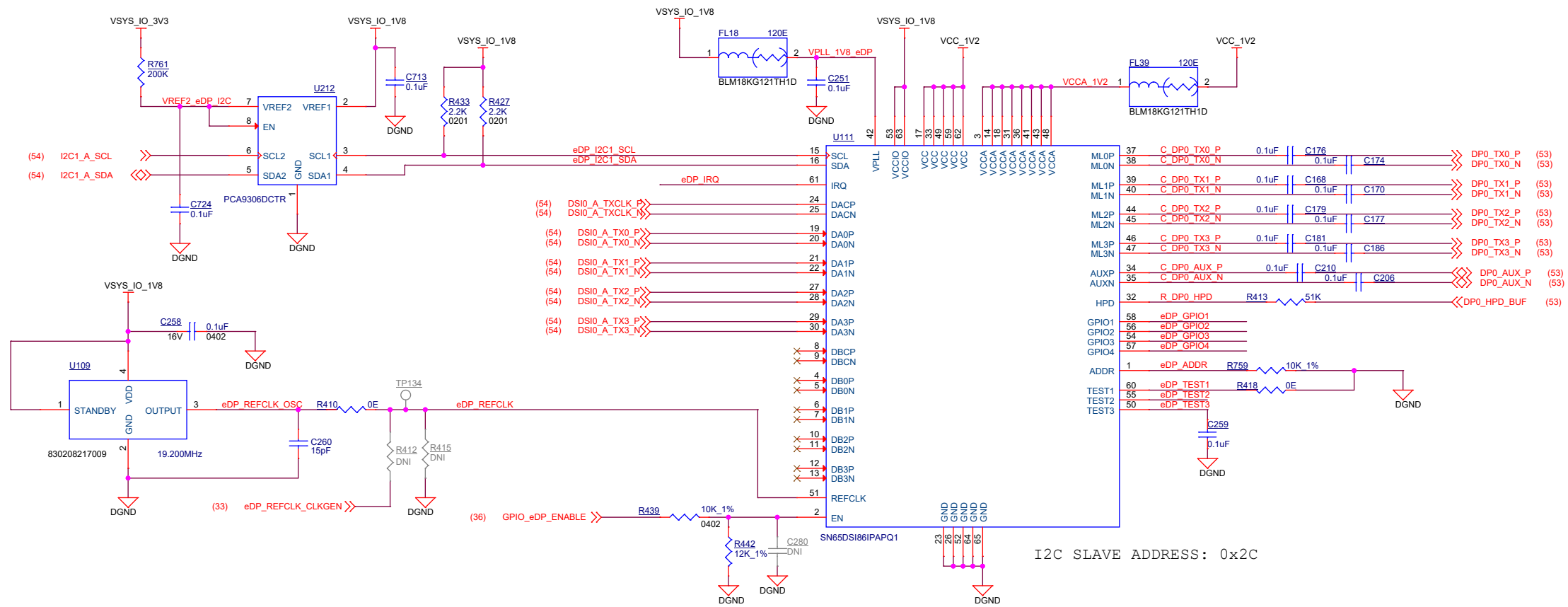


RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

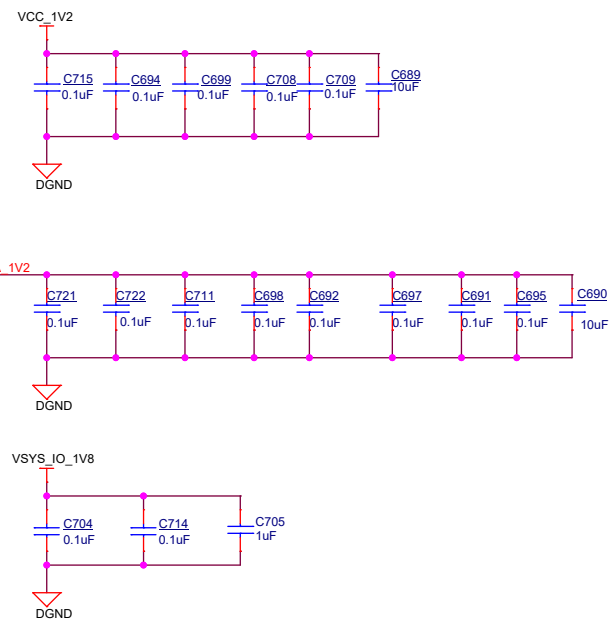
AUDIO CODEC



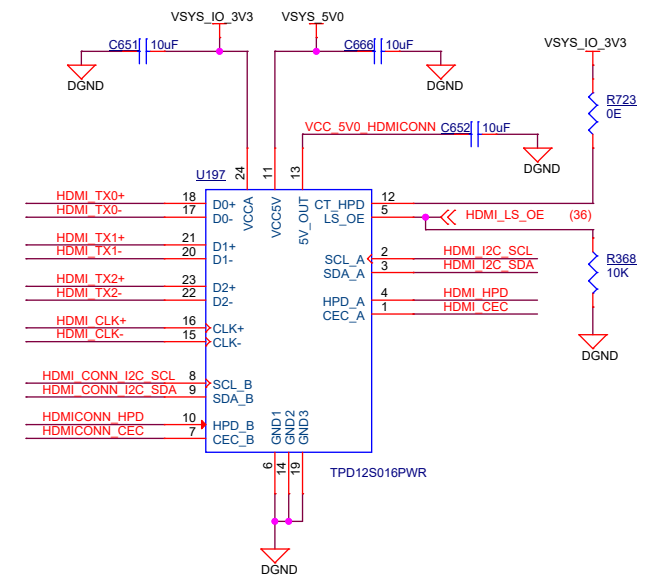
DSI to eDP Bridge



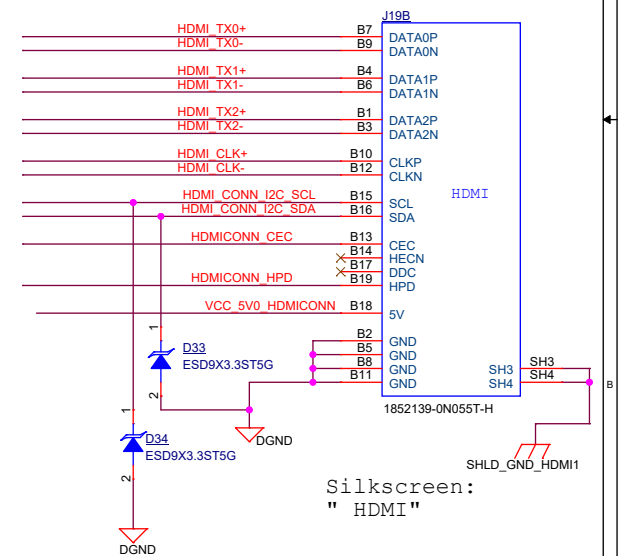
GPIO[3:1] is set as 3'b001 for 19.2MHz External Refclk



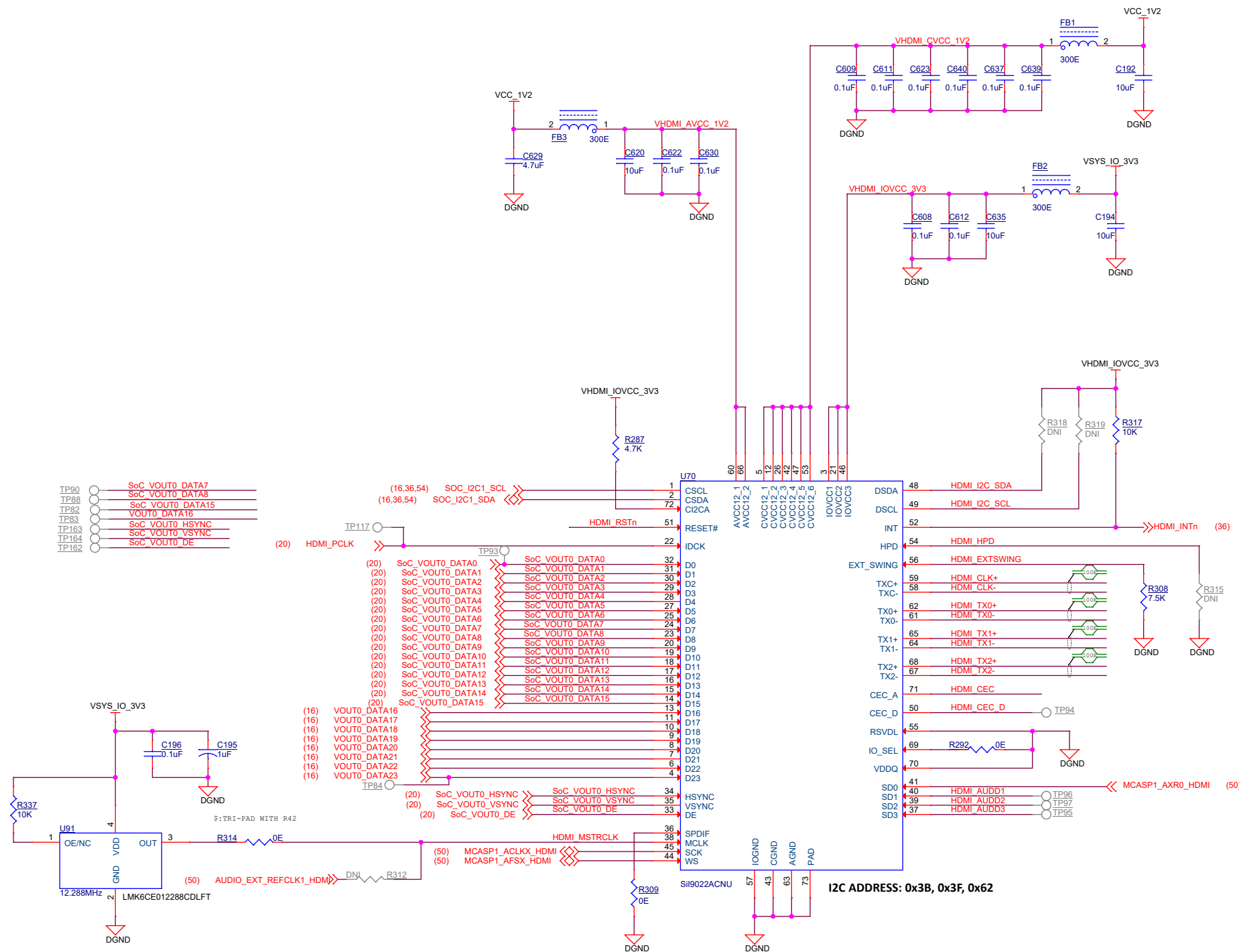
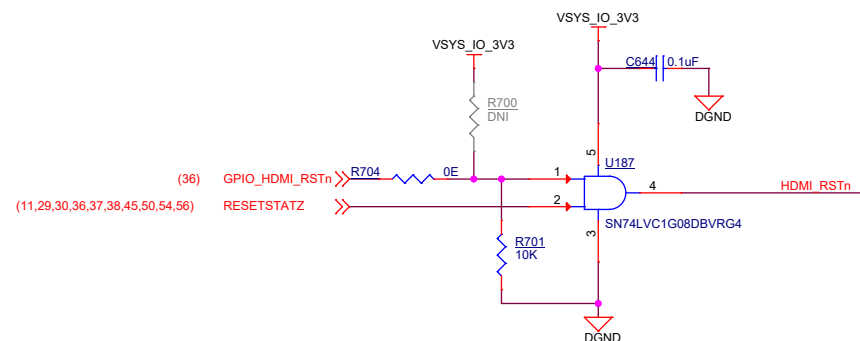
HDMI INTERFACE



NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.



```
Silkscreen:
" HDMI"
```

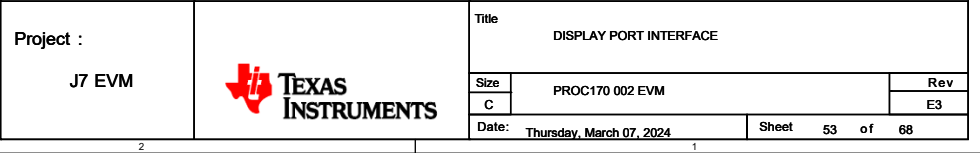


I2C ADDRESS: 0x3B, 0x3F, 0x62

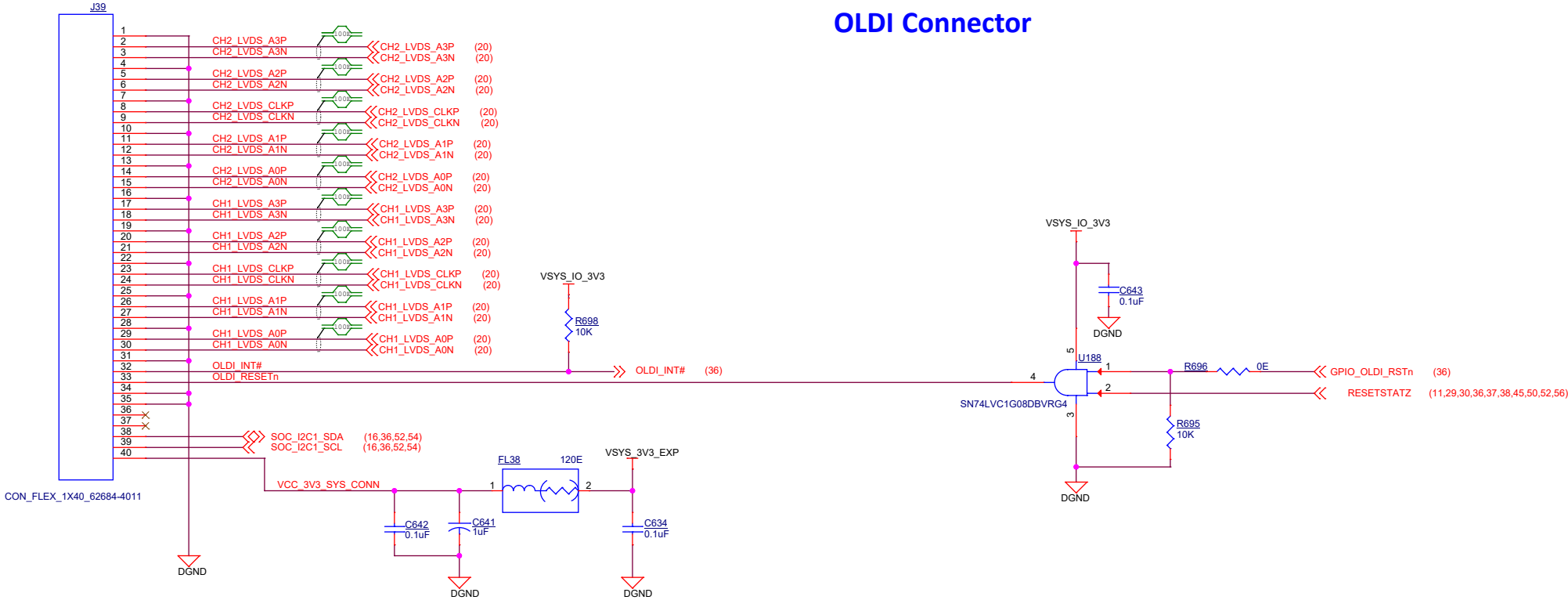
Project : J7 EVM



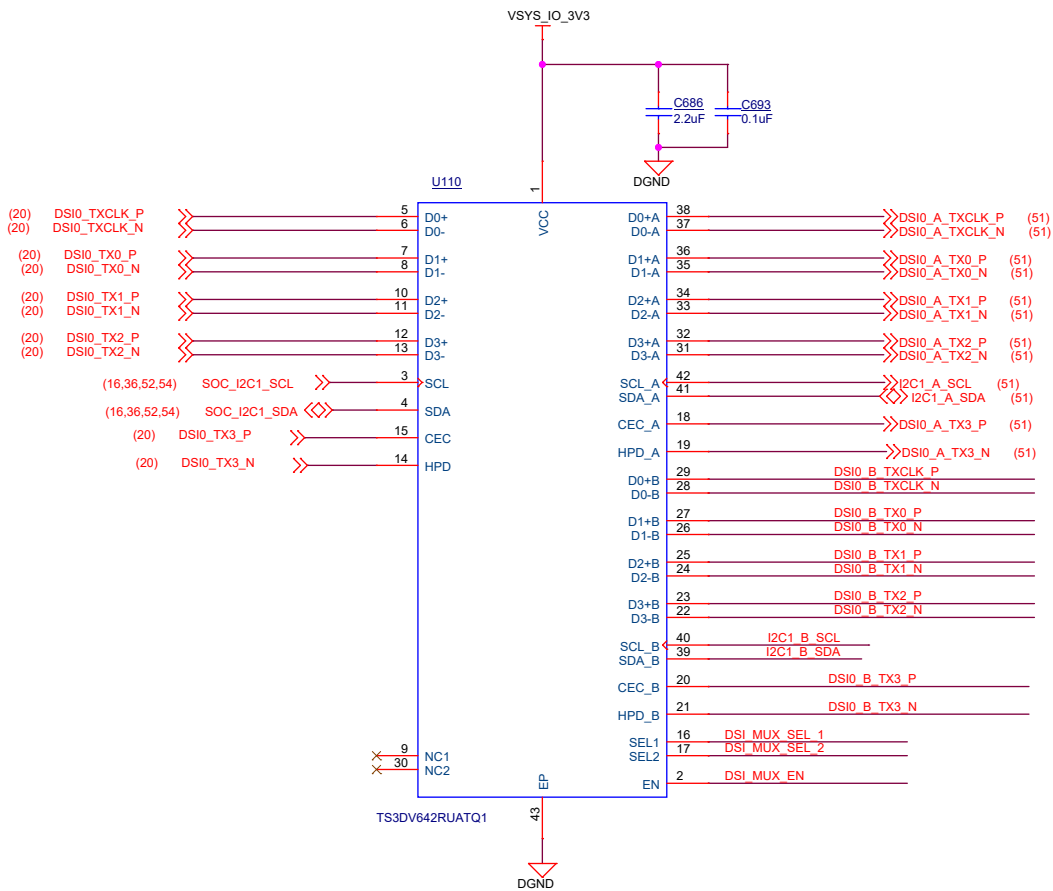
Title SOC DIGITAL IO & SUPPORT POWER 2			
Size	PROC170 002 EVM		Rev
C			E3
Date:	Thursday, March 07, 2024	Sheet 52 of 68	



OLDI Connector

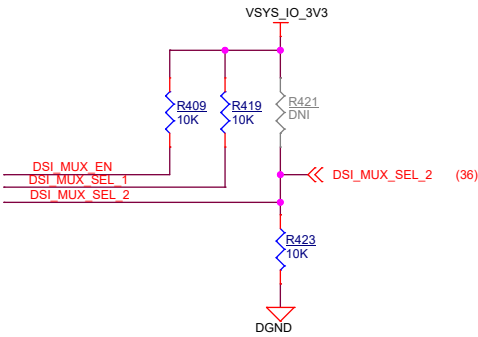


DSI Flex Connector



To DSI to eDP Bridge

To DSI FPC Connector



EN	DSI_MUX_SEL_2	FUNCTION
HIGH	LOW	INPUT --> A Port [DSI to eDP Bridge]
HIGH	HIGH	INPUT -->B port [DSI FPC Connector] (default)
LOW	X	Disconnect

x4 Lane PCIe Connector

C

```
to SOC (18) SOC_SERDES1_REFCLK_P <
(18) SOC_SERDES1_REFCLK_N <
```

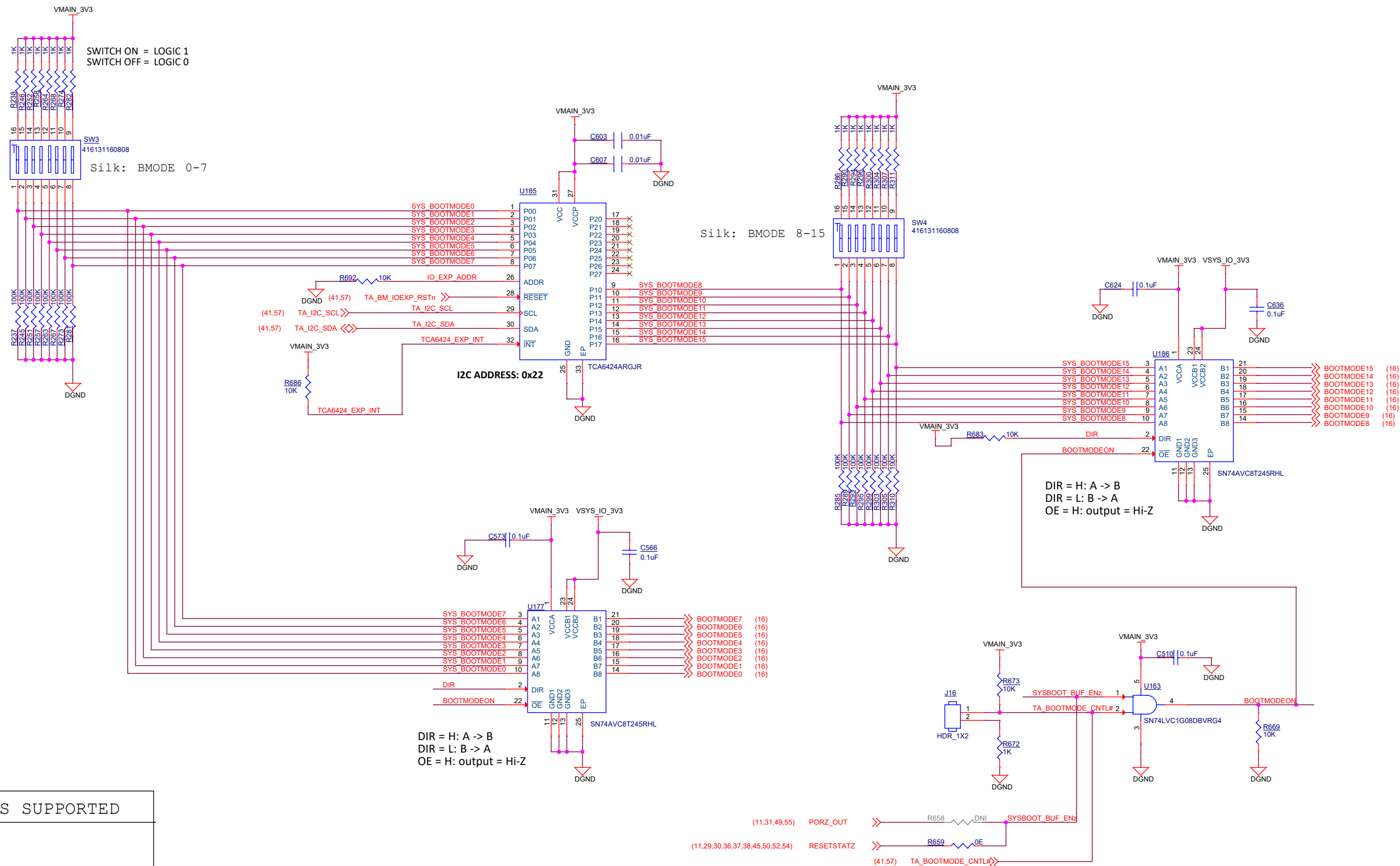
Title			
x1LANE PCIe INTERFACE			
Size	PROC170 002 EVM		Rev
C			E3
Date:	Thursday, March 07, 2024	Sheet	55 of 68

BOOT MODE BUFFER & SWITCHES

BOOT MODE SWITCHES

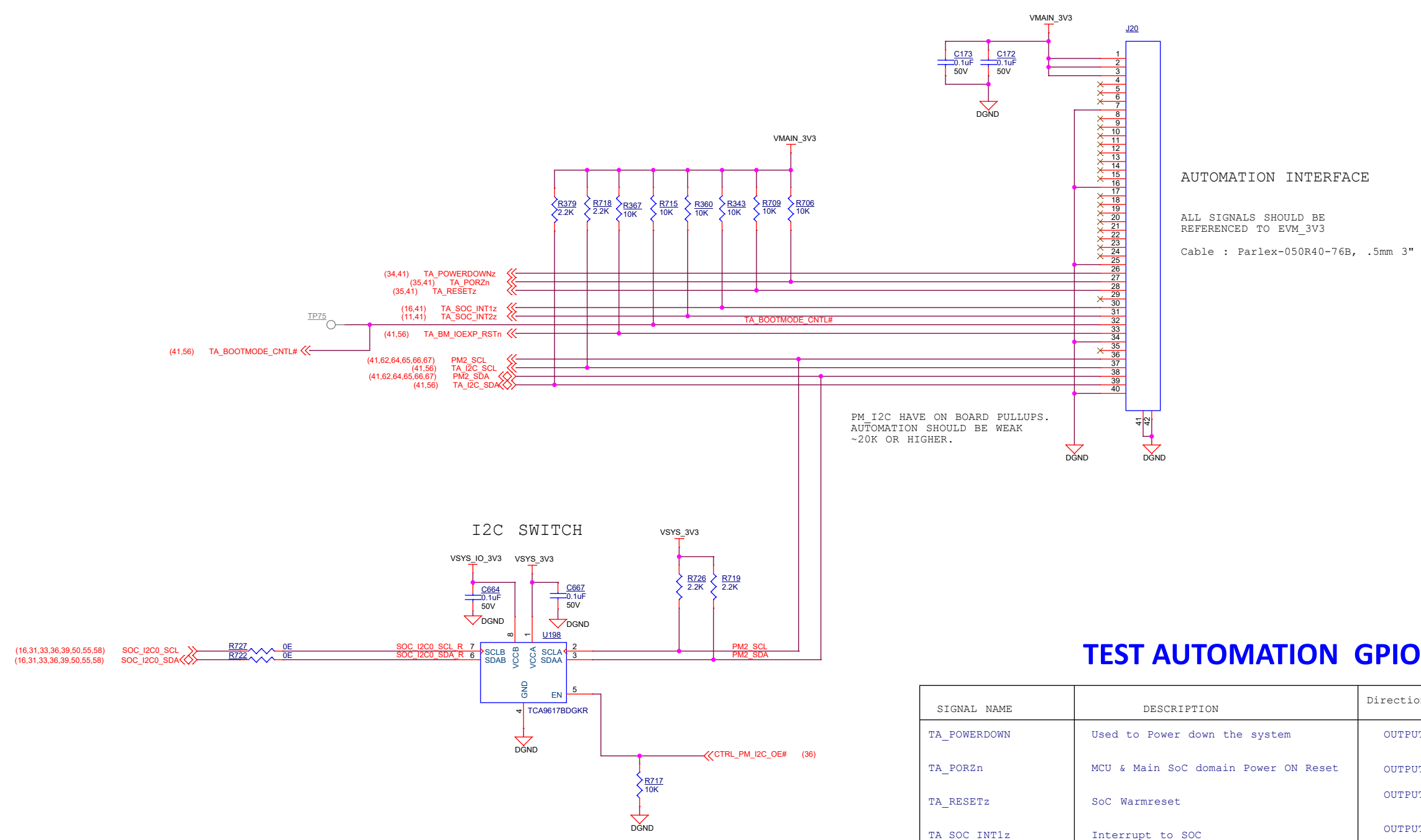
BOOTMODE IO EXPANDER

BOOT MODE BUFFERS



BOOT MODES SUPPORTED
1. OSPI
2. MMC1 - SD CARD (default)
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. No Boot

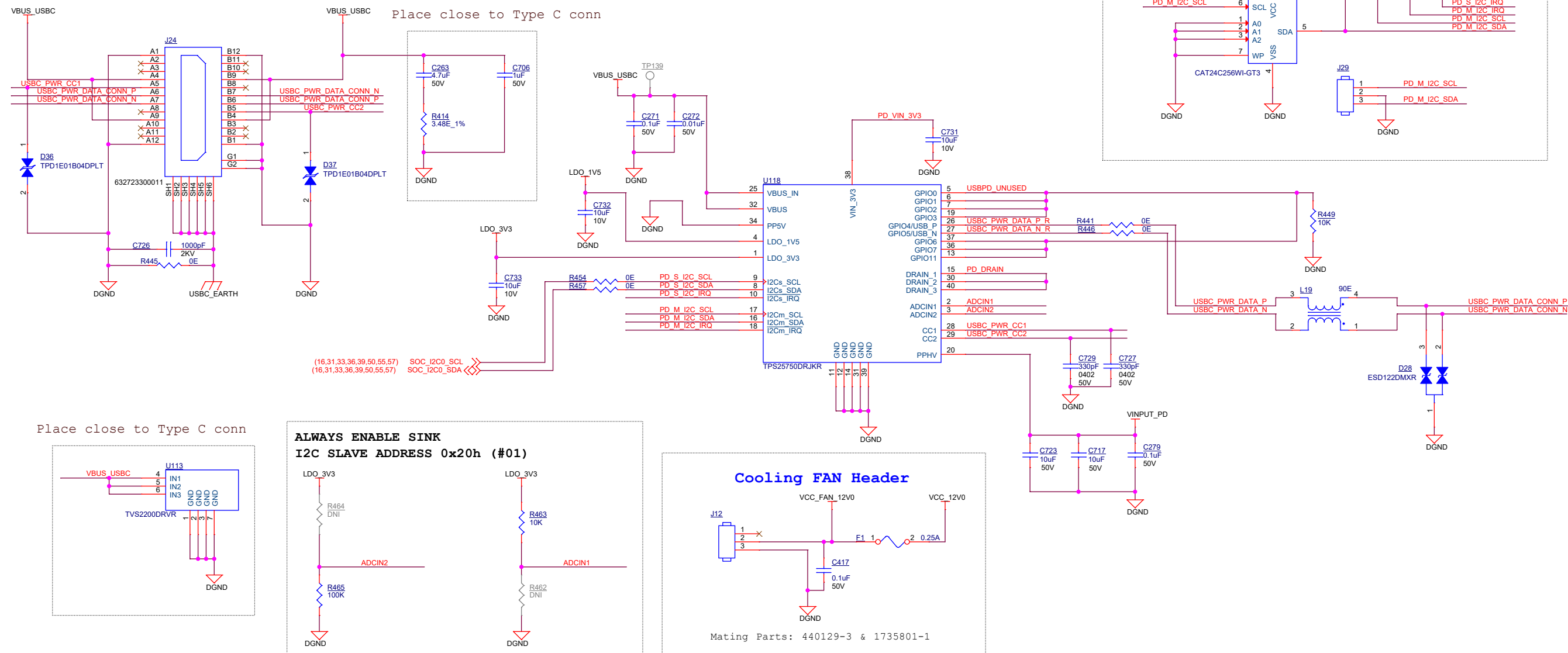
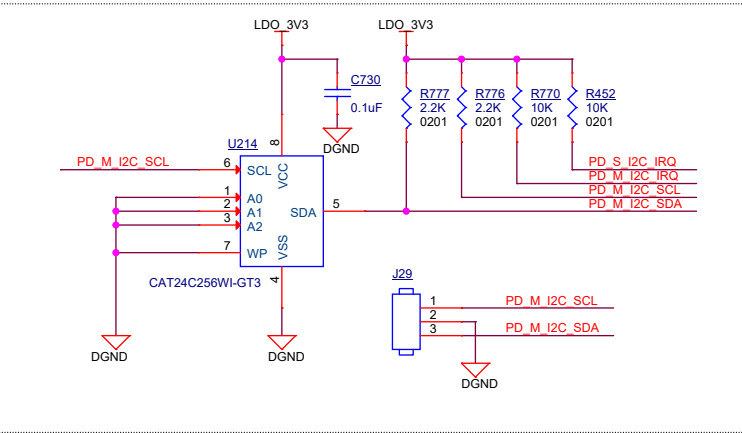
TEST AUTOMATION HEADER



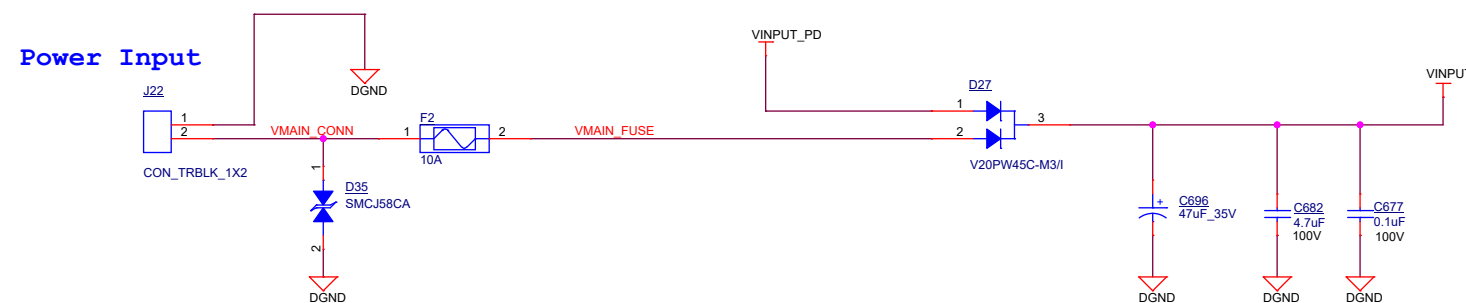
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

USB-C Power



OPTIONAL POWER INPUT



Normal operation Range for VINPVT 20V to 25V.

SILK: POWER IN

Project :

J7 EVM



Title POWER INPUT

Size	PROC170 002 EVM
C	

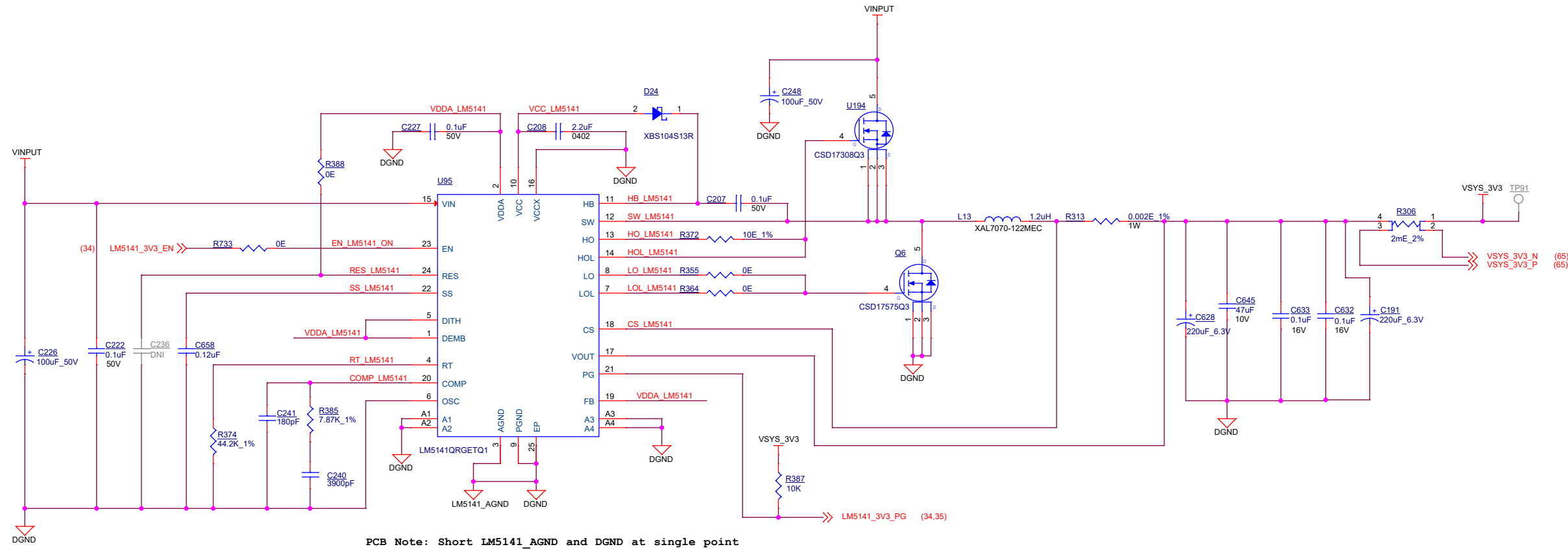
Date: Thursday, March 07, 2024

Sheet 58 of 68

Rev
E3

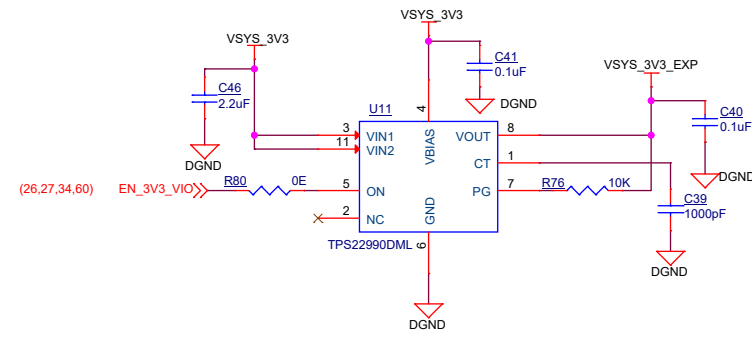
POWER SUPPLY #1
3.3V GENERATION

TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 24V
Vout1 = 3.3V@20A
Ta = 25 deg

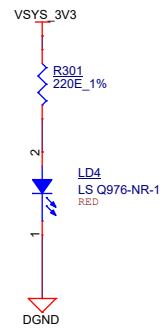


PCB Note: Short LM5141_AGND and DGND at single point

EXP3.3V GENERATION

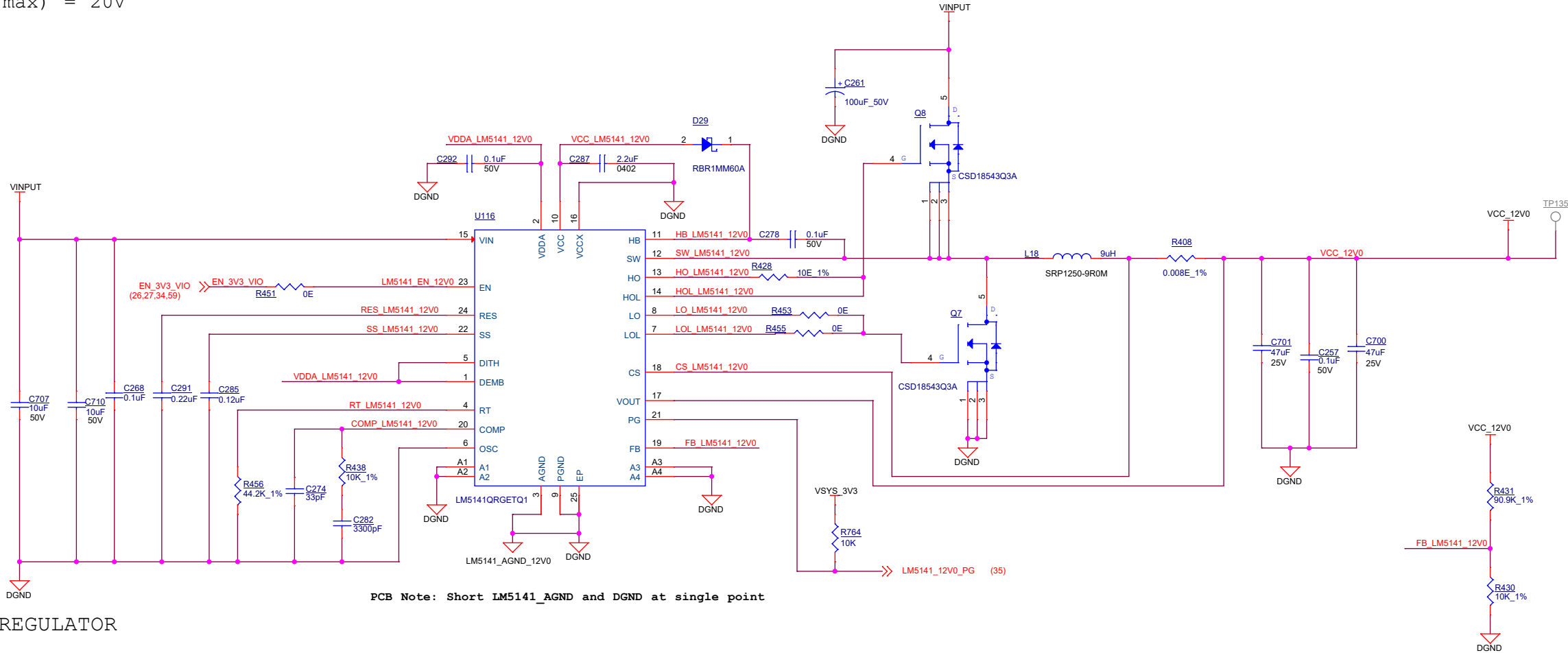


POWER INDICATION LED'S



TI WEBENCH Simulation Inputs:
Vin (min) = 15V Vin (max) = 20V
Vout = 12V@5A
Ta = 25 deg

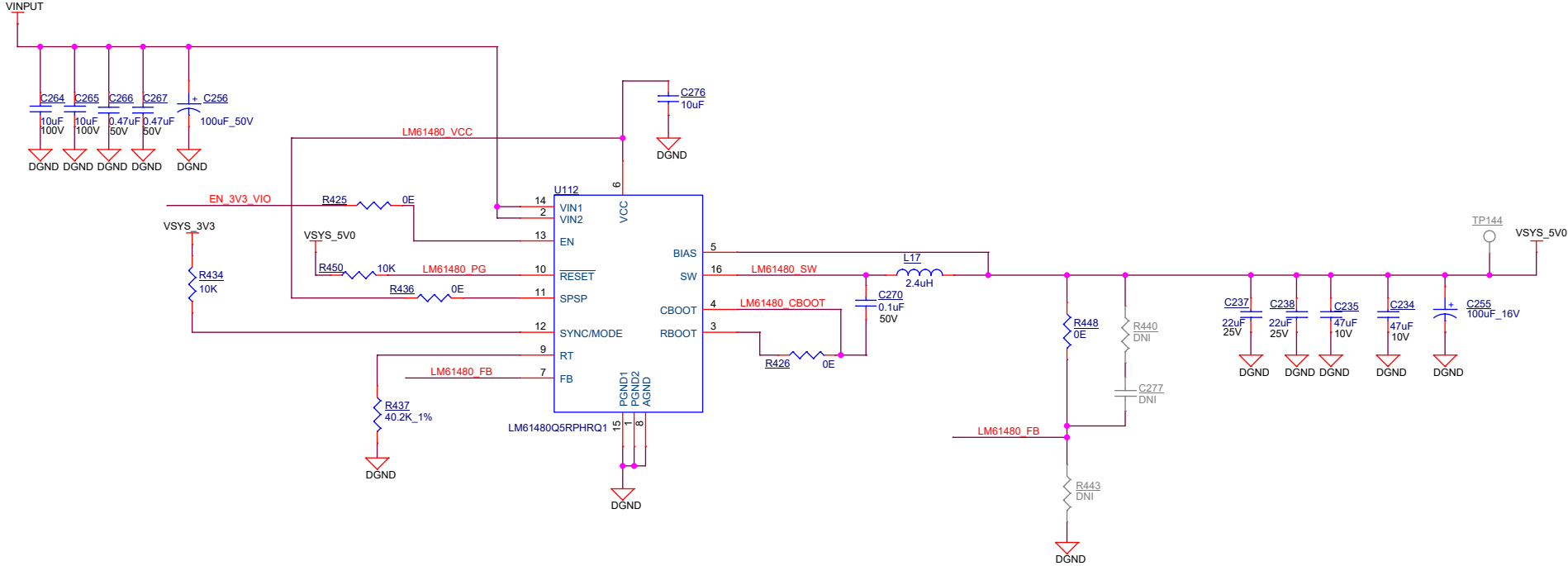
POWER SUPPLY #2



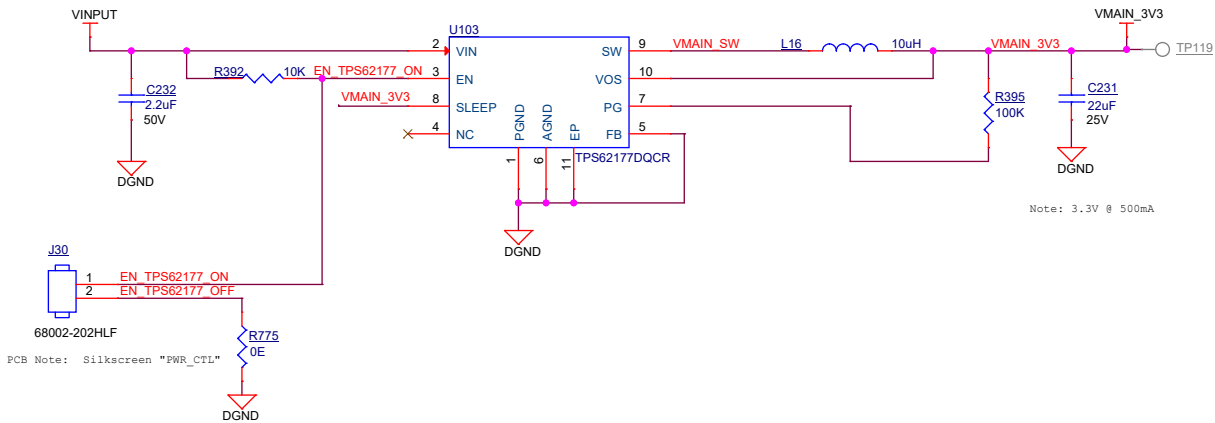
PCB Note: Short LM5141_AGND and DGND at single point

LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 24V
Vout = 5.0V
Iout = 7A

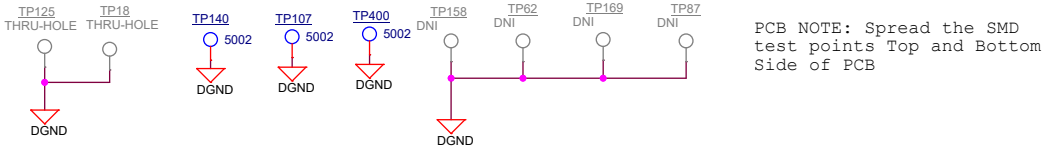
5V GENERATION



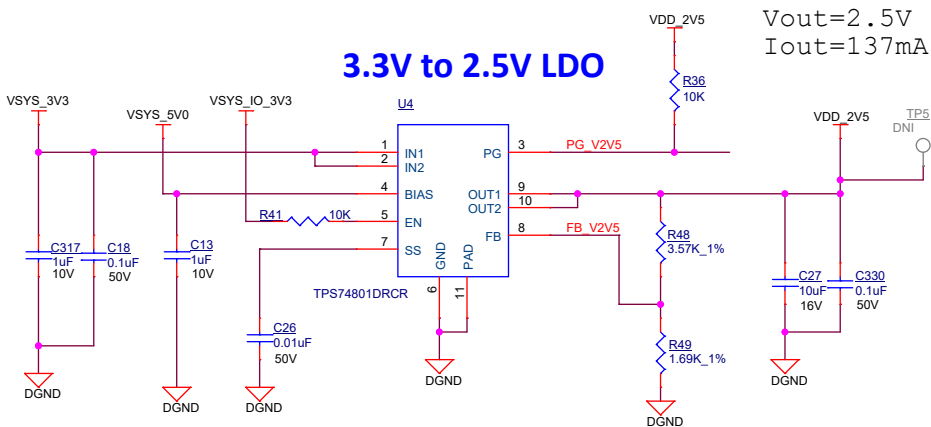
SYSTEM MANAGEMENT 3.3V REGULATOR



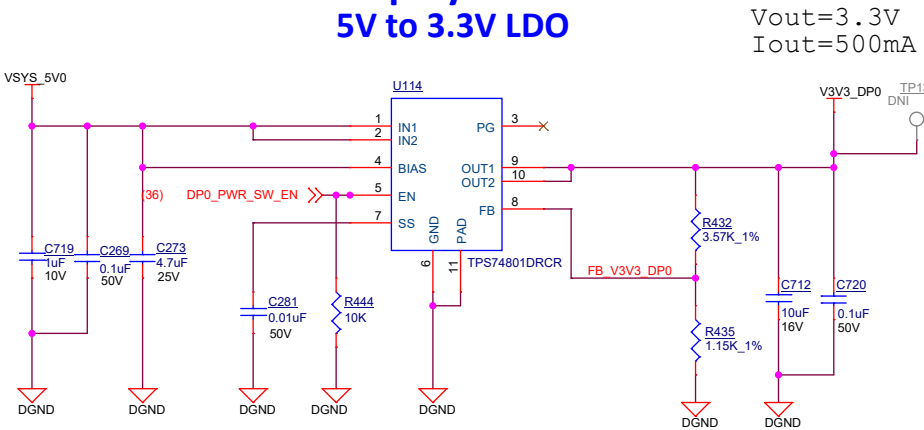
GROUND TEST POINTS



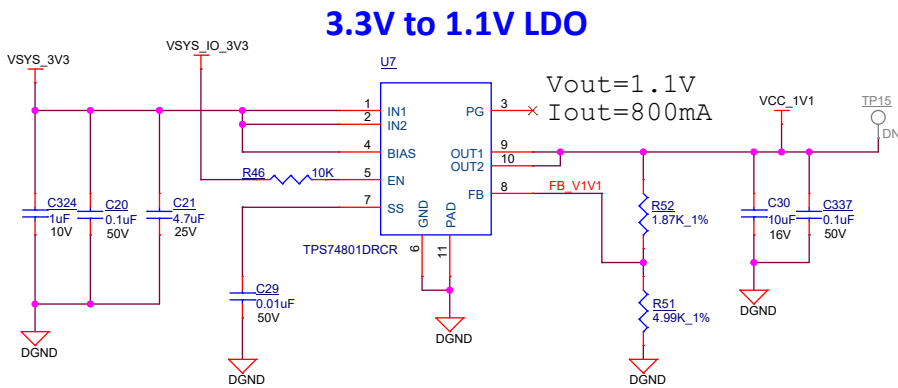
ETHERNET POWER- RGMII1



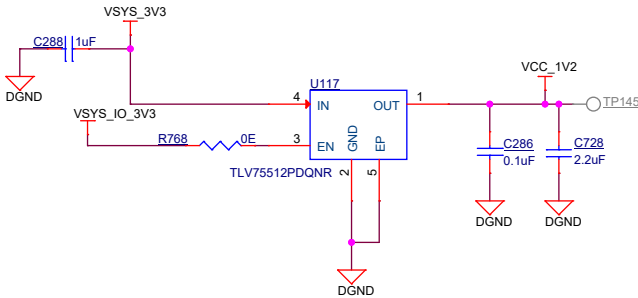
Display Port1
5V to 3.3V LDO



USB HUB POWER & ETHERNET POWER - RGMII1



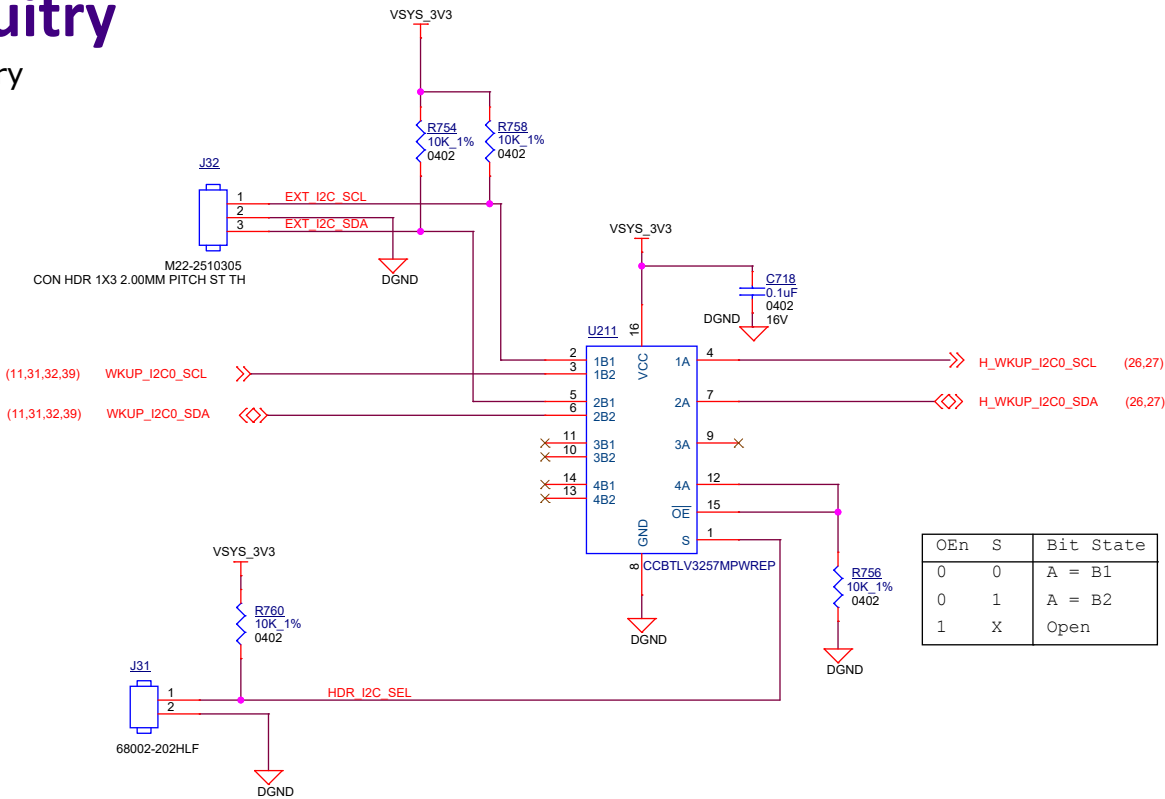
eDP bridge and HDMI Power
1.2V, 0.5AMPS SUPPLY



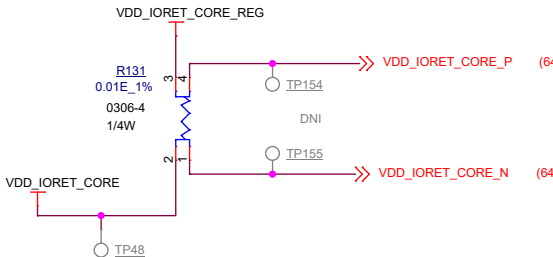
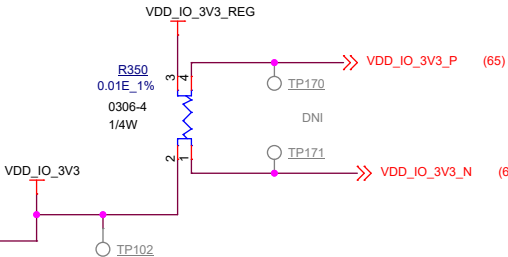
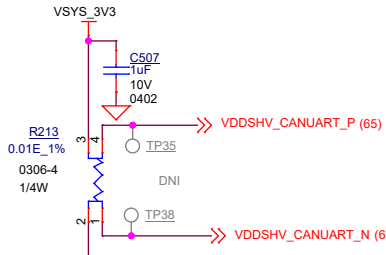
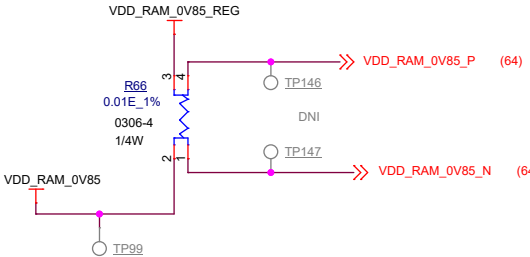
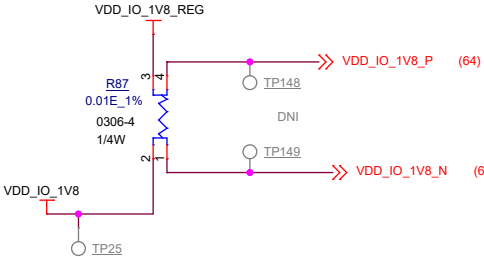
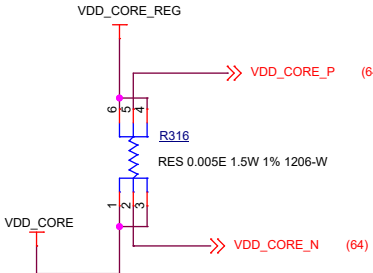
Project : J7 EVM		Title POWER SUPPLY #1	
		Size C	Rev E3
		Date: Thursday, March 07, 2024	Sheet 61 of 68

EVM PMIC Support Circuitry

EVM development & evaluation Test circuitry
(TI EVM Only)

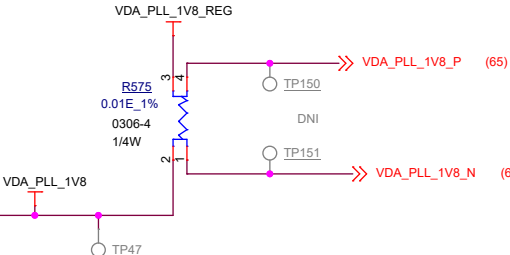
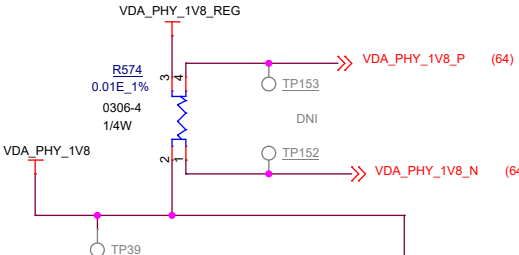


SOC Current Sense Resistors

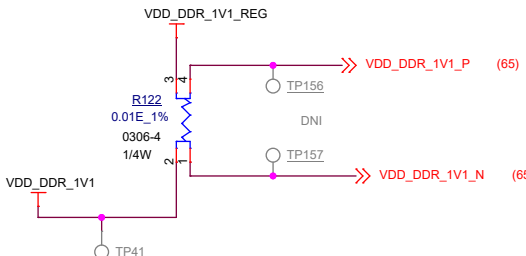
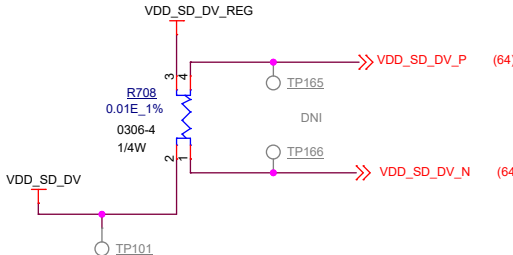


VSYS_3V3 always ON supply from pre-regulator to supply VDDSV3 CANUART for low power modes to wake-up due to CANUART IO signaling. 2x options have been provisioned

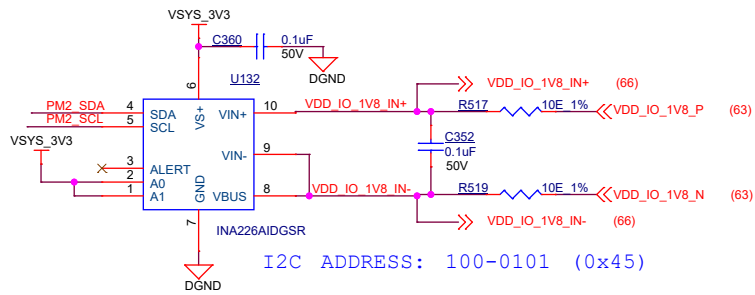
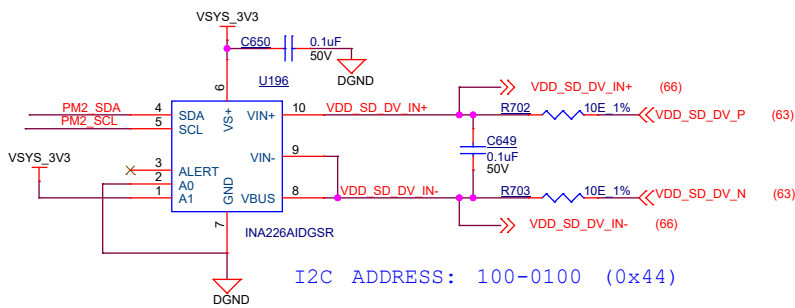
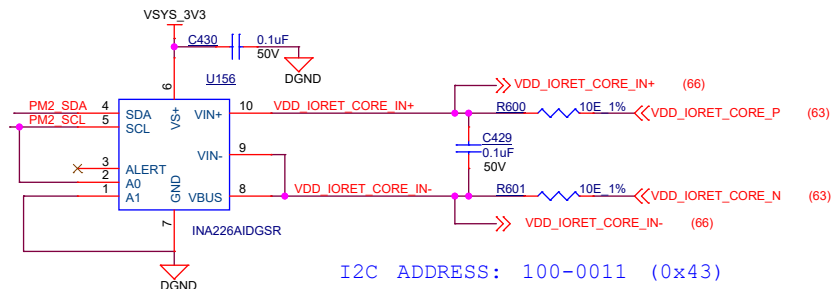
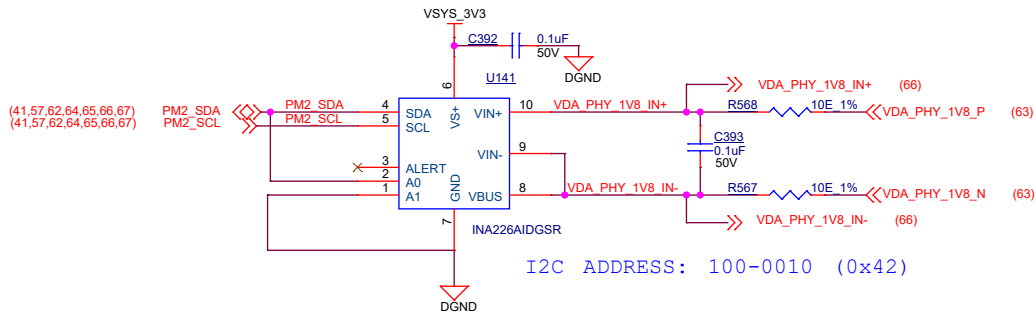
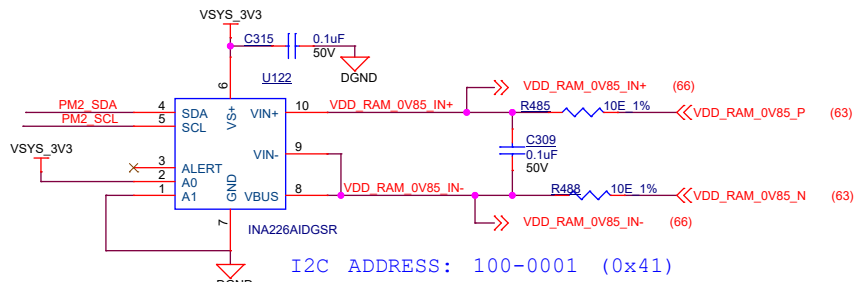
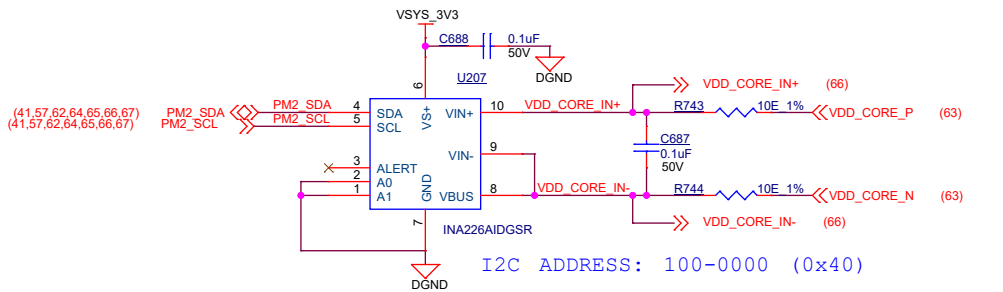
1. when low power modes are not needed:
 - 1. Add VDDSV3 CANUART to be supplied from load switch sourced VDD_3V3V3 all the time. Signals when SoC power control is in low power mode from pre-regulator VSYS_3V3 is desired. (Select this option by: Removing R78 and installing R77)
2. Supply all SoC VDDSV3Hv input supplies from pre-regulator's "always ON" VSYS_3V3 supply whenever SoC is to be fully powered up & active anytime VSYS_3V3 is energized to reduce PDN BOM co



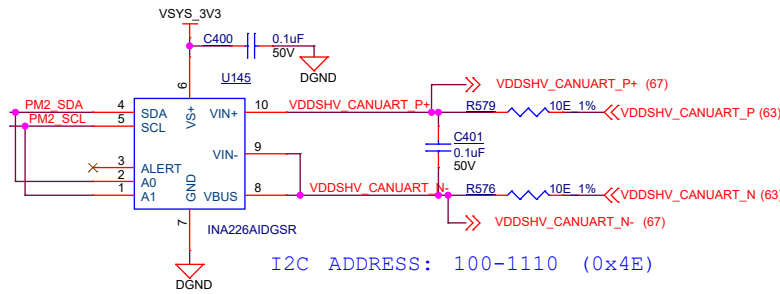
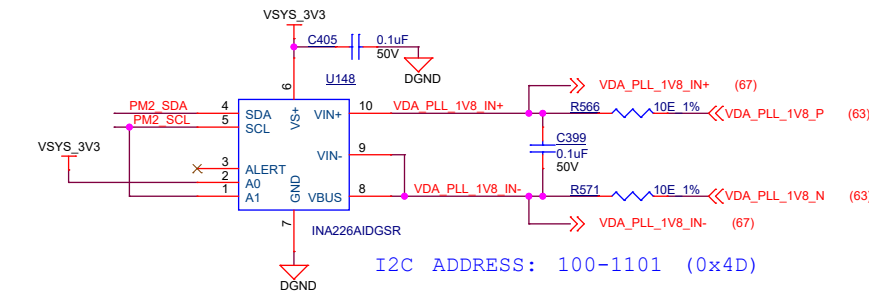
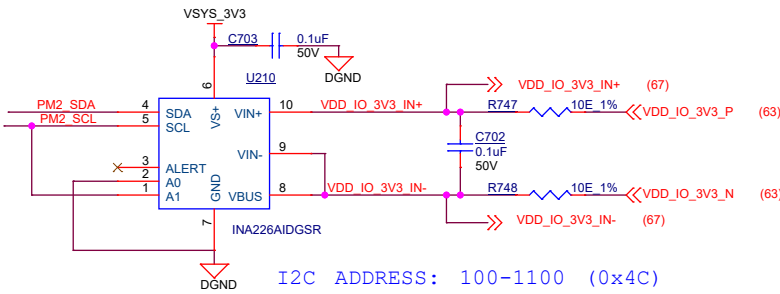
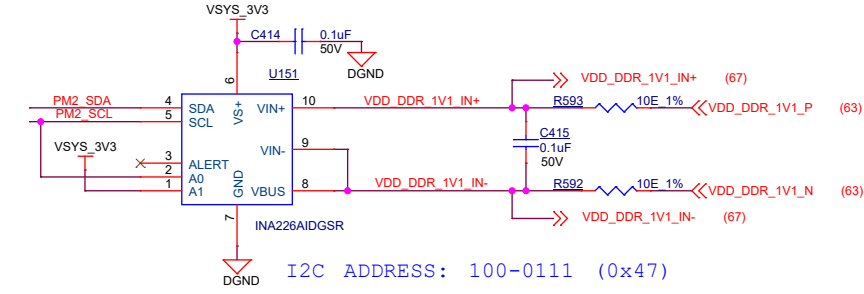
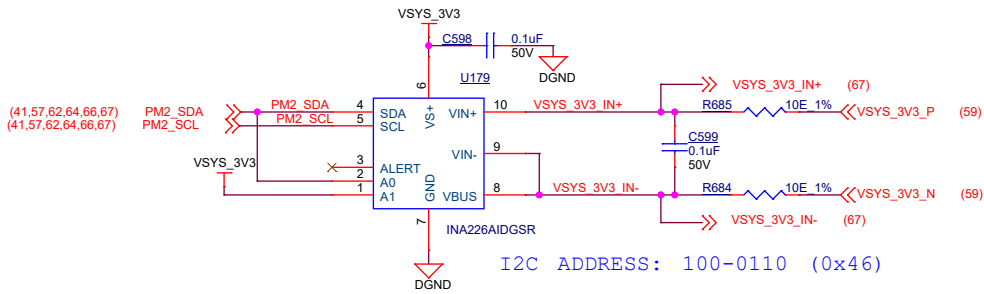
P2N adds default option to supply SoC's
 VDDA OSC/PLL/TEMP/MCU + VDDA_IP8 CSIDSI/OLD/SERDES/USB
 input supply
 groups from 2x independent PMIC LDOs via VDA PLL LV8 +
 VDA PHY LV8 power rails to avoid possible high-speed PH
 switching transient impacts to OSC/PLL/TEMP/MCU +
 VDDA_IP8 SoC clocks.
 An option to supply all SoC 1.8V analog supplies from a
 common 1.8V PMIC LDO power rail has been provisioned for
 future testing to min BOM cost + PCB area by enabling
 PDN/PMIC resource optimizations.



CURRENT MONITORS #1



CURRENT MONITORS #2



Project :

J7 EVM



Title
CURRENT MONITORS #2

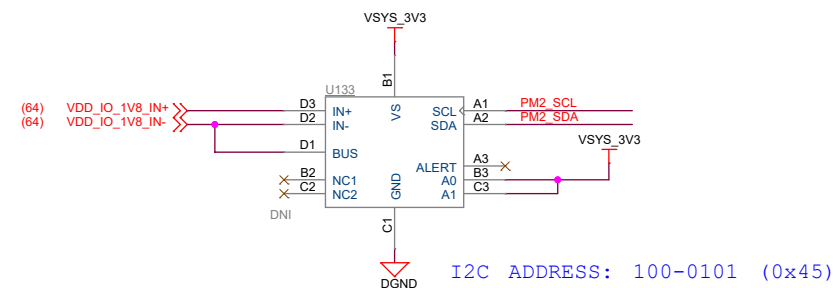
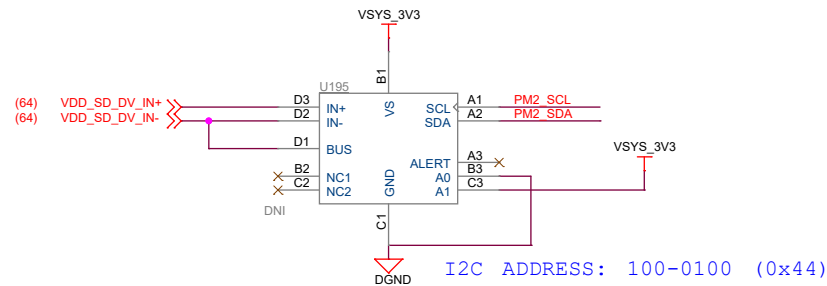
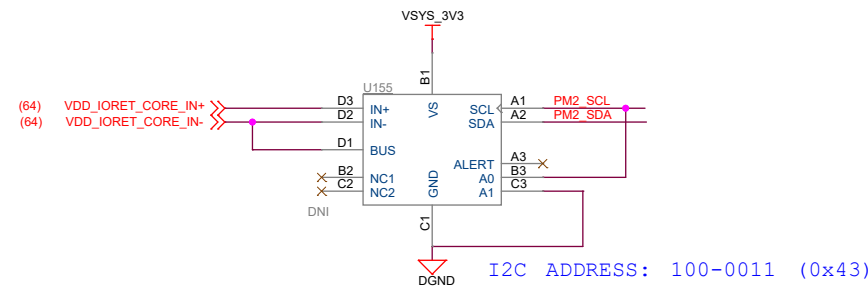
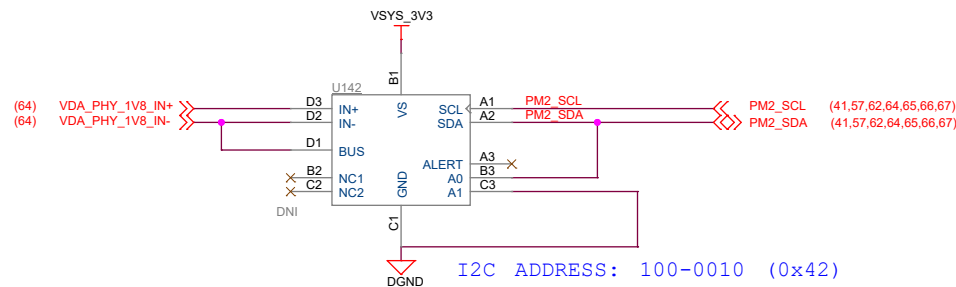
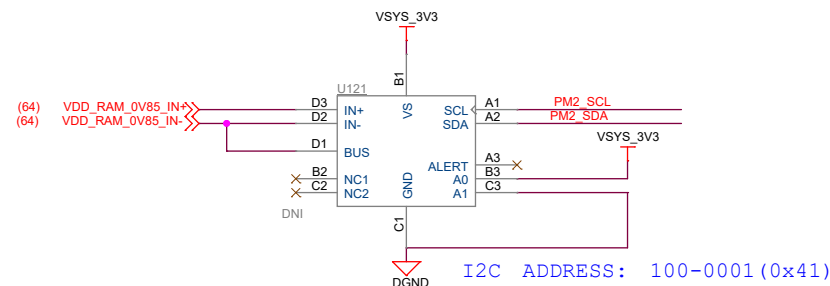
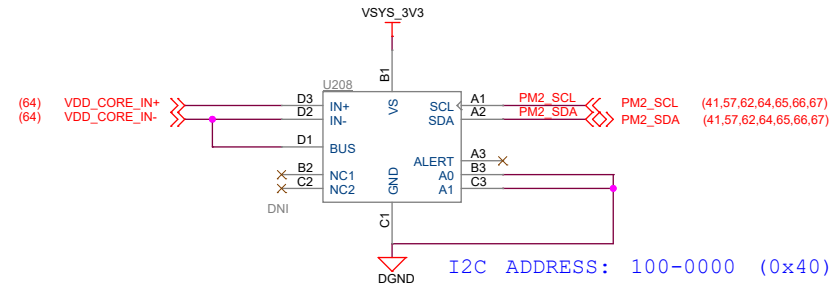
Size
C
PROC170 002 EVM

Date: Thursday, March 07, 2024

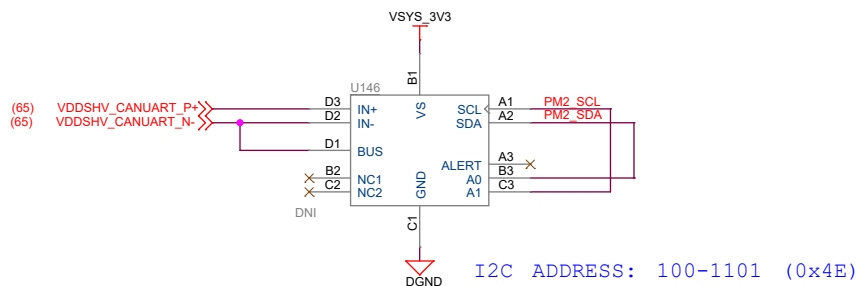
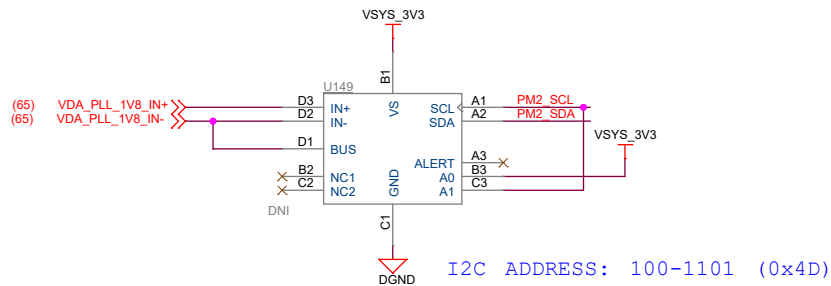
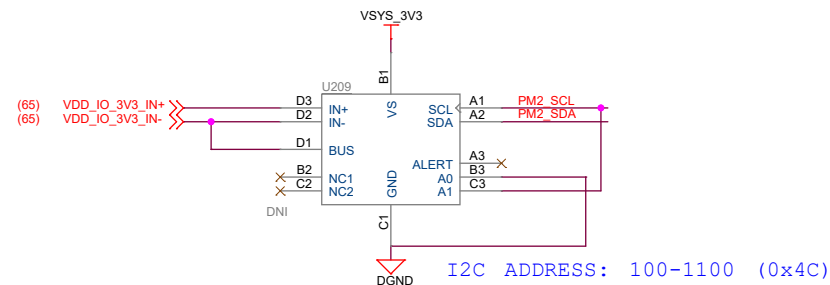
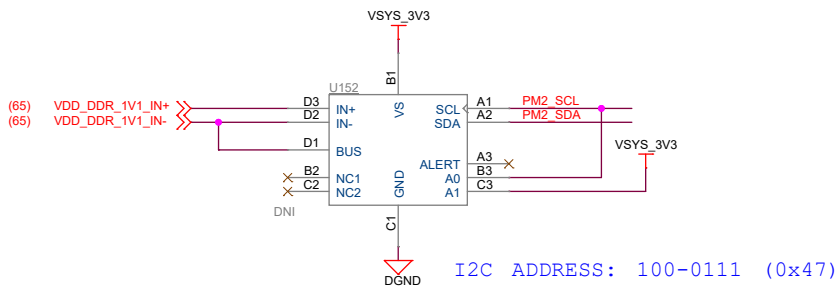
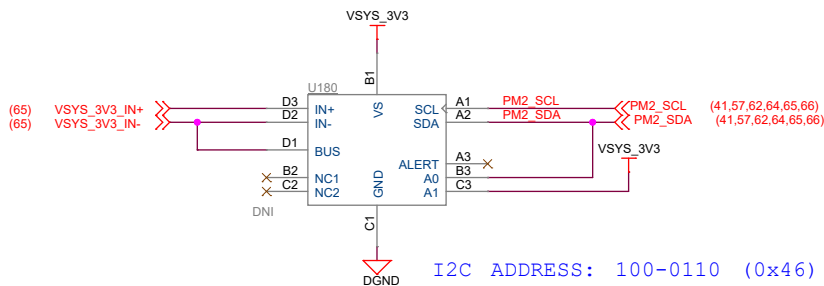
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Rev
E3

CURRENT MONITORS - INA231



CURRENT MONITORS - INA231



NOTES, HW & LABELS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABELS

Board Serial No.



AM6-COMPROCEVM

Assembly Revision.



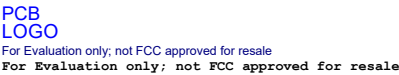
AM6-COMPROCEVM

EVM Orderable Part No.

Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J722SXG01EVM
002:Soldered HS SoC	J722SXH01EVM
003:Socketed SoC	J722SXS01EVM

LOGOs



SCREWS

MH1001



PAN HEAD_M2.5 X 8

MH1002



PAN HEAD_M2.5 X 8

MH1003



PAN HEAD_M2.5 X 8

MH1004



PAN HEAD_M2.5 X 8

MH1005



PAN HEAD_M2.5 X 8

MH1006



PAN HEAD_M2.5 X 8

MH1007



PAN HEAD_M2.5 X 8

STANDOFFS

MH1008



HEX SPACER_M2.5 X 12

MH1009



HEX SPACER_M2.5 X 12

MH1010



HEX SPACER_M2.5 X 12

MH1011



HEX SPACER_M2.5 X 12

MH1012



HEX SPACER_M2.5 X 12

MH1013



HEX SPACER_M2.5 X 12

MH1014



HEX SPACER_M2.5 X 12

WASHER

ACC1



PLAIN WASHER_M2.5

ACC2



PLAIN WASHER_M2.5

ACC3



PLAIN WASHER_M2.5

ACC4



PLAIN WASHER_M2.5

ACC5



PLAIN WASHER_M2.5

ACC6



PLAIN WASHER_M2.5

ACC7



PLAIN WASHER_M2.5

FIDUCIALS



FID1001
FID_40X80



FID1002
FID_40X80



FID1003
FID_40X80



FID1004
FID_40X80



FID1005
FID_40X80



FID1006
FID_40X80

BARE PCB

PCB1



PROC170E3

J722S TDA4VEN TDA4AEN
AM67 SOC

ACC16



DNI

SOCKET

ACC17



DNI

Project :

J7 EVM



Title
HARDWARE SCHEMATICS

Size
C
PROC170 002 EVM

Date: Monday, January 29, 2024

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Rev
E3