SDLS086 – DECEMBER 1983 – REVISED MARCH 1988

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage**
- **Asynchronous Parallel Clear**
- **Active High Decoder**
- **Enable/Disable Input Simplified Expansion**
- **Expandable for N-Bit Applications**
- **Four District Functional Modes**
- **Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

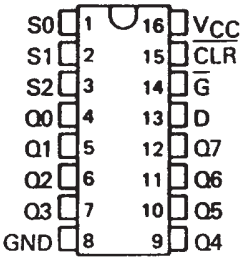
description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

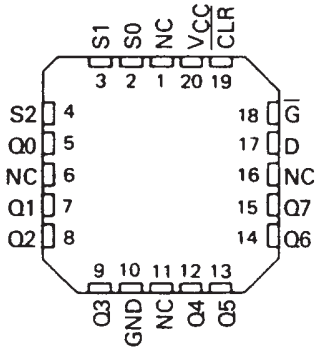
Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possiblity of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54259 and SN54LS259B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74259 and SN74LS259B are characterized for operation from 0°C to 70°C.

SN54259, SN54LS259B . . . J OR W PACKAGE
SN74259 . . . N PACKAGE
SN74LS259B . . . D OR N PACKAGE
(TOP VIEW)

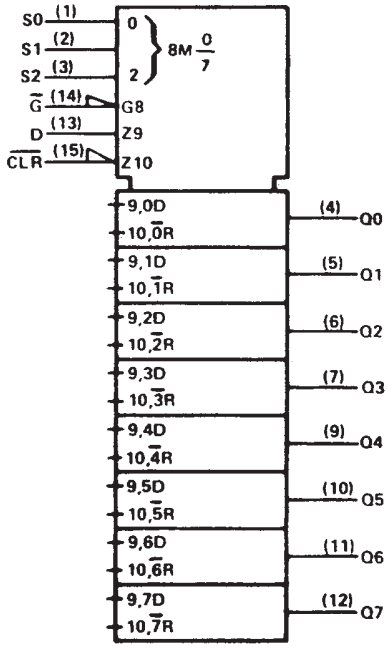


SN54LS259B . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLR}$	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

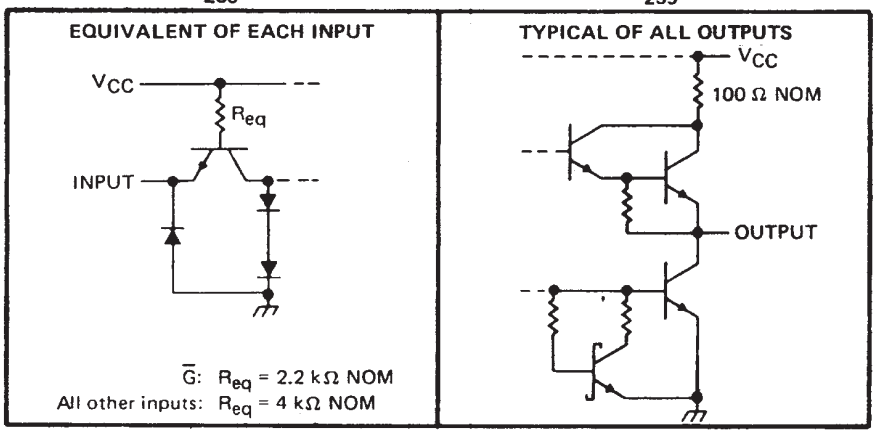
H ≡ high level, L ≡ low level
D ≡ the level at the data input
Q_{i0} ≡ the level of Q_i (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

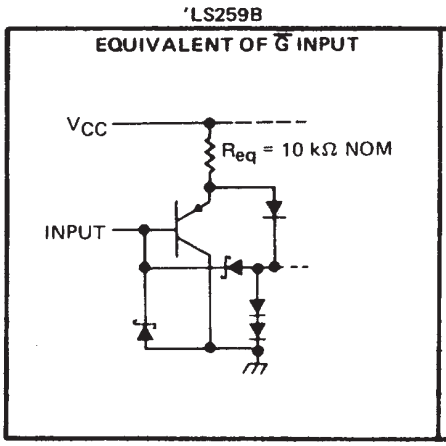
schematic of inputs and outputs

'259

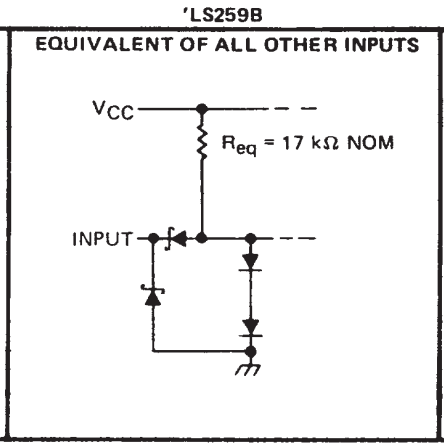


'259

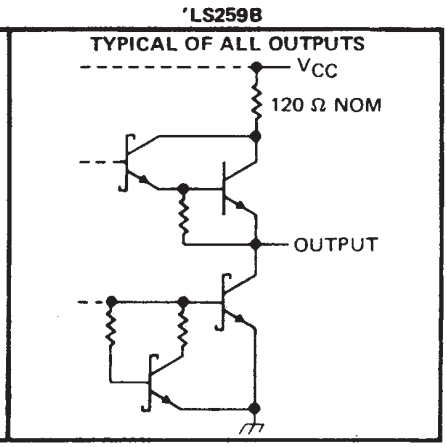
'LS259B



'LS259B



'LS259B



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage: SN54259, SN74259 . . . . . 5.5 V
SN54LS259B, SN74LS259B . . . . . 7 V
Operating free-air temperature range: SN54259, SN54LS259B . . . . . −55°C to 125°C
SN74259, SN74LS259B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54259			SN74259			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–800			–800	μA
Low-level output current, I_{OL}				16			16	mA
Width of clear or enable pulse, t_w		15			15			ns
Setup time, t_{su}	Data	15↑			15↑			ns
	Address	5↑			5↑			
Hold time, t_h	Data	0↑			0↑			ns
	Address	20↑			20↑			
Operating free-air temperature, T_A		–55		125	0		70	°C

†The arrow indicates that the rising edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54259			SN74259			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = 12 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = –800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	$\overline{G}$	V_{CC} = MAX,	V_I = 2.4 V			80			80	μA
		Other inputs					40			40	
I_{IL}	Low-level input current	$\overline{G}$	V_{CC} = MAX,	V_I = 0.4 V			–3.2			–3.2	mA
		Other inputs					–1.6			–1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		–18		–57	–18		–57	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		60	90		60	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 15 pF, R_L = 400 Ω, See Note 3		16	25	ns
t_{PLH}	Data	Any Q			14	24	ns
t_{PHL}					11	20	
t_{PLH}	Address	Any Q			15	28	ns
t_{PHL}					17	28	
t_{PLH}	$\overline{G}$	Any Q			12	20	ns
t_{PHL}					11	20	

t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54LS259B			SN74LS259B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
t_w	Pulse duration	$\overline{G}$ low	17			17			ns
		$\overline{CLR}$ low	10			10			
t_{su}	Set up time	Data before $\overline{G}\uparrow$	20			20			ns
		Address before $\overline{G}\uparrow$	17			17			
		Address before $\overline{G}\downarrow$	0			0			
t_h	Hold time	Data after $\overline{G}\uparrow$	0			0			ns
		Address after $\overline{G}\uparrow$	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS259B			SN74LS259B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	V_{CC} = MAX, See Note 2			27	36		22	36	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Note 3		12	18	ns
t_{PLH}	Data	Any Q			19	30	ns
t_{PHL}					13	20	
t_{PLH}	Address	Any Q			17	27	ns
t_{PHL}					14	20	
t_{PLH}	$\overline{G}$	Any Q			15	24	ns
t_{PHL}					15	24	

t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS259BD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	LS259B
SN74LS259BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS259B
SN74LS259BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS259B
SN74LS259BN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS259BN
SN74LS259BN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS259BN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

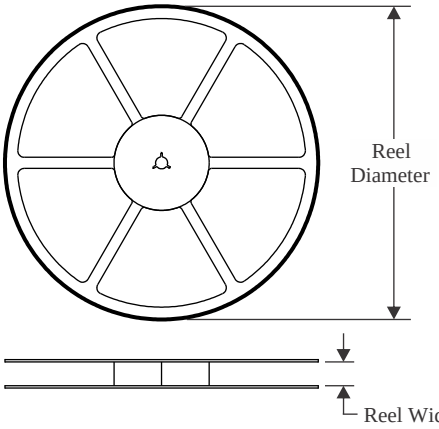
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

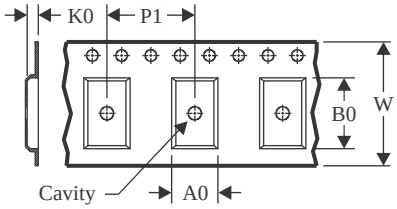
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

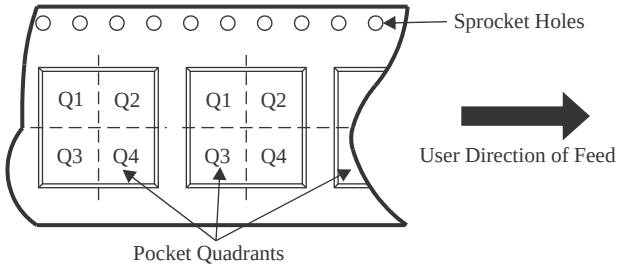


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

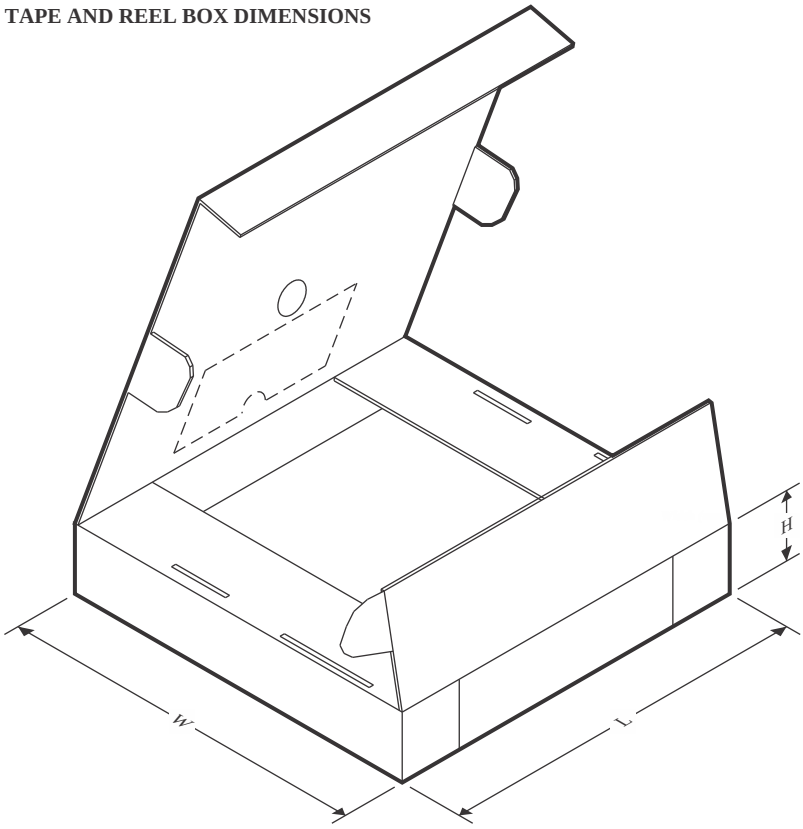
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS259BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

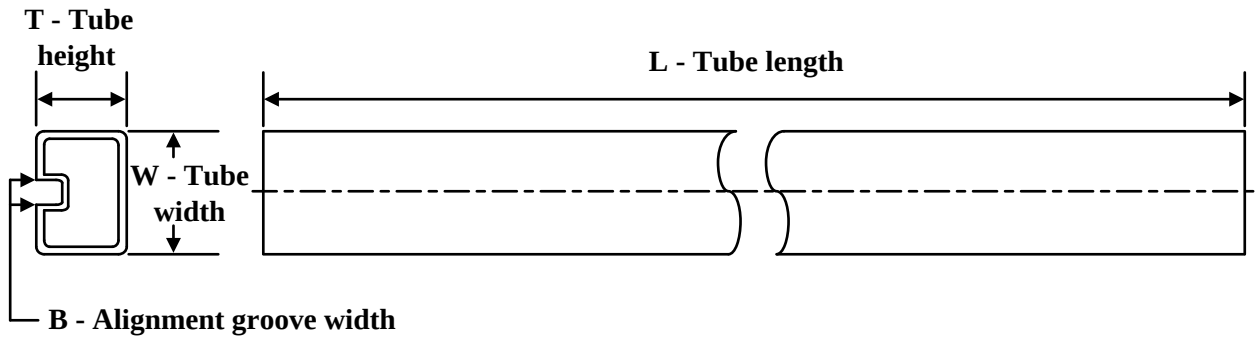
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS259BDR	SOIC	D	16	2500	353.0	353.0	32.0

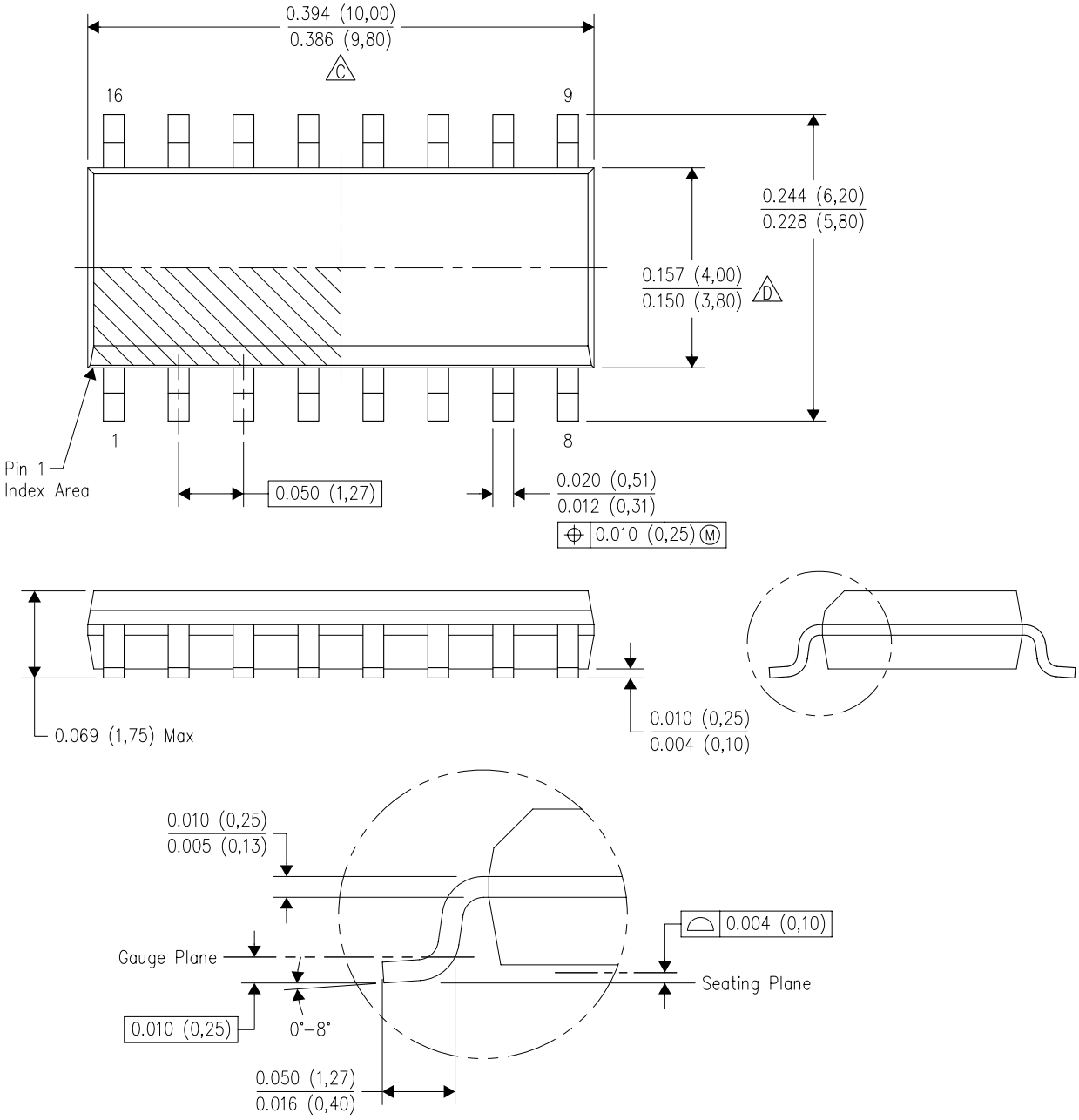
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS259BN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS259BN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS259BN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS259BN.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

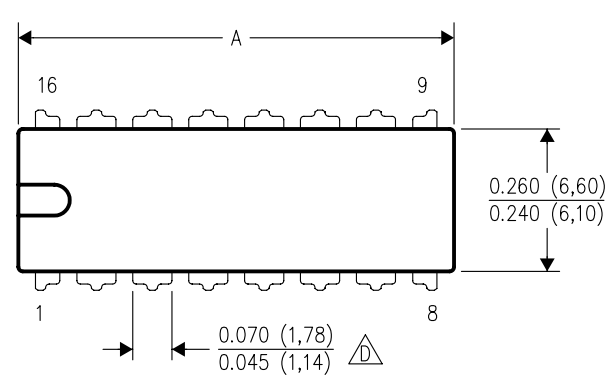


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

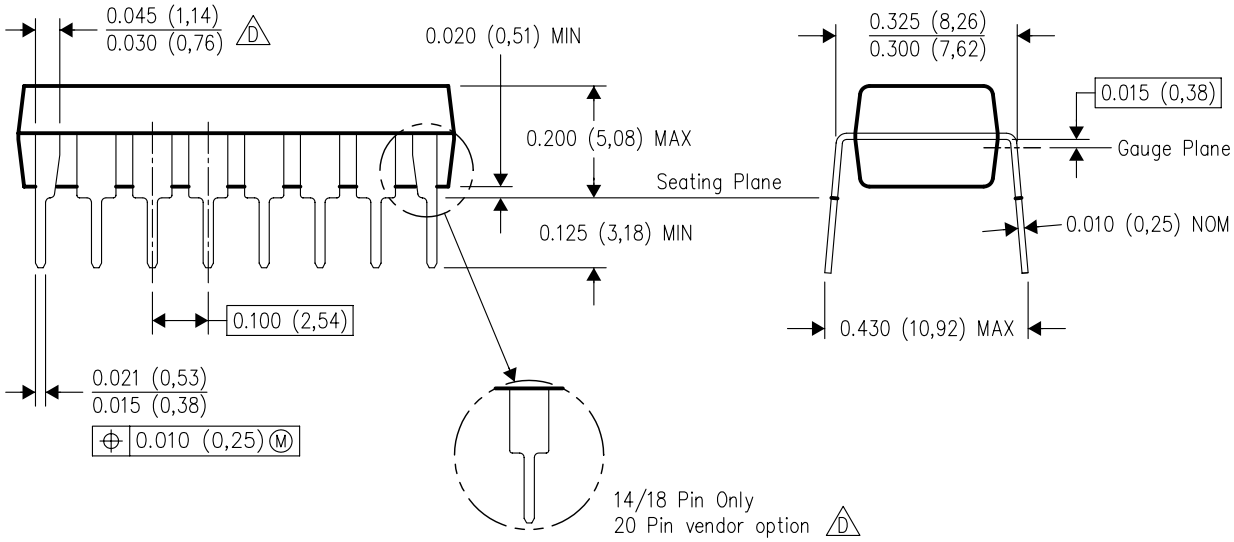
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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