

- Output Swing includes Both Supply Rails
- Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Low Power . . . 500 μA Max
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage  
950 μV Max at T<sub>A</sub> = 25°C (TLC2262A)
- Macromodel Included
- Performance Upgrade for the TS27M2/M4 and TLC27M2/M4
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards

## description

The TLC2262 and TLC2264 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC226x family offers a compromise between the micropower TLC225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

The TLC226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC226xA family is available and has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2262/4 also makes great upgrades to the TLC27M2/L4 or TS27M2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

EQUIVALENT INPUT NOISE VOLTAGE  
vs  
FREQUENCY

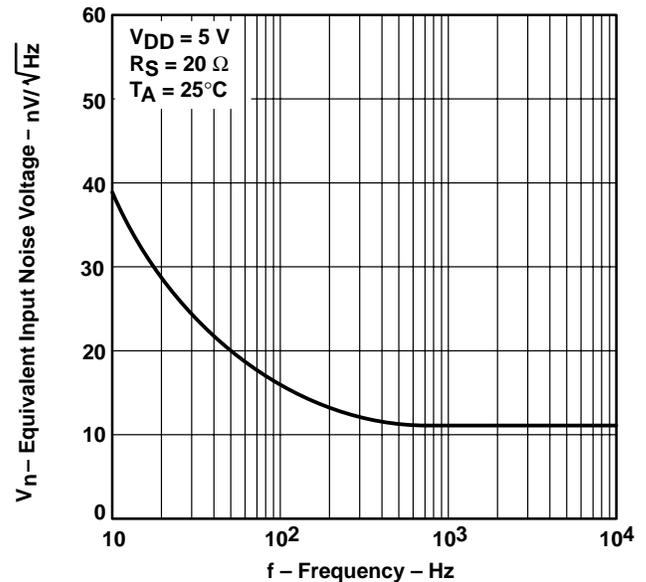


Figure 1



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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## TLC2262 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	2.5 mV	TLC2262CD	—	—	TLC2262CP	TLC2262CPW	—
–40°C to 125°C	950 μV 2.5 mV	TLC2262AID TLC2262ID	— —	— —	TLC2262AIP TLC2262IP	TLC2262AIPW —	— —
–40°C to 125°C	950 μV 2.5 mV	TLC2262AQD TLC2262QD	— —	— —	— —	— —	— —
–55°C to 125°C	950 μV 2.5 mV	— —	TLC2262AMFK TLC2262MFK	TLC2262AMJG TLC2262MJG	— —	— —	TLC2262AMU TLC2262MU

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

## TLC2264 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)
0°C to 70°C	2.5 mV	TLC2264CD	—	—	TLC2264CN	TLC2264CPW	—
–40°C to 125°C	950 μV 2.5 mV	TLC2264AID TLC2264ID	— —	— —	TLC2264AIN TLC2264IN	TLC2264AIPW —	— —
–40°C to 125°C	950 μV 2.5 mV	TLC2264AQD TLC2264QD	— —	— —	— —	— —	— —
–55°C to 125°C	950 μV 2.5 mV	— —	TLC2264AMFK TLC2264MFK	TLC2264AMJ TLC2264MJ	— —	— —	TLC2264AMW TLC2264MW

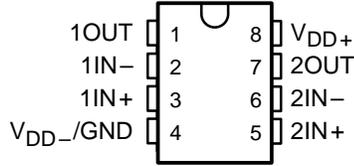
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2264CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.



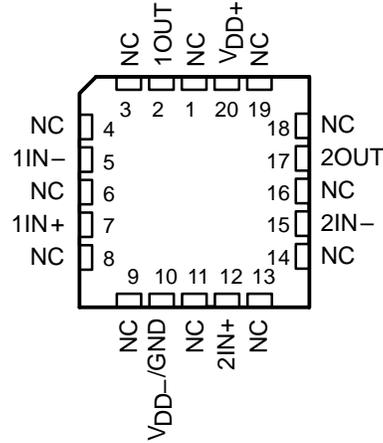
# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2262C, TLC2262AC  
TLC2262I, TLC2262AI  
TLC2262Q, TLC2262AQ  
D, P, OR PW PACKAGE  
(TOP VIEW)**

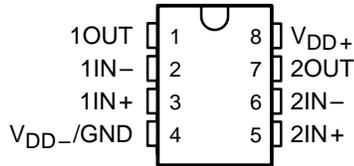


**TLC2262M, TLC2262AM ... FK PACKAGE  
(TOP VIEW)**

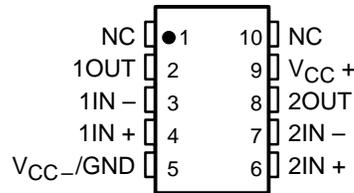


NC – No internal connection

**TLC2262M, TLC2262AM ... JG PACKAGE  
(TOP VIEW)**

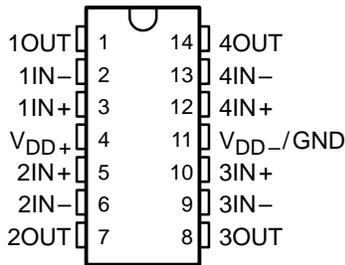


**TLC2262M, TLC2262AM ... U PACKAGE  
(TOP VIEW)**

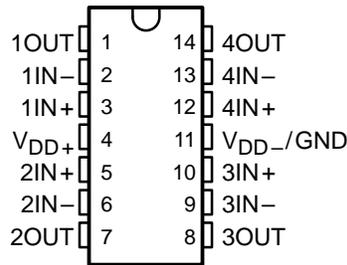


NC – No internal connection

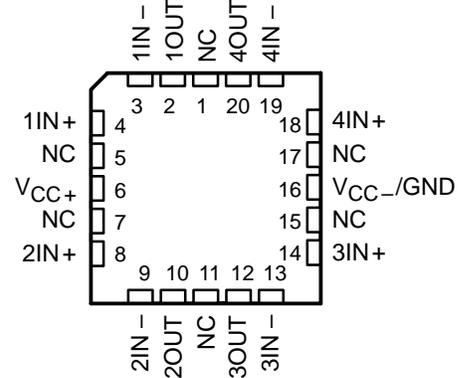
**TLC2264C, TLC2264AC  
TLC2264I, TLC2264AI  
TLC2264Q, TLC2264AQ  
D, N, OR PW PACKAGE  
(TOP VIEW)**



**TLC2264M, TLC2264AM ... J OR W PACKAGE  
(TOP VIEW)**



**TLC2264M, TLC2264AM ... FK PACKAGE  
(TOP VIEW)**

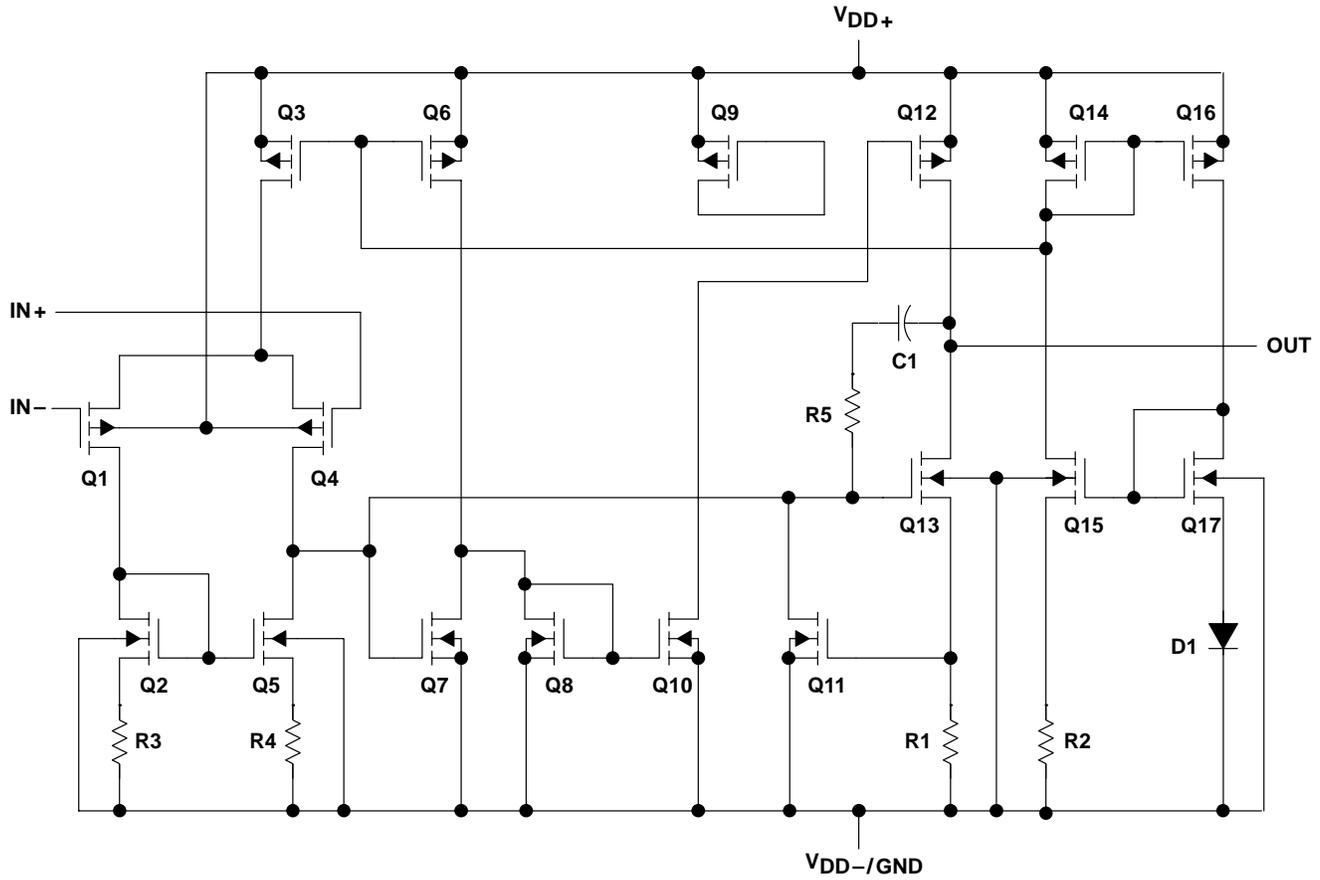


NC – No internal connection

**TLC226x, TLC226xA**  
**Advanced LinCMOS™ RAIL-TO-RAIL**  
**OPERATIONAL AMPLIFIERS**

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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2262	TLC2264
Transistors	38	76
Resistors	28	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{DD+}$ (see Note 1)	8 V
Supply voltage, $V_{DD-}$ (see Note 1)	–8 V
Differential input voltage, $V_{ID}$ (see Note 2)	±16 V
Input voltage, $V_I$ (any input, see Note 1)	$V_{DD-} - 0.3$ V to $V_{DD+}$
Input current, $I_I$ (each input)	±5 mA
Output current, $I_O$	±50 mA
Total current into $V_{DD+}$	±50 mA
Total current out of $V_{DD-}$	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, and PW packages	260°C
J, JG, U, and W packages	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{DD+}$  and  $V_{DD-}$ .  
2. Differential voltages are at  $IN+$  with respect to  $IN-$ . Excessive current flows if input is brought below  $V_{DD-} - 0.3$  V.  
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW–14	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

**recommended operating conditions**

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, $V_I$	$V_{DD-}$	$V_{DD+} - 1.5$	V						
Common-mode input voltage, $V_{IC}$	$V_{DD-}$	$V_{DD+} - 1.5$	V						
Operating free-air temperature, $T_A$	0	70	–40	125	–40	125	–55	125	°C

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2262C electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262C			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	300	2500	$\mu\text{V}$	
		Full range	3000			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5		$\text{pA}$	
		Full range	100			
$I_{IB}$ Input bias current	25°C	1		$\text{pA}$		
	Full range	100				
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO}  \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2	$\text{V}$	
		Full range	0 to 3.5			
$V_{OH}$ High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.99		$\text{V}$	
	$I_{OH} = -100\ \mu\text{A}$	25°C	4.85	4.94		
		Full range	4.82			
	$I_{OH} = -400\ \mu\text{A}$	25°C	4.70	4.85		
Full range		4.60				
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$	25°C	0.01		$\text{V}$	
		25°C	0.09	0.15		
	Full range	0.15				
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 1\text{ mA}$	25°C	0.2	0.3		
		Full range	0.3			
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 4\text{ mA}$	25°C	0.7	1		
		Full range	1.2			
	$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 50\ \text{k}\Omega^\ddagger$	25°C		80
Full range				55		
$R_L = 1\ \text{M}\Omega^\ddagger$			25°C	550		
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$		$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$		$\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz},$ P package	25°C	8		$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz},$ $A_V = 10$	25°C	240		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83	$\text{dB}$	
		Full range	70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95	$\text{dB}$	
		Full range	80			
$I_{DD}$ Supply current	$V_O = 2.5\text{ V},$ No load	25°C	400	500	$\mu\text{A}$	
		Full range	500			

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2262C operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER		TEST CONDITIONS		$T_A$ †	TLC2262C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V},$ $C_L = 100\text{ pF}‡$	$R_L = 50\text{ k}\Omega‡$	25°C	0.35	0.55	V/ $\mu$ s	
				Full range	0.3			
$V_n$	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C	40		nV/ $\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$		25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C	0.7		$\mu$ V	
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C	1.3			
$I_n$	Equivalent input noise current			25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 20\text{ kHz},$ $R_L = 50\text{ k}\Omega‡$	$A_V = 1$	25°C	0.017%			
			$A_V = 10$		0.03%			
Gain-bandwidth product		$f = 10\text{ kHz},$ $C_L = 100\text{ pF}‡$	$R_L = 50\text{ k}\Omega‡$	25°C	0.71		MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 50\text{ k}\Omega‡$	$A_V = 1,$ $C_L = 100\text{ pF}‡$	25°C	185		kHz	
$t_s$	Settling time	$A_V = -1,$ Step = 0.5 V to 2.5 V, $R_L = 50\text{ k}\Omega‡,$ $C_L = 100\text{ pF}‡$	To 0.1%	25°C	6.4		$\mu$ s	
			To 0.01%		14.1			
$\phi_m$	Phase margin at unity gain	$R_L = 50\text{ k}\Omega‡,$	$C_L = 100\text{ pF}‡$	25°C	56°			
	Gain margin			25°C	11		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

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**TLC2262C electrical characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$  (unless otherwise specified)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262C			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C		300	2500	$\mu\text{V}$
		Full range			3000	
$\alpha V_{IO}$ Temperature coefficient of input offset voltage		25°C to 70°C		2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C		0.5		$\text{pA}$
		Full range			100	
$I_{IB}$ Input bias current		25°C		1		$\text{pA}$
		Full range			100	
$V_{ICR}$ Common-mode input voltage range		$ V_{IO}  \leq 5\text{ mV}, R_S = 50\ \Omega$	25°C	-5 to 4	-5.3 to 4.2	$\text{V}$
			Full range	-5 to 3.5		
$V_{OM+}$ Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.99	$\text{V}$	
	$I_O = -100\ \mu\text{A}$	25°C	4.85	4.94		
	$I_O = -400\ \mu\text{A}$	Full range	4.82			
		25°C	4.7	4.85		
$V_{OM-}$ Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C		-4.99	$\text{V}$	
		25°C	-4.85	-4.91		
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	Full range	-4.85			
		25°C	-4.7	-4.8		
	$V_{IC} = 0, I_O = 1\ \text{mA}$	Full range	-4.7			
		25°C	-4	-4.3		
	$V_{IC} = 0, I_O = 4\ \text{mA}$	Full range	-3.8			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200	$\text{V}/\text{mV}$
			Full range	55		
		$R_L = 1\ \text{M}\Omega$	25°C		1000	
$r_{i(d)}$ Differential input resistance		25°C		$10^{12}$	$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C		$10^{12}$	$\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{ P package}$	25°C		8	$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz}, A_V = 10$	25°C		220	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0\ \text{V}, R_S = 50\ \Omega$	25°C	75	88	$\text{dB}$	
		Full range	75			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD\pm} / \Delta V_{IO}$ )	$V_{DD\pm} = 2.2\ \text{V to } \pm 8\ \text{V}, V_{IC} = 0, \text{ No load}$	25°C	80	95	$\text{dB}$	
		Full range	80			
$I_{DD}$ Supply current	$V_O = 0\ \text{V}, \text{ No load}$	25°C	425	500	$\mu\text{A}$	
		Full range		500		

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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**TLC2262C operating characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER		TEST CONDITIONS		$T_A$ †	TLC2262C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.35	0.55	$\text{V}/\mu\text{s}$	
				Full range	0.3			
$V_n$	Equivalent input noise voltage			25°C	43		$\text{nV}/\sqrt{\text{Hz}}$	
				25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.8		$\mu\text{V}$	
				25°C	1.3			
$I_n$	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion pulse duration	$V_O = \pm 2.3\text{ V}$ , $f = 20\text{ kHz}$ , $R_L = 50\text{ k}\Omega$		25°C	$A_V = 1$	0.014%		
					$A_V = 10$	0.024%		
Gain-bandwidth product		$f = 10\text{ kHz}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.73		MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $R_L = 50\text{ k}\Omega$ ,	$A_V = 1$ , $C_L = 100\text{ pF}$	25°C	85		kHz	
$t_s$	Settling time	$A_V = -1$ , Step = $-2.3\text{ V}$ to $2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$		25°C	To 0.1%	7.1		$\mu\text{s}$
					To 0.01%	16.5		
$\phi_m$	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ,	$C_L = 100\text{ pF}$	25°C	57°			
	Gain margin			25°C	11			dB

† Full range is 0°C to 70°C.

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2264C electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264C			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD\pm} = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	300	2500	$\mu\text{V}$	
		Full range	3000			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5		$\text{pA}$	
		Full range	100			
$I_{IB}$ Input bias current	25°C	1		$\text{pA}$		
	Full range	100				
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO}  \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2	$\text{V}$	
		Full range	0 to 3.5			
$V_{OH}$ High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	25°C	4.99		$\text{V}$	
		25°C	4.85	4.94		
		Full range	4.82			
		25°C	4.70	4.85		
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$ $I_{OL} = 500\ \mu\text{A}$ $I_{OL} = 1\text{ mA}$ $I_{OL} = 4\text{ mA}$	25°C	0.01		$\text{V}$	
		25°C	0.09	0.15		
		Full range	0.15			
		25°C	0.2	0.3		
		Full range	0.3			
		25°C	0.7	1		
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	25°C	$R_L = 50\ \text{k}\Omega\ddagger$	80	170	$\text{V}/\text{mV}$
			Full range	55		
		25°C	$R_L = 1\ \text{M}\Omega\ddagger$	550		
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$		$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$		$\Omega$	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz},$ N package	25°C	8		$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$	25°C	240		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83	$\text{dB}$	
		Full range	70			
kSVR Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95	$\text{dB}$	
		Full range	80			
$I_{DD}$ Supply current (four amplifiers)	$V_O = 2.5\text{ V},$ No load	25°C	0.8	1	$\text{mA}$	
		Full range	1			

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4. Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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**TLC2264C operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER		TEST CONDITIONS		$T_A$ †	TLC2264C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.4\text{ V to }2.6\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$		25°C	0.35	0.55	V/ $\mu\text{s}$	
				Full range	0.3			
$V_n$	Equivalent input noise voltage			25°C	40		nV/ $\sqrt{\text{Hz}}$	
				25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.7		$\mu\text{V}$	
				25°C	1.3			
$I_n$	Equivalent input noise current			25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}, f = 20\text{ kHz}, R_L = 50\text{ k}\Omega^\ddagger$		25°C	$A_V = 1$	0.017%		
					$A_V = 10$	0.03%		
Gain-bandwidth product		$f = 10\text{ kHz}, C_L = 100\text{ pF}^\ddagger$		25°C	0.71		MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}, R_L = 50\text{ k}\Omega^\ddagger,$		25°C	185		kHz	
$t_s$	Settling time	$A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$		25°C	To 0.1%	6.4	$\mu\text{s}$	
					To 0.01%	14.1		
$\phi_m$	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$		25°C	56°			
	Gain margin			25°C	11		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

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**TLC2264C electrical characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$  (unless otherwise specified)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC2264C			UNIT
			MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω, V <sub>O</sub> = 0,	25°C	300	2500	μV	
		Full range	3000			
α <sub>VIO</sub> Temperature coefficient of input offset voltage		25°C to 70°C	2		μV/°C	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		μV/mo	
I <sub>IO</sub> Input offset current		25°C	0.5		pA	
		Full range	100			
I <sub>IB</sub> Input bias current		25°C	1		pA	
		Full range	100			
V <sub>ICR</sub> Common-mode input voltage range	V <sub>IO</sub>   ≤ 5 mV, R <sub>S</sub> = 50 Ω	25°C	-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			
V <sub>OM+</sub> Maximum positive peak output voltage	I <sub>O</sub> = -20 μA	25°C	4.99		V	
	I <sub>O</sub> = -100 μA	25°C	4.85	4.94		
		Full range	4.82			
	I <sub>O</sub> = -400 μA	25°C	4.7	4.85		
Full range		4.6				
V <sub>OM-</sub> Maximum negative peak output voltage	V <sub>IC</sub> = 0, I <sub>O</sub> = 50 μA	25°C	-4.99		V	
		25°C	-4.85	-4.91		
	V <sub>IC</sub> = 0, I <sub>O</sub> = 500 μA	Full range	-4.85			
		25°C	-4.7	-4.8		
	V <sub>IC</sub> = 0, I <sub>O</sub> = 1 mA	Full range	-4.7			
		25°C	-4	-4.3		
V <sub>IC</sub> = 0, I <sub>O</sub> = 4 mA	Full range	-3.8				
	A <sub>VD</sub> Large-signal differential voltage amplification	V <sub>O</sub> = ±4 V	R <sub>L</sub> = 50 kΩ	25°C	80	200
Full range				55		
R <sub>L</sub> = 1 MΩ			25°C	1000		
r <sub>i(d)</sub> Differential input resistance		25°C	10 <sup>12</sup>		Ω	
r <sub>i(c)</sub> Common-mode input resistance		25°C	10 <sup>12</sup>		Ω	
c <sub>i(c)</sub> Common-mode input capacitance	f = 10 kHz, N package	25°C	8		pF	
z <sub>o</sub> Closed-loop output impedance	f = 100 kHz, A <sub>V</sub> = 10	25°C	220		Ω	
CMRR Common-mode rejection ratio	V <sub>IC</sub> = -5 V to 2.7 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	75	88	dB	
		Full range	75			
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>DD±</sub> /ΔV <sub>IO</sub> )	V <sub>DD±</sub> = ±2.2 V to ±8 V, V <sub>IC</sub> = 0, No load	25°C	80	95	dB	
		Full range	80			
I <sub>DD</sub> Supply current (four amplifiers)	V <sub>O</sub> = 0, No load	25°C	0.85	1	mA	
		Full range	1			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2264C operating characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER		TEST CONDITIONS		$T_A$ †	TLC2264C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.35	0.55	$\text{V}/\mu\text{s}$	
				Full range	0.3			
$V_n$	Equivalent input noise voltage			25°C	43		$\text{nV}/\sqrt{\text{Hz}}$	
				25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.8		$\mu\text{V}$	
				25°C	1.3			
$I_n$	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$ , $f = 20\text{ kHz}$ , $R_L = 50\text{ k}\Omega$		25°C	$A_V = 1$	0.014%		
					$A_V = 10$	0.024%		
Gain-bandwidth product		$f = 10\text{ kHz}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.73		MHz	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $R_L = 50\text{ k}\Omega$	$A_V = 1$ , $C_L = 100\text{ pF}$	25°C	70		kHz	
$t_s$	Settling time	$A_V = -1$ , Step = $-2.3\text{ V}$ to $2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$		25°C	To 0.1%	7.1		
					To 0.01%	16.5		
$\phi_m$	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	57°			
	Gain margin			25°C	11			

† Full range is 0°C to 70°C.

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2262I electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262I			TLC2262AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0$ , $V_{IC} = 0$ , $R_S = 50\ \Omega$	25°C	300	2500		300	950		$\mu\text{V}$
		Full range			3000		1500		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 85°C		2			2		$\mu\text{V}/^\circ\text{C}$
		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C		0.5			0.5		$\text{pA}$
		85°C			150		150		
		Full range			800		800		$\text{pA}$
$I_{IB}$ Input bias current		25°C		1			1		$\text{pA}$
	85°C			150		150		$\text{pA}$	
	Full range			800		800		$\text{pA}$	
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		$\text{V}$
		Full range	0 to 3.5			0 to 3.5			
$V_{OH}$ High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	25°C		4.99			4.99		$\text{V}$
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V}$ , $I_{OL} = 50\ \mu\text{A}$ $I_{OL} = 500\ \mu\text{A}$ $I_{OL} = 4\text{ mA}$	25°C		0.01			0.01		$\text{V}$
		25°C		0.09	0.15		0.09	0.15	
		Full range			0.15			0.15	
		25°C		0.8	1		0.7	1	
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to } 4\text{ V}$	$R_L = 50\ \text{k}\Omega$ ‡	25°C	80	100		80	170	$\text{V}/\text{mV}$
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$ ‡	25°C		550			550	
$r_{i(d)}$ Differential input resistance		25°C		$10^{12}$			$10^{12}$	$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C		$10^{12}$			$10^{12}$	$\Omega$	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}$ , P package	25°C		8			8	$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz}$ , $A_V = 10$	25°C		240			240	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V}$ , $V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$	25°C	70	83		70	83	$\text{dB}$	
		Full range	70			70			

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2262I operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262I			TLC2262AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
$k_{SVR}$	Supply-voltage re- jection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }16\text{ V}$ , $V_{IC} = V_{DD}/2$ , No load	25°C	80	95		80	95	dB	
			Full range	80			80			
$I_{DD}$	Supply current	$V_O = 2.5\text{ V}$ , No load	25°C		400	500		400	500	$\mu\text{A}$
			Full range			500			500	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}$ , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.35	0.55		0.35	0.55	$\text{V}/\mu\text{s}$	
			Full range	0.25			0.25			
$V_n$	Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		40			40	$\text{nV}/\sqrt{\text{Hz}}$	
			25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		0.7			0.7	$\mu\text{V}$	
			25°C		1.3			1.3		
$I_n$	Equivalent input noise current		25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$ , $f = 20\text{ kHz}$ , $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	25°C	0.017%		0.017%			
			$A_V = 10$		0.03%		0.03%			
	Gain-bandwidth product	$f = 50\text{ kHz}$ , $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡,	25°C	0.82		0.82		MHz	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$ , $R_L = 50\text{ k}\Omega$ ‡,	$A_V = 1$ , $C_L = 100\text{ pF}$ ‡	25°C	185		185		kHz	
$t_s$	Settling time	$A_V = -1$ , Step = $0.5\text{ V to }2.5\text{ V}$ , $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	To 0.1%	25°C	6.4		6.4		$\mu\text{s}$	
			To 0.01%		14.1		14.1			
$\phi_m$	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C	56°		56°			
	Gain margin			25°C	11		11			dB

† Full range is  $-40^\circ\text{C to }125^\circ\text{C}$ .

‡ Referenced to 2.5 V

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2262I electrical characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262I			TLC2262AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, V_O = 0$ $R_S = 50\ \Omega$	25°C	300	2500		300	950	$\mu\text{V}$	
		Full range			3000		1500		
$\alpha V_{IO}$ Temperature coefficient of input offset voltage		25°C to 85°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5			0.5		pA	
		85°C			150		150	pA	
		Full range			800		800	pA	
$I_{IB}$ Input bias current		25°C	1			1		pA	
	85°C			150		150	pA		
	Full range			800		800	pA		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega,  V_{IO}  \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
$V_{OM+}$ Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99			4.99		V	
		25°C	4.85	4.94		4.85	4.94		
	Full range	4.82			4.82				
	$I_O = -400\ \mu\text{A}$	25°C	4.7	4.85		4.7	4.85		
Full range		4.5			4.5				
$V_{OM-}$ Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99	V	
		25°C	-4.85	-4.91		-4.85	-4.91		
	Full range	-4.85			-4.85				
	$V_{IC} = 0, I_O = 4\ \text{mA}$	25°C	-4	-4.3		-4	-4.3		
Full range		-3.8			-3.8				
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200		80	200	V/mV
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$	25°C		1000			1000	
$r_{i(d)}$ Differential input resistance		25°C		1012			1012	$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C		1012			1012	$\Omega$	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{ P package}$	25°C		8			8	pF	
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz}, A_V = 10$	25°C		220			220	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD\pm} / \Delta V_{IO}$ )	$V_{DD} = 4.4\ \text{V to } 16\ \text{V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95	dB	
		Full range	80			80			

† Full range is -40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2262I operating characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262I			TLC2262AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{DD}$ Supply Current	$V_O = 2.5\text{ V}$ , No load	25°C	425	500		425	500		
		Full range		500			500		
SR Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 50\text{ k}\Omega$	25°C	0.35	0.55		0.35	0.55	V/ $\mu\text{s}$	
		Full range	0.25			0.25			
$V_n$ Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		43			43	nV/ $\sqrt{\text{Hz}}$	
		25°C		12			12		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		0.8			0.8	$\mu\text{V}$	
		25°C		1.3			1.3		
$I_n$ Equivalent input noise current		25°C		0.6			0.6	fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $f = 20\text{ kHz}$	25°C		$A_V = 1$		0.014%		0.014%	
				$A_V = 10$		0.024%		0.024%	
Gain-bandwidth product	$f = 10\text{ kHz}$ , $C_L = 100\text{ pF}$	25°C			$R_L = 50\text{ k}\Omega$	0.73		0.73	MHz
$B_{OM}$ Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $R_L = 50\text{ k}\Omega$	25°C			$A_V = 1$ , $C_L = 100\text{ pF}$	85		85	kHz
$t_s$ Settling time	$A_V = -1$ , Step = $-2.3\text{ V to }2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C		To 0.1%		7.1		7.1	$\mu\text{s}$
				To 0.01%		16.5		16.5	
$\phi_m$ Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C				57°		57°	
		25°C				11		11	
Gain margin		25°C							dB

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

**TLC2264I electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{DD} = \pm 2.5\text{ V}$ , $V_O = 0$ , $V_{IC} = 0$ , $R_S = 50\ \Omega$	25°C	300	2500		300	950	$\mu\text{V}$	
		Full range		3000		1500			
$\alpha V_{IO}$ Temperature coefficient of input offset voltage		25°C to 125°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5			0.5		$\text{pA}$	
		85°C		150		150			
		Full range		800		800			
$I_{IB}$ Input bias current		25°C	1			1		$\text{pA}$	
		85°C		150		150			
		Full range		800		800			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
$V_{OH}$ High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.99			4.99		V	
	$I_{OH} = -100\ \mu\text{A}$	25°C	4.85	4.94		4.85	4.94		
	$I_{OH} = -400\ \mu\text{A}$	25°C	4.7	4.85		4.7	4.85		
		Full range	4.5			4.5			
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V}$ , $I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01		V	
	$V_{IC} = 2.5\text{ V}$ , $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09	0.15		
	$V_{IC} = 2.5\text{ V}$ , $I_{OL} = 4\text{ mA}$	25°C	0.8	1		0.7	1		
		Full range		1.2		1.2			
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to }4\text{ V}$	$R_L = 50\text{ k}\Omega$ ‡	25°C	80	100		80	170	V/mV
		$R_L = 1\text{ M}\Omega$ ‡	Full range	50			50		
			25°C	550			550		
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$			$10^{12}$	$\Omega$		
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$			$10^{12}$	$\Omega$		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$ , N package	25°C	8			8	$\text{pF}$		
$z_o$ Closed-loop output impedance	$f = 100\text{ kHz}$ , $A_V = 10$	25°C	240			240	$\Omega$		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$ , $V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }16\text{ V}$ , $V_{IC} = V_{DD}/2$ , No load	25°C	80	95		80	95	dB	
		Full range	80			80			

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2264I operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{DD}$ Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , No load	25°C	0.8	1		0.8	1	$\text{V}/\mu\text{s}$	
		Full range			1		1		
SR Slew rate at unity gain	$V_O = 1.4\text{ V to } 2.6\text{ V}$ , $R_L = 50\text{ k}\Omega^\ddagger$ , $C_L = 100\text{ pF}^\ddagger$	25°C	0.35	0.55		0.35	0.55	$\text{V}/\mu\text{s}$	
		Full range	0.25			0.25			
$V_n$ Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		40			40	$\text{nV}/\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C		12			12		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to } 1\text{ Hz}$	25°C		0.7			0.7	$\mu\text{V}$	
	$f = 0.1\text{ Hz to } 10\text{ Hz}$	25°C		1.3			1.3		
$I_n$ Equivalent input noise current		25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to } 2.5\text{ V}$ , $f = 20\text{ kHz}$ , $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C			0.017%	0.017%		
		$A_V = 10$	25°C			0.03%	0.03%		
Gain-bandwidth product	$f = 50\text{ kHz}$ , $C_L = 100\text{ pF}^\ddagger$ , $R_L = 50\text{ k}\Omega^\ddagger$	25°C		0.71			0.71	MHz	
$B_{OM}$ Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$ , $R_L = 50\text{ k}\Omega^\ddagger$ , $C_L = 100\text{ pF}^\ddagger$	25°C		185			185	kHz	
$t_s$ Settling time	$A_V = -1$ , Step = $0.5\text{ V to } 2.5\text{ V}$ , $R_L = 50\text{ k}\Omega^\ddagger$ , $C_L = 100\text{ pF}^\ddagger$	To 0.1%	25°C			6.4	6.4	$\mu\text{s}$	
		To 0.01%	25°C			14.1	14.1		
$\phi_m$ Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$ , $C_L = 100\text{ pF}^\ddagger$	25°C		56°			56°		
		25°C		11			11		
Gain margin		25°C		11			11	dB	

† Full range is  $-40^\circ\text{C to } 125^\circ\text{C}$ .

‡ Referenced to  $2.5\text{ V}$

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2264I electrical characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	300	2500		300	950	$\mu\text{V}$	
		Full range			3000		1500		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 125°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5			0.5		pA	
	85°C		150		150				
	Full range		800		800				
$I_{IB}$ Input bias current		25°C	1			1		pA	
		85°C		150		150		pA	
		Full range		800		800		pA	
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega,  V_{IO}  \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
$V_{OM+}$ Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99			4.99		V	
	$I_O = -100\ \mu\text{A}$	25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
	$I_O = -400\ \mu\text{A}$	25°C	4.7	4.85		4.7	4.85		
$V_{OM-}$ Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C	-4.99			-4.99		V	
		25°C	-4.85	-4.91		-4.85	-4.91		
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	Full range	-4.85			-4.85			
		25°C	-4	-4.3		-4	-4.3		
$V_{IC} = 0, I_O = 4\ \text{mA}$	Full range	-3.8			-3.8				
	25°C	80	200		80	200	V/mV		
$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	Full range	50		50				
	$R_L = 1\ \text{M}\Omega$	25°C	1000		1000				
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$		$10^{12}$		$\Omega$		
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$		$10^{12}$		$\Omega$		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{N package}$	25°C	8		8		pF		
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz}, A_V = 10$	25°C	220		220		$\Omega$		
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD\pm}/\Delta V_{IO}$ )	$V_{DD\pm} = \pm 2.2\ \text{V to } \pm 8\ \text{V}, V_{IC} = V_{DD}/2, \text{No load}$	25°C	80	95		80	95	dB	
		Full range	80			80			

† Full range is -40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2264I operating characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{DD}$ Supply current (four amplifiers)	$V_O = 0$ , No load	25°C	0.85	1		0.85	1		
		Full range			1		1		
SR Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 50\text{ k}\Omega$	25°C	0.35	0.55		0.35	0.55	V/ $\mu\text{s}$	
		Full range	0.25			0.25			
$V_n$ Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		43			43	nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C		12			12		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		0.8			0.8	$\mu\text{V}$	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.3			1.3		
$I_n$ Equivalent input noise current		25°C		0.6			0.6	fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $f = 20\text{ kHz}$	$A_V = 1$	25°C			0.014%	0.014%		
		$A_V = 10$	25°C			0.024%	0.024%		
Gain-bandwidth product	$f = 10\text{ kHz}$ , $C_L = 100\text{ pF}$ , $R_L = 50\text{ k}\Omega$	25°C		0.73			0.73	MHz	
$B_{OM}$ Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $A_V = 1$ , $C_L = 100\text{ pF}$	25°C		70			70	kHz	
$t_s$ Settling time	$A_V = -1$ , Step = $-2.3\text{ V to }2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$	To 0.1%	25°C			7.1	7.1		
		To 0.01%	25°C			16.5	16.5		
$\phi_m$ Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C		57°			57°		
		Gain margin	25°C		11			11	dB

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2262Q/M electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0$ , $V_{IC} = 0$ , $R_S = 50\ \Omega$	25°C	300	2500		300	950	$\mu\text{V}$	
		Full range			3000		1500		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		5			5	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003	$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C		0.5			0.5	$\text{pA}$	
		125°C			800		800		
$I_{IB}$ Input bias current	25°C		1			1	$\text{pA}$		
	125°C			800		800			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
$V_{OH}$ High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99	V	
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
$V_{OL}$ Low-level output voltage	$I_{OL} = -400\ \mu\text{A}$	25°C		0.01			0.01	V	
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.8	1		0.7	1		
$V_{OL}$ Low-level output voltage	$I_{OL} = 500\ \mu\text{A}$	25°C		0.01			0.01	V	
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.8	1		0.7	1		
$V_{OL}$ Low-level output voltage	$I_{OL} = 4\text{ mA}$	25°C		0.01			0.01	V	
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.8	1		0.7	1		
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to }4\text{ V}$	$R_L = 50\text{ k}\Omega$ ‡	25°C	80	100		80	170	V/mV
			Full range	50			50		
		$R_L = 1\text{ M}\Omega$ ‡	25°C		550			550	
$r_{i(d)}$ Differential input resistance		25°C		$10^{12}$			$10^{12}$	$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C		$10^{12}$			$10^{12}$	$\Omega$	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$ , P package	25°C		8			8	pF	
$Z_o$ Closed-loop output impedance	$f = 100\text{ kHz}$ , $A_V = 10$	25°C		240			240	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$ , $V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }16\text{ V}$ , $V_{IC} = V_{DD}/2$ , No load	25°C	80	95		80	95	dB	
		Full range	80			80			
$I_{DD}$ Supply current	$V_O = 2.5\text{ V}$ , No load	25°C		400	500		400	500	$\mu\text{A}$
		Full range			500			500	

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2262Q/M operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }3.5\text{ V}, R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	0.35	0.55		0.35	0.55		V/ $\mu\text{s}$
		Full range	0.25			0.25			
$V_n$	Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C	40			40			nV/ $\sqrt{\text{Hz}}$
		25°C	12			12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	0.7			0.7			$\mu\text{V}$
		25°C	1.3			1.3			
$I_n$	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}, f = 20\text{ kHz}, R_L = 50\text{ k}\Omega\ddagger$	25°C	$A_V = 1$			0.017%			
			$A_V = 10$			0.03%			
	Gain-bandwidth product $f = 50\text{ kHz}, C_L = 100\text{ pF}\ddagger$	25°C	0.82			0.82			MHz
$B_{OM}$	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}, R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	185			185			kHz
$t_s$	Settling time $A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	To 0.1%			6.4			$\mu\text{s}$
			To 0.01%			14.1			
$\phi_m$	Phase margin at unity gain $R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	56°			56°			
		25°C	11			11			dB

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

‡ Referenced to 2.5 V

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2262Q/M electrical characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	300	2500		300	950	$\mu\text{V}$	
		Full range		3000		1500			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	5			5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5			0.5		$\text{pA}$	
		125°C		800		800			
$I_{IB}$ Input bias current		25°C	1			1		$\text{pA}$	
		125°C		800		800			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega,  V_{IO}  \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4		-5 to 4	-5.3 to 4.2	$\text{V}$	
		Full range	-5 to 3.5			-5 to 3.5			
$V_{OM+}$ Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99			4.99		$\text{V}$	
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
$V_{OM-}$ Maximum negative peak output voltage	$I_O = -400\ \mu\text{A}$	25°C	-4.99			-4.99		$\text{V}$	
		25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
		25°C	-4	-4.3		-4	-4.3		
$V_{IC} = 0, I_O = 4\ \text{mA}$	$I_O = 50\ \mu\text{A}$	25°C	-3.8			-3.8		$\text{V}$	
		Full range	-3.8			-3.8			
		25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200		80	200	$\text{V}/\text{mV}$
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$	25°C	1000			1000		
$r_{i(d)}$ Differential input resistance		25°C	1012			1012		$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C	1012			1012		$\Omega$	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{P package}$	25°C	8			8		$\text{pF}$	
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz}, A_V = 10$	25°C	220			220		$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88	$\text{dB}$	
		Full range	75			75			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD\pm} / \Delta V_{IO}$ )	$V_{DD} = 4.4\ \text{V to } 16\ \text{V}, V_{IC} = V_{DD}/2, \text{No load}$	25°C	80	95		80	95	$\text{dB}$	
		Full range	80			80			
$I_{DD}$ Supply current	$V_O = 0, \text{No load}$	25°C	425	500		425	500	$\mu\text{A}$	
		Full range		500			500		

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2262Q/M operating characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = \pm 2\text{ V}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.35	0.55		0.35	0.55	V/ $\mu\text{s}$	
			Full range	0.25			0.25			
$V_n$	Equivalent input noise voltage		25°C	43			43			nV/ $\sqrt{\text{Hz}}$
			25°C	12			12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		25°C	0.8			0.8			$\mu\text{V}$
			25°C	1.3			1.3			
$I_n$	Equivalent input noise current		25°C	0.6			0.6			fA $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $f = 20\text{ kHz}$	$A_V = 1$	25°C	0.014%			0.014%			
			$A_V = 10$	0.024%			0.024%			
	Gain-bandwidth product $f = 10\text{ kHz}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.73			0.73			MHz
$B_{OM}$	Maximum output-swing bandwidth $V_{O(PP)} = 4.6\text{ V}$ , $R_L = 50\text{ k}\Omega$	$A_V = 1$ , $C_L = 100\text{ pF}$	25°C	85			85			kHz
$t_s$	Settling time $A_V = -1$ , Step = $-2.3\text{ V}$ to $2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$	To 0.1%	25°C	7.1			7.1			$\mu\text{s}$
		To 0.01%		16.5			16.5			
$\phi_m$	Phase margin at unity gain $R_L = 50\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	57°			57°			
	Gain margin		25°C	11			11			

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

# TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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**TLC2264Q/M electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	300	2500		300	950	$\mu\text{V}$	
		Full range		3000		1500			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5\text{ V}$ , $V_O = 0$ , $V_{IC} = 0$ , $R_S = 50\ \Omega$	25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.5			0.5			pA
		125°C	800			800			
$I_{IB}$ Input bias current		25°C	1			1			pA
	125°C	800			800				
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5		0 to 3.5				
$V_{OH}$ High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	25°C	4.99			4.99			V
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V}$ , $I_{OL} = 50\ \mu\text{A}$ $I_{OL} = 500\ \mu\text{A}$ $I_{OL} = 4\text{ mA}$	25°C	0.01			0.01			V
		25°C	0.09	0.15		0.09	0.15		
		Full range	0.15			0.15			
		25°C	0.8	1		0.7	1		
$AVD$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to } 4\text{ V}$	25°C	$R_L = 50\ \text{k}\Omega^\ddagger$			80 100 80 170			V/mV
			Full range			50 50			
		25°C	$R_L = 1\ \text{M}\Omega^\ddagger$			550 550			
$r_{i(d)}$ Differential input resistance		25°C	$10^{12}$			$10^{12}$			$\Omega$
$r_{i(c)}$ Common-mode input resistance		25°C	$10^{12}$			$10^{12}$			$\Omega$
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$ , N package	25°C	8			8			pF
$z_o$ Closed-loop output impedance	$f = 100\text{ kHz}$ , $A_V = 10$	25°C	240			240			$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V}$ , $V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to } 16\text{ V}$ ,	25°C	80	95		80	95	dB	
$I_{DD}$ Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , No load	25°C	0.8	1		0.8	1	mA	
		Full range	1			1			

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2264Q/M operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }3.5\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	0.35	0.55		0.35	0.55		V/ $\mu\text{s}$
		Full range	0.25			0.25			
$V_n$	Equivalent input noise voltage	f = 10 Hz	40			40			nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz	12			12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	0.7			0.7			$\mu\text{V}$
		f = 0.1 Hz to 10 Hz	1.3			1.3			
$I_n$	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}, f = 20\text{ kHz}, R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	0.017%			0.017%			
		$A_V = 10$	0.03%			0.03%			
	Gain-bandwidth product f = 50 kHz, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger, 25^\circ\text{C}$	0.71			0.71			MHz
$B_{OM}$	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, A_V = 1, C_L = 100\text{ pF}^\ddagger$	25°C	185			185			kHz
$t_s$	Settling time $A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	To 0.1%	6.4			6.4			$\mu\text{s}$
		To 0.01%	14.1			14.1			
$\phi_m$	Phase margin at unity gain $R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	56°			56°			
		25°C	11			11			

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

‡ Referenced to 2.5 V

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**TLC2264Q/M electrical characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	300	2500		300	950	$\mu\text{V}$	
		Full range			3000		1500		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003	$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C		0.5			0.5	pA	
		125°C			800		800		
$I_{IB}$ Input bias current	25°C		1			1	pA		
	125°C			800		800			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega,  V_{IO}  \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
$V_{OM+}$ Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.99			4.99	V	
	$I_O = -100\ \mu\text{A}$	25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
	$I_O = -400\ \mu\text{A}$	25°C	4.7	4.85		4.7	4.85		
Full range		4.5			4.5				
$V_{OM-}$ Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99	V	
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
	$V_{IC} = 0, I_O = 4\ \text{mA}$	25°C	-4	-4.3		-4	-4.3		
Full range		-3.8			-3.8				
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200		80	200	V/mV
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$	25°C		1000			1000	
$r_{i(d)}$ Differential input resistance		25°C		$10^{12}$			$10^{12}$	$\Omega$	
$r_{i(c)}$ Common-mode input resistance		25°C		$10^{12}$			$10^{12}$	$\Omega$	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{N package}$	25°C		8			8	pF	
$z_o$ Closed-loop output impedance	$f = 100\ \text{kHz}, A_V = 10$	25°C		220			220	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD\pm}/\Delta V_{IO}$ )	$V_{DD\pm} = \pm 2.2\ \text{V to } \pm 8\ \text{V}, V_{IC} = V_{DD}/2, \text{No load}$	25°C	80	95		80	95	dB	
		Full range	80			80			
$I_{DD}$ Supply current (four amplifiers)	$V_O = 0, \text{No load}$	25°C		0.85	1		0.85	1	mA
		Full range			1			1	

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



**TLC2264Q/M operating characteristics at specified free-air temperature,  $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER	TEST CONDITIONS		$T_A$ †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2\text{ V}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$ ,	25°C	0.35	0.55		0.35	0.55	V/ $\mu\text{s}$
				Full range	0.25		0.25			
$V_n$	Equivalent input noise voltage			25°C	43		43		nV/ $\sqrt{\text{Hz}}$	
				25°C	12		12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.8		0.8		$\mu\text{V}$	
				25°C	1.3		1.3			
$I_n$	Equivalent input noise current			25°C	0.6		0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $f = 20\text{ kHz}$		25°C	$A_V = 1$		0.014%			
					$A_V = 10$		0.024%			
	Gain-bandwidth product	$f = 10\text{ kHz}$ , $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$ ,	25°C	0.73		0.73		MHz	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $R_L = 50\text{ k}\Omega$ ,	$A_V = 1$ , $C_L = 100\text{ pF}$	25°C	70		70		kHz	
$t_s$	Settling time	$A_V = -1$ , Step = $-2.3\text{ V}$ to $2.3\text{ V}$ , $R_L = 50\text{ k}\Omega$ , $C_L = 100\text{ pF}$		25°C	To 0.1%		7.1		$\mu\text{s}$	
					To 0.01%		16.5			
$\phi_m$	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ,	$C_L = 100\text{ pF}$	25°C	57°		57°			
	Gain margin			25°C	11		11			dB

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q suffix,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M suffix.

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**Advanced LinCMOS™ RAIL-TO-RAIL**  
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**TYPICAL CHARACTERISTICS**

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2262  
 INPUT OFFSET VOLTAGE

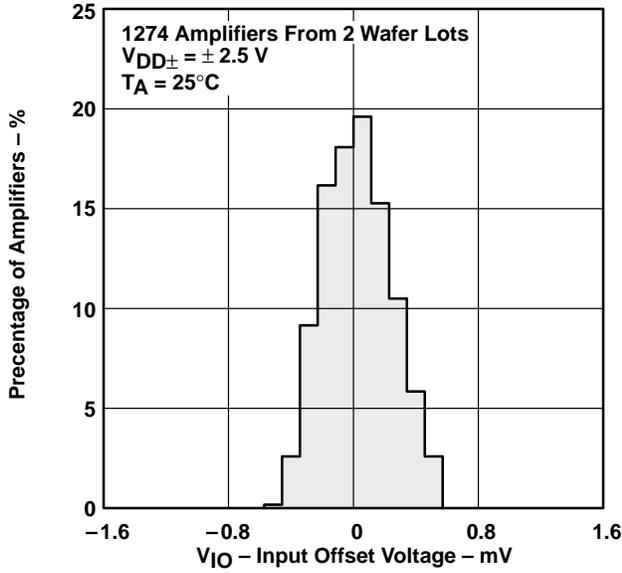


Figure 2

DISTRIBUTION OF TLC2262  
 INPUT OFFSET VOLTAGE

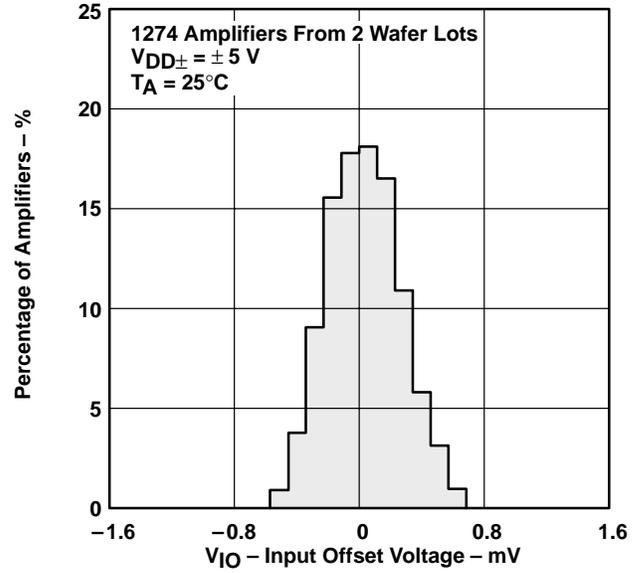


Figure 3

DISTRIBUTION OF TLC2264  
 INPUT OFFSET VOLTAGE

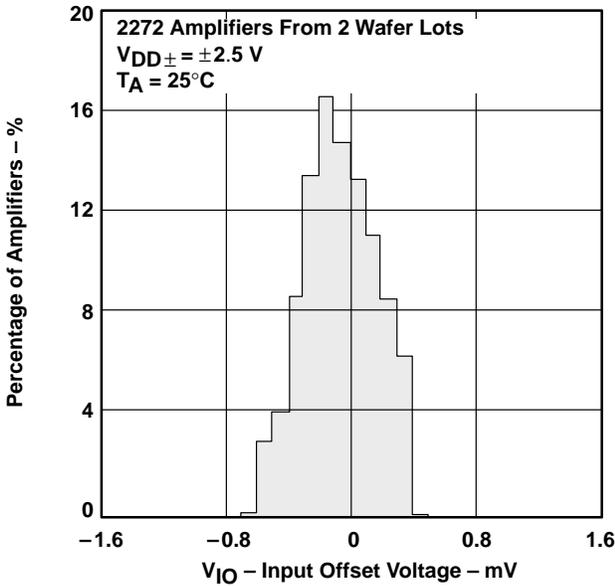


Figure 4

DISTRIBUTION OF TLC2264  
 INPUT OFFSET VOLTAGE

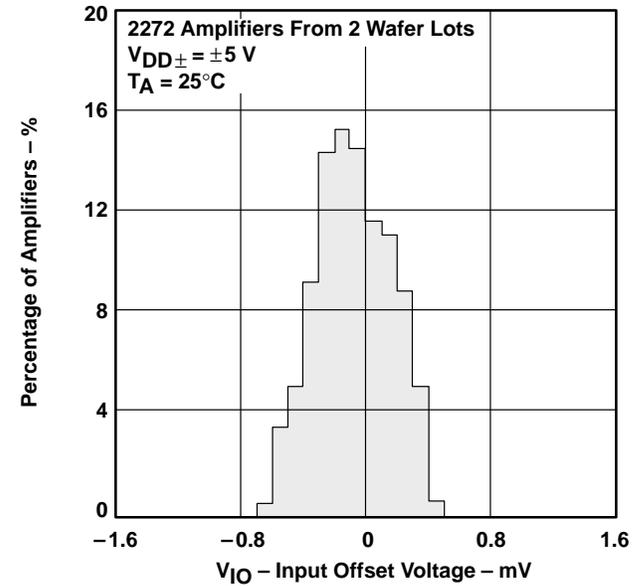
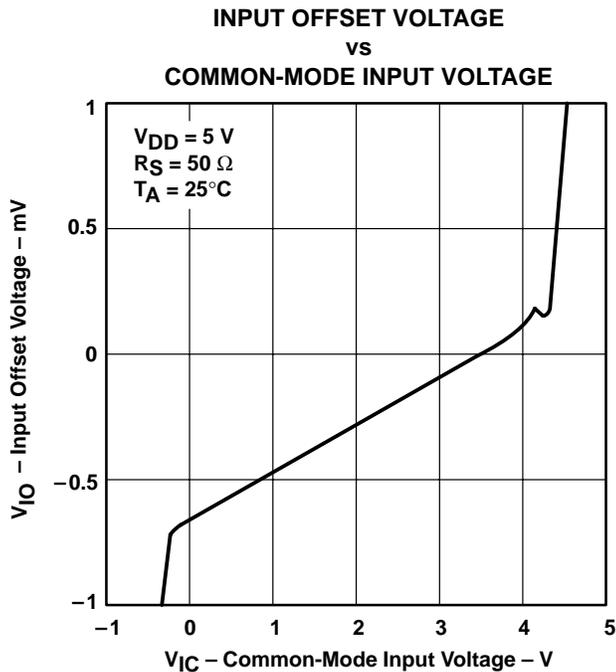
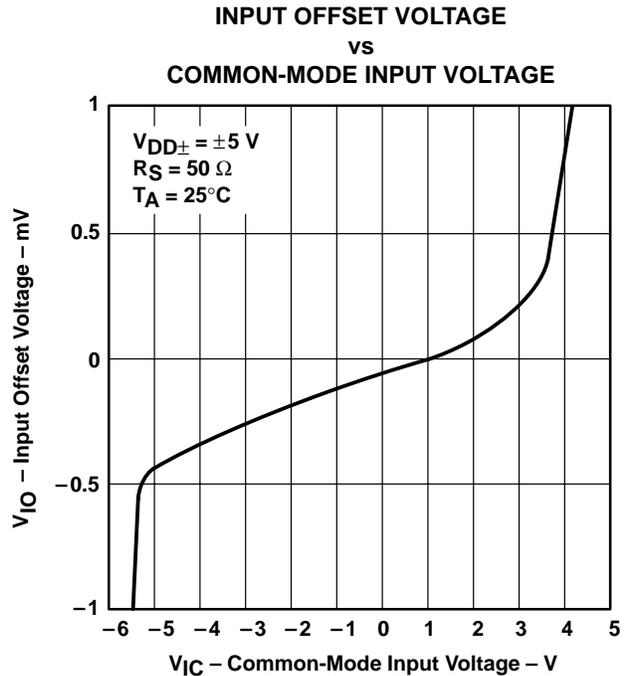


Figure 5

**TYPICAL CHARACTERISTICS**

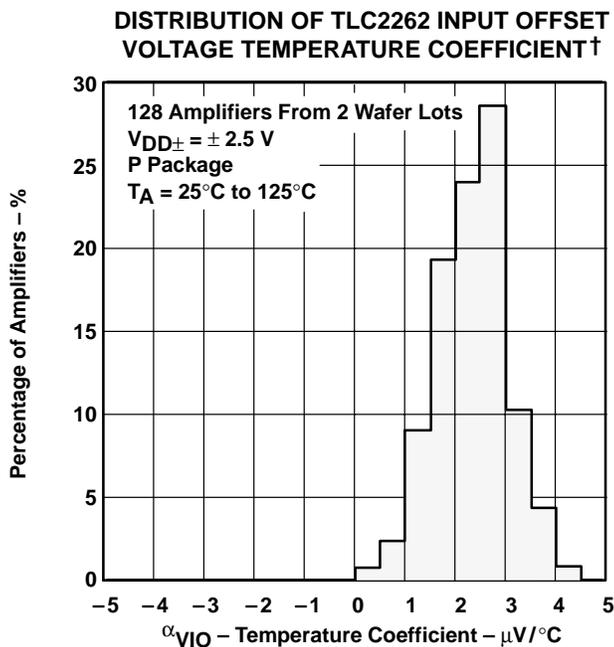


**Figure 6**

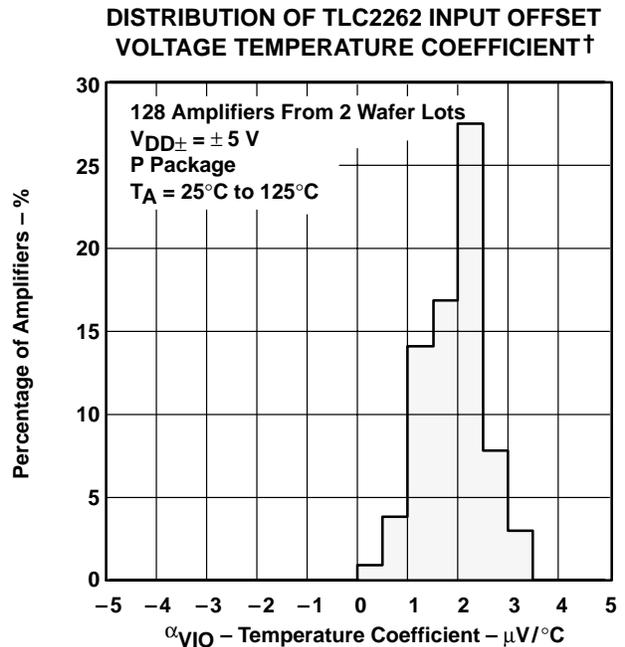


**Figure 7**

† For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.



**Figure 8**



**Figure 9**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

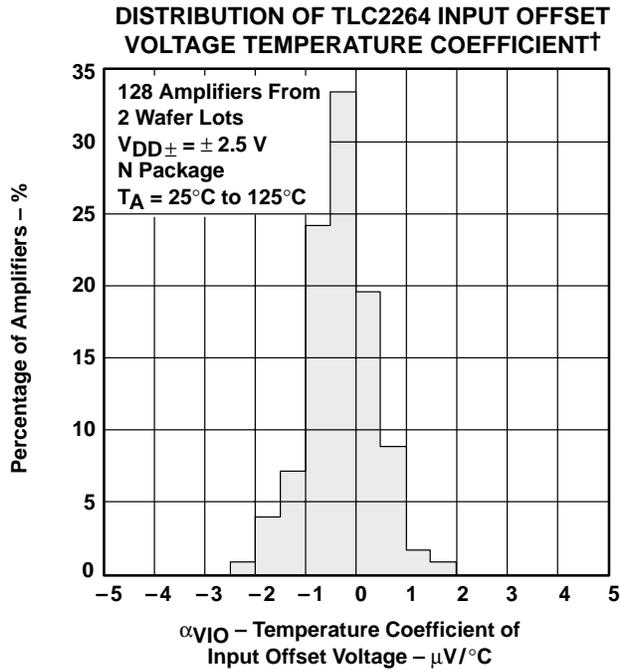


Figure 10

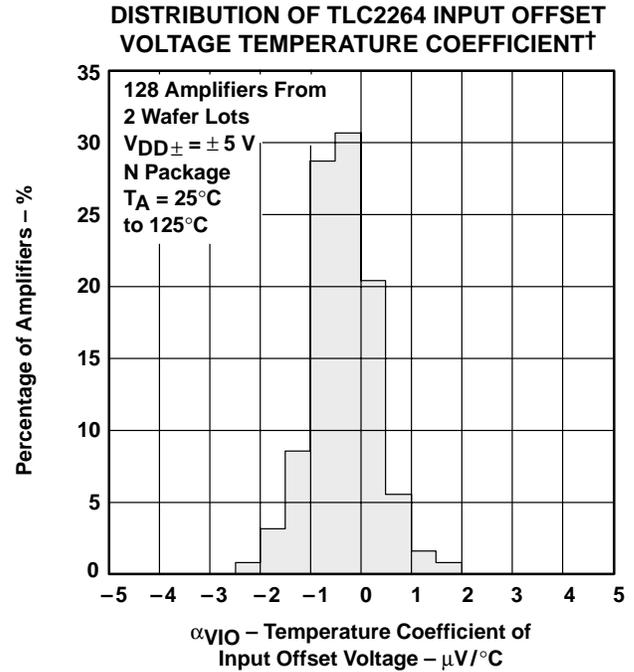


Figure 11

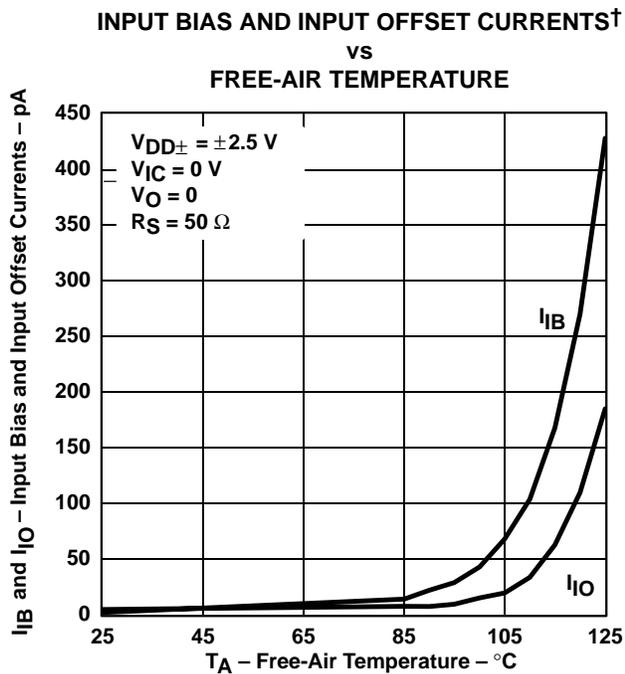


Figure 12

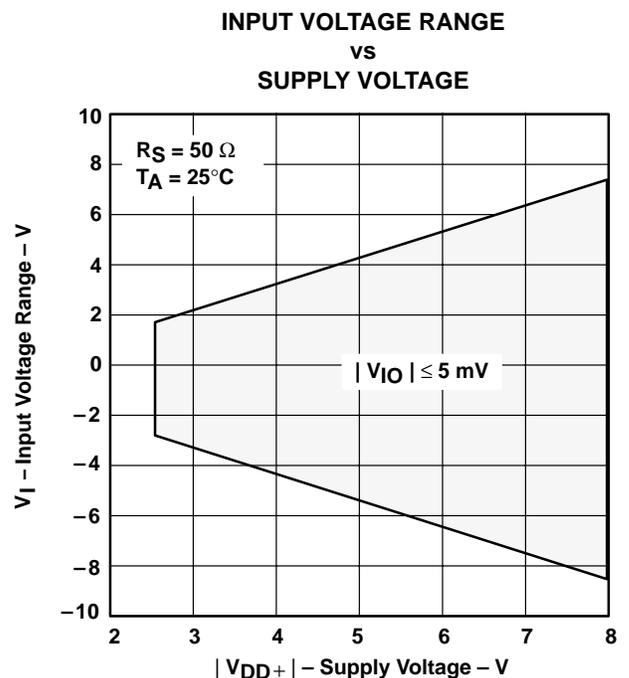


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE†‡  
 vs  
 FREE-AIR TEMPERATURE

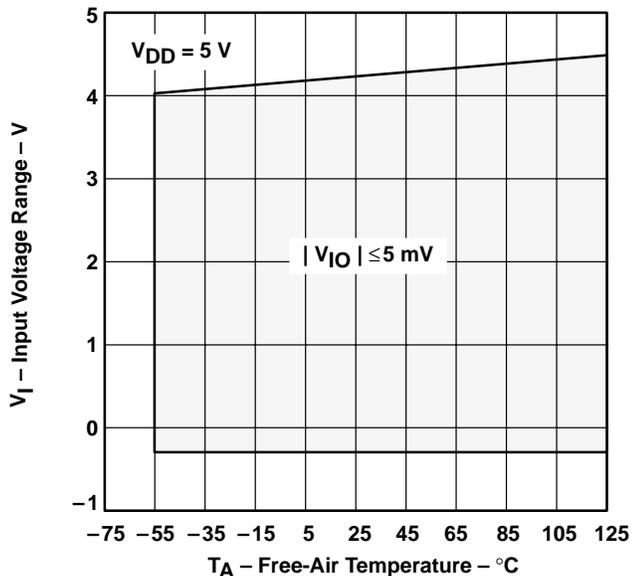


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡  
 vs  
 HIGH-LEVEL OUTPUT CURRENT

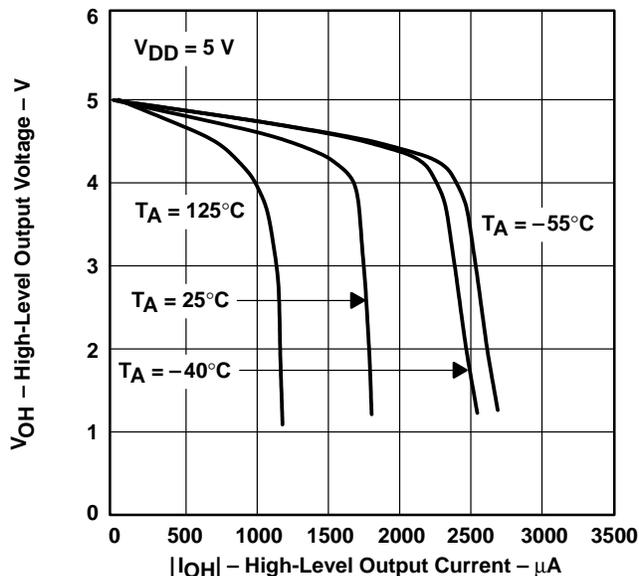


Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡  
 vs  
 LOW-LEVEL OUTPUT CURRENT

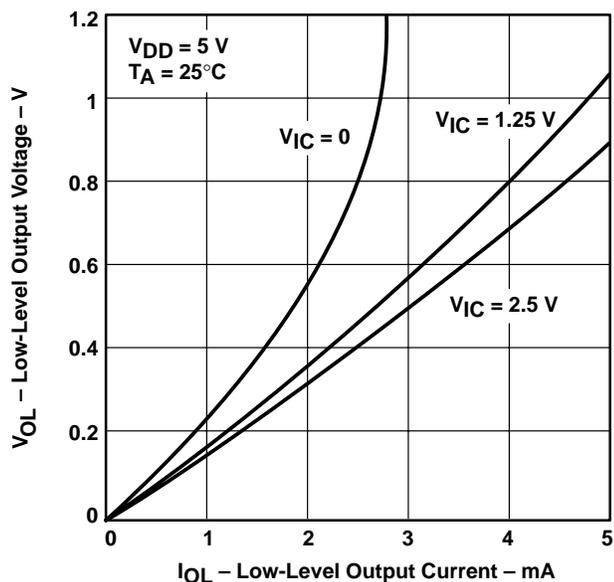


Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡  
 vs  
 LOW-LEVEL OUTPUT CURRENT

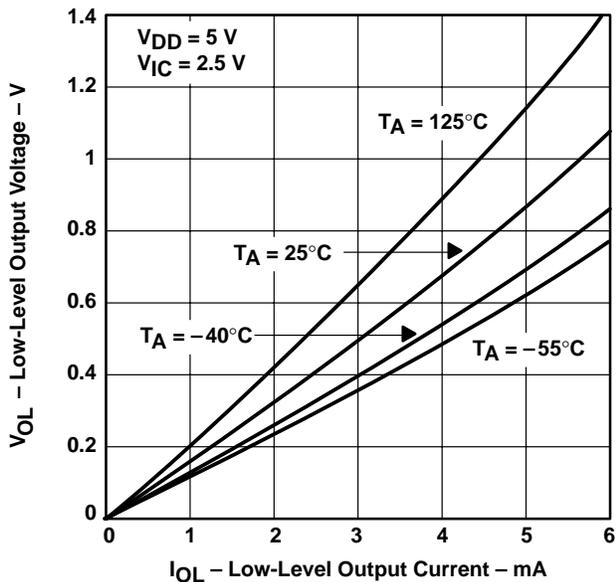


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE†  
vs  
OUTPUT CURRENT

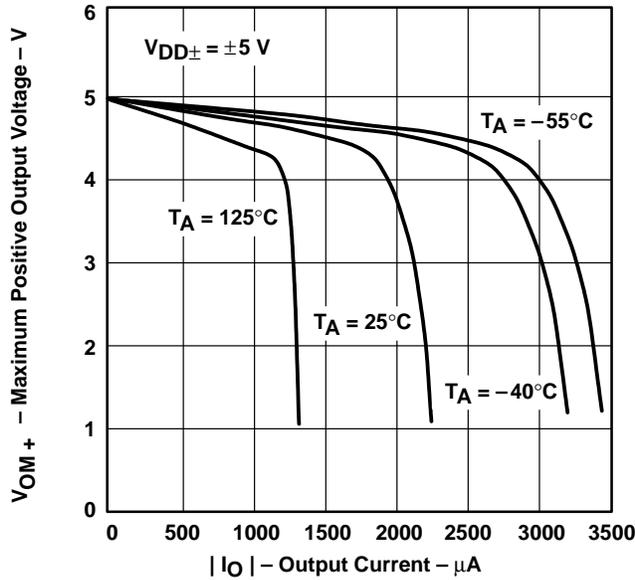


Figure 18

MAXIMUM NEGATIVE OUTPUT VOLTAGE†  
vs  
OUTPUT CURRENT

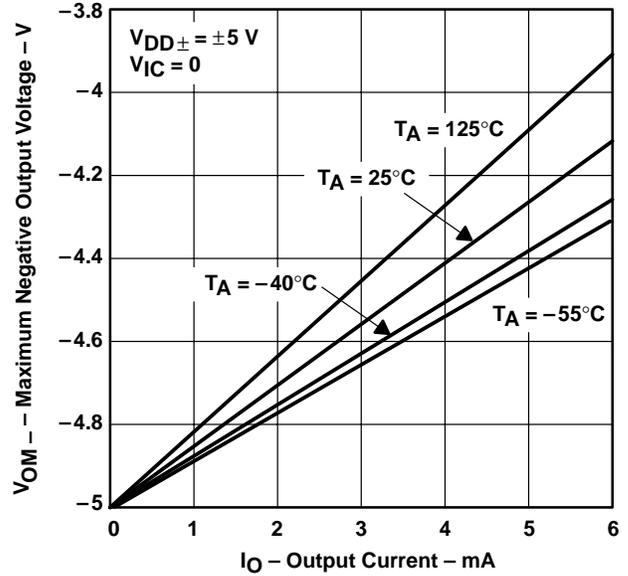


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡  
vs  
FREQUENCY

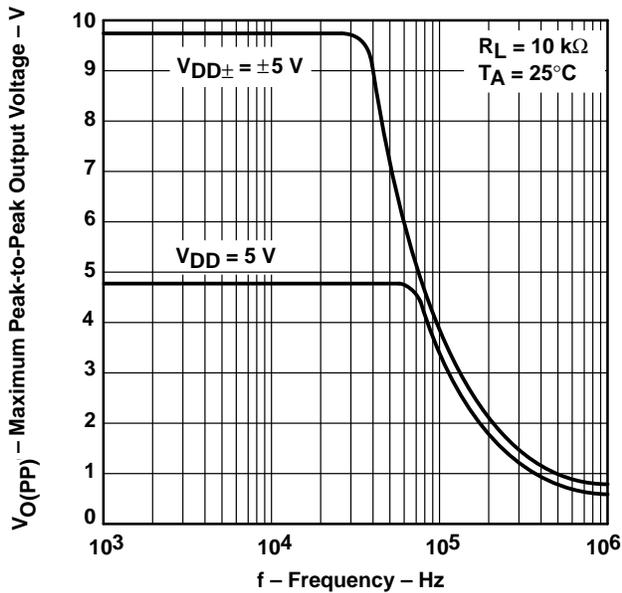


Figure 20

SHORT-CIRCUIT OUTPUT CURRENT  
vs  
SUPPLY VOLTAGE

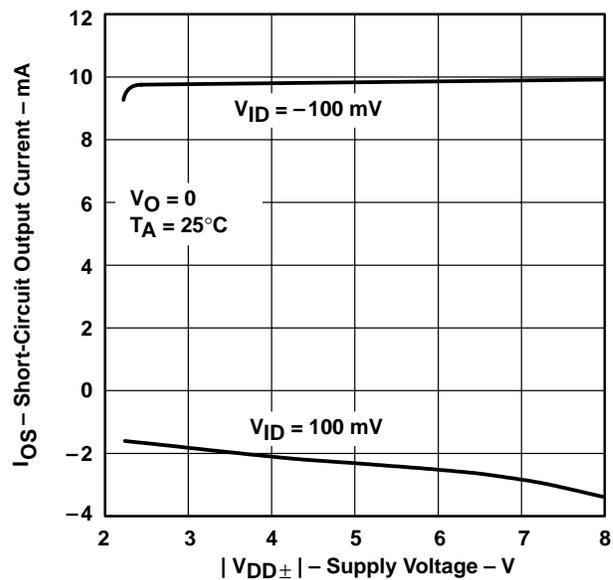


Figure 21

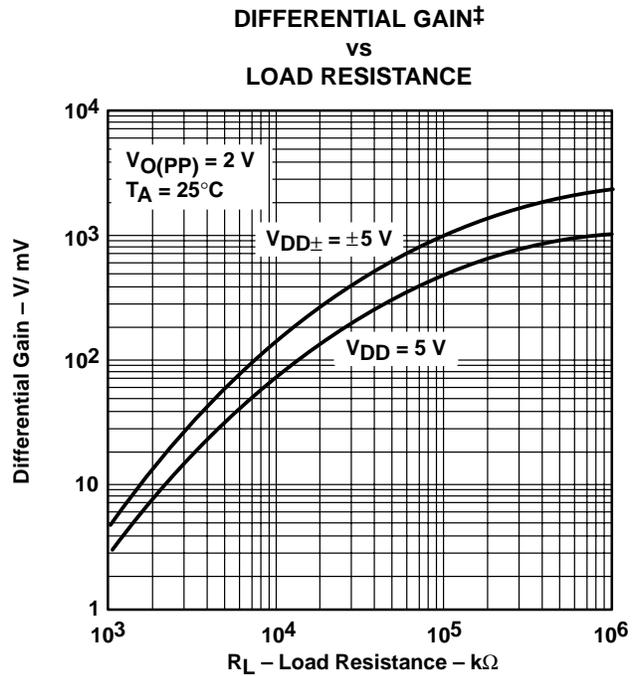
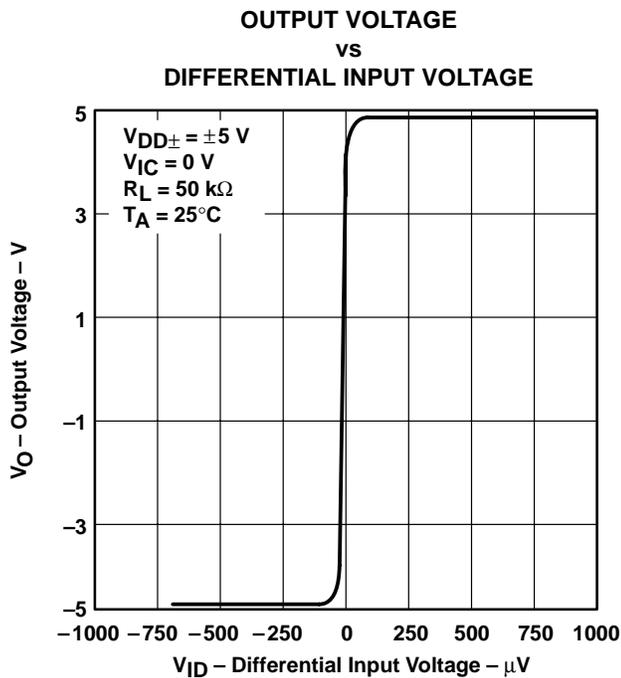
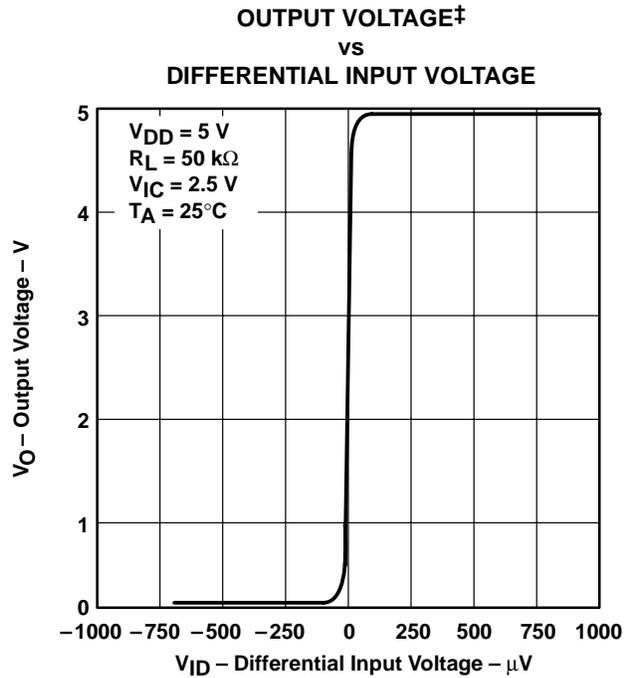
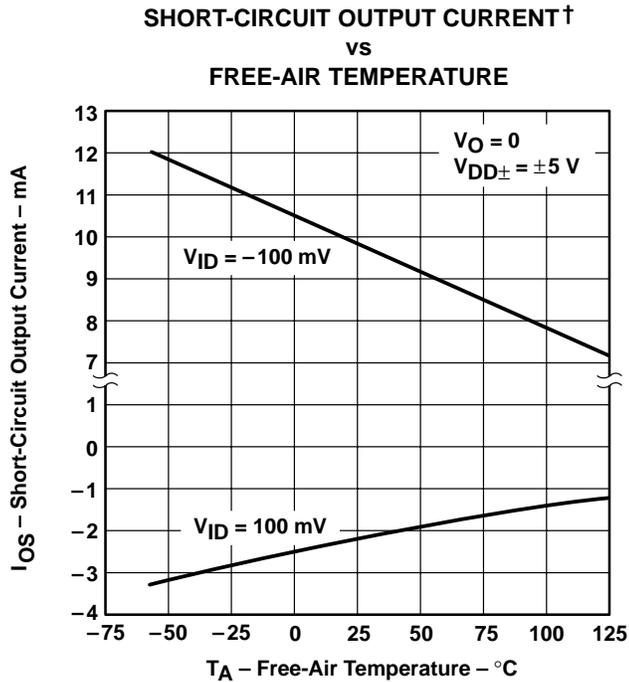
‡ For curves where  $V_{DD} = 5$  V, all loads are referenced to 2.5 V.

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TLC226x, TLC226xA**  
**Advanced LinCMOS™ RAIL-TO-RAIL**  
**OPERATIONAL AMPLIFIERS**

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

**TYPICAL CHARACTERISTICS**



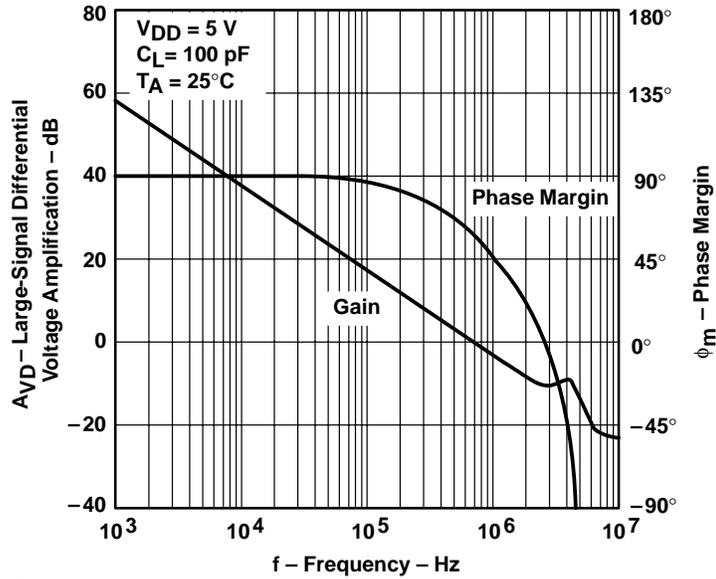
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.



TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE†  
 AMPLIFICATION AND PHASE MARGIN  
 VS  
 FREQUENCY



† For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE MARGIN  
 VS  
 FREQUENCY

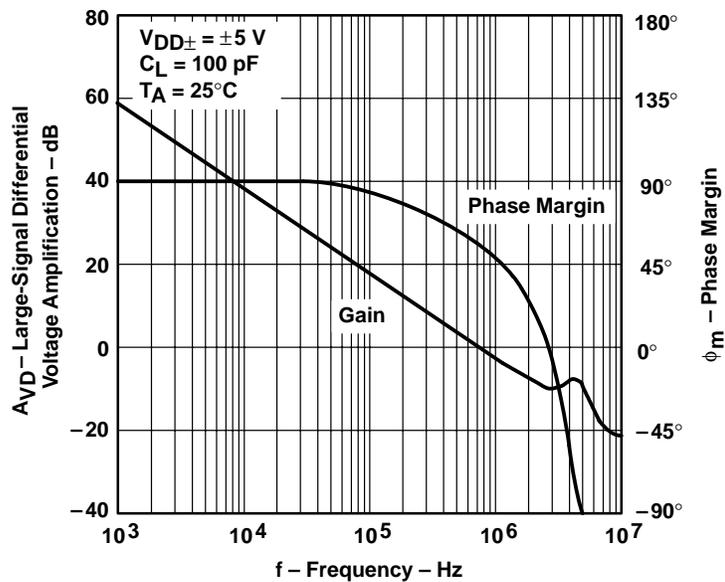
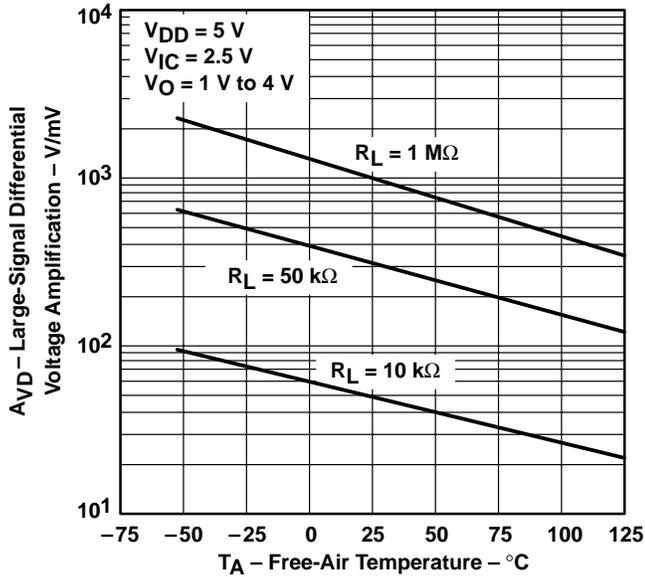


Figure 27

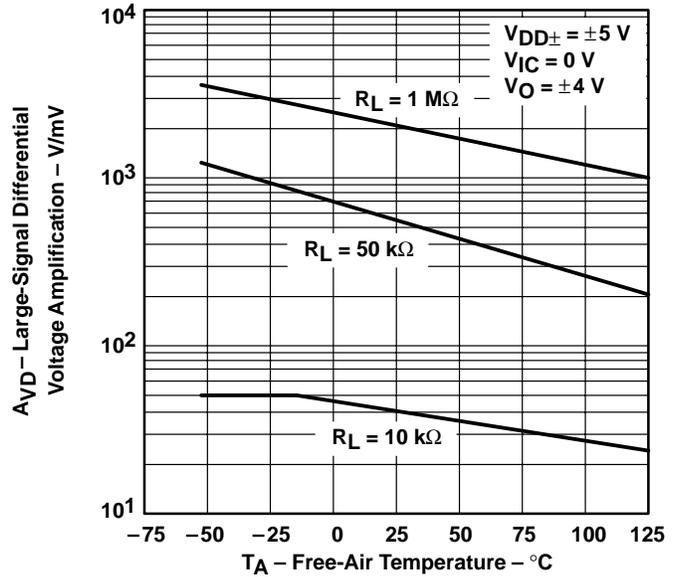
**TYPICAL CHARACTERISTICS**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡**  
**vs**  
**FREE-AIR TEMPERATURE**



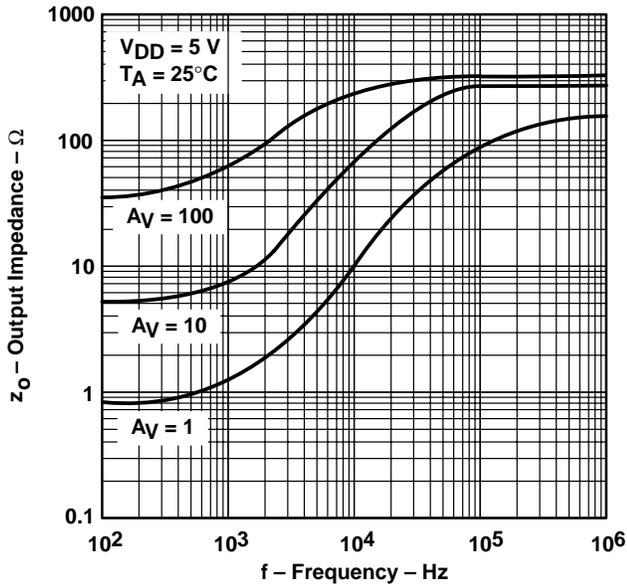
**Figure 28**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†**  
**vs**  
**FREE-AIR TEMPERATURE**



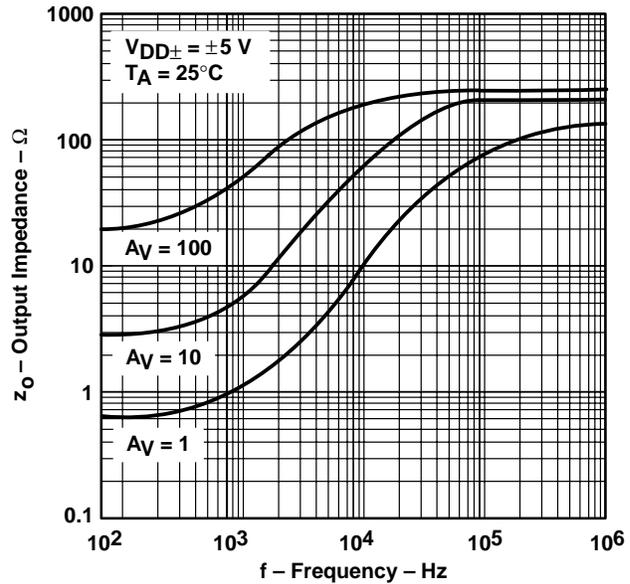
**Figure 29**

**OUTPUT IMPEDANCE‡**  
**vs**  
**FREQUENCY**



**Figure 30**

**OUTPUT IMPEDANCE**  
**vs**  
**FREQUENCY**



**Figure 31**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

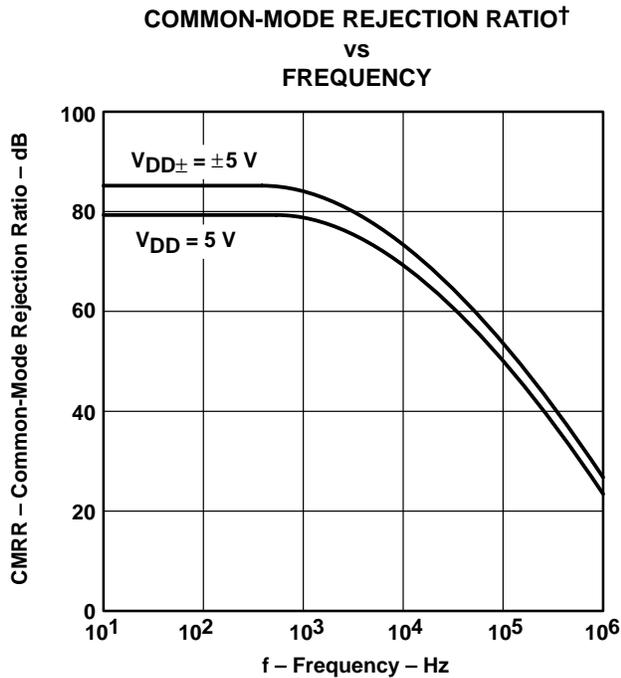


Figure 32

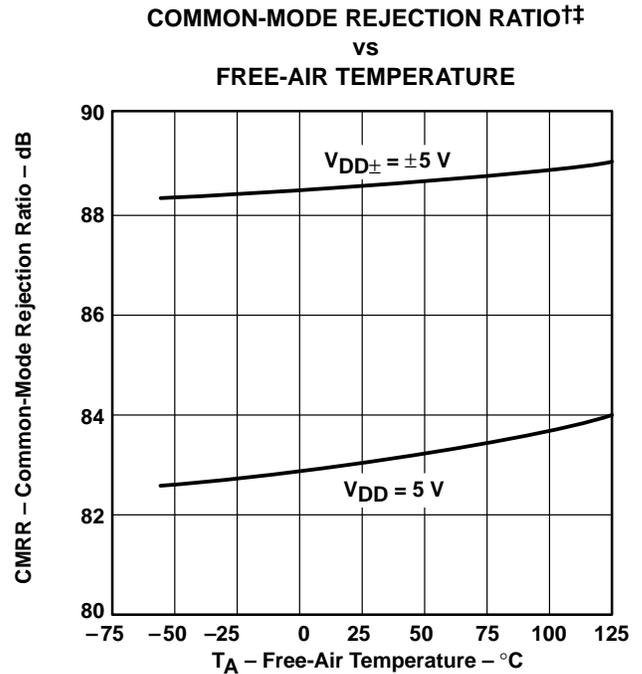


Figure 33

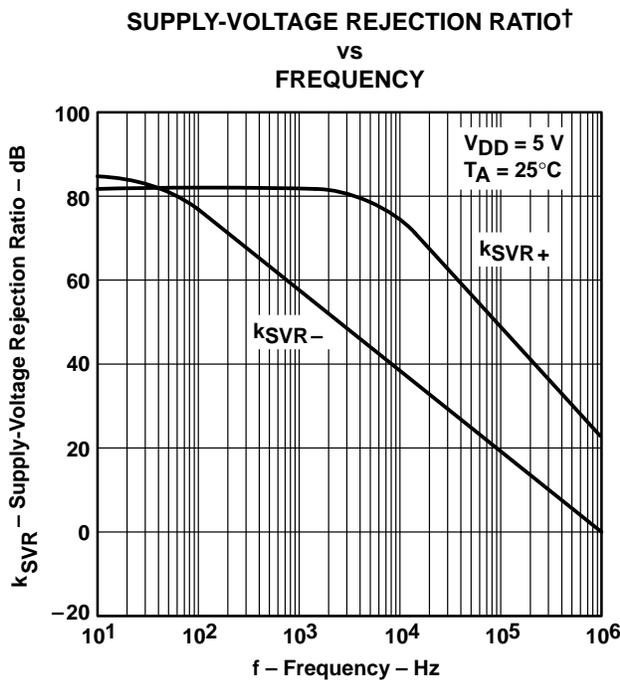


Figure 34

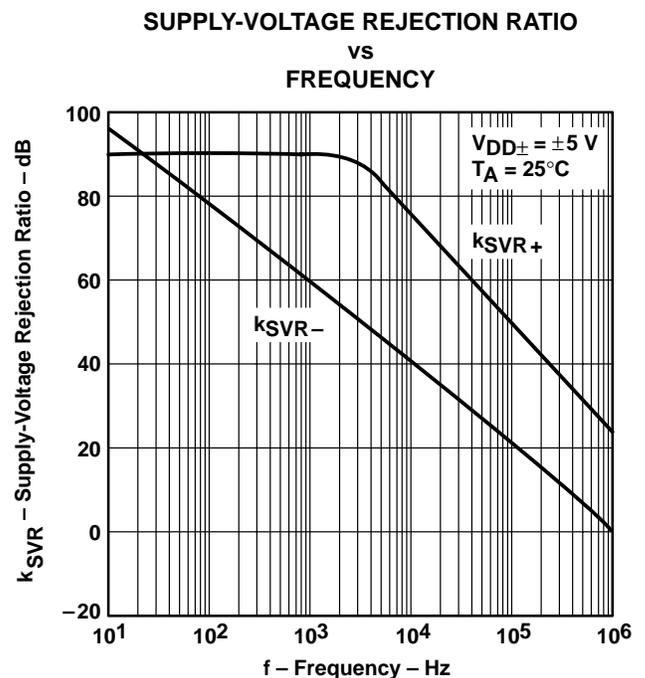
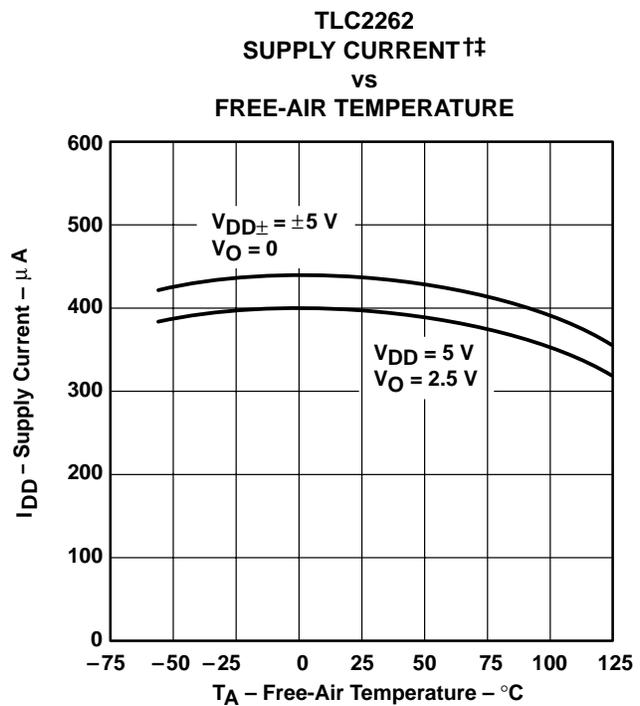
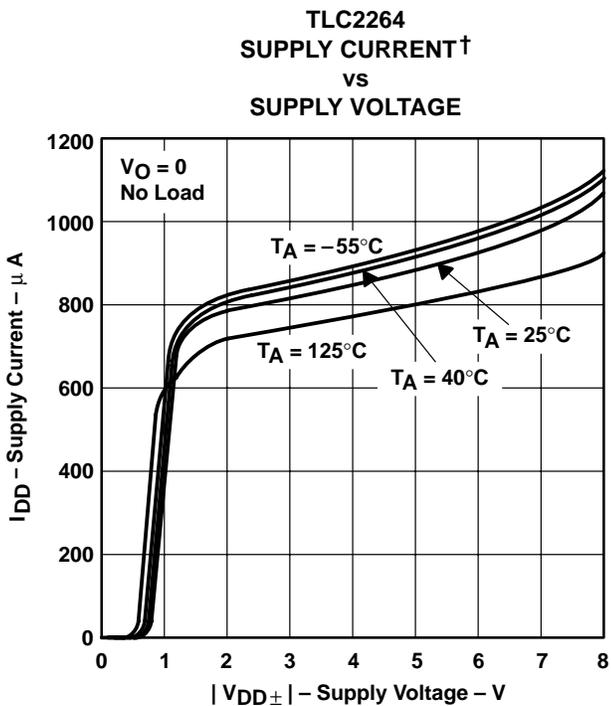
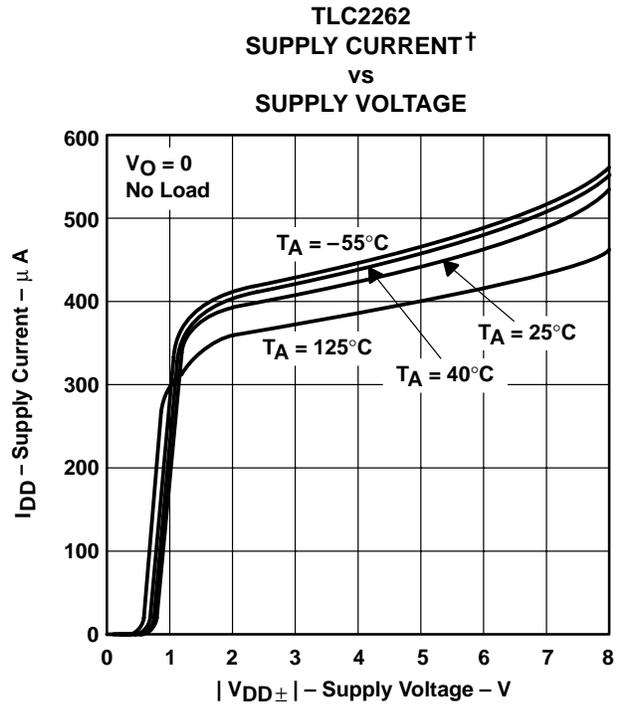
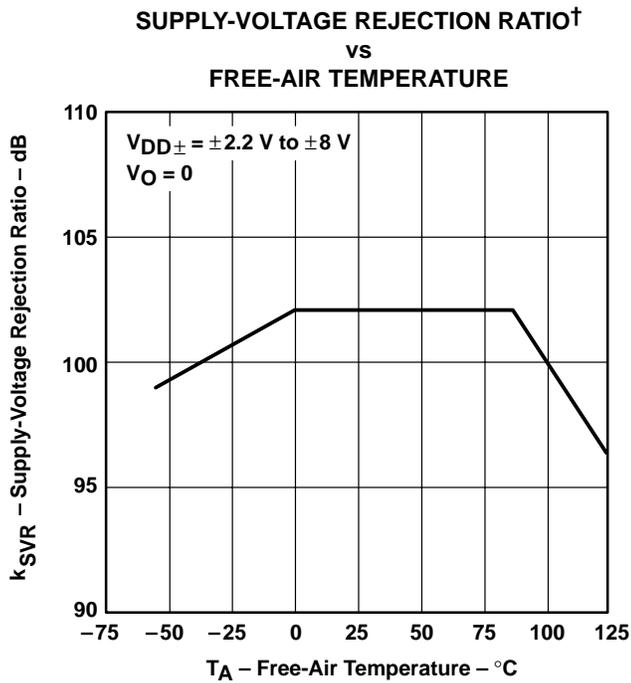


Figure 35

† For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to  $2.5\text{ V}$ .

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

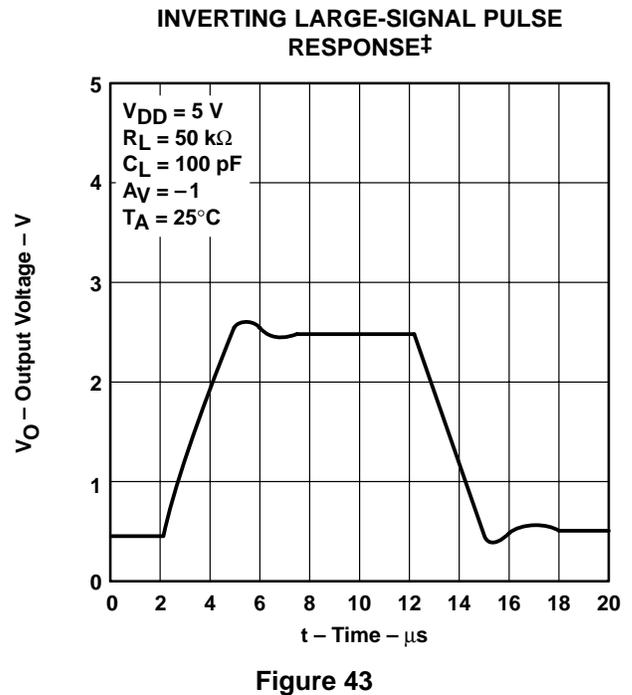
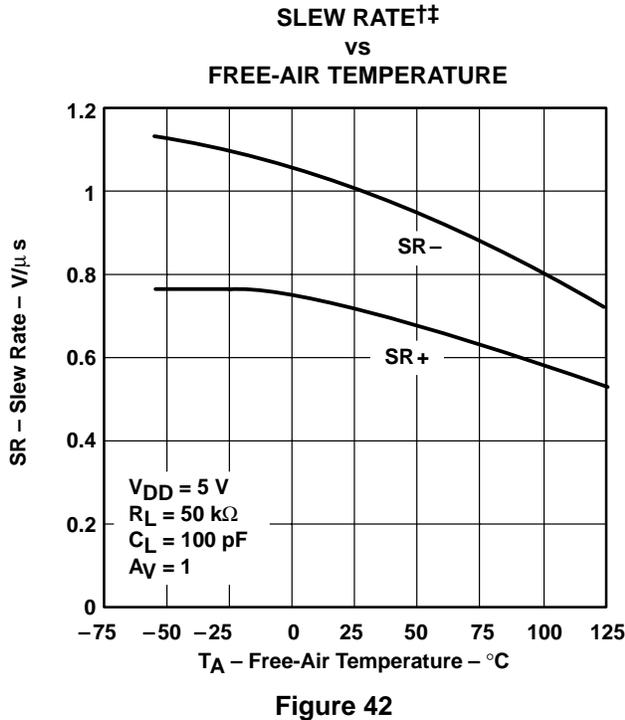
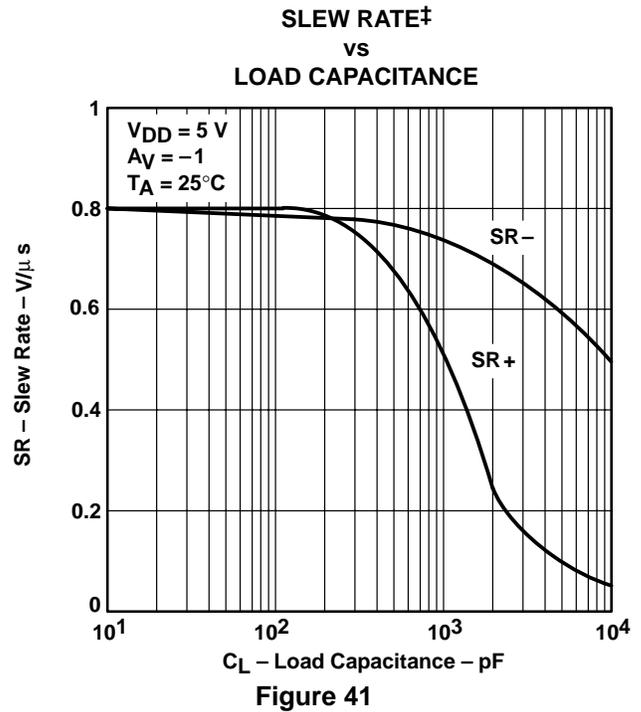
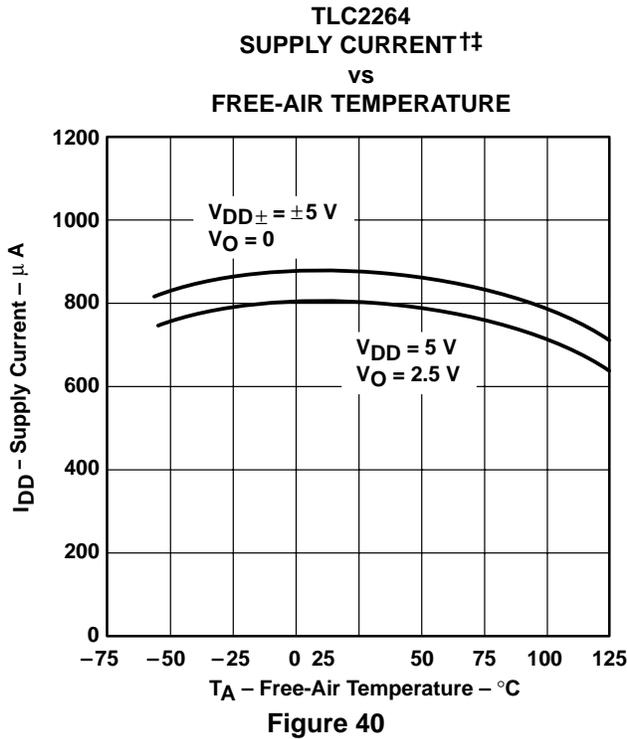
TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

†† For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

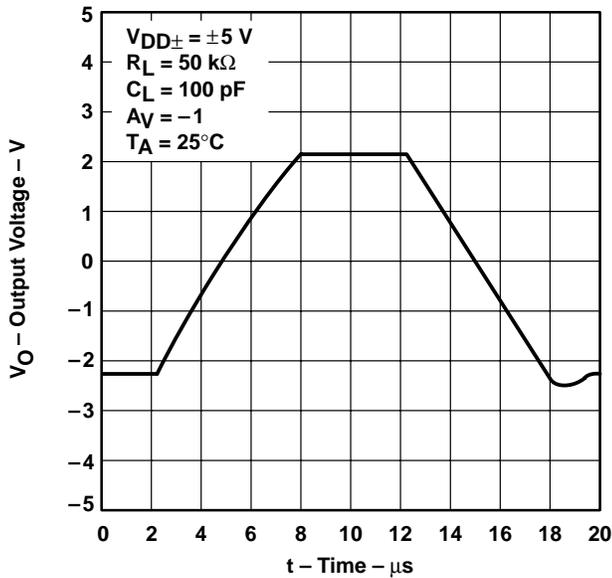


Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

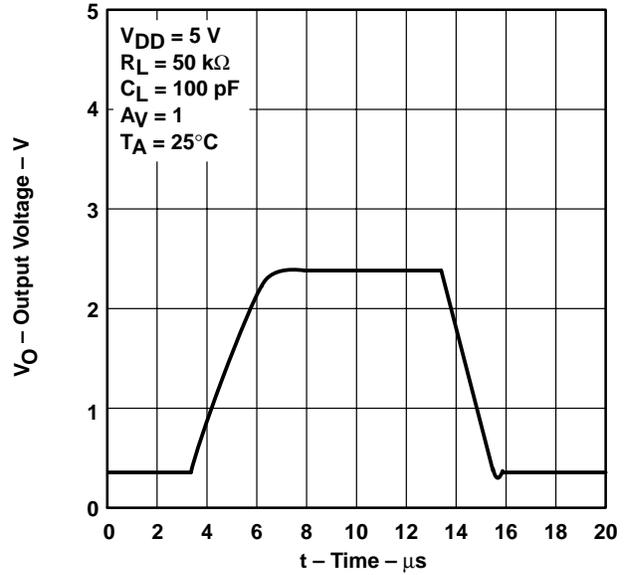


Figure 45

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

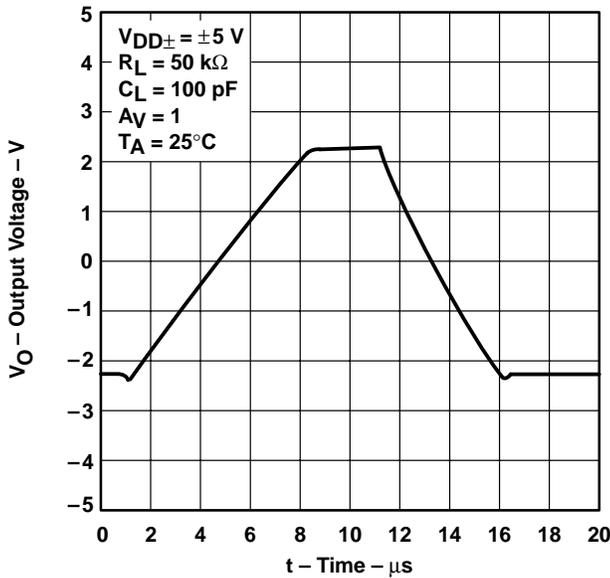


Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†

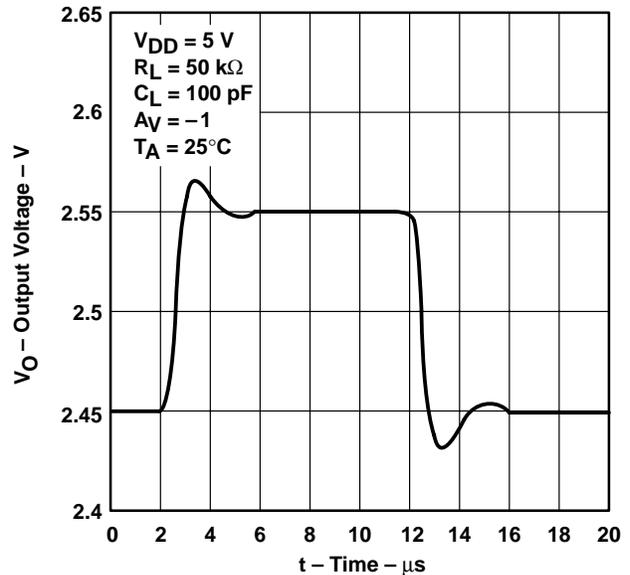


Figure 47

† For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

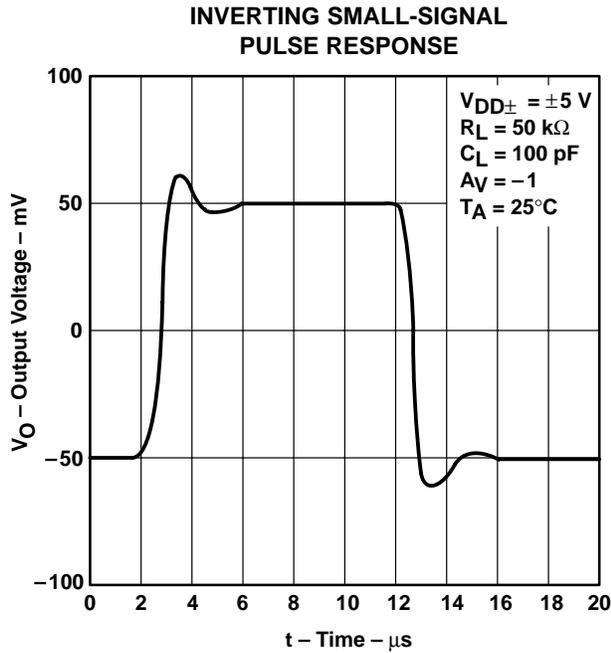


Figure 48

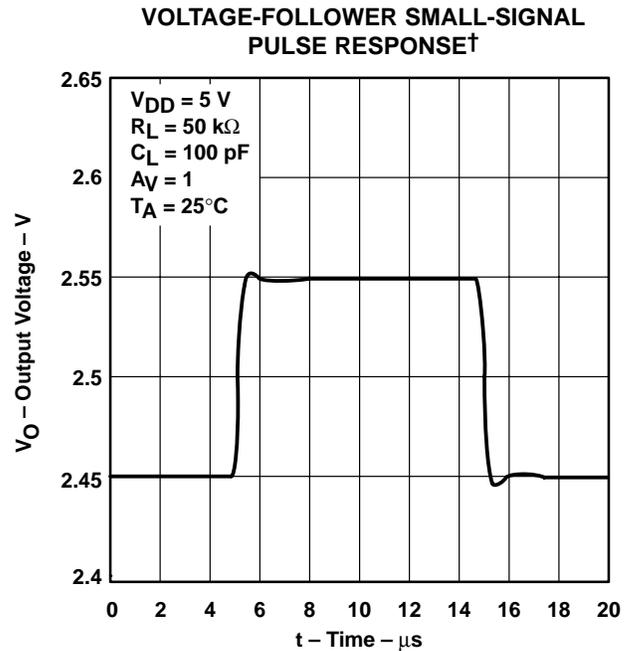


Figure 49

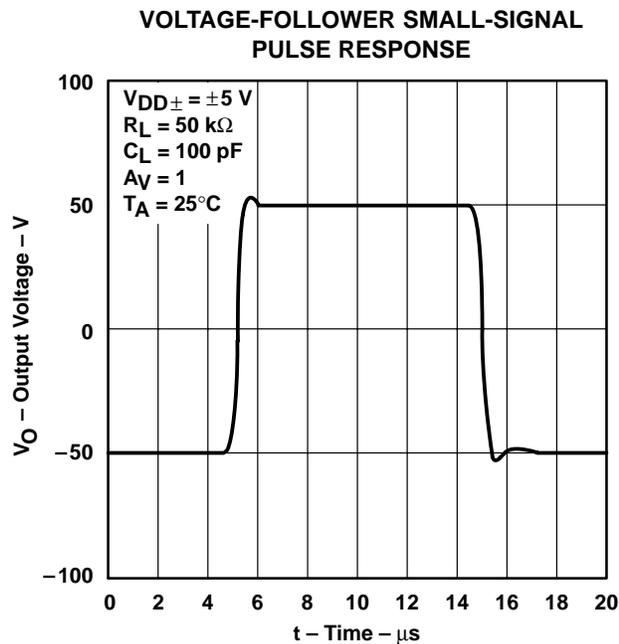


Figure 50

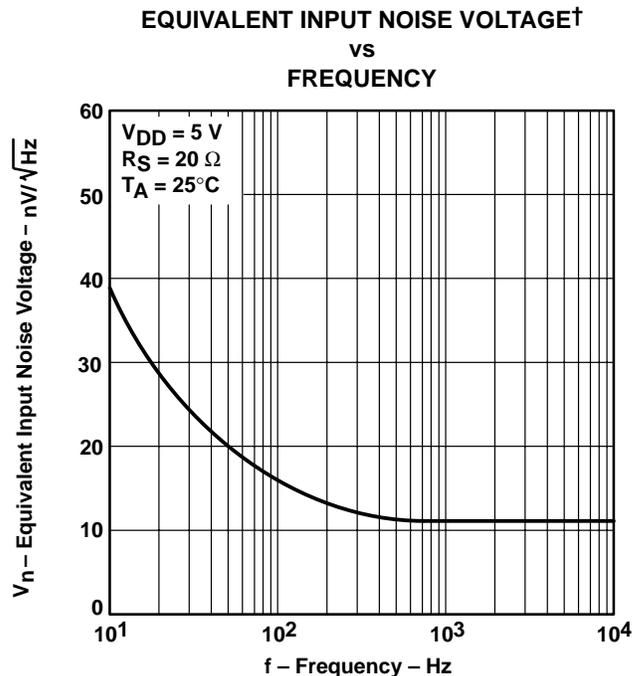


Figure 51

† For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE  
 VS  
 FREQUENCY

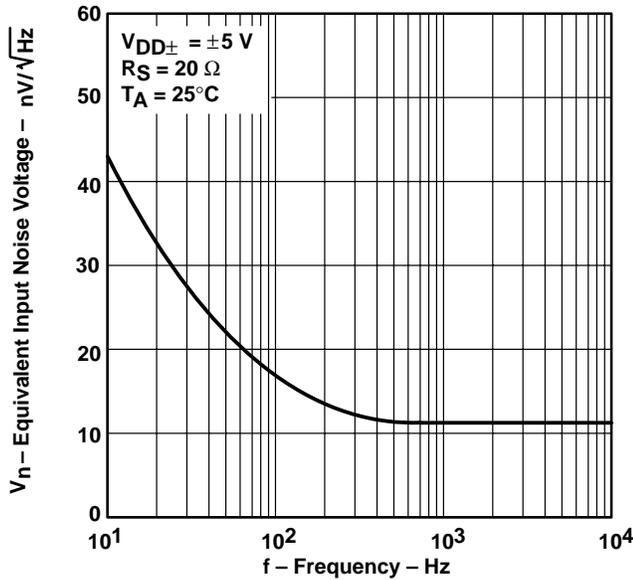


Figure 52

EQUIVALENT INPUT NOISE VOLTAGE OVER  
 A 10-SECOND PERIOD†

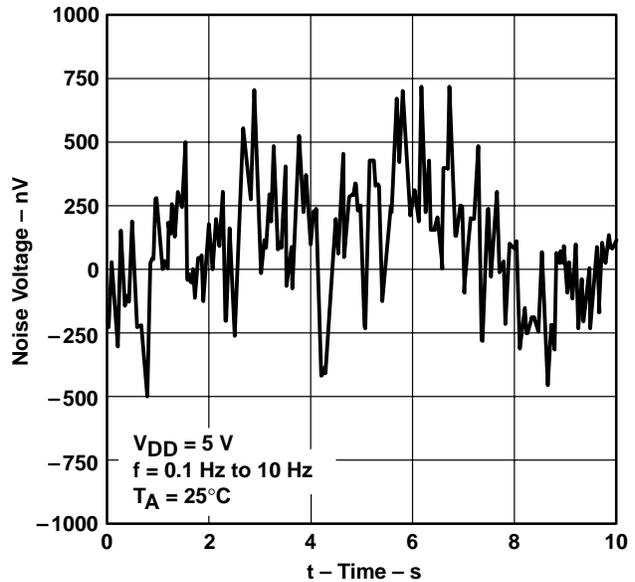


Figure 53

INTEGRATED NOISE VOLTAGE  
 VS  
 FREQUENCY

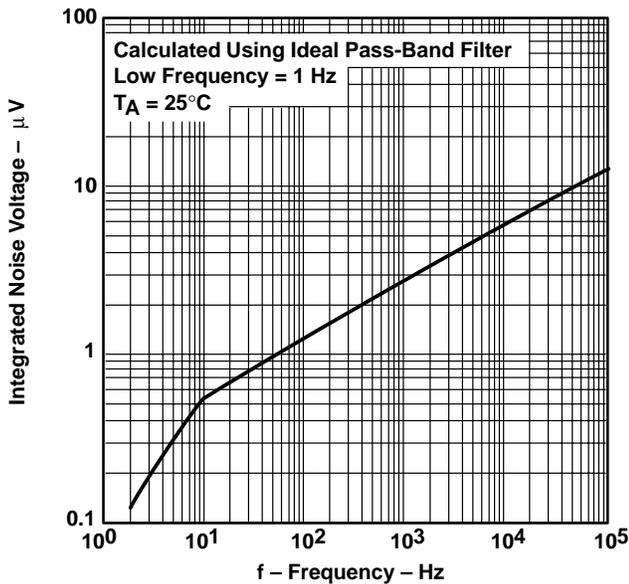


Figure 54

TOTAL HARMONIC DISTORTION PLUS NOISE†  
 VS  
 FREQUENCY

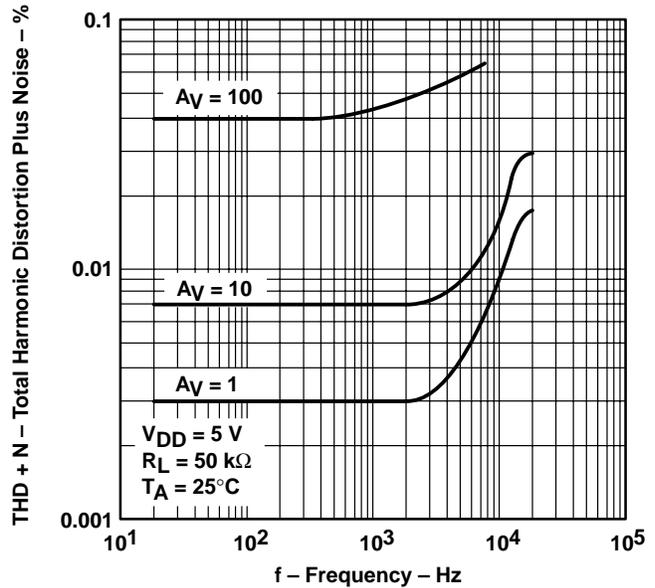


Figure 55

† For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT  
vs  
SUPPLY VOLTAGE

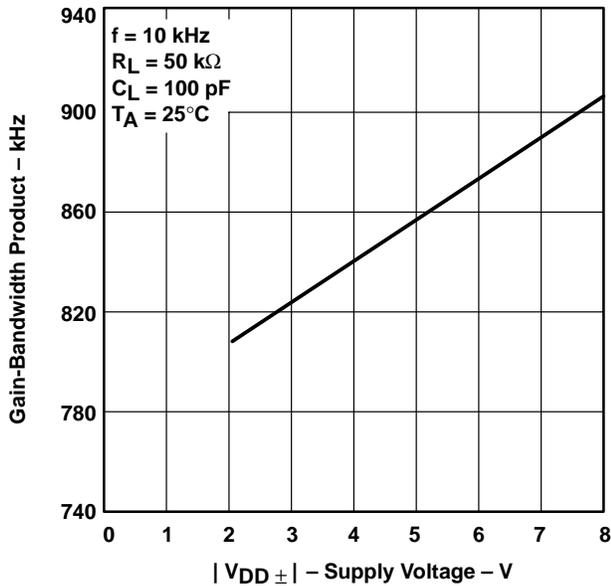


Figure 56

GAIN-BANDWIDTH PRODUCT†‡  
vs  
FREE-AIR TEMPERATURE

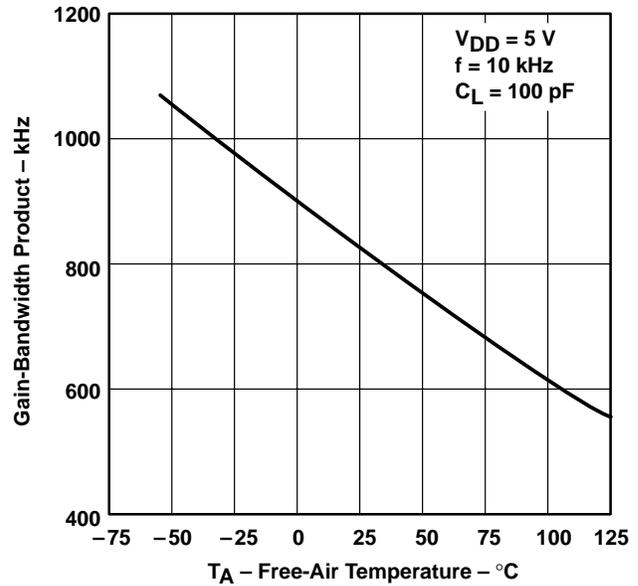


Figure 57

PHASE MARGIN  
vs  
LOAD CAPACITANCE

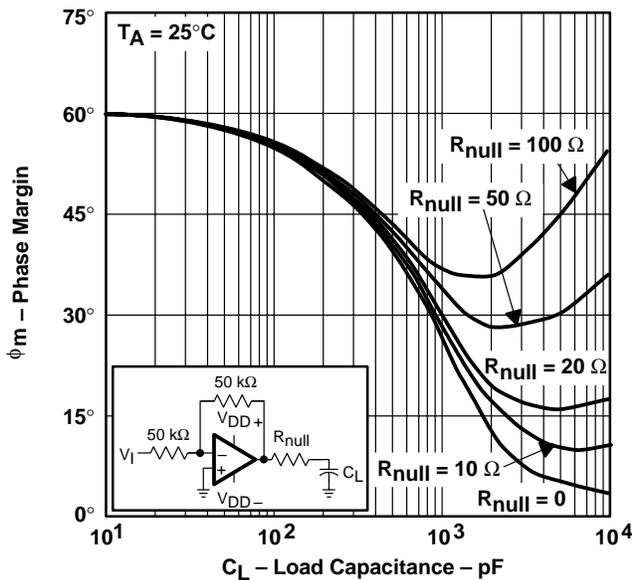


Figure 58

GAIN MARGIN  
vs  
LOAD CAPACITANCE

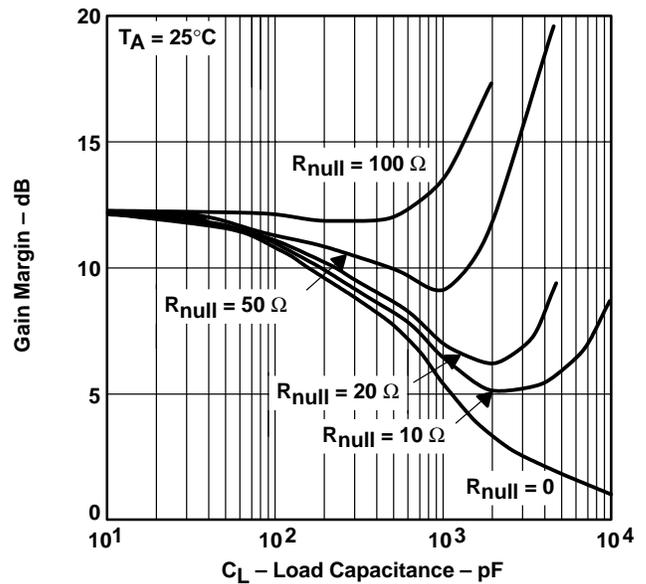
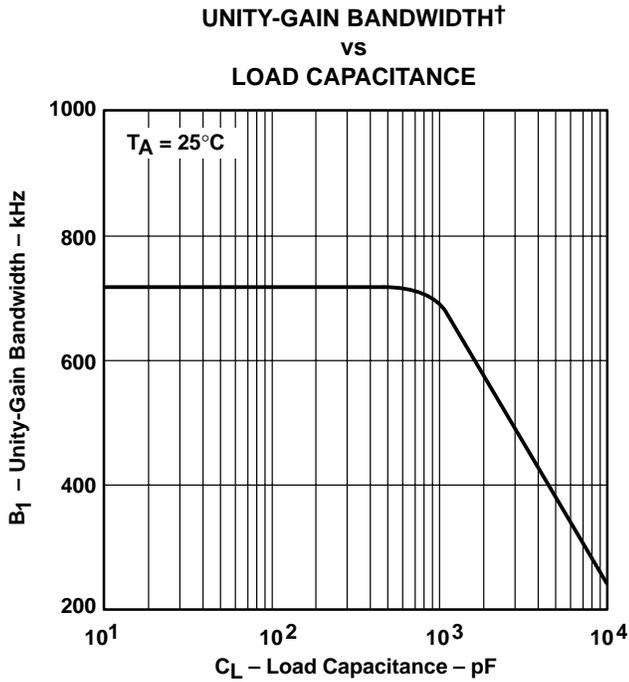


Figure 59

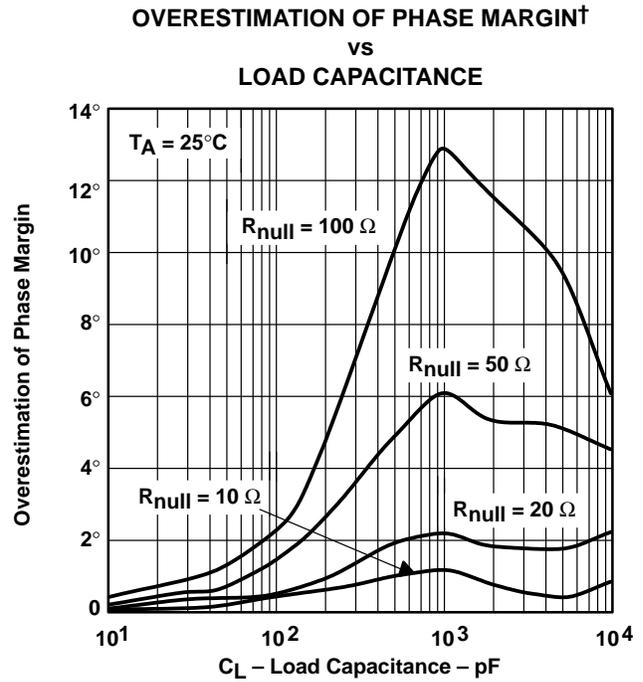
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V.

**TYPICAL CHARACTERISTICS**



**Figure 60**



**Figure 61**

† See application information

## APPLICATION INFORMATION

### driving large capacitive loads

The TLC226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 58 and Figure 59 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins ( $R_{\text{null}} = 0$ ).

A smaller series resistor ( $R_{\text{null}}$ ) at the output of the device (see Figure 62) improves the gain and phase margins when driving large capacitive loads. Figure 58 and Figure 59 show the effects of adding series resistances of 10  $\Omega$ , 20  $\Omega$ , 50  $\Omega$ , and 100  $\Omega$ . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\theta_{m1} = \tan^{-1} \left( 2 \times \pi \times \text{UGBW} \times R_{\text{null}} \times C_L \right) \quad (1)$$

Where :

- $\Delta\theta_{m1}$  = improvement in phase margin
- UGBW = unity-gain bandwidth frequency
- $R_{\text{null}}$  = output series resistance
- $C_L$  = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 60). To use equation 1, UGBW must be approximated from Figure 60.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 61. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{\text{null}}} \quad (2)$$

Where :

- F = factor reducing frequency of pole
- $g_m$  = small-signal output transconductance (typically  $4.83 \times 10^{-3}$  mhos)
- $R_{\text{null}}$  = output series resistance

For the TLC226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with  $C_L$ : at  $C_L = 10$  pF, use 70 MHz, at  $C_L = 1000$  pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation in equation 1 to better approximate the improvement in phase margin.

**APPLICATION INFORMATION**

**driving large capacitive loads (continued)**

$$\Delta\theta_{m2} = \tan^{-1} \left[ \frac{UGBW}{(F \times P_2)} \right] - \tan^{-1} \left( \frac{UGBW}{P_2} \right) \tag{3}$$

Where :

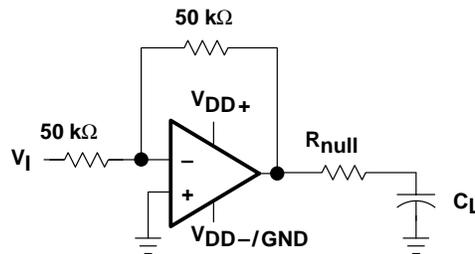
$\Delta\theta_{m2}$  = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation 2

$P_2$  = unadjusted pole (70 MHz @10 pF, 7 MHz @100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.



**Figure 62. Series-Resistance Circuit**

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 63 are generated using the TLC226x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

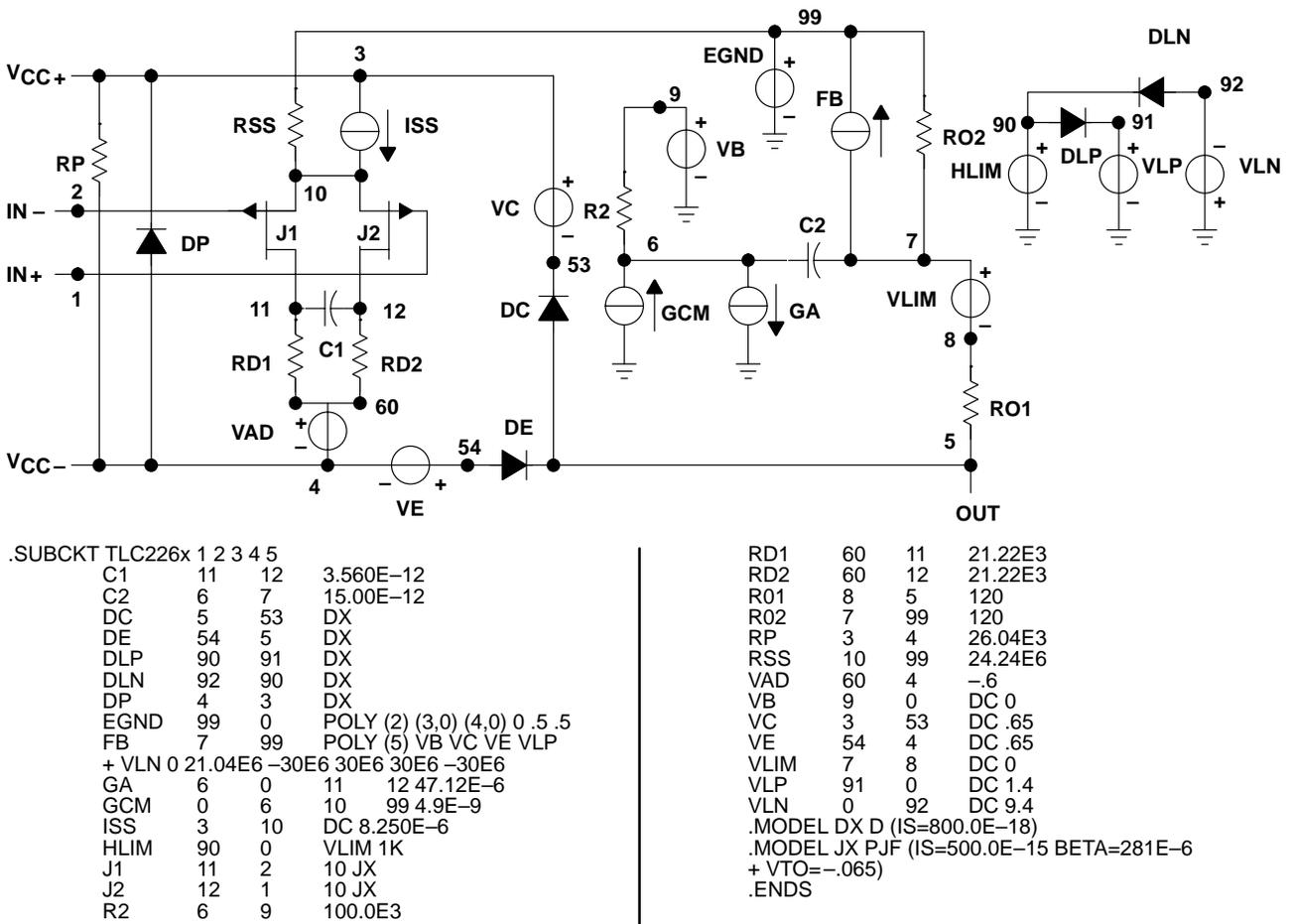


Figure 63. Boyle Macromodel and Subcircuit

*PSpice* and *Parts* are trademarks of MicroSim Corporation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9469201QHA</a>	Active	Production	CFP (U)   10	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9469201QHA TLC2262M
<a href="#">5962-9469203QPA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9469203QPA TLC2262AM
<a href="#">5962-9469204Q2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9469204Q2A TLC2264 AMFKB
<a href="#">5962-9469204QCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9469204QC A TLC2264AMJB
<a href="#">TLC2262AID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI
<a href="#">TLC2262AID.A</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI
<a href="#">TLC2262AIDG4</a>	Active	Production	SOIC (D)   8	75   TUBE	-	Call TI	Call TI	-40 to 125	
<a href="#">TLC2262AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI
<a href="#">TLC2262AIDR.A</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI
<a href="#">TLC2262AIP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2262AI
<a href="#">TLC2262AIP.A</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2262AI
<a href="#">TLC2262AIPW</a>	Obsolete	Production	TSSOP (PW)   8	-	-	Call TI	Call TI	-40 to 125	Y2262A
<a href="#">TLC2262AIPWR</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A
<a href="#">TLC2262AIPWR.A</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A
<a href="#">TLC2262AIPWRG4</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
<a href="#">TLC2262AMJG</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC2262 AMJG
<a href="#">TLC2262AMJG.A</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC2262 AMJG
<a href="#">TLC2262AMJGB</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9469203QPA TLC2262AM
<a href="#">TLC2262AMJGB.A</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9469203QPA TLC2262AM
<a href="#">TLC2262AQD</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	C2262A
<a href="#">TLC2262CD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2262CD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C
<a href="#">TLC2262CDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C
TLC2262CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C
<a href="#">TLC2262CP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2262CP
TLC2262CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2262CP
TLC2262CPE4	Active	Production	PDIP (P)   8	50   TUBE	-	Call TI	Call TI	0 to 70	
<a href="#">TLC2262CPW</a>	Obsolete	Production	TSSOP (PW)   8	-	-	Call TI	Call TI	0 to 70	P2262
<a href="#">TLC2262CPWR</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262
TLC2262CPWR.A	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262
TLC2262CPWRG4	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	-	Call TI	Call TI	0 to 70	
<a href="#">TLC2262ID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2262I
TLC2262ID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262I
TLC2262IDG4	Active	Production	SOIC (D)   8	75   TUBE	-	Call TI	Call TI	See TLC2262ID	
<a href="#">TLC2262IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2262I
TLC2262IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262I
<a href="#">TLC2262IP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2262IP
TLC2262IP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2262IP
<a href="#">TLC2262MUB</a>	Active	Production	CFP (U)   10	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9469201QHA TLC2262M
TLC2262MUB.A	Active	Production	CFP (U)   10	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9469201QHA TLC2262M
<a href="#">TLC2262QD</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	C2262Q
<a href="#">TLC2262QDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262Q
TLC2262QDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262Q
<a href="#">TLC2264AID</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI
TLC2264AID.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI
TLC2264AIDG4	Active	Production	SOIC (D)   14	50   TUBE	-	Call TI	Call TI	-40 to 125	
<a href="#">TLC2264AIDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI
TLC2264AIDR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI
<a href="#">TLC2264AIN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2264AIN
TLC2264AIN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLC2264AIN

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLC2264AIPW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 125	Y2264A
<a href="#">TLC2264AIPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A
TLC2264AIPWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A
TLC2264AIPWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
<a href="#">TLC2264AMFKB</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9469204Q2A TLC2264 AMFKB
TLC2264AMFKB.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9469204Q2A TLC2264 AMFKB
<a href="#">TLC2264AMJB</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9469204QC A TLC2264AMJB
TLC2264AMJB.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9469204QC A TLC2264AMJB
<a href="#">TLC2264AQD</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
TLC2264AQD.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
TLC2264AQD.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
<a href="#">TLC2264AQDRG4</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	PJ2264A
TLC2264AQDRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJ2264A
TLC2264AQDRG4.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJ2264A
<a href="#">TLC2264CD</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C
TLC2264CD.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C
<a href="#">TLC2264CDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C
TLC2264CDR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C
<a href="#">TLC2264CN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2264CN
TLC2264CN.B	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2264CN
<a href="#">TLC2264CPW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	0 to 70	P2264
<a href="#">TLC2264CPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	P2264
TLC2264CPWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLC2264CPWR1G4</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264
<a href="#">TLC2264ID</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC2264I
TLC2264ID.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264I
<a href="#">TLC2264IDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC2264I
TLC2264IDR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264I
<a href="#">TLC2264IN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2264IN
TLC2264IN.B	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2264IN

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

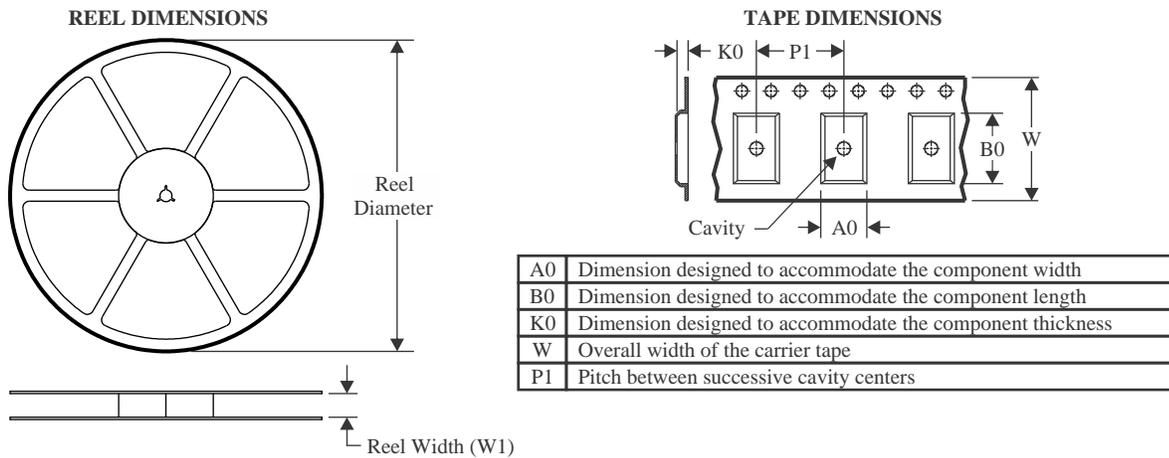
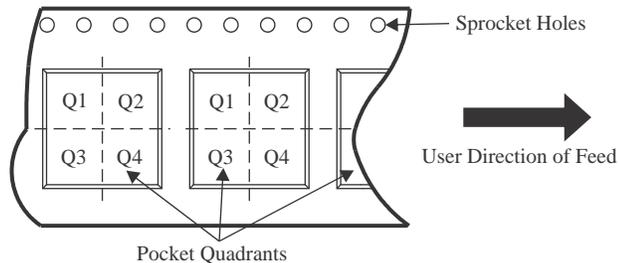
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLC2262, TLC2262A, TLC2262AM, TLC2262M, TLC2264A, TLC2264AM :**

- Catalog : [TLC2262A](#), [TLC2262](#), [TLC2264A](#)
- Automotive : [TLC2264A-Q1](#), [TLC2264A-Q1](#)
- Military : [TLC2262M](#), [TLC2262AM](#), [TLC2264AM](#)

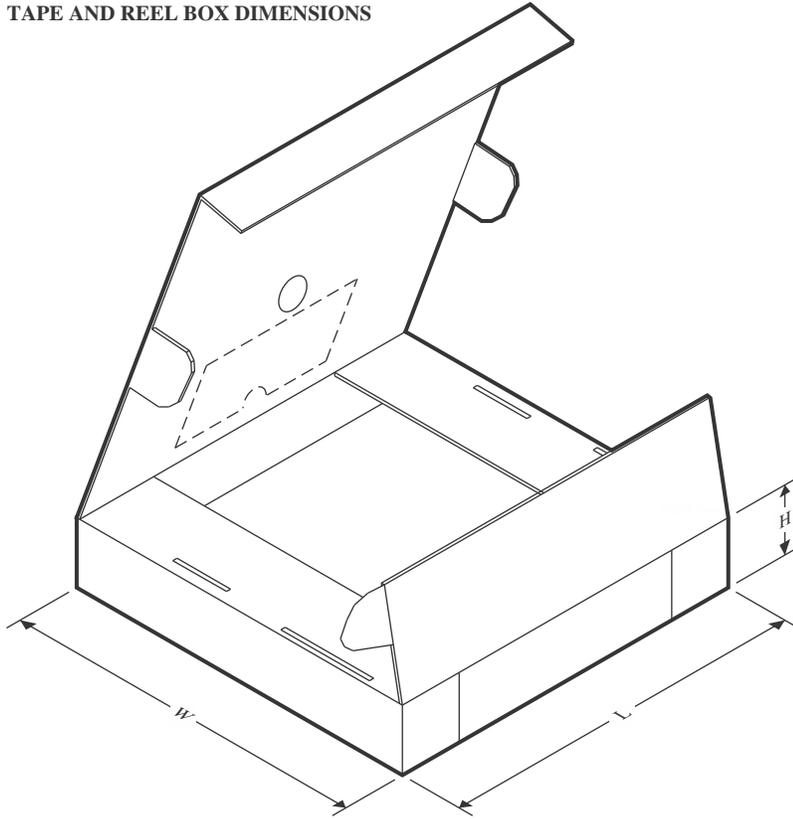
## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


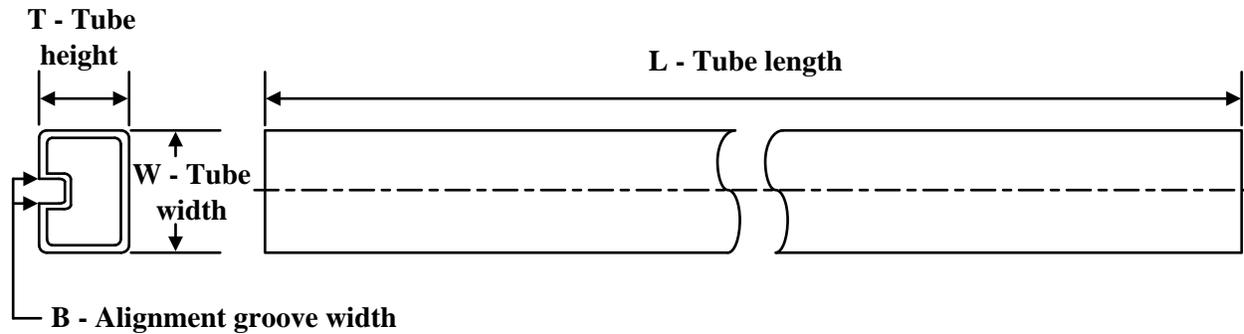
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2262AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLC2264AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264AQDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264CPWR1G4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2262AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2262AIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2262CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2262CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2262IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2262QDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2264AIDR	SOIC	D	14	2500	340.5	336.1	32.0
TLC2264AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2264AQDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TLC2264CDR	SOIC	D	14	2500	353.0	353.0	32.0
TLC2264CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC2264CPWR1G4	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2264IDR	SOIC	D	14	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9469201QHA	U	CFP	10	25	506.98	26.16	6220	NA
5962-9469204Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2262AID	D	SOIC	8	75	507	8	3940	4.32
TLC2262AID	D	SOIC	8	75	505.46	6.76	3810	4
TLC2262AID.A	D	SOIC	8	75	507	8	3940	4.32
TLC2262AID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC2262AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2262AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2262CD	D	SOIC	8	75	507	8	3940	4.32
TLC2262CD.A	D	SOIC	8	75	507	8	3940	4.32
TLC2262CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2262CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2262ID	D	SOIC	8	75	507	8	3940	4.32
TLC2262ID.A	D	SOIC	8	75	507	8	3940	4.32
TLC2262IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2262IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2262MUB	U	CFP	10	25	506.98	26.16	6220	NA
TLC2262MUB.A	U	CFP	10	25	506.98	26.16	6220	NA
TLC2264AID	D	SOIC	14	50	507	8	3940	4.32
TLC2264AID	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264AID.B	D	SOIC	14	50	507	8	3940	4.32
TLC2264AID.B	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2264AIN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC2264AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2264AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2264AQD	D	SOIC	14	50	507	8	3940	4.32
TLC2264AQD.A	D	SOIC	14	50	507	8	3940	4.32
TLC2264AQD.B	D	SOIC	14	50	507	8	3940	4.32

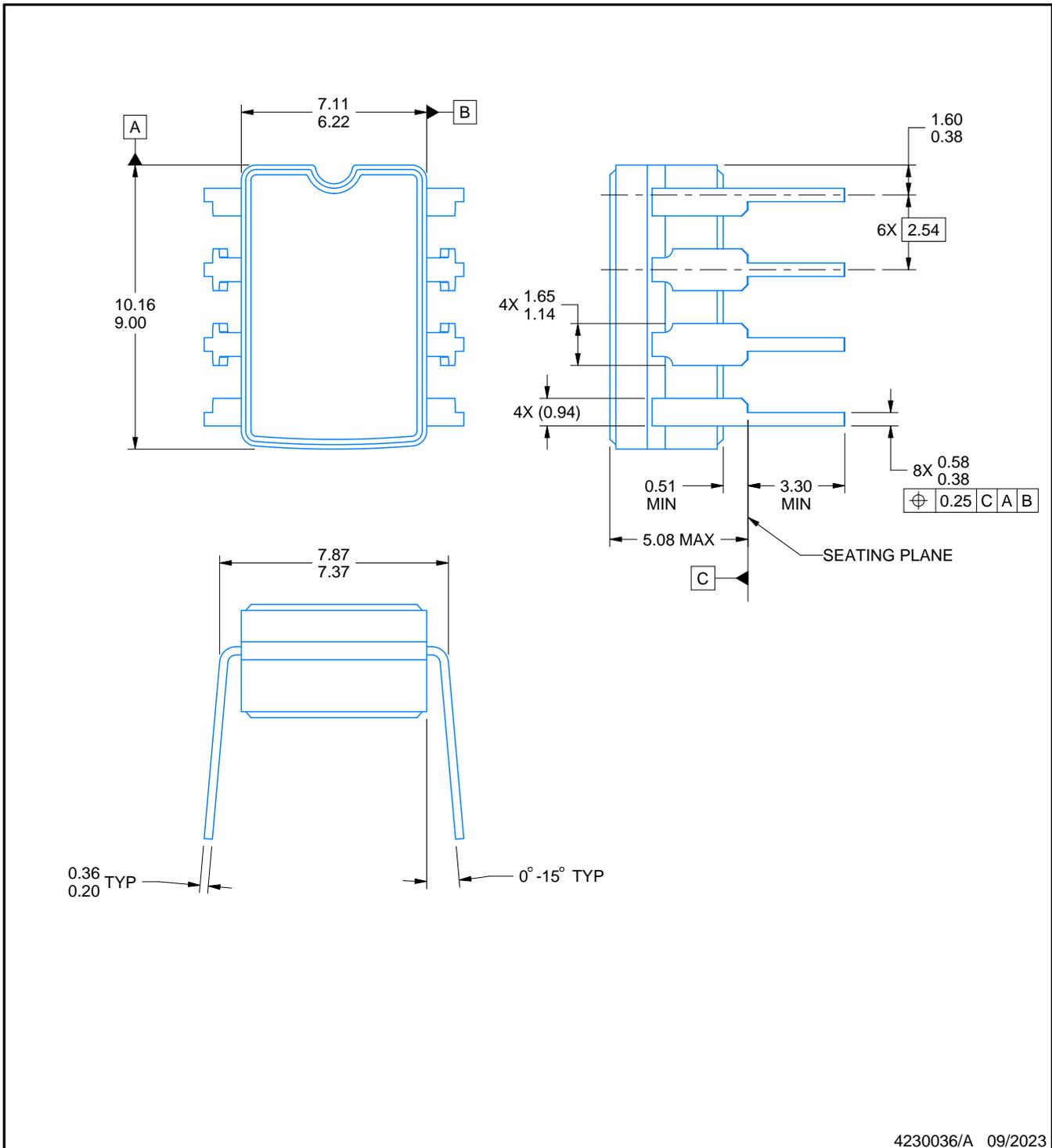
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC2264CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264CD	D	SOIC	14	50	507	8	3940	4.32
TLC2264CD.B	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264CD.B	D	SOIC	14	50	507	8	3940	4.32
TLC2264CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2264CN.B	N	PDIP	14	25	506	13.97	11230	4.32
TLC2264ID	D	SOIC	14	50	507	8	3940	4.32
TLC2264ID.B	D	SOIC	14	50	507	8	3940	4.32
TLC2264IN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2264IN.B	N	PDIP	14	25	506	13.97	11230	4.32

# PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

**NOTES:**

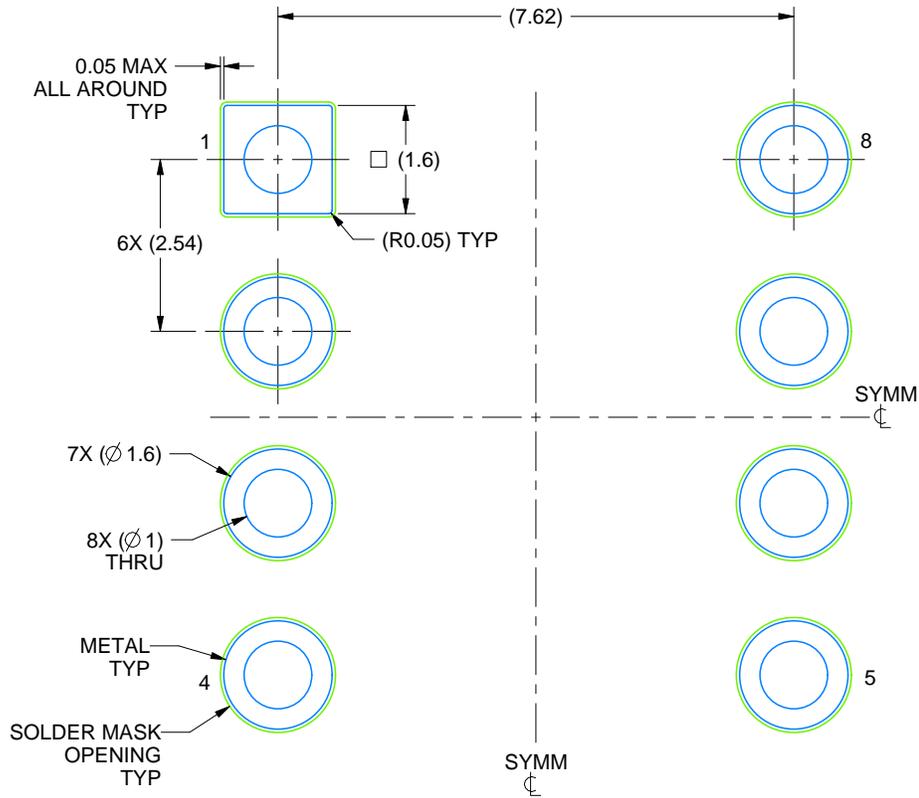
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

# EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE  
NON SOLDER MASK DEFINED  
SCALE: 9X

4230036/A 09/2023



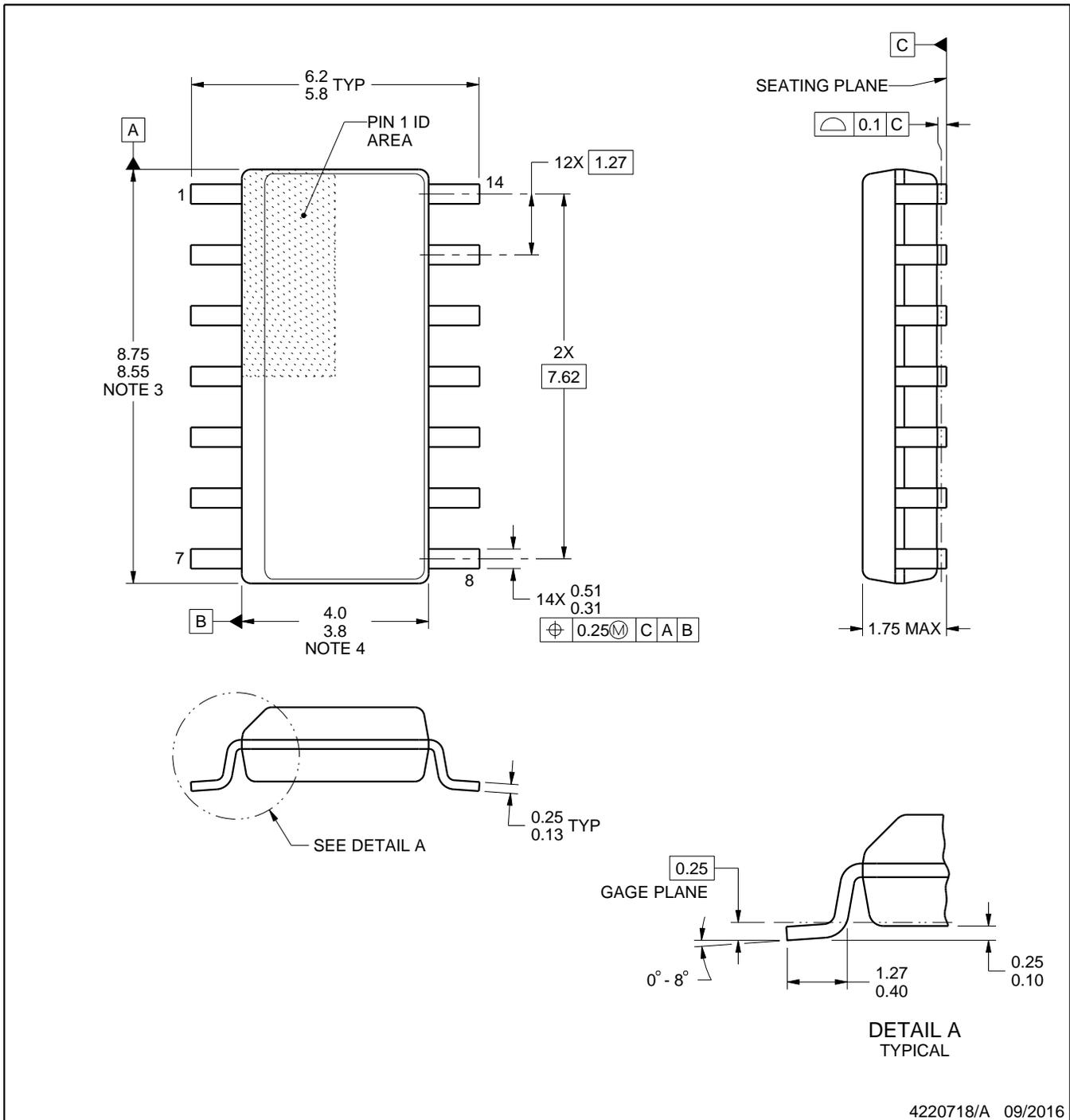
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



**NOTES:**

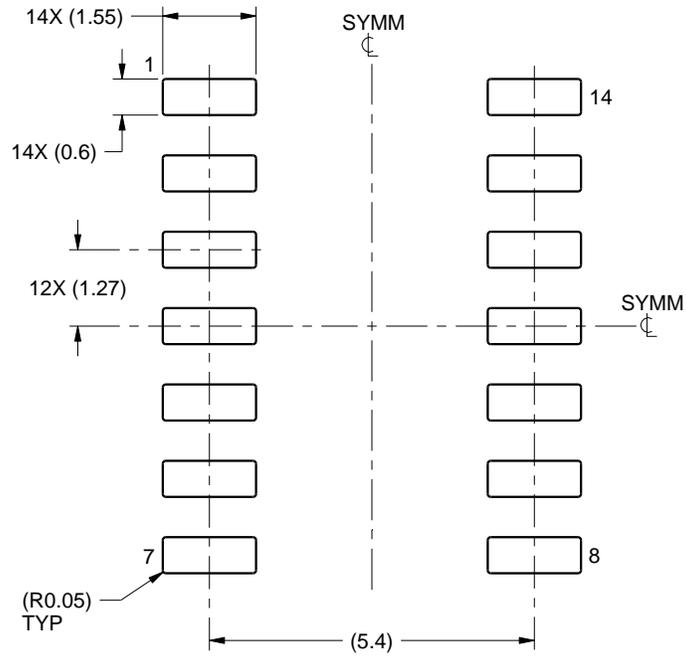
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

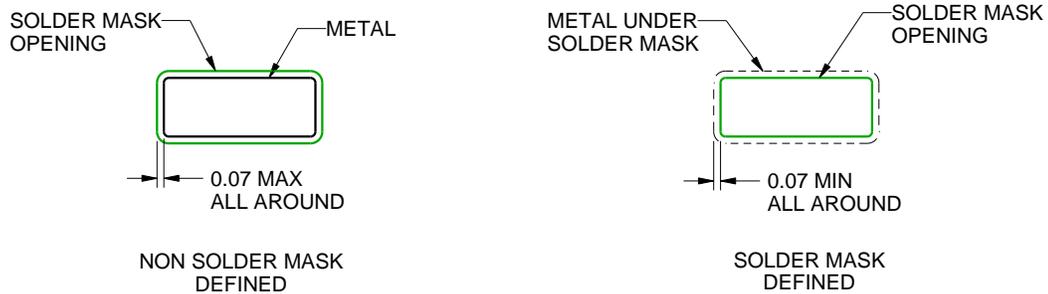
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

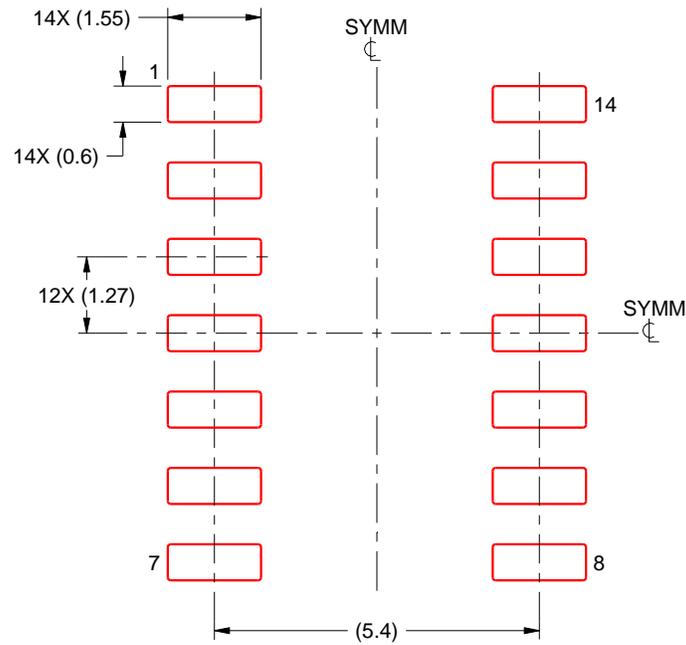
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

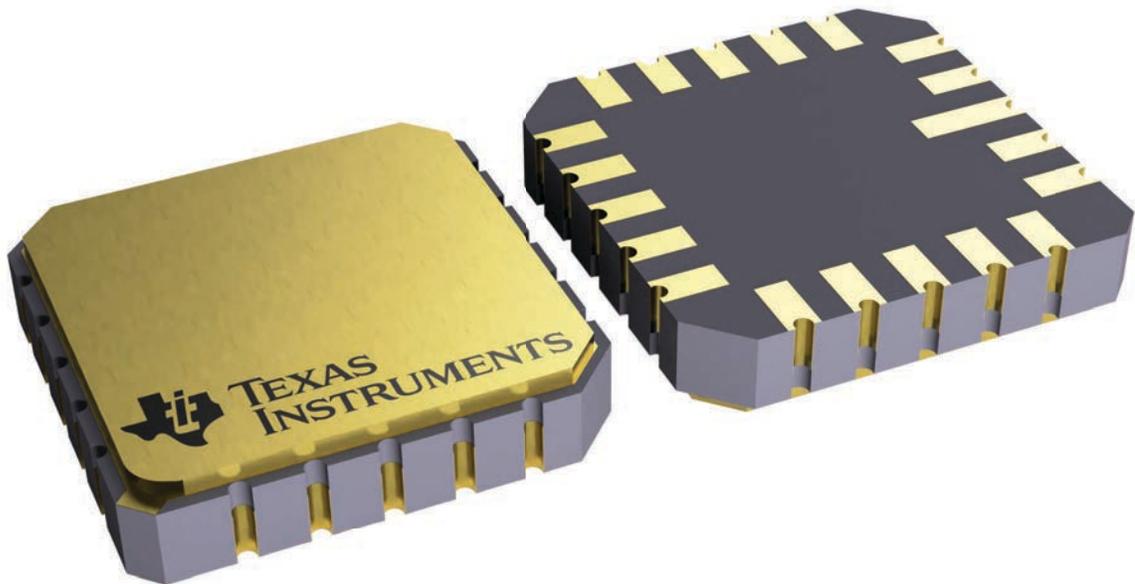
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

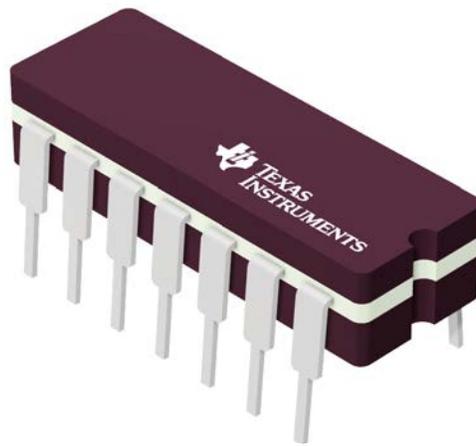
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

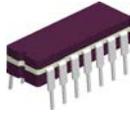
**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

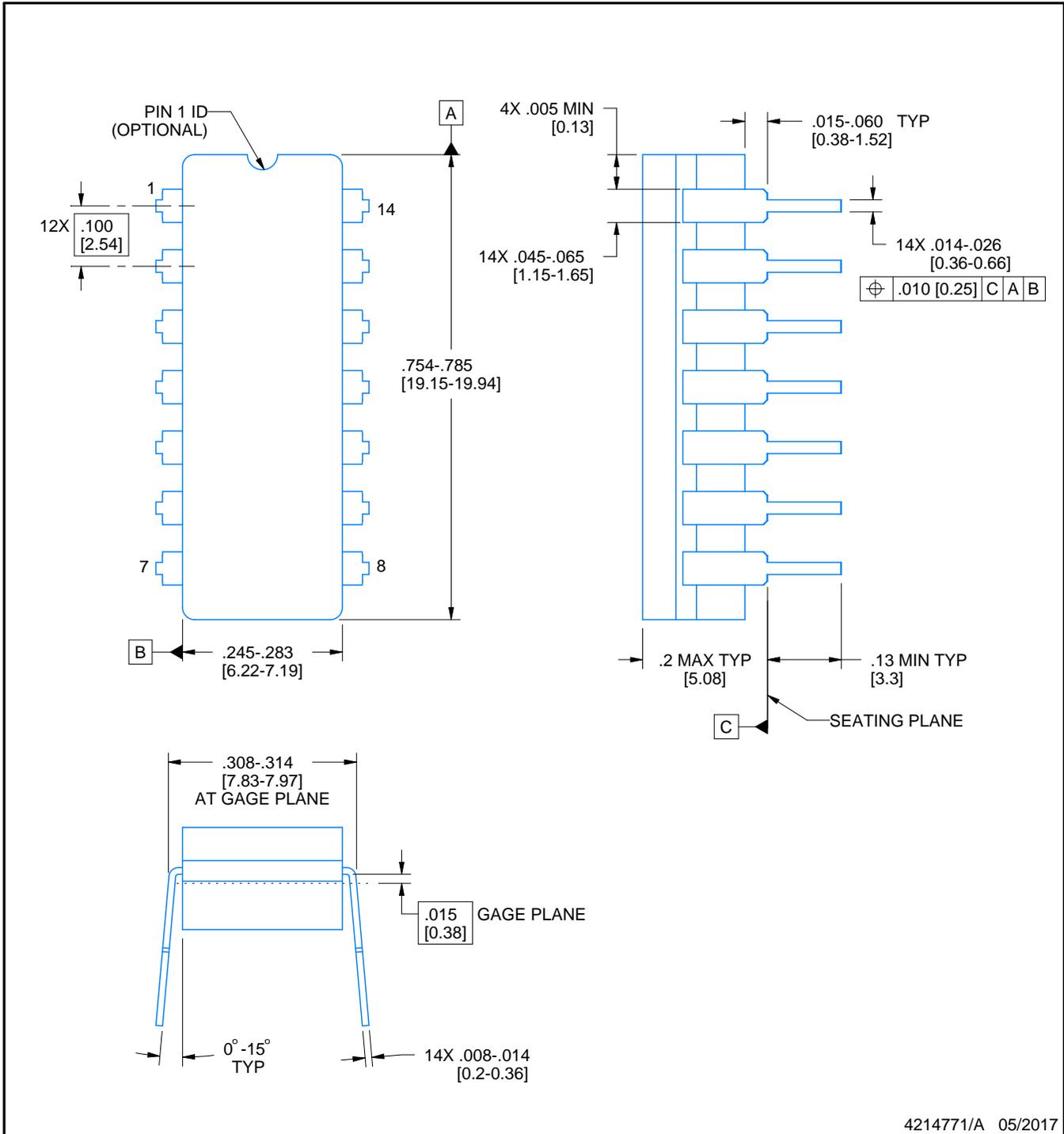
J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

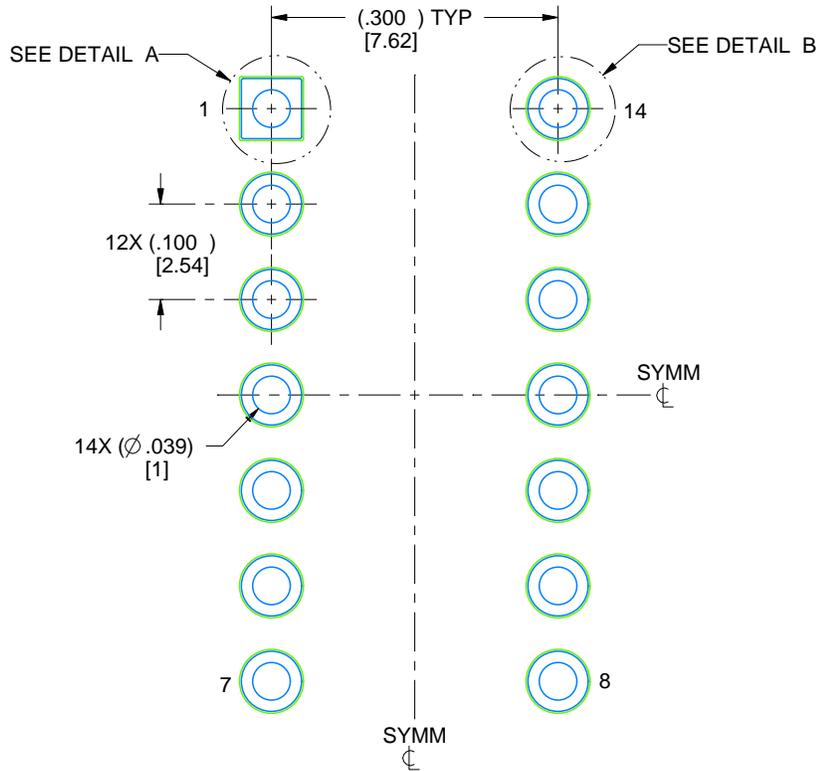
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

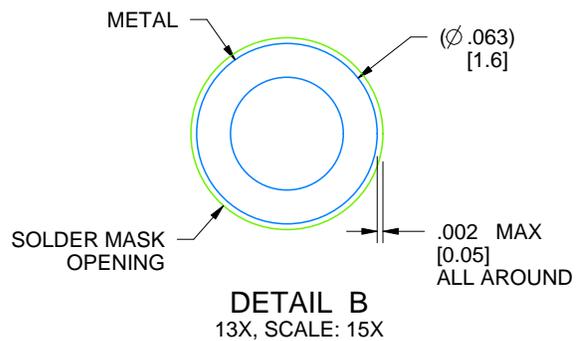
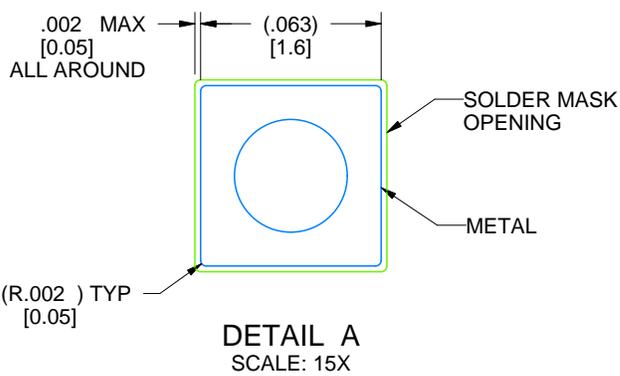
J0014A

CDIP - 5.08 mm max height

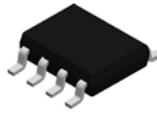
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

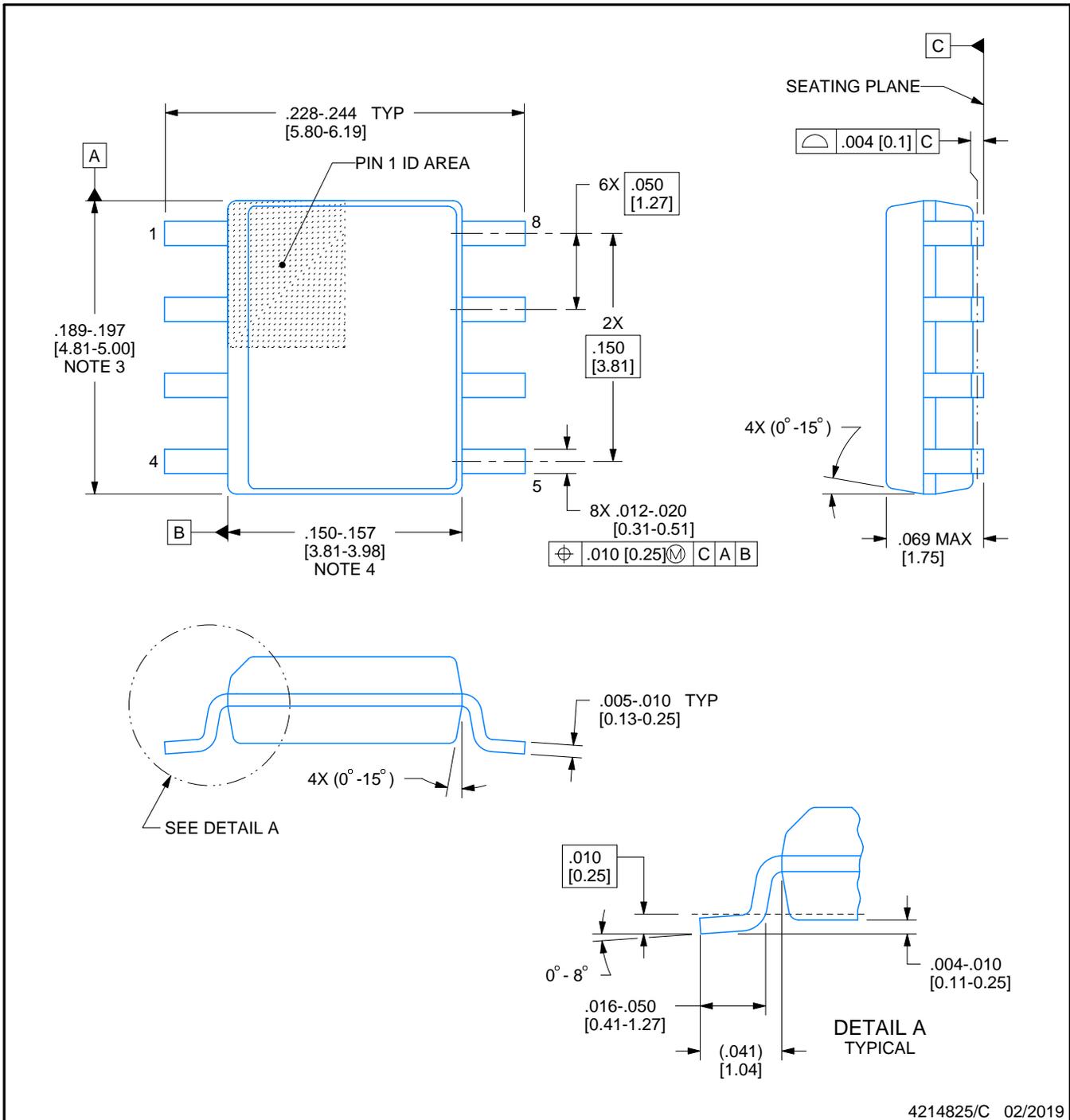


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

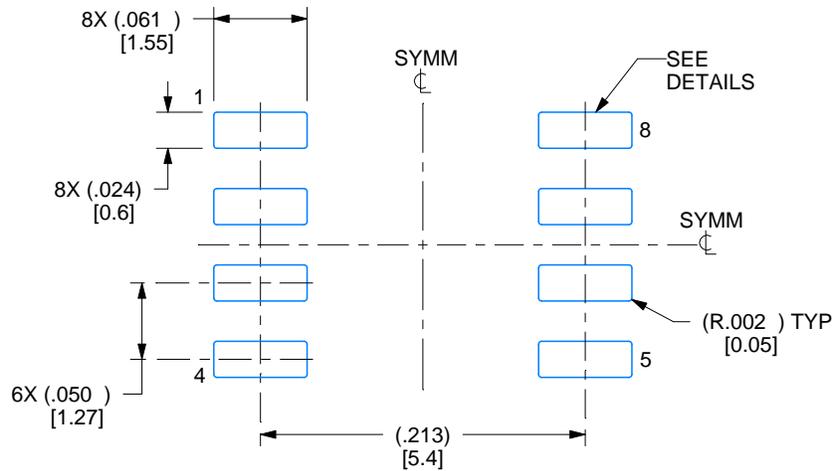
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

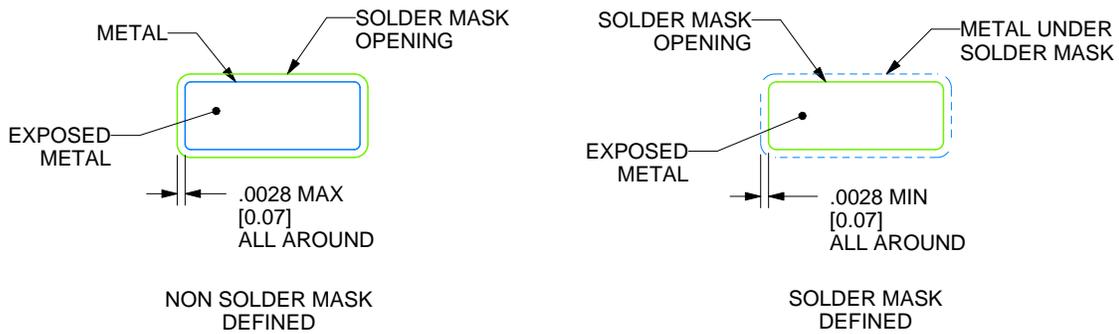
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

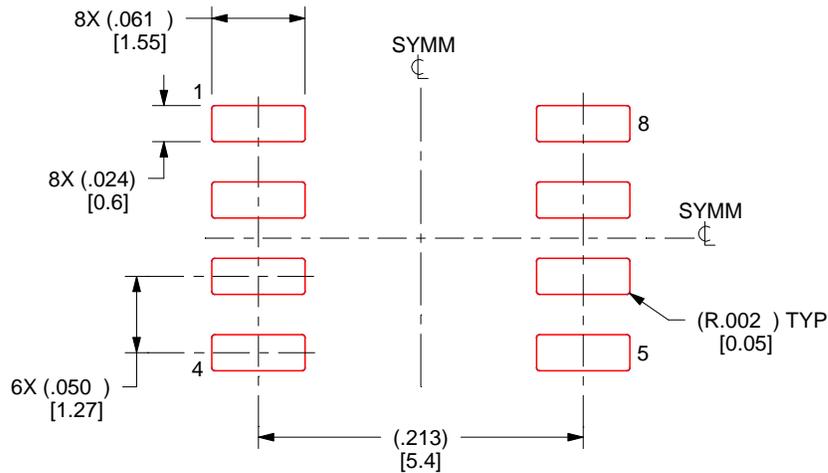
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

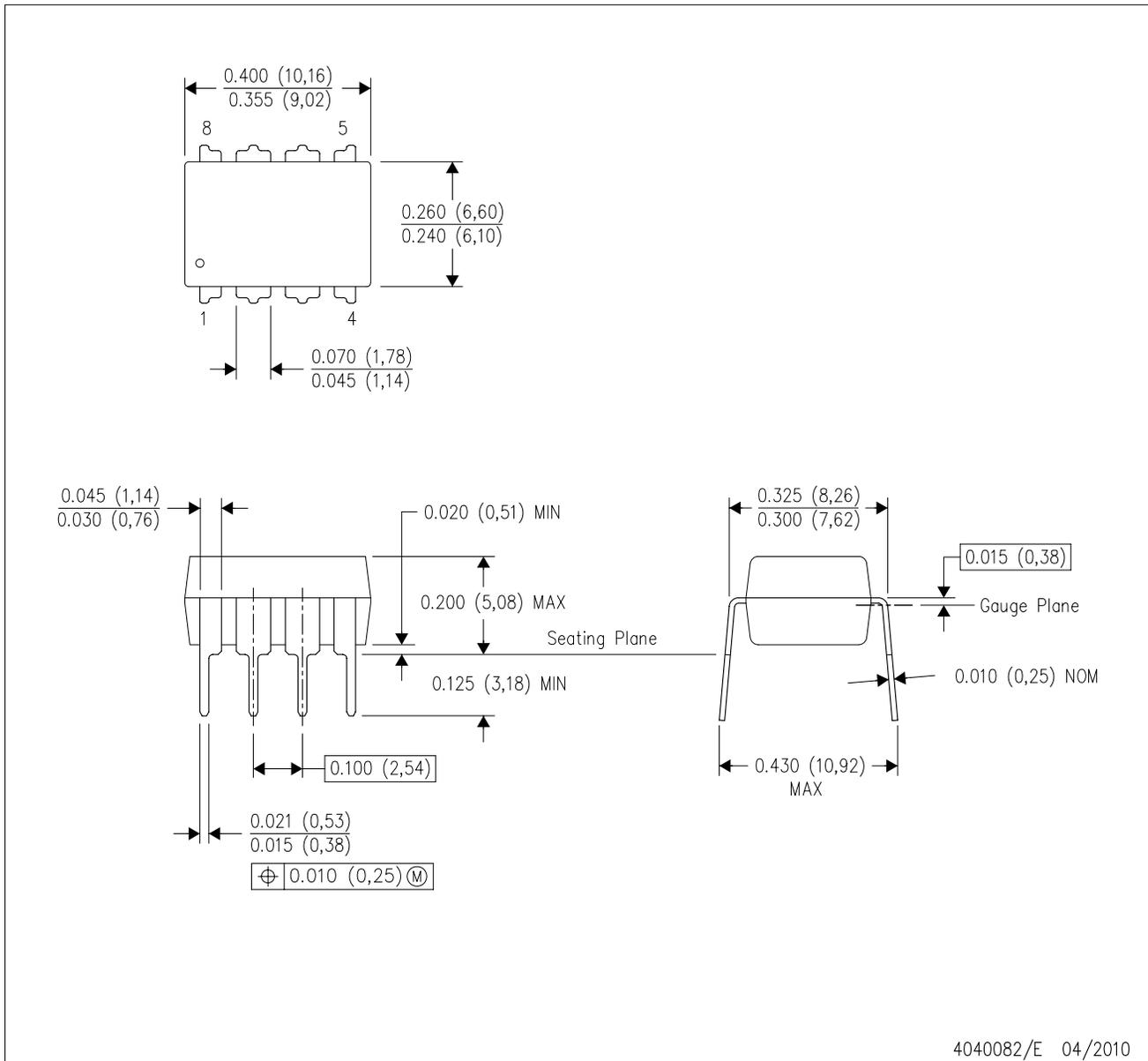
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

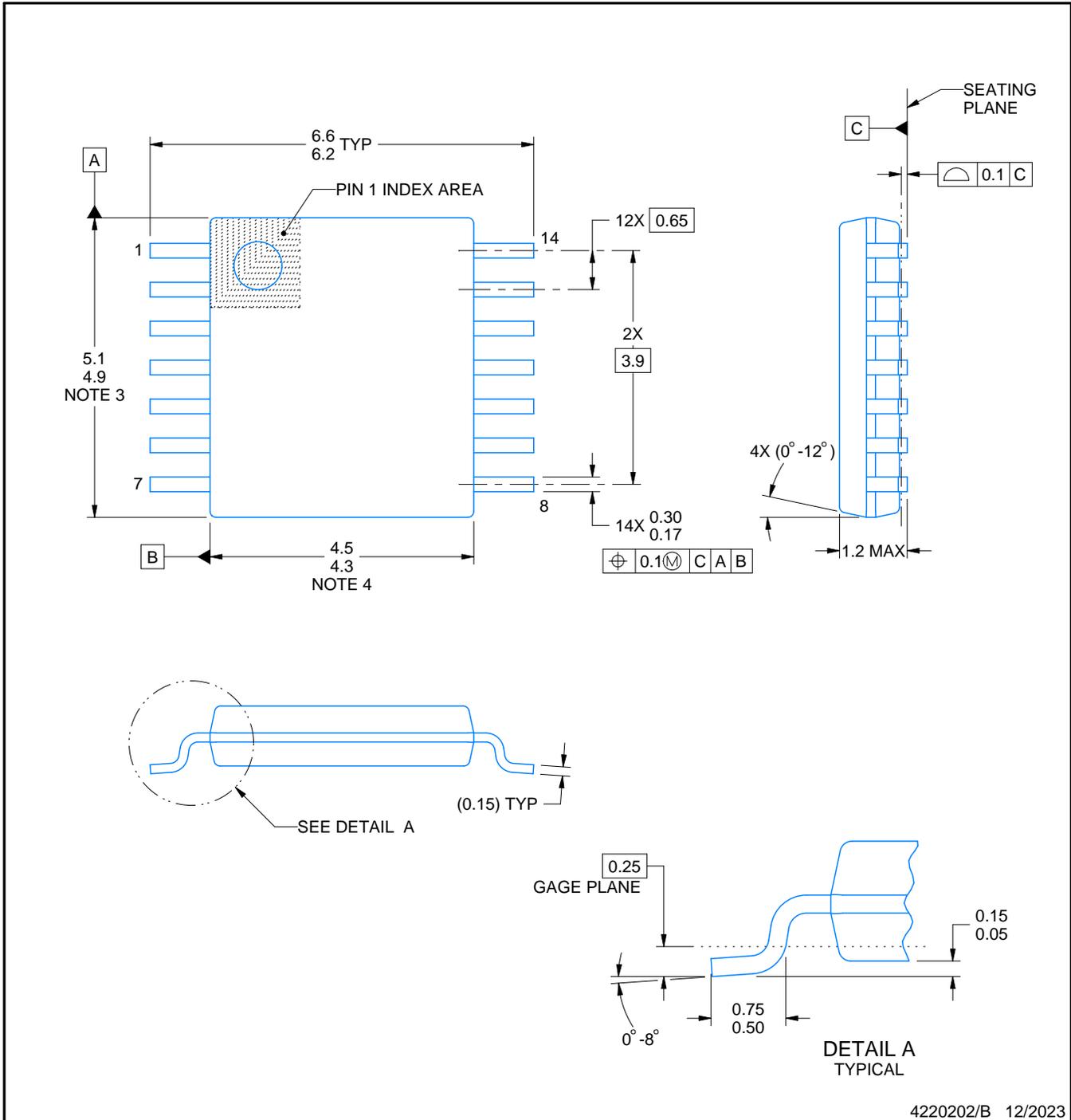
P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.





4220202/B 12/2023

NOTES:

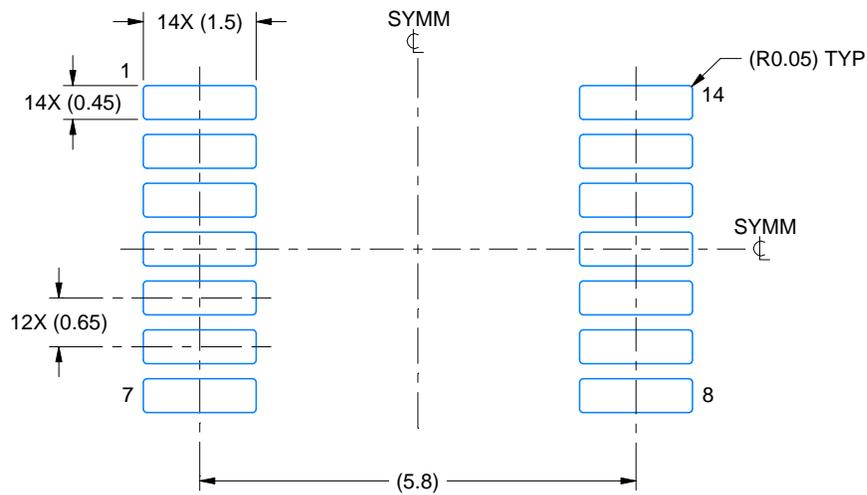
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

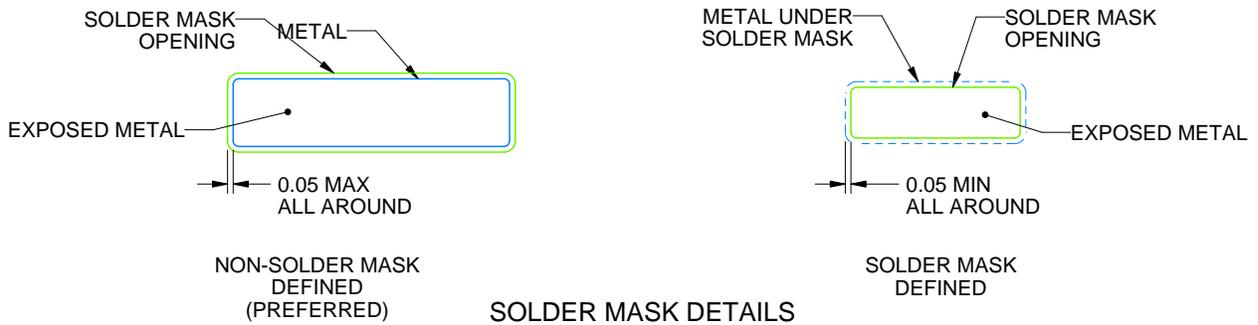
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

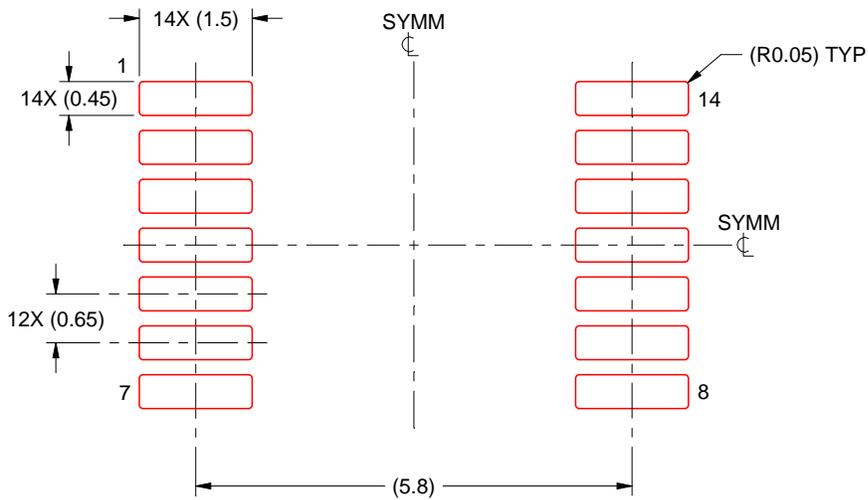
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

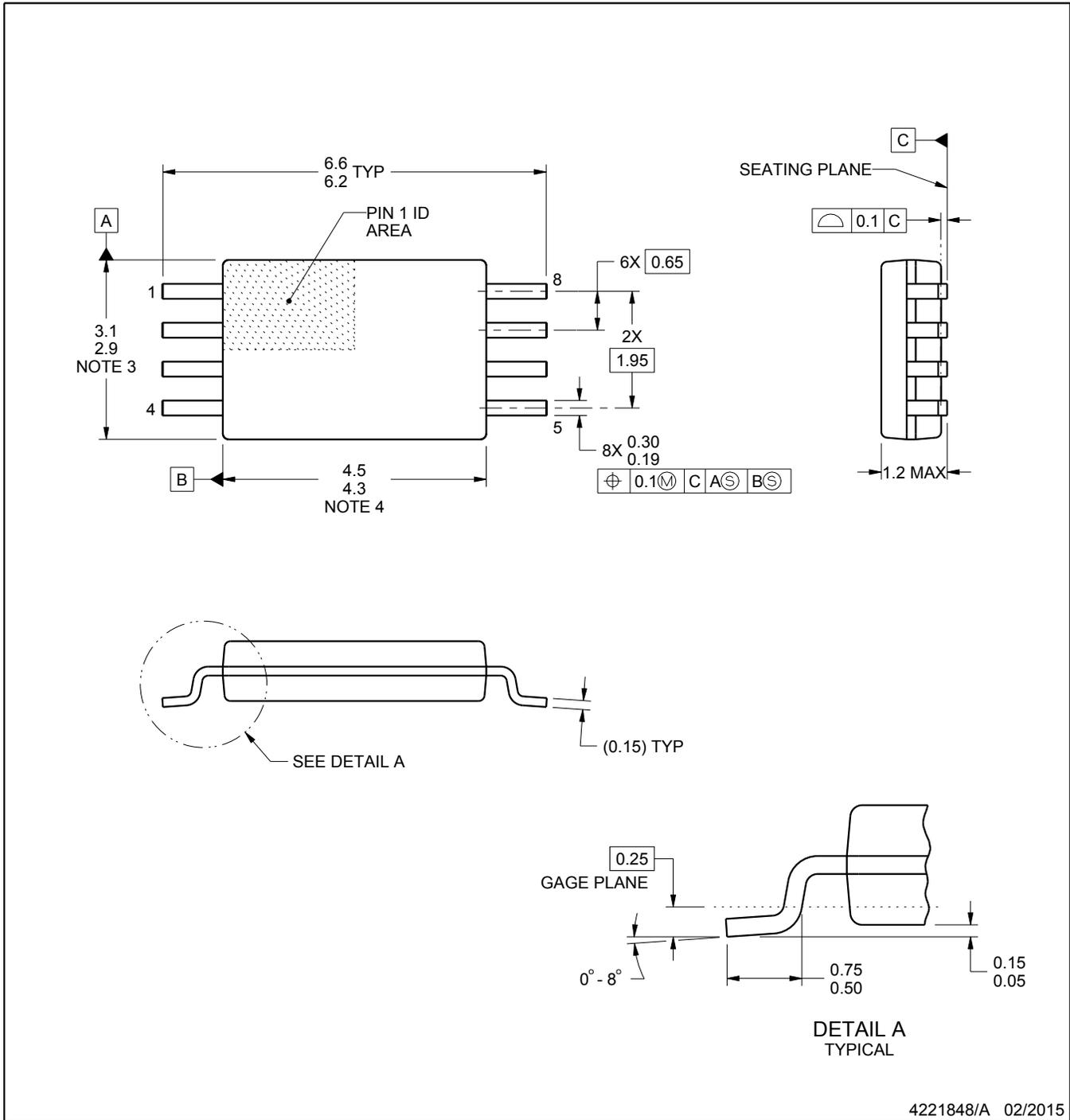
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

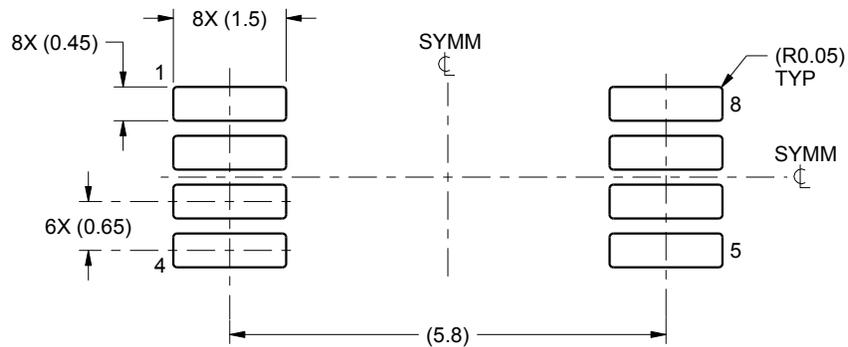
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

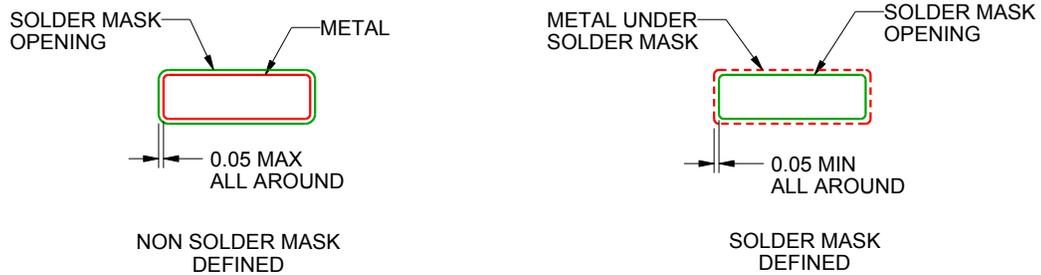
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

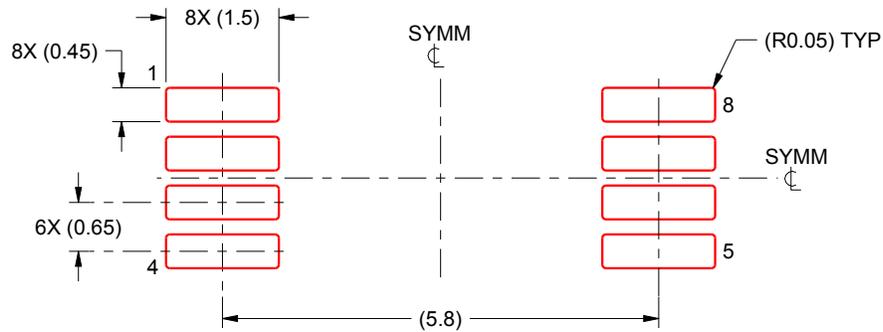
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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