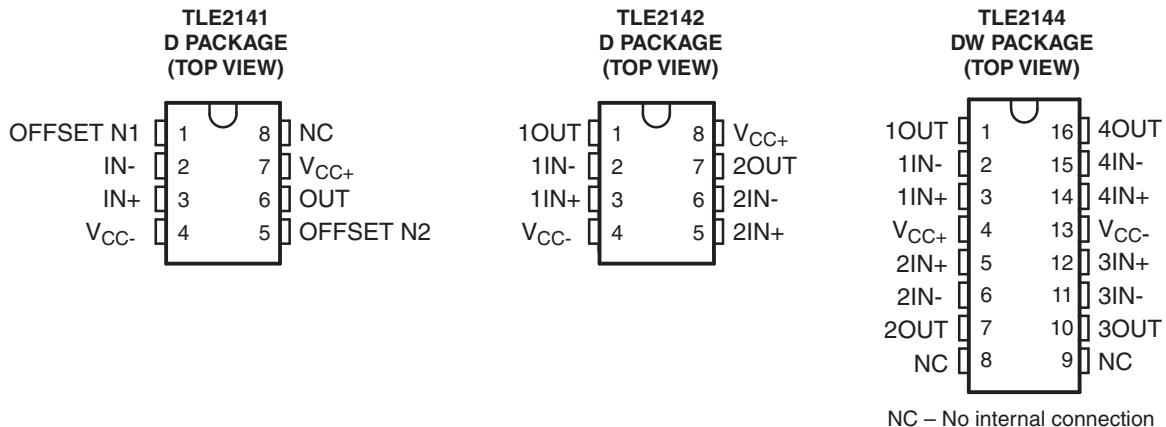


Excilibur™ LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIER

FEATURES

- **Controlled Baseline**
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree⁽¹⁾**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.
- **Low Noise**
 - 10 Hz...15 nV/√Hz
 - 1 kHz...10.5 nV/√Hz
- **10 000-pF Load Capability**
- **20-mA (Min) Short-Circuit Output Current**
- **27-V/μs Slew Rate (Min)**
- **High Gain-Bandwidth Product...5.9 MHz**
- **Low V_{IO} ...900 μV (Max) at 25°C**
- **Single or Split Supply...4 V to 44 V**
- **Fast Settling Time**
 - 340 ns to 0.1%
 - 400 ns to 0.01%
- **Saturation Recovery...150 ns**
- **Large Output Swing... $V_{CC-} + 0.1 V$ to $V_{CC+} - 1 V$**



DESCRIPTION

The TLE214x devices are high-performance, internally compensated operational amplifiers built using the Texas Instruments complementary bipolar Excilibur™ process. They are pin-compatible upgrades to standard industry products.

The design incorporates an input stage that simultaneously achieves low audio-band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Excilibur is a trademark of Texas Instruments.

The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE214x are useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 900-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between $V_{CC-} - 0.3$ V to $V_{CC+} - 1.8$ V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of $V_{CC-} - 0.1$ V to $V_{CC+} - 1$ V under light current-loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

Both versions can also be used as comparators. Differential inputs of $V_{CC±}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

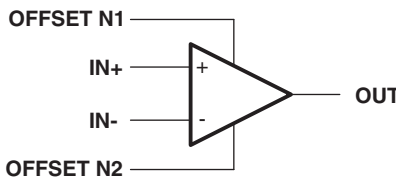
The TLE214x devices are available in industry-standard 8-pin and 16-pin small-outline packages. The devices are characterized for operation from -55°C to 125°C.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾			ORDERABLE PART NUMBER	TOP-SIDE MARKING
	Single	SOIC – D (8 pin)	Reel of 2500		
-55°C to 125°C	Dual	SOIC – D (8 pin)	Reel of 2500	TLE2142MDREP ⁽³⁾	TBD
	Quad	SOIC – DW (16 pin)	Reel of 2000	TLE2144MDWREP ⁽³⁾	TBD

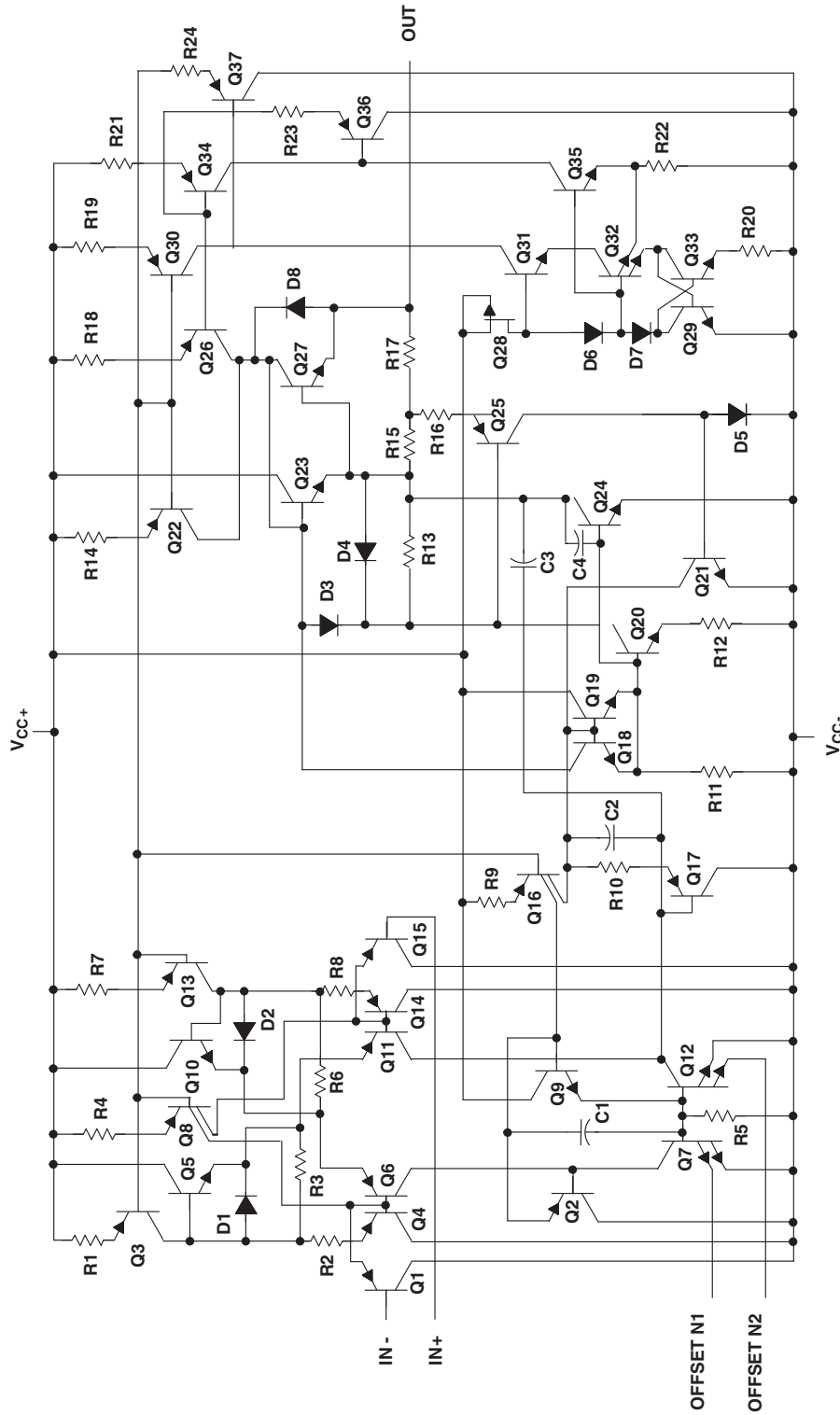
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) Product Preview. Contact your TI sales representative for availability.

SYMBOL



- A. OFFSET N1 and OFFSET N2 are available only on the TLE2141.

EQUIVALENT SCHEMATIC



A. OFFSET N1 and OFFSET N2 are available only on the TLE2141.

DEVICE COMPONENT COUNT

COMPONENT	TLE2141	TLE2142	TLE2144
Transistors	46	65	130
Resistors	24	43	86
Diodes	8	14	28
Capacitors	4	8	16
Epi-FET	1	1	2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC+}	Supply voltage ⁽²⁾		22 V
V_{CC-}	Supply voltage		-22 V
V_{ID}	Differential input voltage ⁽³⁾		±44 V
V_I	Input voltage range (any input)		V_{CC+} V to $(V_{CC-} - 0.3)$ V
I_I	Input current (each input)		±1 mA
I_O	Output current		±80 mA
	Total current into V_{CC+}		80 mA
	Total current out of V_{CC-}		80 mA
	Duration of short-circuit current at (or below) 25°C ⁽⁴⁾		Unlimited
θ_{JA}	Package thermal impedance ⁽⁵⁾⁽⁶⁾	D package	97.1°C/W
		DW package	57.3°C/W
T_A	Operating free-air temperature range		-55°C to 125 °C
T_{stg}	Storage temperature range ⁽⁷⁾		-65°C to 150 °C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
- (3) Differential voltages are at IN+ with respect to IN-. Excessive current flows, if input, are brought below $V_{CC-} - 0.3$ V.
- (4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
- (5) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.
- (7) Long-term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced product packaging.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		±2	±22	V
V_{IC}	Common-mode input voltage	$V_{CC} = 5$ V	0	2.7	V
		$V_{CC\pm} = \pm 15$ V	-15	12.7	
T_A	Operating free-air temperature		-55	125	°C

TLE2141 ELECTRICAL CHARACTERISTICS

 $V_{CC} = 5\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	TLE2141			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		225	1400	μV
		Full range			2100	
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		8	100	nA
		Full range			250	
I_{IB} Input bias current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		-0.8	-2	μA
		Full range			-2.3	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3	-0.3 to 3.2		V
		Full range	0 to 2.7	-0.3 to 2.9		
V_{OH} High-level output voltage	$I_{OH} = -150\ \mu\text{A}$ $I_{OH} = -1.5\text{ mA}$ $I_{OH} = -15\text{ mA}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -10\text{ mA}$	25°C		3.9	4.1	V
				3.8	4	
				3.2	3.7	
		Full range		3.75		
				3.65		
				3.25		
V_{OL} Low-level output voltage	$I_{OL} = 150\ \mu\text{A}$ $I_{OL} = 1.5\text{ mA}$ $I_{OL} = 15\text{ mA}$ $I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 1\text{ mA}$ $I_{OL} = 10\text{ mA}$	25°C		75	125	mV
				150	225	
				1.2	1.6	
		Full range		200		
				250		
				1.25		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_O = 1\text{ V}$ to -1.5 V	25°C	50	220	V/mV	
		Full range	5			
r_i Input resistance		25°C		70	$\text{M}\Omega$	
c_i Input capacitance		25°C		2.5	pF	
z_o Open-loop output impedance	$f = 1\text{ MHz}$	25°C		30	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$, $R_S = 50\ \Omega$	25°C	85	118	dB	
		Full range	80			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$, $R_S = 50\ \Omega$	25°C	90	106	dB	
		Full range	85			
I_{CC} Supply current	$V_O = 2.5\text{ V}$, No load, $V_{IC} = 2.5\text{ V}$	25°C		3.4	4.4	mA
		Full range			4.6	

 (1) Full range is -55°C to 125°C .

TLE2141 OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2141			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$			45		V/ μs
SR-	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$			42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 2.5-V step	To 0.1%		0.16		μs
			To 0.01%		0.22		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 10 Hz		15		nV/ $\sqrt{\text{Hz}}$
			f = 1 kHz		10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92		$\text{pA}/\sqrt{\text{Hz}}$
		f = 1 kHz			0.5		
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }3\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 2$, f = 10 kHz			0.0052		%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$			5.9		MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$, f = 100 kHz			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 1$			660		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$			57		$^\circ$

(1) R_L and C_L terminated to 2.5 V.

TLE2141 ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 15\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	TLE2141			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		200	900	μV
		Full range			1700	
α_{VIO} Temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		7	100	nA
		Full range			250	
I_{IB} Input bias current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		-0.7	-1.5	μA
		Full range			-1.8	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13	-15.3 to 13.2		V
		Full range	-15 to 12.7	-15.3 to 12.9		
V_{OM+} Maximum positive peak output voltage swing	$I_O = -150\ \mu\text{A}$ $I_O = -1.5\ \text{mA}$ $I_O = -15\ \text{mA}$ $I_O = -100\ \mu\text{A}$ $I_O = -1\ \text{mA}$ $I_O = -10\ \text{mA}$	25°C		13.8	14.1	V
				13.7	14	
				13.1	13.7	
		Full range		13.7		
				13.6		
				13.1		
V_{OM-} Maximum negative peak output voltage swing	$I_O = 150\ \mu\text{A}$ $I_O = 1.5\ \text{mA}$ $I_O = 15\ \text{mA}$ $I_O = 100\ \mu\text{A}$ $I_O = 1\ \text{mA}$ $I_O = 10\ \text{mA}$	25°C		-14.7	-14.9	V
				-14.5	-14.8	
				-13.4	-13.8	
		Full range		-14.6		
				-14.5		
				-13.4		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 2\ \text{k}\Omega$	25°C	100	450	V/mV	
		Full range	20			
r_i Input resistance		25°C		65	$\text{M}\Omega$	
c_i Input capacitance		25°C		2.5	pF	
z_o Open-loop output impedance	$f = 1\ \text{MHz}$	25°C		30	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min}), R_S = 50\ \Omega$	25°C	85	108	dB	
		Full range	80			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}, R_S = 50\ \Omega$	25°C	90	106	dB	
		Full range	85			
I_{OS} Short-circuit output current	$V_O = 0$	25°C	$V_{ID} = 1\ \text{V}$	-25	-50	mA
			$V_{ID} = -1\ \text{V}$	20	31	
I_{CC} Supply current	$V_O = 0, \text{No load}, V_{IC} = 2.5\ \text{V}$	25°C		3.5	4.5	mA
		Full range			4.7	

 (1) Full range is -55°C to 125°C .

TLE2141 OPERATING CHARACTERISTICS

$V_{CC} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2141			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		27	45		V/ μs
SR-	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		27	42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 10-V step	To 0.1%	0.34			μs
			To 0.01%	0.4			
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 10 Hz	15			nV/ $\sqrt{\text{Hz}}$
			f = 1 kHz	10.5			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		0.48			μV
		f = 0.1 Hz to 10 Hz		0.51			
I_n	Equivalent input noise current	f = 10 Hz		1.89			pA/ $\sqrt{\text{Hz}}$
		f = 1 kHz		0.47			
THD+N	Total harmonic distortion plus noise	$V_{O(PP)} = 20\text{ V}$, $R_L = 2\text{ k}\Omega$, $A_{VD} = 10$, f = 10 kHz		0.01			%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		6			MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, f = 100 kHz		5.9			MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 20\text{ V}$, $A_{VD} = 1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		668			kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		58			$^\circ$

TLE2142 ELECTRICAL CHARACTERISTICS

 $V_{CC} = 5\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLE2142			UNIT		
			MIN	TYP	MAX			
V_{IO} Input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		220	1900	μV		
		Full range			2600			
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$		
I_{IO} Input offset current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		8	100	nA		
		Full range			200			
I_{IB} Input bias current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		-0.8	-2	μA		
		Full range			-2.3			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3	-0.3 to 3.2		V		
		Full range	0 to 2.7	-0.3 to 2.9				
V_{OH} High-level output voltage	$I_{OH} = -150\ \mu\text{A}$ $I_{OH} = -1.5\text{ mA}$ $I_{OH} = -15\text{ mA}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -10\text{ mA}$	25°C		3.9	4.1	V		
				3.8	4			
				3.4	3.7			
		Full range		3.75				
				3.65				
				3.45				
V_{OL} Low-level output voltage	$I_{OL} = 150\ \mu\text{A}$ $I_{OL} = 1.5\text{ mA}$ $I_{OL} = 15\text{ mA}$ $I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 1\text{ mA}$ $I_{OL} = 10\text{ mA}$	25°C			75	125	mV	
					150	225		
					1.2	1.4		
		Full range					200	mV
							250	
							1.25	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_O = 1\text{ V to }1.5\text{ V}$	25°C	50	220		V/mV		
		Full range	5					
r_i Input resistance		25°C		70		M Ω		
c_i Input capacitance		25°C		2.5		pF		
z_o Open-loop output impedance	$f = 1\text{ MHz}$	25°C		30		Ω		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$, $R_S = 50\ \Omega$	25°C	85	118		dB		
		Full range	80					
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$, $R_S = 50\ \Omega$	25°C	90	106		dB		
		Full range	85					
I_{CC} Supply current	$V_O = 2.5\text{ V}$, No load, $V_{IC} = 2.5\text{ V}$	25°C		6.6	8.8	mA		
		Full range			9.2			

 (1) Full range is -55°C to 125°C .

TLE2142 OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2142			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$			45		V/ μs
SR–	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$			42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 2.5-V step	To 0.1%		0.16		μs
			To 0.01%		0.22		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 10\text{ Hz}$		15		nV/ $\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$		10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$			0.48		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$			0.51		
I_n	Equivalent input noise current	$f = 10\text{ Hz}$			1.92		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			0.5		
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }3\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 2$, $f = 10\text{ kHz}$			0.0052		%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}$			5.9		MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 1$, $C_L = 100\text{ pF}$			660		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}$			57		°

(1) R_L terminated at 2.5 V.

TLE2142 ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 15\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLE2142			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		290	1200	μV
		Full range			2000	
α_{VIO} Temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		7	100	nA
		Full range			250	
I_{IB} Input bias current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		-0.7	-1.5	μA
		Full range			-1.8	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13	-15.3 to 13.2		V
		Full range	-15 to 12.7	-15.3 to 12.9		
V_{OM+} Maximum positive peak output voltage swing	$I_O = -150\ \mu\text{A}$ $I_O = -1.5\ \text{mA}$ $I_O = -15\ \text{mA}$ $I_O = -100\ \mu\text{A}$ $I_O = -1\ \text{mA}$ $I_O = -10\ \text{mA}$	25°C		13.8	14.1	V
				13.7	14	
				13.3	13.7	
		Full range		13.7		
				13.6		
				13.3		
V_{OM-} Maximum negative peak output voltage swing	$I_O = 150\ \mu\text{A}$ $I_O = 1.5\ \text{mA}$ $I_O = 15\ \text{mA}$ $I_O = 100\ \mu\text{A}$ $I_O = 1\ \text{mA}$ $I_O = 10\ \text{mA}$	25°C		-14.7	-14.9	V
				-14.5	-14.8	
				-13.4	-13.8	
		Full range		-14.6		
				-14.5		
				-13.4		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 2\ \text{k}\Omega$	25°C	100	450	V/mV	
		Full range	20			
r_i Input resistance		25°C		65	$\text{M}\Omega$	
c_i Input capacitance		25°C		2.5	pF	
z_o Open-loop output impedance	$f = 1\ \text{MHz}$	25°C		30	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min}), R_S = 50\ \Omega$	25°C	85	108	dB	
		Full range	80			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}, R_S = 50\ \Omega$	25°C	90	106	dB	
		Full range	85			
I_{OS} Short-circuit output current	$V_O = 0$	25°C	$V_{ID} = 1\ \text{V}$	-25	-50	mA
			$V_{ID} = -1\ \text{V}$	20	31	
I_{CC} Supply current	$V_O = 0, \text{No load}, V_{IC} = 2.5\ \text{V}$	25°C		6.9	9	mA
		Full range			9.4	

 (1) Full range is -55°C to 125°C .

TLE2142 OPERATING CHARACTERISTICS

$V_{CC} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2142			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		27	45		V/ μs
SR-	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		27	42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 10-V step	To 0.1%	0.34			μs
			To 0.01%	0.4			
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 10\text{ Hz}$	15			nV/ $\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	10.5			
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		0.48			μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		0.51			
I_n	Equivalent input noise current	$f = 10\text{ Hz}$		1.89			$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.47			
THD+N	Total harmonic distortion plus noise	$V_{O(PP)} = 20\text{ V}$, $R_L = 2\text{ k}\Omega$, $A_{VD} = 10$, $f = 10\text{ kHz}$		0.01			%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		6			MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$		5.9			MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 20\text{ V}$, $A_{VD} = 1$, $R_L = 2\text{ k}\Omega$, $A_{VD} = 1$, $C_L = 100\text{ pF}$		668			kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		58			$^\circ$

TLE2144 ELECTRICAL CHARACTERISTICS

 $V_{CC} = 5\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	TLE2144			UNIT	
			MIN	TYP	MAX		
V_{IO} Input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		0.5	3.8	mV	
		Full range			5.2		
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$	
I_{IO} Input offset current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		8	100	nA	
		Full range			250		
I_{IB} Input bias current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		-0.8	-2	μA	
		Full range			-2.3		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3	-0.3 to 3.2		V	
		Full range	0 to 2.7	-0.3 to 2.9			
V_{OH} High-level output voltage	$I_{OH} = -150\ \mu\text{A}$	25°C		3.9	4.1	V	
	$I_{OH} = -1.5\text{ mA}$			3.8	4		
	$I_{OH} = -15\text{ mA}$			3.4	3.7		
	Full range	$I_{OH} = -100\ \mu\text{A}$		3.75			
		$I_{OH} = -1\text{ mA}$		3.65			
		$I_{OH} = -10\text{ mA}$		3.45			
V_{OL} Low-level output voltage	$I_{OL} = 150\ \mu\text{A}$	25°C			75	125	mV
	$I_{OL} = 1.5\text{ mA}$				150	225	
	$I_{OL} = 15\text{ mA}$				1.2	1.6	V
	Full range	$I_{OL} = 100\ \mu\text{A}$				200	mV
		$I_{OL} = 1\text{ mA}$				250	
		$I_{OL} = 10\text{ mA}$				1.45	V
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_O = 1\text{ V}$ to -1.5 V	25°C	50	95		V/mV	
		Full range	5				
r_i Input resistance		25°C		70		M Ω	
c_i Input capacitance		25°C		2.5		pF	
z_o Open-loop output impedance	$f = 1\text{ MHz}$	25°C		3.		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$, $R_S = 50\ \Omega$	25°C	85	118		dB	
		Full range	80				
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$, $R_S = 50\ \Omega$	25°C	90	106		dB	
		Full range	85				
I_{CC} Supply current	$V_O = 2.5\text{ V}$, No load, $V_{IC} = 2.5\text{ V}$	25°C		13.2	17.6	mA	
		Full range			18.4		

 (1) Full range is -55°C to 125°C .

TLE2144 OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2144			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$			45		V/ μs
SR–	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$			42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 2.5-V step	To 0.1%		0.16		μs
			To 0.01%		0.22		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 10\text{ Hz}$		15		nV/ $\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$		10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$			0.48		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$			0.51		
I_n	Equivalent input noise current	$f = 10\text{ Hz}$			1.92		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			0.5		
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }3\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 2$, $f = 10\text{ kHz}$			0.0052		%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}$			5.9		MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 1$			660		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}$			57		°

(1) R_L terminated at 2.5 V.

TLE2144 ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 15\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLE2144			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		0.6	2.4	mV
		Full range			4	
α_{VIO} Temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		1.7		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		7	100	nA
		Full range			250	
I_{IB} Input bias current	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		-0.7	-1.5	μA
		Full range			-1.8	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13	-15.3 to 13.2		V
		Full range	-15 to 12.7	-15.3 to 12.9		
V_{OM+} Maximum positive peak output voltage swing	$I_O = -150\ \mu\text{A}$ $I_O = -1.5\ \text{mA}$ $I_O = -15\ \text{mA}$ $I_O = -100\ \mu\text{A}$ $I_O = -1\ \text{mA}$ $I_O = -10\ \text{mA}$	25°C		13.8	14.1	V
				13.7	14	
				13.1	13.7	
		Full range		13.7		
				13.6		
				13.1		
V_{OM-} Maximum negative peak output voltage swing	$I_O = 150\ \mu\text{A}$ $I_O = 1.5\ \text{mA}$ $I_O = 15\ \text{mA}$ $I_O = 100\ \mu\text{A}$ $I_O = 1\ \text{mA}$ $I_O = 10\ \text{mA}$	25°C		-14.7	-14.9	V
				-14.5	-14.8	
				-13.4	-13.8	
		Full range		-14.6		
				-14.5		
				-13.4		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 2\ \text{k}\Omega$	25°C	100	170	V/mV	
		Full range	20			
r_i Input resistance		25°C		65	$\text{M}\Omega$	
c_i Input capacitance		25°C		2.5	pF	
z_o Open-loop output impedance	$f = 1\ \text{MHz}$	25°C		30	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min}), R_S = 50\ \Omega$	25°C	85	108	dB	
		Full range	80			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}, R_S = 50\ \Omega$	25°C	90	106	dB	
		Full range	85			
I_{OS} Short-circuit output current	$V_O = 0$	25°C	$V_{ID} = 1\ \text{V}$	-25	-50	mA
			$V_{ID} = -1\ \text{V}$	20	31	
I_{CC} Supply current	$V_O = 0, \text{ No load}, V_{IC} = 2.5\ \text{V}$	25°C		13.8	18	mA
		Full range			18.8	

 (1) Full range is -55°C to 125°C .

TLE2144 OPERATING CHARACTERISTICS

$V_{CC} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2144			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		27	45		V/ μs
SR-	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		27	42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 10-V step	To 0.1%	0.34			μs
			To 0.01%	0.4			
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 10 Hz	15			nV/ $\sqrt{\text{Hz}}$
			f = 1 kHz	10.5			
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		0.48			μV
		f = 0.1 Hz to 10 Hz		0.51			
I_n	Equivalent input noise current	f = 10 Hz		1.89			pA/ $\sqrt{\text{Hz}}$
		f = 10 kHz		0.47			
THD+N	Total harmonic distortion plus noise	$V_{O(PP)} = 20\text{ V}$, $R_L = 2\text{ k}\Omega$, $A_{VD} = 10$, f = 10 kHz		0.01			%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		6			MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, f = 100 kHz		5.9			MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 20\text{ V}$, $A_{VD} = 1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		668			kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		58			$^\circ$

TYPICAL CHARACTERISTICS

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ϕ_m	Phase margin	vs Load capacitance	Figure 36

TLE2141
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

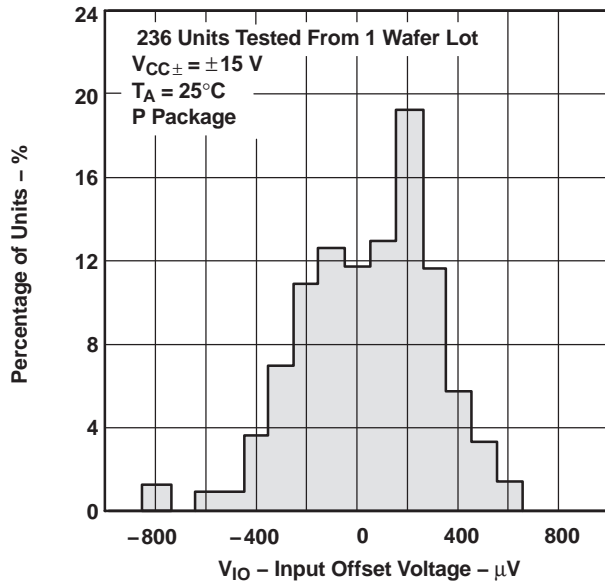


Figure 1.

TLE2142
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

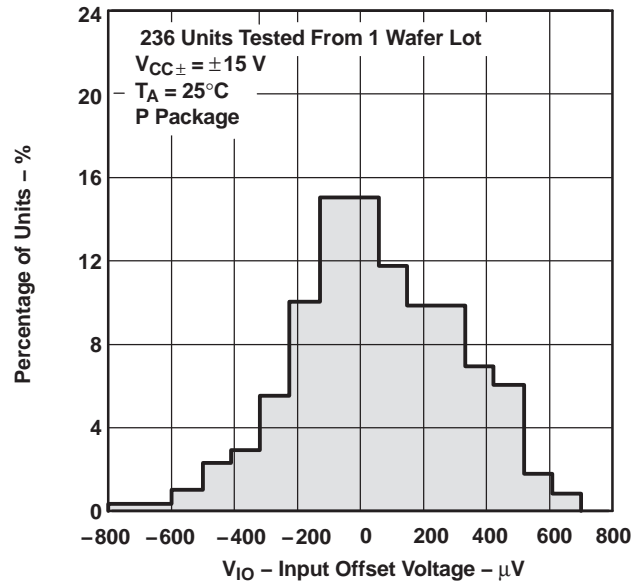


Figure 2.

TLE2144
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

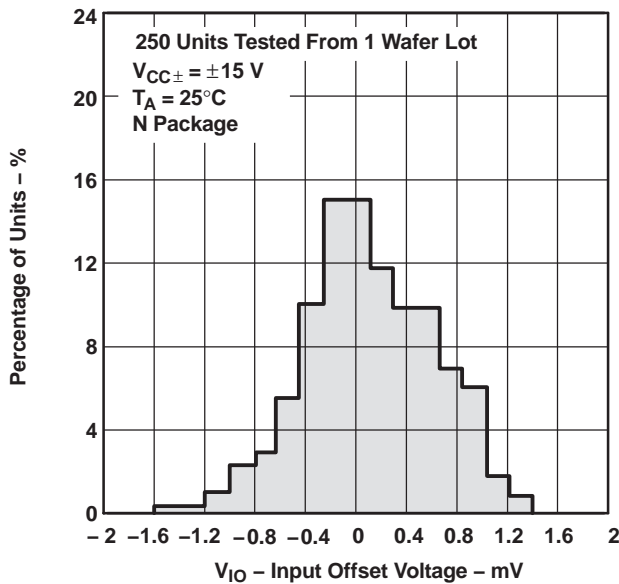


Figure 3.

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

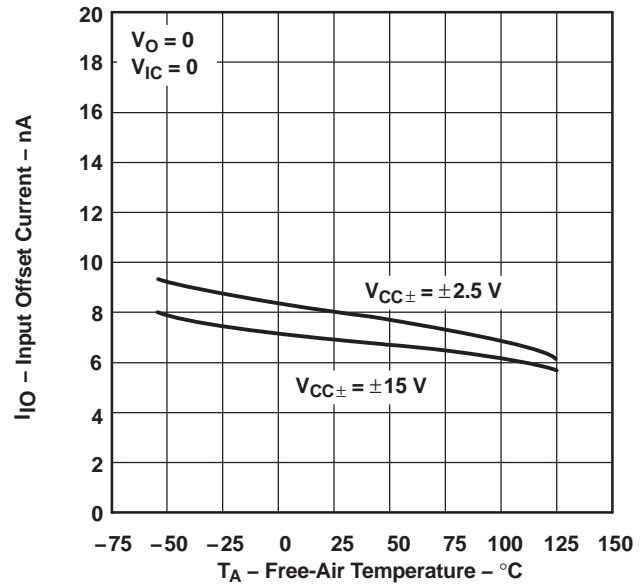


Figure 4.

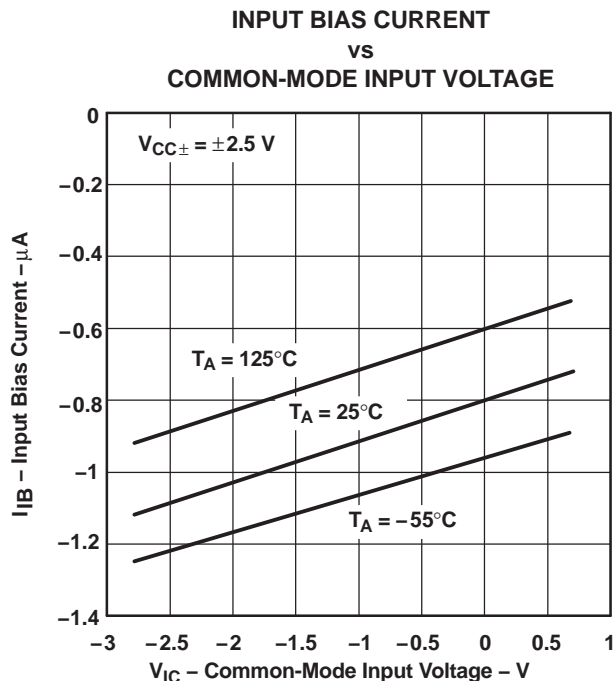


Figure 5.

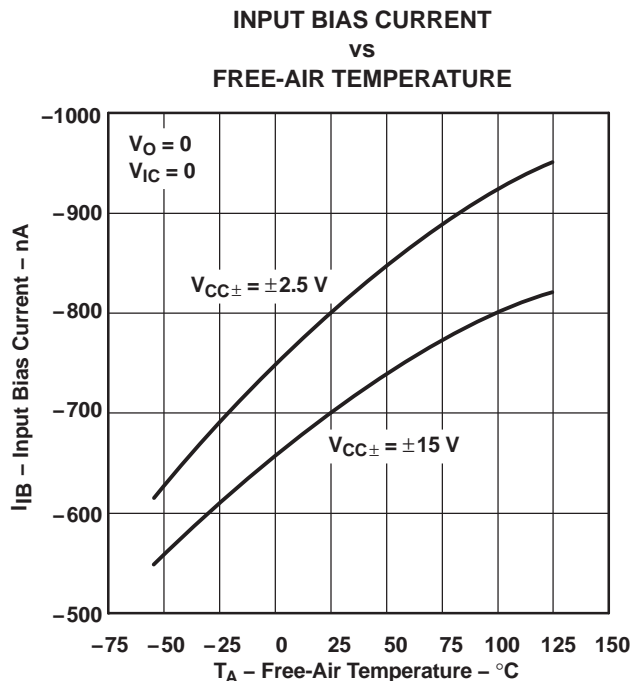


Figure 6.

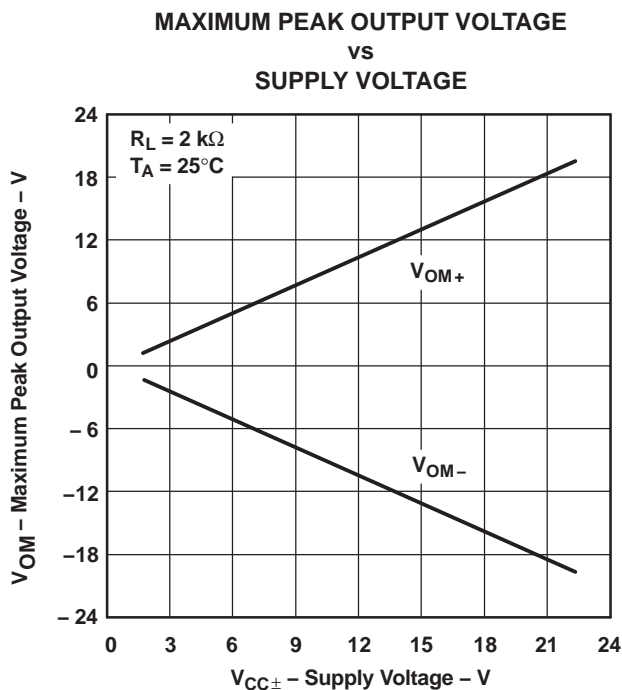


Figure 7.

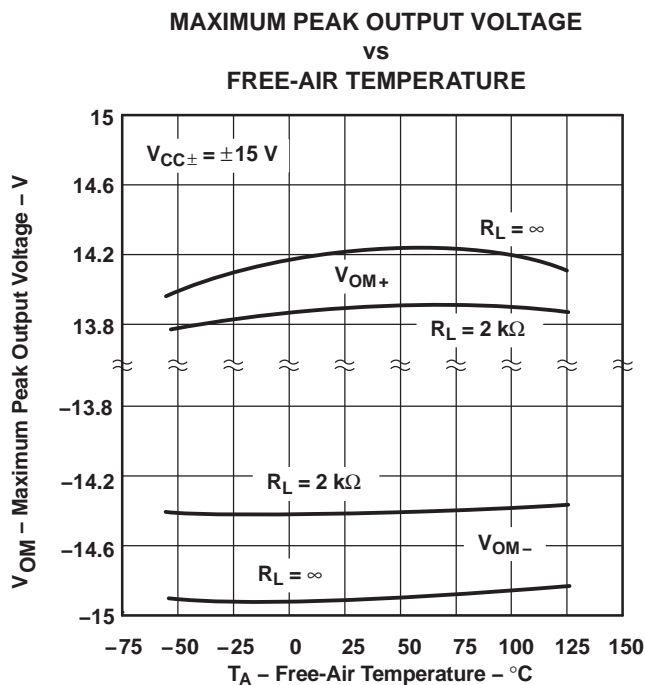


Figure 8.

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
VS
OUTPUT CURRENT

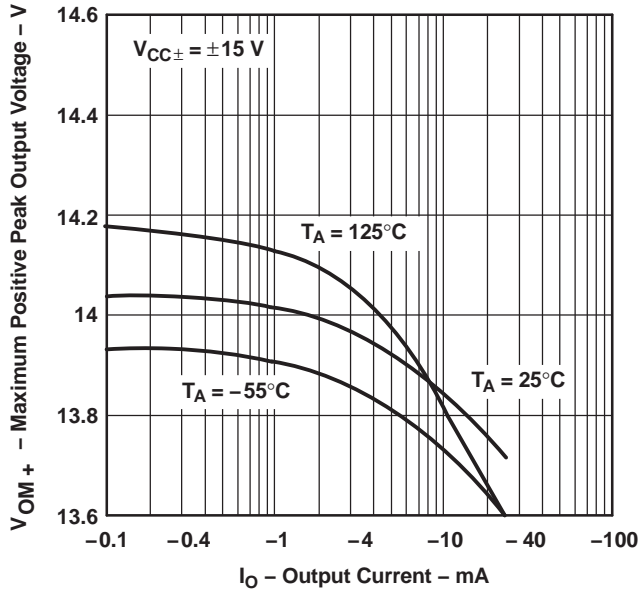


Figure 9.

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
VS
OUTPUT CURRENT

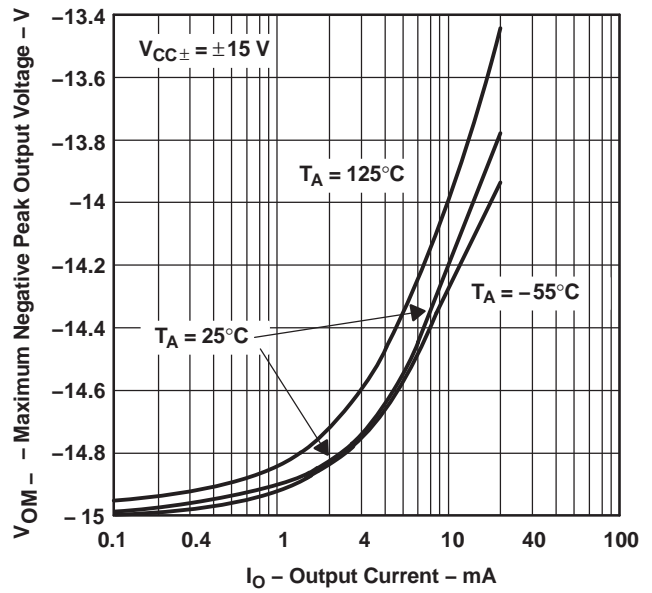


Figure 10.

MAXIMUM PEAK OUTPUT VOLTAGE
VS
SETTLING TIME

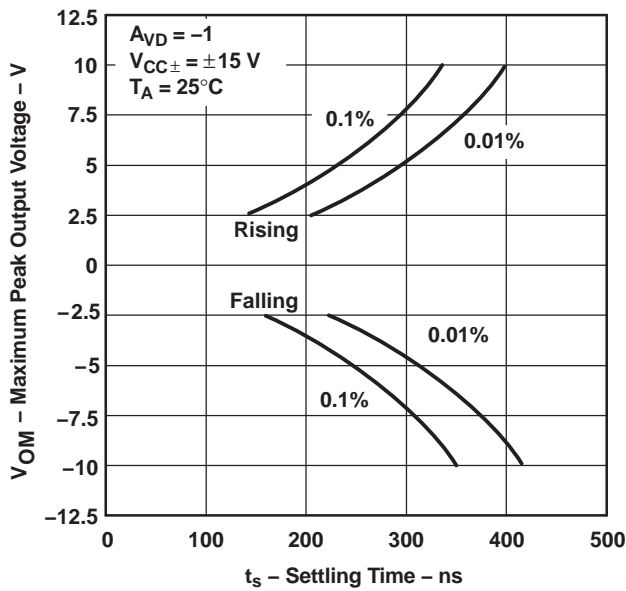


Figure 11.

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
VS
FREQUENCY

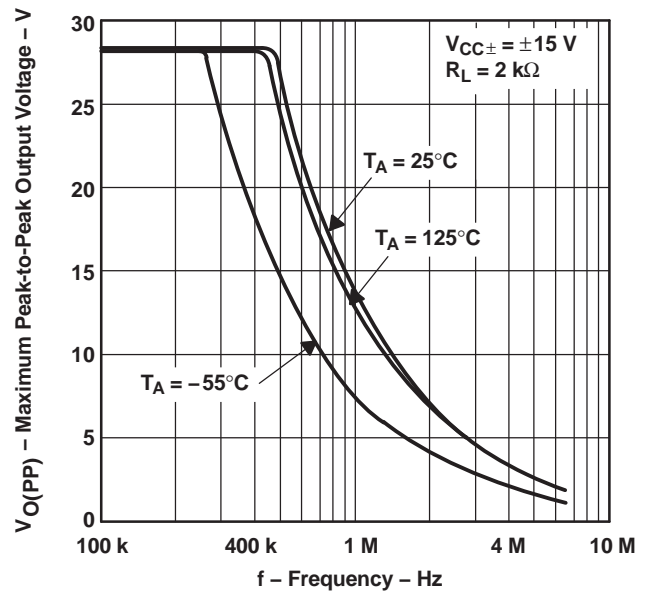


Figure 12.

HIGH-LEVEL OUTPUT VOLTAGE
VS
OUTPUT CURRENT

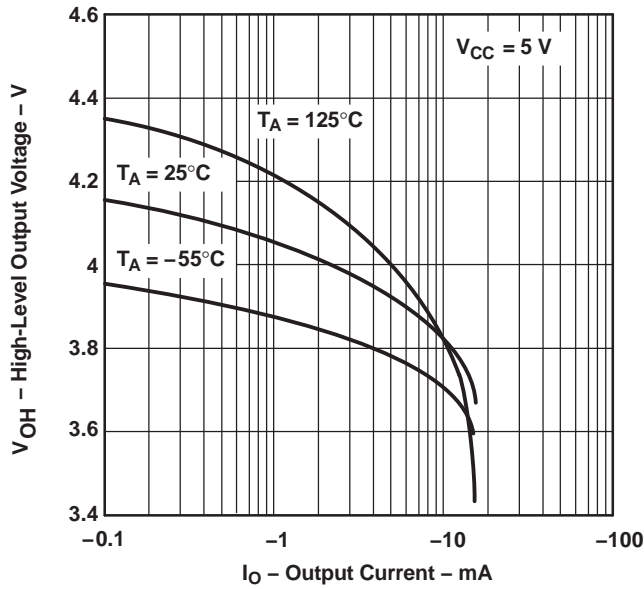


Figure 13.

LOW-LEVEL OUTPUT VOLTAGE
VS
OUTPUT CURRENT

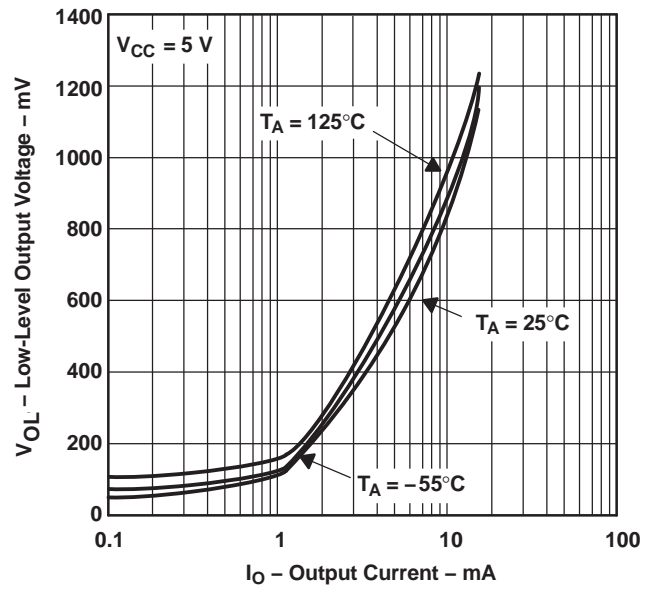


Figure 14.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
VS
FREQUENCY

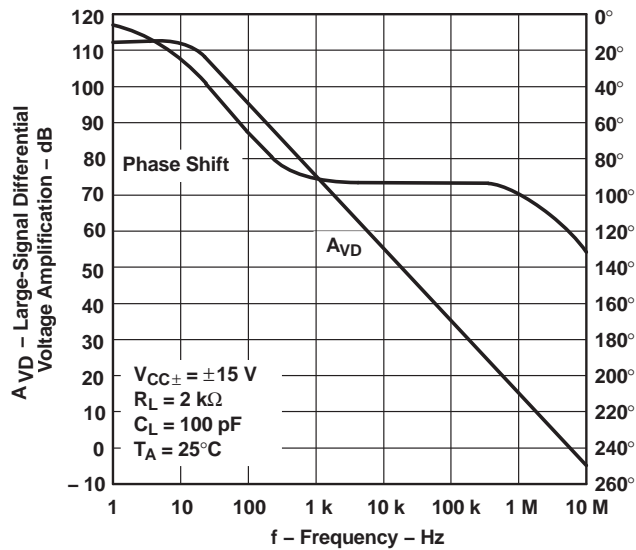


Figure 15.

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
VS
FREE-AIR TEMPERATURE

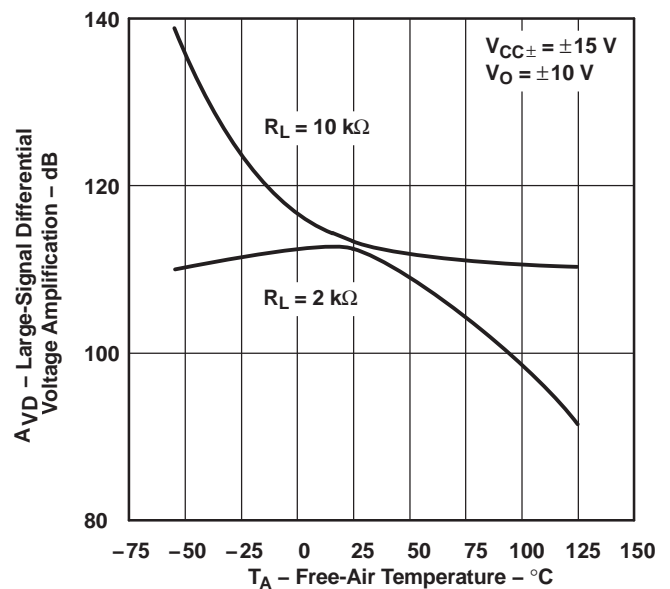
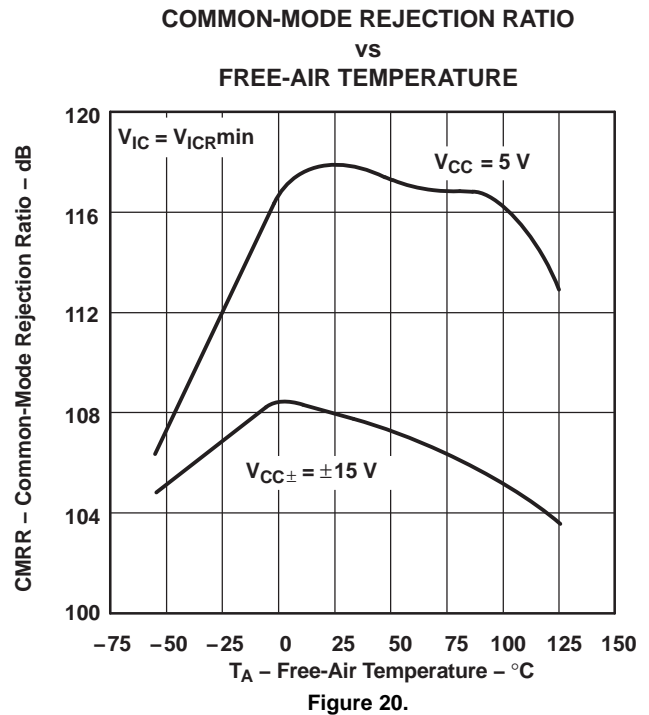
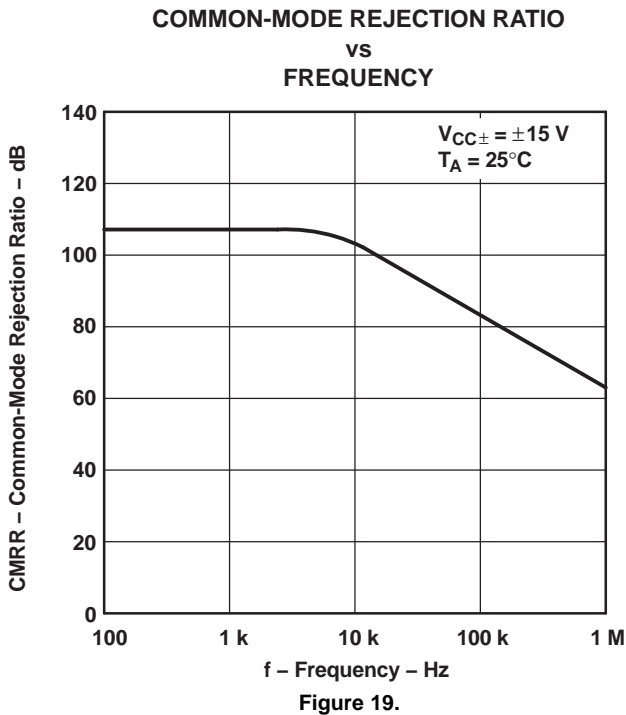
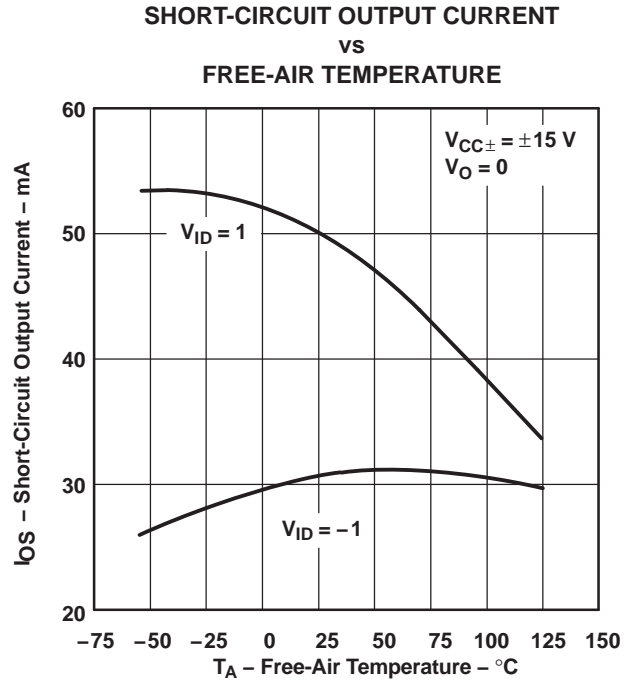
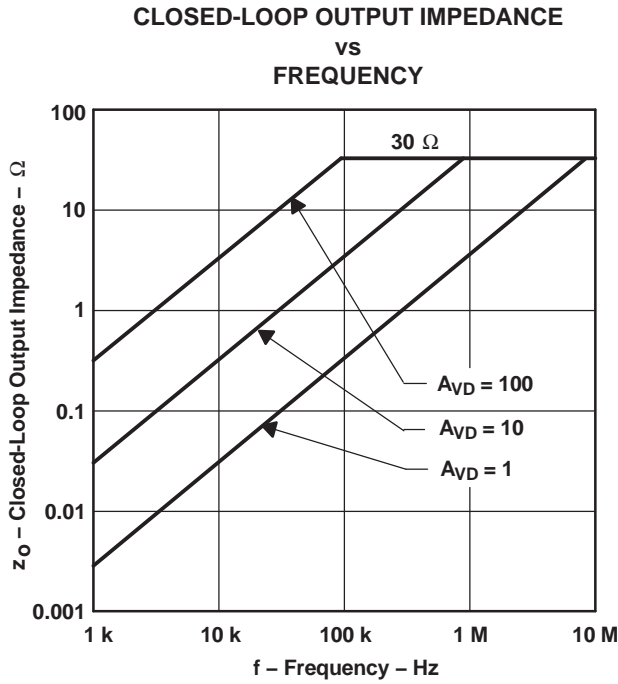


Figure 16.



SUPPLY-VOLTAGE REJECTION RATIO
VS
FREQUENCY

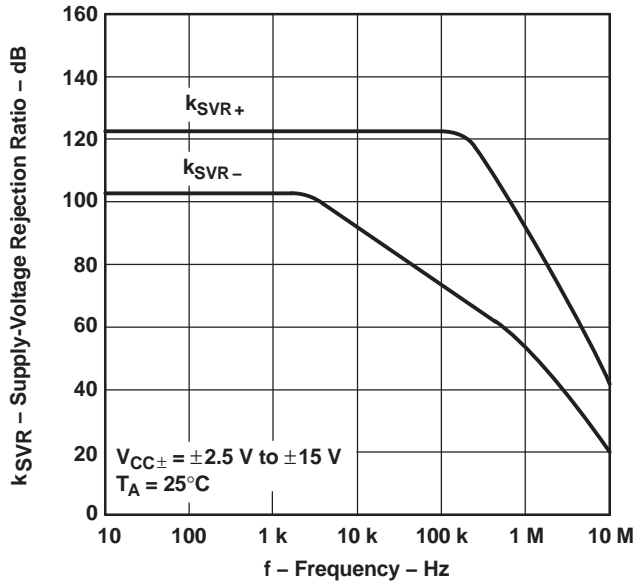


Figure 21.

SUPPLY-VOLTAGE REJECTION RATIO
VS
FREE-AIR TEMPERATURE

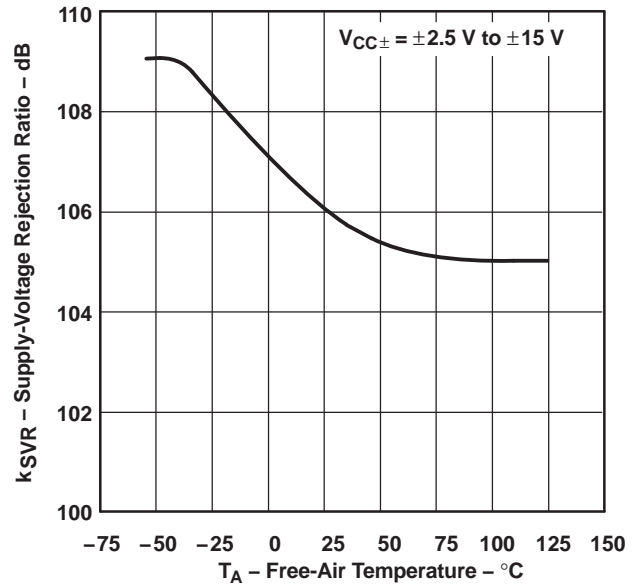


Figure 22.

SUPPLY CURRENT
VS
SUPPLY VOLTAGE

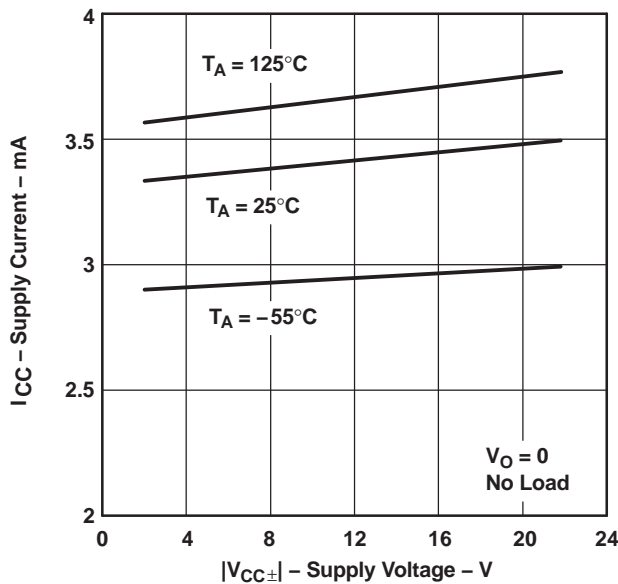


Figure 23.

SUPPLY CURRENT
VS
FREE-AIR TEMPERATURE

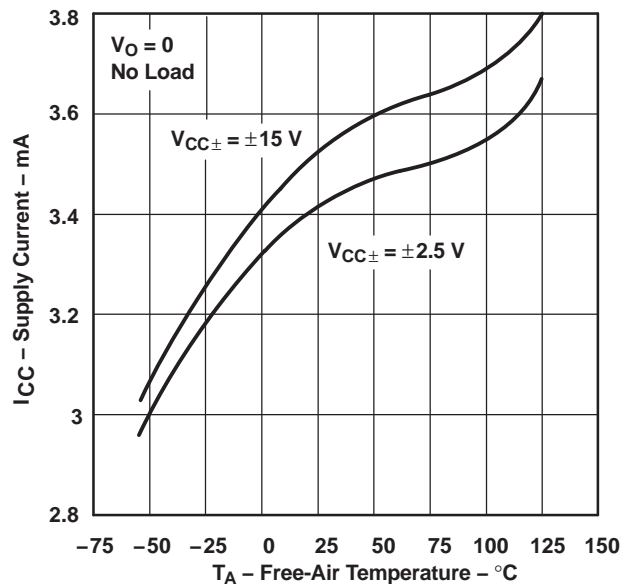


Figure 24.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

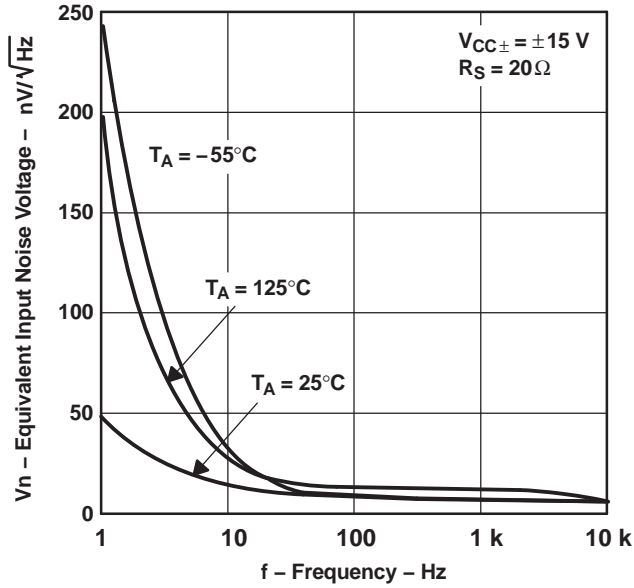


Figure 25.
NOISE CURRENT
vs
FREQUENCY

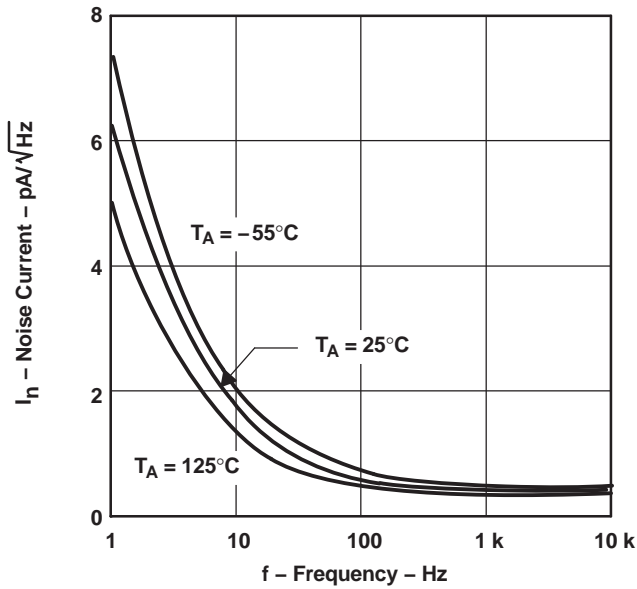


Figure 27.

INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

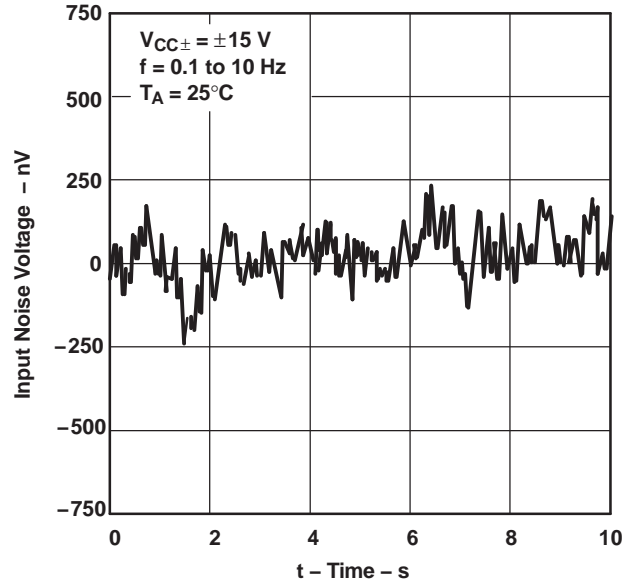


Figure 26.

TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
FREQUENCY

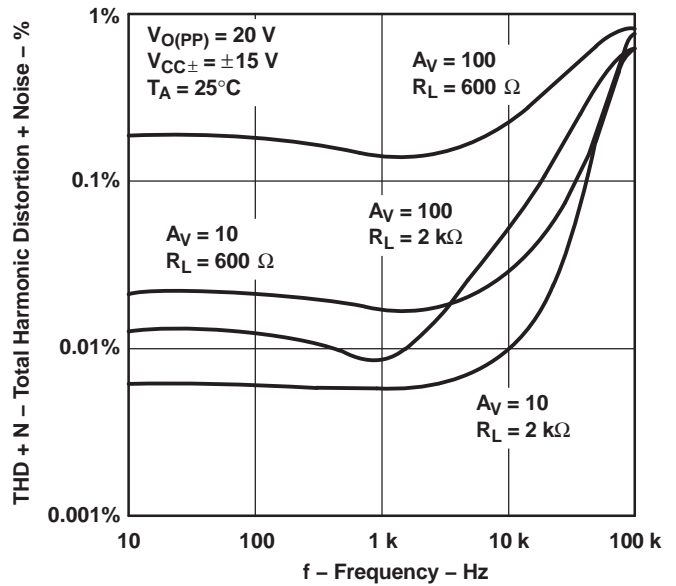
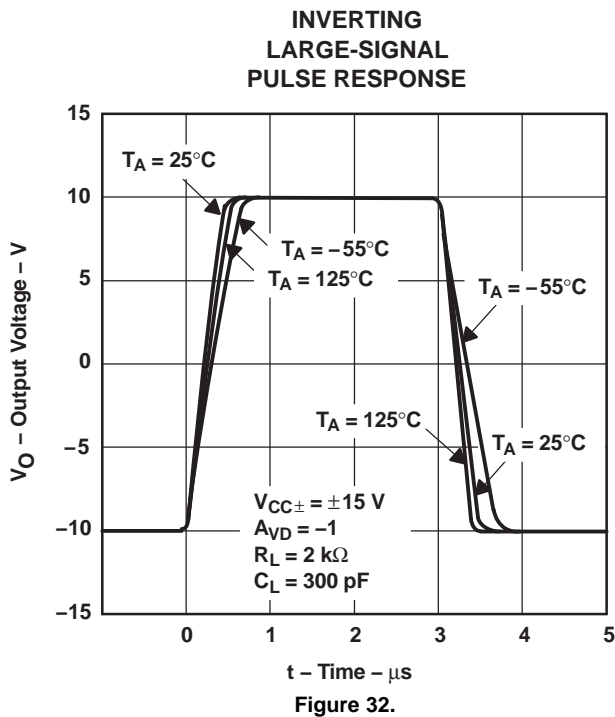
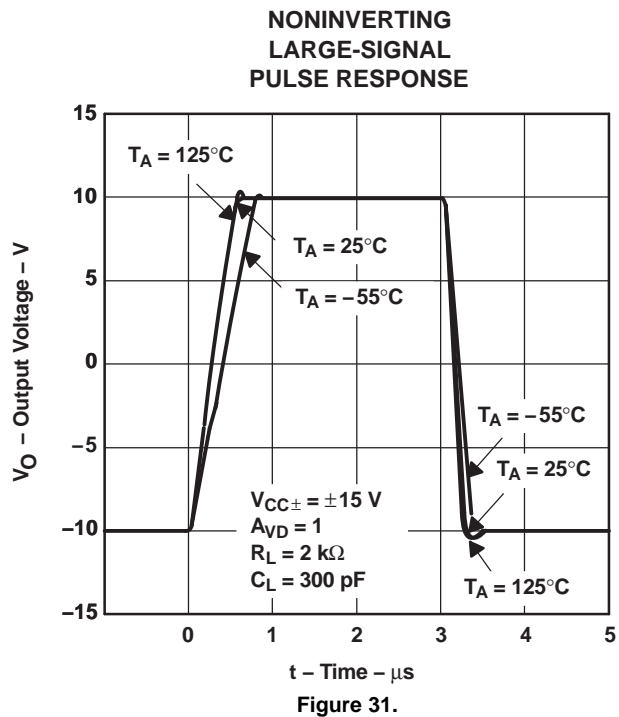
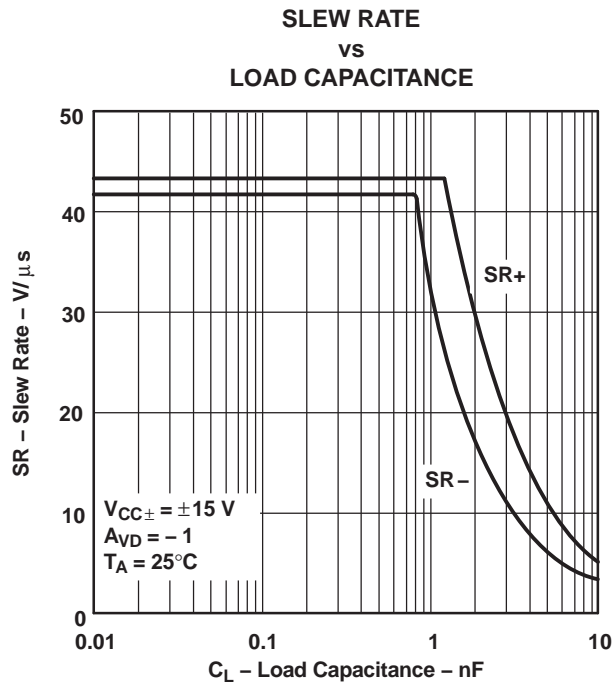
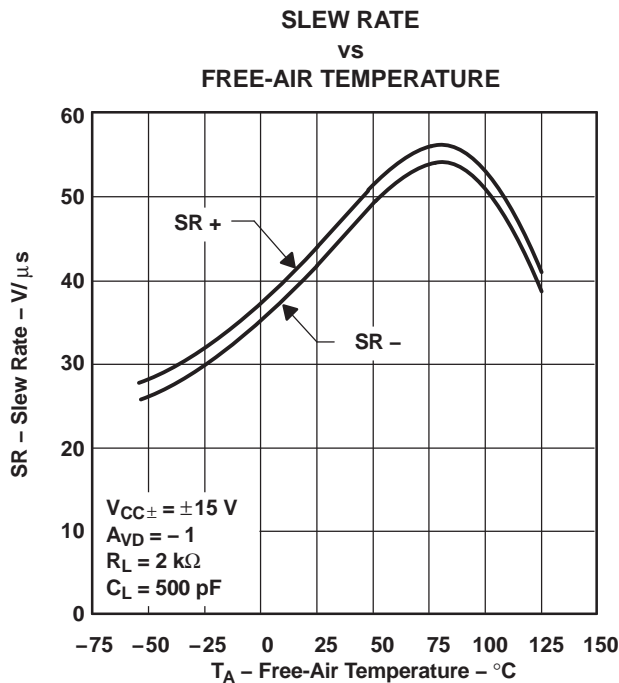


Figure 28.



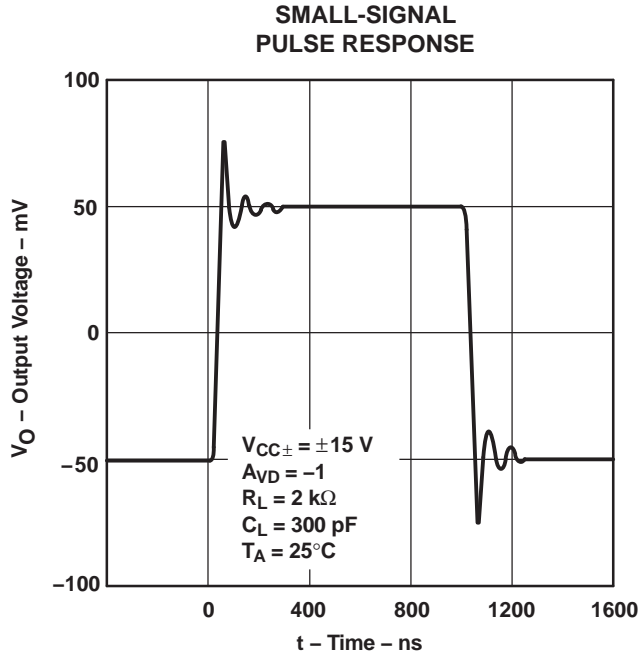


Figure 33.

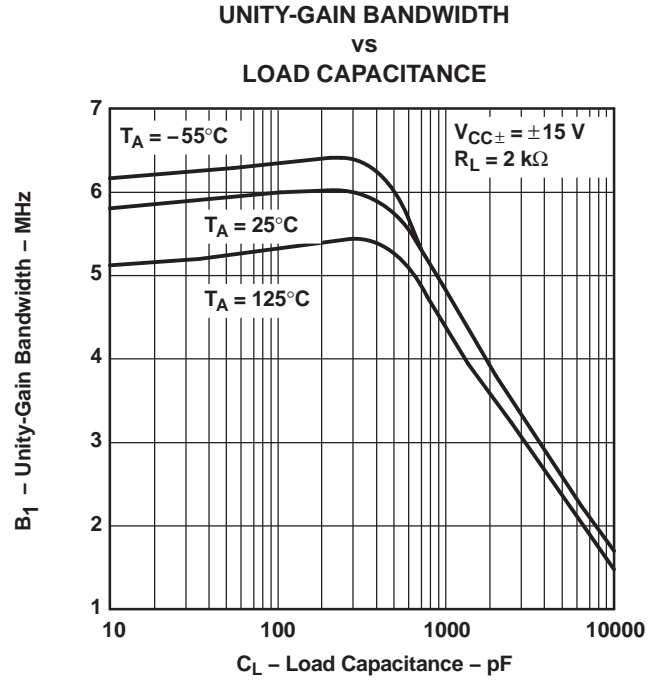


Figure 34.

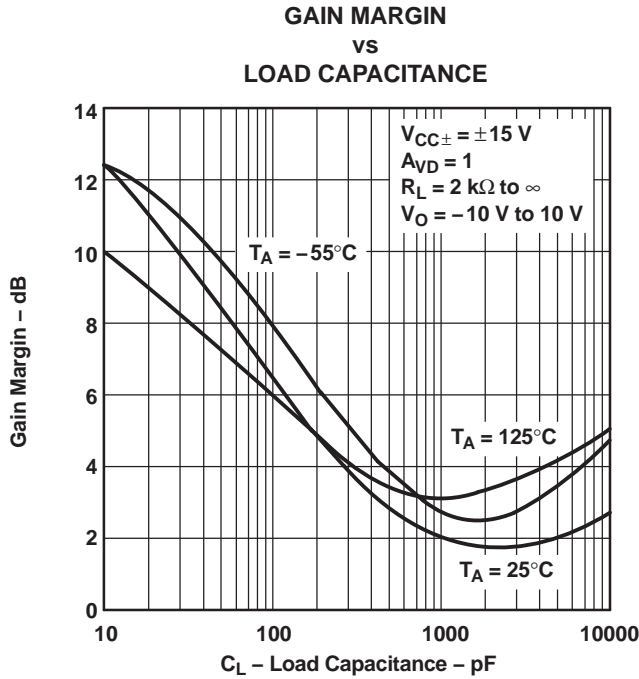


Figure 35.

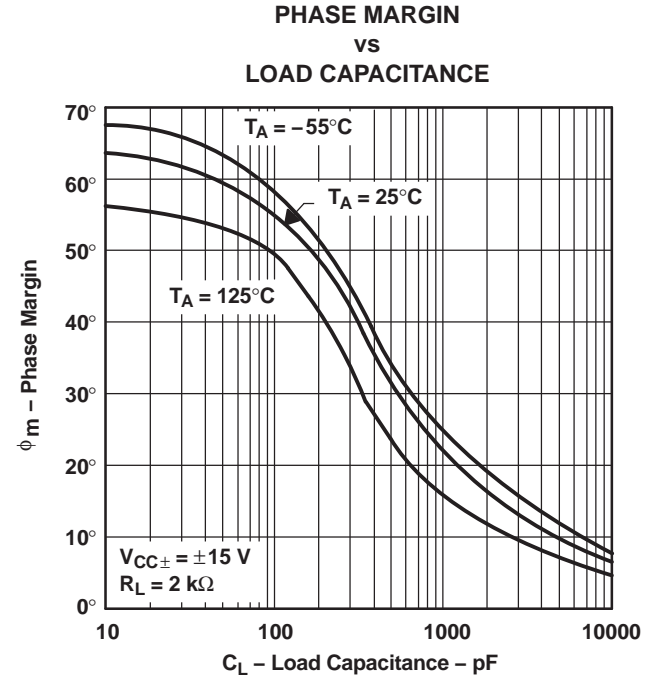


Figure 36.

APPLICATION INFORMATION

Input Offset Voltage Nulling

The TLE2141 offers external null pins that can be used to further reduce the input offset voltage. If this feature is desired, connect the circuit of [Figure 37](#) as shown. If external nulling is not needed, the null pins may be left unconnected.

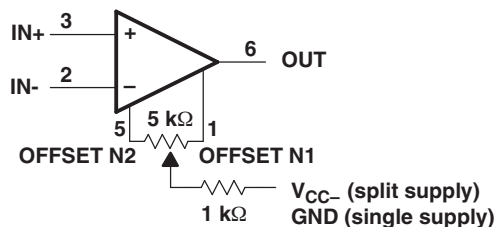


Figure 37. Input Offset Voltage Null Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2141MDREP	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141EP
TLE2141MDREP.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141EP
TLE2144MDWREP	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2144MEP
TLE2144MDWREP.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2144MEP
V62/08620-01XE	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141EP
V62/08620-03YE	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2144MEP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLE2141-EP, TLE2144-EP :

- Catalog : [TLE2141](#), [TLE2144](#)
- Automotive : [TLE2141-Q1](#)
- Military : [TLE2141M](#), [TLE2144M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2141MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2144MDWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2141MDREP	SOIC	D	8	2500	353.0	353.0	32.0
TLE2144MDWREP	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

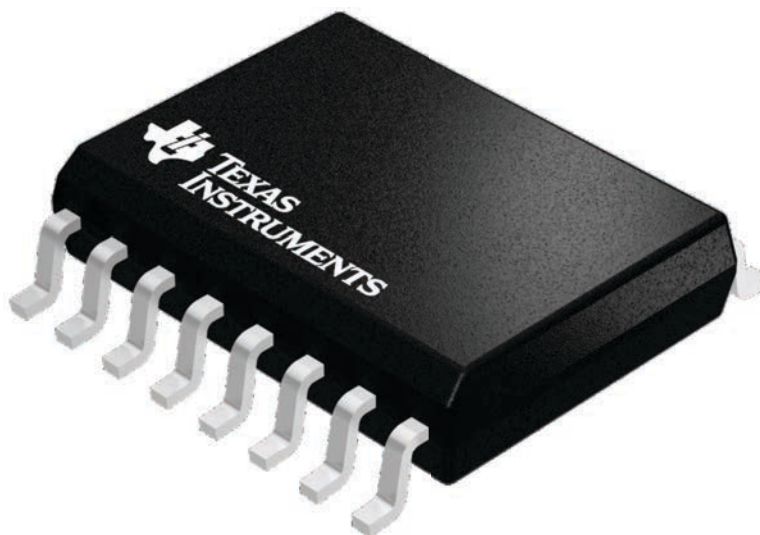
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

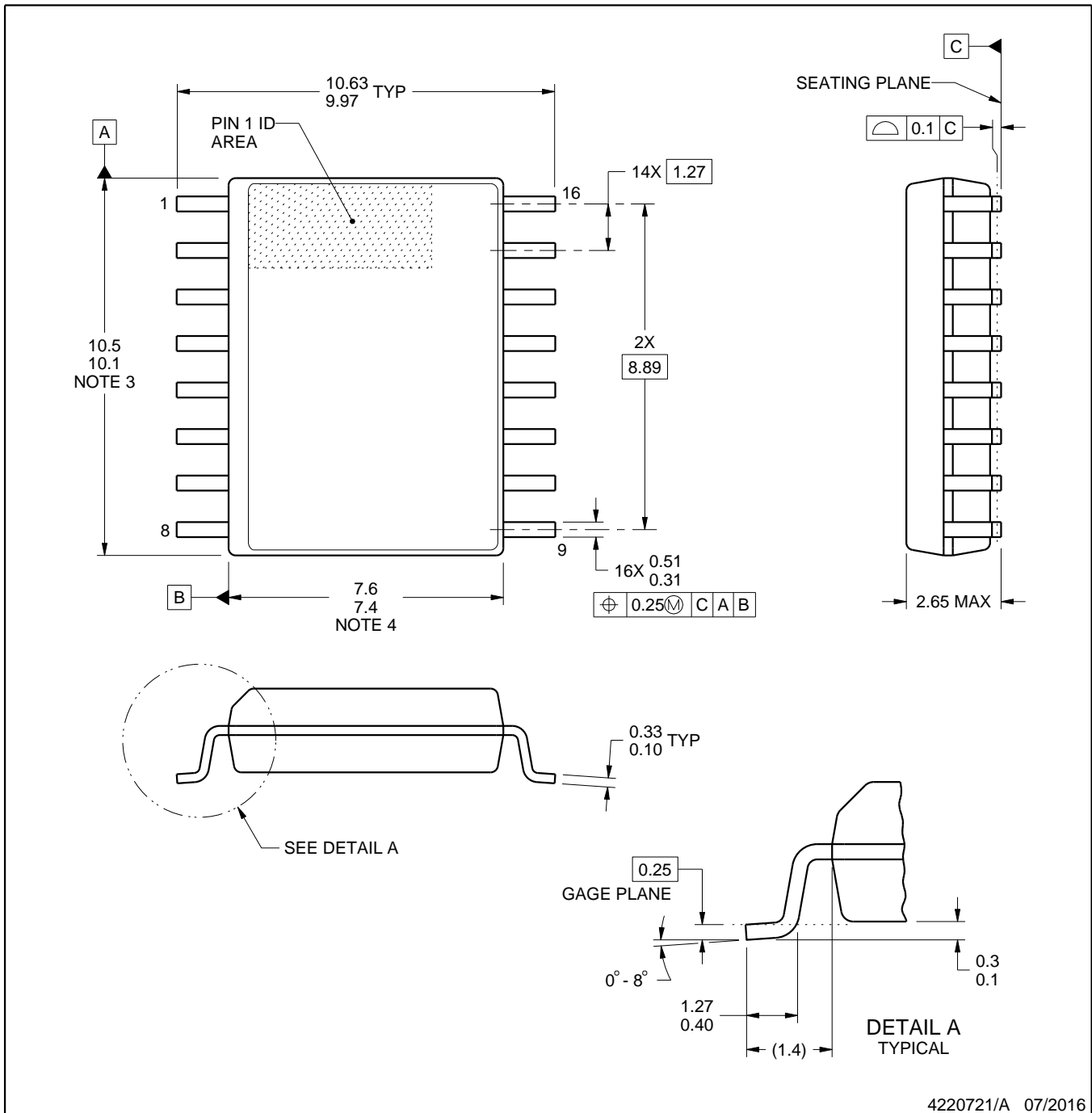


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

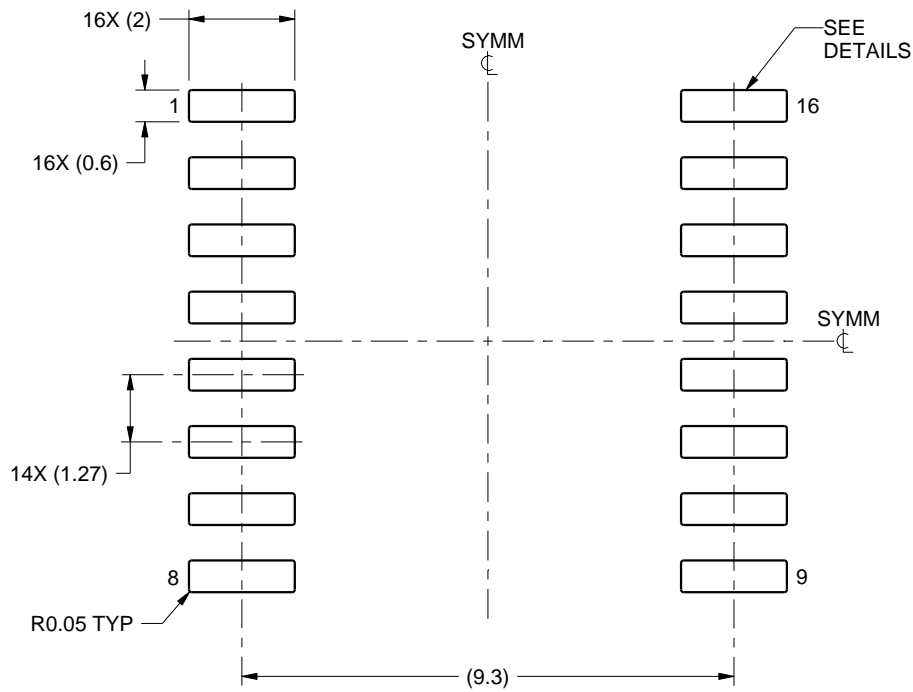
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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