Unitrode Products
from Texas Instruments

application INFO available

UC1856
UC2856
UC3856

# Improved Current Mode PWM Controller

## FEATURES

- Pin-for-Pin Compatible With the UC3846
- 65ns Typical Delay From Shutdown to Outputs, and 50ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4kV ESD Protection

## DESCRIPTION

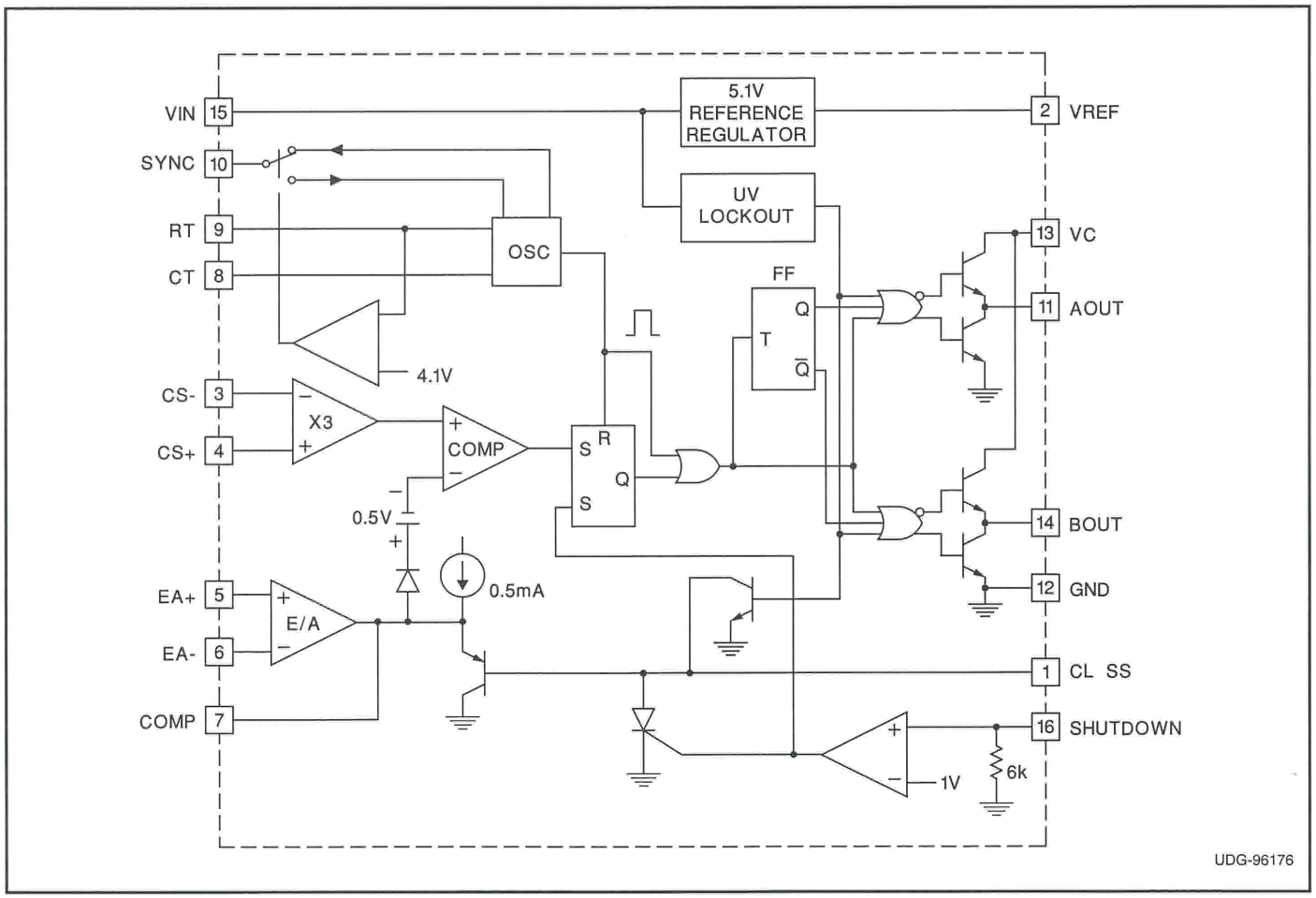
The UC3856 is a high performance version of the popular UC3846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1V, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

## BLOCK DIAGRAM



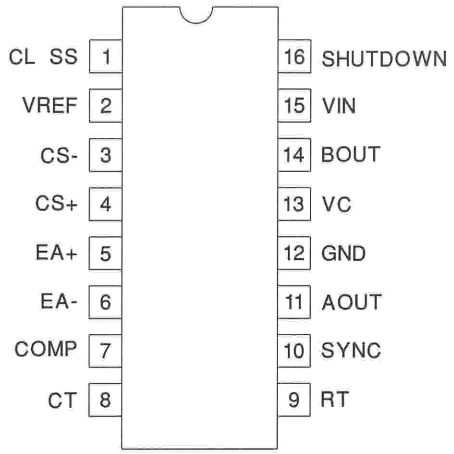
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +40V
Collector Supply Voltage . . . . . +40V
Output Current, Source or Sink
DC . . . . . 0.5A
Pulse (0.5µs) . . . . . 2.0A
Error Amp Inputs . . . . . –0.3V to $+V_{IN}$
Shutdown Input . . . . . –0.3V to +10V
Current Sense Inputs . . . . . –0.3V to +3V
SYNC Output Current . . . . . ±10mA
Error Amplifier Output Current . . . . . –5mA
Soft Start Sink Current . . . . . 50mA
Oscillator Charging Current . . . . . 5mA
Power Dissipation at $T_A$ = 25°C (Note 2) . . . . . 1000mW
Power Dissipation at $T_C$ = 25°C (Note 2) . . . . . 2000mW
Junction Temperature . . . . . –55°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

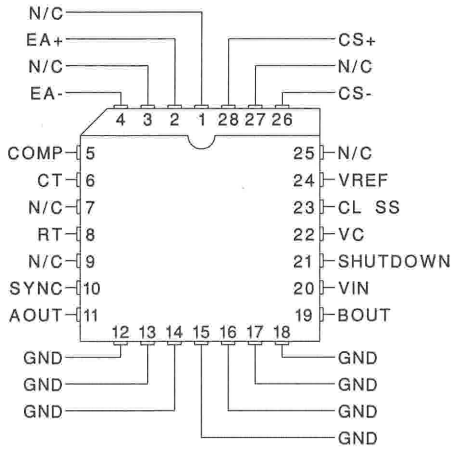
*All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.*

## CONNECTION DIAGRAMS

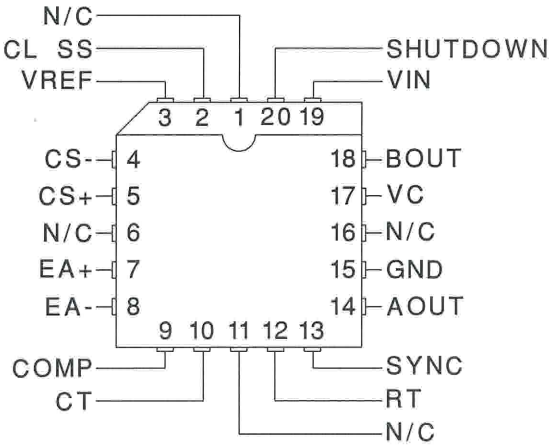
**DIL–16, SOIC-16 (Top View)**
**J or N, DW PACKAGE**




**PLCC-28 (Top View)**
**QP PACKAGE**




**PLCC-20 (Top View)**
**Q PACKAGE**




**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for $T_A$ = –55°C to +125°C for UC1856; –40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1856/UC2856 | | | UC3856 | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **Reference Section** | | | | | | | | |
| Output Voltage | $T_J$ = 25°C, $I_O$ = 1mA | 5.05 | 5.10 | 5.15 | 5.00 | 5.10 | 5.20 | V |
| Line Regulation | VIN = 8V to 40V | | | 20 | | | 20 | mV |
| Load Regulation | $I_O$ = –1mA to –10mA | | | 15 | | | 15 | mV |
| Total Output Variation | Line, Load, and Temperature | 5.00 | | 5.20 | 4.95 | | 5.25 | V |
| Output Noise Voltage | 10Hz < f < 10kHz, $T_J$ = 25°C | | 50 | | | 50 | | µV |
| Long Term Stability | $T_J$ = 125°C, 1000 Hrs (Note 2) | | 5 | 25 | | 5 | 25 | mV |
| Short Circuit Current | VREF = 0V | –25 | –45 | –65 | –25 | –45 | –65 | mA |
| **Oscillator Section** | | | | | | | | |
| Initial Accuracy | $T_J$ = 25°C | 180 | 200 | 220 | 180 | 200 | 220 | kHz |
| | Over Operating Range | 170 | | 230 | 170 | | 230 | kHz |

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for $T_A$ = –55°C to +125°C for UC1856; –40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1856/UC2856 | | | UC3856 | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **Oscillator Section (cont.)** | | | | | | | | |
| Voltage Stability | VIN = 8V to 40V | | | 2 | | | 2 | % |
| Discharge Current | $T_J$ = 25°C, $V_{CT}$ = 2V | 7.5 | 8.0 | 8.8 | 7.5 | 8.0 | 8.8 | mA |
| | $V_{CT}$ = 2V | 6.7 | 8.0 | 8.8 | 6.7 | 8.0 | 8.8 | mA |
| Sync Output High Level | $I_O$ = –1mA | 2.4 | 3.6 | | 2.4 | 3.6 | | V |
| Sync Output Low Level | $I_O$ = +1mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| Sync Input High Level | CT = 0V, RT = VREF | 2.0 | 1.5 | | 2.0 | 1.5 | | V |
| Sync Input Low Level | CT = 0V, RT = VREF | | 1.5 | 0.8 | | 1.5 | 0.8 | V |
| Sync Input Current | CT = 0V, RT = VREF $V_{SYNC}$ = 5V | | 1 | 10 | | 1 | 10 | µA |
| Sync Delay to Outputs | CT = 0V, RT = VREF $V_{SYNC}$ = 0.8V to 2V | | 50 | 100 | | 50 | 100 | ns |
| **Error Amplifier Section** | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 2V | | | 5 | | | 10 | mV |
| Input Bias Current | | | | –1 | | | –1 | µA |
| Input Offset Current | | | | 500 | | | 500 | nA |
| Common Mode Range | VIN = 8V to 40V | 0 | | VIN-2 | 0 | | VIN-2 | V |
| Open Loop Gain | $V_O$ = 1.2V to 3V | 80 | 100 | | 80 | 100 | | dB |
| Unity Gain Bandwidth | $T_J$ = 25°C | 1 | 1.5 | | 1 | 1.5 | | MHz |
| CMRR | $V_{CM}$ = 0V to 38V, VIN = 40V | 75 | 100 | | 75 | 100 | | dB |
| PSRR | VIN = 8V to 40V | 80 | 100 | | 80 | 100 | | dB |
| Output Sink Current | $V_{ID}$ = –15mV, $V_{COMP}$ = 1.2V | 5 | 10 | | 5 | 10 | | mA |
| Output Source Current | $V_{ID}$ = 15mV, $V_{COMP}$ = 2.5V | –0.4 | –0.5 | | –0.4 | –0.5 | | mA |
| Output High Level | $V_{ID}$ = 50mV, $R_L$ (COMP) = 15k | 4.3 | 4.6 | 4.9 | 4.3 | 4.6 | 4.9 | V |
| Output Low Level | $V_{ID}$ = –50mV, $R_L$ (COMP) = 15k | | 0.7 | 1 | | 0.7 | 1 | V |
| **Current Sense Amplifier Section** | | | | | | | | |
| Amplifier Gain | $V_{CS}$ – = 0V, CL SS Open (Notes 3,4) | 2.5 | 2.75 | 3.0 | 2.5 | 2.75 | 3.0 | V/V |
| Maximum Differential Input Signal ($V_{CS+}$ - $V_{CS-}$) | CL SS Open (Note 3) $R_L$ (COMP) = 15k | 1.1 | 1.2 | | 1.1 | 1.2 | | V |
| Input Offset Voltage | $V_{CL\ SS}$ = 0.5VCOMP Open (Note 3) | | 5 | 35 | | 5 | 35 | mV |
| CMRR | $V_{CM}$ = 0V to 3V | 60 | | | 60 | | | dB |
| PSRR | VIN = 8V to 40V | 60 | | | 60 | | | dB |
| Input Bias Current | $V_{CL\ SS}$ = 0.5V, COMP Open (Note 3) | -1 | | 1 | -1 | | 1 | µA |
| Input Offset Current | $V_{CL\ SS}$ = 0.5V, COMP Open (Note 3) | -1 | | 1 | -1 | | 1 | µA |
| Input Common Mode Range | | 0 | | 3 | 0 | | 3 | V |
| Delay to Outputs | $V_{EA+}$ = VREF, EA– = 0V CS+ – CS– = 0V to 1.5V | | 120 | 250 | | 120 | 250 | ns |
| **Current Limit Adjust Section** | | | | | | | | |
| Current Limit Offset | $V_{CS-}$ = 0V $V_{CS+}$ = 0V, COMP = Open (Note 3) | 0.43 | 0.5 | 0.57 | 0.43 | 0.5 | 0.57 | V |
| Input Bias Current | $V_{EA+}$ = VREF, $V_{EA-}$ = 0V | | –10 | –30 | | –10 | –30 | µA |
| **Shutdown Terminal Section** | | | | | | | | |
| Threshold Voltage | | 0.95 | 1.00 | 1.05 | 0.95 | 1.00 | 1.05 | V |
| Input Voltage Range | | 0 | | 5 | 0 | | 5 | V |

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for $T_A$ = –55°C to +125°C for UC1856; –40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1856/UC2856 | | | UC3856 | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **Shutdown Terminal Section (cont.)** | | | | | | | | |
| Minimum Latching Current ($I_{CL\ SS}$) | (Note 5) | 3 | 1.5 | | 3 | 1.5 | | mA |
| Maximum Non-Latching Current ($I_{CL\ SS}$) | (Note 6) | | 1.5 | 0.8 | | 1.5 | 0.8 | mA |
| Delay to Outputs | $V_{SHUTDOWN}$ = 0 to 1.3V | | 65 | 110 | | 65 | 110 | ns |
| **Output Section** | | | | | | | | |
| Collector-Emitter Voltage | | 40 | | | 40 | | | V |
| Off-State Bias Current | VC = 40V | | | 250 | | | 250 | µA |
| Output Low Level | $I_{OUT}$ = 20mA | | 0.1 | 0.5 | | 0.1 | 0.5 | V |
| | $I_{OUT}$ = 200mA | | 0.5 | 2.6 | | 0.5 | 2.6 | V |
| Output High Level | $I_{OUT}$ = –20mA | 12.5 | 13.2 | | 12.5 | 13.2 | | V |
| | $I_{OUT}$ = –200mA | 12 | 13.1 | | 12 | 13.1 | | V |
| Rise Time | C1 = 1nF | | 40 | 80 | | 40 | 80 | ns |
| Fall Time | C1 = 1nF | | 40 | 80 | | 40 | 80 | ns |
| UVLO Low Saturation | VIN = 0V, $I_{OUT}$ = 20mA | | 0.8 | 1.5 | | 0.8 | 1.5 | V |
| **PWM Section** | | | | | | | | |
| Maximum Duty Cycle | | 45 | 47 | 50 | 45 | 47 | 50 | % |
| Minimum Duty Cycle | | | | 0 | | | 0 | % |
| **Undervoltage Lockout Section** | | | | | | | | |
| Startup Threshold | | | 7.7 | 8.0 | | 7.7 | 8.0 | V |
| Threshold Hysterisis | | | 0.7 | | | 0.7 | | V |
| **Total Standby Current** | | | | | | | | |
| Supply Current | | | 18 | 23 | | 18 | 23 | mA |

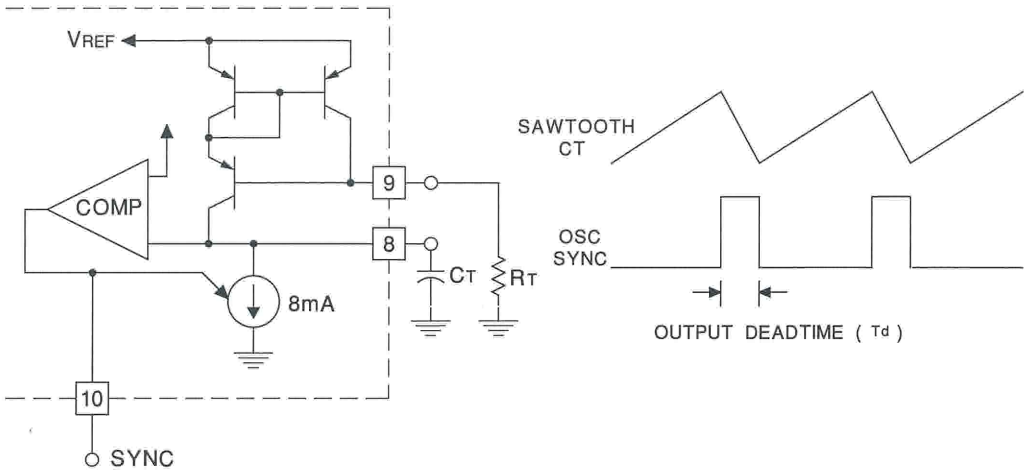
*Note 1: All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.*
*Note 2: This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.*
*Note 3: Parameter measured at trip point of latch with $V_{EA+}$ = VREF, $V_{EA-}$ = 0V.*
*Note 4: Amplifier gain defined as:*

$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS}+}; \qquad \Delta V_{CS}- = 0V\,TO\,1.0V$$

*Note 5: Current into CL SS guaranteed to latch circuit into shutdown state.*
*Note 6: Current into CL SS guaranteed not to latch circuit into shutdown state.*

## APPLICATIONS INFORMATION

### Oscillator Circuit




Output deadtime is determined by size of the external capacitor, $C_T$, according to the formula: $Td = \dfrac{2C_T}{8mA - \dfrac{3.6}{R_T}}$

For large values of $R_T$: $Td = 250C_T$

Oscillator frequency is approximated by the formula: $f_T = \dfrac{2}{R_T\, C_T}$

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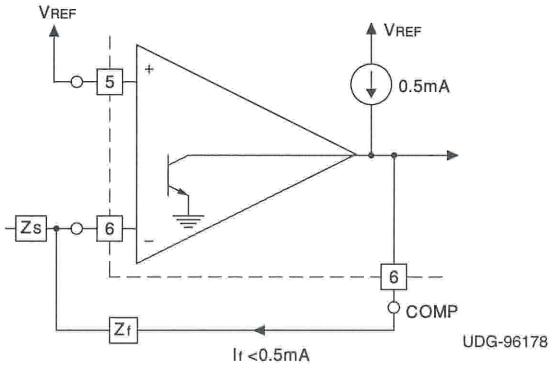
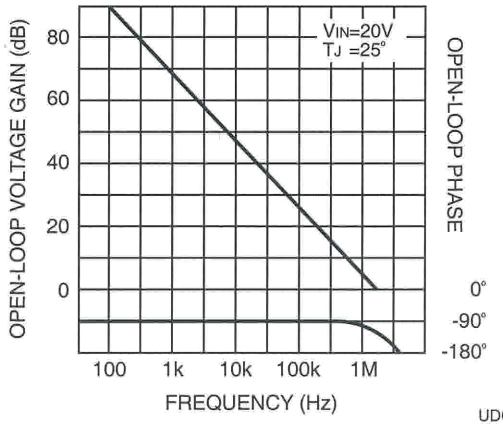
### Error Amplifier Output Configuration

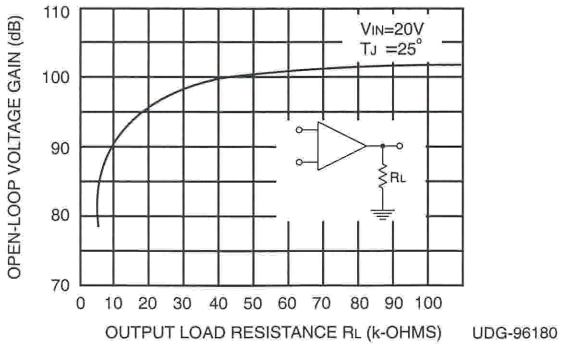



Error Amplifier can source up to 0.5mA.

### Error Amplifier Gain and Phase vs Frequency

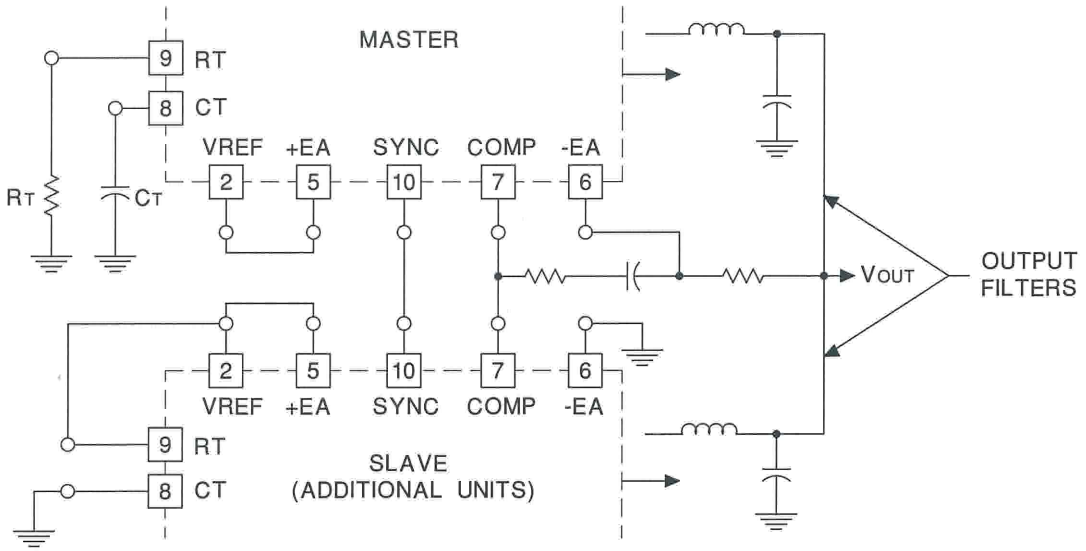



### Error Amplifier Open-Loop D.C. Gain vs Load Resistance



## APPLICATIONS INFORMATION (cont.)

### Parallel Operation

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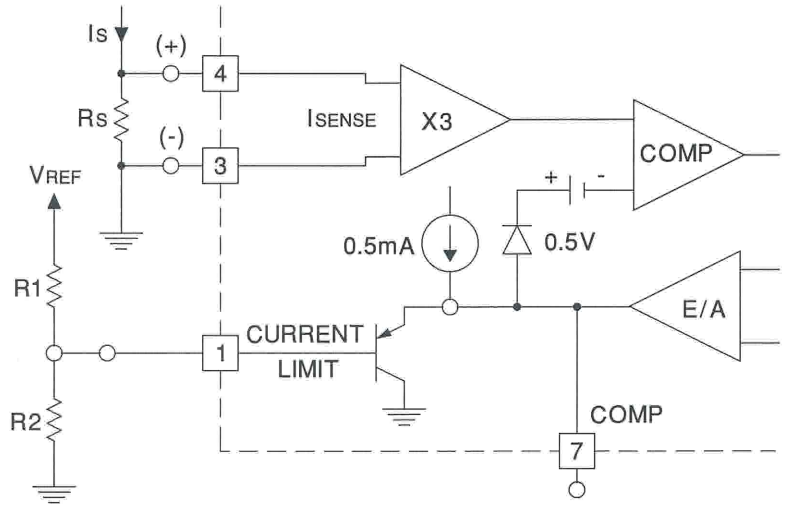
Slaving allows parallel operation of two or more units with equal current sharing.

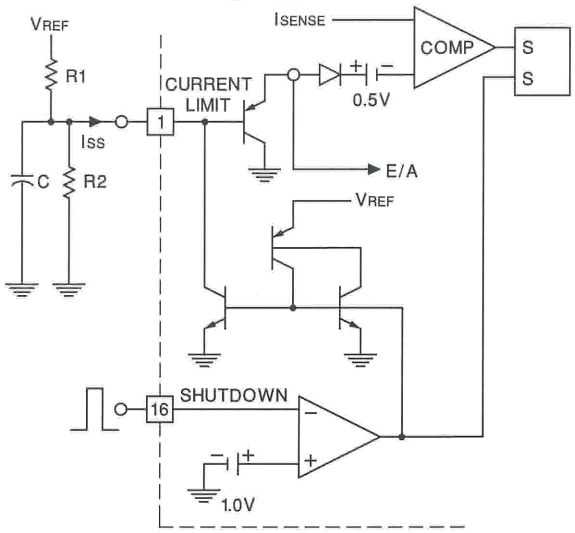
### Pulse by Pulse Current Limiting




UDG-96182

Peak current (Is) is determined by the formula: $Is = \dfrac{\left(\dfrac{R2V_{REF}}{R1+R2}\right) - 0.5}{3R_S}$

## APPLICATIONS INFORMATION (cont.)

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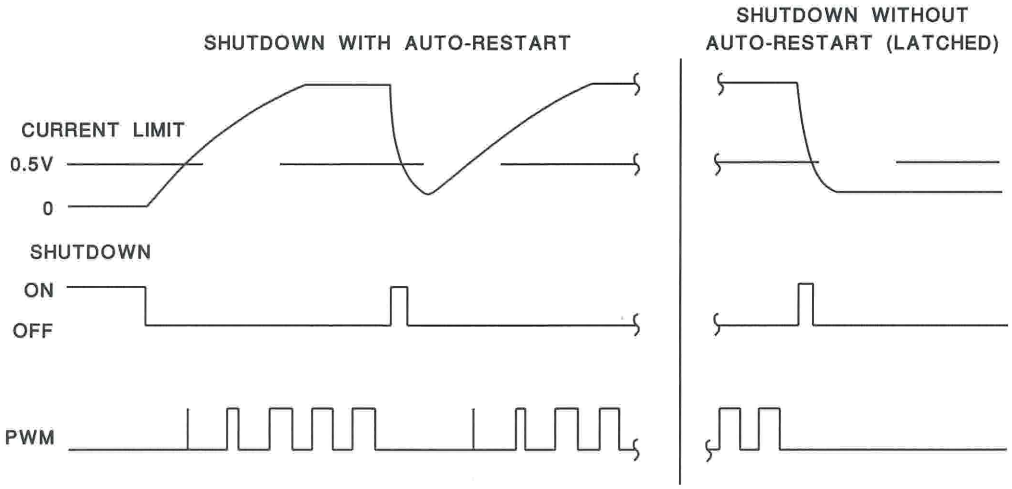


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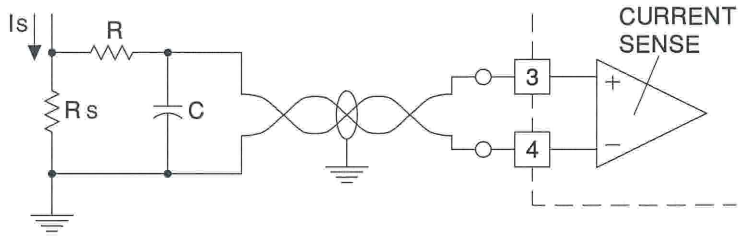
If $\frac{V_{REF}}{R1}$ < 0.8mA, the shutdown latch will commutate when $I_{SS}$ = 0.8mA and a restart cycle will be initiated.

If $\frac{V_{REF}}{R1}$ > 3mA, the device will latch off until power is recycled.

### Current Sense Amplifier Connections

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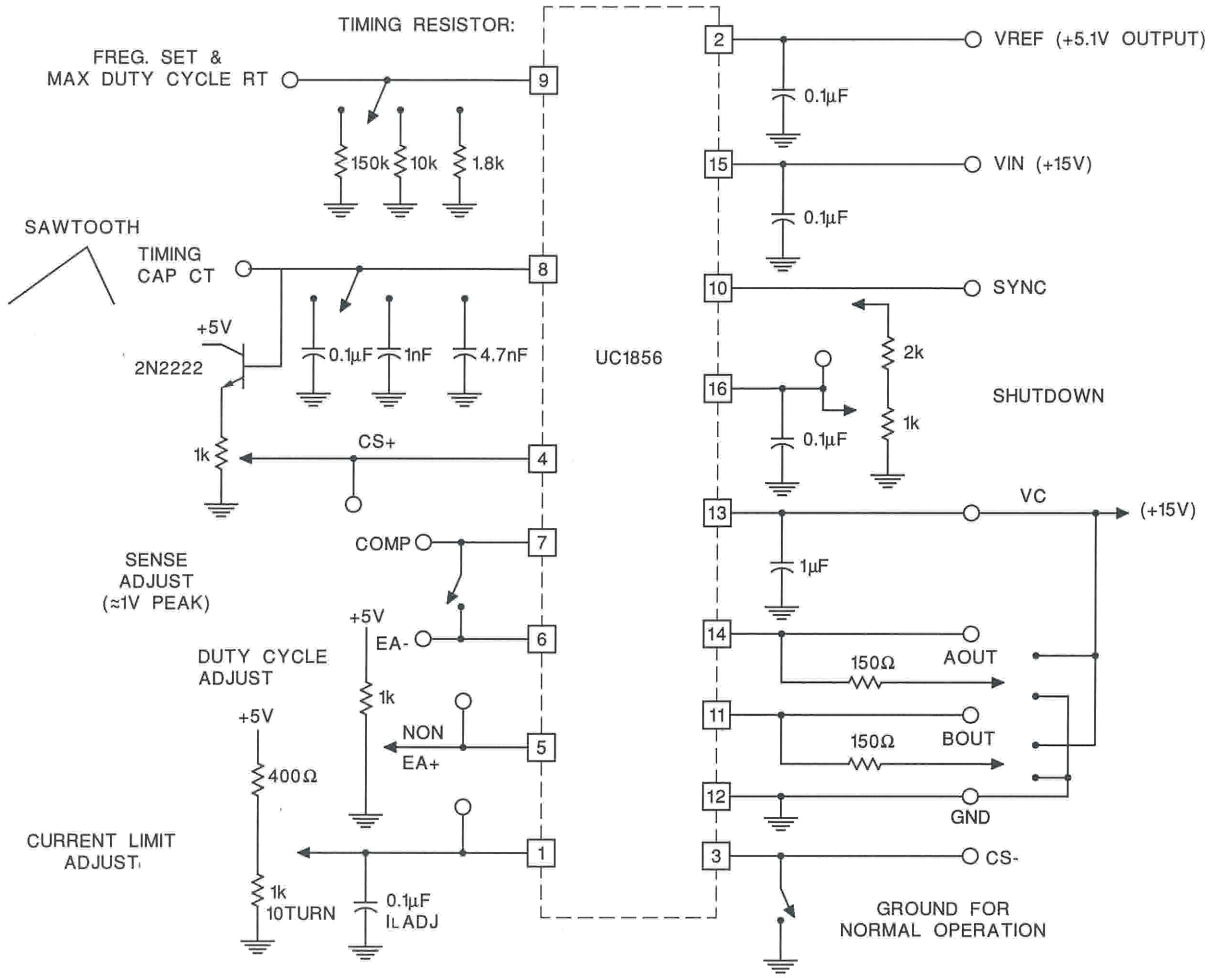
A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise sensing.

## APPLICATIONS INFORMATION (cont.)

### UC1856 Open Loop Test Circuit




- BYPASS CAPS SHOULD BE LOW ESR & ESL TYPE
- SHORT E/A- & COMP FOR UNITY GAIN TESTING

**THE USE OF A GROUND PLANE IS HIGHLY RECOMMENDED**

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9453001M2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9453001M2A UC1856L20/ 883B | Samples |
| 5962-9453001MEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9453001MEA UC1856J/883B | Samples |
| UC1856J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1856J | Samples |
| UC1856J883B | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9453001MEA UC1856J/883B | Samples |
| UC1856L20 | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1856L20 | Samples |
| UC1856L20883B | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9453001M2A UC1856L20/ 883B | Samples |
| UC2856DW | LIFEBUY | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2856DW | |
| UC2856DWG4 | LIFEBUY | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2856DW | |
| UC2856DWTR | LIFEBUY | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2856DW | |
| UC2856DWTRG4 | LIFEBUY | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2856DW | |
| UC2856J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -40 to 85 | UC2856J | Samples |
| UC2856N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | UC2856N | Samples |
| UC3856DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3856DW | Samples |
| UC3856DWTR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3856DW | Samples |
| UC3856N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3856N | Samples |
| UC3856NG4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3856N | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UC1856, UC2856, UC2856M, UC3856 :**

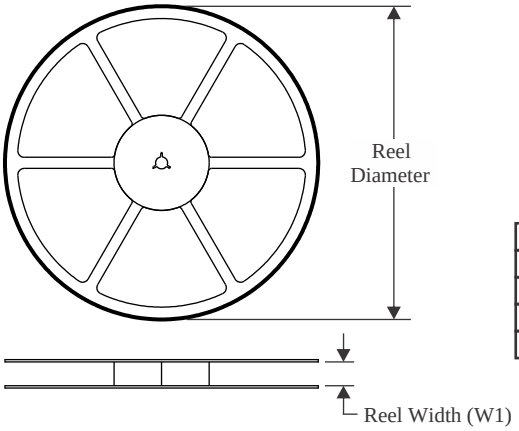
- Catalog : UC3856, UC2856
- Automotive : UC2856-Q1, UC2856-Q1
- Military : UC2856M, UC1856
- Space : UC1856-SP

NOTE: Qualified Version Definitions:

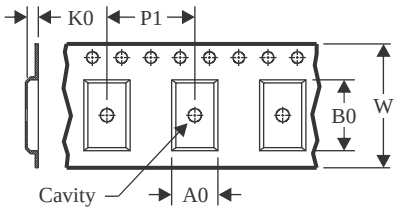
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

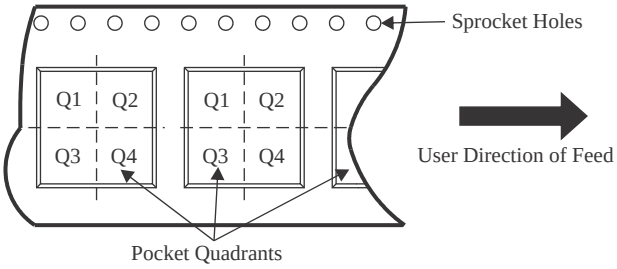



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

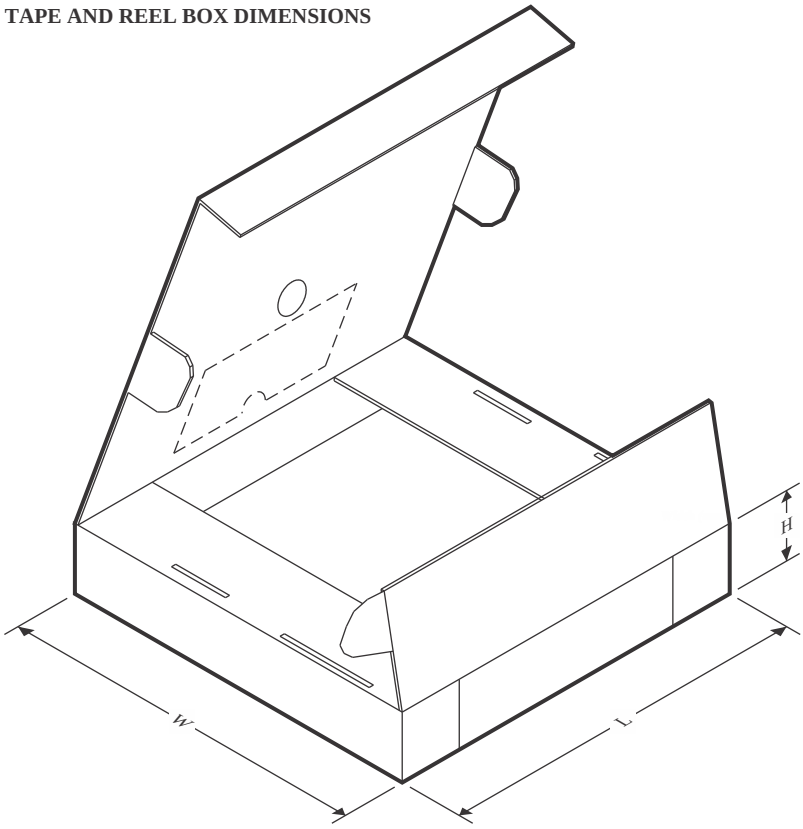
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2856DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3856DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

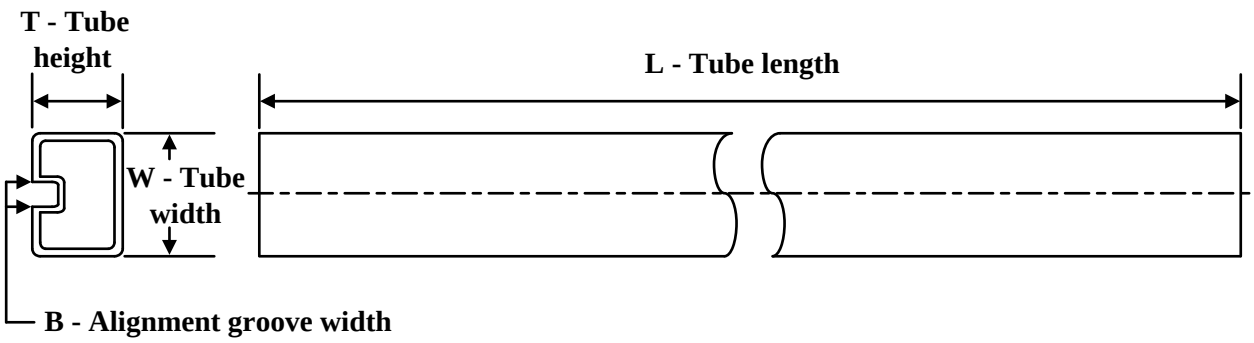
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2856DWTR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| UC3856DWTR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9453001M2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1856L20 | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1856L20883B | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC2856DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2856DWG4 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2856N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3856DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3856N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3856NG4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

# GENERIC PACKAGE VIEW

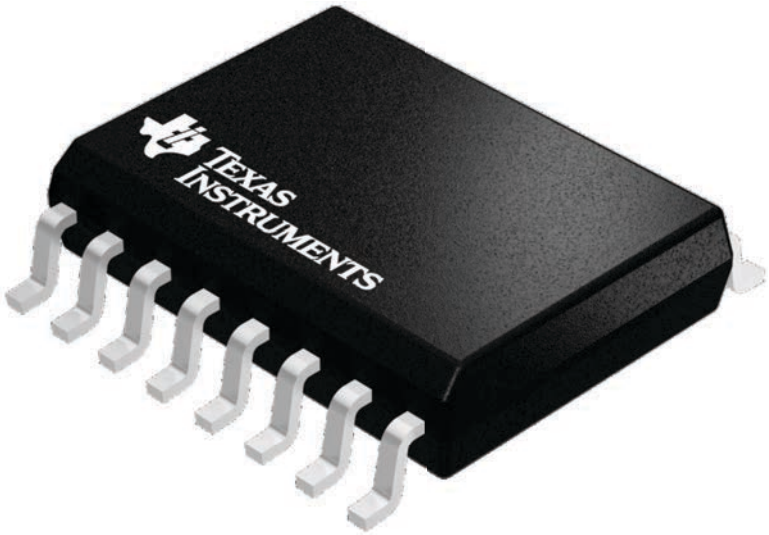
## DW 16

## SOIC - 2.65 mm max height

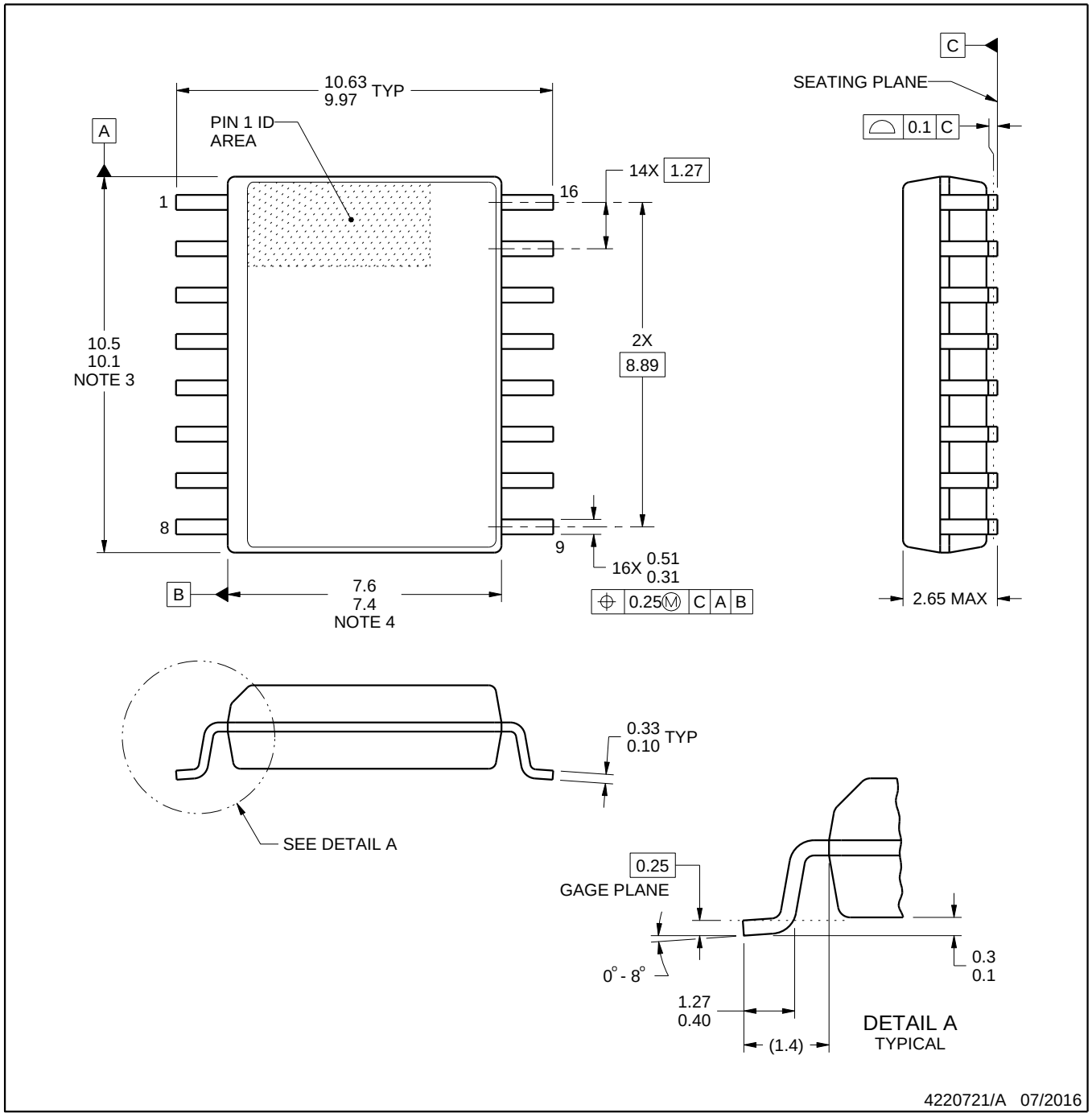
**7.5 x 10.3, 1.27 mm pitch**

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

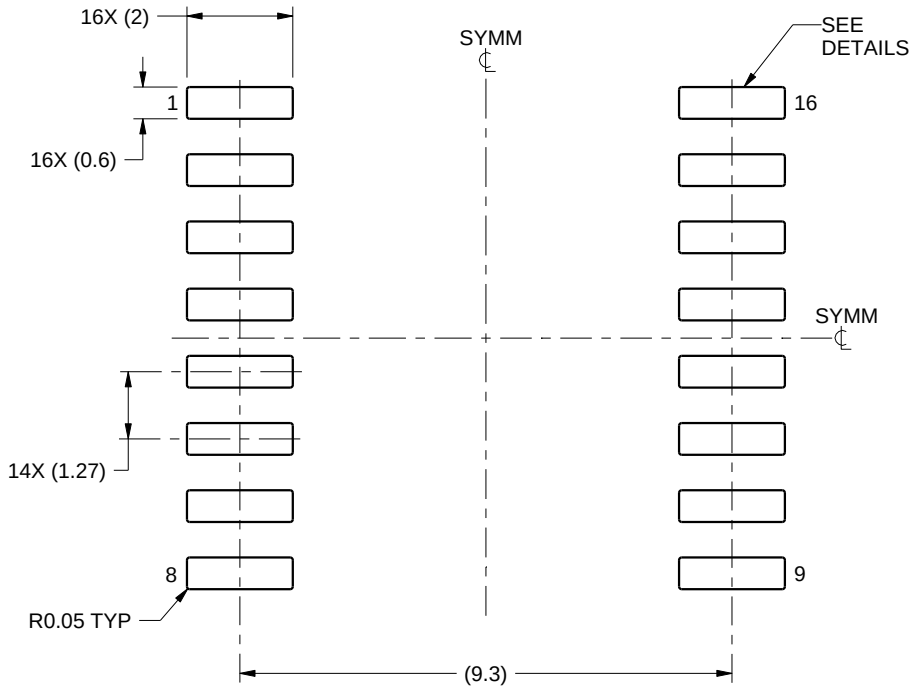



4224780/A

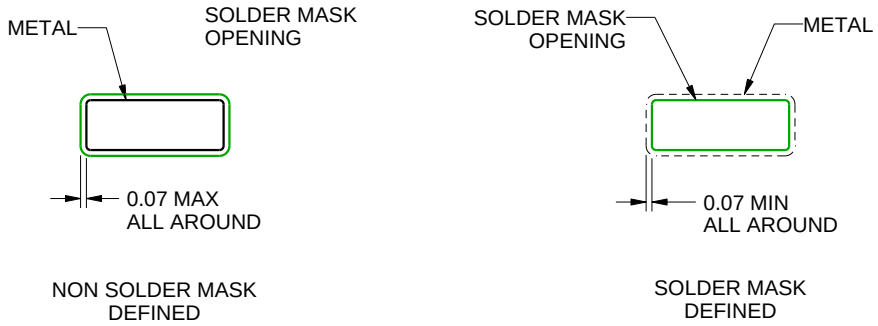



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:7X

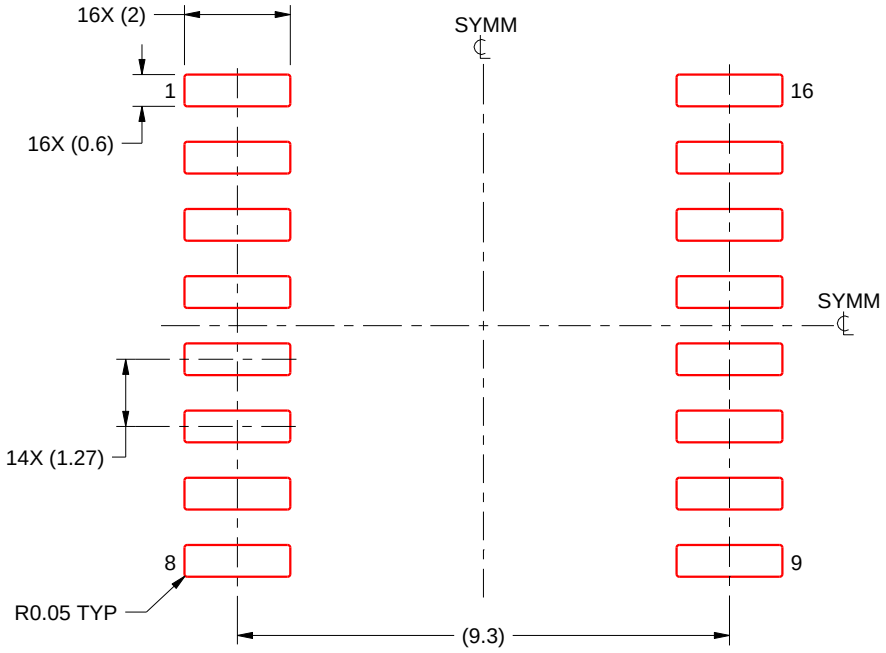



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

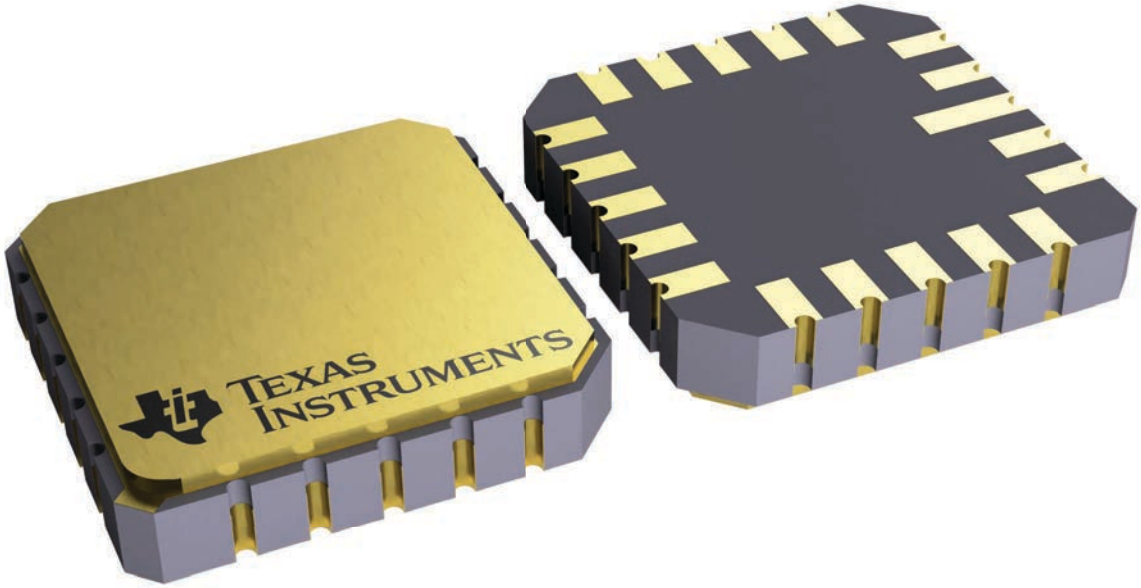
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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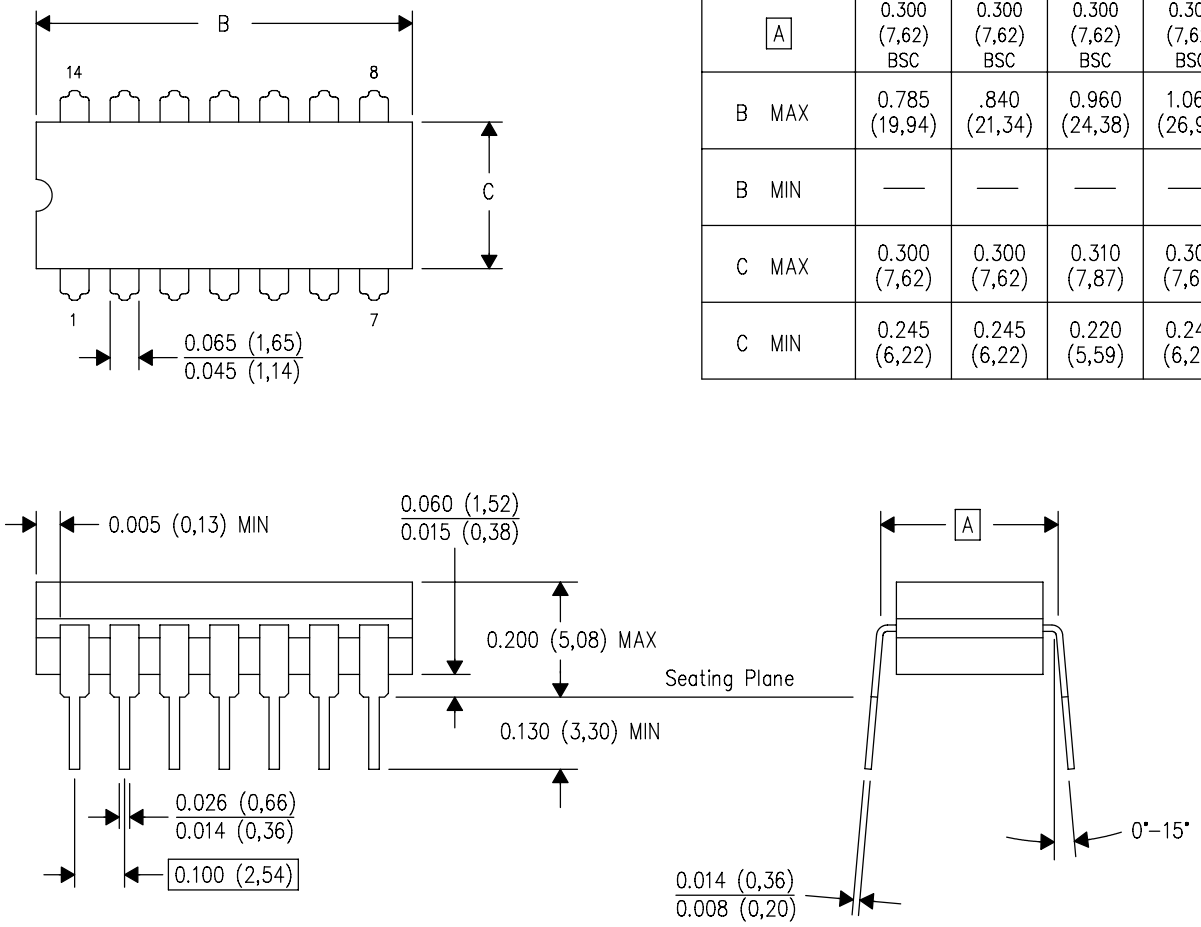
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



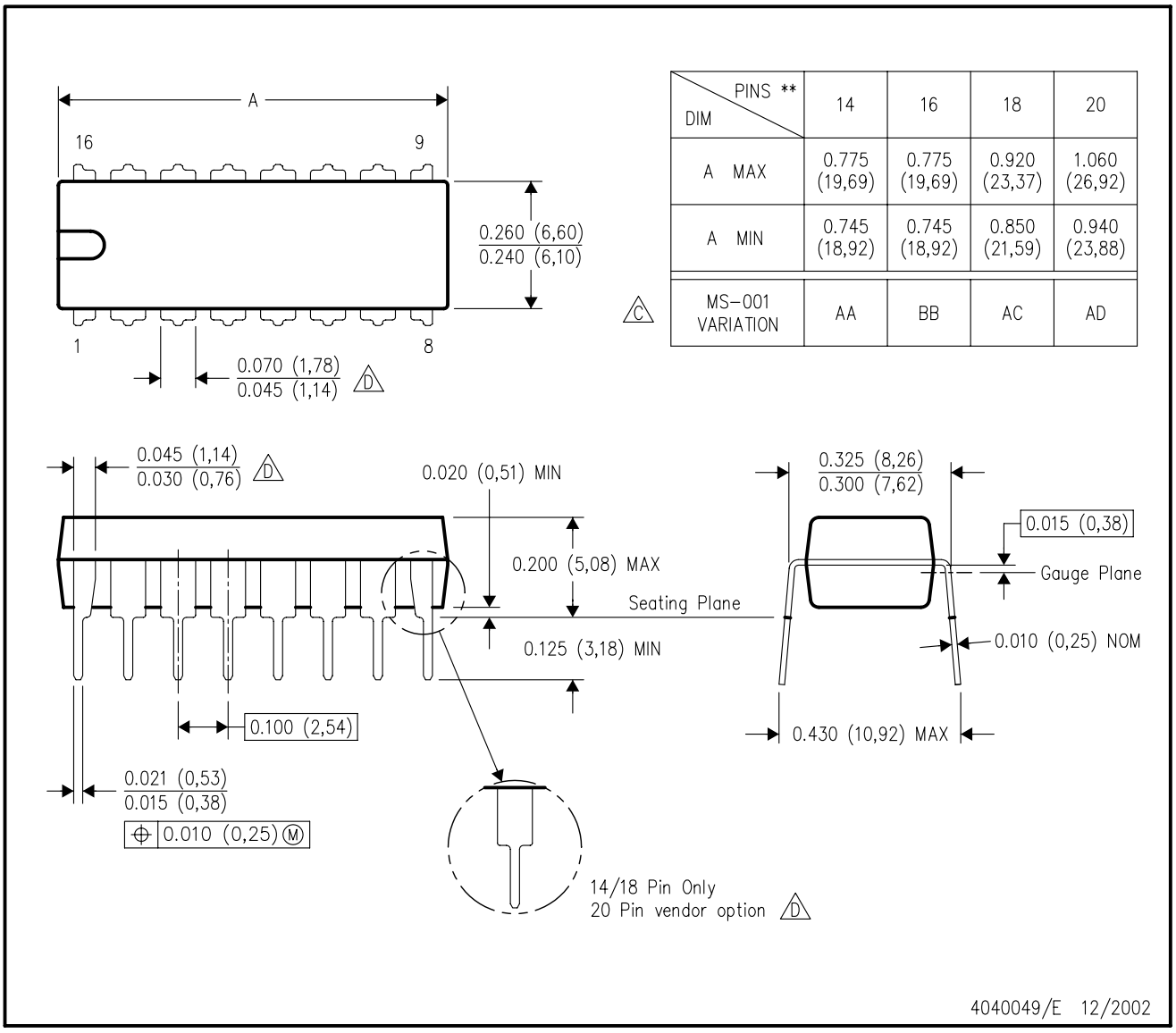

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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