TEXAS INSTRUMENTS
OPA607, OPA2607
JAJSI54J – OCTOBER 2019 – REVISED APRIL 2021

OPAx607 低コスト・システム用 50MHz、低消費電力、レール・ツー・レール出力 CMOS オペアンプ

1 特長

- ゲイン帯域幅積 (GBW):50MHz
- 静止電流:900µA (標準値)
- 広帯域ノイズ:3.8nV/√Hz
- 入力オフセット・ドリフト:1.5µV/℃以下
- オフセット電圧:120µV (標準値)
- 入力バイアス電流:10pA 以下
- レール・ツー・レール出力 (RRO)
- 不完全補償型、ゲイン 6V/V 以上 (安定)
- パワー・ダウン電流:1µA 以下
- 電源電圧範囲:2.2V～5.5V

2 アプリケーション

- 電流センシング
- 魚群探知器とソナー
- 超音波流量計
- 園芸用器具と電動工具
- プリンタ
- ライト・カーテンと安全ガード
- 光モジュール
- ハンドヘルド・テスト機器
- PM2.5 および PM10 パーティクル・センサ

3 概要

OPA607 および OPA2607 デバイスは、最小 6V/V のゲインで安定に動作する、ノイズが 3.8nV/√Hz、GBW が 50MHz の不完全補償型汎用 CMOS オペアンプです。OPAx607 デバイスは低ノイズで広い帯域幅を持っているため、コストと性能を両立させる必要がある汎用アプリケーションに最適です。高インピーダンスの CMOS 入力を備えた OPAx607 デバイスは、高い出力インピーダンスを持つセンサ (圧電トランスデューサなど) と接続するのに理想的なアンプです。

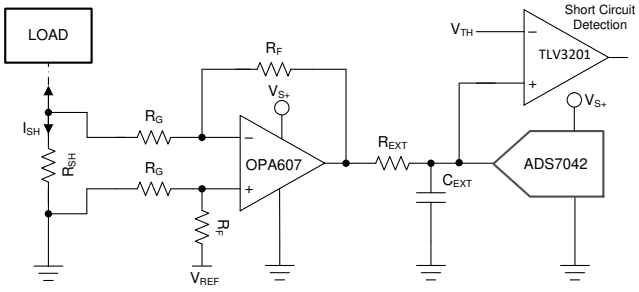
OPAx607 デバイスは、最大静止電流が 1µA 未満のパワーダウン・モードを備えているため、ポータブル・バッテリ駆動アプリケーションに適しています。OPAx607 デバイスのレール・ツー・レール出力 (RRO) は、電源レールから 8mV の電圧まで出力振幅を拡大できるため、ダイナミック・レンジを最大限に広げることができます。

最小 2.2V (±1.1V)、最大 5.5V (±2.75V) の電圧で動作するよう最適化されており、工業用拡張温度範囲の –40℃～+125℃での動作が規定されています。

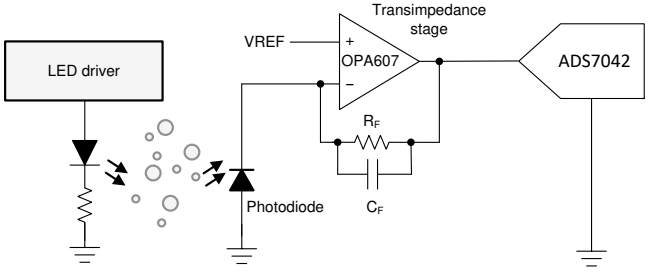
製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
OPA607	SC70 (6)	2.00mm × 1.25mm
	SOT23 (5)	2.90mm × 1.60mm
OPA2607	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
	X2QFN (10)	1.50mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



OPAx607 による電流センシングのアプリケーション



OPAx607 によるトランスインピーダンスのアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (February 2021) to Revision J (April 2021) — **Page**

- *「製品情報」表の* VSSOP (8) および X2QFN (10) パッケージからプレビューの記述を削除 ... 1
- Removed the preview statement from the OPA2607 X2QFN (RUG) package and VSSOP (DGK) in the *Device Comparison* section ... 4
- Removed the preview statement from the OPA2607 D, DGK and OPA2607 RUG package in the *Pin Configuration and Functions* section ... 5

Changes from Revision H (December 2020) to Revision I (February 2021) — **Page**

- データシートのタイトルを更新 ... 1

Changes from Revision G (October 2020) to Revision H (December 2020) — **Page**

- Updated the I/O and Descriptions in the *Pin Functions—Single Channel* table ... 5

Changes from Revision F (September 2020) to Revision G (October 2020) — **Page**

- Removed the *RUG Package 8-Pin X2QFN* pinout to the *Pin Configuration and Functions* section ... 5
- Removed the *N/C* pin decription from the *Pin Functions – Single Channel* table ... 5
- Changed Overdrive Recovery Time from 0.25µs to 0.3µs ... 9
- Updated the Turn-On and Turn-Off Time figure in the *Typical Characteristics* section ... 11
- Updated the Power Down Pin Bias Current vs Power Down Pin Voltage figure in the *Typical Characteristics* section ... 11
- Updated the Input Offset Voltage vs Temperature figure in the *Typical Characteristics* section ... 11
- Updated the Common Mode Rejection Ratio vs Temperature figure in the *Typical Characteristics* section ... 11
- Updated the Short-Circuit Current vs Temperature figure in the *Typical Characteristics* section ... 11
- Updated the Input Bias and Offset Current vs Temperature figure in the *Typical Characteristics* section ... 11
- Updated the Output Voltage vs Output Current Sourcing and Sinking figure in the *Typical Characteristics* section ... 11
- Added the Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency figure to the *Typical Characteristics* section ... 11
- Added the Crosstalk vs Frequency figure to the *Typical Characteristics* section ... 11
- Added the Quiescent Current vs Temperature figure to the *Typical Characteristics* section ... 11

Changes from Revision E (August 2020) to Revision F (September 2020) **Page**

- Deleted blank CMRR specifications from Electrical Characteristics table..... 9

Changes from Revision D (May 2020) to Revision E (August 2020) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新..... 1
- OPA2607 SOIC (8) パッケージのステータスを*プレビュー*から*アクティブに変更* 1

Changes from Revision C (April 2020) to Revision D (May 2020) **Page**

- ステータスを事前情報から *量産データに変更* 1

5 Device Comparison

DEVICE	NO. OF CHANNELS	PACKAGE LEADS				
		SOIC (D)	X2QFN (RUG)(1)	VSSOP (DGK)	SC-70 (DCK)(1)	SOT-23 (DBV)
OPA607	1	—	—	—	6(1)	5
OPA2607	2	8	10(1)	8	—	—

(1) Package with Power Down mode.

DEVICE	INPUT	OFFSET DRIFT (µV/°C, TYP)	MINIMUM STABLE GAIN (V/V)	I_Q / CHANNEL (mA, TYP)	GBW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)
OPAx365	CMOS	1	1	4.6	50	25	4.5
OPAx607	CMOS	0.3	6	0.9	50	24	3.8
OPAx837	Bipolar	0.4	1	0.6	50	105	4.7

6 Pin Configuration and Functions

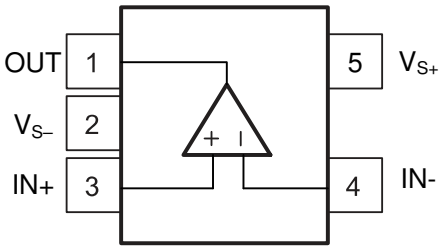


図 6-1. DBV Package
5-Pin SOT-23
Top View

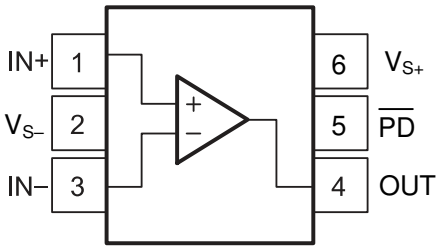


図 6-2. DCK Package
6-Pin SC70
Top View

Pin Functions – Single Channel

PIN			I/O	DESCRIPTION
NAME	DBV	DCK		
IN–	4	3	I	Inverting input
IN+	3	1	I	Non inverting input
OUT	1	4	O	Output
$\overline{PD}$	—	5	I	Power down (can be left floating)
V_{S-}	2	2	—	Negative supply or ground (for single-supply operation)
V_{S+}	5	6	—	Positive supply

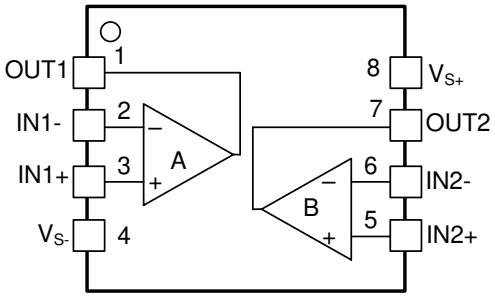


図 6-3. OPA2607 D, DGK Package
8-Pin SOIC, VSSOP
Top View

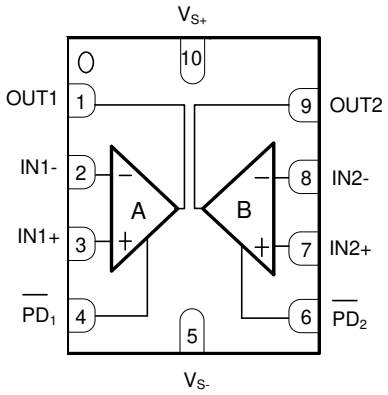


図 6-4. OPA2607 RUG Package
10-Pin X2QFN
Top View

Pin Functions – Dual Channel

PIN			I/O	DESCRIPTION
NAME	D, DGK	RUG		
IN1–	2	2	I	Inverting input, channel 1
IN1+	3	3	I	Noninverting input, channel 1
IN2–	6	8	I	Inverting input, channel 2
IN2+	5	7	I	Noninverting input, channel 2
OUT1	1	1	O	Output, channel 1
OUT2	7	9	O	Output, channel 2
$V_{S–}$	4	5	—	Negative (lowest) supply or ground (for single-supply operation)
V_{S+}	8	10	—	Positive (highest) supply
$\overline{PD1}$	—	4	I	Low = amplifier 1 disabled, high = amplifier 1 enabled; see the *Power Down Mode* section for more information.
$\overline{PD2}$	—	6	I	Low = amplifier 2 disabled, high = amplifier 2 enabled; see the *Power Down Mode* section for more information.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$(V_{S+}) – (V_{S–})$	Supply voltage, V_s		6	V
V_{IN+}, $V_{IN–}$	Input voltage	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
$V_{\overline{PD}}$	$\overline{PD}$ voltage	$(V_{S–}) – 0.5$	6	V
V_{ID}	Differential input voltage(4)		±5	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±20	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Long term drift of offset voltage (> 1mV) if a differential input in excess of ≈ 2V is applied continuously between the IN+ and IN- pins at elevated temperatures.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		D Package , Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage $(V_{S+}) – (V_{S–})$	2.2		5.5	V
		±1.1		±2.75	
T_A	Ambient operating temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPAx607					UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT23)	DCK (SC70)	RUG (X2QFN)	
		8 PINS	8 PINS	5 PINS	6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.1	179	196.5	219.7	152	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.2	71	118.7	182.6	58	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.5	101	64.5	105.7	77	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.5	13	41.1	87	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.3	100	64.2	105.4	77	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At T_A = 25°C, V_S = 2.2 V to 5.5 V, G = 6 V/V[5], R_F = 5 kΩ, C_F = 2.5 pF, V_{CM} = (V_S / 2) – 0.5 V, C_L = 10 pF, R_L = 10 kΩ connected to (V_S / 2) – 0.5 V, and, $\overline{PD}$ connected to (V_{S+}) (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		–0.6	0.12	0.6	mV
	Input offset voltage	T_A = –40°C to +125°C	–0.7	0.12	0.7	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±0.3	±1.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.2 V to 5.5 V	95	120		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		($V_{S–}$)		(V_{S+})–1.1	V
CMRR	Common-mode rejection ratio[3]	($V_{S–}$) < V_{CM} < (V_{S+}) – 1.1 V	90	100		dB
INPUT BIAS CURRENT						
I_B	Input bias current[2]			±3	±10	pA
		T_A = –40°C to 125°C		See Fig. 29		
I_{OS}	Input offset current[2]			±3	±10	
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		1.6		μV_{PP}
e_N	Input voltage noise density	f = 10 kHz, 1/f corner at 1 kHz		3.8		nV/√Hz
i_N	Input current noise density	f = 1 kHz		46		fA/√Hz
INPUT IMPEDANCE						
C_{IN}	Differential			11.5		pF
	Common-mode			5.5		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain[3]	($V_{S–}$) + 400 mV < V_{OUT} < (V_{S+}) – 400 mV	110	130		dB
	Phase margin			65		°
AC Characteristics (V_S = 5 V)						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mVpp		9		MHz
GBW	Gain-bandwidth product	G = 20 V/V		50		
SR	Slew rate	3-V output step (10-90%), V_{OCM} = mid-supply		24		V/µs
t_S	Settling time	To 0.1%, 3-V step, G = 40, V_{OCM} = mid-supply		1		µs
		To 0.01%, 3-V step, G = 40, V_{OCM} = mid-supply		1.8		
	Overdrive recovery time	V_{IN+} × Gain > V_S		0.3		µs
THD + N	Total Harmonic Distortion + Noise[6]	V_{OUT} = 2 V_{PP}, f = 1 kHz , R_L = 10 kΩ		-103		dB
		V_{OUT} = 2 V_{PP}, f = 20 kHz , R_L = 10 kΩ		-91.5		
		V_{OUT} = 2 V_{PP}, f = 1 kHz , R_L = 1 kΩ		-96		
		V_{OUT} = 2 V_{PP}, f = 20 kHz , R_L = 1 kΩ		-72.8		
HD2	Second-order harmonic distortion	V_{OUT} = 2 V_{PP} f = 20 kHz		-105		dBc
HD3	Third-order harmonic distortion	V_{OUT} = 2 V_{PP} f = 20 kHz		-95		
	Channel-to-channel crosstalk	V_{OUT} = 2 V_{PP}, f = 100 kHz		-114		dBc

7.5 Electrical Characteristics (continued)

At T_A = 25°C, V_S = 2.2 V to 5.5 V, G = 6 V/V(5), R_F = 5 kΩ, C_F = 2.5 pF, V_{CM} = (V_S / 2) – 0.5 V, C_L = 10 pF, R_L = 10 kΩ connected to (V_S / 2) – 0.5 V, and, $\overline{PD}$ connected to (V_{S+}) (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Output voltage swing from supply rails			8	12	mV
		T_A = – 40°C to +125°C			12	
I_{SC}	Output Short-circuit current			60		mA
Z_O	Open-loop output impedance	f = 1 MHz		500		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		900	1100	µA
		I_O = 0 mA, T_A = –40°C to +125°C			1200	
POWER DOWN (Device Enabled When Floating)						
	Power Down quiescent current per amplifier(4)	$\overline{PD}$ = $V_{S–}$		750	1000	nA
	Power Down pin bias current per amplifier(7)	$\overline{PD}$ = $V_{S–}$		–750	–1000	
	Enable voltage threshold	Logic-High threshold			0.7 x V_S	V
	Disable voltage threshold	Logic-Low threshold	0.2 x V_S			
t_{ON}	Turn-on time delay(2)			10	15	µs
t_{OFF}	Turn-off time delay			0.5		

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization or both ; not production tested.
(3) Production Tested at V_S = 5.5V
(4) In Power Down mode current drawn by the opamp is equal to the bias current sourced on the $\overline{PD}$ pin
(5) All Gains (G) mentioned are in V/V unless otherwise noted.
(6) Lowpass-filter bandwidth is 92kHz for f = 20 kHz and 20 kHz for f = 1 kHz.
(7) Negative value of the Power Down bias current indicates current being sourced from the opamp's $\overline{PD}$ pin towards external circuit.

7.6 Typical Characteristics

At T_A = +25°C, V_S = 5.5 V, R_L = 10 kΩ, R_F= 5 kΩ, C_F= 2.5 pF, V_{CM} = midsupply – 0.5 V, G = 6 V/V (unless otherwise noted).

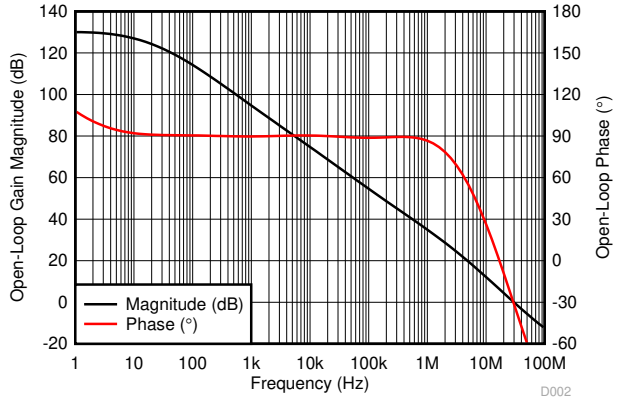


図 7-1. Open Loop Gain and Phase vs Frequency

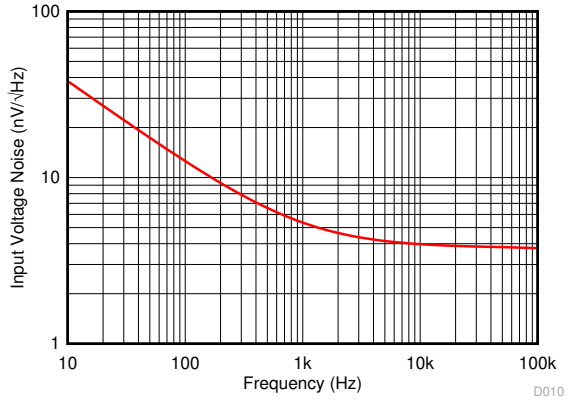


図 7-2. Input Voltage Noise Density vs Frequency

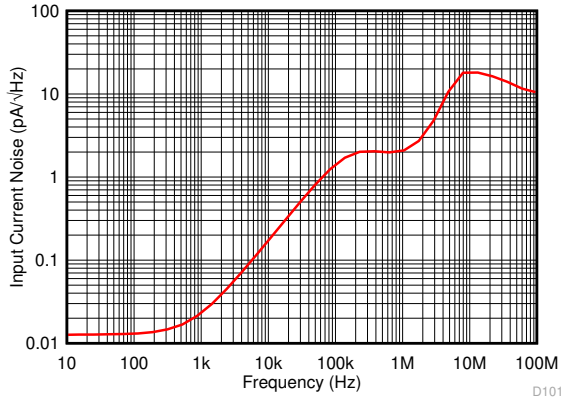
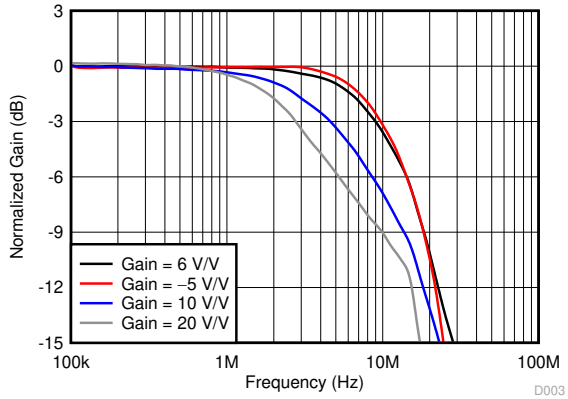
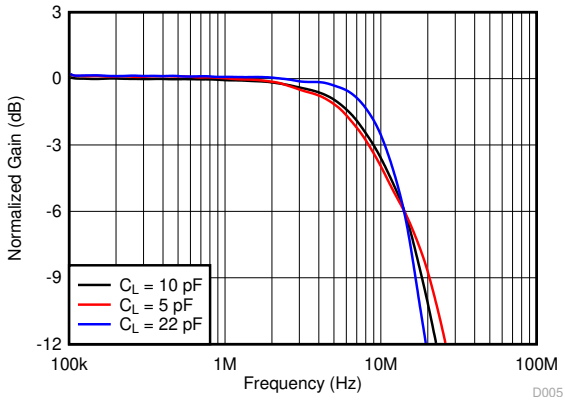


図 7-3. Input Current Noise Density vs Frequency



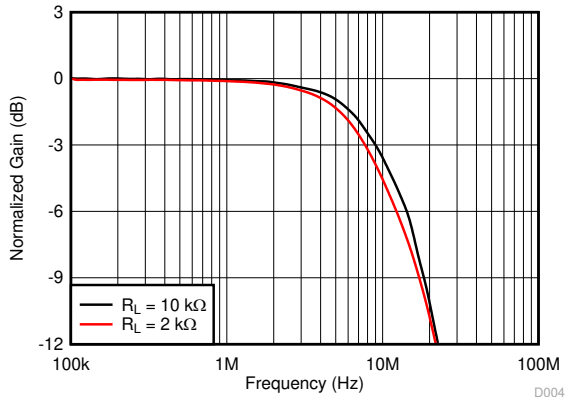
V_{OUT} = 20 mV_{PP}

図 7-4. Small-Signal Frequency Response vs Gain



V_{OUT} = 20 mV_{PP}

図 7-5. Small-Signal Frequency Response vs Capacitive Load



V_{OUT} = 20 mV_{PP}

図 7-6. Small-Signal Frequency Response vs Output Load

7.6 Typical Characteristics (continued)

At T_A = +25°C, V_S = 5.5 V, R_L = 10 kΩ, R_F= 5 kΩ, C_F= 2.5 pF, V_{CM} = midsupply – 0.5 V, G = 6 V/V (unless otherwise noted).

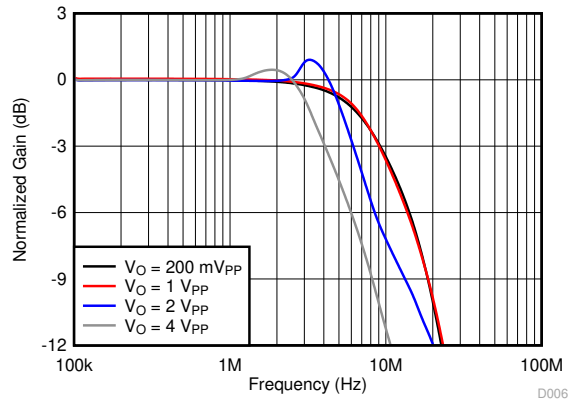


図 7-7. Large-Signal Frequency Response vs Output Voltage

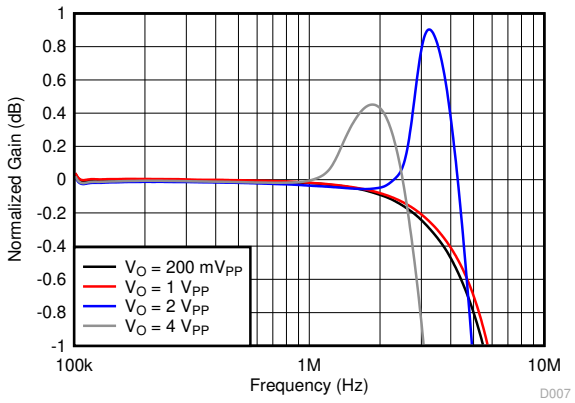
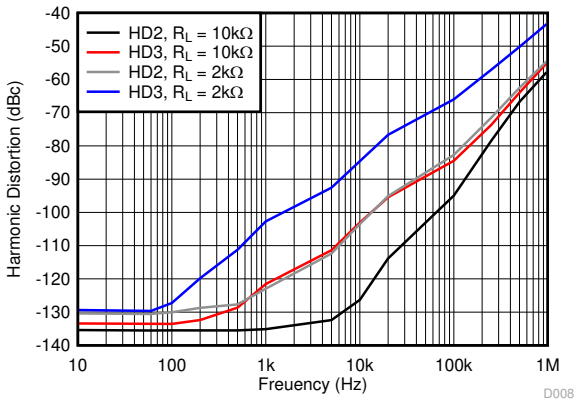
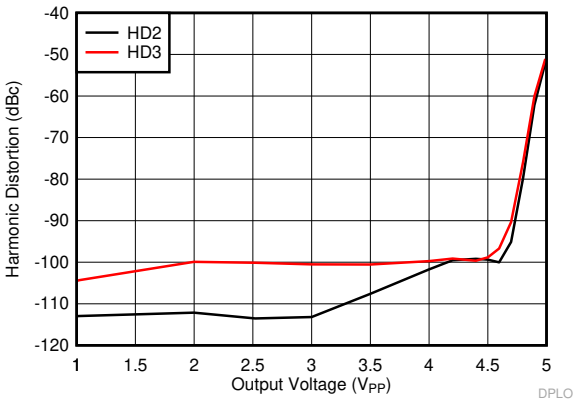


図 7-8. Large-Signal Response Flatness vs Frequency



V_{OUT} = 2 V_{PP}

図 7-9. Harmonic Distortion vs Frequency



Frequency = 20 kHz

図 7-10. Harmonic Distortion vs Output Voltage

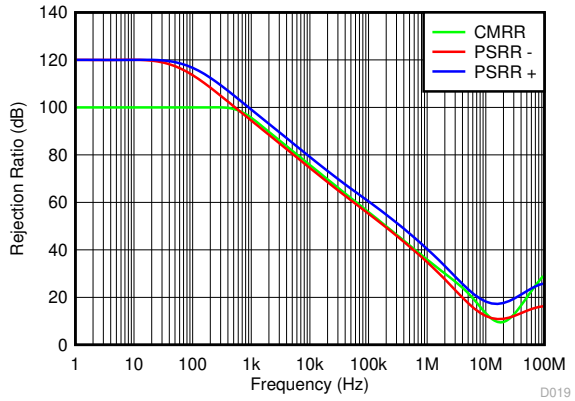


図 7-11. Rejection Ratio vs frequency

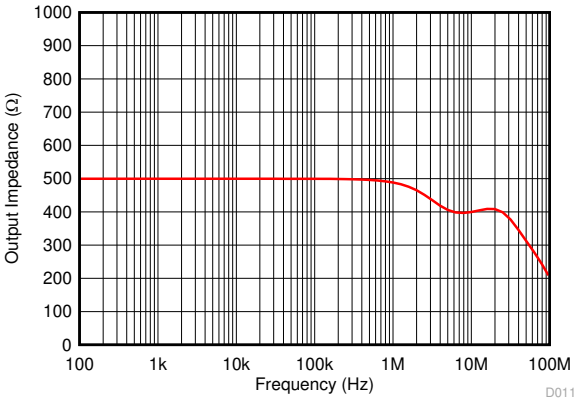


図 7-12. Open Loop Output Impedance vs Frequency

7.6 Typical Characteristics (continued)

At T_A = +25°C, V_S = 5.5 V, R_L = 10 kΩ, R_F= 5 kΩ, C_F= 2.5 pF, V_{CM} = midsupply – 0.5 V, G = 6 V/V (unless otherwise noted).

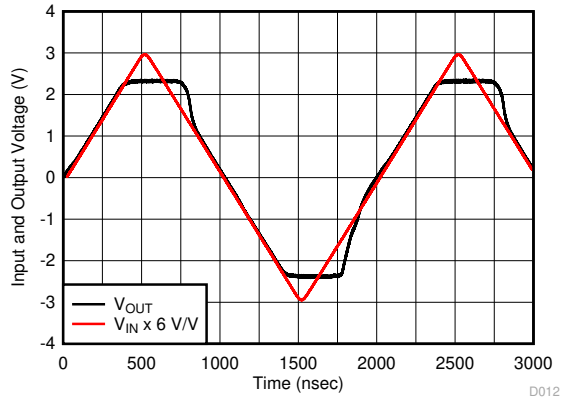
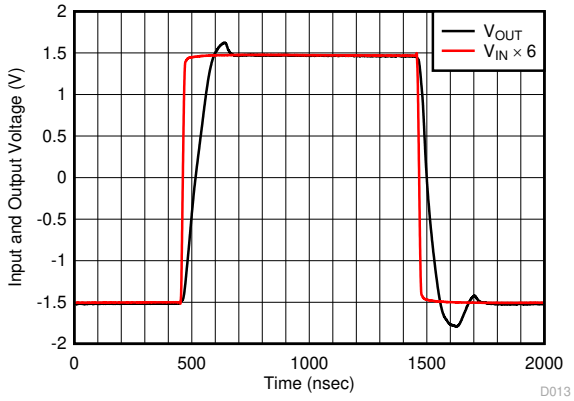
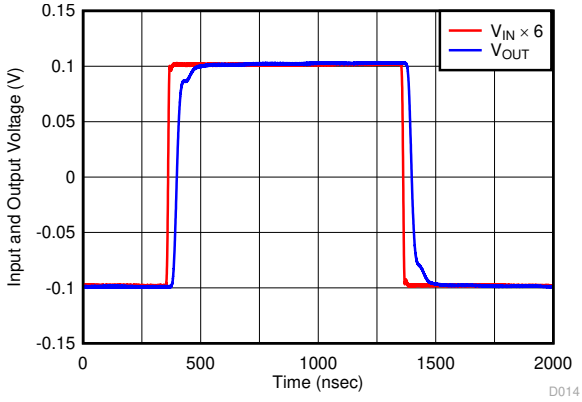


図 7-13. Output Overdrive Recovery



T_{RISE} = 1 µsec , T_{FALL} = 0.7 µsec

図 7-14. Large-Signal Transient Response



T_{RISE} = T_{FALL} = 40 nsec

図 7-15. Small-Signal Transient Response

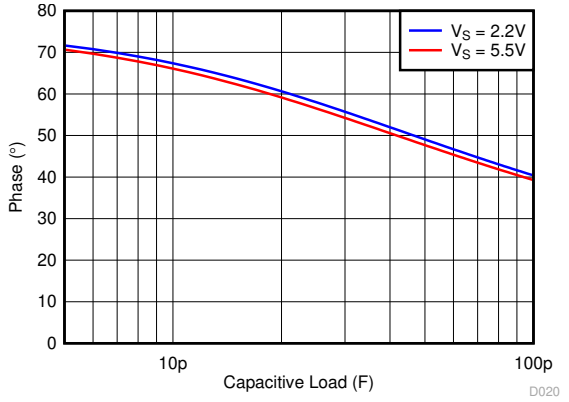
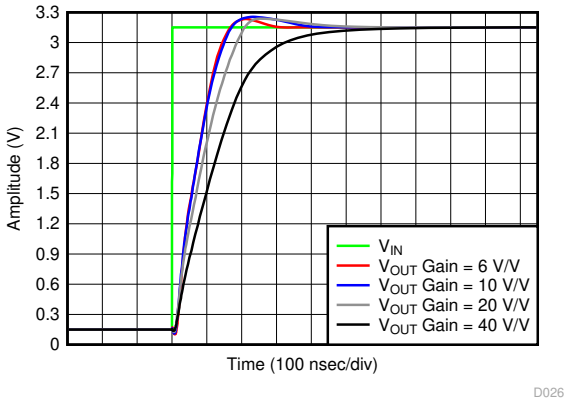


図 7-16. Phase Margin vs Capacitive Load



Simulated

図 7-17. Step Settling Time

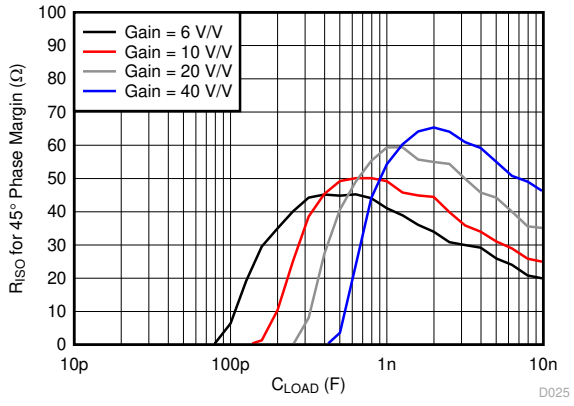
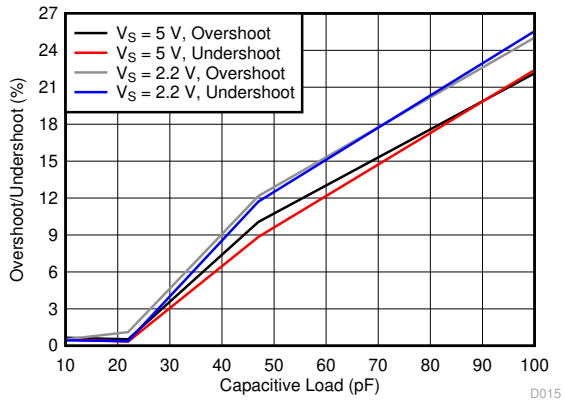


図 7-18. Recommended Isolation Resistor vs Capacitive Load

7.6 Typical Characteristics (continued)

At T_A = +25°C, V_S = 5.5 V, R_L = 10 kΩ, R_F= 5 kΩ, C_F= 2.5 pF, V_{CM} = midsupply – 0.5 V, G = 6 V/V (unless otherwise noted).



V_{OUT} = 200 mV_{PP}

図 7-19. Overshoot vs Capacitive Load

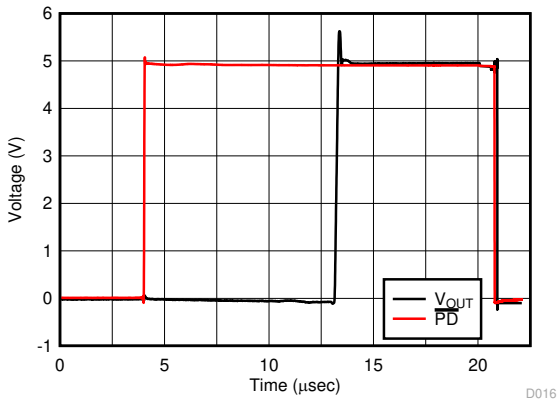


図 7-20. Turn-On and Turn-Off Time

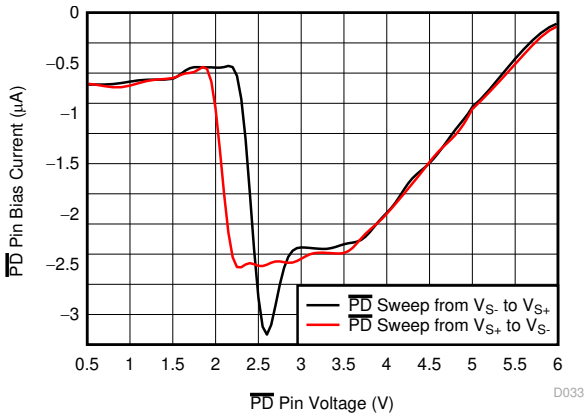
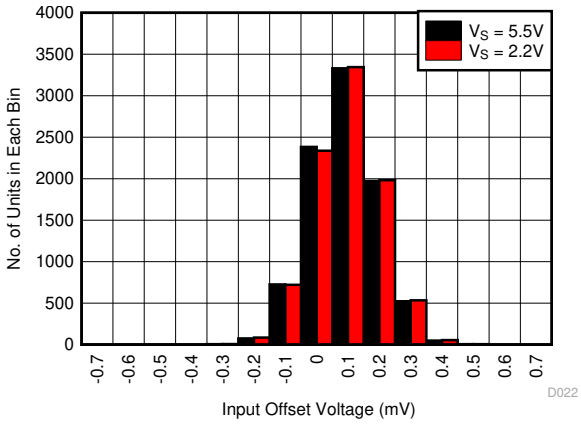
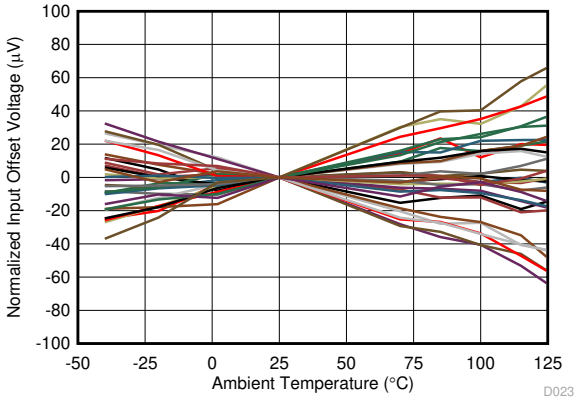


図 7-21. Power Down Pin Bias Current vs Power Down Pin Voltage



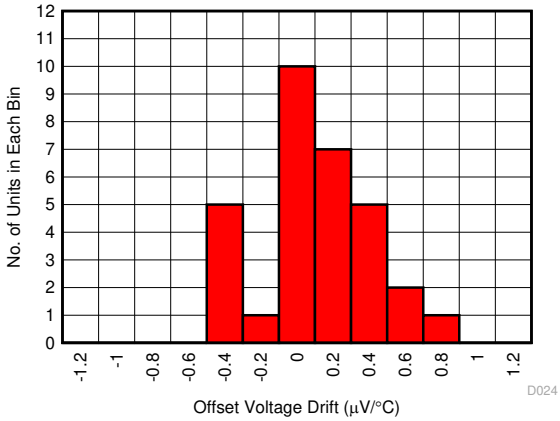
9000 units

図 7-22. Input Offset Voltage Distribution



32 Units, Normalized to
V_{OS} = 0V at 25°C

図 7-23. Input Offset Voltage vs Temperature

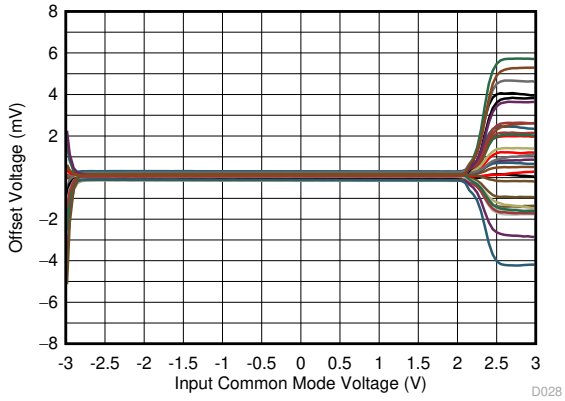


32 Units, –40°C to
+125°C

図 7-24. Input Offset Drift Distribution

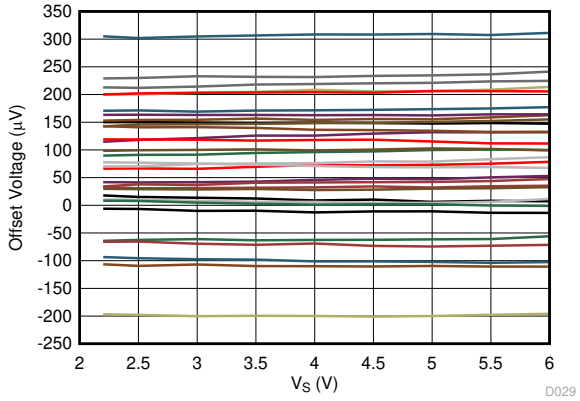
7.6 Typical Characteristics (continued)

At T_A = +25°C, V_S = 5.5 V, R_L = 10 kΩ, R_F= 5 kΩ, C_F= 2.5 pF, V_{CM} = midsupply – 0.5 V, G = 6 V/V (unless otherwise noted).



V_S = ±2.75 V

図 7-25. Input Offset vs Common Mode Voltage



32 Units

図 7-26. Input Offset vs Supply

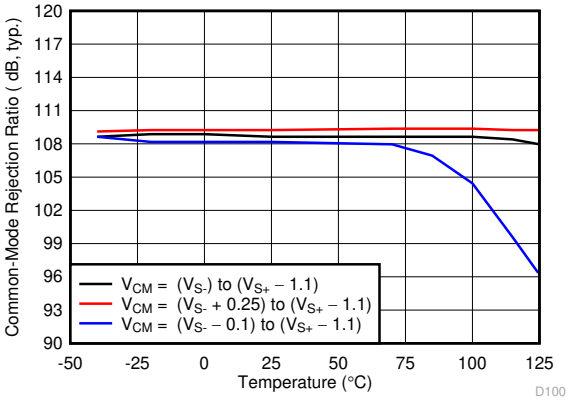


図 7-27. Common Mode Rejection Ratio vs Temperature

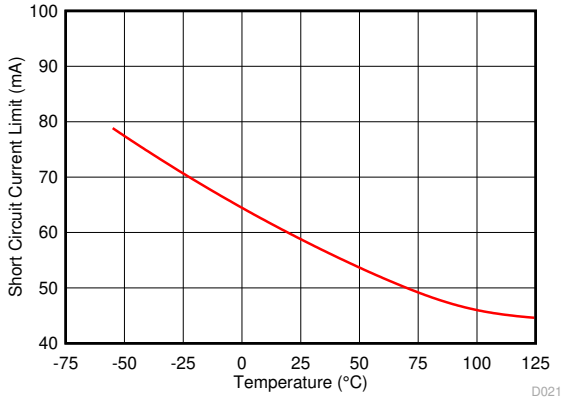


図 7-28. Short-Circuit Current vs Temperature

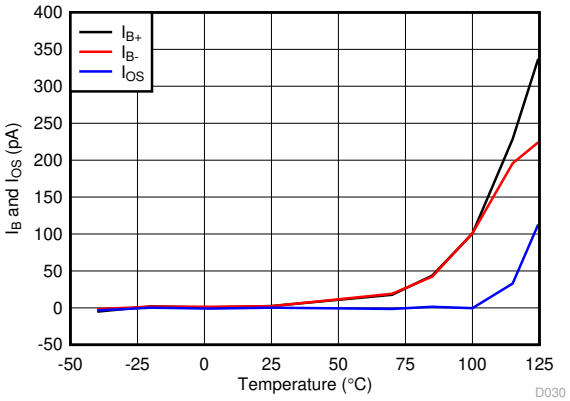


図 7-29. Input Bias and Offset Current vs Temperature

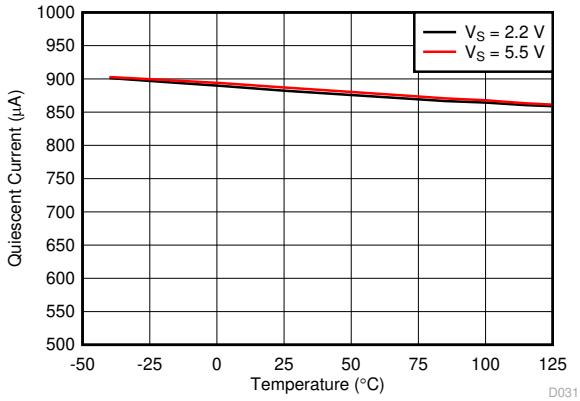


図 7-30. Quiescent Current vs Temperature

7.6 Typical Characteristics (continued)

At T_A = +25°C, V_S = 5.5 V, R_L = 10 kΩ, R_F= 5 kΩ, C_F= 2.5 pF, V_{CM} = midsupply – 0.5 V, G = 6 V/V (unless otherwise noted).

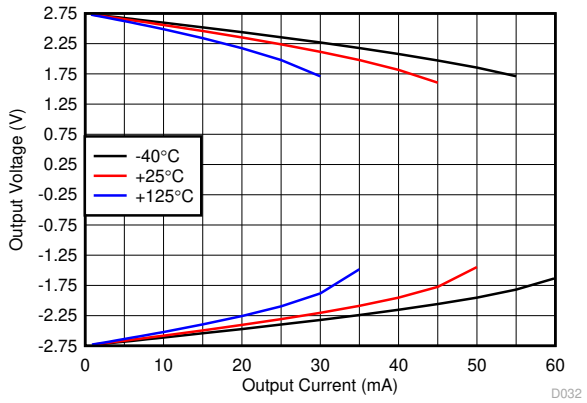


図 7-31. Output Voltage vs Output Current Sourcing and Sinking

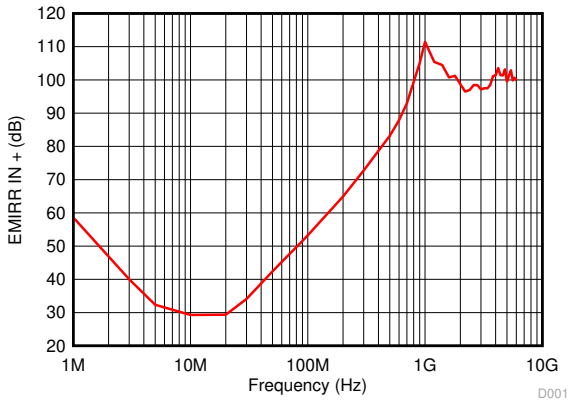


図 7-32. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

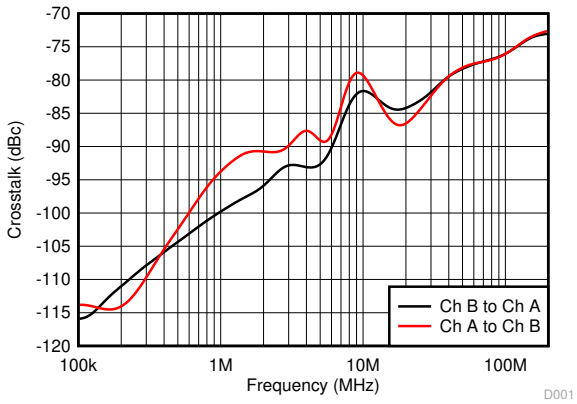


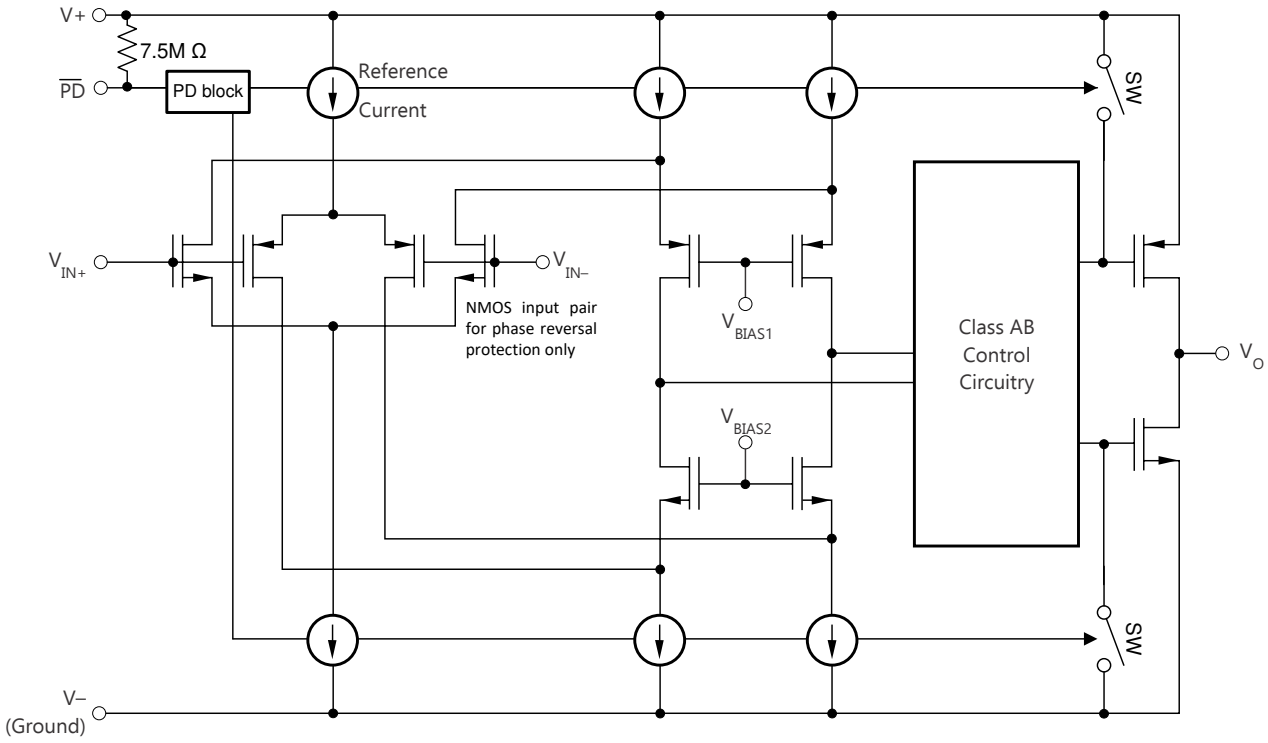
図 7-33. Crosstalk vs Frequency

8 Detailed Description

8.1 Overview

The OPAx607 devices are low-noise, rail-to-rail output (RRO) operational amplifiers (op amp). The devices operate from a supply voltage of 2.2 V to 5.5 V. The input common-mode voltage range also extends down to the negative rail allowing the OPAx607 to be used in most single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply, voltage-range applications, which results in complete usage of the full-scale range of the consecutive analog-to-digital converters (ADCs). The decompensated architecture allows for a favorable tradeoff of low-quiescent current for a very-high gain-bandwidth product (GBW) and low-distortion performance in high-gain applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPAx607 operational amplifiers are fully specified and assured for operation from 2.2 V to 5.5 V, applicable from –40°C to +125°C. The OPAx607 devices are completely operational with asymmetric, symmetric and single supply voltages applied across the supply pins. The total voltage (that is, (V_{S+}) – ($V_{S–}$)) must be less than the supply voltage mentioned in セクション 7.1.

8.3.2 Rail-to-Rail Output and Driving Capacitive Loads

Designed as a low-power, low-voltage operational amplifier, the OPAx607 devices are capable of delivering a robust output drive. For resistive loads of 10 kΩ, the output swings to within a few millivolts of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails. The OPAx607 devices drive up to a nominal capacitive load of 47 pF on the output with no special consideration and without the need of a series isolation resistor R_{ISO} while still being able to achieve 45° of phase margin. When driving capacitive loads greater than 47 pF, TI recommends using R_{ISO} as shown in 図 8-1 in series with the output as close to the device as possible. Refer to Recommended Isolation Resistor vs Capacitive Load for looking up different values of R_{ISO} required for C_L to achieve 45° phase margin. Without R_{ISO}, the external capacitance (C_L) interacts with the output impedance (Z_O) of the amplifier, resulting in stability issues. Inserting R_{ISO} isolates C_L from Z_O and restores the phase margin. 図 8-1 shows the test circuit.

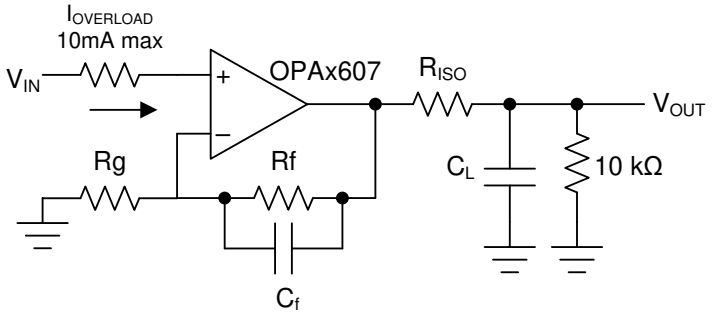
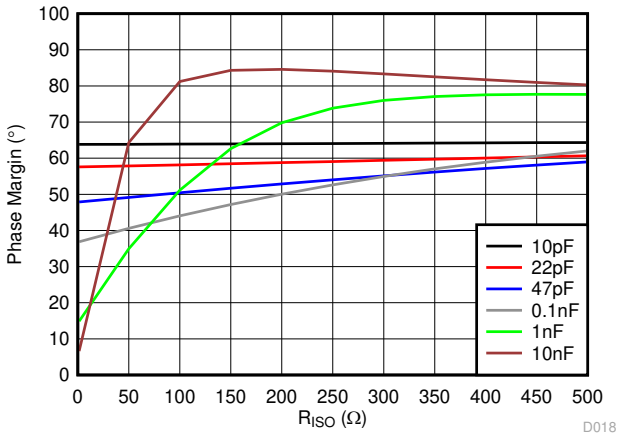


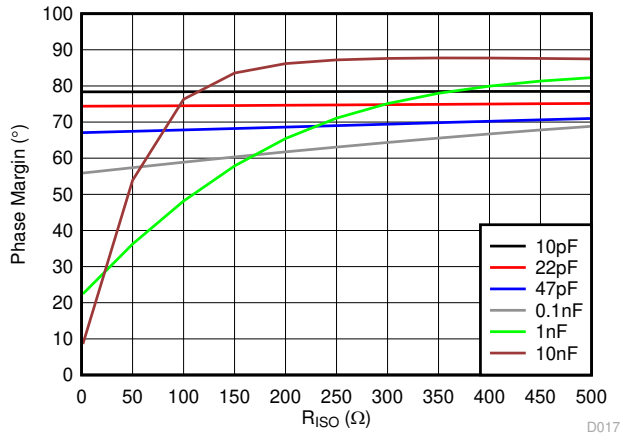
図 8-1. Input Current Protection and Driving Capacitive Loads

Phase Margin vs. Series Isolation Resistor and Phase Margin vs. Series Isolation Resistor show the phase margin achieved with varying R_{ISO} with different values of C_L.



Gain = 10 V/V, C_f = 2.5 pF, R_L = 10 kΩ

図 8-2. Phase Margin vs. Series Isolation Resistor



Gain = 20 V/V, C_f = 2.5 pF, R_L = 10 kΩ

図 8-3. Phase Margin vs. Series Isolation Resistor

8.3.3 Input and ESD Protection

When the primary design goal is a linear amplifier with high CMRR, do not exceed the op amp input common-mode voltage range (V_{CM}). This CMRR is used to set the common-mode input range specifications in セクション 7.5. The typical V_{CM} specifications for the OPAx607 devices are from the negative rail to 1.1 V below the positive rail. Assuming the op amp is in linear operation, the voltage difference between the input pins is small (ideally 0 V) and the input common-mode voltage can be analyzed at either input pin; the other input pin is assumed to be at the same potential. The voltage at V_{IN+} is easy to evaluate. In a noninverting configuration (図 8-1) the input signal, V_{IN+}, must not exceed the V_{CM} rating. However, in an inverting amplifier configuration, V_{IN+} must be connected to the voltage within V_{CM}. The input signal applied at V_{IN-} can be any voltage, such that the output voltage swings with a headroom of 10 mV from either of the supply rails.

The input voltage limits have fixed headroom to the power rails and track the power-supply voltages. For single 5-V supply, the linear input voltage range is 0 V to 3.9 V and with a 2.2-V supply this range is 0 V to 1.1 V. The headroom to each power-supply rail is the same in either case: 0 V and 1.1 V. A weak NMOS input pair from V_{IN+} to V_{IN+} – 1.1 V ensures that an output phase reversal issue does not occur when the V_{CM} is violated.

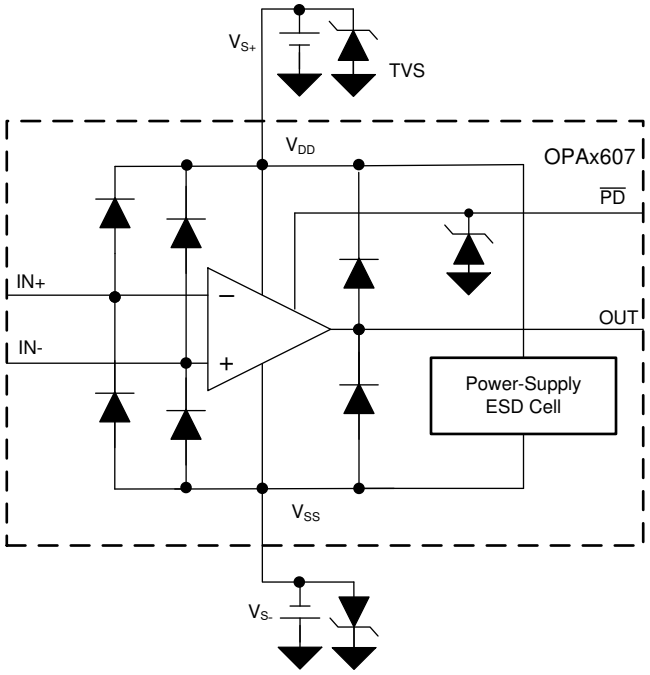


図 8-4. Internal ESD Structure

The OPAx607 devices also incorporate internal electrostatic discharge (ESD) protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provides input overdrive protection, as long as the current is limited with a series resistor to 10 mA, as stated in セクション 7.1. 図 8-1 shows a series input resistor can be added to the driven input to limit the input current.

8.3.4 Decompensated Architecture with Wide Gain-Bandwidth Product

Amplifiers such as the OPAx607 devices are not unity-gain stable are referred to as *decompensated amplifiers*. The decompensated architecture typically allows for higher GBW, higher slew rate, and lower noise compared to a unity-gain stable amplifier with similar quiescent currents. The increased available bandwidth reduces the rise time and the settling time of the op amp, allowing for sampling at faster rates in an ADC-based signal chain.

As shown in 図 8-5, the dominant pole f_d is moved to the frequency f_1 in the case of a decompensated op amp. The solid A_{OL} plot is the open-loop gain plot of a traditional unity-gain stable op amp. The change in internal compensation in a decompensated amp such as the OPAx607, increase the bandwidth for the same amount of power. That is, the decompensated op amp has an increased bandwidth to power ratio when compared to a unity-gain stable op amp of equivalent architecture. Besides the advantages in the above mentioned parameters, an increased slew rate and a better distortion (HD2 and HD3) value is achieved because of the higher available loop-gain, compared to its unity-gain counterpart. The most important factor to consider is ensuring that the op amp is in a noise gain (NG) greater than G_{min}. A value of NG lower than G_{min} results in instability, as shown in 図 8-5, because the 1/ß curve intersects the A_{OL} curve at 40 dB/decade. This method of analyzing stability is called the *rate of closure method*. See the precision lab training videos from TI for a better understanding on device stability and for different techniques of ensuring stability.

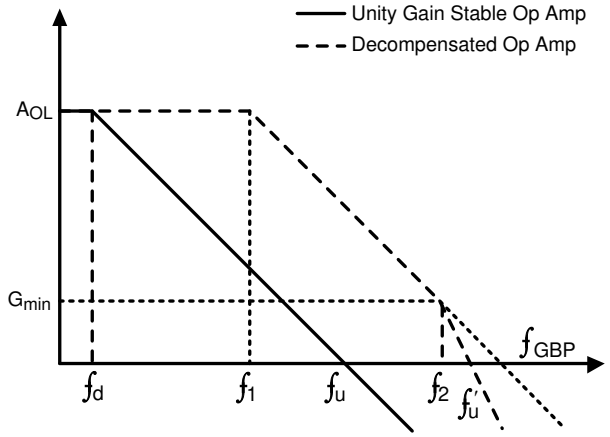


図 8-5. Gain vs Frequency Characteristics for a Unity-Gain Stable Op Amp and a Decompensated Op Amp

The OPAx607 devices are stable in a noise gain of 6 V/V (15.56 dB) or higher in conventional gain circuits; see 図 8-6. The device has 9 MHz of small-signal bandwidth (SSBW) in this gain configuration with approximately 65° of phase margin. The high GBW and low voltage noise of the OPAx607 devices make them suitable for general-purpose, high-gain applications.

8.4 Device Functional Modes

The OPAx607 devices have two functional modes: normal operating mode and Power Down ($\overline{PD}$) mode.

8.4.1 Normal Operating Mode

The OPAx607 devices are operational when the power-supply voltage is between 2.2 V (±1.1 V) and 5.5 V (±2.75 V). Most newer systems use a single power supply to improve efficiency and simplify the power tree design. The OPAx607 devices can be used with a single-supply power ($V_{S–}$ connected to GND) with no change in performance from split supply, as long as the input and output pins are biased within the linear operating region of the device. The valid input and output voltage ranges are given in セクション 7.5. The outputs nominally swing rail-to-rail with approximately 10-mV headroom required for linear operation. The inputs can typically swing up to the negative rail (typically ground) and to within 1.1 V from the positive supply. 図 8-6 shows changing from a ±2.5-V split supply to a 5-V single-supply.

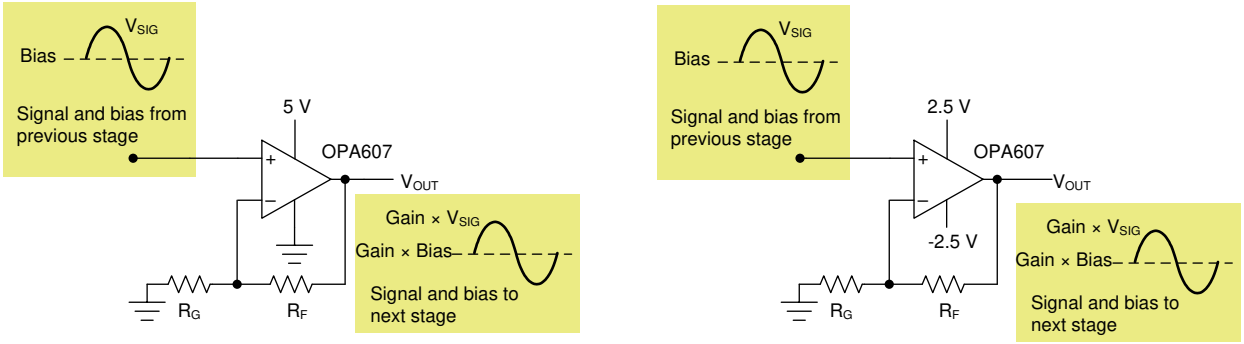


図 8-6. Single-Supply and Dual-Supply Operation

8.4.2 Power Down Mode

The OPAx607 devices feature a Power Down mode for power critical applications. Under logic control, the amplifier can be switched from normal operation (consuming ≤ 1 mA) to a Power Down current of less than 1 µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting the $\overline{PD}$ pin to logic low disables the amplifier and places the output in a high-impedance state. The output of an op amp is high impedance similar to a tri-state high-impedance gate under a Power Down condition; however, the feedback network behaves as a parallel load.

If the Power Down mode is not used, connect $\overline{PD}$ to the positive supply pin or leave floating. See the *Power Down (Device Enabled When Floating)* section in セクション 7.5 table for the enable and disable threshold voltages. The $\overline{PD}$ pin can be left floating to keep the op amp always enabled, which is primarily possible because of the presence of an internal pullup resistor within the op amp that, by default, always keeps the $\overline{PD}$ pin weakly tied to V_{S+}. However it is also acceptable to strengthen the pull up from the $\overline{PD}$ pin by connecting a low value resistance from the $\overline{PD}$ pin to V_{S+}. This helps make the part less susceptible to noise and transient pick up on the $\overline{PD}$ pin. Looking at the $\overline{PD}$ pin bias current in Power Down Pin Bias Current vs Power Down Pin Voltage can help us get an accurate understanding of the voltage required to be applied on the $\overline{PD}$ pin for enabling and powering down. Note: the hysteresis present in Power Down Pin Bias Current vs Power Down Pin Voltage help with single shot power up and power down of OPAx607 devices.

The $\overline{PD}$ pin exhibits a special type of ESD protection which allows users to apply any voltage between $V_{S–}$ to 6 V irrespective of the voltage at the V_{S+}. Special ESD structure at the $\overline{PD}$ pin helps in relaxing the requirements on power sequencing during power up and power down condition. Refer to 図 8-4 for details of the internal ESD structure. The absolute voltage limits applicable on $\overline{PD}$ pin can be found in セクション 7.1 table. Another key care about in PD condition is to ensure the IN+ and IN– are not exposed to a high differential voltage continuously. In a power up condition the op-amp's loop gain ensure the IN+ pin and the IN– track each other closely. However in PD condition the op-amp is inactive and IN– will be usually weakly tied to GND through the R_G resistor. Exposing the IN+ pin continuously to a high voltage in such a condition will result in irreversible offset voltage (V_{OS}) shift.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPAx607 devices feature a 50-MHz GBW with 900 µA of supply current, providing good AC performance at low-power consumption. The low input noise voltage of 3.8 nV/√ Hz, the approximate pA of bias current, and a typical input offset voltage of 0.1 mV make the device very suitable for both AC and DC applications.

9.2 Typical Applications

9.2.1 100-kΩ Gain Transimpedance Design

The high GBW and low input voltage and current noise for the OPAx607 devices make it an excellent wideband transimpedance amplifier for moderate to high transimpedance gains.

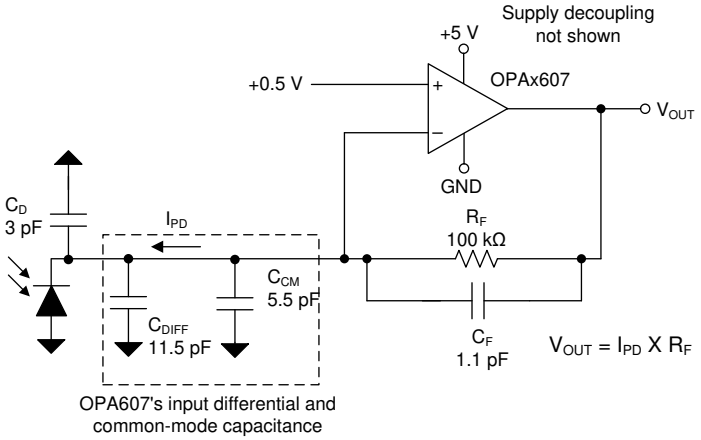


図 9-1. Wideband, High-Sensitivity, Transimpedance Amplifier

9.2.1.1 Design Requirements

Design a high-bandwidth, high-transimpedance-gain amplifier with the design requirements shown in 表 9-1.

表 9-1. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE-GAIN (kΩ)	PHOTODIODE CAPACITANCE (pF)
2	100	3

9.2.1.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance-gain benefit from the low input voltage noise of the OPAx607 devices. Use the Excel™ calculator available at *What You Need To Know About Transimpedance Amplifiers – Part 1* to help with the component selection based on total input capacitance and C_{TOT}. C_{TOT} is referred as C_{IN} in the calculator. C_{TOT} is the sum of C_D, C_{DIFF}, and C_{CM} which is 20 pF. Using this value of C_{TOT}, and the targeted closed-loop bandwidth (f_{-3dB}) of 2 MHz and transimpedance gain of 100 kΩ results in amplifier GBW of approximately 50 MHz and a feedback capacitance (C_F) of 1.1 pF as shown in 図 9-2. These results are for a Butterworth response with a Q = 0.707 and a phase margin of approximately 65° which corresponds to 4.3% overshoot.

Calculator II		
Closed-loop TIA Bandwidth (f_{-3dB})	2.00	***MHz***
Feedback Resistance (R_F)	100.00	***kOhm***
Input Capacitance (C_{IN})	20.00	***pF***
Opamp Gain Bandwidth Product (GBP)	50.27	***MHz***
Feedback Capacitance (C_F)	1.110	***pF***

図 9-2. Results of Inputting Design Parameters in the TIA Calculator

The OPA607's 50 MHz GBW, is suitable for the above design requirements. If the required feedback capacitance C_F comes out to be a very low value capacitor to be practically achievable, a T-Network capacitor circuit as shown below can be used. A very low capacitor value (C_{EQ}) can be achieved between $Port_1$ and $Port_2$ using standard value capacitors in a T-Network circuit as shown in 図 9-3.

$$C_{EQ} = \frac{C_1 \times C_2}{C_1 + C_2 + C_T} \quad (1)$$

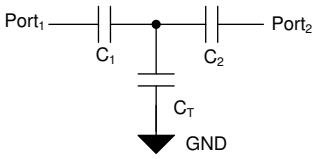


図 9-3. T-Network

9.2.1.3 Application Curves

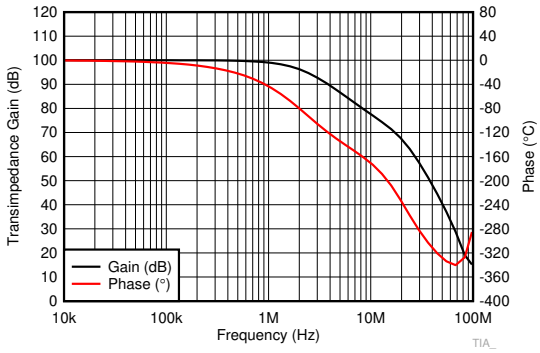


図 9-4. Simulated Closed-Loop Bandwidth of TIA

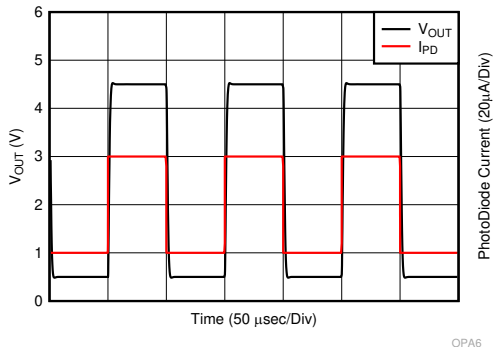


図 9-5. Simulated Time Domain Response

9.2.2 Noninverting Gain of 3 V/V

The OPAx607 devices are normally stable in noise gain configurations (see SBOA066) of greater than 6 V/V when conventional feedback networks are used, which is discussed in セクション 8.3.4. The OPAx607 devices can be configured in noise gains of less than 6 V/V by using capacitors in the feedback path and between the inputs to maintain the desired gain at lower frequencies and increase the gain greater that 6 V/V at higher frequencies such that the amplifier is stable. Configuration (a) in 図 9-6 shows OPAx607 devices configured in a gain of 3 V/V by using capacitors and resistors to shape the noise gain and achieve a phase margin of approximately 56° that is very close to the phase margin achieved for the conventional 6 V/V configuration (b) in 図 9-6.

The key benefit of using a decompensated amplifier (such as the OPAx607) below the minimum stable gain, is that it takes advantage of the low noise and low distortion performance at quiescent powers smaller than comparable unity-gain stable architectures. By reducing the 100-pF input capacitor, higher closed-loop bandwidth can be achieved at the expense of increased peaking and reduced phase margin. Ensure that low parasitic capacitance layout techniques on the IN– pin are as small as 1 pF to 2 pF of parasitic capacitance on the inverting input, which will require tweaking the noise-shaping component values to get a flat frequency response and the desired phase margin. Configurations in 図 9-6 does not take into account this parasitic capacitance but it must be considered for practical purposes. Details on the benefits of decompensated architectures are discussed in *Using a decompensated op amp for improved performance*. The *one-capacitor, externally compensated type* method is used for noise gain shaping in the below circuit.

In a difference amplifier circuit, typically used for low side current sensing applications, the (noise gain) = (signal gain + 1).

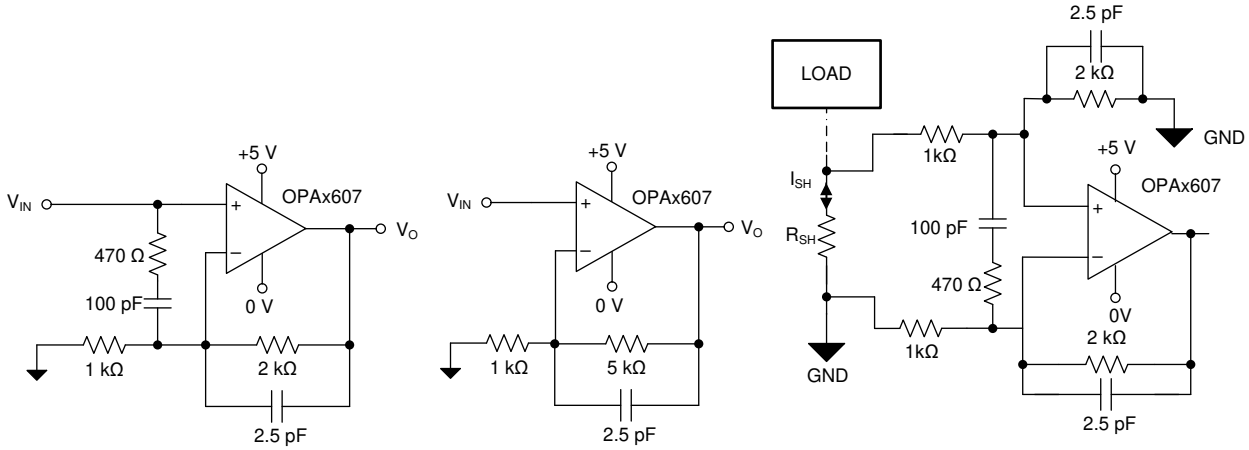


図 9-6. Noninverting Gain of 3 V/V, 6 V/V Configurations and Difference Amplifier in Signal Gain of 2 V/V

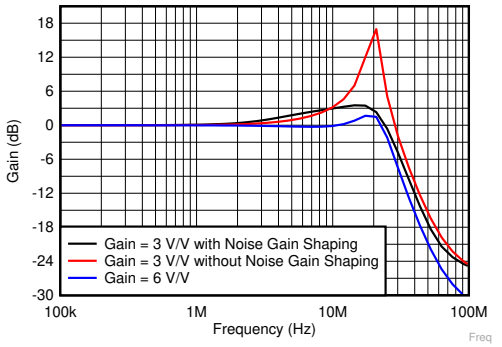


図 9-7. Small-Signal Frequency Response in Gains of 3V/V (a) and 6V/V (b)

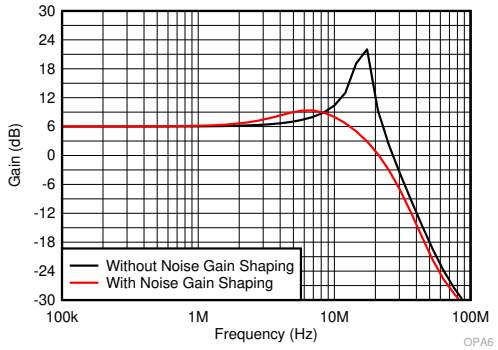


図 9-8. Small-Signal Frequency Response of Difference Amplifier (c) With and Without Noise Gain Shaping

9.2.3 High-Input Impedance (Hi-Z), High-Gain Signal Front-End

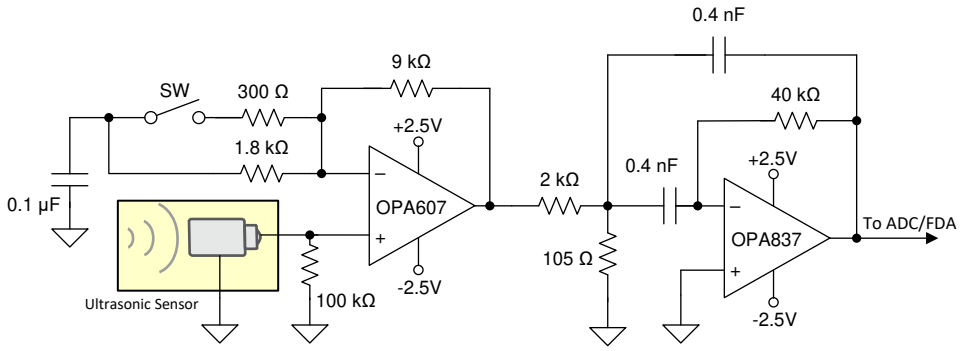


図 9-9. Hi-Z, High-Gain Front-End Circuit

9.2.3.1 Design Requirements

The objective is to design a high-input impedance, high-dynamic range, signal-conditioning front-end. An example application for such a front-end circuit is the receive signal chain in an ultrasonic-based end equipment (EE) such as fish finders, printers and flow meters. 表 9-2 lists the design requirements for this application.

表 9-2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Amplifier supply	±2.5 V
Input signal frequency	200 kHz
Minimum voltage	300 µVrms
Minimum SNR at 300 µVrms	40 dB

9.2.3.2 Detailed Design Procedure

To achieve a SNR of greater than 40 dB for signals from 300 uVrms to 30 mV the front-end stage has two gain settings: 6 V/V and 31 V/V. The SW (switch, relay, or analog mux) can be dynamically toggled to ensure maximum sensitively to the receiving signal. The OPAx607 devices prove to be an attractive solution for this front-end signal chain because of the right balance of low noise and high input impedance. The ultrasonic sensors (Ex. piezo crystal) have high output impedance. The OPAx607 devices have an input bias current of 20 pA (maximum). This small bias current results in reduced distortion and signal loss across the source impedance when compared with a bipolar amplifier with input bias currents in the range of a few hundreds of nano-amperes. The OPAx607's high-gain front-end is followed by a narrowband band-pass filter that is tuned to a 200-kHz center frequency. The narrowband filter is designed using the OPA837. OPA837 can be used as a variable gain mux / PGA as shown in TIDA-01565. In this application section the OPA837-based band-pass filter was designed using the techniques mentioned in the *Filter Design in Thirty Seconds* application report.

図 9-11 shows the frequency response of circuit in 図 9-9. As shown in 図 9-11, the frequency response is a high-Q factor band-pass filter centered around 200 kHz. Designing such a high-Q band-pass filter helps eliminate white band noise along with other interferences present in the circuitry, resulting in a high SNR signal chain. The OPAx607's front-end combined with the OPA837-based band-pass filter help to achieve a total gain of 33 dB (44 V/V) or 50 dB (316 V/V) based on the SW (switch) position.

9.2.3.3 Application Curves

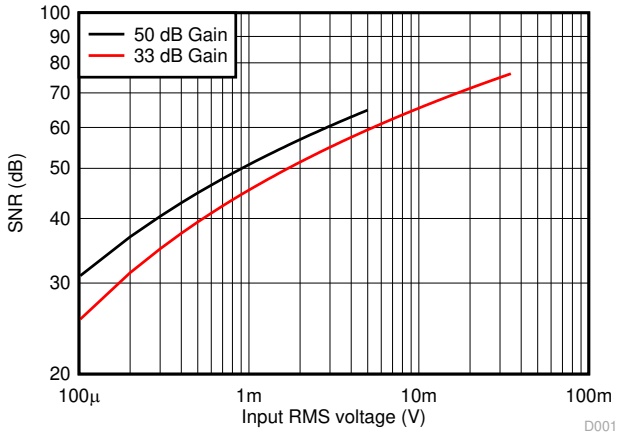


図 9-10. Hi-Z, High-Gain Front-End Circuit SNR vs Input

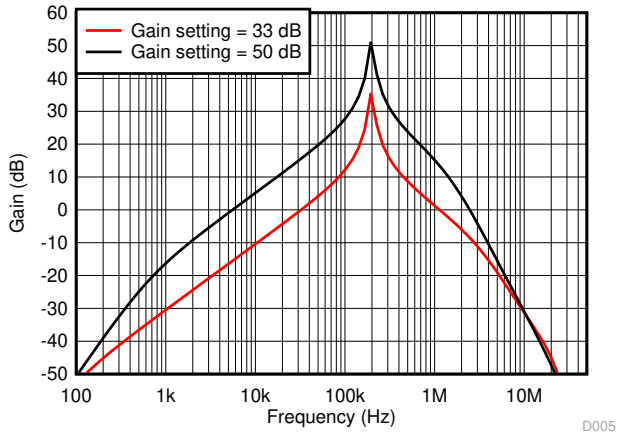


図 9-11. Hi-Z, High-Gain Front-End Circuit Gain vs Frequency

9.2.4 Low-Cost, Low Side, High-Speed Current Sensing

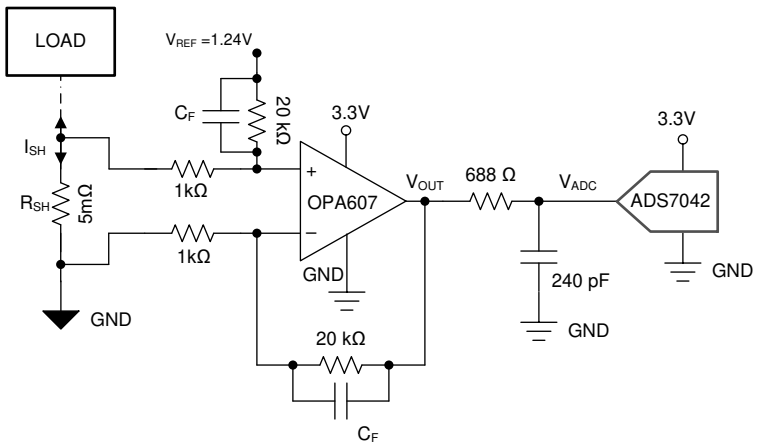


図 9-12. Low Side Current Sensing

9.2.4.1 Design Requirements

The objective is to design a high-speed, high-gain bidirectional current-sensing circuit for power systems and motor drive systems. セクション 9.2.4.2 lists the design requirements of this application.

表 9-3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Amplifier and ADC supply	3.3 V
Peak current to be measured from load to ground	20 A
Peak current to be measured from ground to load	12 A
Required Accuracy of current measurement	0.1%
Signal-Setting time at ADC input	< 1 µs
Current sensing direction	Bidirectional

9.2.4.2 Detailed Design Procedure

The aim of this application section is to measure bidirectional current with relatively high accuracy in a low-side-sensing-based, high-frequency switching system.

As shown in 図 9-12, a single op amp of high bandwidth is capable of sensing current in a high gain configuration as well as have the required effective bandwidth to drive the consecutive SAR ADC input. The SAR ADC can be a standalone ADC or integrated inside a Micro-controller.

$$V_{OUT} = (20\ k\Omega / 1\ k\Omega \times V_{DIFF}) + V_{REF}, \text{ where } V_{DIFF} = I_{SH} \text{ X } R_{SH} \quad (2)$$

The reference voltage is 1.24 V. When the I_{SH} flowing across R_{SH} equals zero, the V_{OUT} of the difference amplifier sits ideal at 1.24 V.

When the current (I_{SH}) flows from LOAD to GND, the output of the OPAx607 increase above 1.24 V with a value equal to 20 × V_{SH} and when the current flows from GND to LOAD (in the opposite direction) the output of the OPAx607 decrease below 1.24 V with a value proportional to 20 × V_{SH}.

One of the main challenges in a high speed current sensing design is to choose an op amp of with sufficient GBW that can drive a SAR ADC, while still being able to gain the signal by the required amount. The 0.1% and 0.01% settling of OPAx607 can found in セクション 7.5. Another key care about is to ensure the op amp output rises in less than 1 µs so as to feed the output to a comparator for short-circuit protection. This comparator based short circuit protection loop is extremely fast and enables to turn off the switching devices very quickly. This requirement makes a low cost high speed part like the OPAx607 very desirable in a current-sensing circuit. Equation of the rise time as a function of bandwidth is shown below.

t_R (10% to 90%) = 0.35 Hz / BW (3)

For an ADC like ADS7042 running at a sampling rate of 500 kSPS of a clock of 12.5 MHz, the effective bandwidth of the op amp required to drive such an ADC is approximately 2.7 MHz. See the TI precision lab videos on driving SAR ADCs to understand the underlying calculation. The OPAx607 has a GBW of 50 MHz. With a gain of 20 V/V, the closed loop bandwidth turns out to approximately 2.5 MHz, making this device the most suitable, cost-optimized amplifier for this application. The RC charge bucket (240 Ω and 688 pF in 図 9-12) designed at the input of the SAR ADC is derived from the calculations provided in the SAR ADC precision lab videos. The fundamental concept behind the design of this charge bucket filter is to ensure that the sample and hold capacitor is charged to the required final voltage within the acquisition window of the ADC.

As shown in 図 9-14, a DC accuracy of higher than 0.05% is achieved with the OPAx607. The simulations are captured with and without voltage offset calibration. Frequency response shown in 図 9-13 indicate different signal bandwidth at V_{OUT}, V_{ADC} and with and without C_F of 220 pF.

9.2.4.3 Application Curves

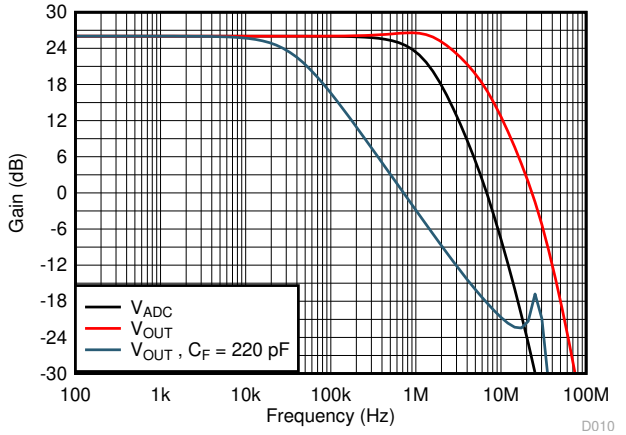


図 9-13. Frequency Response of Low Side Current Sensing

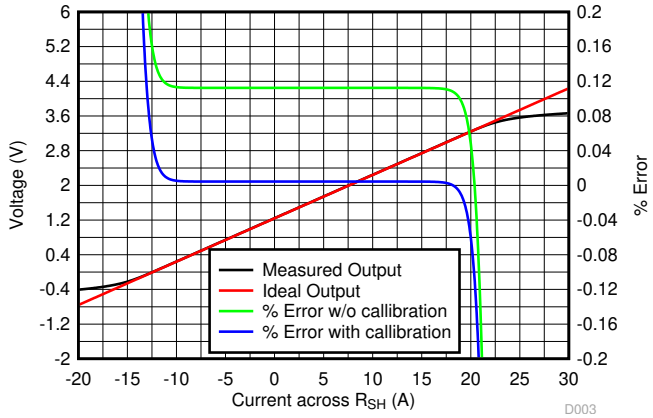


図 9-14. DC Current-Sense Transfer Function

9.2.5 Ultrasonic Flow Meters

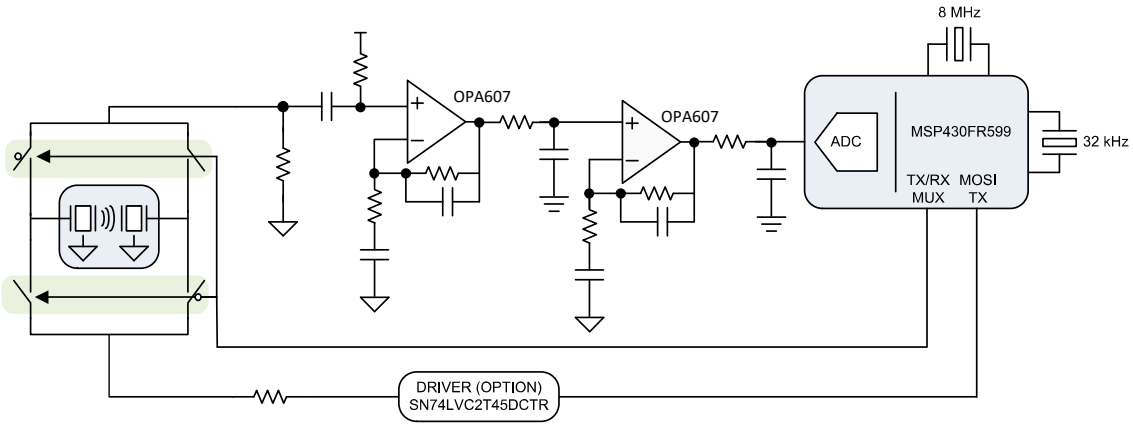


図 9-15. High-Gain Ultrasonic Front-End

9.2.5.1 Design Requirements

The OPAx607 devices have a wide operating voltage range of 2.2 V to 5.5 V with a maximum quiescent current of 1 mA. The availability of the inbuilt shutdown function enables designers to power cycle the front-end signal chain, reducing the net quiescent current even further. The minimum operating voltage range of 2.2 V proves to be very suitable for battery-powered and power sensitive applications such as the ultrasonic-based flow meters. The high GBW of the OPAx607 devices enable the gain stages and the ADC drive stages to be designed and combined, thereby reducing component count. A schematic similar to that of 図 9-12 can be used in ultrasonic flow meters for the front-end signal chain.

The *Ultrasonic sensing subsystem reference design for gas flow measurement* design guide has a detailed design procedure for ultrasonic-based sensing for gas flow measurement. The OPAx607 devices are very suitable op amps for the discrete front-end design described in this design guide.

10 Power Supply Recommendations

The OPAx607 devices are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V), applicable from –40°C to +125°C. Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

CAUTION

Supply voltages larger than 6 V can permanently damage the device (see セクション 7.1).

For more detailed information on bypass capacitor placement, see *セクション 11.1*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power-supply pins of the circuit as a whole and of the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-equivalent series resistance (ESR), 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance; see 図 11-1 and 図 11-2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

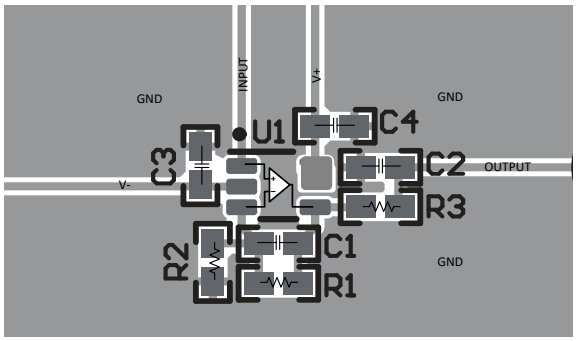


図 11-1. Operational Amplifier Board Layout for a Noninverting Configuration

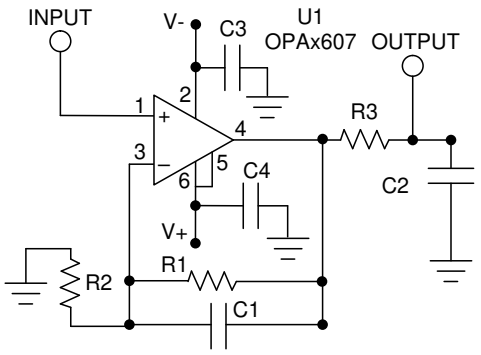


図 11-2. Layout Example Schematic

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Texas Instruments, precision lab videos

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA2834 50-MHz, 170-µA, Negative-Rail In, Rail-to-Rail Out, Voltage-Feedback Amplifier* data sheet
- Texas Instruments, *ADS7042 Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC* data sheet
- Texas Instruments, *Ultrasonic Sensing Subsystem Reference Design For Gas Flow Measurement* design guide
- Texas Instruments, *OPAx836 Very-Low-Power, Rail-to-Rail Out, Negative Rail In, Voltage-Feedback Operational Amplifiers* data sheet
- Texas Instruments, *Filter Design in Thirty Seconds* application report

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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TI E2E™ is a trademark of Texas Instruments.
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12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2607IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2FRT
OPA2607IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2FRT
OPA2607IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2FRT
OPA2607IDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2FRT
OPA2607IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2607
OPA2607IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2607
OPA2607SIRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	KJF
OPA2607SIRUGR.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	KJF
OPA607IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	O6BV
OPA607IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O6BV
OPA607IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	O6BV
OPA607IDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O6BV
OPA607IDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1G4
OPA607IDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1G4
OPA607IDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1G4
OPA607IDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1G4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA2607, OPA607 :

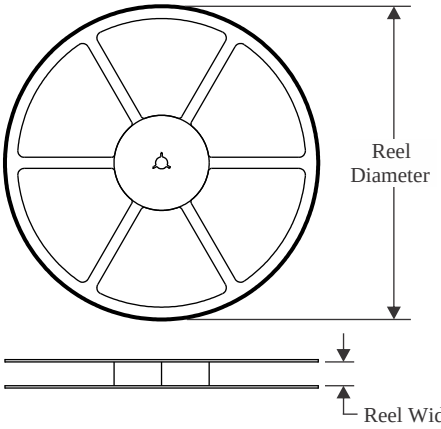
- Automotive : OPA2607-Q1, OPA607-Q1

NOTE: Qualified Version Definitions:

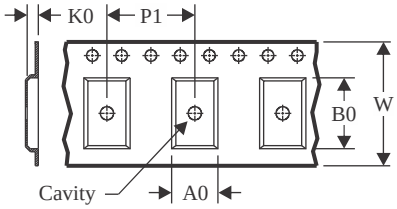
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

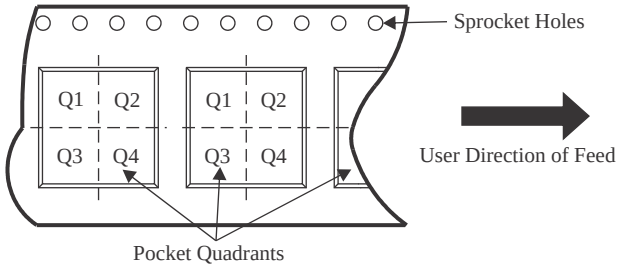


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

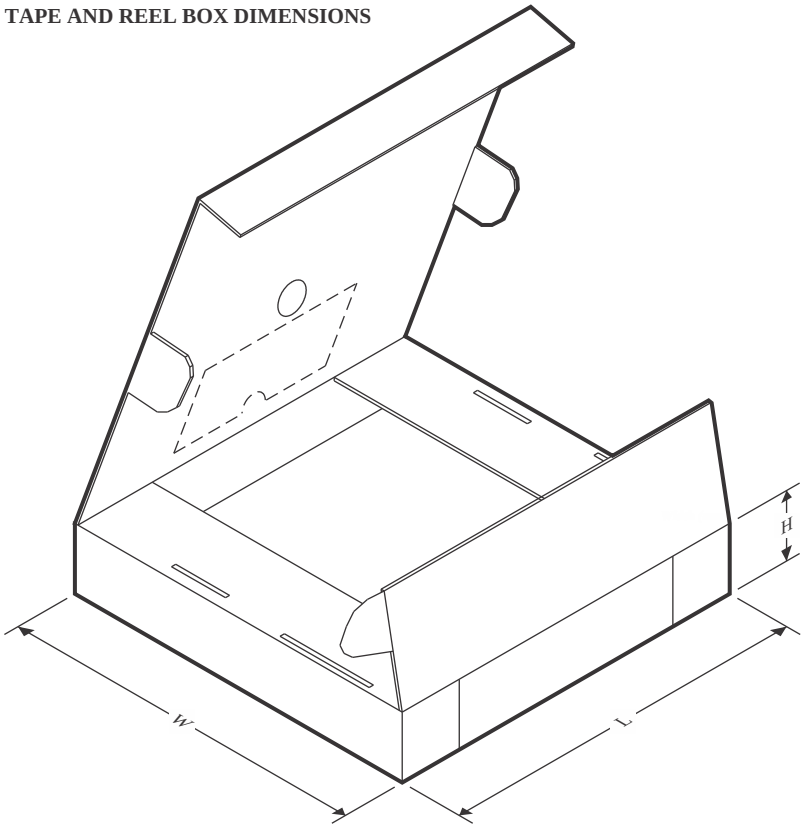
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2607IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2607IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2607IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2607SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
OPA607IDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA607IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA607IDCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
OPA607IDCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
OPA607IDCKT	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

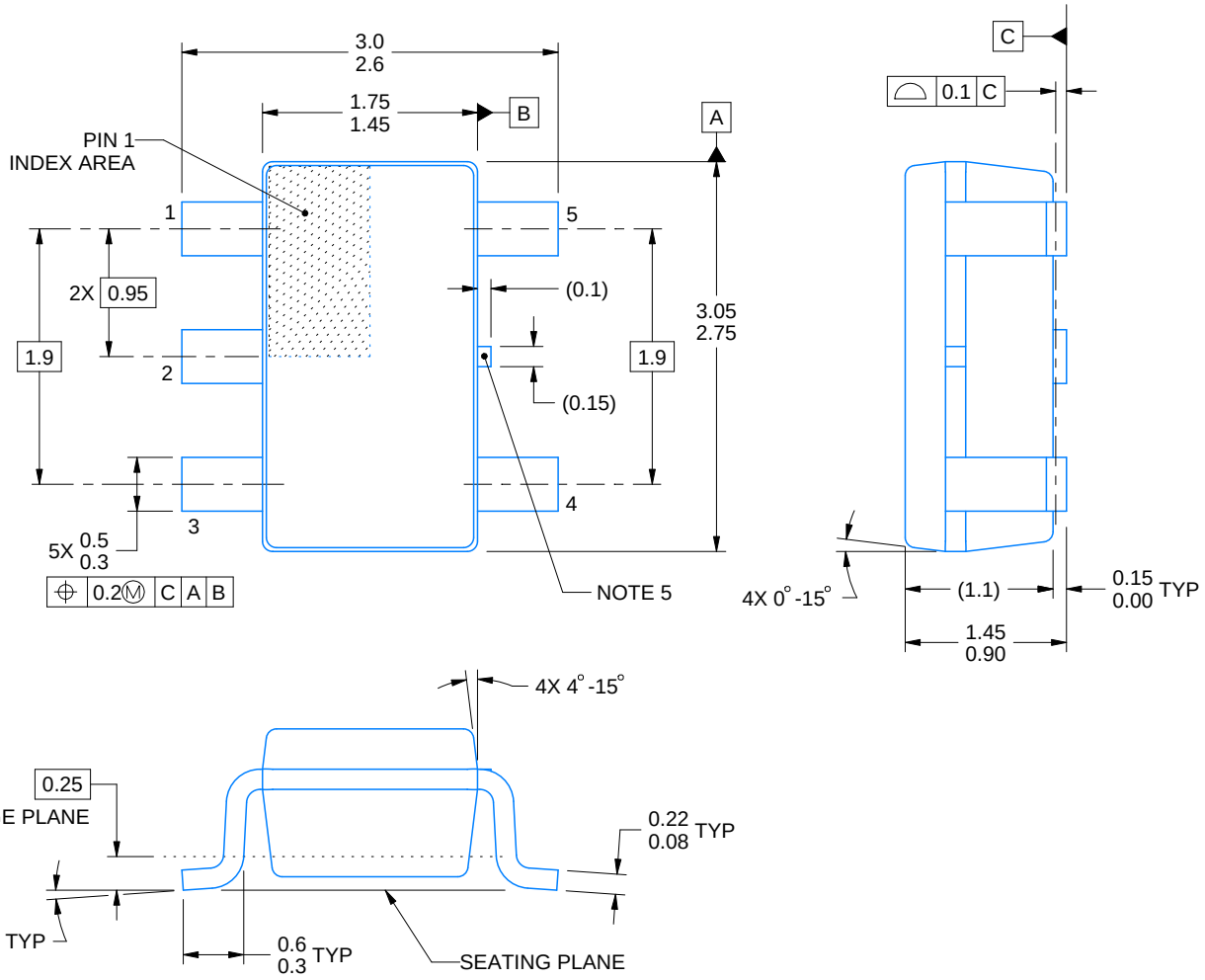
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2607IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2607IDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2607IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2607SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
OPA607IDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
OPA607IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA607IDCKR	SC70	DCK	6	3000	210.0	185.0	35.0
OPA607IDCKT	SC70	DCK	6	250	210.0	185.0	35.0
OPA607IDCKT	SC70	DCK	6	250	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

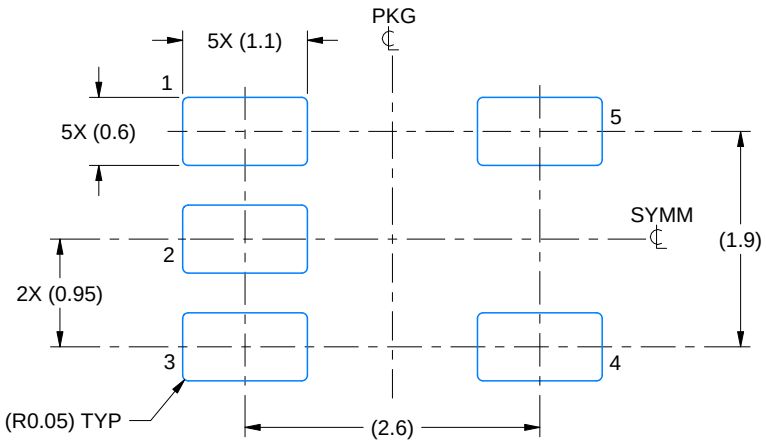
SMALL OUTLINE TRANSISTOR



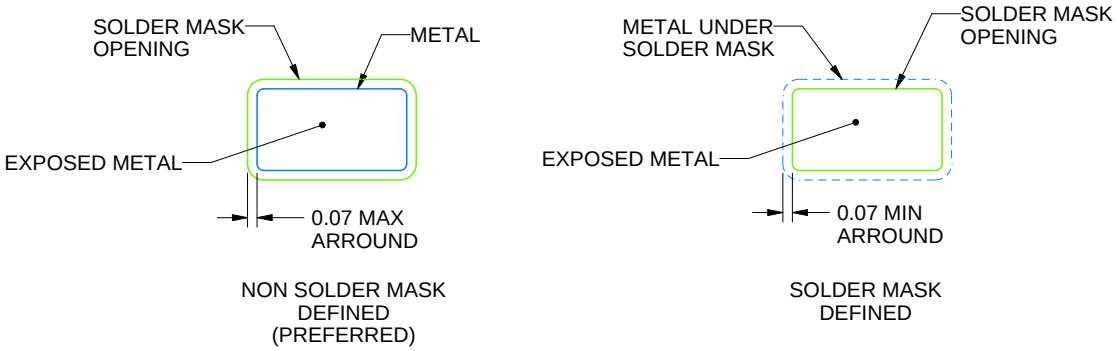
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

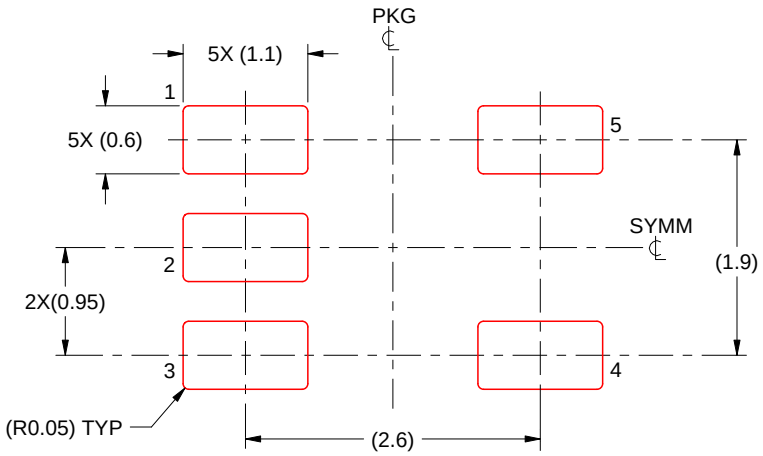


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

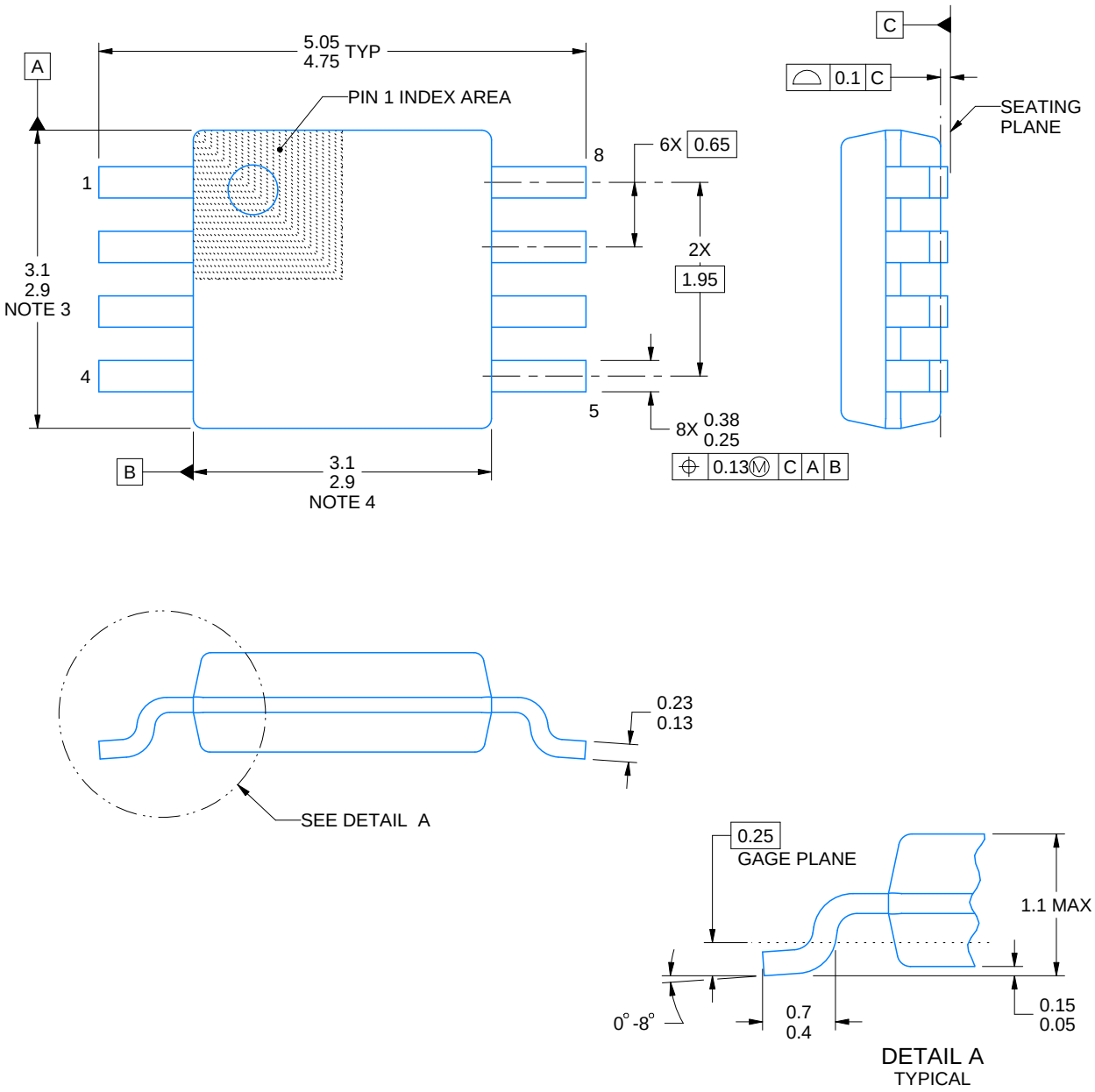
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

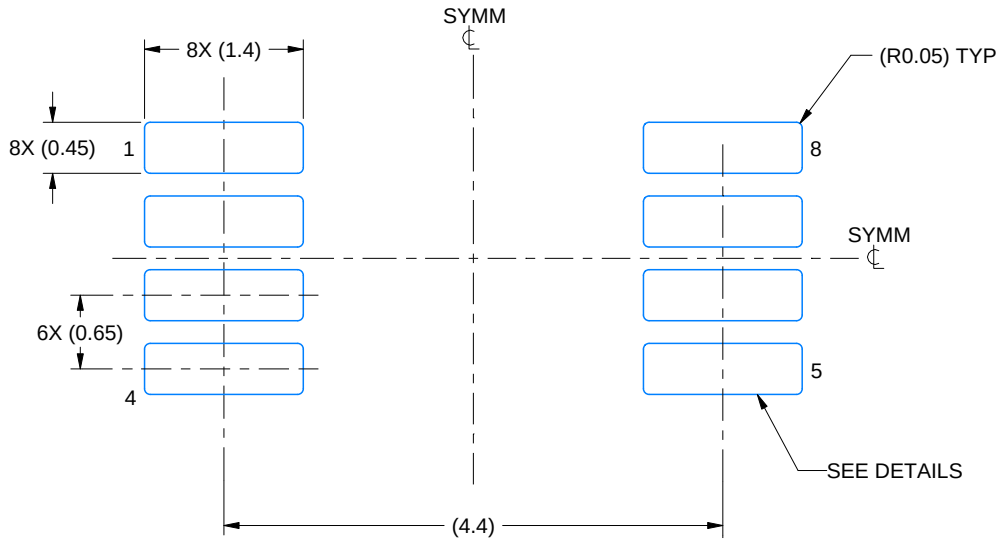
SMALL OUTLINE PACKAGE



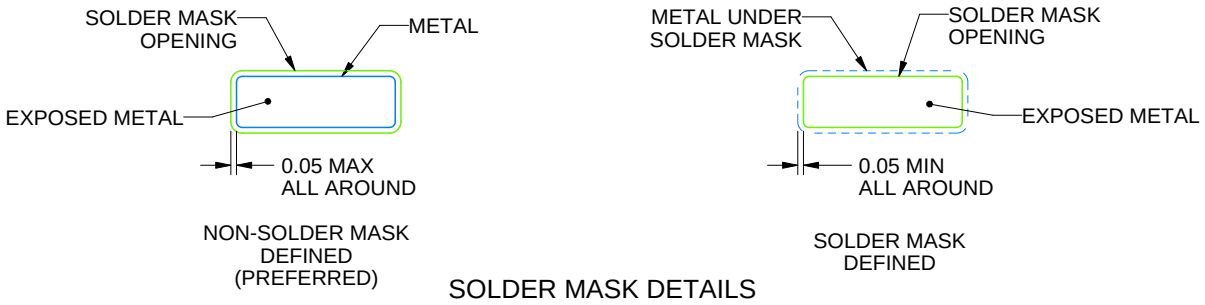
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

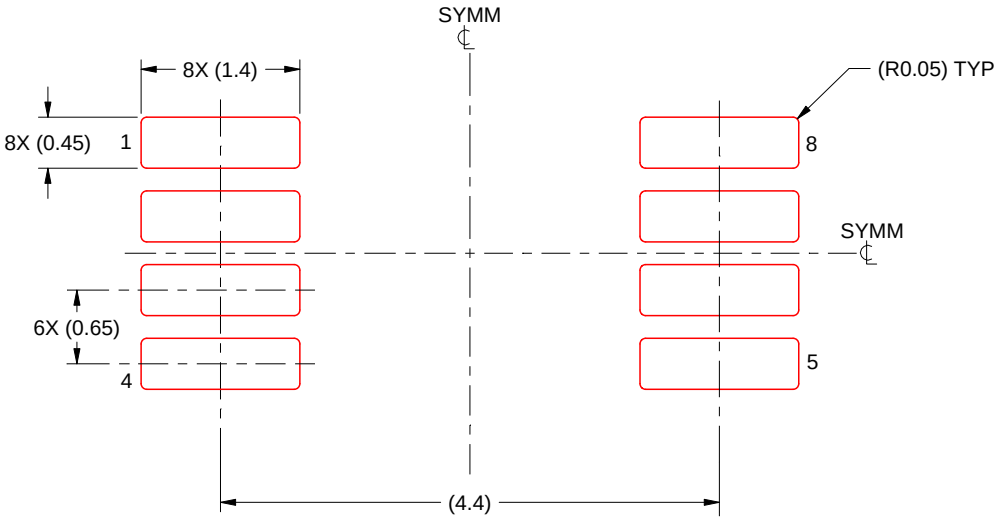


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

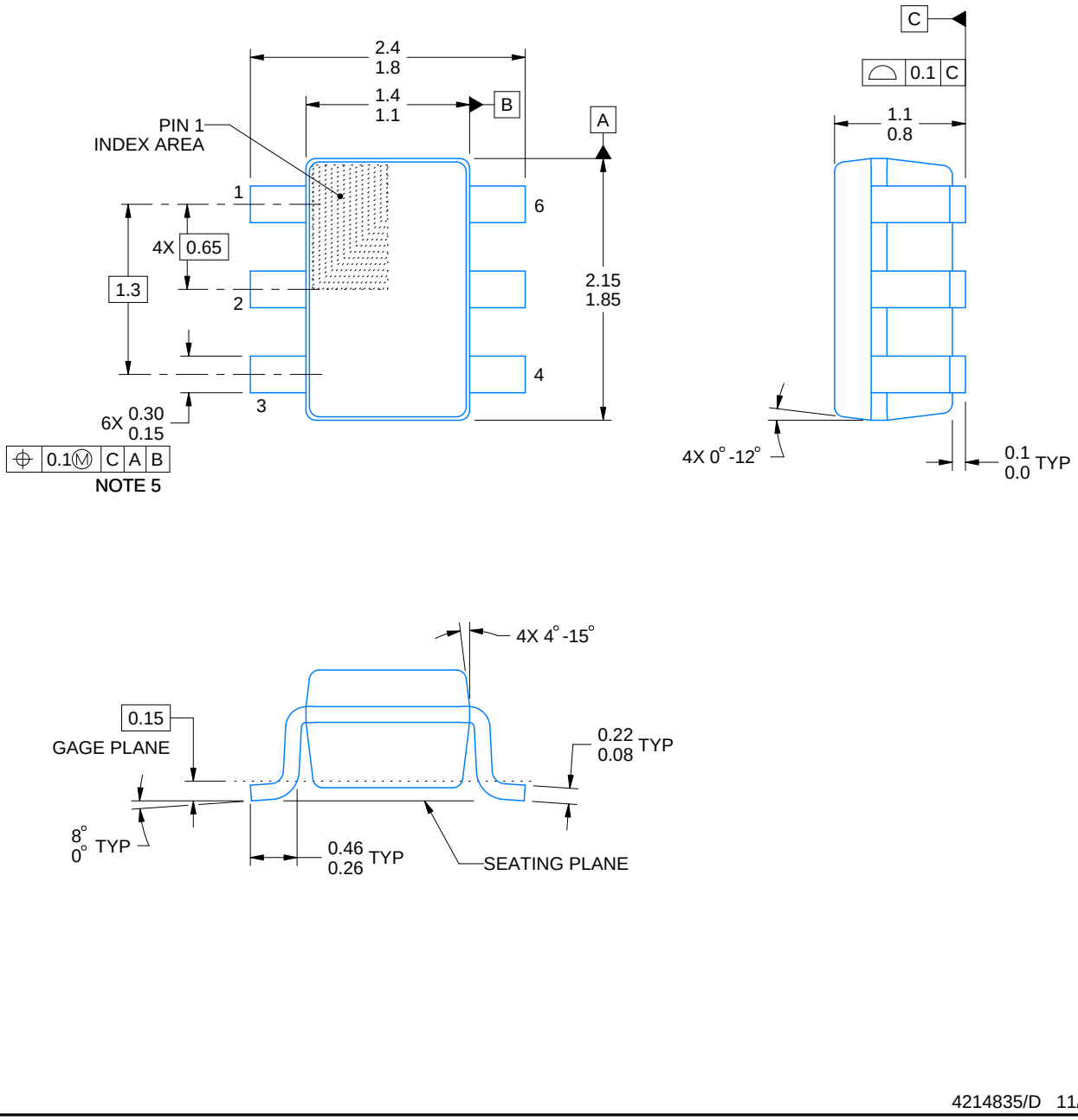
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

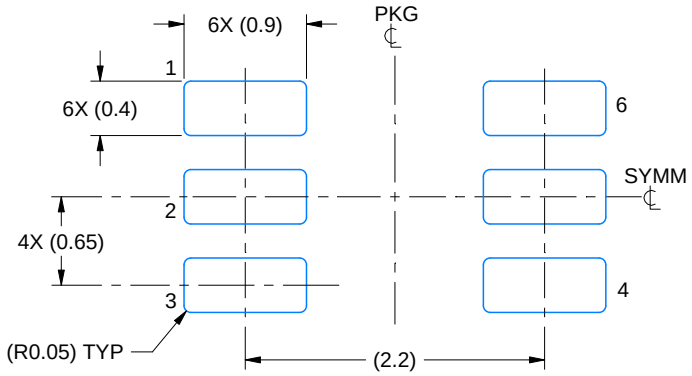
SMALL OUTLINE TRANSISTOR



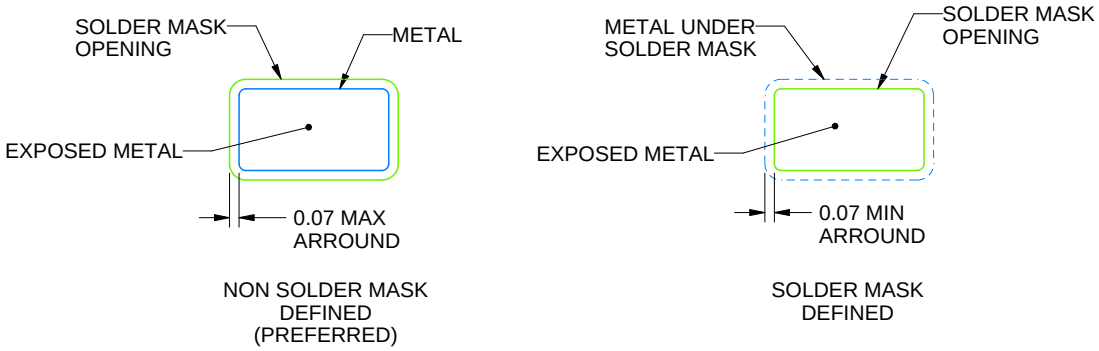
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

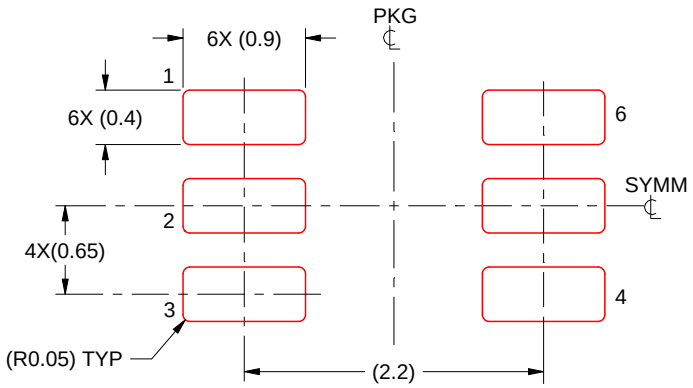


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

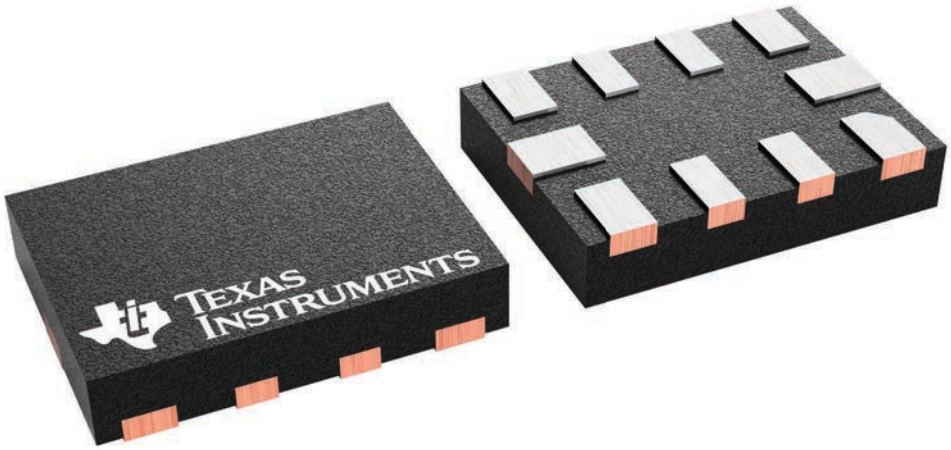
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

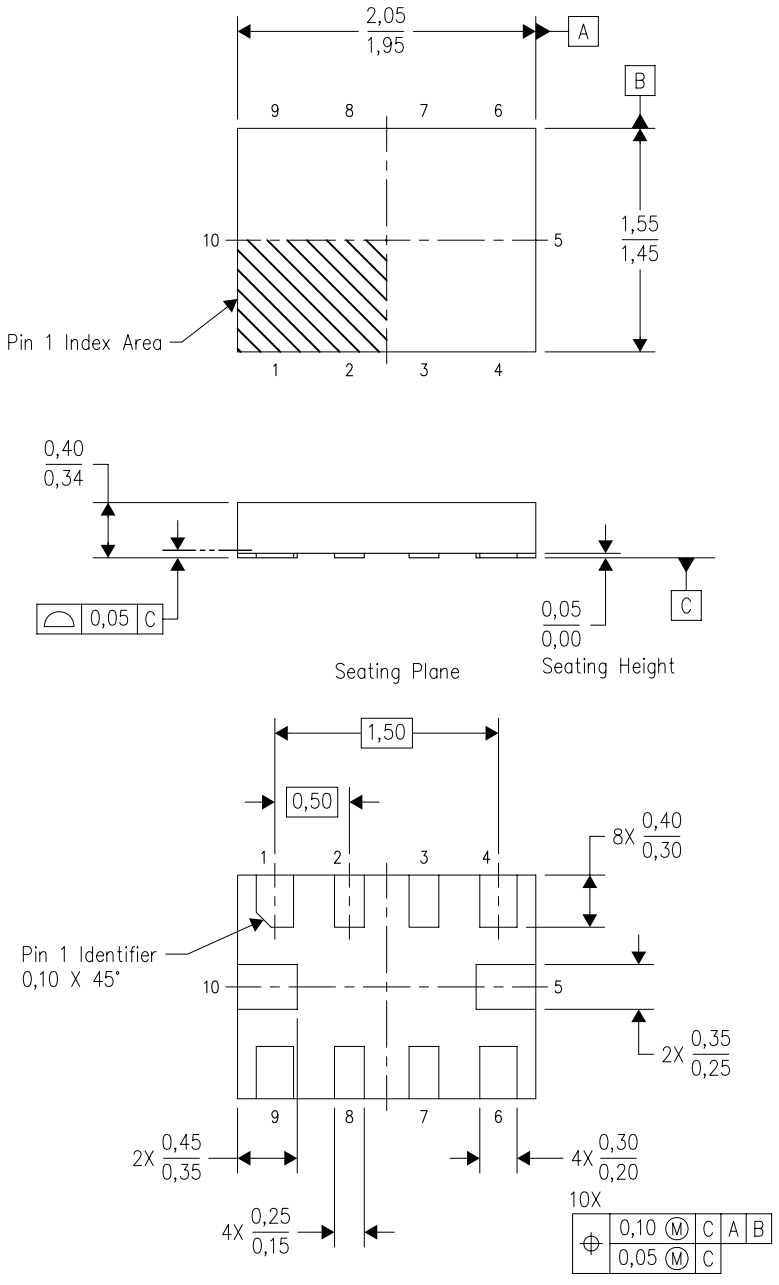
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231768/A

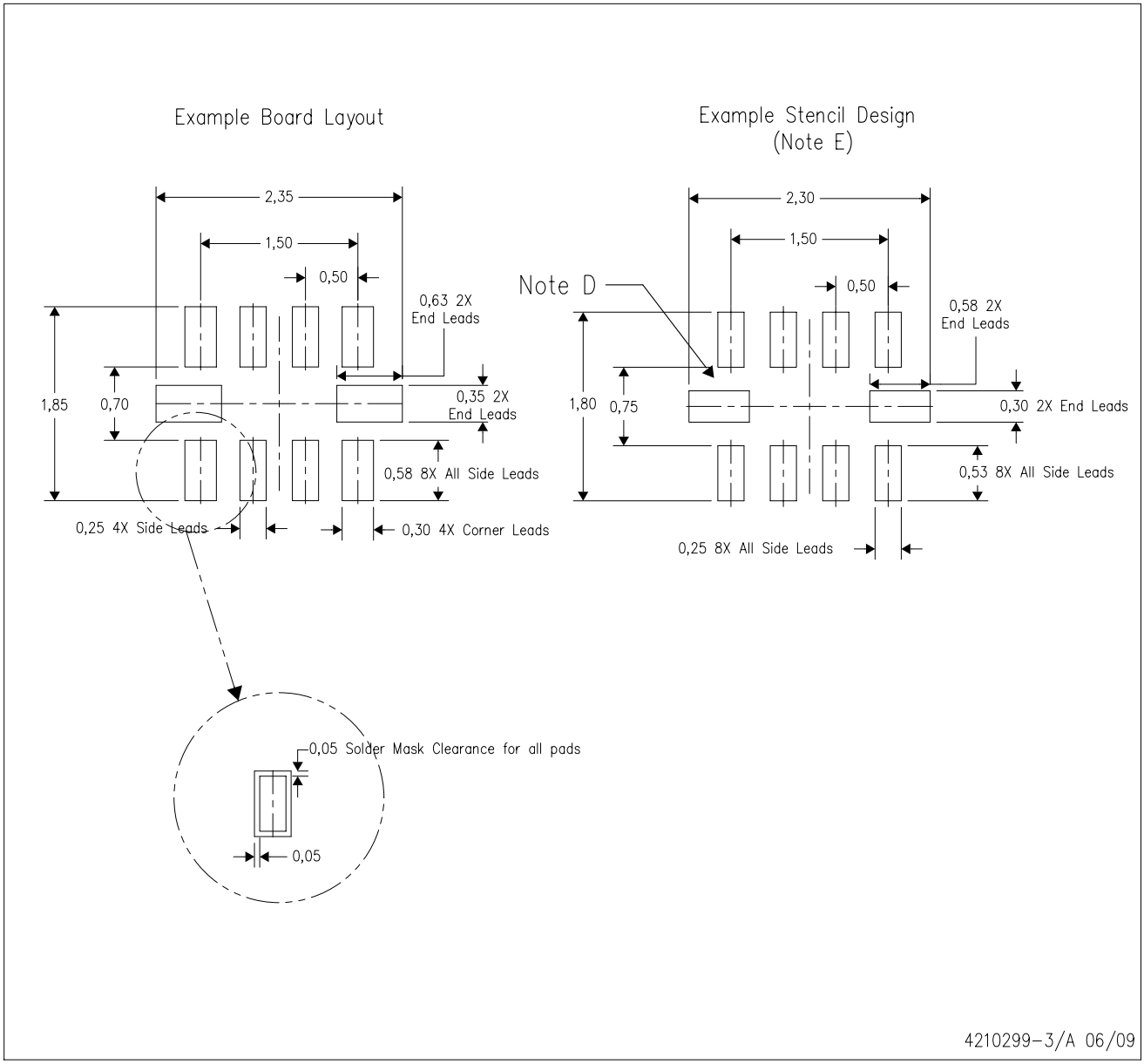
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



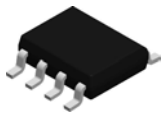
4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

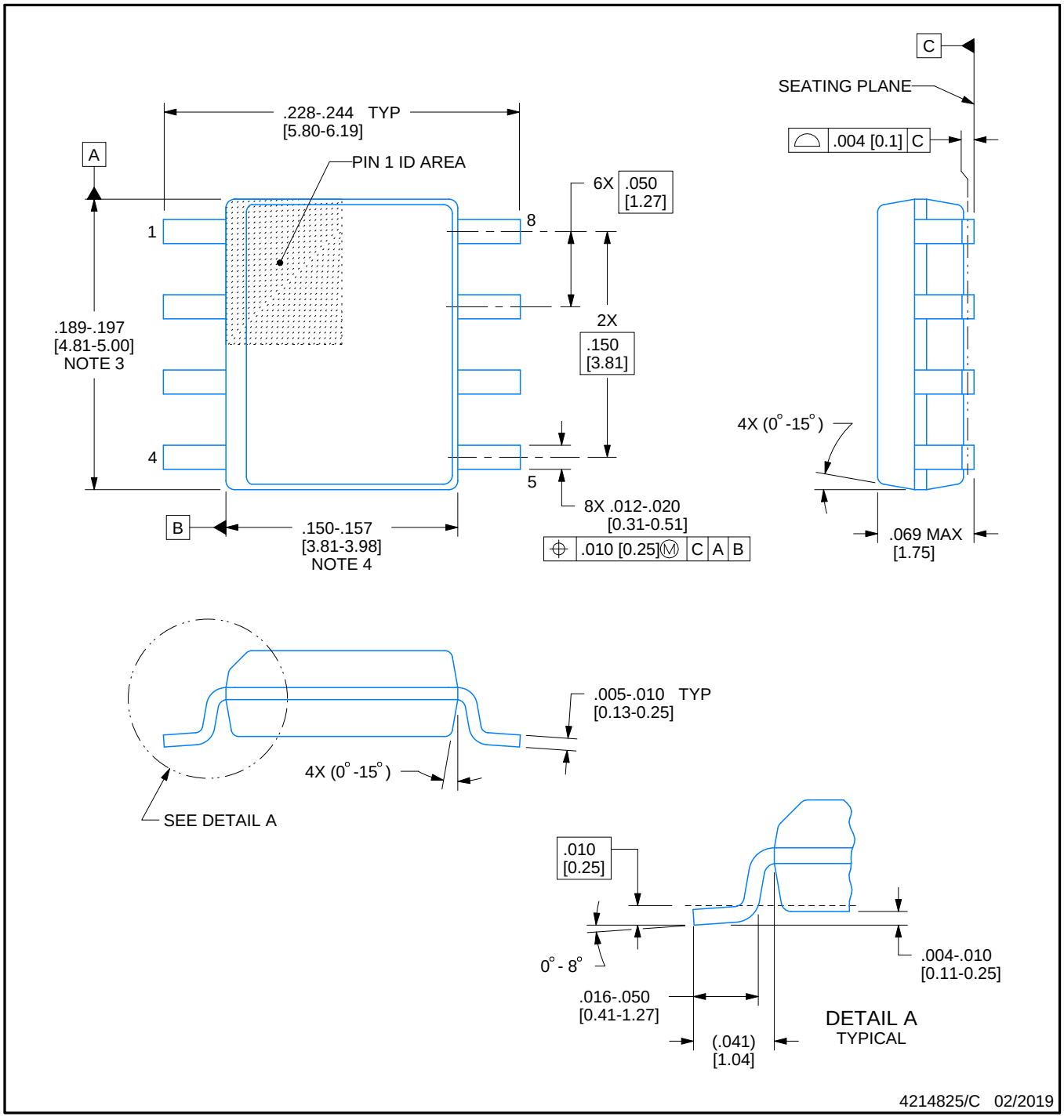


PACKAGE OUTLINE

D0008A

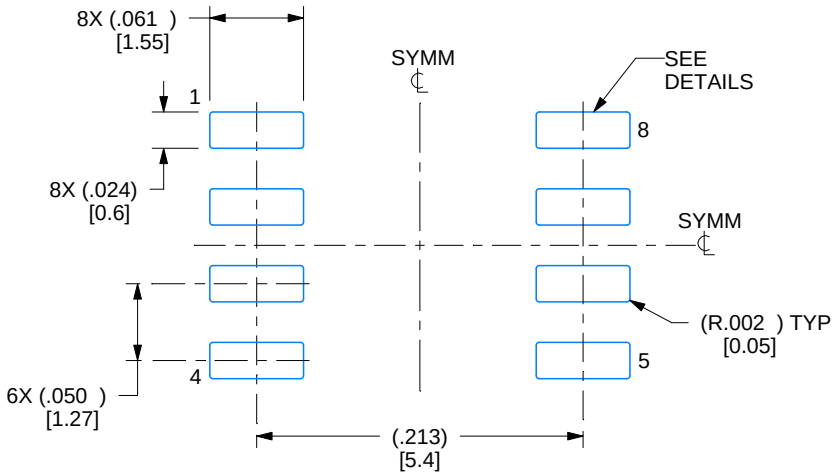
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

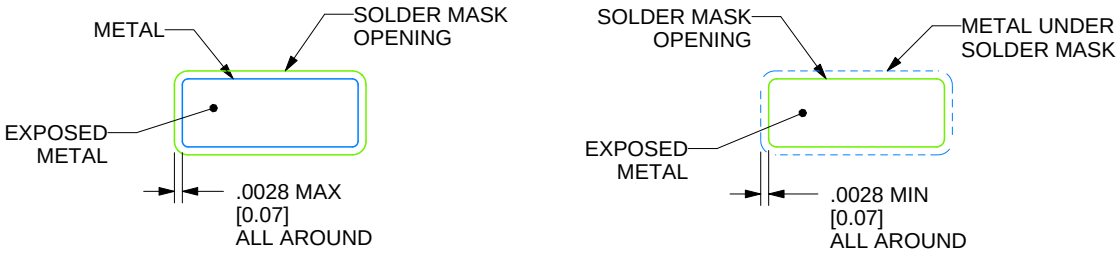


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

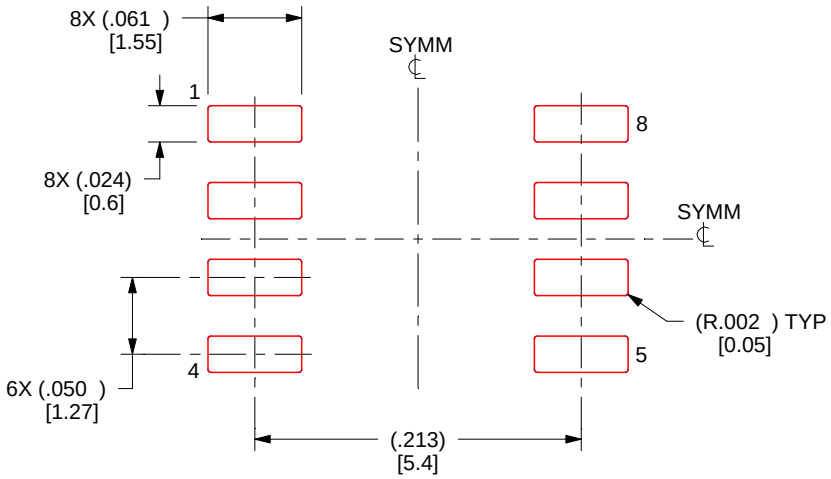
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月