

TPS624xx-Q1 車載用 2.25MHz、固定 VOUT、デュアル降圧型コンバータ

1 特長

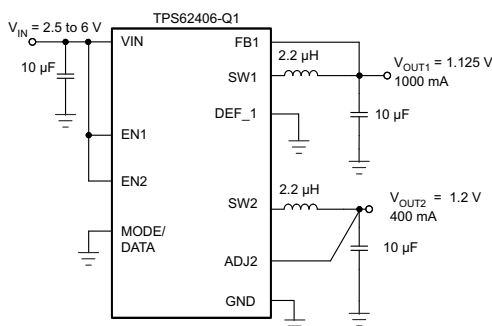
- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
 - デバイス温度グレード 1: 動作時の接合部温度範囲: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C4B
- 高効率: 最大 95%
- V_{IN} 範囲: 2.5V~6V
- 2.25MHz 固定周波数動作
- TPS62406-Q1 の出力電流: 1000mA/400mA
- TPS62407-Q1 の出力電流: 400mA/600mA
- TPS62422-Q1 の出力電流: 1000mA/600mA
- TPS62423-Q1 の出力電流: 800mA/800mA
- TPS62424-Q1 の出力電流: 800mA/800mA
- 固定出力電圧
- EasyScale™ によるオプションの 1 ピン・シリアル・インターフェイス
- 軽負荷電流時のパワー・セーブ・モード
- 位相差 180° の動作
- PWM モードで $\pm 1\%$ の出力電圧精度
- 両方のコンバータについて、静止電流 32 μA (標準値)
- 100% デューティ・サイクル動作による最小のドロップアウト電圧

2 アプリケーション

- 車載用ポイント・オブ・ロード・レギュレータ
- [ADAS カメラ・モジュール](#)
- [ミラー代替 \(CMS\)](#)
- [インフォテインメントとクラスタ](#)

3 概要

TPS624xx-Q1 ファミリのデバイスは、先進運転支援システム (ADAS) など車載アプリケーション用の同期デュアル



概略回路図

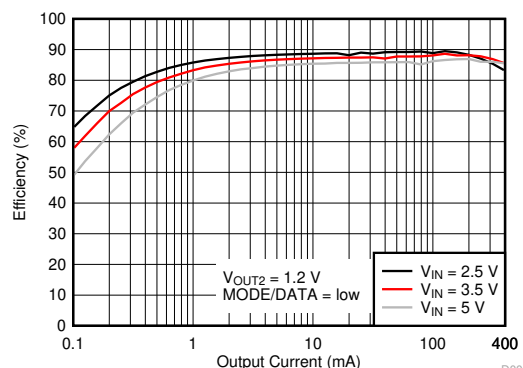
降圧 DC-DC コンバータです。これらのデバイスは、標準の 3.3V または 5V 電圧レールで給電される 2 つの独立した出力電圧レールと、ADAS カメラ・モジュールの CMOS イメージまたはシリアルライザ - デシリアルライザに給電するために最適化された固定電圧を備えています。

EasyScale™ シリアル・インターフェイスにより、動作中に出力電圧の変更が可能です。固定出力電圧バージョンの TPS624xx-Q1 は、低消費電力プロセッサ向けに、1 ピンで制御される単純な動的電圧スケールをサポートしています。

TPS624xx-Q1 ファミリのデバイスは 2.25MHz の固定スイッチング周波数で動作し、負荷電流が軽いときはパワー・セーブ・モードに移行し、負荷電流の全範囲について高い効率を維持します。低ノイズのアプリケーションでは、MODE/DATA ピンを HIGH にして、デバイスを強制的に固定周波数の PWM モードにすることもできます。シャットダウン・モードでは、消費電流が 1.2 μA (標準値) に低下します。このデバイスは小さなインダクタとコンデンサを使用できるため、ソリューションを小型化できます。

製品情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
TPS62406-Q1	VSON (10)	3.00mm × 3.00mm
TPS62407-Q1		
TPS62422-Q1		
TPS62423-Q1		
TPS62424-Q1		



TPS62406-Q1 の効率と出力電流 $V_{\text{OUT}2}$ との関係



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (August 2018) to Revision E (March 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Removed manual package option addendum, tape and reel information, and package drawings.....	32

Changes from Revision * (December 2014) to Revision A (October 2015)	Page
• Changed the I_{OUT1} and I_{OUT2} current for the TPS62406-Q1 device in the <i>Device Comparison Table</i>	3
• Changed forward current limit PMOS and NMOS for the TPS62406-Q1.....	5

5 Device Comparison Table

PART NUMBER	DEFAULT OUTPUT VOLTAGE			OUTPUT CURRENT	
	V _{OUT1}	Fixed default	DEF_1 = High 1.125 V DEF_1 = Low 1.125 V	I _{OUT1}	1000 mA
TPS62406-Q1	V _{OUT2}	Fixed default 1.2 V		I _{OUT2}	400 mA
	V _{OUT1}	Fixed default	DEF_1 = High 1.225 V DEF_1 = Low 1.225 V	I _{OUT1}	400 mA
TPS62407-Q1	V _{OUT2}	Fixed default 1.85 V		I _{OUT2}	600 mA
	V _{OUT1}	Fixed default	DEF_1 = High 1.8 V DEF_1 = Low 1.15 V	I _{OUT1}	1000 mA
TPS62422-Q1	V _{OUT2}	Fixed default 1.2V		I _{OUT2}	600 mA
	V _{OUT1}	Fixed default	DEF_1 = High 1.5 V DEF_1 = Low 1.2 V	I _{OUT1}	800 mA
TPS62423-Q1	V _{OUT2}	Fixed default 1.8V		I _{OUT2}	800 mA
	V _{OUT1}	Fixed default	DEF_1 = High 1.3 V DEF_1 = Low 1.1 V	I _{OUT1}	800 mA
TPS62424-Q1	V _{OUT2}	Fixed default 1.8V		I _{OUT2}	800 mA

6 Pin Configuration and Functions

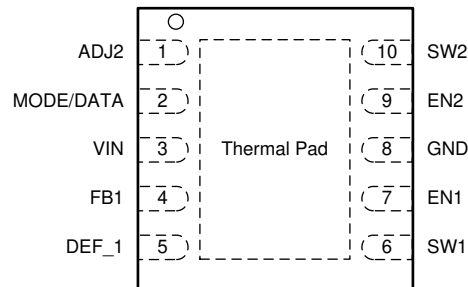


图 6-1. DRC Package 10-Pin VSON With Thermal Pad Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ2	1	I	Output voltage sense pin for the internal feedback divider. This pin must connect directly to the output. If using the EasyScale interface-on converter 2, this pin must also connect directly to the output.
DEF_1	5	I	This pin defines the output voltage of converter 1 and is a digital input, that selects between two fixed default output voltages. See セクション 5 for output voltage setting of the different device options. For TPS62406-Q1 and TPS62407-Q1 the output voltage is same independent of DEF_1 pin level. This pin must be terminated.
EN1	7	I	Enable input for converter 1, active-high. This pin must be terminated.
EN2	9	I	Enable input for converter 2, active-high. This pin must be terminated.
FB1	4	I	Output voltage sense pin for the internal feedback divider. This pin is connected to the output.
GND	8	—	GND for both converters; connect this pin to the thermal pad.

表 6-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
MODE/DATA	2	I/O	This pin has two functions: <ol style="list-style-type: none"> 1. Operation-mode selection: With low level, enables power-save mode where the device operates in PFM mode at light loads and automatically enters PWM mode at heavy loads. Pulling this PIN to high forces the device to operate in PWM mode over the whole load range. 2. EasyScale interface function: One-wire serial interface to change the output voltage of both converters. The pin has an open-drain output to provide an acknowledge condition if requested. The current into the open-drain output stage may not exceed 500 μA. The EasyScale interface is active if either EN1 or EN2 is high.
SW1	6	I/O	Switch pin of converter 1. Connect to inductor
SW2	10	I/O	Switch pin of converter 2. Connect to inductor
VIN	3	I	Input pin, connect to supply or battery voltage, 2.5 V to 6 V. Connect the input capacitor C_{IN} as close as possible between VIN pin and GND pin.
Thermal pad		—	Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
Input voltage ⁽²⁾	V _{IN}	-0.3	7	V	
Voltage ⁽²⁾	EN, MODE/DATA, DEF_1	-0.3	V _{IN} + 0.3, ≤ 7	V	
	SW1, SW2	-0.3	7	V	
	ADJ2, FB1	-0.3	V _{IN} + 0.3, ≤ 7	V	
Current	MODE/DATA		≤ 0.5	mA	
Maximum operating junction temperature, T _{Jmax}			150	°C	
Storage temperature, T _{stg}			-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V	
		Charged device model (CDM), per AEC Q100-011	All pins	±500	V
			Corner pins (1, 5, 6, and 10)	±750	

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Supply voltage	2.5	6	V
T _J	Operating junction temperature	-40	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS624xx-Q1	UNIT
		DRC (VSON)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	42.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	46.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	18.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	18.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

V_{IN} = 3.6 V, EN1 = EN2 = V_{IN}, MODE = GND, L1 = L2 = 2.2 μH, C_{OUT1} = C_{OUT2} = 20 μF, T_J = -40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT					
V _{IN}	Input voltage range	2.5		6	V

$V_{IN} = 3.6\text{ V}$, $EN1 = EN2 = V_{IN}$, $MODE = GND$, $L1 = L2 = 2.2\ \mu\text{H}$, $C_{OUT1} = C_{OUT2} = 20\ \mu\text{F}$, $T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I_Q	Operating quiescent current	One converter, no load on the output. PFM mode enabled (MODE/DATA = GND) device not switching, $EN1 = 1$ or $EN2 = 1$		19	35	μA	
		Two converters, no load on the output. PFM mode enabled (MODE/DATA = GND) device not switching, $EN1 = EN2 = 1$		32	50		
		No load on the output, MODE/DATA = GND, for one converter ⁽¹⁾		23			
			No load on the output, MODE/DATA = V_{IN} , for one converter ⁽¹⁾		3.6		mA
I_{SD}	Shutdown current	$EN1, EN2 = GND$, $V_{IN} = 3.6\text{ V}$ ⁽²⁾		1.2	3	μA	
		$EN1, EN2 = GND$, V_{IN} ramped from 0 V to 3.6 V ⁽³⁾		0.1	1.5		
V_{UVLO}	Undervoltage lockout threshold	Falling		1.5	2.35	V	
		Rising			2.4		
ENABLE EN1, EN2							
V_{IH}	High-level input voltage range, EN1, EN2		1.2		V_{IN}	V	
V_{IL}	Low-level input voltage range, EN1, EN2		0		0.4	V	
I_{IN}	Input bias current, EN1, EN2	$EN1, EN2 = GND$ or V_{IN}		0.05	1	μA	
DEF_1 INPUT							
V_{DEF_1H}	DEF_1 high-level digital input voltage range		0.9		V_{IN}	V	
V_{DEF_1L}	DEF_1 low-level digital input voltage range		0		0.4	V	
I_{IN}	Input bias current DEF_1	$DEF_1 = GND$ or V_{IN}		0.01	1	μA	
MODE/DATA							
V_{IH}	High-level input voltage range, MODE/DATA		1.2		V_{IN}	V	
V_{IL}	Low-level input voltage range, MODE/DATA		0		0.4	V	
I_{IN}	Input bias current, MODE/DATA	$MODE/DATA = GND$ or V_{IN}		0.01	1	μA	
V_{OH}	Acknowledge output voltage high	Open drain, through external pullup resistor			V_{IN}	V	
V_{OL}	Acknowledge output voltage low	Open drain, sink current 500 μA	0		0.4	V	
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on-resistance, converter 1 and 2	$V_{IN} = V_{GS} = 3.6\text{ V}$		280	620	$\text{m}\Omega$	
I_{LK_PMOS}	P-channel leakage current	$V_{DS} = 6\text{ V}$			1	μA	
$r_{DS(on)}$	N-channel MOSFET on-resistance converter 1 and 2	$V_{IN} = V_{GS} = 3.6\text{ V}$		200	450	$\text{m}\Omega$	
$I_{LK_SW1/SW2}$	Leakage current into SW1 or SW2 pin	Includes N-channel leakage current, $V_{IN} = \text{open}$, $V_{SW} = 6\text{ V}$, $EN = GND$ ⁽⁴⁾		6	7.5	μA	
I_{LIMF}	Forward current limit PMOS and NMOS	TPS62406-Q1 V_{OUT1}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	1.18	1.4	1.61	A
		TPS62406-Q1 V_{OUT2}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	0.68	0.8	0.92	
		TPS62407-Q1 V_{OUT1}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	0.68	0.8	0.92	
		TPS62407-Q1 V_{OUT2}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	0.75	1	1.15	
		TPS62422-Q1 V_{OUT1}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	1.18	1.4	1.61	
		TPS62422-Q1 V_{OUT2}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	0.75	1	1.15	
		TPS62423-Q1 V_{OUT1}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	1	1.2	1.38	
		TPS62423-Q1 V_{OUT2}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	1	1.2	1.38	
		TPS62424-Q1 V_{OUT1}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	1	1.2	1.38	
		TPS62424-Q1 V_{OUT2}	$2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$	1	1.2	1.38	

$V_{IN} = 3.6\text{ V}$, $EN1 = EN2 = V_{IN}$, $MODE = GND$, $L1 = L2 = 2.2\ \mu\text{H}$, $C_{OUT1} = C_{OUT2} = 20\ \mu\text{F}$, $T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown	Increasing junction temperature		150		$^\circ\text{C}$
	Thermal shutdown hysteresis	Decreasing junction temperature		20		$^\circ\text{C}$
OUTPUT						
V_{ref}	Internal Reference voltage			600		mV
$V_{OUTx(PFM)}$	DC output voltage accuracy	Voltage positioning active, $MODE/DATA = GND$, device operating in PFM mode, $V_{IN} = 2.5\text{ V}$ to 5 V ⁽⁵⁾ ⁽⁶⁾	-1.5%	1%	2.5%	
$V_{OUTx(PWM)}$		$MODE/DATA = GND$; device operating in PWM mode, $V_{IN} = 2.5\text{ V}$ to 6 V ⁽⁶⁾	-1%	0%	1%	
		$V_{IN} = 2.5\text{ V}$ to 6 V , $MODE/DATA = V_{IN}$. Fixed PWM operation, $0\text{ mA} < I_{OUT1} < 400\text{ mA}$; $0\text{ mA} < I_{OUT2} < 600\text{ mA}$ ⁽⁷⁾	-1%	0%	1%	
	DC output voltage load regulation	PWM operation mode			0.5	%/A

- (1) Device is switching with no load on the output, $L1 = L2 = 3.3\ \mu\text{H}$, value includes losses of the coil.
- (2) These values are valid after enabling the device one time ($EN1$ or $EN2 = \text{high}$) and maintaining supply voltage V_{IN} .
- (3) These values are valid when the device is disabled ($EN1$ and $EN2$ low) and supply voltage V_{IN} is powered up. The values remain valid until enabling the device the first time ($EN1$ or $EN2 = \text{high}$). After the first enable, Note 3 becomes valid.
- (4) An internal resistor of $1\ \text{M}\Omega$ connects pins SW1 and SW2 to GND.
- (5) Configuration L1 or L2 typ. $2.2\ \mu\text{H}$, C_{OUTx} typ $20\ \mu\text{F}$. See parameter measurement information, the output voltage ripple in PFM mode depends on the effective capacitance of the output capacitor; larger output capacitors lead to tighter output voltage tolerance.
- (6) In power-save mode, the device typically enters PWM operation at $I_{PSM} = V_{IN} / 32\ \Omega$.
- (7) For $V_{OUTx} > 2\text{ V}$, $V_{IN\ min} = V_{OUTx} + 0.5\text{ V}$

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
INTERFACE TIMING						
t_{Start}	Start time		2			μs
$t_{\text{H_LB}}$	High-time low bit, logic 0 detection	Signal level on MODE/DATA pin is > 1.2 V	2		200	μs
$t_{\text{L_LB}}$	Low-time low bit, logic 0 detection	Signal level on MODE/DATA pin < 0.4 V	$2 \times t_{\text{H_LB}}$		400	μs
$t_{\text{L_HB}}$	Low-time high bit, logic 1 detection	Signal level on MODE/DATA pin < 0.4 V	2		200	μs
$t_{\text{H_HB}}$	High-time high bit, logic 1 detection	Signal level on MODE/DATA pin is > 1.2 V	$2 \times t_{\text{L_HB}}$		400	μs
t_{EOS}	End of stream		2			μs
t_{ACKN}	Duration of acknowledge condition (MODE/DATA line pulled low by the device)	V_{IN} 2.5 V to 6 V	400		520	μs
t_{valACK}	Acknowledge valid time				2	μs
t_{timeout}	Time-out for entering power-save mode	MODE/DATA pin changes from high to low			520	μs

7.7 Switching Characteristics

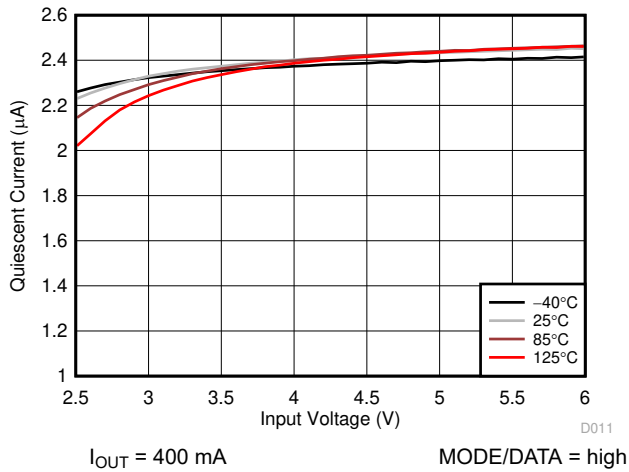
$V_{\text{IN}} = 3.6 \text{ V}$, $\text{EN1} = \text{EN2} = V_{\text{IN}}$, $\text{MODE} = \text{GND}$, $L1 = L2 = 2.2 \mu\text{H}$, $C_{\text{OUT1}} = C_{\text{OUT2}} = 20 \mu\text{F}$, $T_{\text{J}} = -40^\circ\text{C}$ to 125°C , typical values are at $T_{\text{J}} = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_{SW}	Oscillator frequency	$3 \text{ V} \leq V_{\text{IN}} \leq 6 \text{ V}^{(1)}$	2	2.25	2.7	MHz
OUTPUT						
$t_{\text{Start up}}$	Start-up time	Activation time to start switching ⁽²⁾		170		μs
t_{Ramp}	V_{OUTx} ramp-up time	Time to ramp from 5% to 95% of V_{OUTx}		750		μs

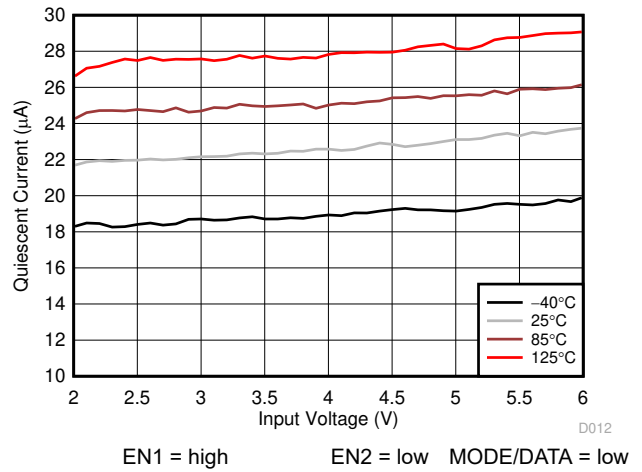
(1) For $V_{\text{OUTx}} > 2 \text{ V}$, $V_{\text{IN min}} = V_{\text{OUTx}} + 0.5 \text{ V}$

(2) This time is valid if one converter turns from shutdown mode ($\text{EN2} = 0$) to active mode ($\text{EN2} = 1$) with the other converter already enabled (for example, $\text{EN1} = 1$). In case both converters are turned from shutdown mode (EN1 and $\text{EN2} = 0$) to active mode (EN1 and/or $\text{EN2} = 1$), a typical value of typ 80 μs for ramp up of internal circuits must be added. After t_{start} , the converter starts switching and ramps V_{OUTx} .

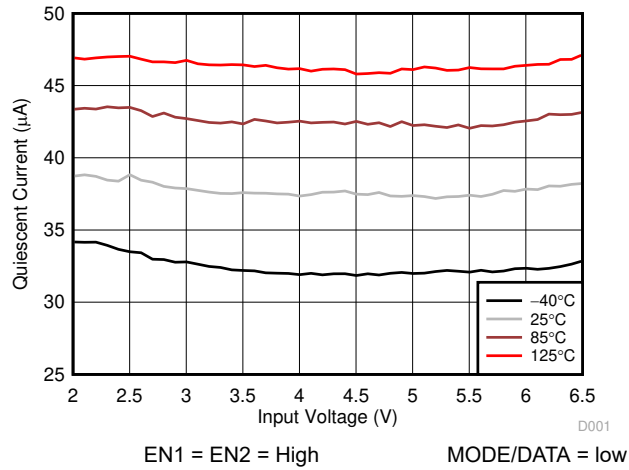
7.8 Typical Characteristics



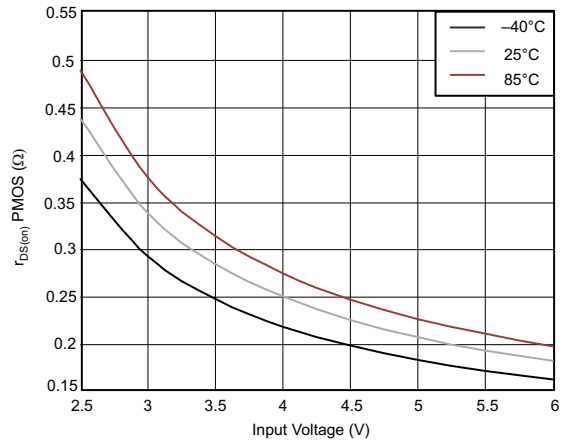
7-1. TPS62407-Q1 Switching Frequency



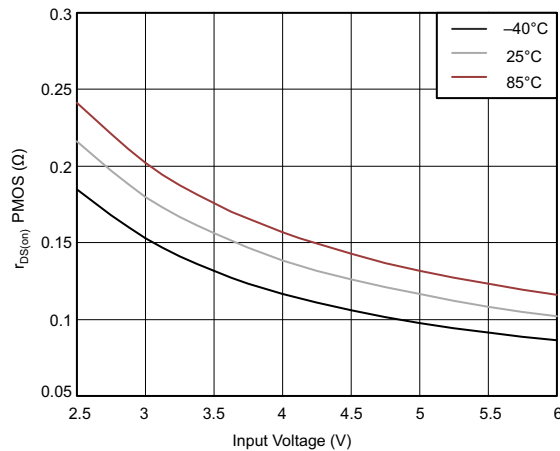
7-2. TPS62407-Q1 Quiescent Current, One Converter On



7-3. TPS62407-Q1 Quiescent Current, Both Converters On



7-4. $r_{\text{DS(on)}}$ PMOS vs V_{IN}



7-5. $r_{\text{DS(on)}}$ NMOS vs V_{IN}

8 Detailed Description

8.1 Overview

The TPS624xx-Q1 device includes two synchronous step-down converters. The converters operate with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. With the power-save mode enabled, the converters automatically enter power-save mode at light load currents and operate in PFM (pulse frequency modulation).

During PWM operation, the converters use a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch turns on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

Each converter integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET turns off and the N-channel MOSFET turns on. If the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit.

The two DC-DC converters operate synchronized to each other. A 180° phase shift between converter 1 and converter 2 decreases the input rms current.

8.1.1 Converter 1

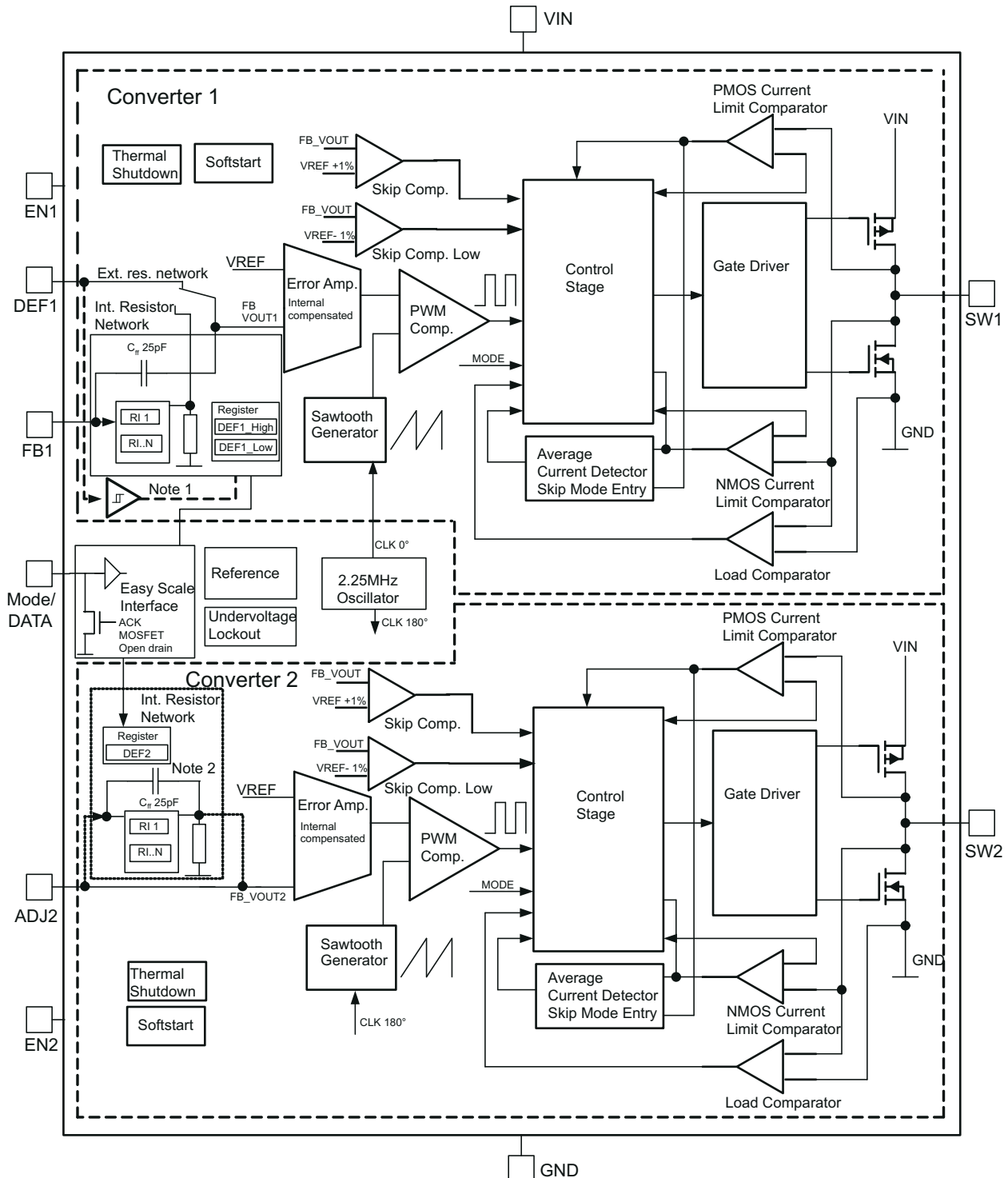
It is possible to change the output voltage of converter 1 with the EasyScale serial Interface. This makes the device very flexible for output-voltage adjustment. In this case, the device uses an internal resistor network.

The output voltage can also be selected using the DEF_1 pin configuration as a digital input. For these voltage version the DEF_1 pin select the same output voltage for DEF_1=high or DEF_1=low.

8.1.2 Converter 2

It is also possible to change the output voltage of converter 2 via the EasyScale interface.

8.2 Functional Block Diagram



- A. In the fixed output-voltage version, the DEF_1 pin connects to an internal digital input and disconnects from the error amplifier.
- B. To set the output voltage of converter 2 through the EasyScale™ interface, the ADJ2 pin must directly connect to V_{OUT2}.

8.3 Feature Description

8.3.1 Enable

The device has a separate EN pin for each converter to start up each converter independently. If EN1 or EN2 is set to high, the corresponding converter starts up with soft start.

Pulling EN1 and EN2 pin low forces the device into shutdown, with a shutdown quiescent current of typically 1.2 μ A. In this mode, the P- and N-channel MOSFETs turn off and the entire internal control circuitry switches off. For proper operation, terminate the EN1 and EN2 pins, do not leave them floating.

8.3.2 DEF_1 Pin Function

The DEF_1 pin, dedicated to converter 1, makes the output voltage selection very flexible to support dynamic voltage management. Having this pin tied to a low level sets the output voltage according to the value in register REG_DEF_1_Low. The default voltage is 1.125 V for TPS62406-Q1. Having the pin tied to a high level sets the output voltage according to the value in register REG_DEF_1_High. The default value in this case is 1.125 V as well. The level of the DEF_1 pin selects between the two registers, REG_DEF_1_Low and REG_DEF_1_High, for the output-voltage setting. One can change the content of each register (and therefore output voltage) individually through the EasyScale interface. This makes the device very flexible in terms of output voltage setting; see [表 8-3](#)

8.3.3 180° Out-of-Phase Operation

In PWM mode, the converters operate with a 180° turn-on phase shift of the PMOS (high side) transistors. This prevents the high-side switches of both converters from turning on simultaneously, reducing the input current ripple. This feature reduces the surge current drawn from the supply.

8.3.4 Short-Circuit Protection

Both outputs are short-circuit protected with maximum output current = I_{LIMF} (P-MOS and N-MOS). Once the PMOS switch reaches its current limit, it turns off and the NMOS switch turns on. The PMOS only turns on again once the current in the NMOS decreases below the NMOS current limit.

8.3.5 Thermal Shutdown

As soon as the junction temperature, T_J , exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs turn off. The device continues its operation when the junction temperature falls below the thermal-shutdown hysteresis.

8.3.6 EasyScale Interface: One-Pin Serial Interface for Dynamic Output-Voltage Adjustment

8.3.6.1 General

The EasyScale interface is a simple but very flexible one-pin interface to configure the output voltage of both DC-DC converters. A master-slave structure is the basis of the interface, where the master is typically a microcontroller or application processor. [图 8-3](#) and [表 8-2](#) give an overview of the protocol. The protocol consists of a device-specific address byte and a data byte. The device-specific address byte is fixed to 4E hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the request-for-acknowledge condition. The acknowledge condition only applies after correct reception of the protocol.

The advantage of the EasyScale interface compared to other one-pin interfaces is that its bit detection is to a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7 kb/s and up to 160 kb/s. Furthermore, the interface shares the MODE/DATA pin and requires no additional pin.

8.3.6.2 Protocol

Transmission of all bits is MSB first and LSB last. [图 8-4](#) shows the protocol without the acknowledge request (bit RFA = 0), [图 8-5](#) with the acknowledge request (bit RFA = 1).

Prior to both bytes, device address byte and data byte, one must apply a start condition. For this, pull the MODE/DATA pin high for at least t_{Start} before the bit transmission starts with the falling edge. In case the MODE/DATA

line was already at a high level (forced PWM mode selection), the device requires no start condition prior to the device address byte.

Close the transmission of each byte with an end-of-stream condition for at least t_{EOS} .

8.4 Device Functional Modes

8.4.1 Power-Save Mode

Setting the MODE/DATA pin to low for both converters enables power-save mode. If the load current of a converter decreases, this converter enters power-save-mode operation automatically. The transition of a converter to power-save mode is independent from the operating condition of the other converter. During power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage in PFM mode to typically 1% above nominal V_{OUTx} . This voltage positioning feature minimizes voltage drops caused by a sudden load step.

In order to optimize the converter efficiency at light load, the device monitors average inductor current. The device changes from PWM mode to power-save mode if in PWM mode the inductor current falls below a certain threshold. The typical output current threshold, which one can calculate using 式 1 for each converter, depends on V_{IN} .

式 1: Average output current threshold to enter PFM mode

$$I_{OUT_PFM_enter} = \frac{V_{IN_DCDC}}{32 \Omega} \quad (1)$$

式 2: Average output current threshold to leave PFM mode

$$I_{OUT_PFM_leave} = \frac{V_{IN_DCDC}}{24 \Omega} \quad (2)$$

To keep the output-voltage ripple in power-save mode low, a single threshold comparator (skip comparator) monitors the output voltage. As the output voltage falls below the skip-comparator threshold (skip comp) of 1% above nominal V_{OUTx} , the corresponding converter starts switching for a minimum time period of typically 1 μ s and provides current to the load and the output capacitor. Therefore, the output voltage increases and the device maintains switching until the output voltage trips the skip comparator threshold (skip comp) again. At this moment, all switching activity stops and the quiescent current reduces to minimum. The output capacitor supplies the load until the output voltage has dropped below the threshold again. Hereupon, the device starts switching again.

The converter leaves power-save mode and enters PWM mode if the output current exceeds the $I_{OUT_PFM_leave}$ current or if the output voltage falls below a second comparator threshold, called the skip-comparator-low (Skip Comp Low) threshold. This skip-comparator-low threshold is 2% below nominal V_{OUTx} and enables a fast transition from power-save mode to PWM mode during a load step.

Power-save mode typically reduces the quiescent current to 19 μ A for one converter and 32 μ A for both converters active. This single-skip comparator threshold method in power-save mode results in a very low output-voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing output capacitor values minimizes the output ripple. One can disable the power-save mode by setting the MODE/DATA pin to high. Both converters then operate in fixed PWM mode. Power-save mode enable or disable applies to both converters.

8.4.1.1 Dynamic Voltage Positioning

This feature reduces the voltage under- and overshoots at load steps from light to heavy load and from heavy to light load. Power-save-mode operation activates dynamic voltage positioning and provides more headroom for both the voltage drop at a load step and the voltage increase when a load is switched off, which improves load-transient behavior.

At light loads, in which the converter operates in PFM mode, the output voltage regulation is typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to 2% below the nominal value and enters PWM mode. During a load transition from heavy load to light load, the device also minimizes voltage overshoot because of active regulation turning on the N-channel switch.

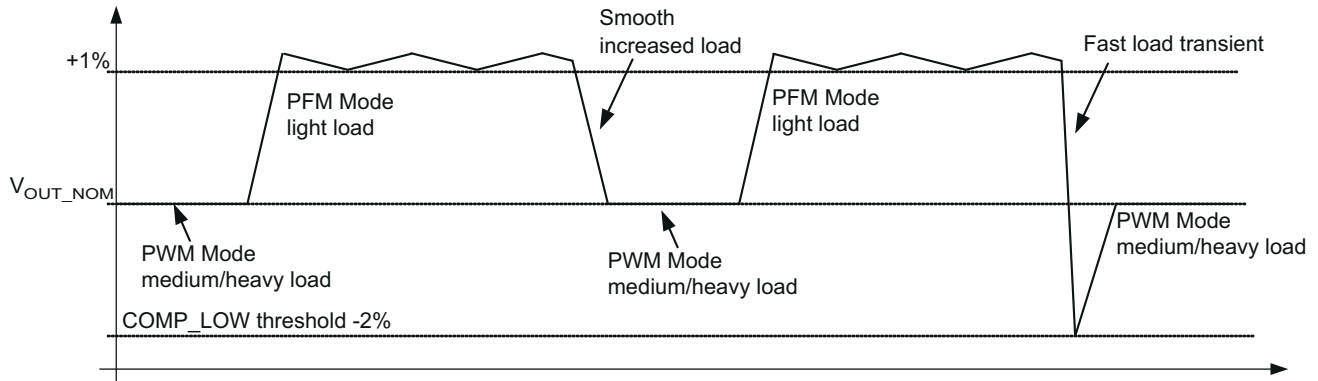


Figure 8-1. Dynamic Voltage Positioning

8.4.1.2 Soft Start

The two converters have an internal soft-start circuit that limits the inrush current during startup. Figure 8-2 shows control of the output-voltage ramp-up during soft start.

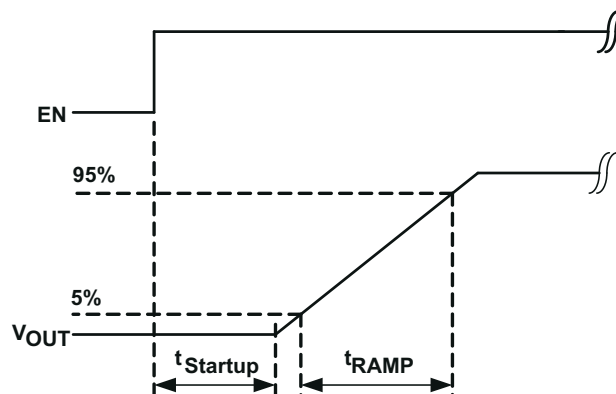


Figure 8-2. Soft Start

8.4.1.3 100% Duty-Cycle Low-Dropout Operation

The converters offer a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery-voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, which one can calculate as:

$$V_{in_{min}} = V_{out_{max}} + I_{out_{max}} \times (R_{DS(on)_{max}} + R_L) \quad (3)$$

with

- $I_{OUTx_{max}}$ = maximum output current plus inductor ripple current
- $r_{DS(on)_{max}}$ = maximum P-channel switch $r_{DS(on)}$
- R_L = dc resistance of the inductor
- $V_{OUTx_{max}}$ = nominal output voltage plus maximum output-voltage tolerance

With decreasing load current, the device automatically switches into pulse-skipping operation, in which the power stage operates intermittently based on load demand. Running cycles periodically minimizes the switching losses, and the device runs with a minimum quiescent current, maintaining high efficiency.

8.4.1.4 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunction at low input voltages and from excessive discharge of the battery, and disables the converters. The undervoltage lockout threshold is typically 1.5 V; maximum of 2.35 V. In case the interface overwrites the default register values, the new values in the registers REG_DEF_1_High, REG_DEF_1_Low and REG_DEF_2 remain valid as long the supply voltage does not fall below the undervoltage lockout threshold, independent of disabling of the converters.

8.4.2 Mode Selection

The MODE/DATA pin allows mode selection between forced PWM mode and power-save mode for both converters. Furthermore, this pin is a multipurpose pin and provides (besides mode selection) a one-pin interface to receive serial data from a host to set the output voltage, as described in the [EasyScale Interface](#) section.

Connecting this pin to GND enables the automatic PWM and power-save-mode operation. The converters operate in fixed-frequency PWM mode at moderate-to-heavy loads, and in the PFM mode during light loads, maintaining high efficiency over a wide load-current range.

Pulling the MODE/DATA pin high forces both converters to operate constantly in the PWM mode, even at light load currents. The advantage is that the converters operate with a fixed frequency, allowing simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

In the case of changing the operation mode from forced PWM mode (MODE/DATA = high) to power-save mode (MODE/DATA = 0), enabling the power-save mode occurs after a delay time of t_{timeout} , which is 520 μs maximum.

Setting the MODE/DATA to 1 enables forced-PWM-mode operation immediately.

8.5 Programming

8.5.1 Addressable Registers

Three registers with a data content of 5 bits are addressable. With 5-bit data content, 32 different values for each register are available. [表 8-1](#) shows the addressable registers to set the output voltage when the DEF_1 pin works as a digital input. In this case, converter 1 has a related register for each DEF_1 pin condition, and one register for converter 2. A high or low condition on pin DEF_1 selects either the content of register REG_DEF_1_High or REG_DEF_1_Low, thus setting the output voltage of converter 1 according to the values in Selectable Output Voltage Converter 1, With Pin DEF_1 as Digital Input. Use of a precise internal resistor divider network to generate these output voltages makes external resistors unnecessary (less board space) and provides higher output-voltage accuracy. Enabling at least one of the converters (EN1 or EN2 is high) activates the interface. After the startup time t_{start} (170 μs), the interface is ready for data reception.

表 8-1. Addressable Registers for Default Fixed-Output Voltage Options (PIN DEF_1 = Digital Input)

DEVICE	REGISTER	DESCRIPTION	DEF_1 PIN	A1	A0	D4	D3	D2	D1	D0
TPS624xx-Q1 ,	REG_DEF_1_High	Converter 1 output voltage setting for DEF_1 = High condition. The content of the register is active with the DEF_1 pin high.	High	0	1	Output voltage setting, see 表 8-3				
	REG_DEF_1_Low	Converter 1 output voltage setting for DEF_1 = Low condition.	Low	0	0	Output voltage setting, see 表 8-3				
	REG_DEF_2	Converter 2 output voltage	Not applicable	1	0	Output voltage setting, see 表 8-4				
		Do not use		1	1					

8.5.1.1 Bit Decoding

The bit detection is based on a PWM scheme, where the criterion is the relation between the low time and high time of the low or high bit (t_{L_xB} and t_{H_xB}). Bit detection can be simplified to:

High bit: $t_{H_HB} > t_{L_HB}$, but with t_{H_HB} at least $2 \times t_{L_HB}$, see [Figure 8-3](#).

Low bit: $t_{L_LB} > t_{H_LB}$, but with t_{L_LB} at least $2 \times t_{H_LB}$, see [Figure 8-3](#).

The bit detection starts with a falling edge on the MODE/DATA pin and ends with the next falling edge. Detection of a 0 or 1 depends on the relation between t_{L_xB} and t_{H_xB} .

8.5.1.2 Acknowledge

The device only applies the acknowledge condition if all of the following occurs:

- A set RFA bit requests an acknowledge
- The transmitted device address matches with the device address of the device
- Correct reception of 16 bits occurred

In this case, the device turns on the internal ACKN-MOSFET and pulls the MODE/DATA pin low for the time t_{ACKN} , which is 520 μ s maximum. The acknowledge condition is valid after an internal delay time t_{valACK} . This means the internal ACKN-MOSFET turns on after t_{valACK} , on detection of the last falling edge of the protocol. The master controller keeps the line low during this time.

The master device can detect the acknowledge condition with its input by releasing the MODE/DATA pin after t_{valACK} and reading back a 0.

In case of an invalid device address, or not-correctly-received protocol, application of a no-acknowledge condition does not occur; thus, the internal MOSFET does not turn on, and the external pullup resistor pulls the MODE/DATA pin high after t_{valACK} . One can use the MODE/DATA pin again after the acknowledge condition ends.

Note

The master device must have an open-drain output in order to request the acknowledge condition.

In case of a push-pull output stage, TI recommends using a series resistor in the MODE/DATA line to limit the current to 500 μ A in case of an accidentally requested acknowledge, to protect the internal ACKN-MOSFET.

8.5.1.3 Mode Selection

Use of the MODE/DATA pin for two functions, interface and mode selection, necessitates a determination of when to decode the bit stream or to change the operation mode.

The device enters forced PWM mode operation immediately whenever the MODE/DATA pin turns to high level. The device also stays in forced PWM mode during the entire protocol reception time.

With a falling edge on the MODE/DATA pin, the device starts bit decoding. If the MODE/DATA pin stays low for at least $t_{timeout}$, the device gets an internal time-out and enables power-save-mode operation.

The device ignores a protocol sent within this time because the first interpretation of a falling edge for the mode change is at the start of the first bit. In this case, TI recommends sending the protocol first, and then changing to power-save mode at the end of the protocol.

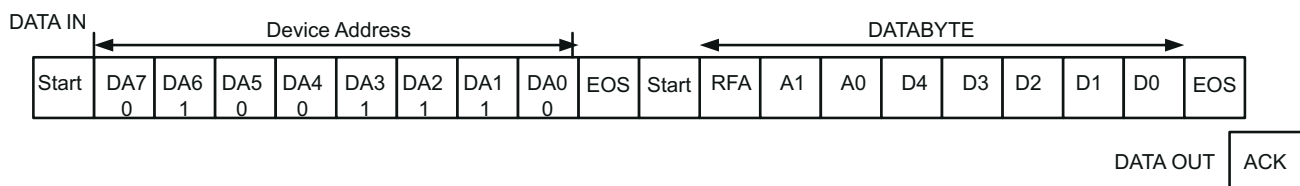


Figure 8-3. EasyScale Protocol Overview

表 8-2. EasyScale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device address byte 4E hex	7	DA7	IN	0 MSB device address
	6	DA6	IN	1
	5	DA5	IN	0
	4	DA4	IN	0
	3	DA3	IN	1
	2	DA2	IN	1
	1	DA1	IN	1
	0	DA0	IN	0 LSB device address
Data byte	7 (MSB)	RFA	IN	Request for acknowledge; if high, the device applies an acknowledge condition.
	6	A1		Address bit 1
	5	A0		Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, the device applies this condition only in the case of a set RFA bit. Open-drain output, the host must pull the line high with a pullup resistor. One can only use this feature if the master has an open-drain output stage. In case of a push-pull output stage, do not request an acknowledge condition.

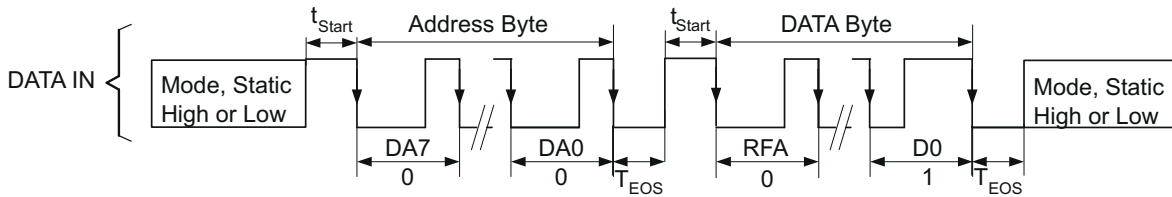


图 8-4. EasyScale Protocol Without Acknowledge

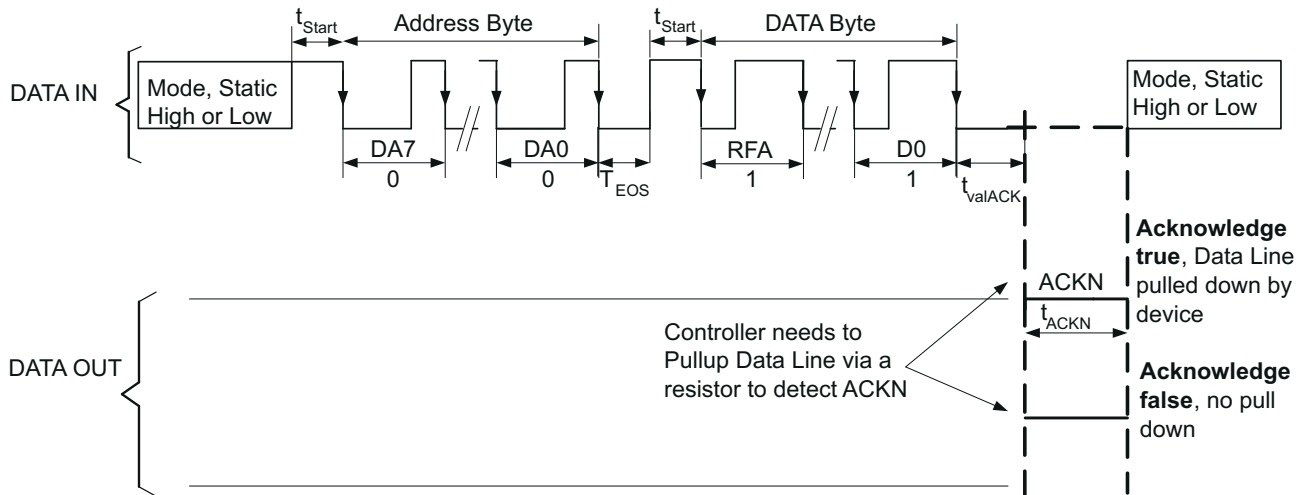
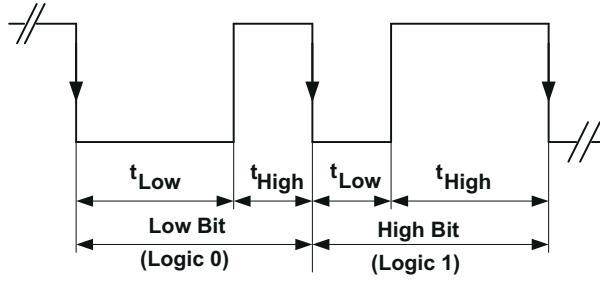
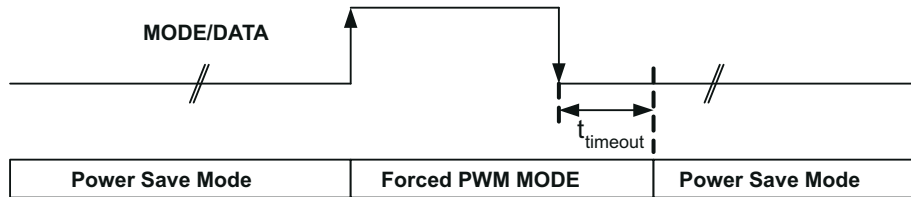


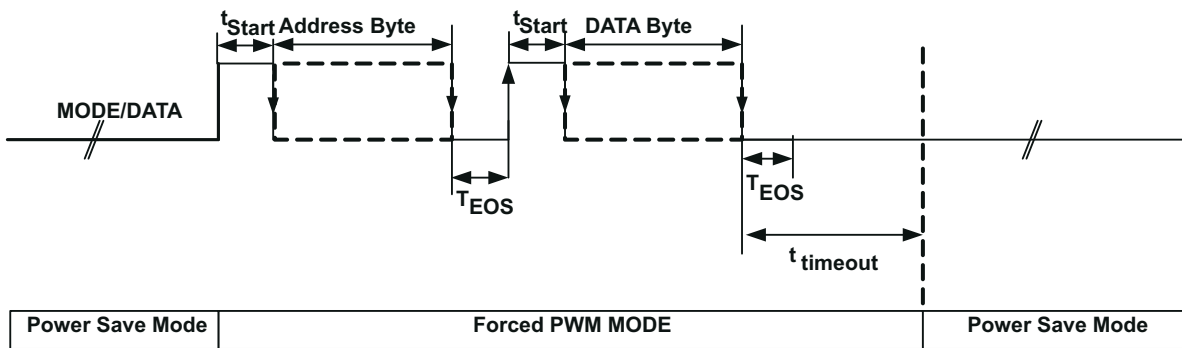
图 8-5. EasyScale Protocol Including Acknowledge



8-6. EasyScale – Bit Coding



8-7. MODE/DATA PIN: Mode Selection



8-8. MODE/DATA Pin: Power-Save-Mode and Interface Communication

表 8-3. Selectable Output Voltages for Converter 1,
With Pin DEF_1 as Digital Input

	TPS624xx-Q1 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_LOW	TPS624xx-Q1 VOLTAGE [V] REGISTER REG_DEF_1_HIGH	D4	D3	D2	D1	D0
0	0.8	0.9	0	0	0	0	0
1	0.825	0.925	0	0	0	0	1
2	0.85	0.95	0	0	0	1	0
3	0.875	0.975	0	0	0	1	1
4	0.9	1.0	0	0	1	0	0
5	0.925	1.025	0	0	1	0	1
6	0.95	1.050	0	0	1	1	0
7	0.975	1.075	0	0	1	1	1
8	1.0	1.1	0	1	0	0	0
9	1.025	1.125	0	1	0	0	1
10	1.050	1.150	0	1	0	1	0
11	1.075	1.175	0	1	0	1	1
12	1.1	1.2	0	1	1	0	0
13	1.125	1.225	0	1	1	0	1
14	1.150	1.25	0	1	1	1	0
15	1.175	1.275	0	1	1	1	1
16	1.2	1.3	1	0	0	0	0
17	1.225	1.325	1	0	0	0	1
18	1.25	1.350	1	0	0	1	0
19	1.275	1.375	1	0	0	1	1
20	1.3	1.4	1	0	1	0	0
21	1.325	1.425	1	0	1	0	1
22	1.350	1.450	1	0	1	1	0
23	1.375	1.475	1	0	1	1	1
24	1.4	1.5	1	1	0	0	0
25	1.425	1.525	1	1	0	0	1
26	1.450	1.55	1	1	0	1	0
27	1.475	1.575	1	1	0	1	1
28	1.5	1.6	1	1	1	0	0
29	1.525	1.7	1	1	1	0	1
30	1.55	1.8	1	1	1	1	0
31	1.575	1.9	1	1	1	1	1

**表 8-4. Selectable Output Voltages for Converter 2,
 (ADJ2 Connected to V_{OUT2})**

	OUTPUT VOLTAGE [V] FOR REGISTER REG_DEF_2	D4	D3	D2	D1	D0
0	0.6	0	0	0	0	0
1	0.85	0	0	0	0	1
2	0.9	0	0	0	1	0
3	0.95	0	0	0	1	1
4	1	0	0	1	0	0
5	1.05	0	0	1	0	1
6	1.1	0	0	1	1	0
7	1.15	0	0	1	1	1
8	1.2	0	1	0	0	0
9	1.25	0	1	0	0	1
10	1.3	0	1	0	1	0
11	1.35	0	1	0	1	1
12	1.4	0	1	1	0	0
13	1.45	0	1	1	0	1
14	1.5	0	1	1	1	0
15	1.55	0	1	1	1	1
16	1.6	1	0	0	0	0
17	1.7	1	0	0	0	1
18	1.8	1	0	0	1	0
19	1.85	1	0	0	1	1
20	2	1	0	1	0	0
21	2.1	1	0	1	0	1
22	2.2	1	0	1	1	0
23	2.3	1	0	1	1	1
24	2.4	1	1	0	0	0
25	2.5	1	1	0	0	1
26	2.6	1	1	0	1	0
27	2.7	1	1	0	1	1
28	2.8	1	1	1	0	0
29	2.85	1	1	1	0	1
30	3	1	1	1	1	0
31	3.3	1	1	1	1	1

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.1.1 Application Information

The TPS624xx-Q1 family of devices are synchronous dual step-down DC-DC converters. The devices provide two independent output voltage rails. The following information provides guidance on selecting external components to complete the application design.

9.2 Typical Application

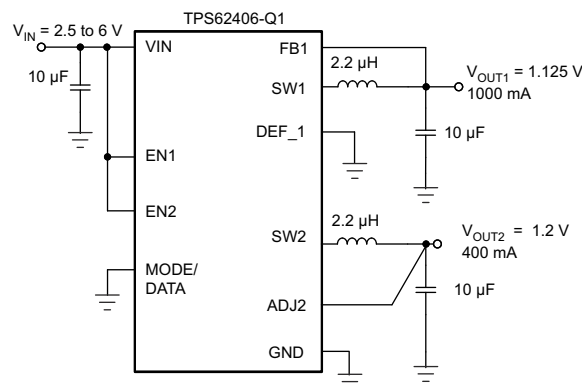


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs. The following design procedure is adequate for whole V_{IN} , V_{OUTx} and load current range of the TPS624xx-Q1 family of devices.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

9.2.2.1.1 Converter 1 Fixed Default Output-Voltage Setting

The DEF_1 pin selects output voltage V_{OUT1} .

Pin DEF_1 = low:

- TPS62406-Q1, TPS62407-Q1 = 1.125 V
- TPS62422-Q1 = 1.15V
- TPS62423-Q1 = 1.2V
- TPS62424-Q1 = 1.1V

Pin DEF_1 = high:

- TPS62406-Q1 = 1.125 V
- TPS62407-Q1 = 1.225 V
- TPS62422-Q1 = 1.8V
- TPS62423-Q1 = 1.5V
- TPS62424-Q1 = 1.3V

9.2.2.1.2 Converter 2 Fixed Default Output-Voltage Setting

ADJ2 pin must be directly connected with V_{OUT2} :

- TPS62406-Q1, V_{OUT2} default = 1.2 V
- TPS62407-Q1, V_{OUT2} default = 1.85 V
- TPS62422-Q1, V_{OUT2} default = 1.2 V
- TPS62423-Q1, V_{OUT2} default = 1.8 V
- TPS62424-Q1, V_{OUT2} default = 1.8 V

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The converters operate with a minimum inductance of 1.75 μ H and minimum capacitance of 6 μ F. The device operation is optimum with inductors of 2.2 μ H to 4.7 μ H and output capacitors of 10 μ F to 22 μ F.

9.2.2.2.1 Inductor Selection

Select the inductor based on its ratings for dc resistance and saturation current. The dc resistance of the inductor directly influences the efficiency of the converter. Therefore, select an inductor with lowest dc resistance for highest efficiency.

式 4 calculates the maximum inductor current under static load conditions. The saturation-current rating of the inductor should be higher than the maximum inductor current as calculated with 式 5. TI makes this recommendation because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \quad (4)$$

where

- ΔI_L = Peak-to-peak inductor ripple current
- L = Inductor value
- f = Switching frequency (2.25 MHz typical)

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (5)$$

where

- I_{Lmax} = Maximum inductor current
and the highest inductor current occurs at maximum V_{IN} .

Open-core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Take into consideration that the core material from inductor to inductor differs, and this difference has an impact on the efficiency.

See 表 9-1 and the typical application circuit examples for possible inductors.

表 9-1. List of Inductors

DIMENSIONS [mm]	INDUCTOR TYPE	SUPPLIER
3.2 × 2.6 × 1	MIPW3226	FDK
3 × 3 × 0.9	LPS3010	Coilcraft
2.8 × 2.6 × 1	VLF3010	TDK
2.8 × 2.6 × 1.4	VLF3014	TDK
3 × 3 × 1.4	LPS3015	Coilcraft

表 9-1. List of Inductors (continued)

DIMENSIONS [mm]	INDUCTOR TYPE	SUPPLIER
3.9 × 3.9 × 1.7	LPS4018	Coilcraft

9.2.2.2.2 Output-Capacitor Selection

The advanced fast-response voltage-mode control scheme of the converters allows the use of tiny ceramic capacitors with a typical value of 10 μF to 22 μF, without having large output-voltage under- and overshoots during heavy load transients. Ceramic capacitors with low ESR values result in lowest output-voltage ripple, and TI therefore recommends them. The output capacitor requires either X7R or X5R dielectric. TI does not recommend Y5V and Z5U dielectric capacitors because of their wide variation in capacitance.

If using ceramic output capacitors, the capacitor rms ripple-current rating always meets the application requirements. The rms ripple current calculation is:

$$I_{\text{RMS}C_{\text{out}}} = V_{\text{out}} \times \frac{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (6)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR, plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{\text{out}} = V_{\text{out}} \times \frac{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}{L \times f} \times \left(\frac{1}{8 \times C_{\text{out}} \times f} + \text{ESR} \right) \quad (7)$$

where

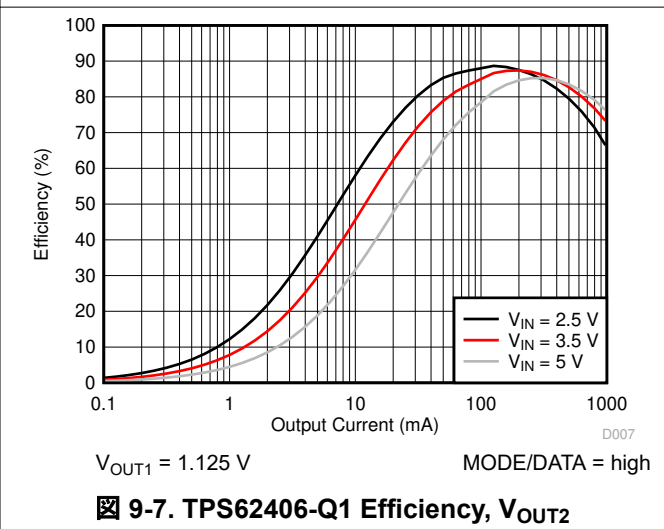
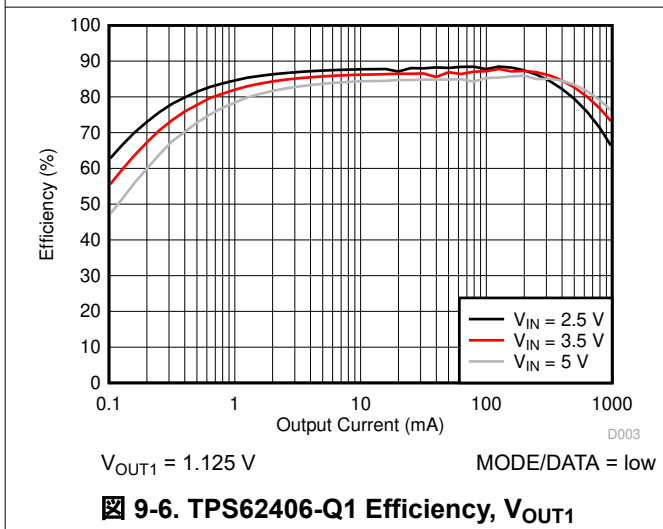
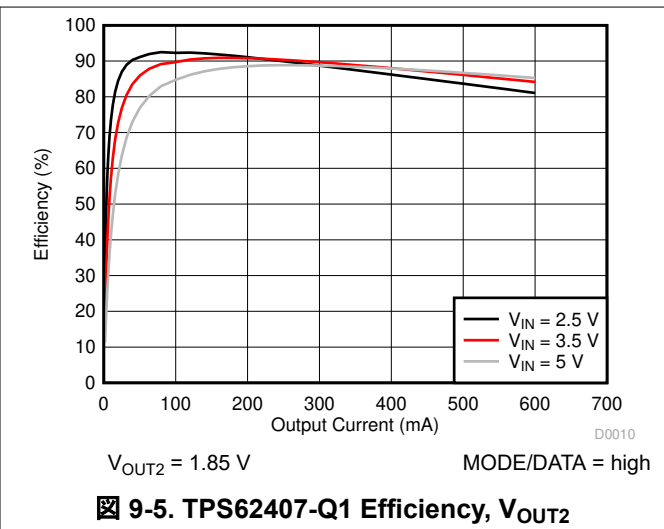
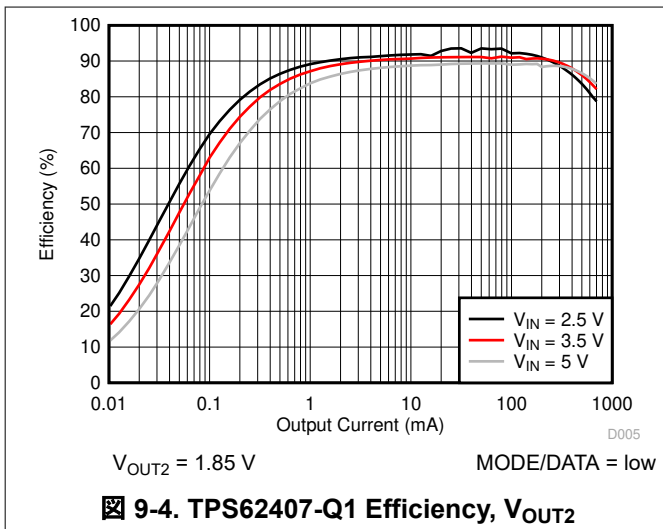
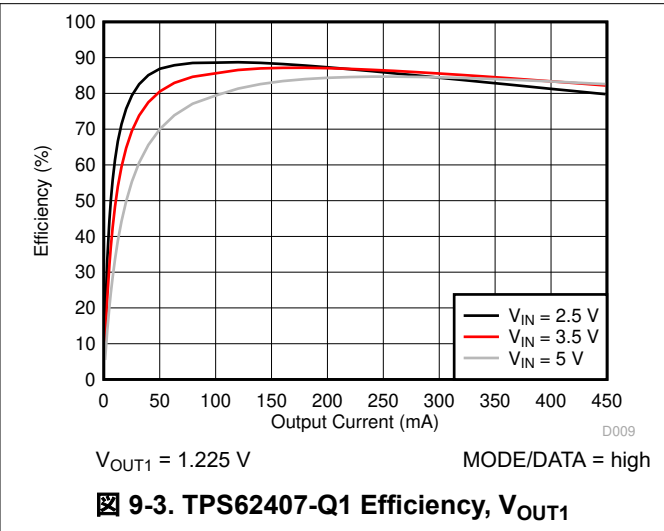
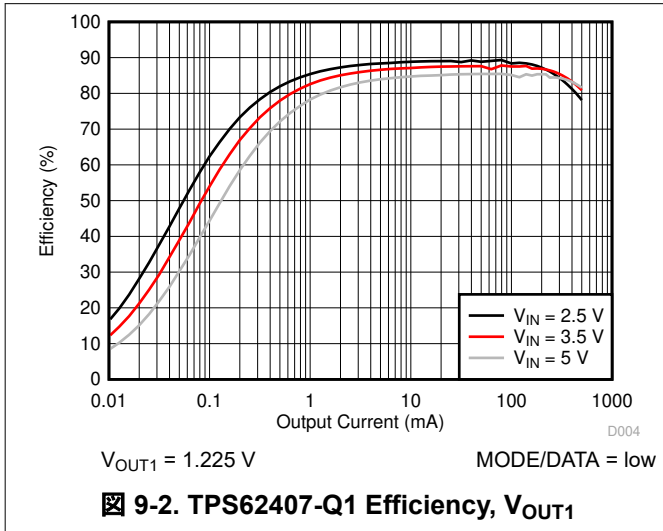
- The highest output-voltage ripple occurs at the highest input voltage, V_{IN} .

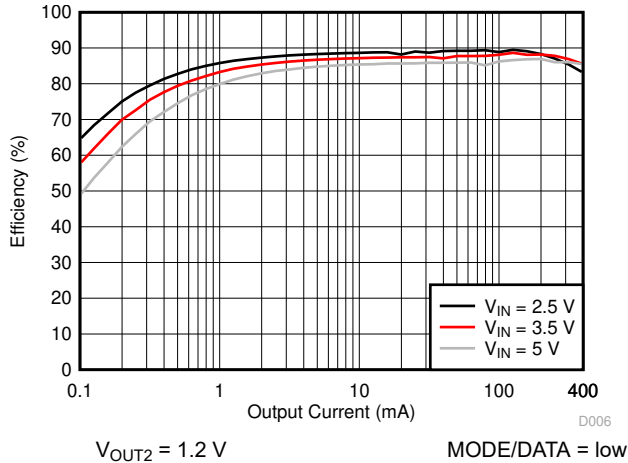
At light load currents, the converters operate in power-save mode and the output-voltage ripple depends on the output-capacitor value. The internal comparator delay and the external capacitor set the output-voltage ripple. Higher output capacitors like 22 μF values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

9.2.2.2.3 Input Capacitor Selection

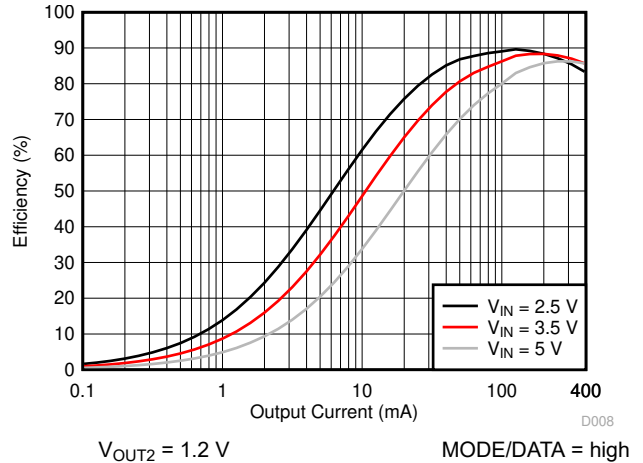
Because of the nature of the buck converter having a pulsating input current, the device requires a low-ESR input capacitor to prevent large voltage transients that can cause misbehavior of the device or interference with other circuits in the system. An input capacitor of 10 μF is sufficient.

9.2.3 Application Curves

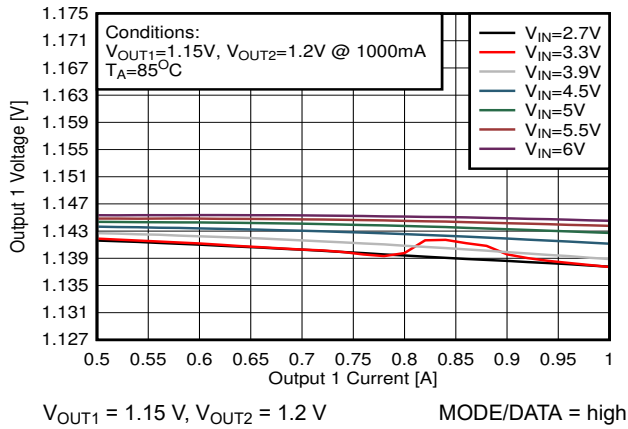




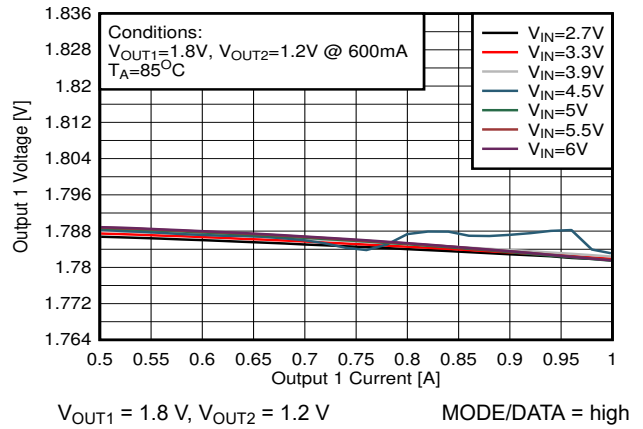
9-8. TPS62406-Q1 Efficiency, V_{OUT2}



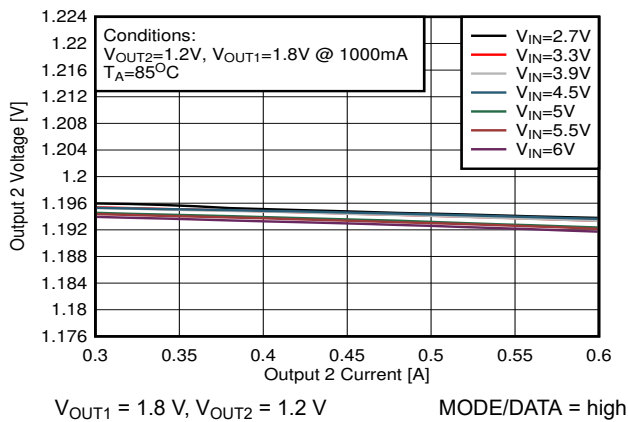
9-9. TPS62406-Q1 Efficiency, V_{OUT2}



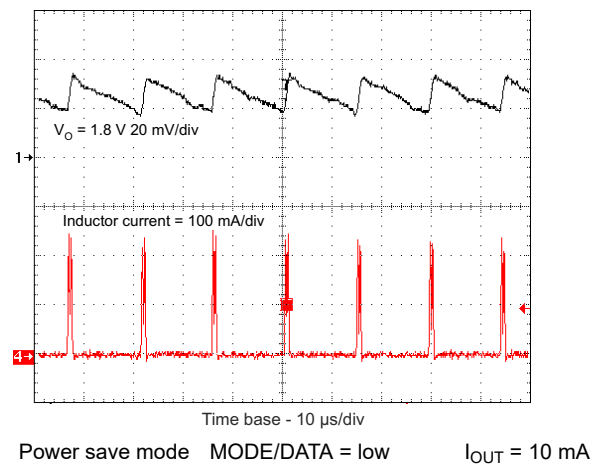
9-10. TPS62422-Q1 V_{OUT1} vs. I_{OUT1}



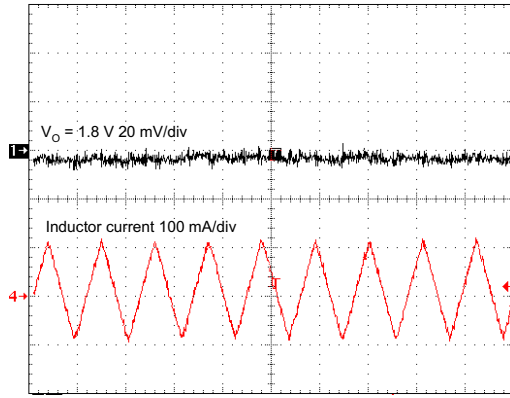
9-11. TPS62422-Q1 V_{OUT1} vs. I_{OUT1}



9-12. TPS62422-Q1 V_{OUT2} vs. I_{OUT2}

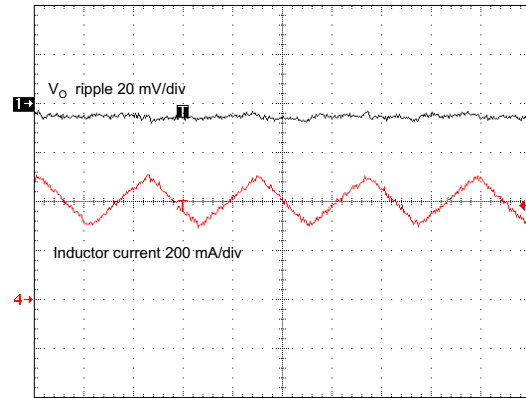


9-13. Light-Load Output-Voltage Ripple in Power-Save Mode



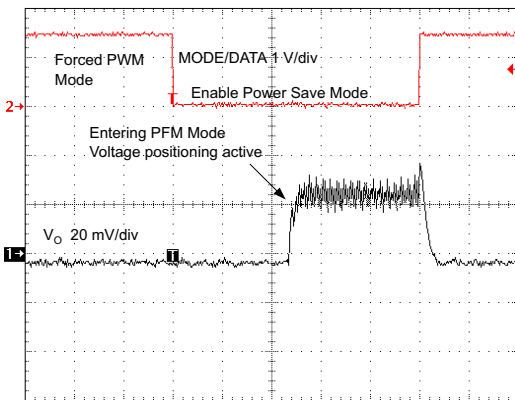
Time base - 400 ns/div
Forced PWM mode MODE/DATA = high $I_{OUT} = 10\text{ mA}$

9-14. Output-Voltage Ripple in Forced-PWM Mode



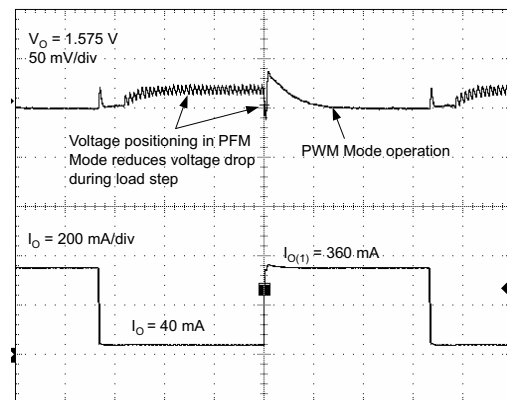
Time base - 200 ns/div
PWM mode $V_{OUT} = 1.8\text{ V}$ $I_{OUT} = 400\text{ mA}$

9-15. Output-Voltage Ripple in PWM Mode



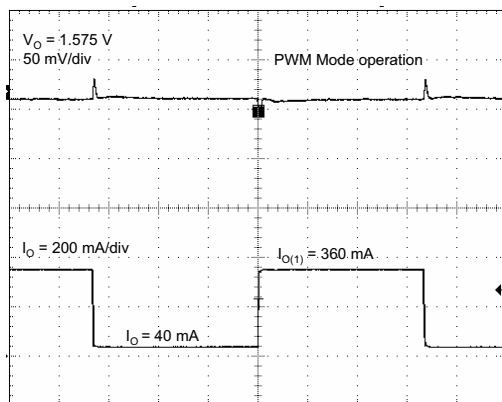
Time base - 200 μs/div
 $V_{OUT} = 1.8\text{ V}$ $I_{OUT} = 20\text{ mA}$

9-16. Forced PWM-to-PFM Mode Transition



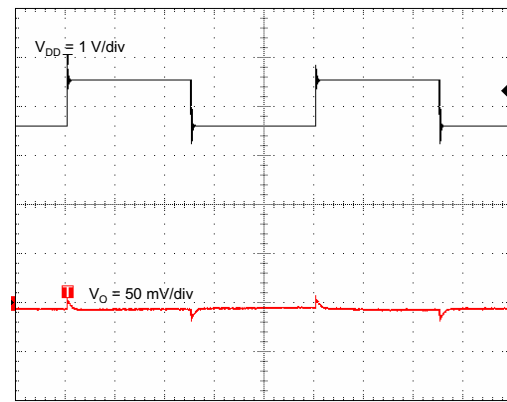
Time base - 50 μs/div
MODE/DATA = low

9-17. Load-Transient Response, PFM-to-PWM



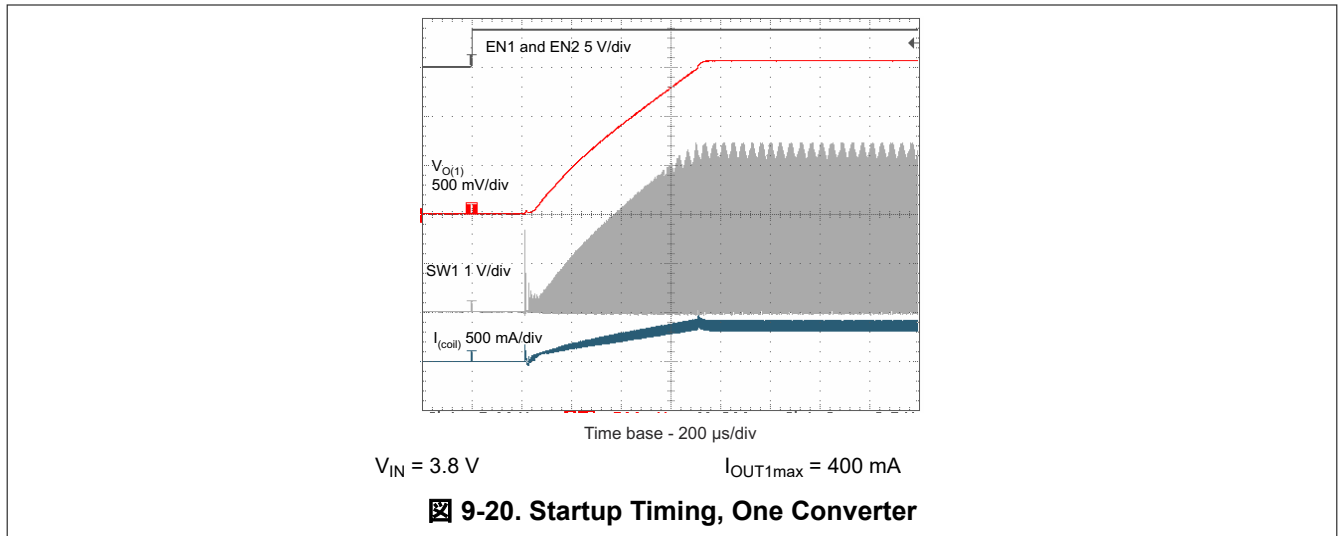
Time base - 50 μs/div
PWM mode MODE/DATA = high

9-18. Load-Transient Response, PWM Operation

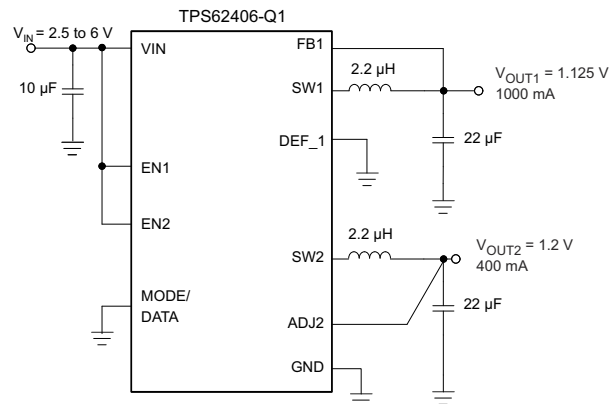


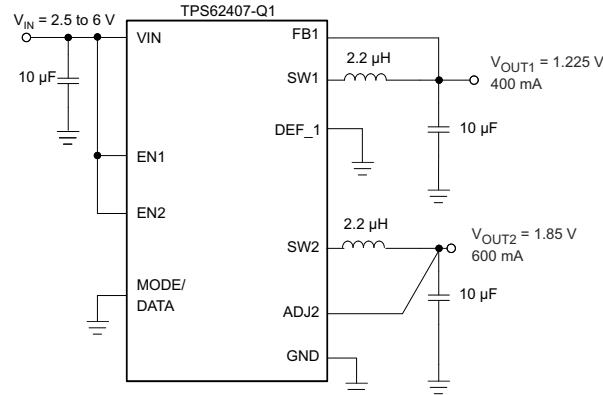
Time base - 400 μs/div
MODE/DATA = low $V_{IN} = 3.6\text{ to }4.6\text{ V}$ $V_{OUT1} = 1.575\text{ V}$
 $I_{OUT1} = 200\text{ mA}$

9-19. Line-Transient Response

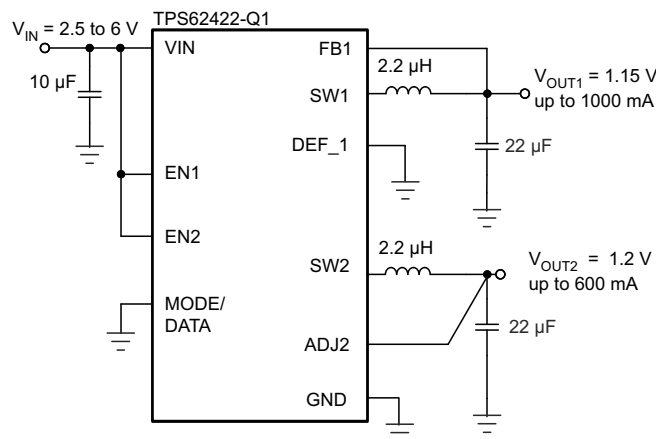


9.3 System Examples

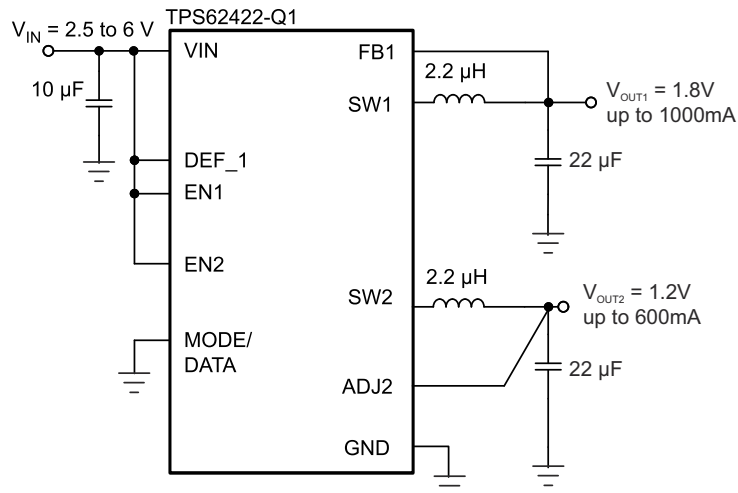




9-22. TPS62407-Q1 Fixed 1.225-V and 1.85-V Outputs



9-23. TPS62422-Q1 Fixed 1.15-V and 1.2-V Outputs



9-24. TPS62422-Q1 Fixed 1.8-V and 1.2-V Outputs

10 Power Supply Recommendations

This device has no special recommendation for the power supply. TI recommends to use the values listed in the [セクション 7.3](#) table.

11 Layout

11.1 Layout Guidelines

- As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout.
- It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the main current paths as indicated in bold in [Figure 11-1](#).
- Place the input capacitor as close as possible to the IC pins VIN and GND, the inductor and output capacitor as close as possible to the pins SW1 and GND.
- Connect the GND pin of the device to the PowerPAD of the PCB and use this pad as a star point. For each converter, use a common power GND node and a different node for the signal GND to minimize the effects of ground noise.
- Connect these ground nodes together to the PowerPAD (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors, as short as possible to avoid ground noise.
- Connect the output voltage-sense lines (FB 1, DEF_1, ADJ2) right to the output capacitor and route them away from noisy components and traces (for example, the SW1 and SW2 lines).
- If operating the EasyScale interface with high transmission rates, route the MODE/DATA trace away from the ADJ2 line to avoid capacitive coupling into the ADJ2 pin.
- A GND guard ring between the MODE/DATA pin and ADJ2 pin avoids potential noise coupling.

11.2 Layout Example

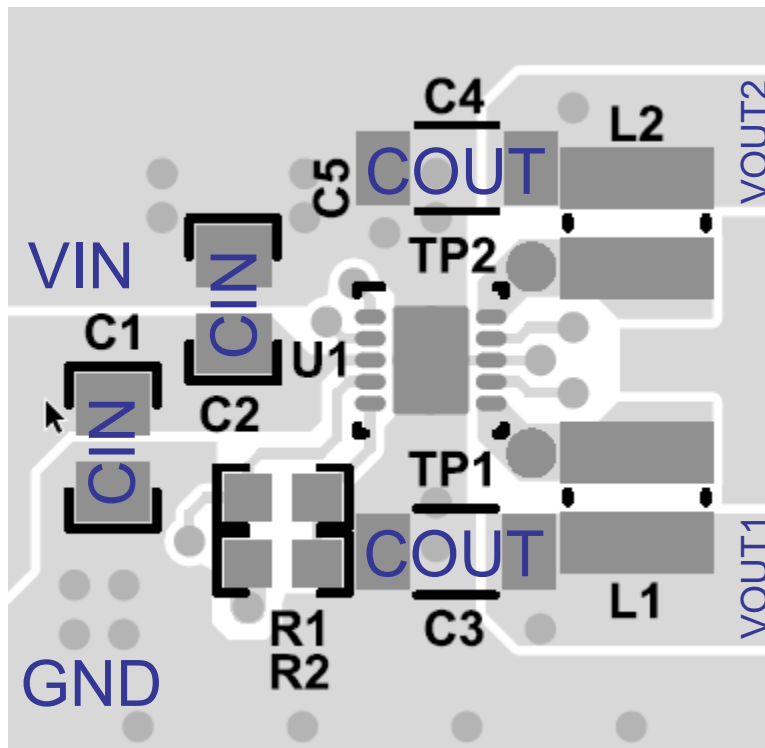


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 サポート・リソース

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62406QDRCRQ1	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2406Q
TPS62406QDRCRQ1.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2406Q
TPS62407QDRCRQ1	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SHU
TPS62407QDRCRQ1.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	SHU
TPS62422QDRCRQ1	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2422Q
TPS62422QDRCRQ1.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2422Q
TPS62423QDRCRQ1	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2423Q
TPS62423QDRCRQ1.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2423Q
TPS62424QDRCRQ1	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2424Q
TPS62424QDRCRQ1.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2424Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62406QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62407QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62422QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62423QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62424QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62406QDRCRQ1	VSON	DRC	10	3000	346.0	346.0	33.0
TPS62407QDRCRQ1	VSON	DRC	10	3000	346.0	346.0	33.0
TPS62422QDRCRQ1	VSON	DRC	10	3000	338.0	355.0	35.0
TPS62423QDRCRQ1	VSON	DRC	10	3000	338.0	355.0	35.0
TPS62424QDRCRQ1	VSON	DRC	10	3000	338.0	355.0	35.0

GENERIC PACKAGE VIEW

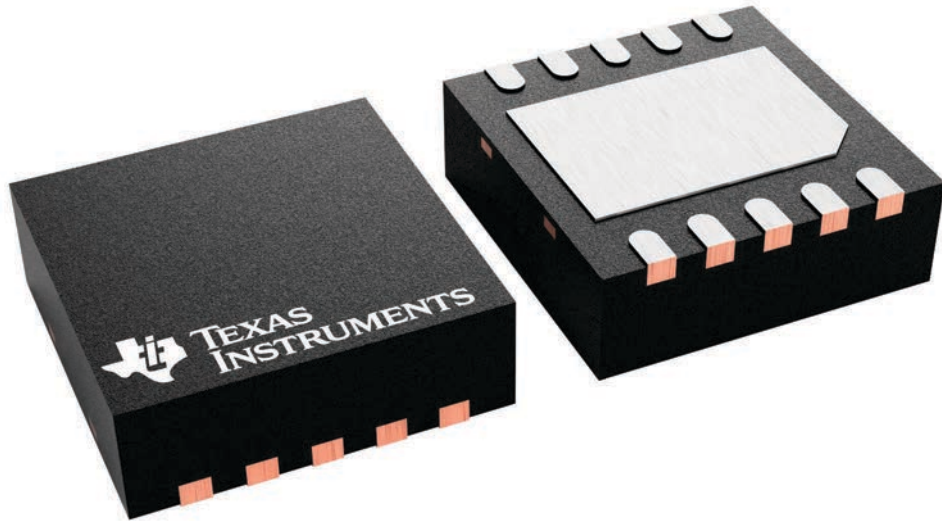
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



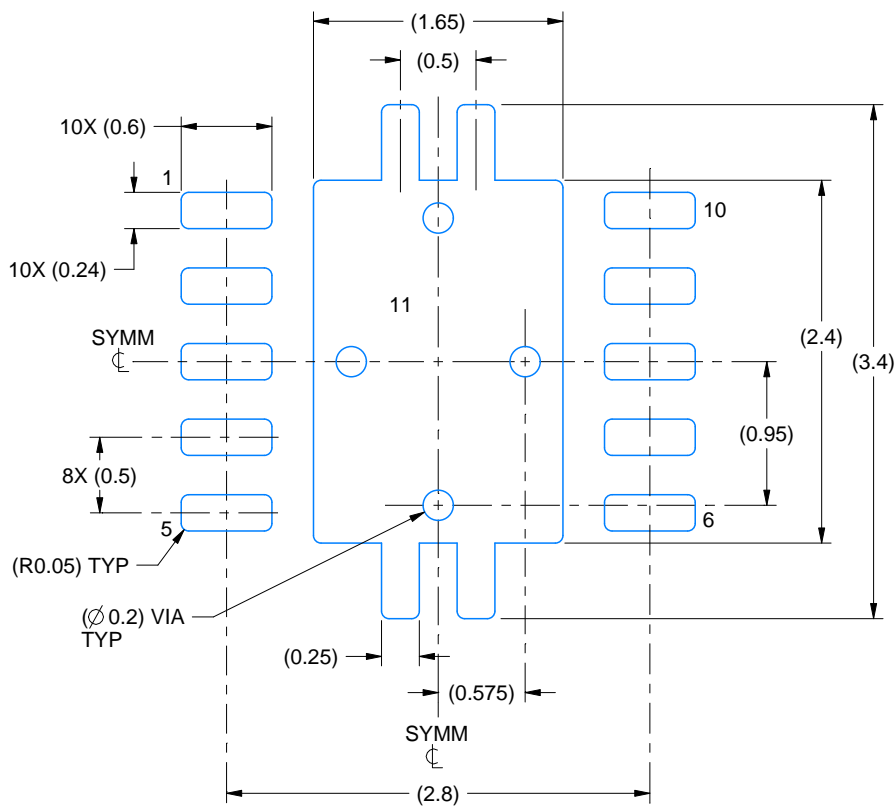
4226193/A

EXAMPLE BOARD LAYOUT

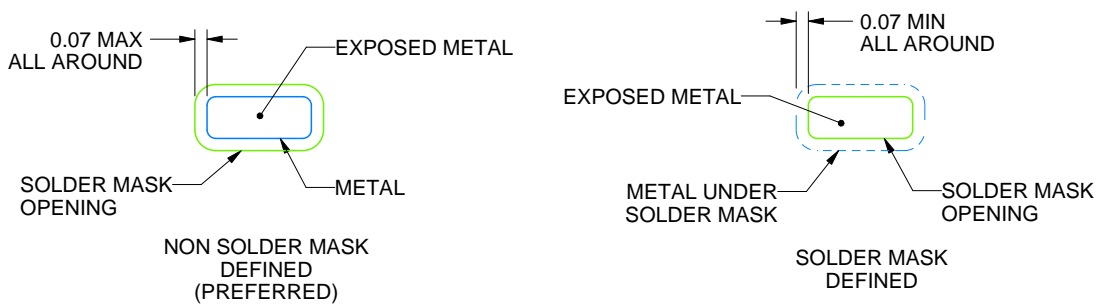
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

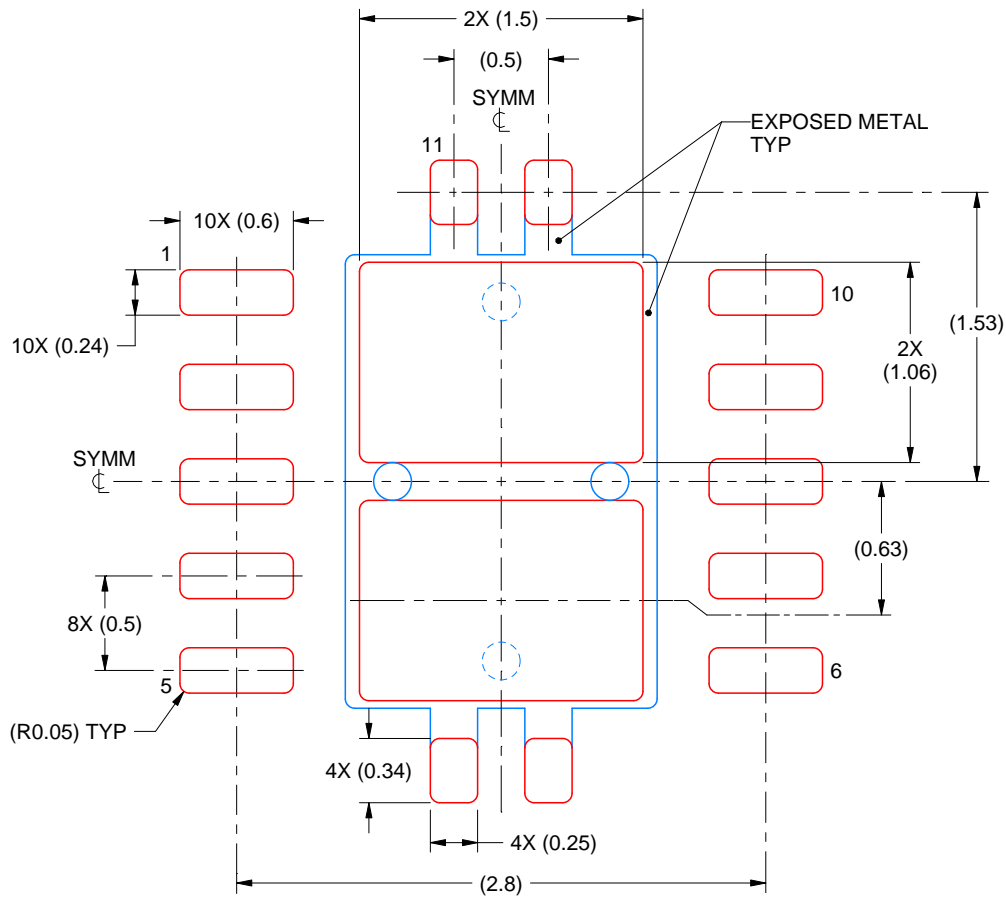
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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