ADS123x、2 および 4 チャネル、24 ビット、デルタ・シグマ ADC、ブリッジ・センサ用

1 特長

- ブリッジ センサ用の包括的なフロントエンド
- ゲイン= 1 で 23.5 ビットの実効分解能
- ゲイン= 64 で 19.2 ビットのノイズフリー分解能
- 低ノイズ PGA
- 1、2、64、128 のゲインを選択可能
- RMS ノイズ:
  - ゲイン 128、10SPS 動作時のノイズは 17nV
  - ゲイン 128、80SPS 動作時のノイズは 44nV
- 50Hz と 60Hz を同時に除去時に 100dB
- 柔軟性の高いクロッキング:
  - 高精度内部発振回路
  - 外付け水晶振動子 (オプション)
- 10SPS または 80SPS のデータ レートを選択可能
- 容易なレシオメトリック測定:
  - 広い入力電圧範囲 (最大 5V)
- 2 チャネル差動入力、温度センサ内蔵 (ADS1232)
- 4 チャネル差動入力 (ADS1234)
- 2 線式シリアル インターフェイス
- 電源電圧範囲:2.7V ～ 5.3V
- 温度範囲:-40℃ ～ +105℃
- パッケージ:TSSOP-24 (ADS1232) または TSSOP-28 (ADS1234)

2 アプリケーション

- 計量器
- PLC 重量計モジュール
- 圧力センサ

3 説明

ADS1232 および ADS1234 (ADS123x) は、高精度の 24 ビット A/D コンバータ (ADC) です。低ノイズのプログラマブル ゲイン アンプ (PGA)、高精度デルタ シグマ ADC、内部発振器を搭載しています。ADS123x は、重量計、歪みゲージ、圧力センサなどのブリッジ センサ アプリケーション用の包括的なフロント エンド ソリューションを提供します。

入力マルチプレクサ (MUX) は、2 つ (ADS1232) または 4 つ (ADS1234) の差動入力を受け入れます。ADS1232 には、周囲温度を監視する温度センサも搭載されています。低ノイズ PGA は、1、2、64、128 のゲインを選択でき、±2.5V、±1.25V、±39mV、±19.5mV のフルスケール差動入力をサポートします。

デルタ シグマ ADC は、最大 23.5 ビットの有効分解能を実現し、次の 2 つのデータ レートをサポートします。10SPS (50Hz および 60Hz 除去) および 80SPS。ADS123x は、発振器または水晶振動子、または内部発振器を使用して、外部からクロックを供給できます。

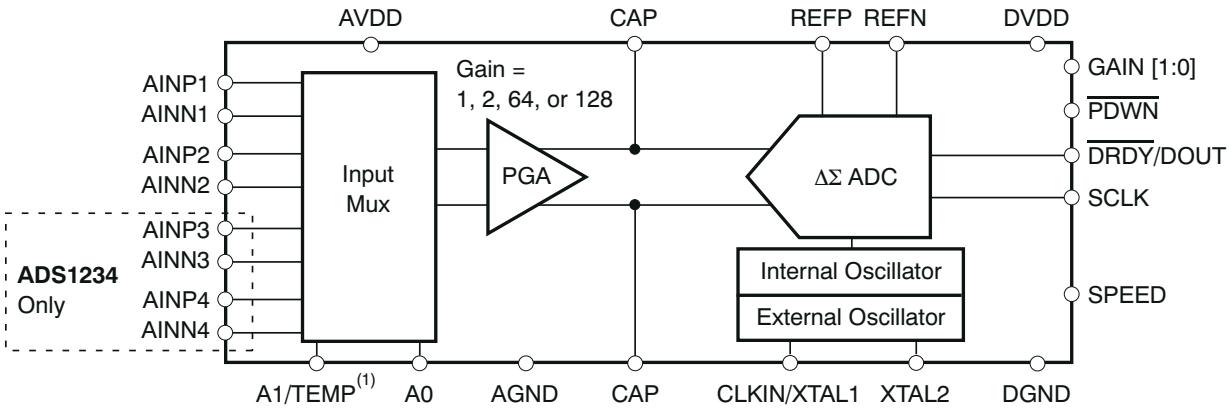
オフセット キャリブレーションは、オンデマンドで実行され、ADS123x は、低消費電力のスタンバイ モードにするか、電源オフ モードで完全にシャットオフすることができます。ADS123x は、シンプルなピン駆動制御で動作します。プログラムするためのデジタル レジスタはありません。

データは 2 線式のシリアル インターフェイスを経由して出力され、MSP430 や他のマイクロコントローラに直接接続できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ADS1232	PW (TSSOP、24)	7.8mm × 6.4mm
ADS1234	PW (TSSOP、28)	9.7mm × 6.4mm

(1) 詳細については、*メカニカル、パッケージ、および注文情報*をご覧ください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンを含みます。



NOTE: (1) A1 for ADS1234, TEMP for ADS1232.

ブロック図

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4 Pin Configuration and Functions

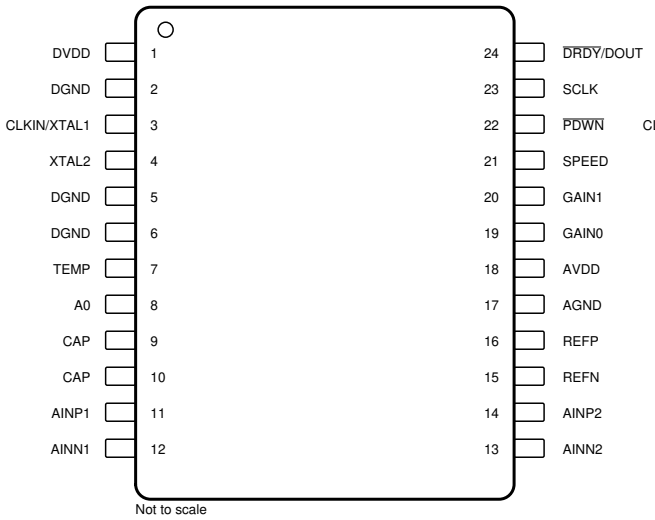


図 4-1. ADS1232 PW Package, 24-Pin TSSOP (Top View)

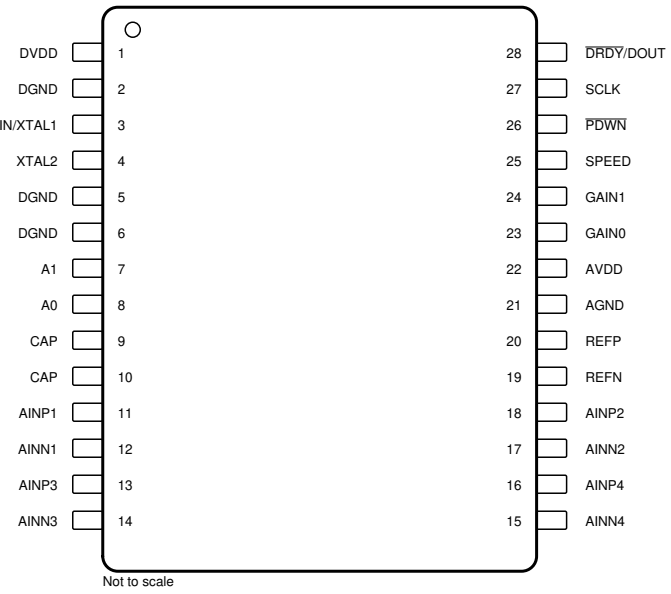


図 4-2. ADS1234 PW Package, 28-Pin TSSOP (Top View)

表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	ADS1232	ADS1234		
A0	8	8	Digital input	Input MUX select pins. See 表 7-1 and 表 7-2 for more information.
A1	—	7	Digital input	Input MUX select pins. See 表 7-1 and 表 7-2 for more information.
AGND	17	21	Analog	Analog ground
AINN1	12	12	Analog input	Negative analog input channel 1
AINN2	13	17	Analog input	Negative analog input channel 2
AINN3	—	14	Analog input	Negative analog input channel 3
AINN4	—	15	Analog input	Negative analog input channel 4
AINP1	11	11	Analog input	Positive analog input channel 1
AINP2	14	18	Analog input	Positive analog input channel 2
AINP3	—	13	Analog input	Positive analog input channel 3
AINP4	—	16	Analog input	Positive analog input channel 4
AVDD	18	22	Analog	Analog power supply: 2.7V to 5.3V
CAP	9, 10	9, 10	Analog	PGA bypass, connect a 0.1µF capacitor across pins 9 and 10
CLKIN/XTAL1	3	3	Digital input	External crystal connection 1, or external clock input, or tie low to activate internal oscillator. See the *Clock Sources* section for more information.
DGND	2, 5, 6	2, 5, 6	Digital	Digital ground
$\overline{\text{DRDY}}$/DOUT	24	28	Digital output	Dual-purpose output: *Data ready* indicates valid data by going low. *Data output* outputs data, MSB first, on the first rising edge of SCLK.
DVDD	1	1	Digital	Digital power supply: 2.7V to 5.3V
GAIN0	19	23	Digital input	Gain select pins. See the *Low-Noise PGA* section for more information.
GAIN1	20	24	Digital input	Gain select pins. See the *Low-Noise PGA* section for more information.
REFN	15	19	Analog input	Negative reference input
REFP	16	20	Analog input	Positive reference input
$\overline{\text{PDWN}}$	22	26	Digital input	Power-down: hold this pin low to power down and reset the ADC. Toggle the pin at device power-up. See the *Power-Up Sequence* section for more information.

表 4-1. Pin Functions (続き)

PIN			TYPE	DESCRIPTION
NAME	ADS1232	ADS1234		
SCLK	23	27	Digital input	Serial clock: clock out data on the rising edge. Also used to initiate offset calibration and standby modes. See the *Offset Calibration Mode* and *Standby Mode With Offset-Calibration* sections for more information.
SPEED	21	25	Digital input	Data rate select. See the *Data Rate* section for more information.
TEMP	7	—	Digital input	Temperature sensor select. See 表 7-1 for more information.
XTAL2	4	4	Digital	External crystal connection 2

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	6	V
	DVDD to DGND	–0.3	6	
	AGND to DGND	–0.3	0.3	
Analog input voltage	AINNx, AINPx, REFP, REFN	AGND – 0.3	AVDD + 0.3	V
Digital input voltage	A0, A1, CLKIN/XTAL1, XTAL2, $\overline{\text{DRDY}}$/DOUT, GAIN0, GAIN1, $\overline{\text{PWDN}}$, SCLK, SPEED	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, all pins except power-supply pins(2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input and output pins are diode-clamped to the internal power supplies. Limit the input current to 10mA in the event the analog input voltage exceeds AVDD + 0.3V or AGND – 0.3V, or if the digital input voltage exceeds DVDD + 0.3V or DGND – 0.3V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±750	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AGND	2.7		5.3	V
	Digital power supply	DVDD to DGND	2.7		5.3	V
ANALOG INPUTS						
	Full-scale input voltage	$V_{(AINPx)} – V_{(AINNx)}$	±0.5 V_{REF} / Gain			V
	Common-mode input range	Gain = 1 and 2	AGND – 0.1		AVDD + 0.1	V
		Gain = 64 and 128	AGND + 1.5		AVDD – 1.5	
VOLTAGE REFERENCE INPUTS						
V_{REF}	Voltage reference input	$V_{REF} = V_{(REFP)} – V_{(REFN)}$	1.5	AVDD	AVDD + 0.1	V
$V_{(REFN)}$	Negative reference input		AGND – 0.1		$V_{(REFP)}$ – 1.5	V
$V_{(REFP)}$	Positive reference input		$V_{(REFN)}$ + 1.5		AVDD + 0.1	V
EXTERNAL CLOCK INPUT						
f_{CLK}	External clock frequency		0.2	4.9152	8	MHz
SERIAL INTERFACE CLOCK INPUT						
$f_{(SCLK)}$	Serial clock frequency				5	MHz
DIGITAL INPUTS						
	Input voltage		DGND		DVDD + 0.1	V
TEMPERATURE						
T_A	Operating ambient temperature		–40		105	°C

5.4 Thermal Information

THERMAL METRIC(1)		ADS1232	ADS1234	UNIT
		PW (TSSOP)	PW (TSSOP)	
		24 PINS	28 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	82.4	74.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	25.5	21.9	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	38.1	32.9	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	1.3	1.1	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	37.6	32.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +105°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = DVDD = $V_{(REFP)}$ = 5V, $V_{(REFN)}$ = AGND, and f_{CLK} = 4.9152MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input current	Gain = 1		±3		nA
		Gain = 2		±6		
		Gain = 64, 128		±3.5		
SYSTEM PERFORMANCE						
	Resolution	No missing codes	24			Bits
f_{DATA}	Data rate	Internal oscillator, SPEED = high	78	80	82.4	SPS
		Internal oscillator, SPEED = low	9.75	10	10.3	
		External oscillator, SPEED = high		f_{CLK} / 61,440		
		External oscillator, SPEED = low		f_{CLK} / 491,520		
	Digital filter settling time	Full settling, readings synchronized with A0, A1 pins		4		Conversions
INL	Integral nonlinearity	Differential input, end-point fit, gain = 1, 2	–0.001	±0.0002	0.001	% of FSR(1)
		Differential input, end-point fit, gain = 64, 128		±0.0004		
	Input offset error(2)	Gain = 1	–5	±0.2	5	ppm of FS
		Gain = 128	–1	±0.02	1	
	Input offset drift	Gain = 1		±0.3		µV/°C
		Gain = 128		±10		nV/°C
	Gain error(3)	Gain = 1	–0.02	±0.001	0.02	%
		Gain = 128	–0.1	±0.01	0.1	
	Gain drift	Gain = 1		±0.2		ppm/°C
		Gain = 128		±2.5		
NMRR	Normal-mode rejection ratio (4)	Internal oscillator, f_{DATA} = 10SPS f_{IN} = 50Hz or 60Hz, ±1Hz	100	110		dB
		External oscillator, f_{DATA} = 10SPS f_{IN} = 50Hz or 60Hz, ±1Hz	120	130		
CMRR	Common-mode rejection ratio	At DC, gain = 1, ΔV = 1V, V_{CM} = AVDD / 2	95	110		dB
		At DC, gain = 128, ΔV = 0.1V, V_{CM} = AVDD / 2	95	110		
e_n	Input-referred noise		See the *Noise Performance* section			
PSRR	Power-supply rejection	AVDD, at DC, gain = 1, ΔV = 1V		85		dB
		AVDD, at DC, gain = 128, ΔV = 0.1V	100	120		
VOLTAGE REFERENCE INPUT						
	Input current			10		nA
DIGITAL LOGIC LEVELS						
V_{IH}	High-level input voltage		0.7 DVDD			V
V_{IL}	Low-level input voltage				0.2 DVDD	V
V_{OH}	High-level output voltage	I_{OH} = 1mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA			0.2 DVDD	V
	Input leakage current	0V < V_{IN} < DVDD	–10		10	µA

5.5 Electrical Characteristics (続き)

minimum and maximum specifications apply from T_A = –40°C to +105°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = DVDD = $V_{(REFP)}$ = 5V, $V_{(REFN)}$ = AGND, and f_{CLK} = 4.9152MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$I_{(AVDD)}$	Analog supply current	Normal mode, AVDD = 3V, gain = 1, 2		600	1300	μA
		Normal mode, AVDD = 3V, gain = 64, 128		1350	2500	
		Normal mode, AVDD = 5V, gain = 1, 2		650	1300	
		Normal mode, AVDD = 5V, gain = 64, 128		1350	2500	
		Standby mode		0.1	1	
		Power-down		0.1	1	
$I_{(DVDD)}$	Digital supply current	Normal mode, DVDD = 3V, gain = 1, 2		60	95	μA
		Normal mode, DVDD = 3V, gain = 64, 128		75	120	
		Normal mode, DVDD = 5V, gain = 1, 2		95	130	
		Normal mode, DVDD = 5V, gain = 64, 128		75	120	
		Standby mode, SCLK = high, DVDD = 3V		45	80	
		Standby mode, SCLK = high, DVDD = 5V		65	80	
		Power-down		0.2	1.3	
P_D	Power dissipation, total	Normal mode, AVDD = DVDD = 3V, gain = 1, 2		2	4.2	mW
		Normal mode, AVDD = DVDD = 5V, gain = 1, 2		3.7	7.2	
		Normal mode, AVDD = DVDD = 3V, gain = 64, 128		4.3	7.9	
		Normal mode, AVDD = DVDD = 5V, gain = 64, 128		7.1	13.1	
		Standby mode, AVDD = DVDD = 5V		0.3	0.4	

(1) FSR = full-scale range = V_{REF} / Gain.
(2) Input offset error specified after calibration. Recalibration minimizes these errors to the level of noise at any temperature.
(3) Gain errors are calibrated at the factory (AVDD = 5V, all gains, T_A = 25°C).
(4) Specification is verified by the combination of design and final production test.

5.6 Typical Characteristics

at T_A = 25°C, AVDD = DVDD = $V_{(REFP)}$ = 5V, and $V_{(REFN)}$ = AGND (unless otherwise noted)

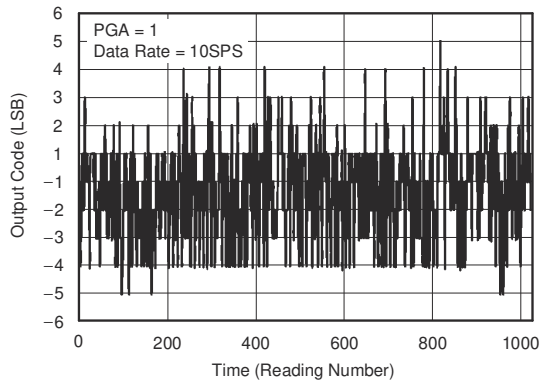


図 5-1. Noise Plot

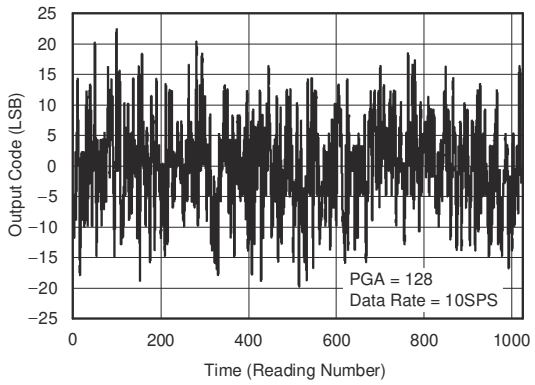


図 5-2. Noise Plot

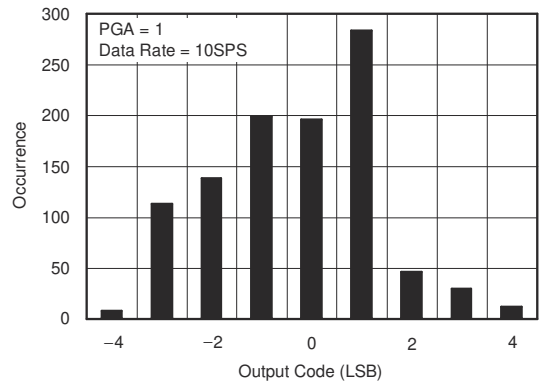


図 5-3. Noise Histogram

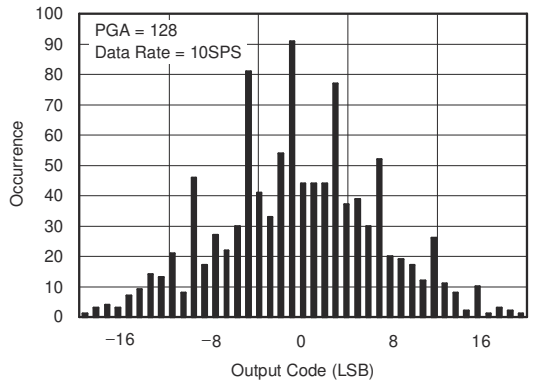


図 5-4. Noise Histogram

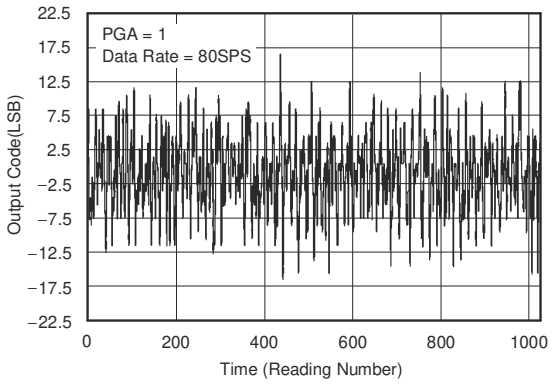


図 5-5. Noise Plot

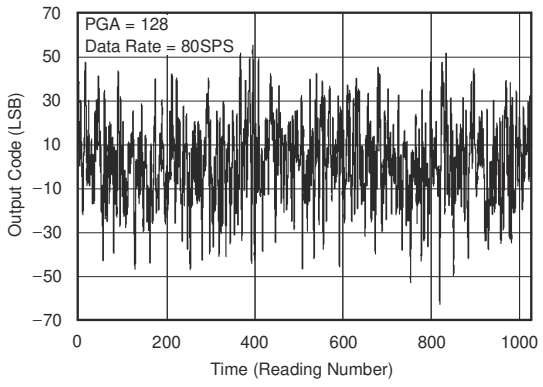


図 5-6. Noise Plot

5.6 Typical Characteristics (continued)

at T_A = 25°C, AVDD = DVDD = $V_{(REFP)}$ = 5V, and $V_{(REFN)}$ = AGND (unless otherwise noted)

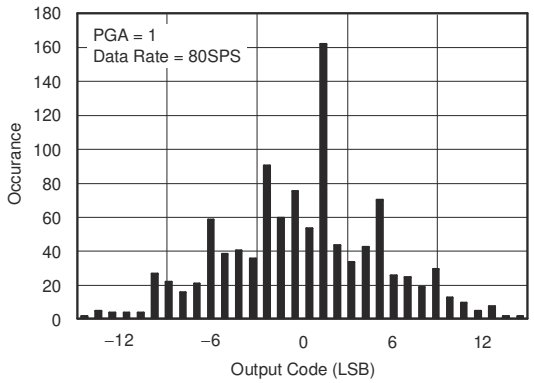


図 5-7. Noise Histogram

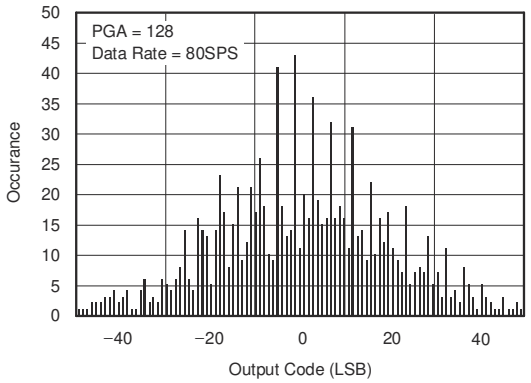


図 5-8. Noise Histogram

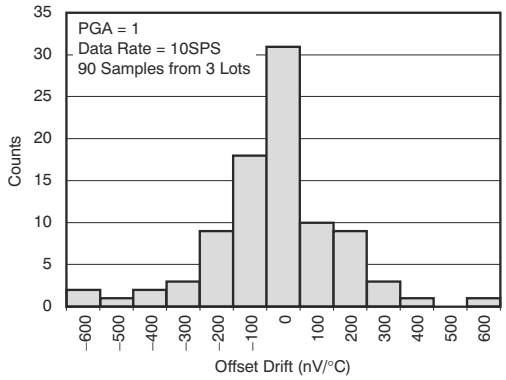


図 5-9. Offset Drift (–40°C to +25°C)

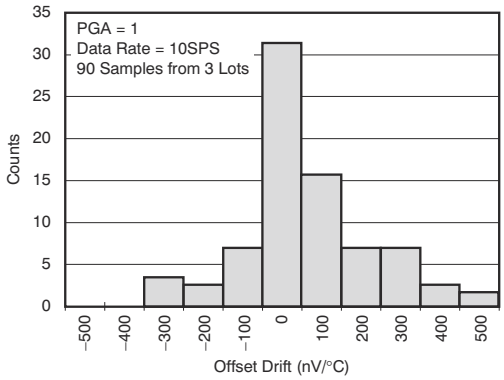


図 5-10. Offset Drift (25°C to 105°C)

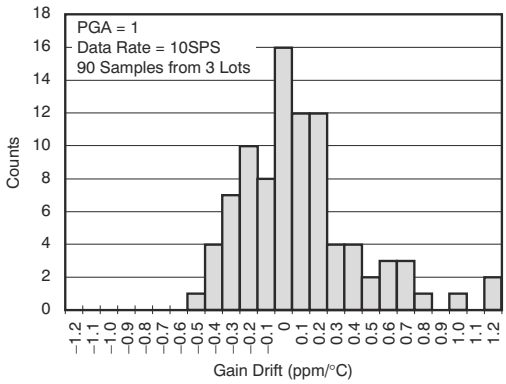


図 5-11. Gain Drift (–40°C to +25°C)

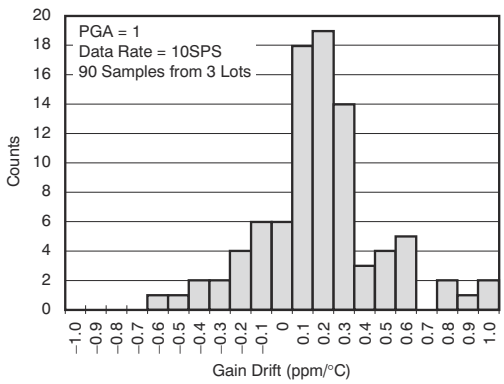


図 5-12. Gain Drift (25°C to 105°C)

5.6 Typical Characteristics (continued)

at T_A = 25°C, AVDD = DVDD = $V_{(REFP)}$ = 5V, and $V_{(REFN)}$ = AGND (unless otherwise noted)

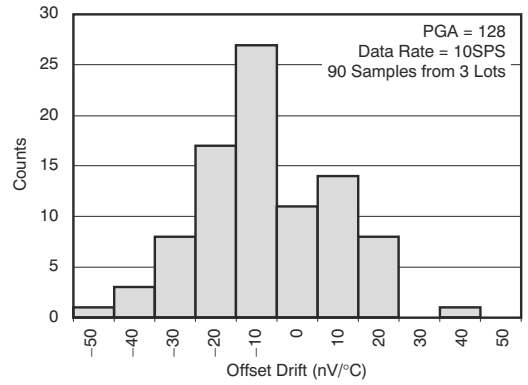


図 5-13. Offset Drift (–40°C to +25°C)

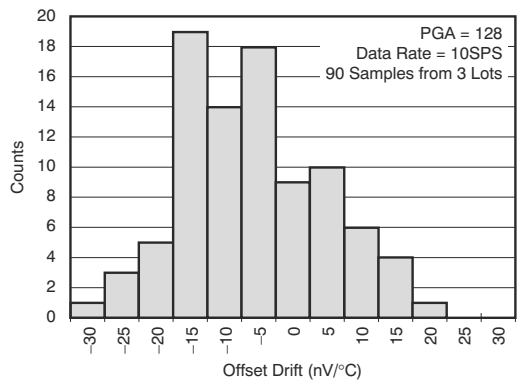


図 5-14. Offset Drift (25°C to 105°C)

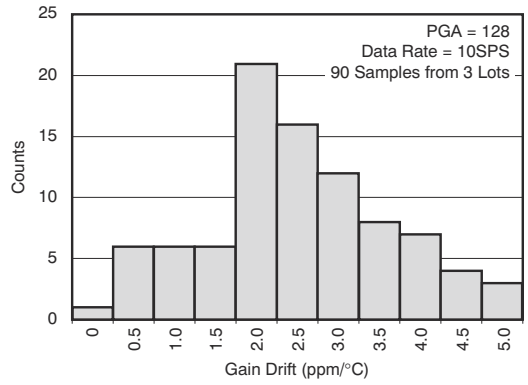


図 5-15. Gain Drift (–40°C to +25°C)

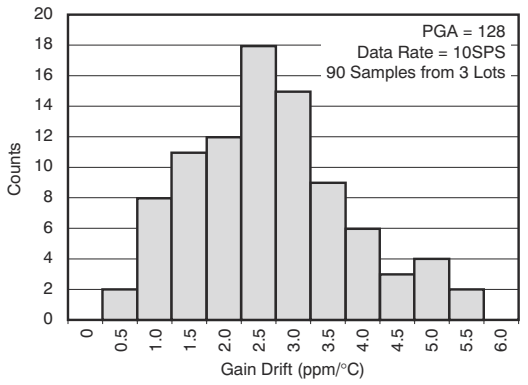


図 5-16. Gain Drift (25°C to 105°C)

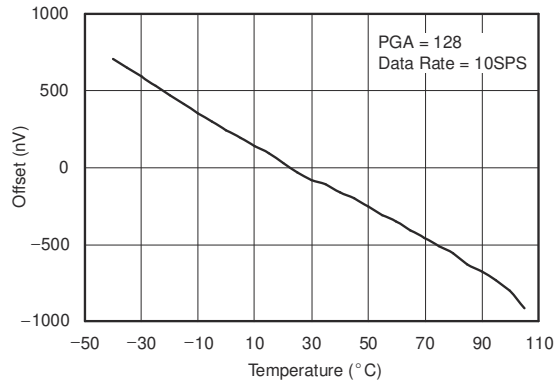


図 5-17. Offset vs Temperature

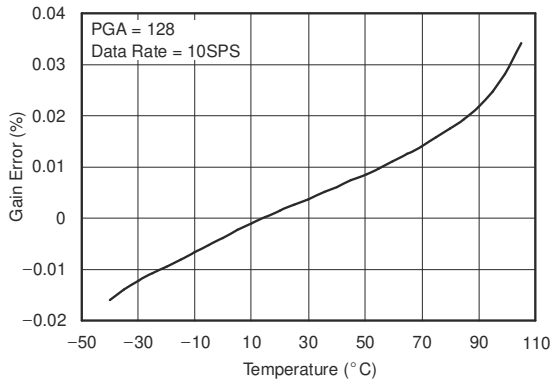


図 5-18. Gain Error vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C, AVDD = DVDD = $V_{(REFP)}$ = 5V, and $V_{(REFN)}$ = AGND (unless otherwise noted)

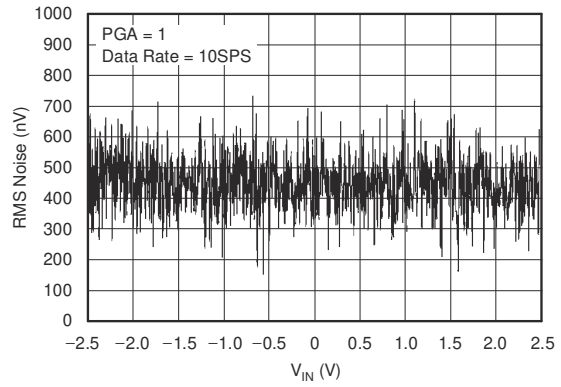


図 5-19. Noise vs Input Signal

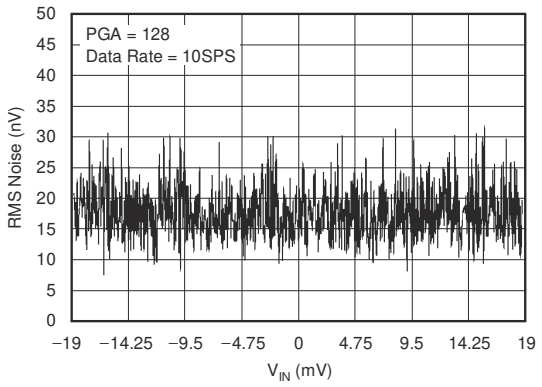


図 5-20. Noise vs Input Signal

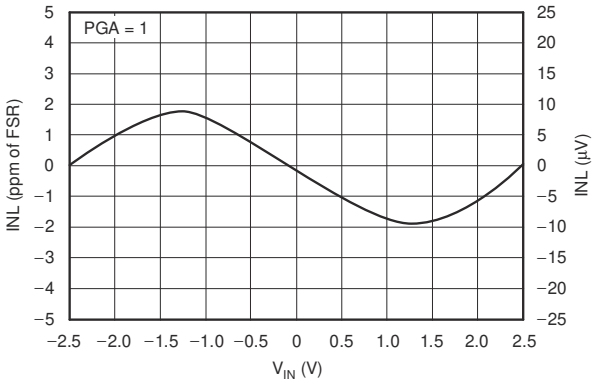


図 5-21. Integral Nonlinearity vs Input Signal

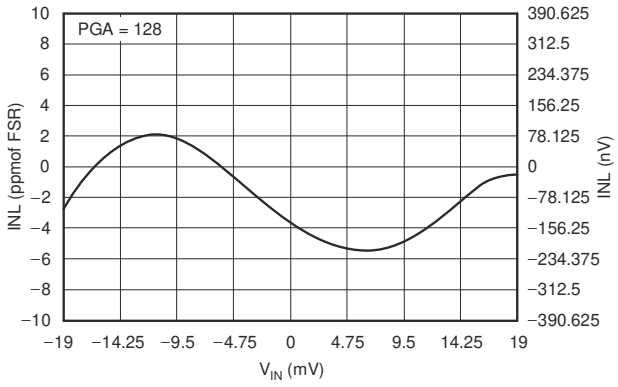


図 5-22. Integral Nonlinearity vs Input Signal

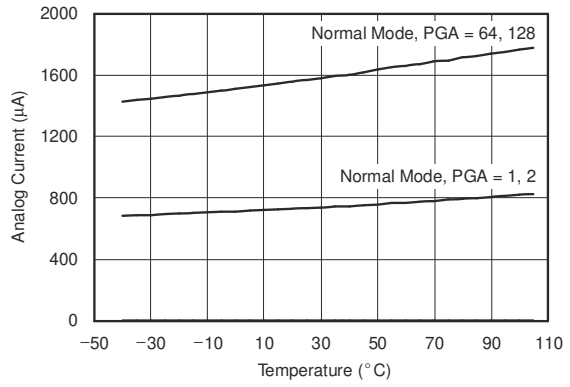


図 5-23. Analog Supply Current vs Temperature

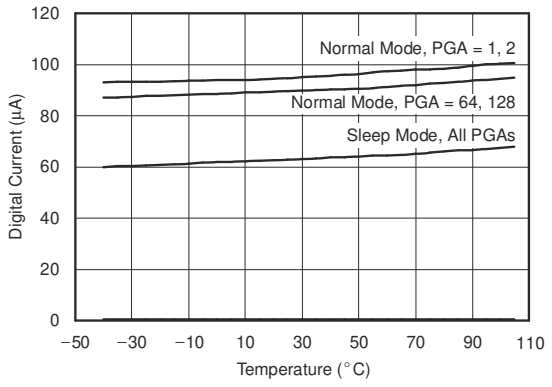


図 5-24. Digital Supply Current vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C, AVDD = DVDD = $V_{(REFP)}$ = 5V, and $V_{(REFN)}$ = AGND (unless otherwise noted)

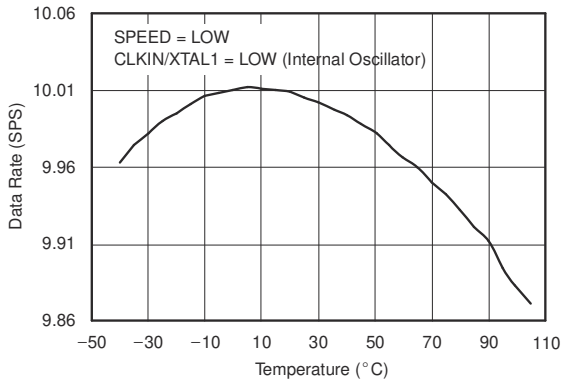


図 5-25. Data Rate vs Temperature

6 Parameter Measurement Information

6.1 Noise Performance

The ADS123x offer outstanding noise performance that can be optimized for a given full-scale range using the programmable gain amplifier (PGA). AVDD = 5V, V_{REF} = 5V, Data Rate = 10SPS through AVDD = 3V, V_{REF} = 3V, Data Rate = 80SPS summarize the typical noise performance with inputs shorted externally for different gains, data rates, and voltage reference values. The RMS and peak-to-peak noise data are referred to the input.

The effective resolution of the ADC is defined as:

$$\text{Effective Resolution (Bits)} = \ln (\text{FSR} / \text{RMS Noise}) / \ln (2) \quad (1)$$

The noise-free resolution of the ADC is defined as:

$$\text{Noise-Free Resolution (Bits)} = \ln (\text{FSR} / \text{Peak-to-Peak Noise}) / \ln (2) \quad (2)$$

where

- FSR = full-scale range = V_{REF} / gain

表 6-1. AVDD = 5V, V_{REF} = 5V, Data Rate = 10SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	EFFECTIVE RESOLUTION (Bits)	NOISE-FREE RESOLUTION (Bits)
1	420nV	1.79µV	23.5	21.4
2	270nV	900nV	23.1	21.4
64	19nV	125nV	22.0	19.2
128	17nV	110nV	21.1	18.4

(1) Peak-to-peak noise data are based on direct measurement.

表 6-2. AVDD = 5V, V_{REF} = 5V, Data Rate = 80SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	EFFECTIVE RESOLUTION (Bits)	NOISE-FREE RESOLUTION (Bits)
1	1.36µV	8.3µV	21.8	19.2
2	850nV	5.5µV	21.5	18.8
64	48nV	307nV	20.6	18
128	44nV	247nV	19.7	17.2

(1) Peak-to-peak noise data are based on direct measurement.

表 6-3. AVDD = 3V, V_{REF} = 3V, Data Rate = 10SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	EFFECTIVE RESOLUTION (Bits)	NOISE-FREE RESOLUTION (Bits)
1	450nV	2.8µV	22.6	20
2	325nV	1.8µV	22.1	19.7
64	20nV	130nV	21.2	18.5
128	18nV	115nV	20.3	17.6

(1) Peak-to-peak noise data are based on direct measurement.

表 6-4. AVDD = 3V, V_{REF} = 3V, Data Rate = 80SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	EFFECTIVE RESOLUTION (Bits)	NOISE-FREE RESOLUTION (Bits)
1	2.2µV	12µV	20.4	17.9
2	1.2µV	6.8µV	20.2	17.8
64	54nV	340nV	19.7	17.1
128	48nV	254nV	18.9	16.5

(1) Peak-to-peak noise data are based on direct measurement of 1024 samples.

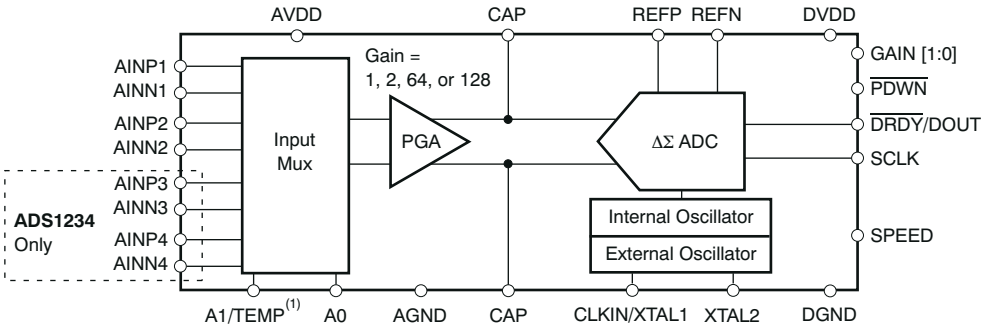
7 Detailed Description

7.1 Overview

The ADS1232 and ADS1234 (ADS123x) are highly integrated, 24-bit ADCs that include an input multiplexer, low-noise PGA, third-order delta-sigma (ΔΣ) modulator, and fourth-order digital filter. With input-referred RMS noise down to 17 nV, the ADS123x are ideally suited for measuring the very low signals produced by bridge sensors in applications such as weigh scales, strain gauges, and pressure sensors.

Clocking can be supplied by an external oscillator, an external crystal, or by a precision internal oscillator. Data can be output at 10 SPS for excellent 50-Hz and 60-Hz rejection, or at 80 SPS when higher speeds are needed. The ADS123x are easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

7.2 Functional Block Diagram



NOTE: (1) A1 for ADS1234, TEMP for ADS1232.

7.3 Feature Description

7.3.1 Analog Inputs (AINPX, AINNX)

The input signal to be measured is applied to the input pins AINPx and AINNx. The positive internal input is generalized as AINP, and the negative internal input generalized as AINN. The signal is selected through the input MUX, which is controlled by pins A0 and TEMP (ADS1232) and pins A0 and A1 (ADS1234), as shown in 表 7-1 and 表 7-2.

The ADS123x accepts differential input signals, but can also accept single-ended signals. When measuring single-ended signals, it is permissible to connect the negative input (AINNx) to ground only for gain = 1 or 2. When using gain = 64 or 128, connect AINNx to a level-shift voltage equal to mid-AVDD supply to comply with the input range requirement. Connect the signal to the positive input (AINPx). When the ADS123x are configured this way, only half of the converter full-scale range is used because only positive digital output codes are produced.

The analog and reference inputs are protected by ESD diodes. See 図 7-3 for the similar connection of the ESD diodes for the analog inputs.

表 7-1. ADS1232 Input Channel Selection With A0 and TEMP

MUX PINS		SELECTED ANALOG INPUTS	
TEMP	A0	POSITIVE INPUT	NEGATIVE INPUT
0	0	AINP1	AINN1
0	1	AINP2	AINN2
1	x	Temperature sensor	Temperature sensor

表 7-2. ADS1234 Input Channel Selection With A0 and A1

MUX PINS		SELECTED ANALOG INPUTS	
A1	A0	POSITIVE INPUT	NEGATIVE INPUT
0	0	AINP1	AINN1
0	1	AINP2	AINN2
1	0	AINP3	AINN3
1	1	AINP4	AINN4

7.3.2 Temperature Sensor (ADS1232 Only)

On-chip diodes provide temperature-sensing capability. By setting the TEMP pin high, the selected analog inputs are disconnected and the inputs to the ADC are connected to the anodes of two diodes scaled to 1x and 80x in current and size, as shown in 図 7-1. By measuring the difference in voltage of these diodes, temperature changes can be inferred from a baseline temperature. Typically, the difference in diode voltage is 111.7 mV at 25°C with a temperature coefficient of 379 µV/°C. With PGA gain = 1 and 2, the difference voltage output from the PGA is 111.7 mV and 223.4 mV, respectively. The temperature sensor function is impossible to use with PGA gain = 64 and 128.

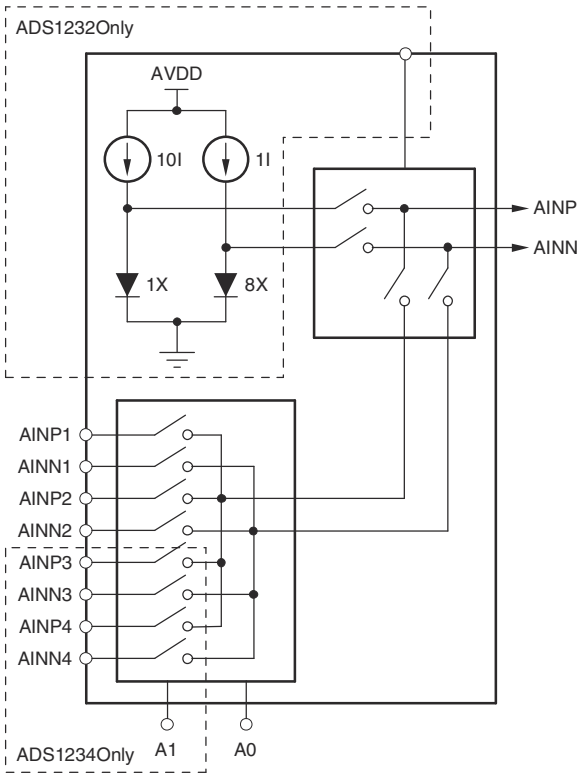


図 7-1. Measurement of the Temperature Sensor in the Input Multiplexer

7.3.3 Low-Noise PGA

The ADS123x feature a low-drift, low-noise PGA that provides a complete front-end solution for bridge sensors. A simplified diagram of the PGA is shown in 図 7-2. The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately matched resistors (R_1, R_{F1}, and R_{F2}), which construct a differential front-end stage with a gain of 64, followed by gain stage A3. The PGA inputs are equipped with an EMI filter, as shown in 図 7-2. The cut-off frequency of the EMI filter is 19.6 MHz. If the PGA gain is set to 1 or 2, the gain-of-64 stage is bypassed and shut down to save power. With the combination of both gain stages, the PGA gain can be set to 64 or 128. The PGA gain of the ADS123x is set to 1, 2, 64, or 128 by pins GAIN1 (MSB) and GAIN0 (LSB). 表 7-3 shows the gain setting of the PGA.

表 7-3. PGA Gain

GAIN[1:0] INPUT PINS	PGA GAIN
00	1
01	2
10	64
11	128

By using AVDD as the reference input, the bipolar input ranges from ±2.5 V to ±19.5 mV, while the unipolar ranges from 2.5 V to 19.5 mV. When the PGA gain is set to 1 or 2, the absolute inputs can go rail-to-rail without significant performance degradation. However, the inputs of the ADS123x are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent damage to the input circuitry. On the other hand, when the PGA gain is set to 64 or 128, the operating input range is limited to (AGND + 1.5 V) to (AVDD – 1.5 V), in order to prevent saturating the differential front-end circuitry and degrading performance.

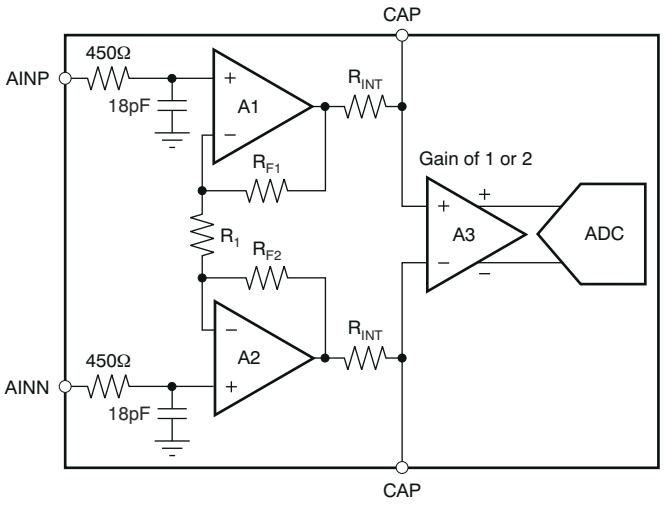


図 7-2. Simplified Diagram of the PGA

7.3.3.1 PGA Bypass Capacitor

By applying a 0.1µF external capacitor (C_{EXT}) across two PGA output pins (pins 9 and 10 and the combination of the internal 2kΩ resistor (R_{INT}), a low-pass filter with a corner frequency of 720Hz is created to band limit the signal path prior to the modulator input. This low-pass filter serves two purposes. First, the input signal is band-limited to prevent aliasing, as well as to filter high-frequency noise. Second, the low-pass filter attenuates the chopping residue from the PGA (for gains of 64 and 128 only) to improve temperature drift performance. High-quality capacitors (such as high-k ceramic or tantalum capacitors) are not required for a general application. However, high-quality capacitors, such as C0G dielectric ceramic or poly, are recommended for high-linearity applications.

7.3.4 Voltage Reference Inputs (REFP, REFN)

The voltage reference used by the modulator is generated from the voltage difference between pins REFP and REFN: $V_{REF} = V_{(REFP)} - V_{(REFN)}$. The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, a switching buffer circuitry is used to reduce the input equivalent capacitance. The reference drift and noise impact ADC performance. In order to achieve best results, pay close attention to the reference noise and drift specifications. A simplified diagram of the circuitry on the reference inputs is shown in 図 7-3. The switches and capacitors can be modeled with an effective impedance of:

$$Z_{EFF} = \frac{1}{2 f_{MOD} C_{BUF}}$$

where

- f_{MOD} = modulator sampling frequency = f_{CLK} / 64 = (76.8 kHz)
- C_{BUF} = input capacitance of the buffer

For the ADS123x:

$$Z_{EFF} = \frac{1}{(2)(76.8\text{kHz})(13\text{fF})} = 500\text{M}\Omega$$

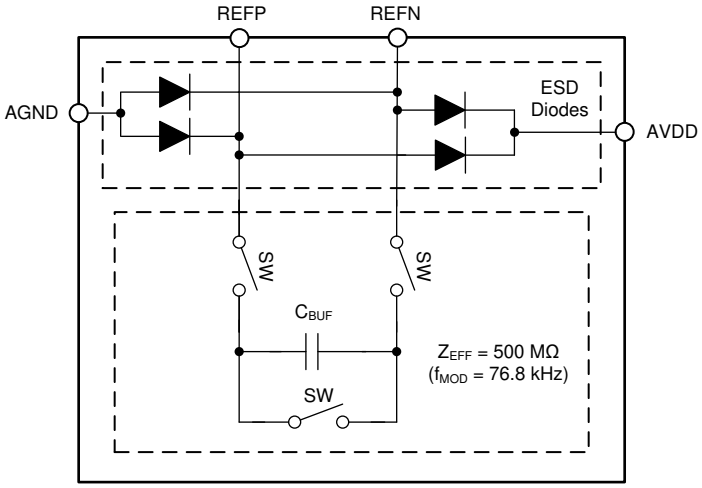


図 7-3. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 100 mV; and likewise, do not exceed AVDD by 100 mV:

AGND – 100 mV < $V_{(REFP)}$ or $V_{(REFN)}$ < AVDD + 100 mV

7.3.5 Clock Sources

The ADS123x can use an external clock source, external crystal, or internal oscillator to accommodate a wide variety of applications. 図 7-4 shows the equivalent circuitry of the clock source. The CLK_DETECT block determines whether a crystal oscillator or external clock signal is applied to the CLKIN/XTAL1 pin so that the internal oscillator is bypassed or activated. When the CLKIN/XTAL1 pin frequency is above approximately 200 kHz, the CLK_DETECT output goes low and shuts down the internal oscillator. When the CLKIN/XTAL1 pin frequency is below approximately 200 kHz, the CLK_DETECT output goes high and activates the internal oscillator. Connect the CLKIN/XTAL1 pin to ground when the internal oscillator is chosen.

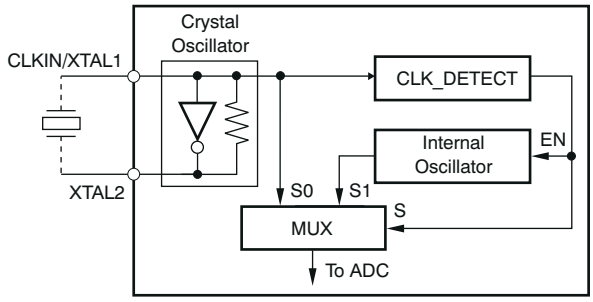


図 7-4. Equivalent Circuitry of the Clock Source

For crystal operation, connect the 4.9152-MHz crystal across the CLKIN/XTAL1 and XTAL2 pins. 表 7-4 shows the recommended crystal part numbers. As a result of the low-power design of the internal parallel-resonant circuit, both the CLKIN/XTAL1 and XTAL2 pins are only for use with the external crystal; do not use these pins as clock output drivers for external circuitry. No external capacitors are used with the crystal. Place the crystal as close as possible to the device pins in order to reduce board stray capacitance and in order to help ensure proper crystal operation.

表 7-4. Recommended Crystals

MANUFACTURER	FREQUENCY	PART NUMBER
ECS	4.9152 MHz	ECS-49-20-1
ECS	4.9152 MHz	ECS-49-20-4

An external clock oscillator can be used by driving the CLKIN/XTAL1 pin from the oscillator output and leave XTAL2 disconnected.

7.3.6 Digital Filter Frequency Response

The ADS123x use a sinc^4 digital filter with the frequency response (f_{CLK} = 4.9152 MHz) shown in 図 7-5. The frequency response repeats at multiples of the modulator sampling frequency of 76.8 kHz. The overall response is that of a low-pass filter with a –3-dB cutoff frequency of 2.4 Hz with the SPEED pin tied low (10-SPS data rate) and 19 Hz with the SPEED pin tied high (80-SPS data rate).

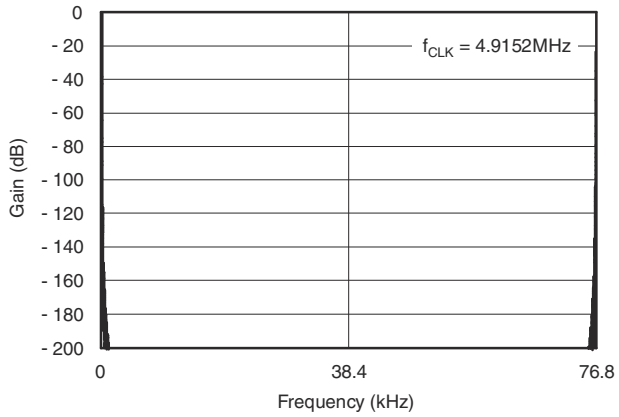


図 7-5. Digital Filter Frequency Response

To better demonstrate the response at lower frequencies, 図 7-6(a) illustrates the response out to 100 Hz, when the data rate = 10 SPS. Notice that signals at multiples of 10 Hz are rejected, and therefore, simultaneous rejection of 50 Hz and 60 Hz interference is achieved.

The benefit of using a sinc^4 filter is that every frequency notch has four zeros at the same location. This response, combined with the low-drift internal oscillator, provides an excellent normal-mode rejection of line-cycle interference.

図 7-6(b) shows the plot enlarged for both 50-Hz and 60-Hz notches with the SPEED pin tied low (10-SPS data rate). With only a ±3% variation of the internal oscillator, over 100 dB of normal-mode rejection is achieved.

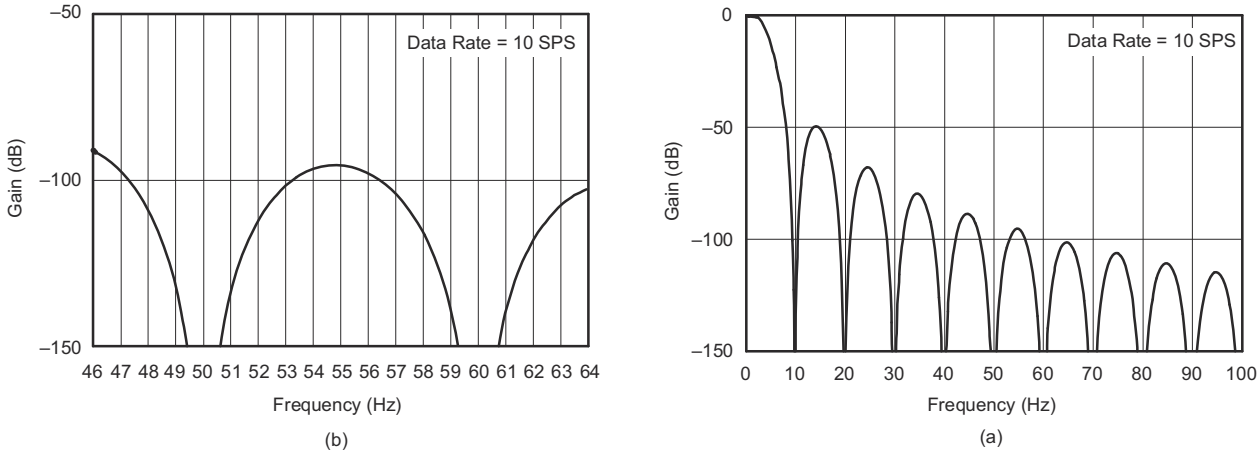


図 7-6. Digital Filter Frequency Response to 100 Hz

The ADS123x data rate and frequency response scale directly with clock frequency. For example, if f_{CLK} increases from 4.9152 MHz to 6.144 MHz when the SPEED pin is tied high, the data rate increases from 80 SPS to 100 SPS, while filter notches also increase from 80 Hz to 100 Hz. Frequency scaling is only possible when the external clock source is applied.

7.3.7 Settling Time

After changing the input multiplexer, the first data are fully settled. In both ADS123x devices, the digital filter is allowed to settle after toggling either the A1 or A0 pin. Toggling any of these digital pins holds the $\overline{DRDY}$/DOUT line high until the digital filter is fully settled. For example, if A0 changes from low to high, selecting a different input channel, $\overline{DRDY}$/DOUT immediately goes high, and $\overline{DRDY}$/DOUT goes low when fully settled data are ready for retrieval. There is no need to discard any data. 図 7-7 shows the timing of the $\overline{DRDY}$/DOUT line as the input multiplexer changes.

In certain instances, large or abrupt input changes require four data cycles to settle. One example of such a change is an external multiplexer in front of the ADS123x, which can cause large changes in input voltage simply by switching input channels. Another example is toggling the TEMP pin, which switches the internal AINP, AINN signals to connect to either the external AINPx, AINNx pins or to the TEMP diode (see 図 7-1).

To acquire fully settled data after an input step change, five readings are required. Five readings are required because if the change in input occurs in the middle of the first conversion, four additional full conversions of the fully settled input are required to get fully settled data. Discard the first four readings because they contain only partially settled data. 図 7-8 illustrates the settling time for the ADS123x in continuous conversion mode.

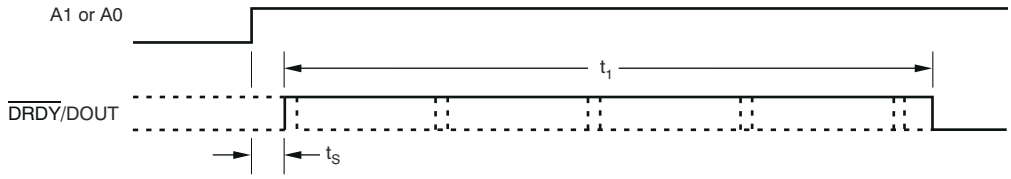


図 7-7. Example of Settling Time After Changing the Input Multiplexer

表 7-5. Timing Requirements for 図 7-7

PARAMETER(1)			MIN	MAX	UNIT
t_S	Setup time for changing the A1 or A0 pins		40	50	µs
t_1	Settling time ($\overline{DRDY}$/DOUT held high)	SPEED = 1	51	51	ms
		SPEED = 0	401	401	ms

(1) Values given for f_{CLK} = 4.9152 MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

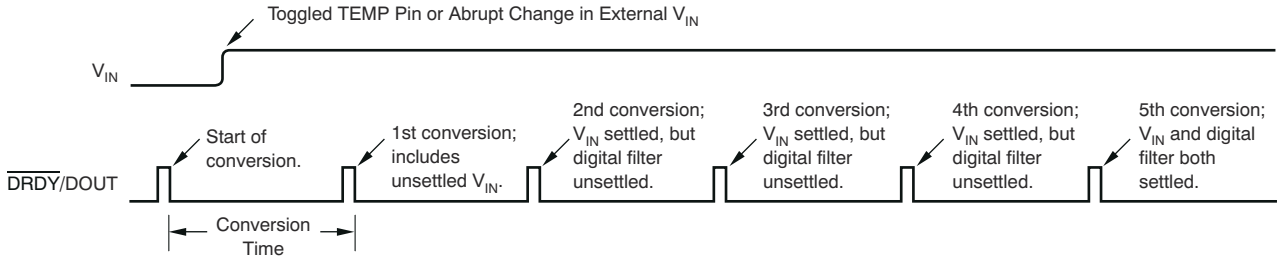


図 7-8. Settling Time in Continuous Conversion Mode

7.3.8 Data Rate

The ADS123x data rate is set by the SPEED pin, as shown in 表 7-6. When SPEED is low, the data rate is nominally 10 SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50-Hz and 60-Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of 80 SPS.

表 7-6. Data Rate Settings

SPEED PIN	DATA RATE	
	INTERNAL OSCILLATOR OR 4.9152-MHz CRYSTAL	EXTERNAL OSCILLATOR
0	10 SPS	f_{CLK} / 491,520
1	80 SPS	f_{CLK} / 61,440

7.3.9 Data Format

The ADS123x output 24 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of 0.5 V_{REF} / (2^{23} – 1). The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. 表 7-7 summarizes the ideal output codes for different input signals.

表 7-7. Ideal Output Code Versus Input Signal (1)

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE
≥ 0.5 V_{REF} / Gain	7FFFFFh
(0.5 V_{REF} / Gain) / (2^{23} – 1)	000001h
0	000000h
(–0.5 V_{REF} / Gain) / (2^{23} – 1)	FFFFFFh
≤ –0.5 V_{REF} / Gain	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

7.3.10 Data Ready and Data Output ($\overline{DRDY}$/DOUT)

This digital output pin serves two purposes. First, $\overline{DRDY}$/DOUT indicates when new data are ready by going low. Afterwards, on the first rising edge of SCLK, the $\overline{DRDY}$/DOUT pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced high with an additional SCLK. $\overline{DRDY}$/DOUT then remains high until new data are ready. This configuration is useful when polling on the status of $\overline{DRDY}$/DOUT to determine when to begin data retrieval.

7.3.11 Serial Clock Input (SCLK)

This digital input shifts serial data out with each rising edge. This input has built-in hysteresis, but care must be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, make sure the rise-and-fall times of SCLK are less than 50 ns.

7.3.12 Data Retrieval

The ADS123x continuously converts the analog input signal. To retrieve data, wait until $\overline{DRDY}$/DOUT goes low, as shown in 図 7-9. After $\overline{DRDY}$/DOUT goes low, begin shifting out the data by applying SCLKs. Data are shifted out MSB first. Not all 24 bits of data are required to be shifted out, but the data must be retrieved before new data are updated (within t_7) or else the data are overwritten. Avoid data retrieval during the update period (t_6). $\overline{DRDY}$/DOUT remains at the state of the last bit shifted out until taken high (see t_6), indicating that new data are being updated. To avoid having $\overline{DRDY}$/DOUT remain in the state of the last bit, the user can shift SCLK to force $\overline{DRDY}$/DOUT high, as shown in 図 7-10. This technique is useful when a host controlling the device is polling $\overline{DRDY}$/DOUT to determine when data are ready.

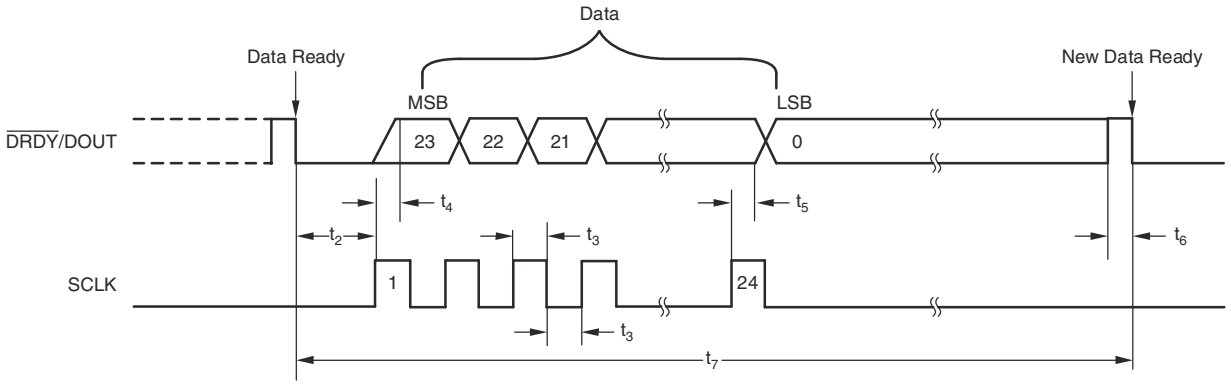


図 7-9. Data Retrieval Timing

表 7-8. Timing Requirements for 図 7-9

PARAMETER			MIN	TYP	MAX	UNIT
t_2	$\overline{DRDY}$/DOUT low to first SCLK rising edge		0			ns
t_3	SCLK positive or negative pulse width		100			ns
t_4	SCLK rising edge to new data bit valid: propagation delay				50	ns
t_5	SCLK rising edge to old data bit valid: hold time		0			ns
t_6 (1)	Data updating: no readback allowed		39			µs
t_7 (1)	Conversion time (1/data rate)	SPEED = 1		12.5		ms
		SPEED = 0		100		

(1) Values given for f_{CLK} = 4.9152 MHz. For different f_{CLK} frequencies, scale proportional to the CLK period.

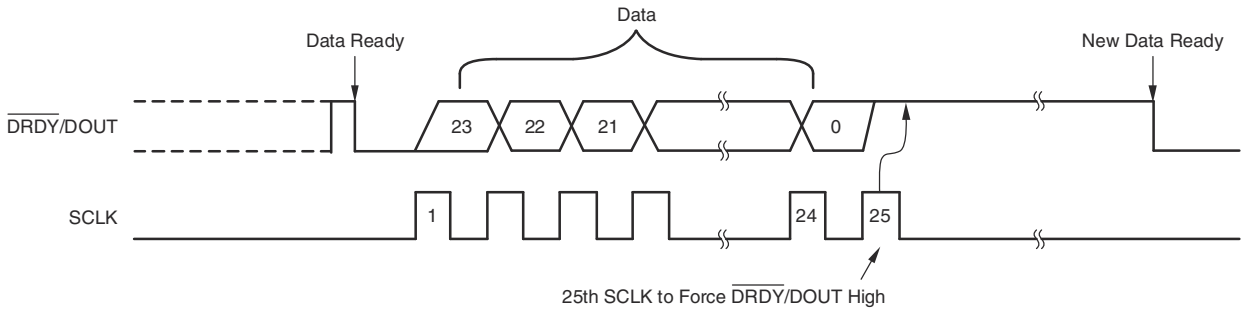


図 7-10. Data Retrieval With $\overline{DRDY}$/DOUT Forced High Afterwards

7.4 Device Functional Modes

In addition to the active conversion mode, the device has other functional modes: offset calibration mode (to calibrate the ADC internal offset), standby mode (saving power when not converting), and a power-down mode (for complete device shutdown).

7.4.1 Offset Calibration Mode

Offset calibration can be initiated at any time to remove the ADS123x offset error. To initiate offset calibration, apply at least two additional SCLKs after retrieving 24 bits of data. 図 7-11 shows the timing pattern. The 25th SCLK sends $\overline{\text{DRDY}}$/DOUT high. The falling edge of the 26th SCLK begins the calibration cycle. Additional SCLK pulses can be sent after the 26th SCLK; however, minimize activity on SCLK during offset calibration for best results. The analog input pins are disconnected within the ADC and the appropriate signal is applied internally to perform the calibration.

When the calibration is completed, $\overline{\text{DRDY}}$/DOUT goes low, indicating that new data are ready. The first conversion after a calibration is fully settled and valid for use. The offset calibration takes exactly the same time as specified in (t_8) right after the falling edge of the 26th SCLK.

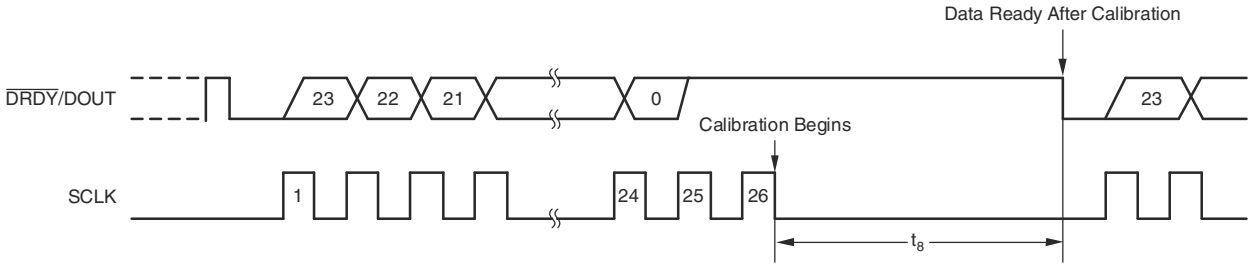


図 7-11. Offset-Calibration Timing

表 7-9. Timing Requirements for 図 7-11

PARAMETER			MIN	MAX	UNIT
t_8 (1)	First data ready after calibration	SPEED = 1 (80 SPS)	101.28	101.29	ms
		SPEED = 0 (10 SPS)	801.02	801.03	

(1) Values given for f_{CLK} = 4.9152 MHz. For different f_{CLK} frequencies, scale proportional to the CLK period. Expect a ±3% variation when the internal oscillator is used.

7.4.2 Standby Mode

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. In standby mode, the entire analog circuitry is powered down and only the clock source circuitry is awake to reduce the wake-up time from the standby mode. To enter standby mode, simply hold SCLK high after $\overline{\text{DRDY}}$/DOUT goes low; see 図 7-12. Standby mode can be initiated at any time during readback; all 24 bits of data are not required to be retrieved beforehand.

When t_{10} has passed with SCLK held high, standby mode activates. $\overline{\text{DRDY}}$/DOUT stays high when standby mode begins. SCLK must remain high to stay in standby mode. To exit standby mode (wakeup), set SCLK low. The first data after exiting standby mode is valid.

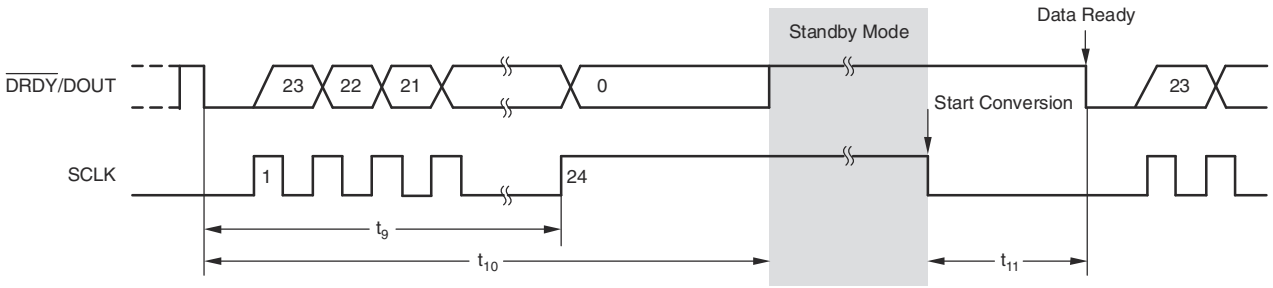


図 7-12. Standby Mode Timing (Can be Used for Single Conversions)

表 7-10. Timing Requirements for 図 7-12

PARAMETER			MIN	MAX	UNIT
t_9 (1)	SCLK high after DRDY/DOUT goes low to activate standby mode	SPEED = 1	0	12.44	ms
		SPEED = 0	0	99.94	
t_{10} (1)	Standby mode activation time	SPEED = 1	12.46		ms
		SPEED = 0	99.96		
t_{11} (1)	Data ready after exiting standby mode	SPEED = 1	52.51	52.51	ms
		SPEED = 0	401.8	401.8	

(1) Values given for f_{CLK} = 4.9152 MHz. For different f_{CLK} frequencies, scale proportional to the CLK period. Expect a ±3% variation when an internal oscillator is used.

7.4.3 Standby Mode With Offset-Calibration

Offset-calibration can be set to run immediately after exiting standby mode. This feature is useful when the ADS123x is put in standby mode for long periods of time, and offset-calibration is desired afterwards to compensate for temperature or supply voltage changes.

To force an offset-calibration with standby mode, shift 25 SCLKs and take the SCLK pin high to enter standby mode. Offset-calibration then begins after wake-up; 図 7-13 shows the appropriate timing. Note the extra time needed after wake-up for calibration before data are ready. The first data after standby mode with offset-calibration is fully settled and can be used right away.

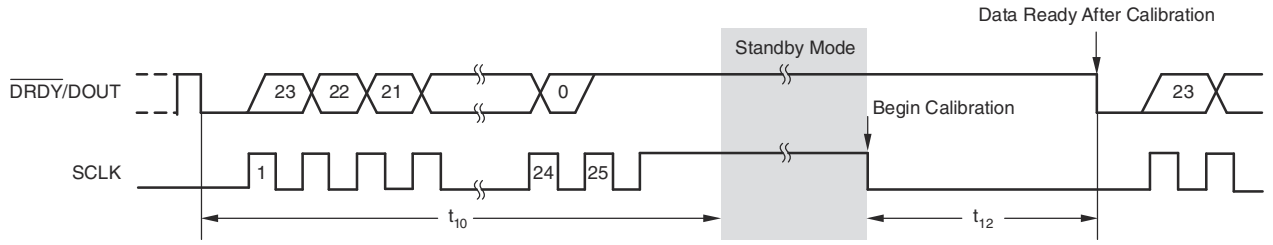


図 7-13. Standby Mode With Offset-Calibration Timing (Can be Used for Single Conversions)

表 7-11. Timing Requirements for 図 7-13

PARAMETER			MIN	MAX	UNIT
t_{12} (1)	Data ready after exiting standby mode and calibration	SPEED = 1	103	103	ms
		SPEED = 0	803	803	

(1) Values given for f_{CLK} = 4.9152 MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

7.4.4 Power-Down Mode

Power-down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter power-down mode, hold the $\overline{PDWN}$ pin low. Power-down mode also resets the entire circuitry to free the ADC circuitry from locking up to an unknown state. Power-down mode can be initiated at any time during readback; not all 24 bits of data must be retrieved beforehand. 図 7-14 shows the wake-up timing from power-down mode.

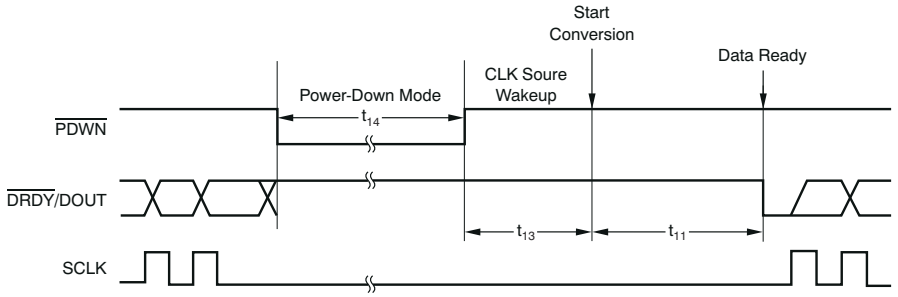


図 7-14. Wake-Up Timing From Power-Down Mode

表 7-12. Timing Requirements for 図 7-14

PARAMETER			MIN	TYP	UNIT
t_{13}	Wake-up time after power-down mode	Internal clock		7.95	µs
		External clock		0.16	µs
		Crystal oscillator(1)		5.6	ms
t_{14} (2)	$\overline{PDWN}$ pulse duration		26		µs

(1) No capacitors on CLKIN/XTAL1 or XTAL2 outputs.
(2) Value given for f_{CLK} = 4.9152 MHz. For different f_{CLK} frequencies, the scale is proportional to the CLK period except for a ±3% variation when an internal oscillator is used.

7.4.5 Power-Up Sequence

When powering up the ADS123x, follow the prescribed $\overline{PWDN}$ pin sequence as shown in 図 7-15. At power-up, hold the $\overline{PWDN}$ pin low until after AVDD and DVDD have stabilized above the minimum specified voltage levels. After an initial delay where $\overline{PWDN}$ must be held low (t_{15}), take $\overline{PWDN}$ high then toggle $\overline{PWDN}$ low to high with pulse durations (t_{16} and t_{17}) as shown in 図 7-15 and 表 7-13. The ADC then begins operation as shown in 図 7-14 and 表 7-12. Control $\overline{PDWN}$ by the host processor to provide the required power-on timing.

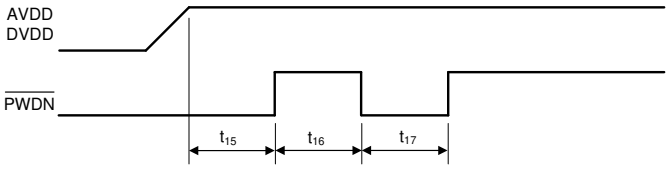


図 7-15. Power-Up Timing Sequence

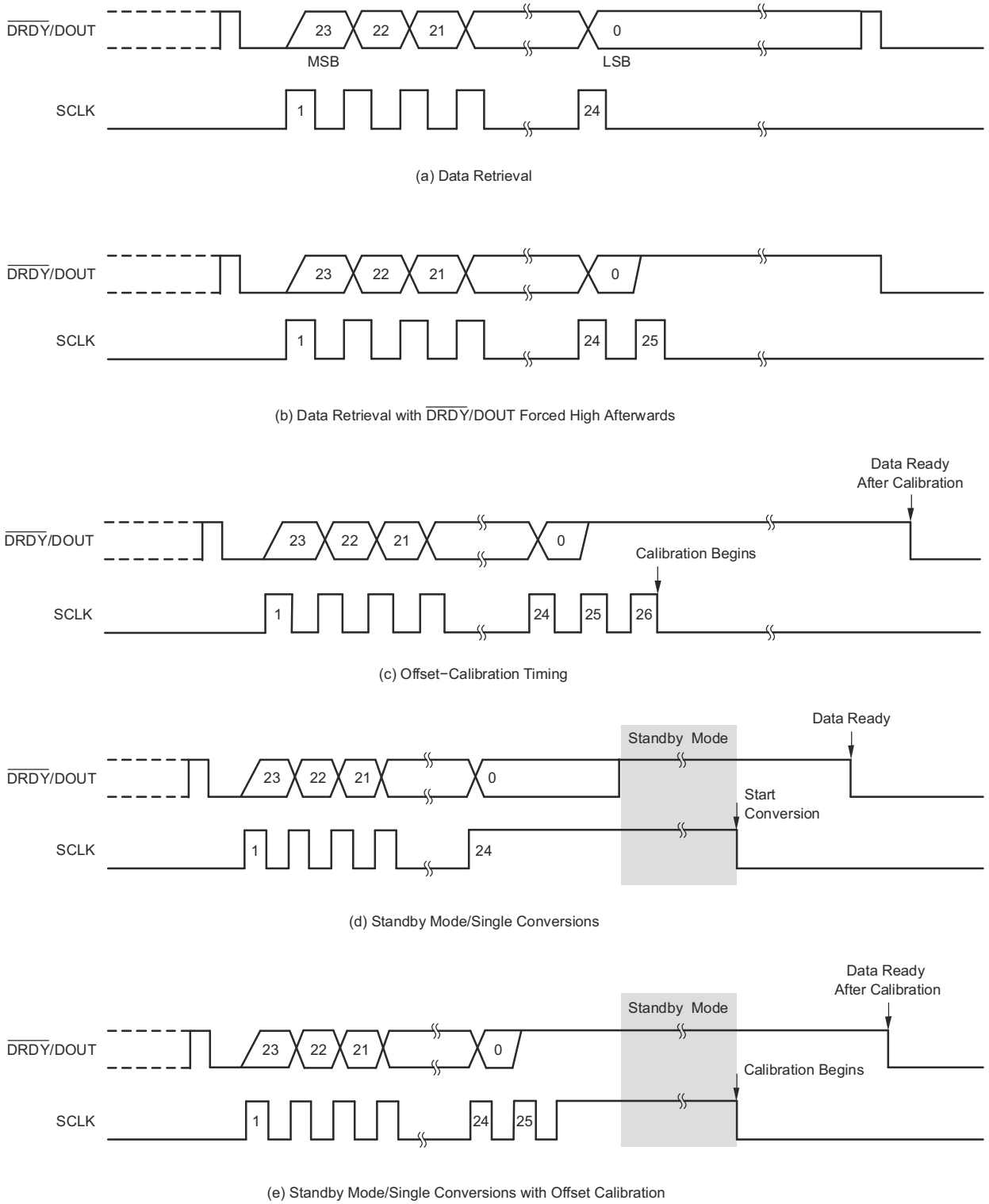
表 7-13. Power-up Timing Requirements for 図 7-15

PARAMETER		MIN(1)	UNIT
t_{15}	Delay time, $\overline{PWDN}$ high after AVDD, DVDD stable	10	µs
t_{16}	Pulse duration, $\overline{PWDN}$ high	26	µs
t_{17}	Pulse duration, $\overline{PWDN}$ low	26	µs

(1) f_{CLK} = 4.9152 MHz. For f_{CLK} < 4.9152 MHz, adjust the $\overline{PWDN}$ delay time and pulse duration accordingly.

7.4.6 Summary of Serial Interface Waveforms

図 7-16 summarizes the serial interface waveforms.



(a) Data Retrieval

(b) Data Retrieval with $\overline{\text{DRDY}}$/DOUT Forced High Afterwards

(c) Offset−Calibration Timing

(d) Standby Mode/Single Conversions

(e) Standby Mode/Single Conversions with Offset Calibration

図 7-16. Summary of Serial Interface Waveforms

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The ADS123x devices are high-resolution, 24-bit ADCs with an integrated low-noise PGA. Best performance is achieved by following the guidelines and recommendations described in the *Typical Application* section.

8.2 Typical Application

図 8-1 shows a circuit diagram of the ADS1232 as part of a weigh scale system. In this setup, the ADS1232 is configured to channel 1 input, gain = 128, and 10SPS data rate. Gain = 128 is selected by tying the GAIN[1:0] pins to logic high (3V in this example). Input channel 1 and data rate = 10SPS are selected by tying input channel select pins A0 and TEMP to ground, and by tying the data rate select pin SPEED to ground. The unused channel 2 inputs are tied to ground.

The internal oscillator is selected by grounding the CLKIN/XTAL1 pin. The other clock options are 1) 4.9152MHz crystal across the CLKIN/XTAL1 and XTAL2 pins, or 2) apply a clock to the CLKIN/XTAL1 pin (pin XTAL2 unconnected). The $\overline{\text{PWDN}}$ pin of the ADC is routed to the controller because this pin must be toggled after the ADC is powered. The bridge excitation voltage is connected to the ADC reference input pins (REFP, REFN). Not shown in 図 8-1 are R-C input filters for the signal and reference inputs. If these filters are used, match the filter time constants to maintain cancellation of noise common to both signal and reference inputs.

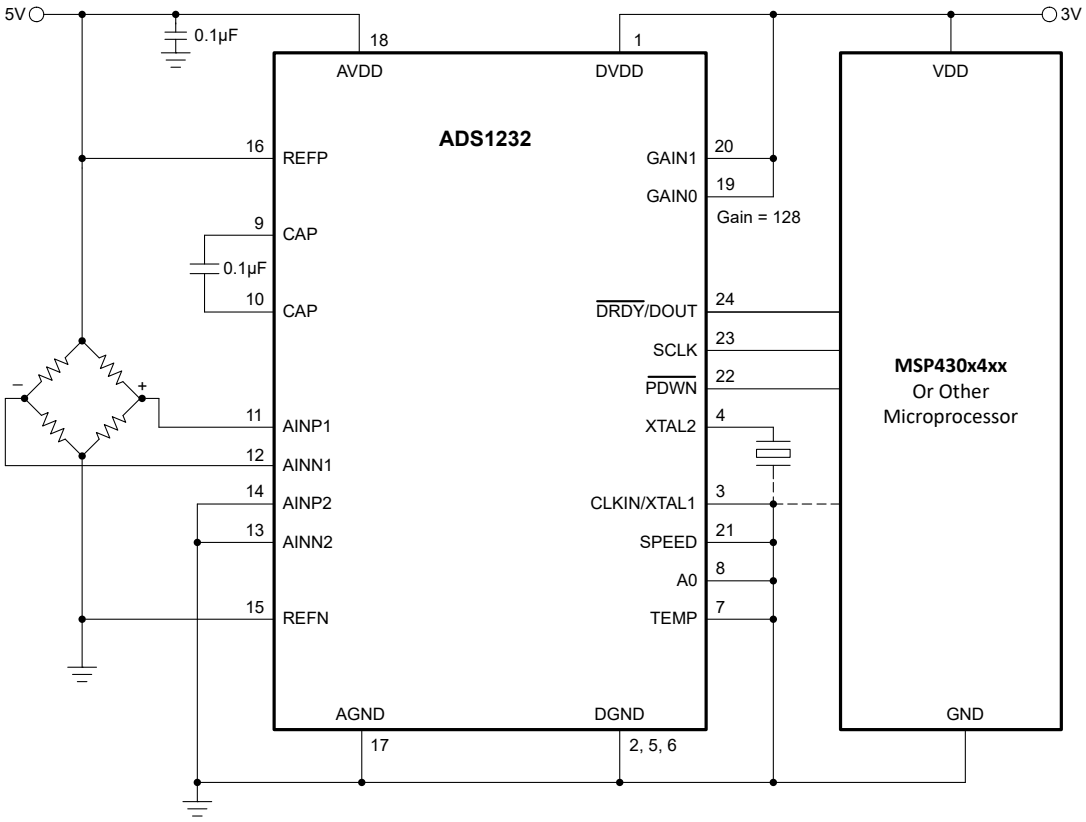


図 8-1. Weigh-Scale Application

8.2.1 Design Requirements

表 8-1 summarizes the design performance goals. 表 8-2 summarizes the system design parameters.

表 8-1. Design Goals

DESIGN GOAL	VALUE
Noise-free resolution	80,000 counts / 130,000 counts (post averaging)
Sample rate	10 SPS
Input step settling time	500 ms / 900 ms (post averaging)
50-Hz and 60-Hz noise rejection	>100 dB

表 8-2. Design Parameters

DESIGN PARAMETERS	DESIGN VALUE
Bridge resistance	1 kΩ
Bridge excitation voltage	5 V
Load cell sensitivity	2 mV/V
Bridge full-scale output	10 mV
ADC analog power supply	5 V
Host controller and ADC digital power supply	3 V

8.2.2 Detailed Design Procedure

Common performance metrics of a weigh scale are noise-free resolution (or counts) and offset and gain stability (drift) after calibrating the weigh scale. 表 6-1 to 表 6-4 illustrate ADC noise performance expressed as an input-referred quantity over gain, data rate, and analog supply voltage.

In this design example, the ADC analog supply voltage (5 V) is used as the bridge excitation voltage. 5-V excitation optimizes the bridge signal output compared to 3-V excitation and also has the benefit of optimizing the ADC conversion noise. Gain = 128 is selected because it also provides optimal noise performance. The front end circuitry of the ADC easily accommodates the 10-mV bridge output. In summary, the ADC configuration that yields the highest resolution while achieving the sample rate and settling time requirements is AVDD = 5 V, bridge excitation = 5 V, gain = 128, and sample rate = 10 SPS.

Signal-to-noise performance is improved by using a higher gauge-factor bridge (example 3 mV/V bridge), or by increasing the excitation voltage. If the excitation voltage > 5 V, a voltage divider is required to reduce the voltage at the ADC reference inputs.

Noise-free counts are improved by post averaging the data (for example, a moving-average filter performed in the microcontroller). A moving average filter reduces noise by a factor of $\sqrt{N}$, where N is the number of readings averaged. However, a moving average filter increases the input step settling time due to the latency caused by averaging.

The other key performance attributes are DC offset and gain drift, and 50-Hz and 60-Hz noise rejection. 図 5-14 and 図 5-16 illustrate the distributions of offset and gain drift performance. 50-Hz and 60-Hz noise rejection is described in 図 7-6. The ADC provides over 100-dB rejection with ±3% variation of the ADC clock frequency.

8.2.3 Application Curves

To evaluate the ADC's noise performance, four fixed-value, 1-kΩ low-drift precision resistors are connected in a bridge arrangement to simulate a bridge sensor. The simulator provides the same thermal noise generated by a physical bridge. One of the four bridge resistors is modified to 1.008 kΩ in order to provide a 10-mV output signal. The 10-mV signal is typical of a 2-mV/V load cell using 5-V excitation.

図 8-2 shows the ADC performance with data taken over a 60-second period. The 60-second period reveals true ADC peak-to-peak noise performance. 図 8-3 shows the same conversion data processed by an external moving average filter (average x4). The noise-free resolution of the ADC is approximately 85,000 counts. Over the same 60-second period, the moving average filter improves noise-free resolution to 135,000 counts. The noise-free resolution (bits) corresponding to unfiltered and filtered data are 16.3 bits and 17.1 bits. See 式 2 to calculate noise-free resolution in bits. In order to evaluate the actual noise-free resolution of the system, the 10-mV signal is used in the calculation, rather than the full input range of the ADC (39 mV = V_{REF} / 128),

As shown in the noise plots, the moving average filter reduces noise by approximately one-half. As a consequence of the post filter operation, the input step settling time increases from 500 ms to 900 ms (500 ms because of the ADC settling response time, 400 ms because of the post-averaging filter).

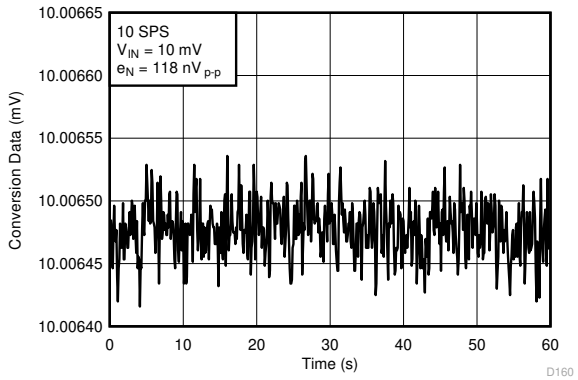


図 8-2. Unfiltered Conversion Data

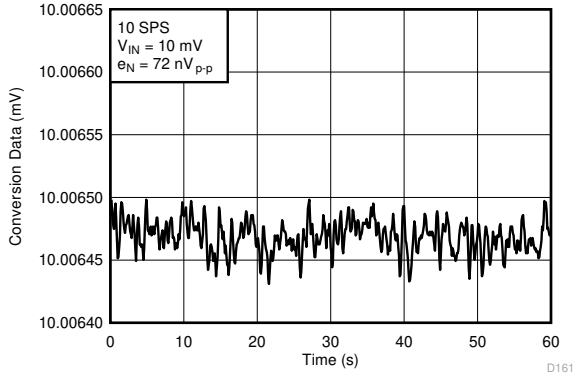


図 8-3. Filtered Conversion Data

8.3 Power Supply Recommendations

At device power-on, follow the $\overline{PWDN}$ pin toggle sequence as detailed in the *Power-Up Sequence* section.

The ADC has an analog power supply (AVDD) and digital power supply (DVDD). The supply range is 2.7V to 5.25V. The analog and digital supplies can be tied together, however the digital power supply must be clean and free of glitches and transients, which can be generated by the operation of LEDs, relays, and so forth. The bridge excitation voltage is often the same as the ADC supply voltage, so the supply voltage must be free of transients.

Voltage ripple produced by switching power supplies can also degrade ADC performance. The use a low-dropout regulator (LDOs) can reduce voltage ripple caused by switching power supplies.

8.3.1 Power-Supply Decoupling

Good power-supply decoupling is important in order to achieve rated performance. The power supplies must be decoupled close to the power-supply pins using short, direct connections to ground. For both analog and digital power supplies, connect a 0.1-µF capacitor (X7R-dielectric ceramic) from the power-supply pins to the ground plane.

8.4 Layout

Good layout practices are crucial to realize the full-performance of the ADC. Poor grounding can quickly degrade the noise performance. The following layout guidelines help provide the best results.

8.4.1 Layout Guidelines

For best performance, dedicate a PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on space limitations, a dedicated ground plane may not be practical. If a continuous ground plane is not possible, connect the individual plane segments in one place at the ADC.

Route digital traces away from the PGA output pins (CAP) and away from all analog inputs and associated components to minimize interference. Maintain differential trace routing for the input signal and reference signal to minimize RFI susceptibility.

Use C0G capacitors for analog and reference input filters and the PGA output capacitors in high-linearity applications. High-K type capacitors (such as Y5V and X7R) should be avoided. Place supply bypass and the PGA bypass capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections (such as multiple vias) on the ground-side connections of the bypass capacitors.

Avoid long traces on $\overline{\text{DRDY}}$/DOUT, because high trace capacitance can lead to increased ADC noise. Use a series resistor or a local buffer if long traces are used. When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer helps control reflections and overshoot. Glitches present on the clock signal can lead to increased noise and possible mis-operation and must be avoided.

図 8-4 illustrates a PCB layout example. Separate 5V analog and a 3.3V digital supplies are shown. The ADC configuration is through hard-tie of the control pins as shown in 表 8-3.

表 8-3. Layout Example Pin Connections

MODE	PIN CONTROL	VOLTAGE
Data rate = 10 SPS	SPEED	0V
Gain = 128	GAIN[1:0]	3.3V
Input = channel 1	A0, TEMP	0V

8.4.2 Layout Example

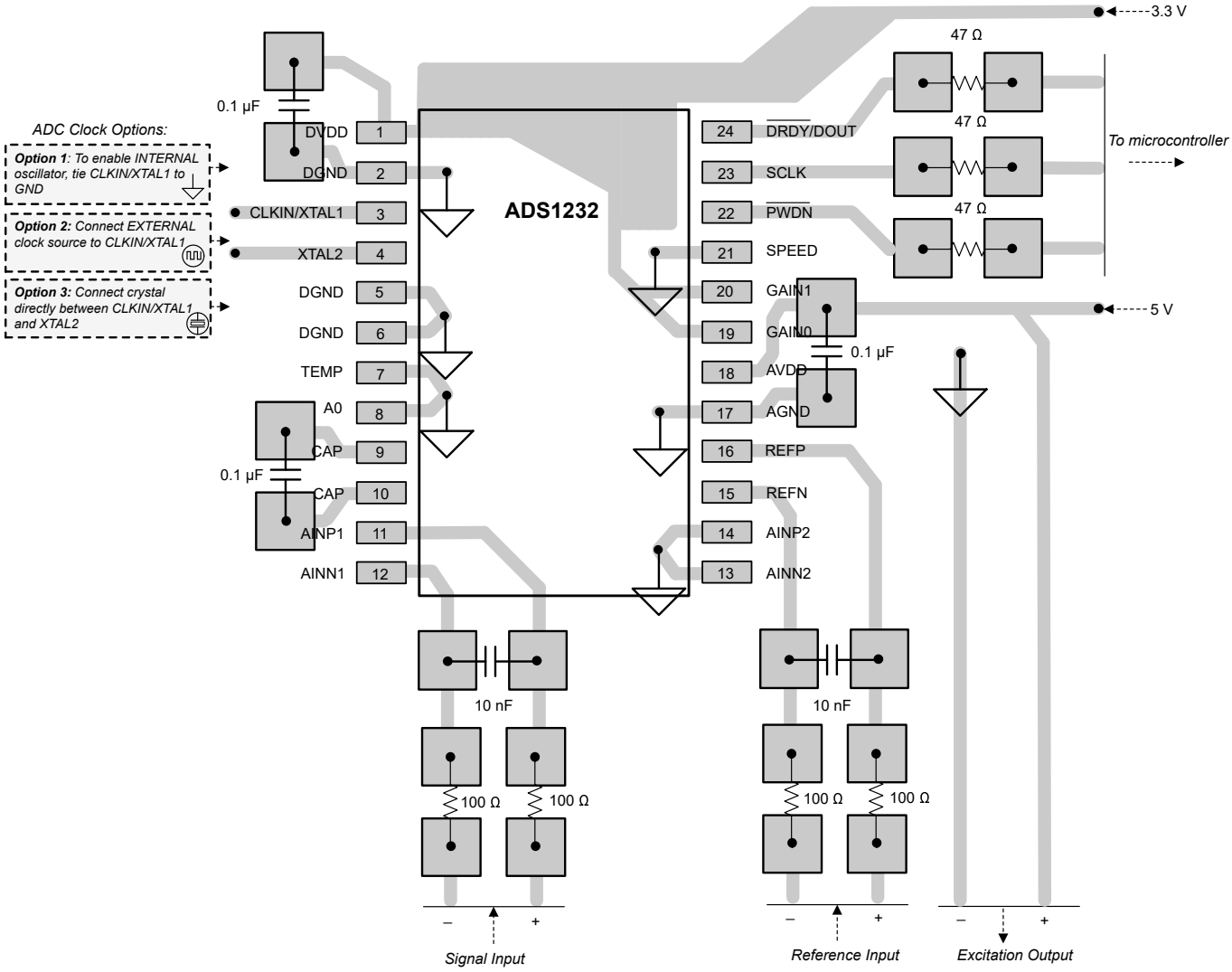


図 8-4. ADS1232 Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.3 Trademarks

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9.4 静電気放電に関する注意事項

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (January 2021) to Revision H (June 2025)	Page
• Changed ESD (HBM) rating from ±*1000V* to ±*750V*	6
• Changed *AINN3* to *AINN4* in *ADS1234 Input Channel Selection With A0 and A1* table	16

Changes from Revision F (February 2008) to Revision G (January 2021)	Page
• *ドキュメント全体にわたって表、図、相互参照の採番方法を更新*	1
• 「*製品情報*」および「*ESD 定格*」表、「*推奨動作条件*」および「*熱に関する情報*」表、「*詳細説明*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加	1
• Deleted *Ordering Information* section; all ordering information available in package option addendum located at end of data sheet	4
• Added analog input voltage specification to *Absolute Maximum Ratings*	6
• Added digital input voltage specification to *Absolute Maximum Ratings*	6
• Deleted momentary input current specification from *Absolute Maximum Ratings*	6
• Added input current note to *Absolute Maximum Ratings*	6
• Added common-mode voltage condition to Common-Mode Rejection specification in *Electrical Characteristics* table	8
• Deleted power-supply rejection (gain = 1) MIN specification from *Electrical Characteristics* table	8

- Changed power-supply rejection (gain = 1) TYP specification in *Electrical Characteristics* table 8
- Changed text in *Analog Inputs (AINPX, AINNX)* section..... 16
- Added *ADS1232 Input Channel Selection With A0 and TEMP* table..... 16
- Deleted link to *Using the MSC121x as a High-Precision Intelligent Temperature Sensor* 17
- Changed 10 SPS –3-dB frequency from 3.32 Hz to 2.4 Hz, and 80 SPS –3-dB frequency from 11.64 Hz to 19 Hz..... 21
- Changed *Power-Up Sequence* section..... 27
- Deleted Thermocouple application from *Application Information* 29
- Deleted RTDs and Thermistor application from *Application Information* 29
- Added weigh scale application to *Application Information* 29

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS1232IPW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1232IPW.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1232IPW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1232IPWG4	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1232IPWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1232IPWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1232IPWR.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1232IPWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1232
ADS1234IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1234
ADS1234IPW.A	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1234
ADS1234IPW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1234
ADS1234IPWG4	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1234
ADS1234IPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1234
ADS1234IPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1234
ADS1234IPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1234

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

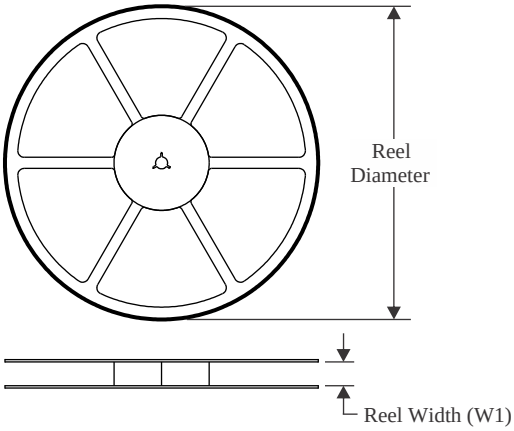
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

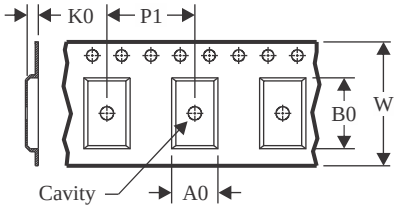
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

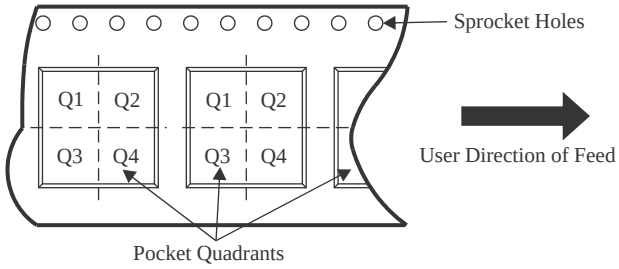


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

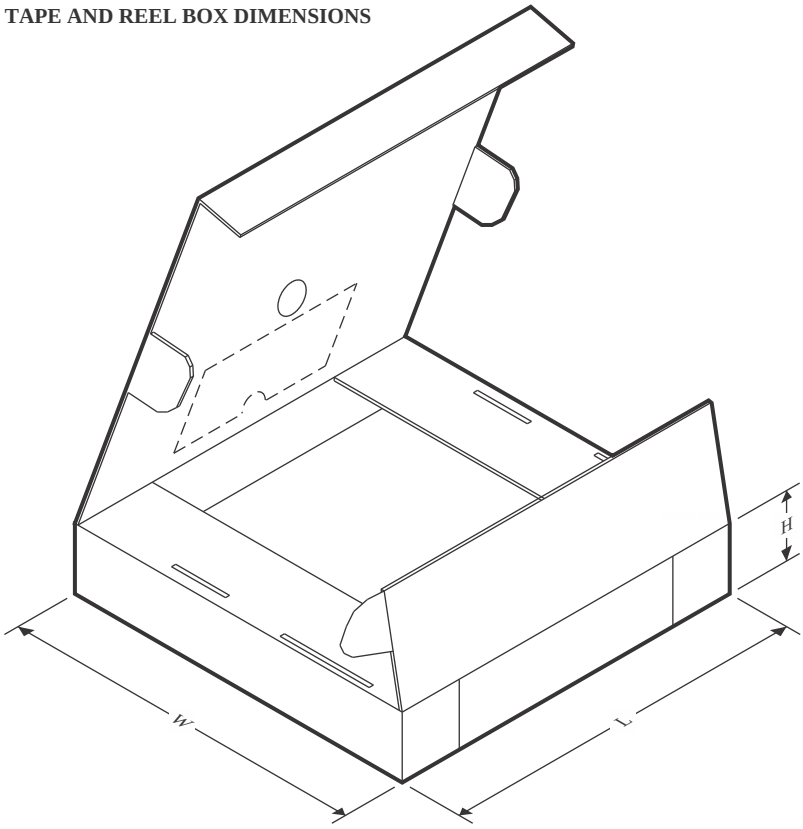
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1232IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS1234IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

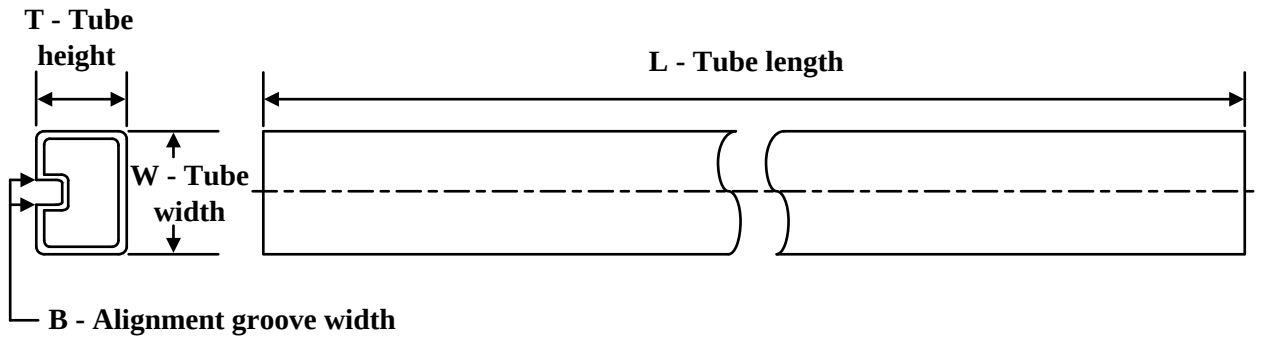
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1232IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
ADS1234IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0

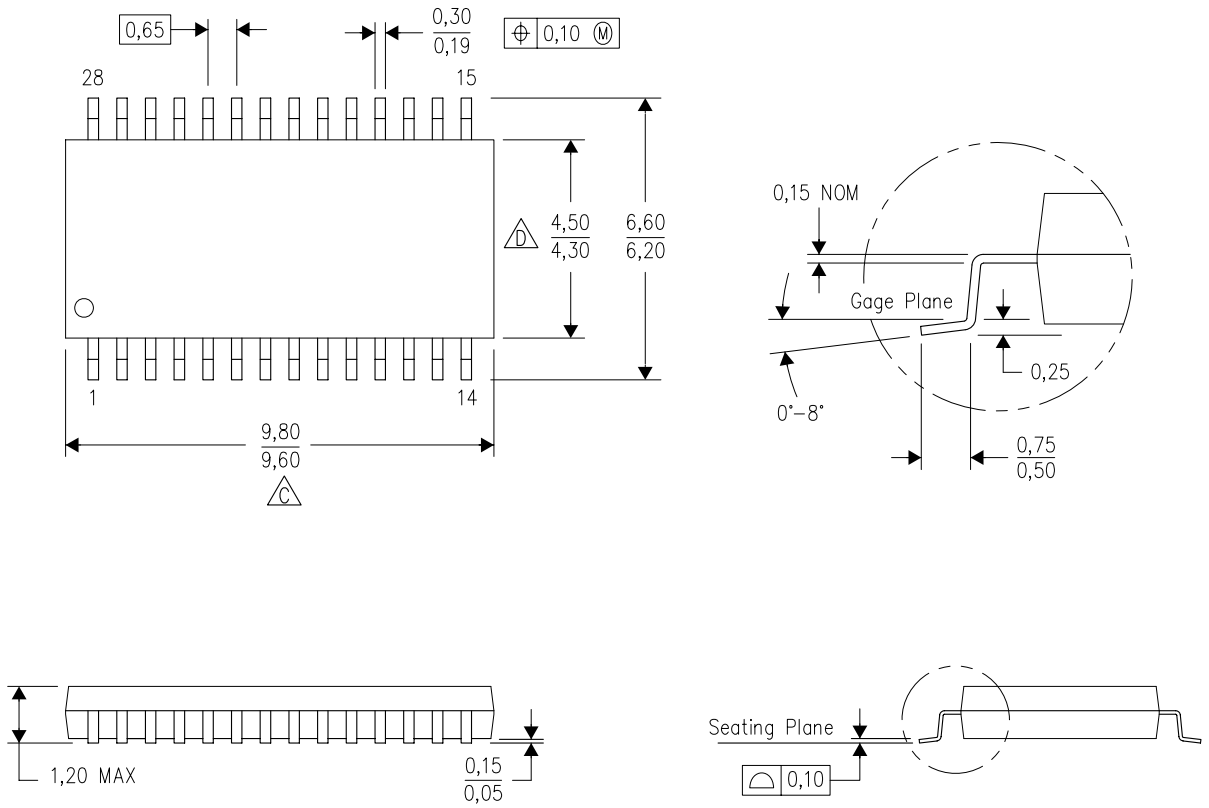
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1232IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
ADS1232IPW.A	PW	TSSOP	24	60	530	10.2	3600	3.5
ADS1232IPW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
ADS1232IPWG4	PW	TSSOP	24	60	530	10.2	3600	3.5
ADS1234IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
ADS1234IPW.A	PW	TSSOP	28	50	530	10.2	3600	3.5
ADS1234IPW.B	PW	TSSOP	28	50	530	10.2	3600	3.5
ADS1234IPWG4	PW	TSSOP	28	50	530	10.2	3600	3.5

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

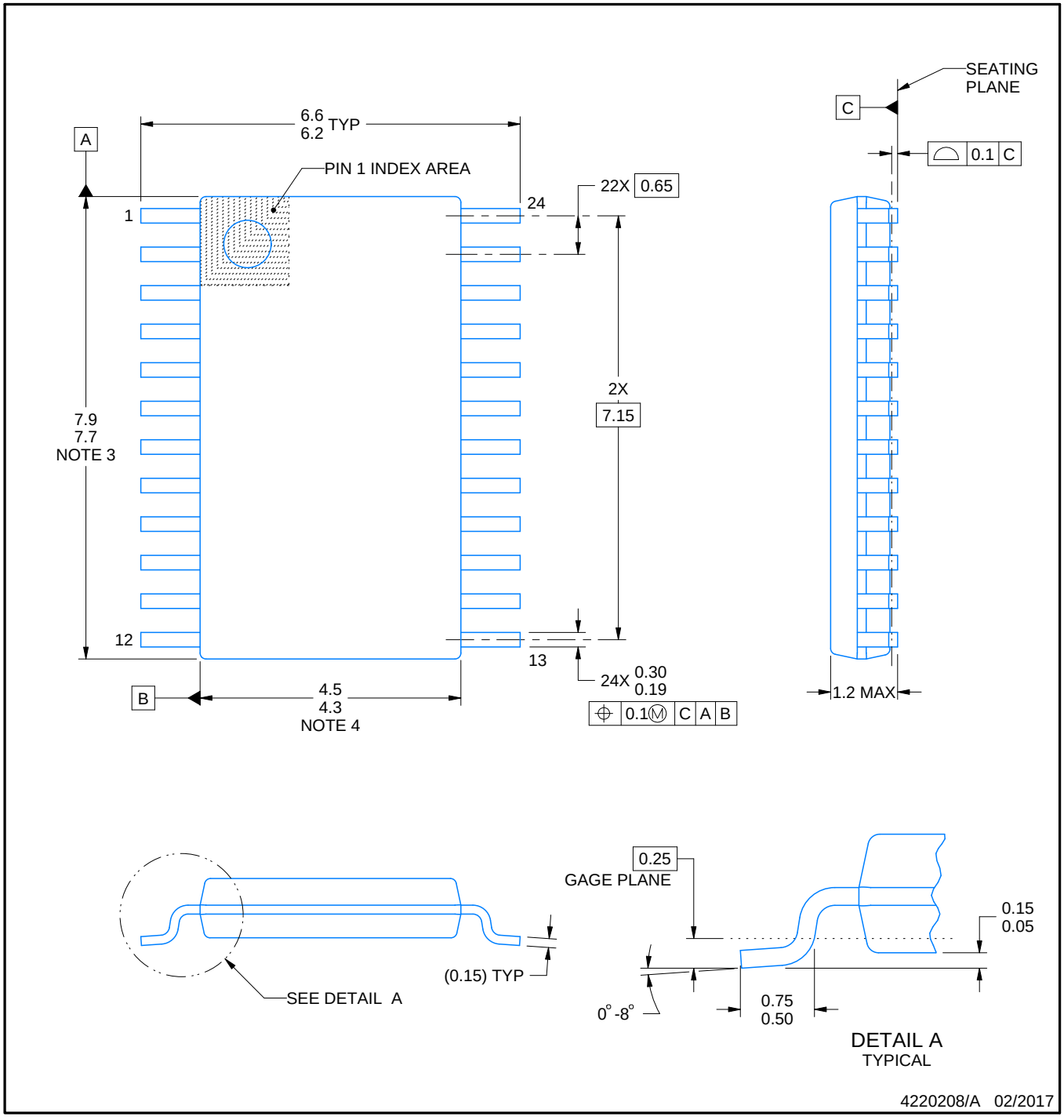
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PACKAGE OUTLINE

PW0024A

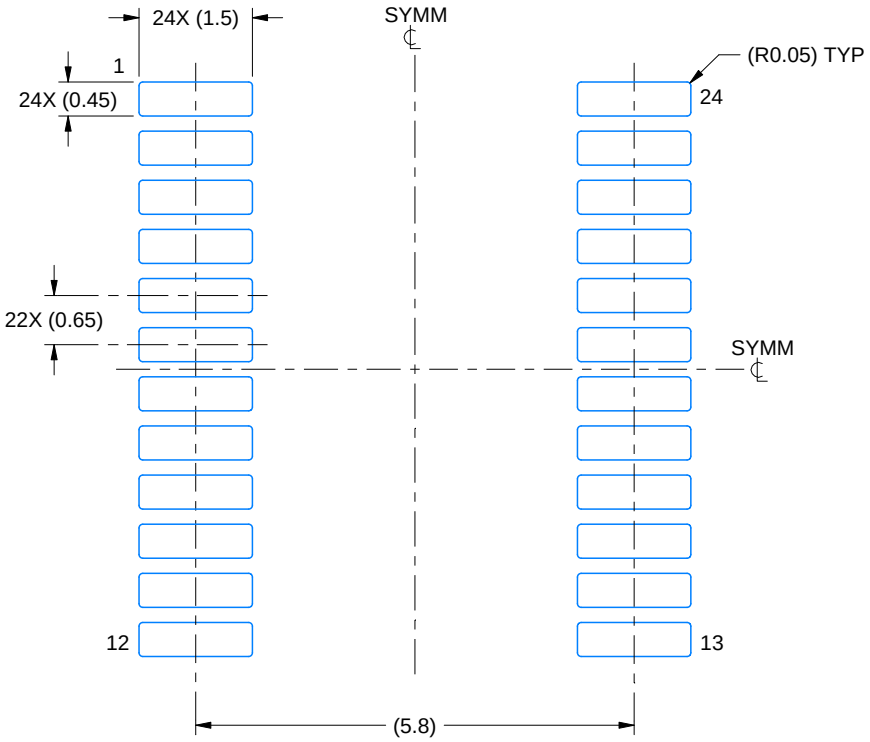
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

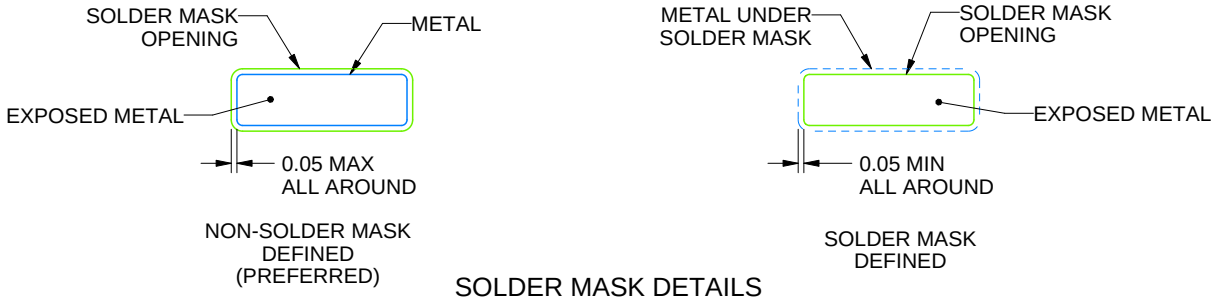


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

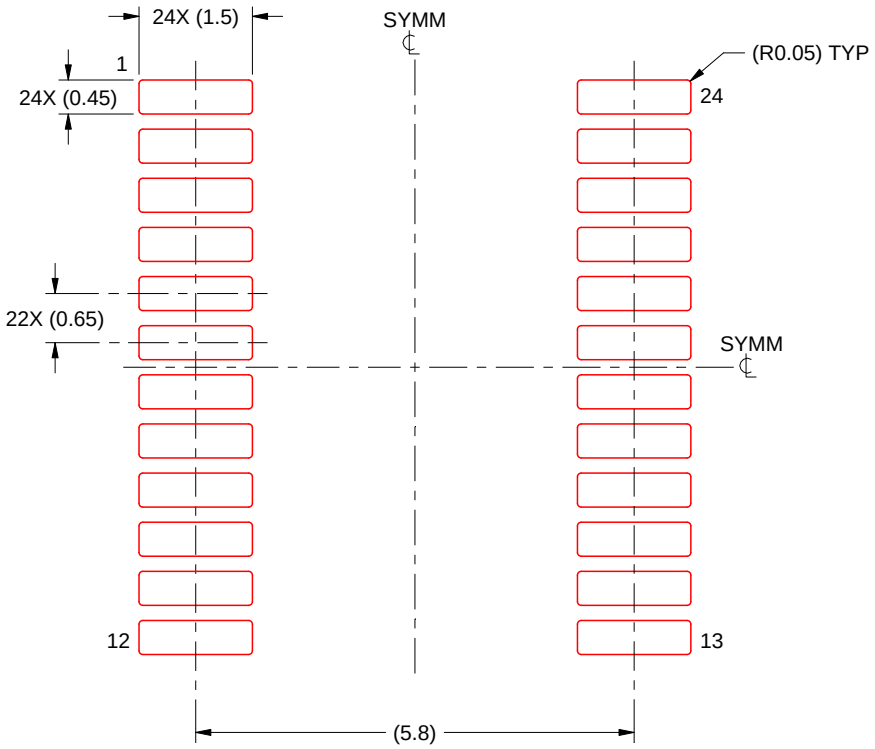


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月