

UCC27324-Q1 デュアル、4A ピーク、高速ローサイド・パワー MOSFET ドライバ

1 特長

- 車載アプリケーション向けに認定済み
- 業界標準のピン配置
- ミラー・プラトー領域で $\pm 4A$ の大電流駆動能力
- 低電源電圧でも高効率の定電流供給
- 電源電圧から独立した TTL/CMOS 互換入力
- 標準立ち上がり時間 20ns、標準立ち下がり時間 15ns (1.8nF 負荷時)
- 標準伝播遅延時間: 25ns (入力立ち下がり時)、35ns (入力立ち上がり時)
- 電源電圧: 4V~15V
- 電源電流: 0.3mA
- 2つの出力を並列に使用することで、より高い駆動電流を実現可能
- $T_J = -40^\circ\text{C} \sim 125^\circ\text{C}$ で仕様を規定
- TrueDrive™ 出力アーキテクチャ、バイポーラおよび CMOS トランジスタを並列に使用

2 アプリケーション

- スイッチ・モード電源
- DC/DC コンバータ
- モーター・コントローラ
- ライン・ドライバ
- Class-D スwitching・アンプ

3 概要

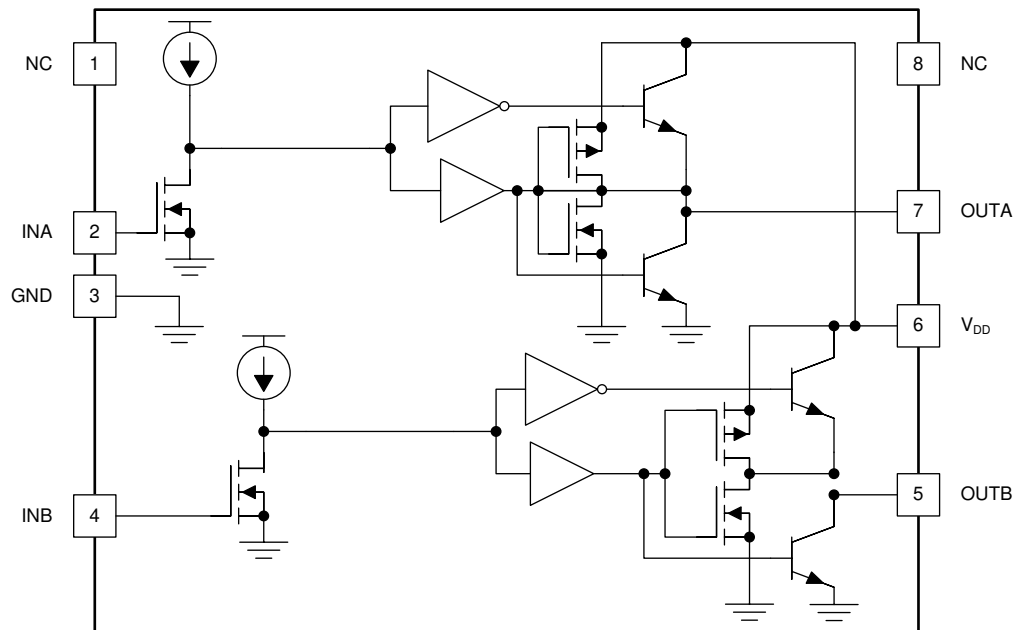
UCC27324-Q1 高速デュアル MOSFET ドライバは、容量性負荷に大きなピーク電流を供給できます。本質的に貫通電流を最小限に抑える設計により、MOSFET のスイッチング遷移中のミラー・プラトー領域で最も必要とされる 4A の電流を供給します。また、独自のバイポーラおよび MOSFET の並列ハイブリッド出力段により、低い電源電圧でも高効率の電流ソース/シンクを実現します。

本デバイスは、標準の SOIC-8 (D) パッケージで供給されます。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
UCC27324-Q1	SOIC (8)	4.90mm × 3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



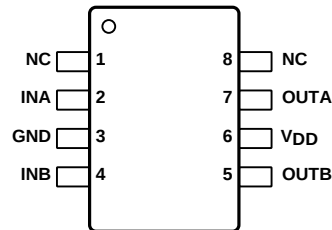
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4 Pin Configuration and Functions



NC – No internal connection

☒ 4-1. D Package 8-Pin SOIC Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	No connection. Should be grounded.
2	INA	I	Input A. Input signal of the A driver. Has logic-compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
3	GND	—	Common ground. Should be connected very closely to the source of the power MOSFET that the driver is driving.
4	INB	I	Input B. Input signal of the B driver. Has logic-compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
5	OUTB	O	Driver output B. The output stage can provide 4-A drive current to the gate of a power MOSFET.
6	V_{DD}	I	Supply. Supply voltage and the power input connection for this device.
7	OUTA	O	Driver output A. The output stage can provide 4-A drive current to the gate of a power MOSFET.
8	NC	—	No connection. Should be grounded.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{DD}	Supply voltage	-0.3	16	V
I _O	Output current (OUTA, OUTB)	DC, I _{OUT_DC}	0.3	A
		Pulsed (0.5 μs), I _{OUT_PULSED}	4.5	
T _J	Junction operating temperature	-55	150	°C
T _{lead}	Lead temperature		300	°C
T _{stg}	Storage temperature, soldering, 10 s	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	4		15	V

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC27324-Q1		UNIT
		D (SOIC)		
		8 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	113		°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	61.7		°C/W
R _{θJB}	Junction-to-board thermal resistance	53.2		°C/W
ψ _{JT}	Junction-to-top characterization parameter	16		°C/W
ψ _{JB}	Junction-to-board characterization parameter	52.7		°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—		°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Overall Electrical Characteristics

V_{CC} = 4.5 V to 15 V, T_A = -40°C to 125°C (unless otherwise noted), T_A = T_J

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{DD}	INA = 0 V	INB = 0 V		2	80	μA
		INB = HIGH		300	450	
	INA = HIGH	INB = 0 V		300	450	
		INB = HIGH		600	800	

5.6 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Power dissipation	$T_A = 25^\circ\text{C}$		650	mW	μA

5.7 Input (INA, INB) Electrical Characteristics

$V_{CC} = 4.5\text{ V to }15\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} Logic 1 input threshold		1.6	2.2	2.5	V
V_{IL} Logic 0 input threshold		1.8	2.7	3.5	V
Input current	$0\text{ V} \leq V_{IN} \leq V_{DD}$	-10	0	10	μA

5.8 Output (OUTA, OUTB) Electrical Characteristics

$V_{CC} = 4.5\text{ V to }15\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output current ⁽¹⁾	$V_{DD} = 14\text{ V}$		4		A
R_{OH} Output resistance high ⁽²⁾	$I_{OUT} = -10\text{ mA}$		0.6	1.5	Ω
R_{OL} Output resistance low ⁽²⁾	$I_{OUT} = 10\text{ mA}$		0.4	1	Ω

- (1) Parameter not tested in production
- (2) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure.

5.9 Switching Characteristics

$V_{CC} = 4.5\text{ V to }15\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted) (see [Figure 5-1](#))

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R Rise time (OUTA, OUTB)	$C_{LOAD} = 1.8\text{ nF}$		20	40	ns
t_F Fall time (OUTA, OUTB)	$C_{LOAD} = 1.8\text{ nF}$		15	40	ns
t_{D1} Delay time, IN rising (IN to OUT)	$C_{LOAD} = 1.8\text{ nF}$		25	40	ns
t_{D2} Delay time, IN falling (IN to OUT)	$C_{LOAD} = 1.8\text{ nF}$		35	50	ns

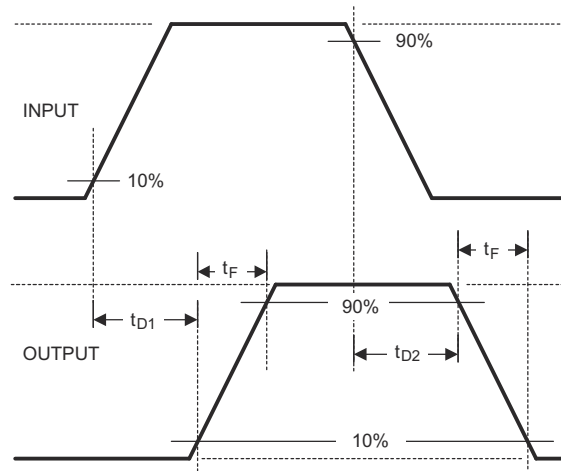
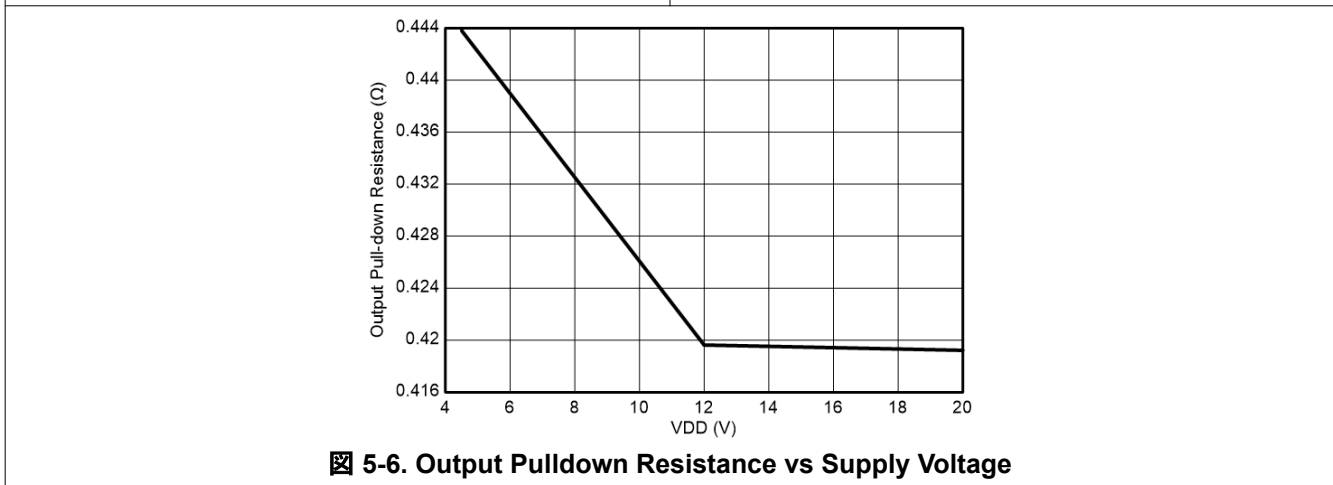
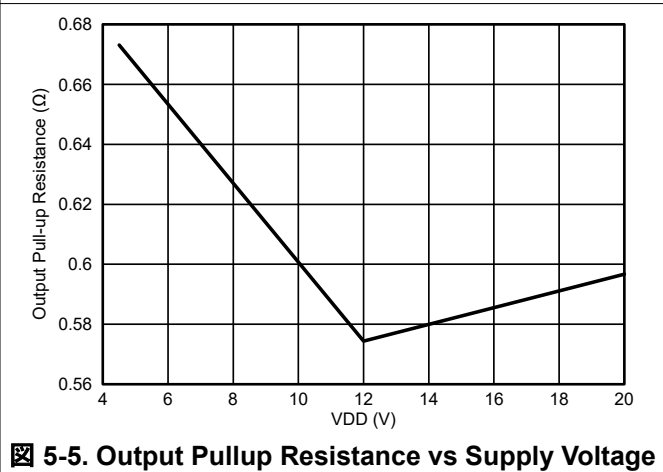
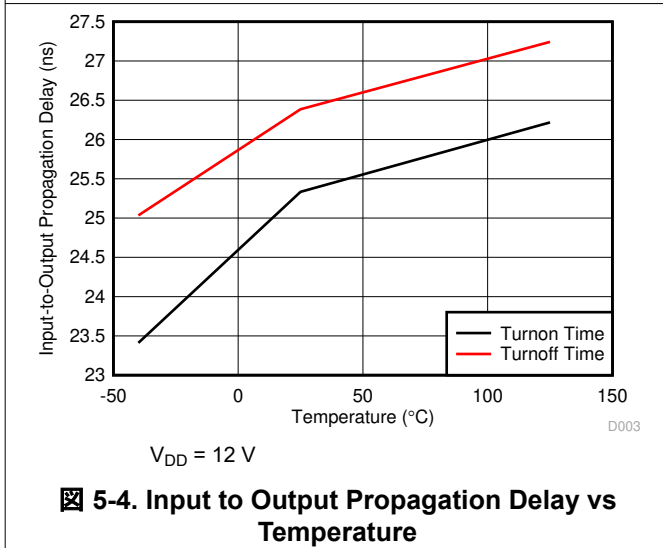
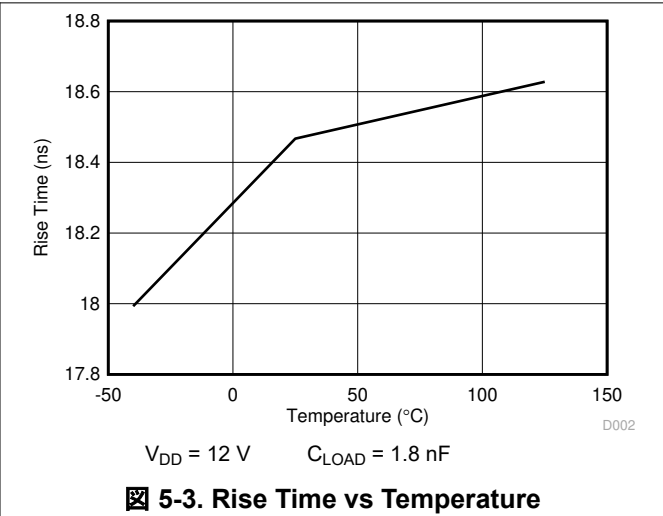
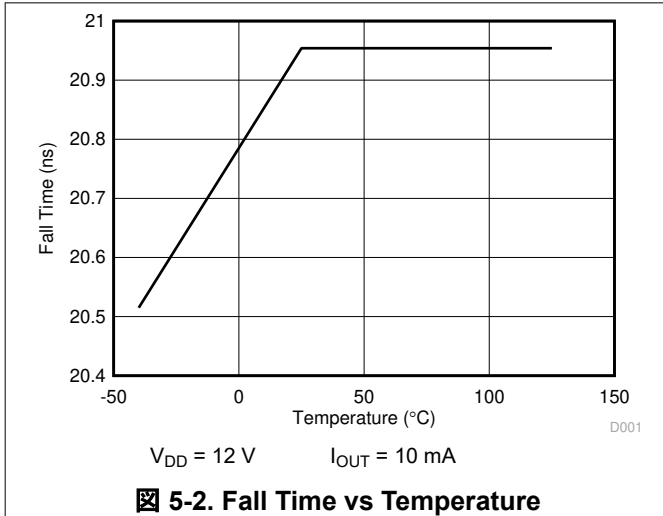


Figure 5-1. Switching Waveforms for Noninverting Driver

5.10 Typical Characteristics

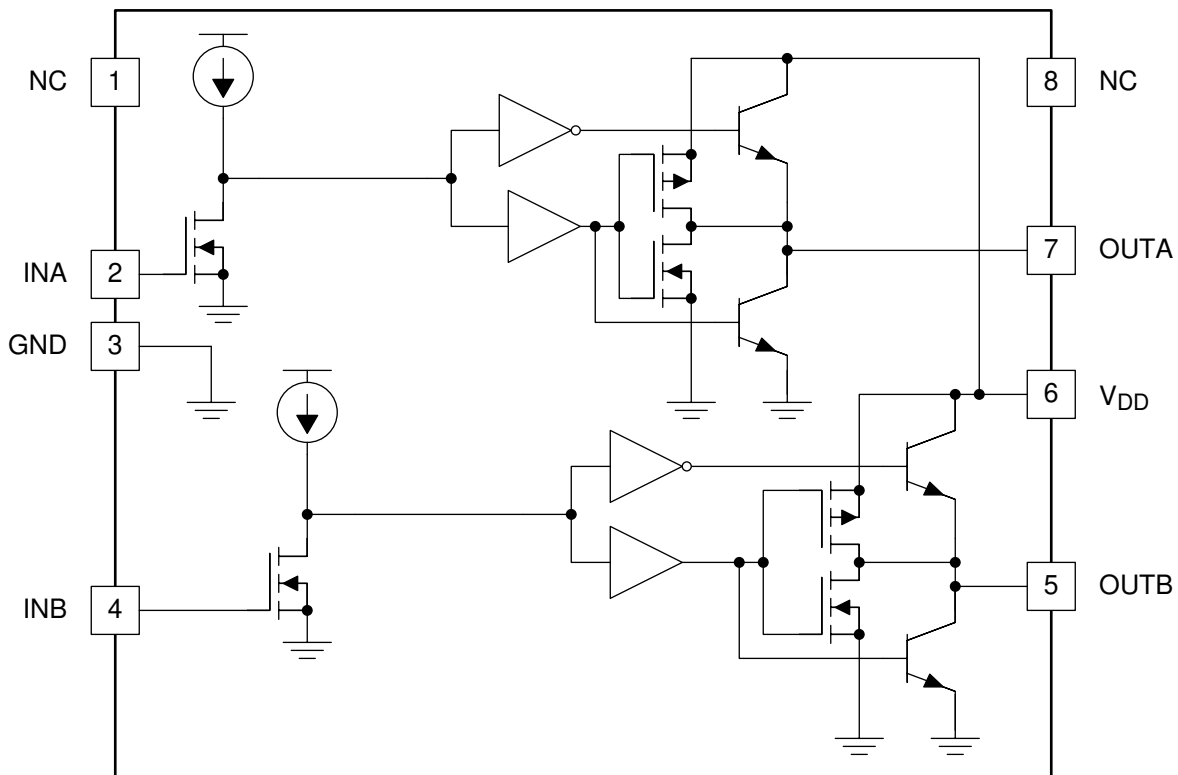


6 Detailed Description

6.1 Overview

The UCC27324-Q1 device represents Texas Instruments' latest generation of dual-channel, low-side, high-speed gate-driver devices featuring a 4-A source and sink capability. With industry leading switching characteristics, automotive qualification, and a host of other features shown on the first page, the UCC27324-Q1 provides an efficient, robust, and reliable solution to your high current low-side driver needs in automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltage, yet it is equally compatible with 0 V to V_{DD} signals.

The inputs of UCC27324-Q1 device are designed to withstand 500-mA reverse current without damage to the device or logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor also may help remove power dissipation from the device package, as discussed in the [セクション 9.3](#) section.

6.3.2 Output Stage

Noninverting outputs of the UCC27324-Q1 are intended to drive external N-channel MOSFETs.

Each output stage is capable of supplying ± 4 -A peak current pulses and swings to both V_{DD} and GND. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot, due to the body diode of the external MOSFET. This means that, in many cases, external Schottky-clamp diodes are not required.

The UCC27324-Q1 device delivers a 4-A gate drive when it is most needed during the MOSFET switching transition—at the Miller plateau region—providing improved efficiency gains. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

6.4 Device Functional Modes

表 6-1 lists the device functions.

表 6-1. Function Table

INPUTS		UCC27324-Q1 OUTPUTS	
INA	INB	OUTA	OUTB
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

High-frequency power supplies often require high-speed high-current drivers such as the UCC27324-Q1 device. A leading application is the need to provide a high-power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver is used to drive the power device gates through a drive transformer. Synchronous rectification supplies must also simultaneously drive multiple devices, which can present an extremely large load to the control circuitry.

Drivers are used when using the primary PWM regulator to directly drive the switching devices is not feasible for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, minimizing the effect of high-frequency switching noise by placing the high-current driver physically close to the load may be necessary. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. The PWM outputs are intended to drive only the high-impedance input to a driver such as the UCC27324-Q1. Finally, the control device may be under thermal stress because power dissipation, and an external driver can help by moving the heat from the controller to an external package.

7.1.1 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together (respectively). Then, a single signal can control the paralleled combination as shown in [Figure 7-1](#).

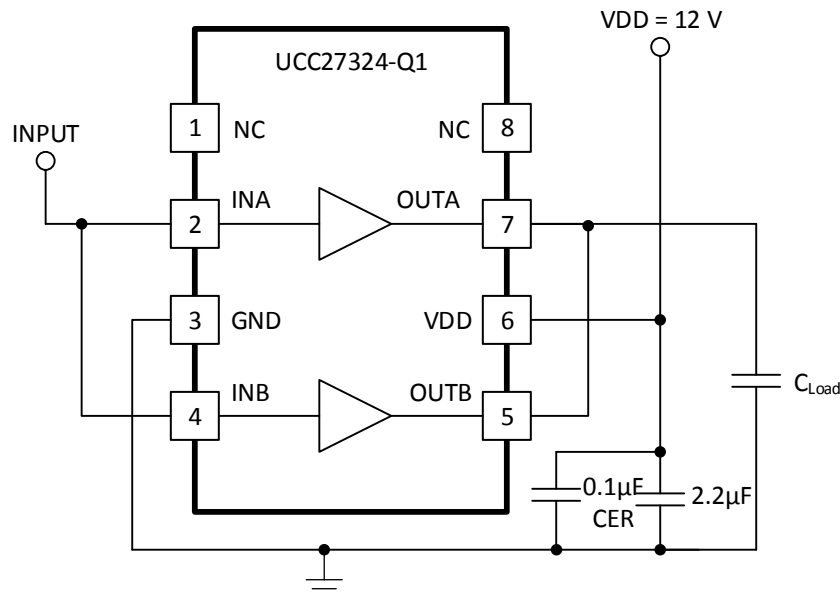


図 7-1. Combined Input and Output Configuration

7.2 Typical Application

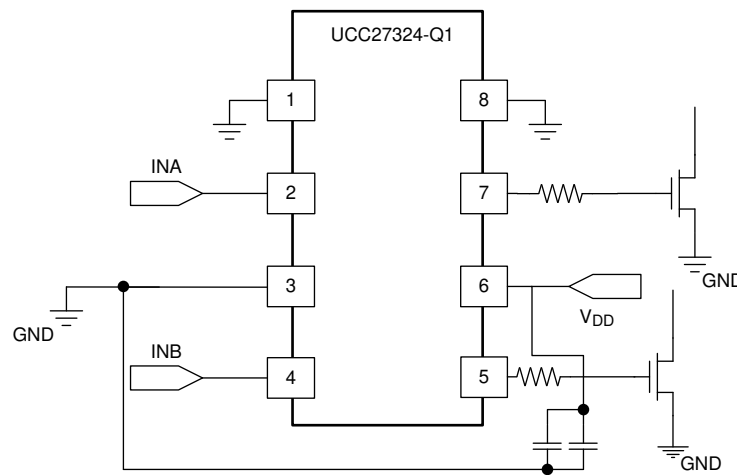


図 7-2. Typical Application Schematic

7.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. These design considerations include V_{DD} , drive current, and power dissipation.

7.2.2 Detailed Design Procedure

7.2.2.1 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27324-Q1 device features fast 25-ns propagation delays which ensures very little pulse distortion and allows operation at high frequencies. See the [クシヨシ 5.9](#) table for the propagation and switching characteristics of the UCC27324-Q1 device.

7.2.2.2 Source and Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC27324-Q1 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging or discharging of the drain-gate capacitance with current supplied or removed by the driver.

Two circuits are used to test the current capabilities of the UCC27324-Q1 driver. In each case, external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period when the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in [図 7-3](#) is used to verify the current sink capability when the output of the driver is clamped at approximately 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC27324-Q1 is found to sink 4.5 A at $V_{DD} = 15$ V and 4.28 A at $V_{DD} = 12$ V.

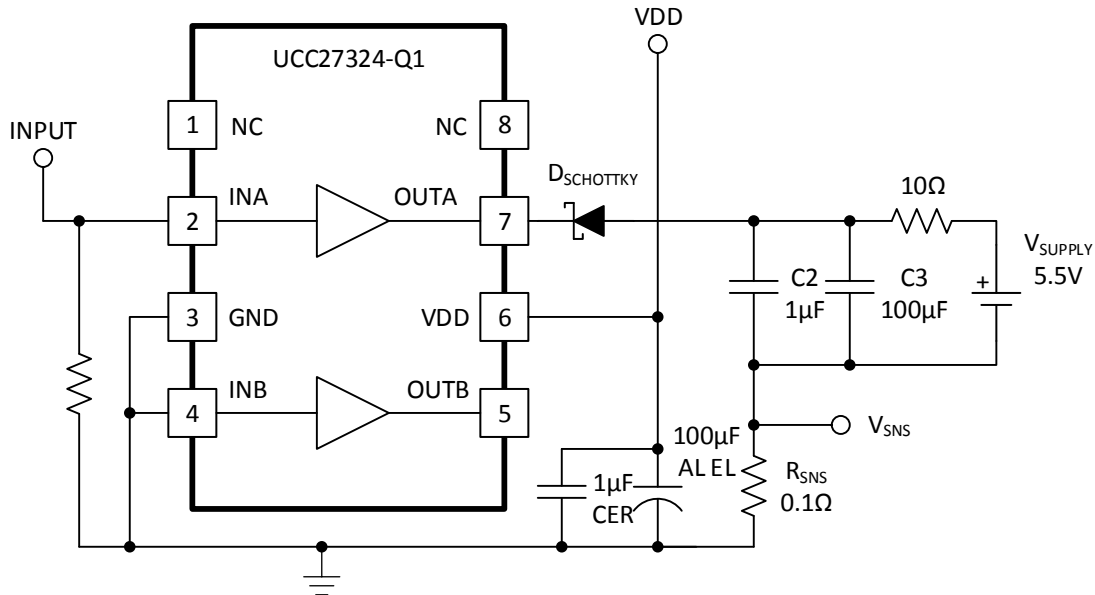


図 7-3. Current Sink Test Circuit

The circuit in 図 7-4 is used to test the current source capability with the output clamped to approximately 5 V with a string of Zener diodes. The UCC27324-Q1 device can source 4.8 A at $V_{DD} = 15$ V and 3.7 A at $V_{DD} = 12$ V.

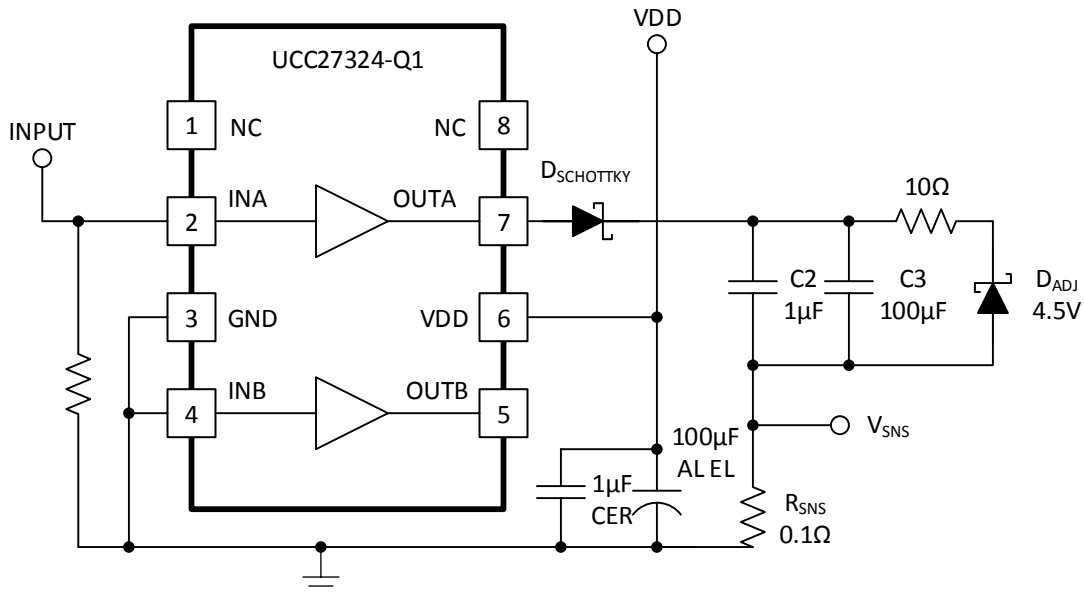


図 7-4. Current Source Test Circuit

注

The current-sink capability is slightly stronger than the current source capability at lower V_{DD} because of the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications, the fact that the turn-off capability of a driver is stronger than the turn-on capability is advantageous which helps to ensure that the MOSFET is held off during common power-supply transients that may turn the device back on.

7.2.2.3 Supply Voltage (V_{DD})

Although quiescent V_{DD} current is very low, total supply current is higher, depending on the OUTA and OUTB current and the programmed oscillator frequency. The total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. With the known operating frequency and the MOSFET gate charge (Q_g), use 式 1 to calculate the average OUT current.

$$I_{OUT} = Q_g \times f \quad (1)$$

where

- f is frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1- μ F ceramic capacitor must be located closest to the V_{DD} to ground connection. In addition, a larger capacitor (such as 1- μ F) with relatively low ESR must be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors must present a low impedance characteristic for the expected current levels in the driver application

7.2.2.4 Drive Current and Power Requirements

The UCC27324-Q1 drivers are capable of delivering 4 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to quickly turn on the device. Then, to turn off the device, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion, because it is the most common type of switching device used in high-frequency power-conversion equipment.

Reference [1] in the セクション 10.2.1 section discuss the current required to drive a power MOSFET and other capacitive-input switching devices and includes information on the previous generation of bipolar gate drivers.

When a driver is tested with a discrete capacitive load, calculating the power that is required from the bias supply is fairly simple. Use 式 2 to calculate the energy that must be transferred from the bias supply to charge the capacitor.

$$E = \frac{1}{2}CV^2 \quad (2)$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver

An equal amount of energy transferred to ground when the capacitor is discharged which leads to power loss. Use 式 3 to calculate this power loss.

$$P = 2 \times \frac{1}{2}CV^2f \quad (3)$$

where

- f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

Use 式 4 to calculate the power loss with the following values: $V_{DD} = 12$ V, $C_{LOAD} = 10$ nF, and $f = 300$ kHz.

$$P = 10 \text{ nF} \times (12)^2 \times (300 \text{ kHz}) = 0.432 \text{ W} \quad (4)$$

For a 12-V supply, use 式 5 to calculate the current

$$I = P / V = 0.432 \text{ W} / 12 \text{ V} = 0.036 \text{ A} \quad (5)$$

The actual current measured from the supply was 0.037 A, which is very close to the predicted value. But, the I_{DD} current that is due to the internal consumption should be considered. With no load, the current draw is 0.0027 A. Under this condition, the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high-frequency switching spikes and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to the expected value.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the on and off states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g , one can determine the power that must be dissipated when charging a capacitor. Use 式 6 and the equivalence $Q_g = C_{eff}V$ to calculate this power.

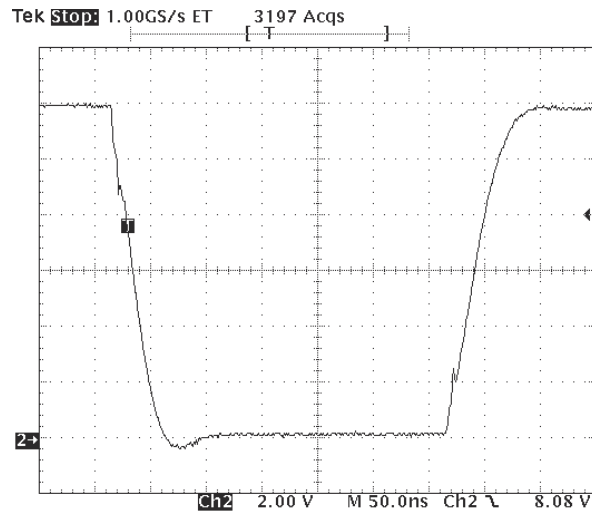
$$P = C \times V^2 \times f = V \times Q_g \times f \quad (6)$$

式 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

7.2.3 Application Curve

☒ 7-5 shows the circuit performance achievable with a single driver (half of the 8-pin device) driving a 10-nF load. The input pulse width (not shown) is set to 300 ns to show both transitions in the output waveform. The rising and falling edges of the switching waveforms are fairly linear which is because of the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

Sink and source currents of the driver are dependent upon the V_{DD} value and the output capacitive load. The larger the V_{DD} value the higher the current capability, and the larger the capacitive load the higher the current sink/source capability. Trace resistance and inductance, including wires and cables for testing, slows down the rise and fall times of the outputs which reduces the current capabilities of the driver. To achieve higher current results, reduce resistance and inductance on the board as much as possible and increase the capacitive output load value to swap out the effect of the inductance values.



7-5. Single Driver With 10-nF Load, 300-ns Pulse-Width Input

8 Power Supply Recommendations

The bias supply voltage range for which the UCC27324-Q1 device is rated to operate is from 4 V to 15 V. A quiet, robust power supply capable of delivering at least 4 A should be used to ensure proper operation of the device.

9 Layout

9.1 Layout Guidelines

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1- μF ceramic capacitor should be located closest to the V_{DD} to ground connection. In addition, a larger capacitor (such as 1- μF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low-impedance characteristic for the expected current levels in the driver application.

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high $\Delta i/\Delta t$. This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver as close as possible to the leads. The driver layout has ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections also should be made with a small enclosed loop area to minimize the inductance.

PCB layout is a critical step in the production process in high-current fast-switching circuits to ensure appropriate operation and design robustness. The UCC27324-Q1 MOSFET driver is capable of delivering large current peaks with rapid rise and fall times at the gate of a power MOSFET to facilitate voltage transitions quickly. At higher V_{DD} voltages, the peak current capability is even higher. High di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled.

- Locate the driver device as close as possible to the power device in order to minimize the length of high-current traces between the output pins and the gate of the MOSFET being driven.
- Locate the V_{DD} bypass capacitors between V_{DD} and GND as close as possible to the driver with minimal trace length to improve the noise filtering. Place these capacitors as close to each other as is allowed, as shown by C1 and C2 in [Figure 9-1](#) which ensures minimal trace inductance and gives the effect of a *capacitor bank*. These capacitors support high peak current being drawn from V_{DD} during turn-on of the power MOSFET. The use of low inductance surface mount components is highly recommended.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected the other circuit nodes such as the source of the power MOSFET and ground of the PWM controller at one single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead, the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help with thermal protection.
- Tie pins 1 and 8 to GND to eliminate any chance of noise causing malfunction on a floating node.

9.2 Layout Example

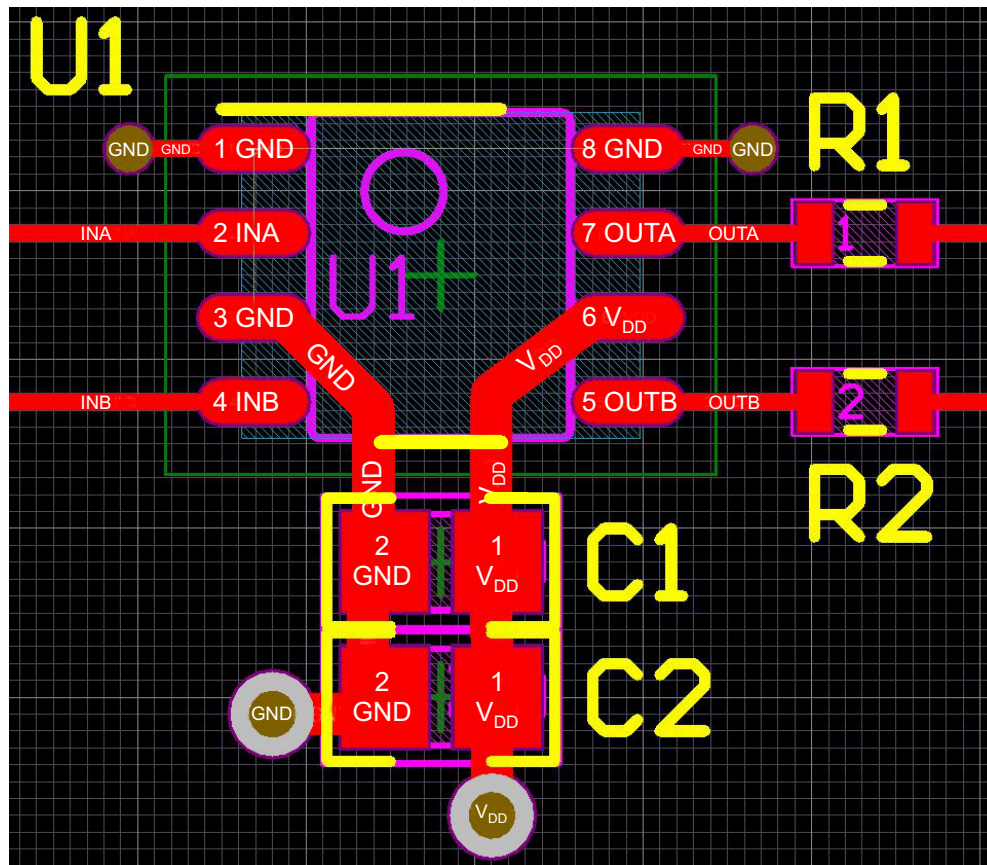


図 9-1. UCC27324-Q1 Layout Example

9.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC27324-Q1 device of drivers is available in three different packages to cover a range of application requirements.

As shown in [セクション 5.4](#), the SOIC-8 (D) package has power ratings of approximately 0.5 W at $T_A = 70^\circ\text{C}$. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in our earlier example is 0.432 W with a 10-nF load, 12-V V_{DD} , switched at 300 kHz. Thus, only one load of this size could be driven using the D or P package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

1. *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, Bill Andreyckak, [SLUA105](#)
2. *PowerPAD Thermally Enhanced Package*, [SLMA002](#)
3. *PowerPAD Made Easy*, [SLMA004](#)

10.3 ドキュメントの更新通知を受け取る方法

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10.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (June 2018) to Revision D (November 2023)	Page
• Changed input threshold voltage values in Input (INA, INB) Electrical Characteristics.....	5
• Deleted V_{OH} output high level and V_{OL} output low level, changed output resistance high and output resistance low values and deleted Latch-up protection in Output (OUTA, OUTB) Electrical Characteristics.....	5
• Changed title on 図 5-2 and changed 図 5-5 and 図 5-6	6
Changes from Revision B (September 2015) to Revision C (June 2018)	Page
• Changed Figures 8,10,11 to show non-inverting device internally.....	10
• Added to equation 6 to correctly multiply by V.	12
Changes from Revision A (April 2012) to Revision B (September 2015)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• データシートから UCC27323 -Q1 (デュアル反転) および UCC27325 -Q1 (反転 × 1、非反転 × 1) デバイスを削除	1
• UCC27324-Q1 デバイスの MSOP-PowerPAD パッケージおよび PDIP パッケージへの参照を削除.....	1
• 「注文情報」表を削除	1
• Deleted <i>Dissipation Ratings</i> table	4
Changes from Revision * (March, 2008) to Revision A (April, 2012)	Page
• Added $T_A = T_J$ to header of Overall Electrical Characteristics table.....	4
• Added an extra paragraph before Figure 5.....	13

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27324QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UCC27324-Q1 :

- Catalog : [UCC27324](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27324QDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27324QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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