

Application Note

ESD Packaging and Layout Guide



ABSTRACT

Electrostatic discharge (ESD) protection is essential on a system-level design for a wide range of end-equipment in consumer, industrial, and automotive spaces. One ESD strike to an unprotected system could cause permanent damage to the overall system. By splitting into three sections, this guide helps with selecting the proper transient voltage suppressor (TVS) for ESD protection in a system design. The first section helps define the key parameters for ESD devices. The second section offers tips for printed circuit board (PCB) layout designs. The last section provides TI ESD devices that are categorized by the package types, allowing a quick selection process for ESD devices based on the package and footprint.

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1 Definitions of ESD Device Specifications

1.1 Working Voltage (V_{RWM})

The working voltage is the recommended operating voltage range of the device. The signal voltage of the application should not be operating outside of the working voltage of the ESD device. Exceeding the working voltage in either negative or positive range will lead to unwanted clamping and leakage, damaging the device and system.

1.2 Capacitance

ESD devices introduce some parasitic capacitance to the system because the ESD diodes are connected in parallel to the signal trace. For high-speed interfaces, it is important to minimize the capacitance to maintain signal integrity.

1.3 IEC 61000-4-2 Rating

The IEC61000-4-2 rating consists of the contact rating and the air-gap rating that shows the robustness of the ESD device. The contact rating is the maximum voltage that an ESD device can withstand when the source discharges directly onto the device. The air-gap rating is the maximum voltage that an ESD device can withstand when the source discharges over a gap of air onto the device. The IEC61000-4-2 rating is designed for real world applications and is split into 4 levels. A higher IEC 61000-4-2 rating correlates to a higher voltage that the ESD device can withstand.

1.4 Channels

ESD devices are available in single and multiple channels. Depending on the application, a multi-channel device might offer a smaller solution size and save board space since it would consolidate multiple single-channel devices. Conversely, a single-channel device might offer more design flexibility.

1.5 Unidirectional vs. Bidirectional

A bidirectional ESD diode has both a negative and a positive working voltage range, generally from -3.6 V to 3.6 V or -5.5 V to 5.5 V . This allows for the bidirectional ESD device to function with the interfaces whose data signals toggle between positive and negative voltages. A unidirectional ESD only has a positive working voltage range while having better negative clamping.

For more information on application-specific ESD devices, see the [System-Level ESD Protection Guide](#).

2 ESD Layout Tips

2.1 Optimizing Impedance for Dissipating ESD

When designing a circuit to dissipate ESD, inductance is an important parasitic to consider. Based on the parasitic inductance, a change in current would cause a change in the overall voltage, destabilizing the overall board performance. [Figure 2-1](#) shows four parasitic inductances between the ESD source and the transient voltage suppressor (TVS) or ESD diodes.

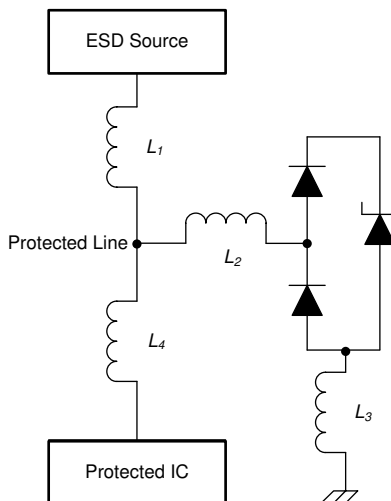


Figure 2-1. PCB Inductance Around a Single-Channel TVS

In a well-designed system, any inductance is minimized between the ESD source and the path to ground through the TVS. Use the following 5 layout tips to minimize inductance:

1. Minimize any inductance between the ESD source and the path to ground through the TVS
2. Place the TVS as close to the ESD source or connector as design rules allow
3. Place the protected IC much further from the TVS than the TVS is to the connector. Following tips 2 and 3 will ensure $L_4 \gg L_1$, *steering* the I_{ESD} towards TVS. Minimizing L_1 is further covered in [Section 2.2](#) and [Section 2.3](#).
4. Do not use L_2 stubs between the TVS and the protected line. Route directly from the ESD source to the TVS. In a well-designed system, L_2 should not be present. Please avoid design practices that introduce inductance between the protected line and the TVS.
5. Minimize L_3 inductance between the TVS and ground, which is further covered in [Section 2.4](#). This inductance is the most predominant parasitic influencing the overall V_{ESD} .

2.2 Limiting EMI From ESD

Without proper steps for suppression, fast transients such as ESD with high di/dt can cause electromagnetic interference (EMI). [Figure 2-2](#) shows that the primary source of radiation occurs between the ESD source and the TVS.

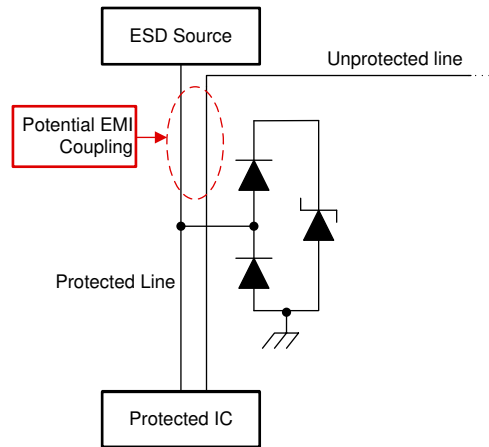


Figure 2-2. EMI Coupling Onto an Adjacent Unprotected Trace

Even without inductance L1 from [Figure 2-1](#), the rapidly changing electric field during ESD can affect nearby circuits. Having any L1 would further amplify the EMI. The PCB designer should avoid any design practices in this region with unprotected PCB traces. In an ESD event, the potential EMI coupling with an unprotected line could damage the system by having direct contact with an IC or carrying the EMI further into the system. Use these 4 tips to limit EMI:

1. Do not route unprotected circuits in the area between the ESD source and the TVS
2. Place the TVS as close to the ESD source or connector as design rules allow
3. Route with straight traces between the ESD source and the TVS, if possible
4. If corners must be used, curves are preferred and a maximum of 45° is acceptable

2.3 Routing With VIAs

It is strongly recommended to route traces on the PCB from the ESD source to TVS without switching layers by VIA. [Figure 2-3](#) shows three cases of routing with VIAs.

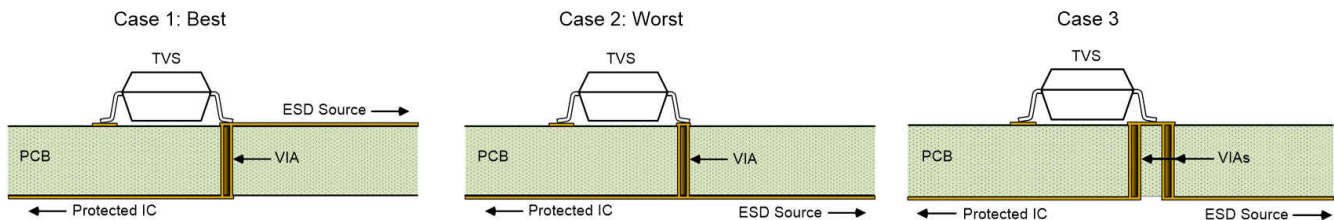


Figure 2-3. Routing With VIAs

If VIA is required between the ESD source and the protected IC, Case 1 is the preferred method, Case 2 should be avoided, and Case 3 is acceptable if there is no alternative. In Case 1, I_{ESD} is forced to the TVS protection pin before passing through VIA to the protected IC. The VIA correlates to L4 in [Figure 2-1](#). In Case 2, I_{ESD} branches between the protected IC and VIA to the TVS protection pin. The VIA correlates to L2 in [Figure 2-1](#). This practice should be avoided as the protected IC can take the brunt of the current during an ESD event. In Case 3, I_{ESD} is forced to the protection pin of the TVS before passing to the protected IC. Use these 2 tips when routing with VIAs:

1. Avoid VIAs between the ESD source and TVS
2. If VIA is required between the ESD source and the protected IC, route directly from the ESD Source to the TVS before using the VIA

2.4 Optimizing Ground Schemes for ESD

For TVS, having a very low impedance path to ground is very important. Eliminating all the parasitic inductances between the ESD source and the TVS will only be effective if the TVS is optimally grounded. [Figure 2-4](#) shows the ground pad of a TVS connected to the top layer ground plane.

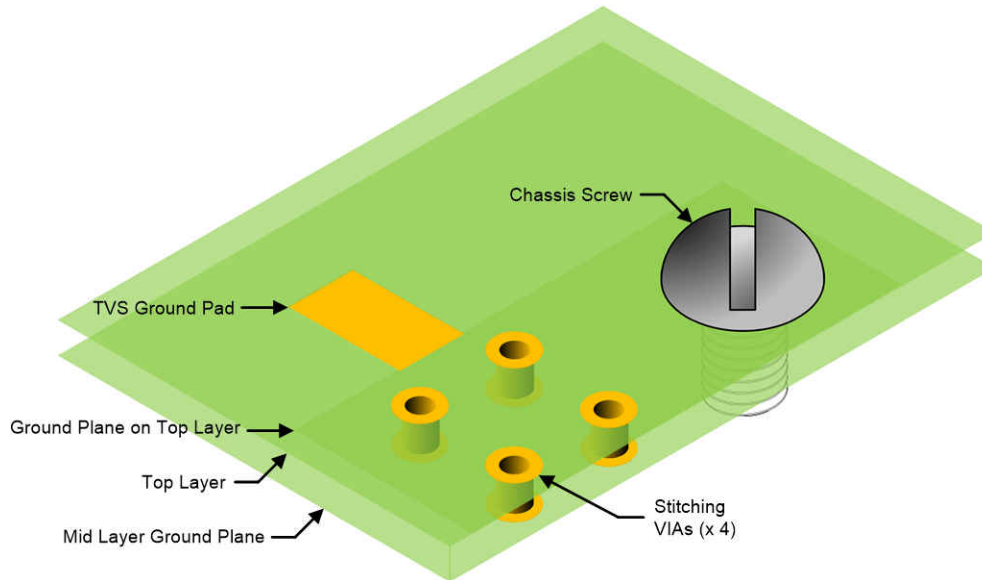


Figure 2-4. Two Layer PCB - Top Ground Plane Stitched to a Mid-layer Ground Plane

The TVS ground pin should connect to a same layer ground plane that is coupled with another ground plane on an immediately adjacent layer. These ground planes should be stitched together with VIAs, with one VIA immediately adjacent to the ground pin of the TVS. Use the following tips to optimize the grounding scheme with very low impedance:

1. Connect the TVS ground pin directly to a same layer ground plane that has nearby VIAs stitching to an adjacent internal ground plane
2. Use multiple ground planes when possible
3. Use a grounded chassis screw to connect the PCB ground and position it near the TVS and ESD source as the connector ground shield
4. Use VIAs of large diameter with a large drill, which lowers impedance

For more detailed explanations, see the [ESD Protection Layout Guide Application Report](#).

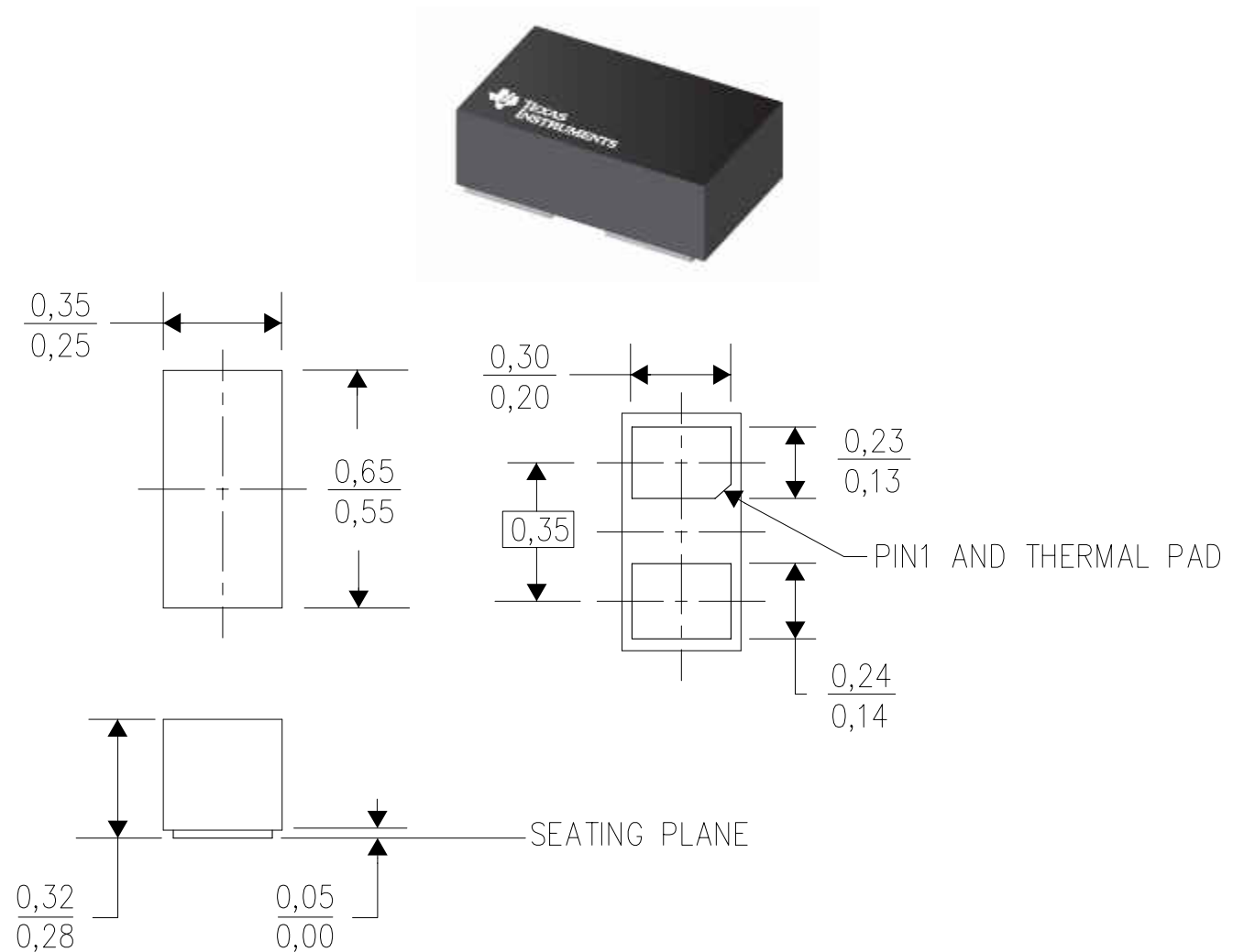
3 ESD Solutions by Package Types

Not all devices in the same package type have the same pin outs. See the data sheet of each device for details.

3.1 0201 2-pin SON (TI: DPL) | 0.6 mm x 0.3 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD1E0B04	1	bidirectional	±3.6	0.13	8
TPD1E01B04 (Q1)	1	bidirectional	±3.6	0.18	15
TPD1E04U04	1	bidirectional	±3.6	0.5	16
ESD341	1	bidirectional	±3.6	0.66	30
TPD1E6B06	1	bidirectional	±5	6	15

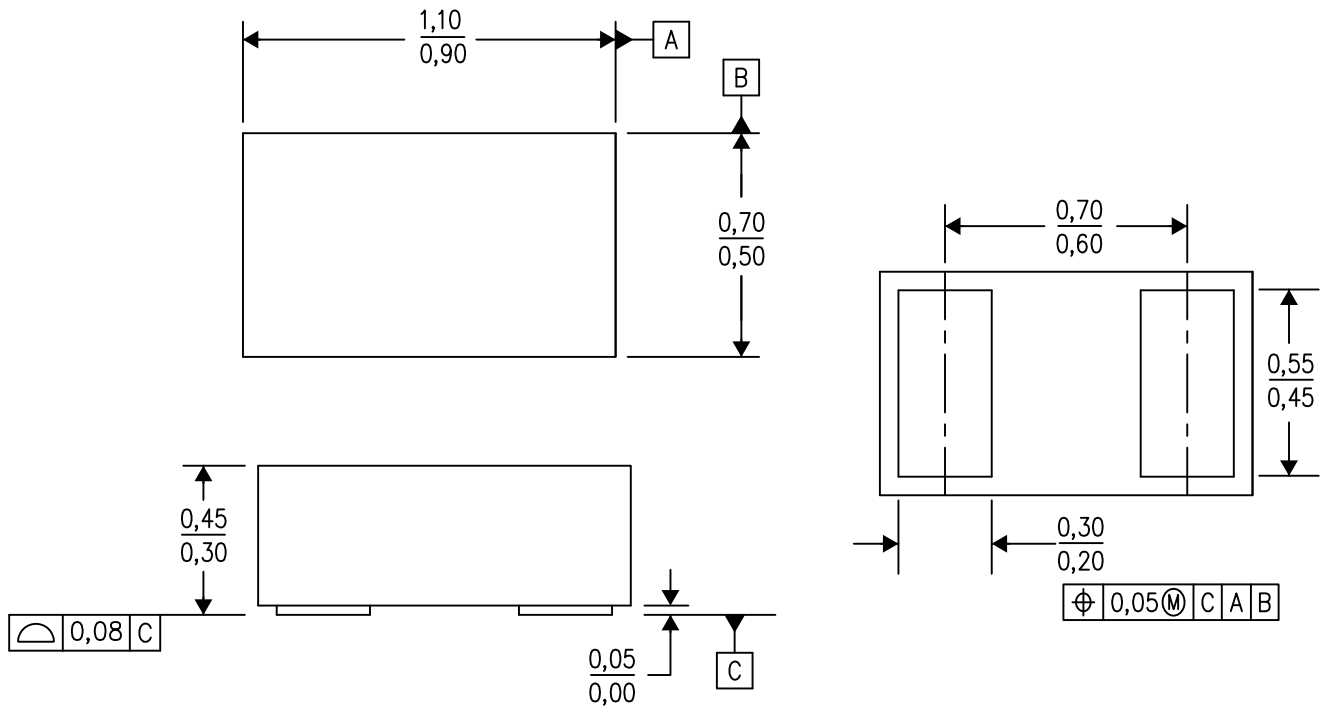
[Link to Package Drawing](#)



3.2 0402 2-pin SON (TI: DPY) | 1.0 mm × 0.6 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD1E0B04	1	bidirectional	±3.6	0.13	8
TPD1E01B04 (Q1)	1	bidirectional	±3.6	0.18	15
ESD321	1	unidirectional	3.6	0.9	30
TPD1E1B04	1	bidirectional	±3.6	1	30
TPD1E05U06 (Q1)	1	unidirectional	5.5	0.4	12
ESD401	1	bidirectional	±5.5	0.77	24
TPD1E10B06 (Q1)	1	bidirectional	±5.5	12	30
TPD1E10B09 (Q1)	1	bidirectional	±9	10	20

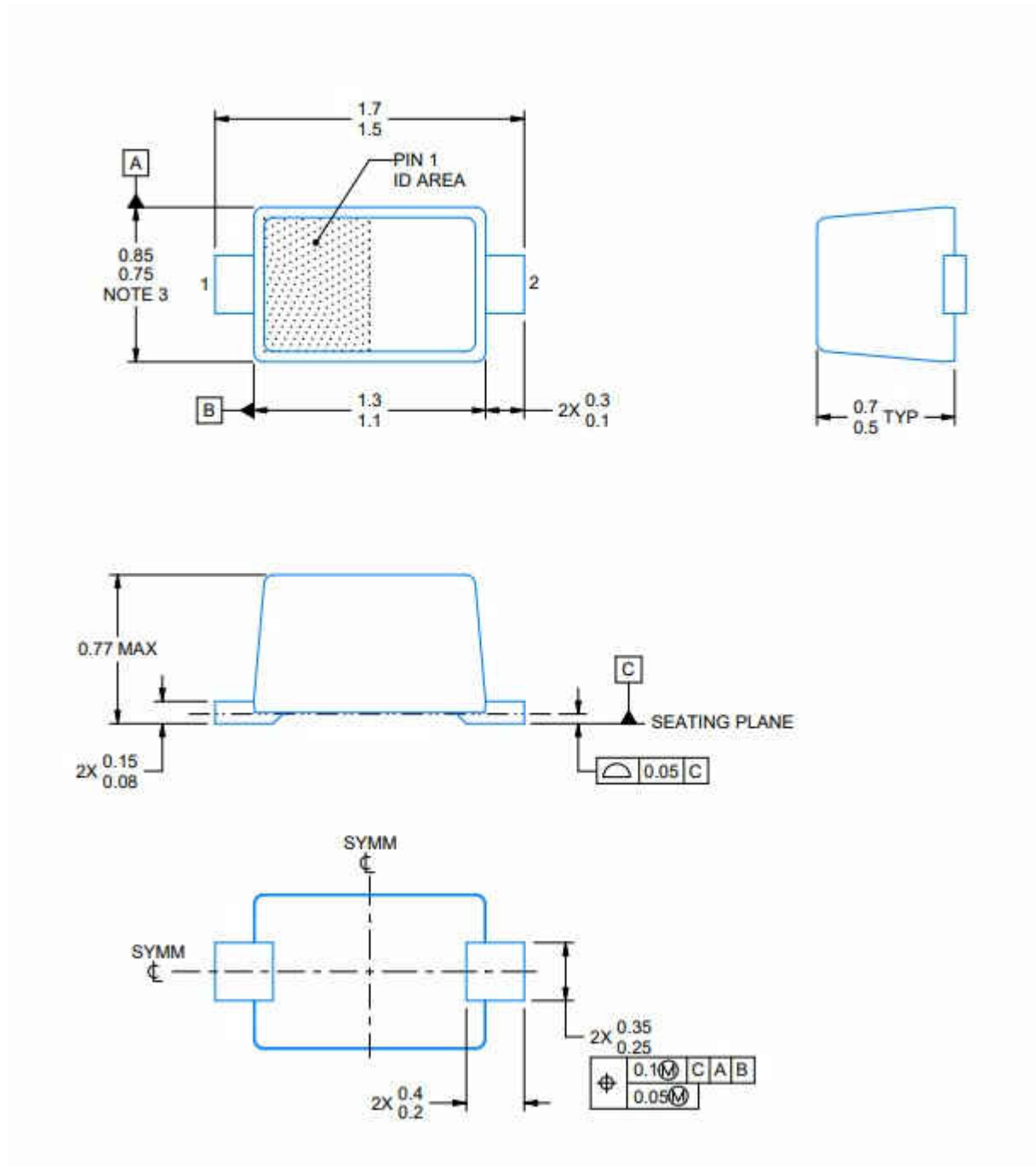
[Link to Package Drawing](#)



3.3 2-pin SOD-523 (TI: DYA) | 1.2 mm x 0.8 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD1E05U06	1	unidirectional	5.5	0.4	12
TPD1E10B06 (Q1)	1	bidirectional	±5.5	12	30

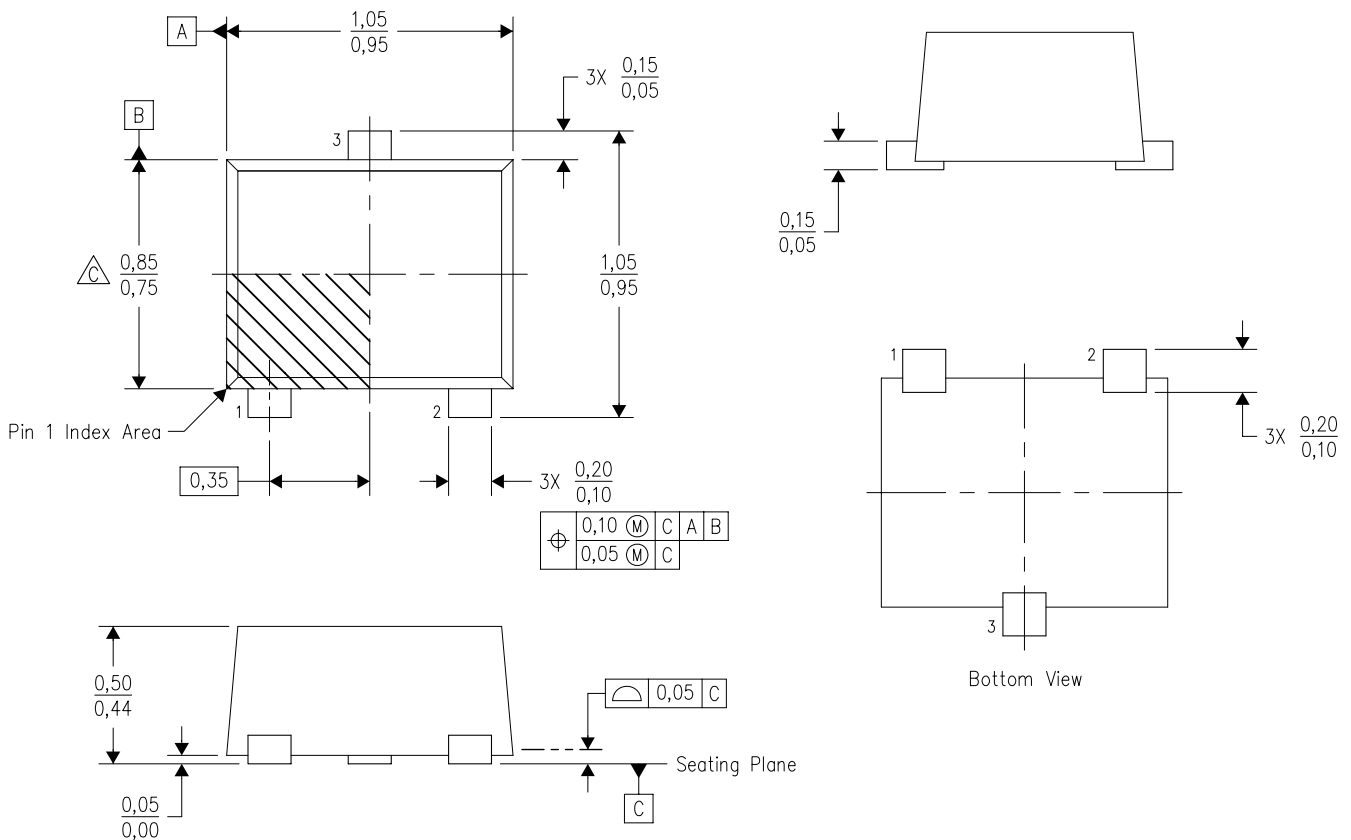
[Link to Package Drawing](#)



3.4 3-pin SOT-9X3 (TI: DRT) | 1 mm × 1 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD2EUSB30A	2	unidirectional	3.6	0.7	8
TPD2EUSB30	2	unidirectional	5.5	0.7	8
TPD2E009	2	unidirectional	5.5	0.7	8

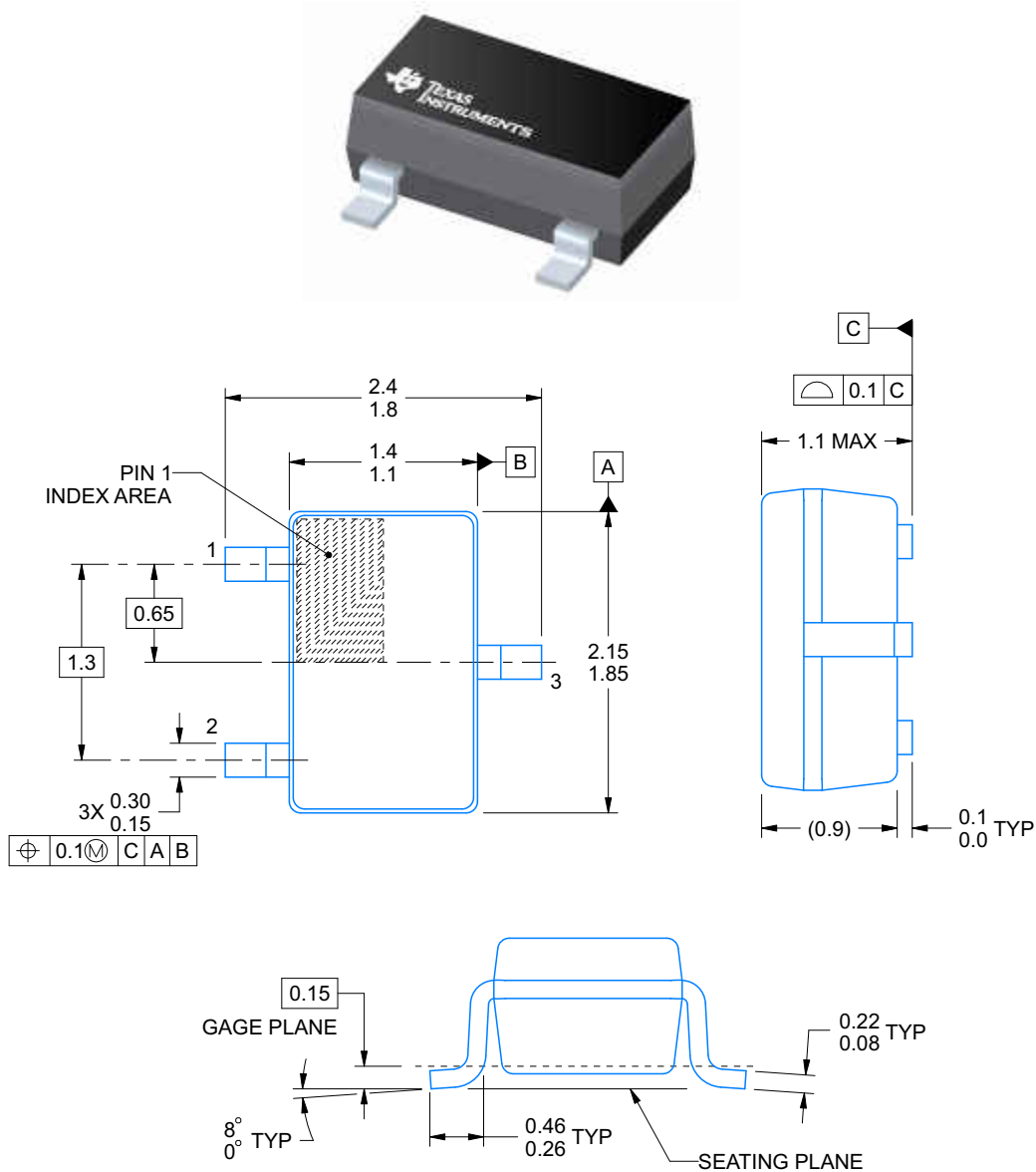
[Link to Package Drawing](#)



3.5 3-pin SC70 (TI: DCK) | 2 mm × 1.25 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD2E2U06 (Q1)	2	unidirectional	5.5	1.5	25
TPD2E007	2	bidirectional	±13	15	8
ESD752	2	bidirectional	±24	2.5	30
ESD2CAN24-Q1	2	bidirectional	±24	3	30

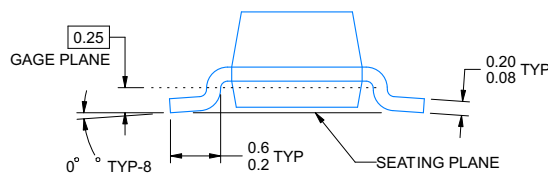
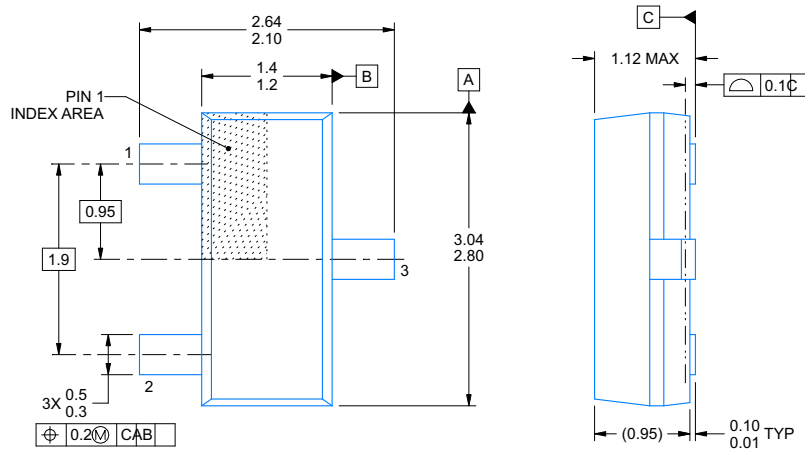
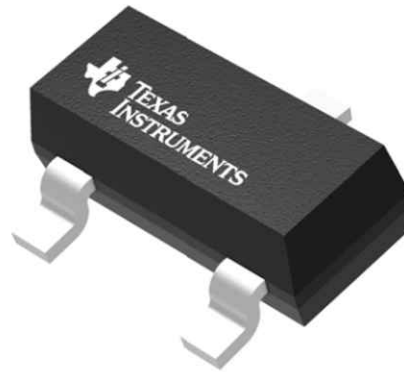
[Link to Package Drawing](#)



3.6 3-pin SOT23 (TI:DBZ) | 3.04 mm × 2.64 mm

Device Name	Channel	Direction	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TSM36A	1	unidirectional	36	90	30
TPD2E009	2	unidirectional	5.5	0.7	8
TPD2E2U06 (Q1)	2	bidirectional	5.5	1.5	25
ESD752	2	bidirectional	24	2.5	30
ESD2CAN24-Q1	2	bidirectional	24	3	30

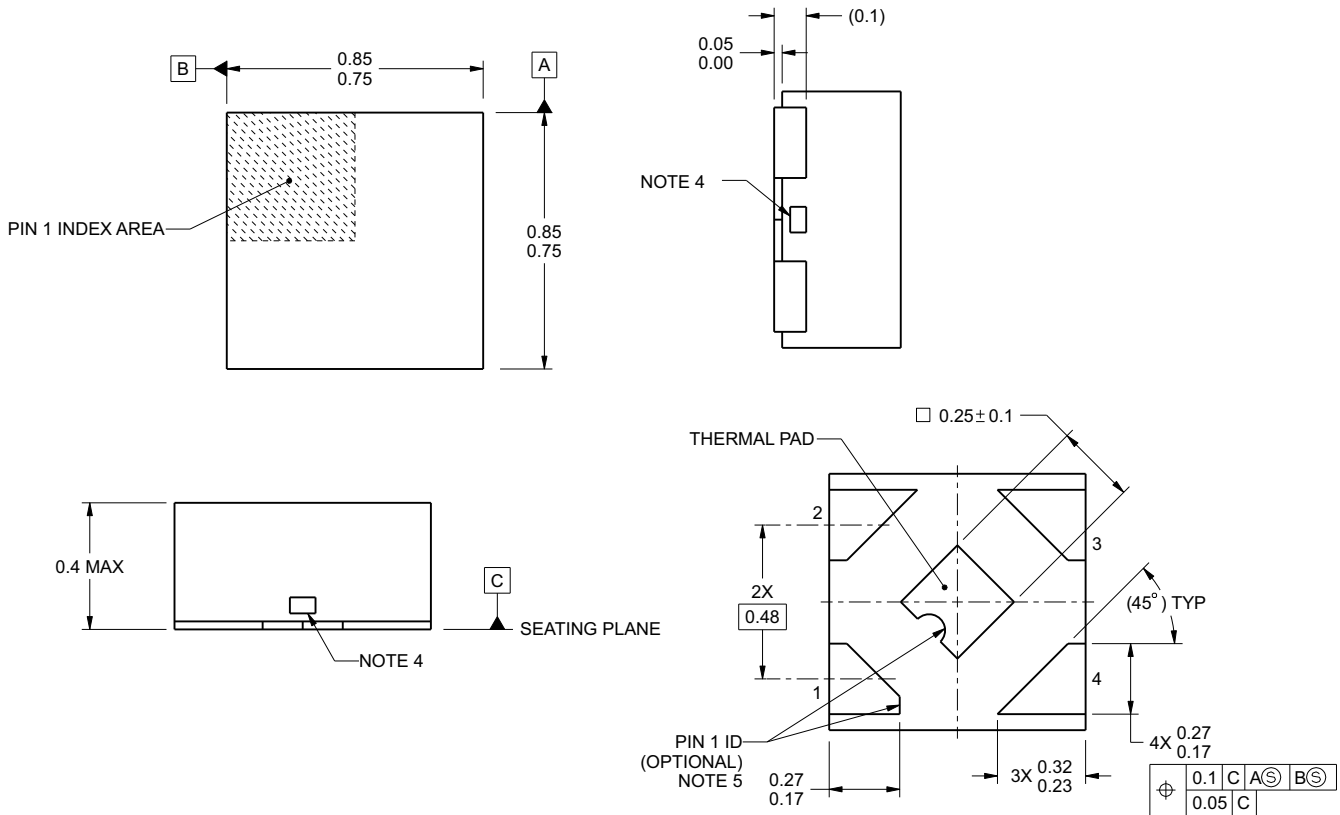
[Link to Package Drawing](#)



3.7 4-pin SON (TI: DPW) | 0.8 mm × 0.8 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD4E110	4	bidirectional	±5.5	0.5	12
TPD4E101	4	bidirectional	±5.5	4.8	15
TPD4E6B06	4	bidirectional	±5.5	4.8	15

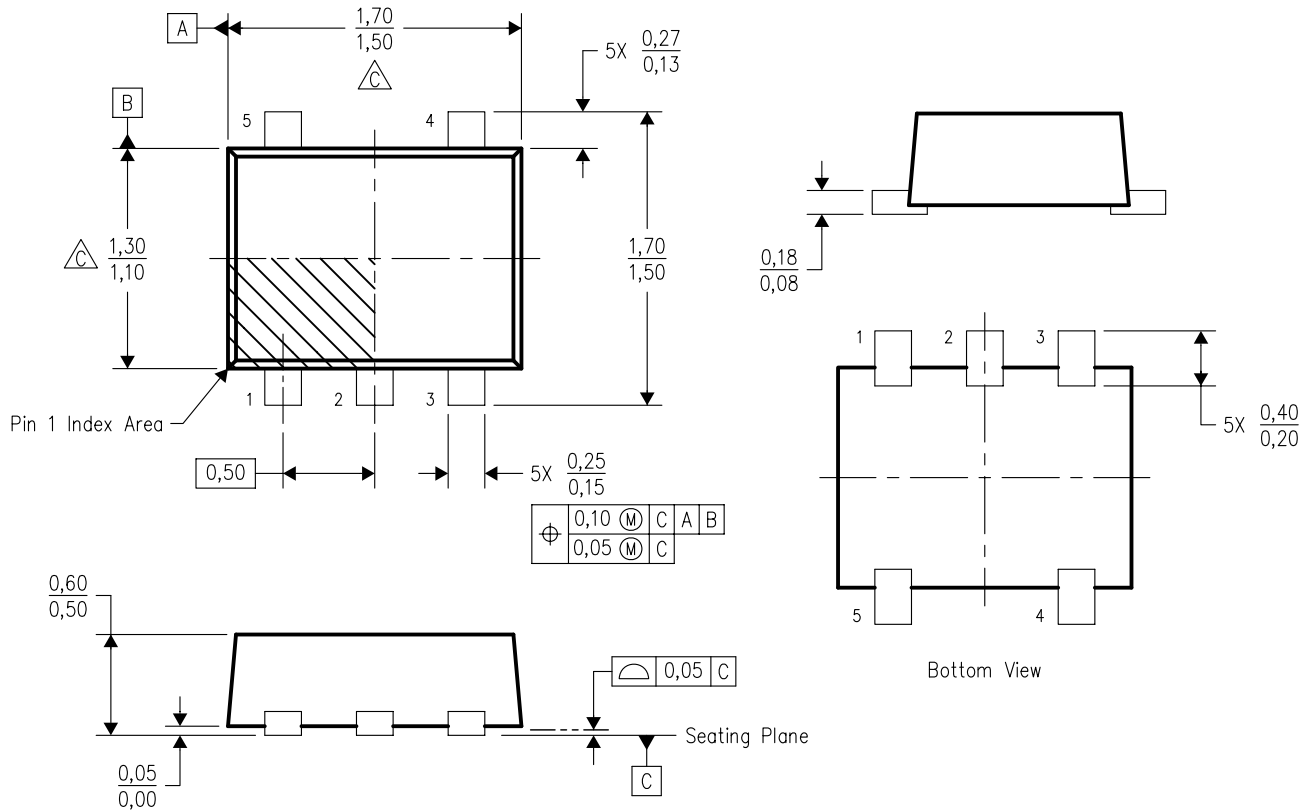
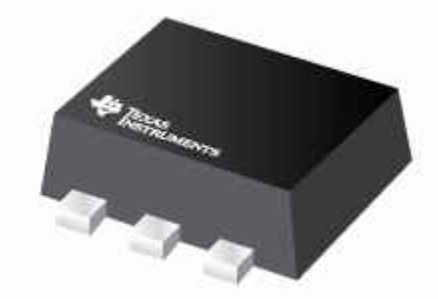
[Link to Package Drawing](#)



3.8 5-pin SOT-5X3 (TI: DRL) | 1.6 mm × 1.2 mm

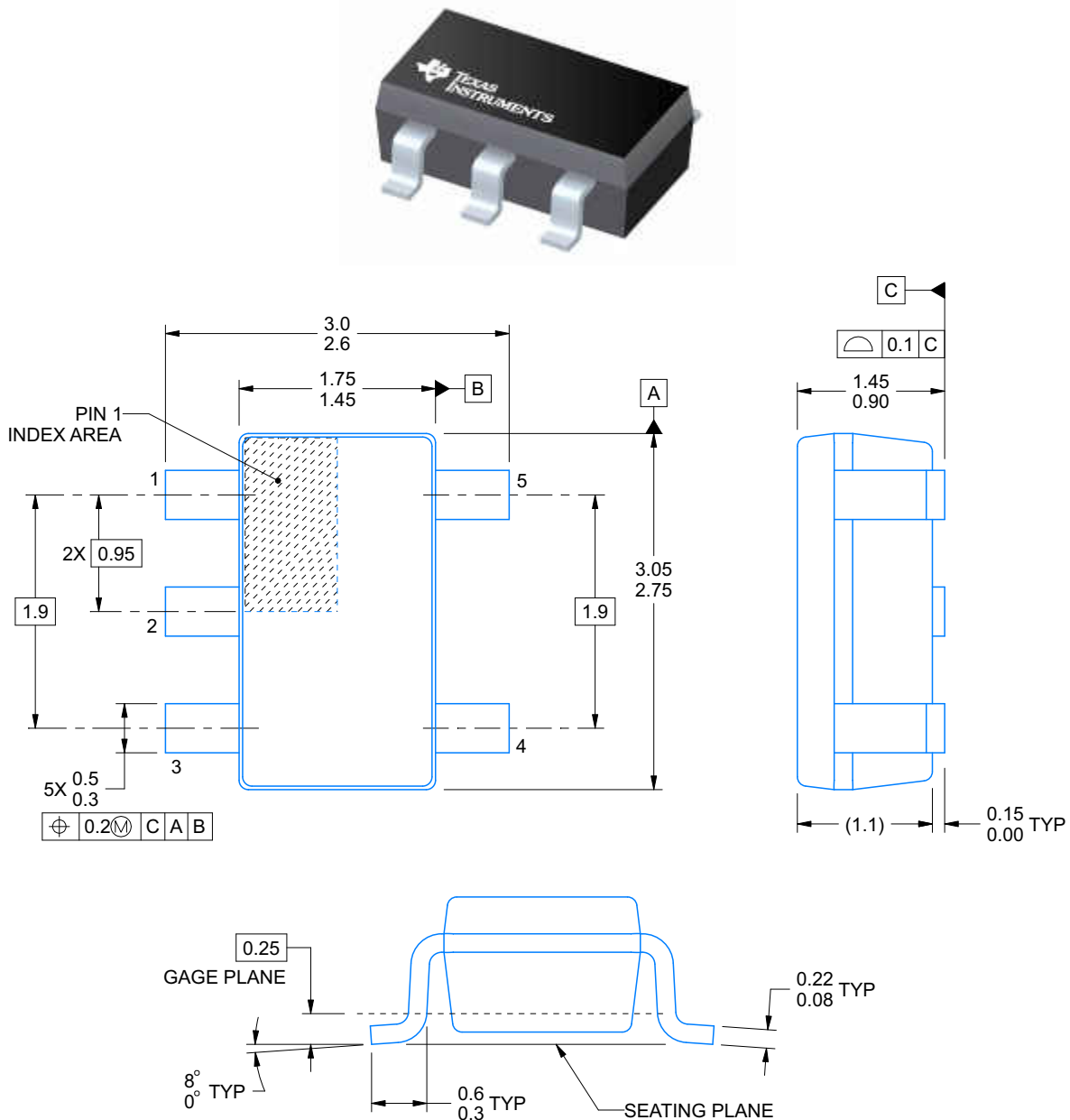
Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD2E2U06	2	unidirectional	5.5	1.5	25
TPD2E001 (Q1)	2	unidirectional	5.5	1.5	8
TPD3E001	3	unidirectional	5.5	1.5	8
TPD4E002	4	unidirectional	5	11	15

[Link to Package Drawing](#)



3.9 5-pin SOT-23 (TI: DBV) | 2.9 mm × 1.6 mm

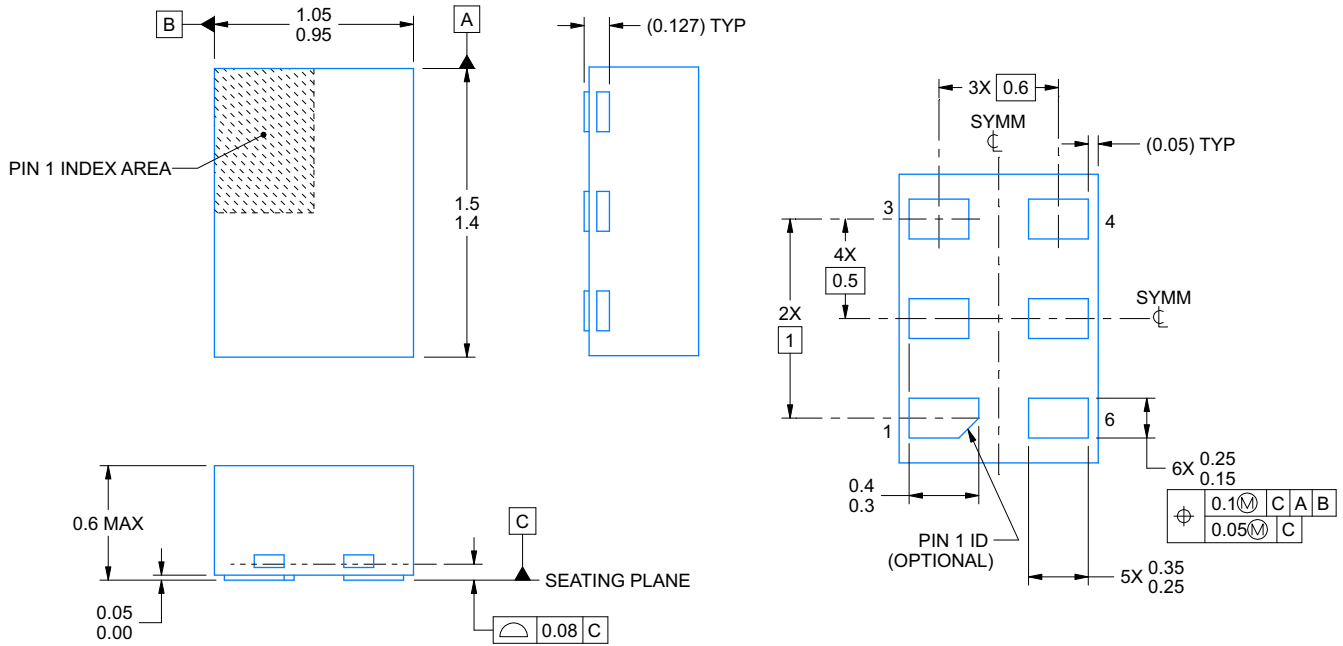
Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
ESDS302	2	unidirectional	3.6	2.3	30
ESDS312	2	unidirectional	3.6	4.5	30
ESDS304	4	unidirectional	3.6	2.3	30
ESDS314	4	unidirectional diagonally</td <td>3.6</td> <td>4.5</td> <td>30</td>	3.6	4.5	30

[Link to Package Drawing](#)


3.10 6-pin SON (TI: DRY) | 1.45 mm × 1 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD2E001	2	unidirectional	5.5	1.5	8
TPD3E001	3	unidirectional	5.5	1.5	8
TPD4S009	4	unidirectional	5.5	0.8	8
TPD4E004	4	unidirectional diagonal</td <td>5.5</td> <td>1.6</td> <td>8</td>	5.5	1.6	8
TPD4S012	4	unidirectional	5.5	4	10

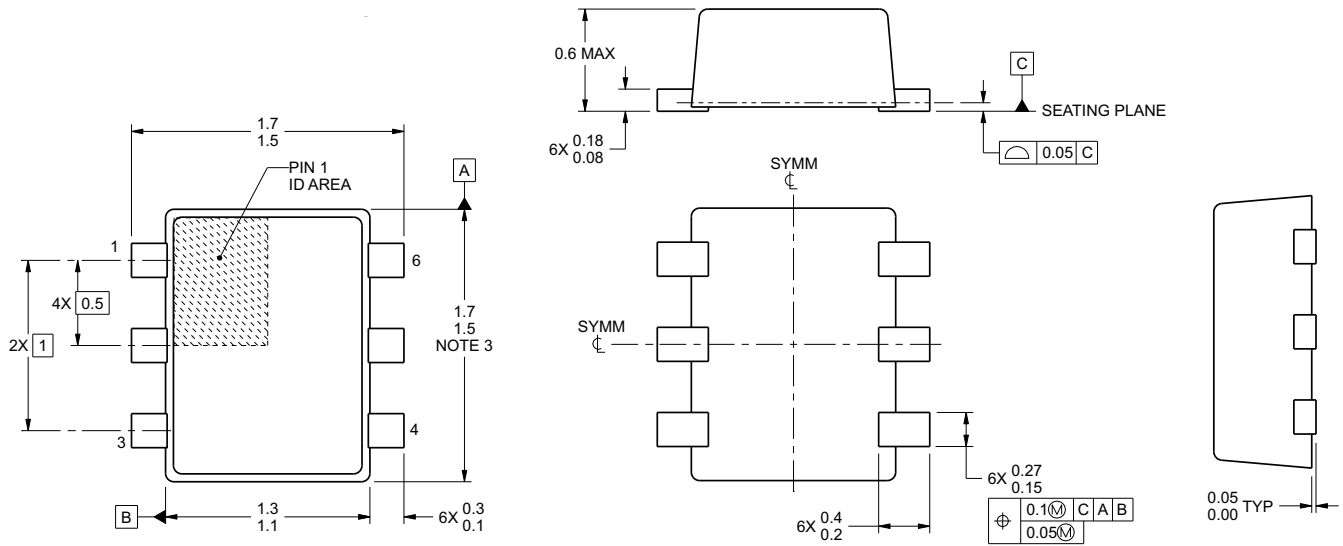
[Link to Package Drawing](#)



3.11 6-pin SOT-5X3 (TI: DRL) | 1.6 mm × 1.2 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD2E1B06	2	bidirectional	±5.5	1	10
TPD4E1B06	4	bidirectional	±5.5	0.7	12
TPD4E001	4	unidirectional	5.5	1.5	8

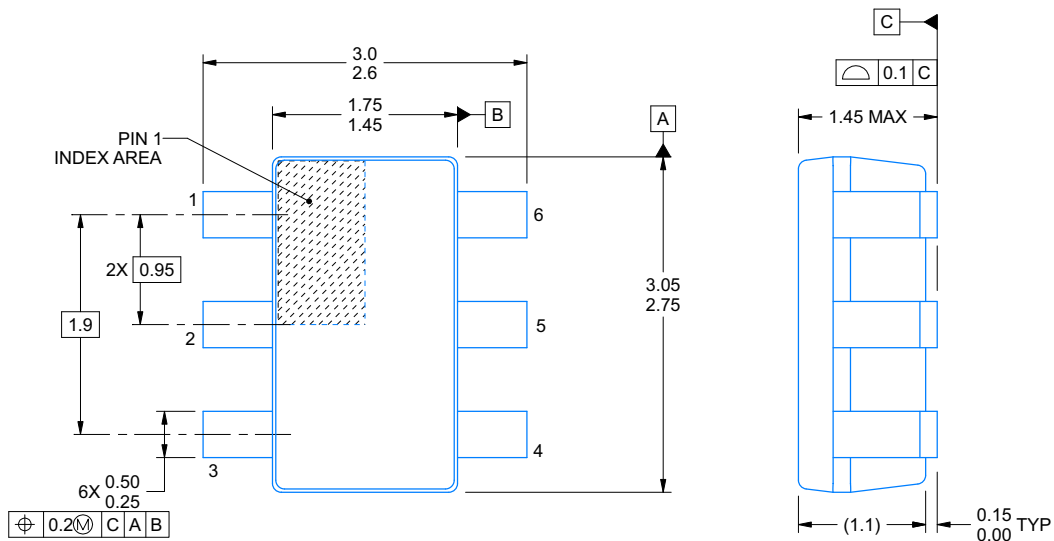
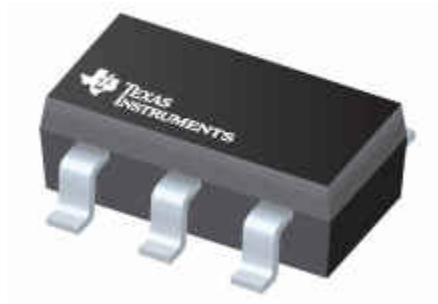
[Link to Package Drawing](#)



3.12 6-pin SOT-23 (TI: DBV) | 1.6 mm × 2.9 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD4E1U06	4	unidirectional	5.5	0.8	15
TPD4S009	4	unidirectional	5.5	0.8	8
TPD4E001 (Q1)	4	unidirectional	5.5	1.5	8

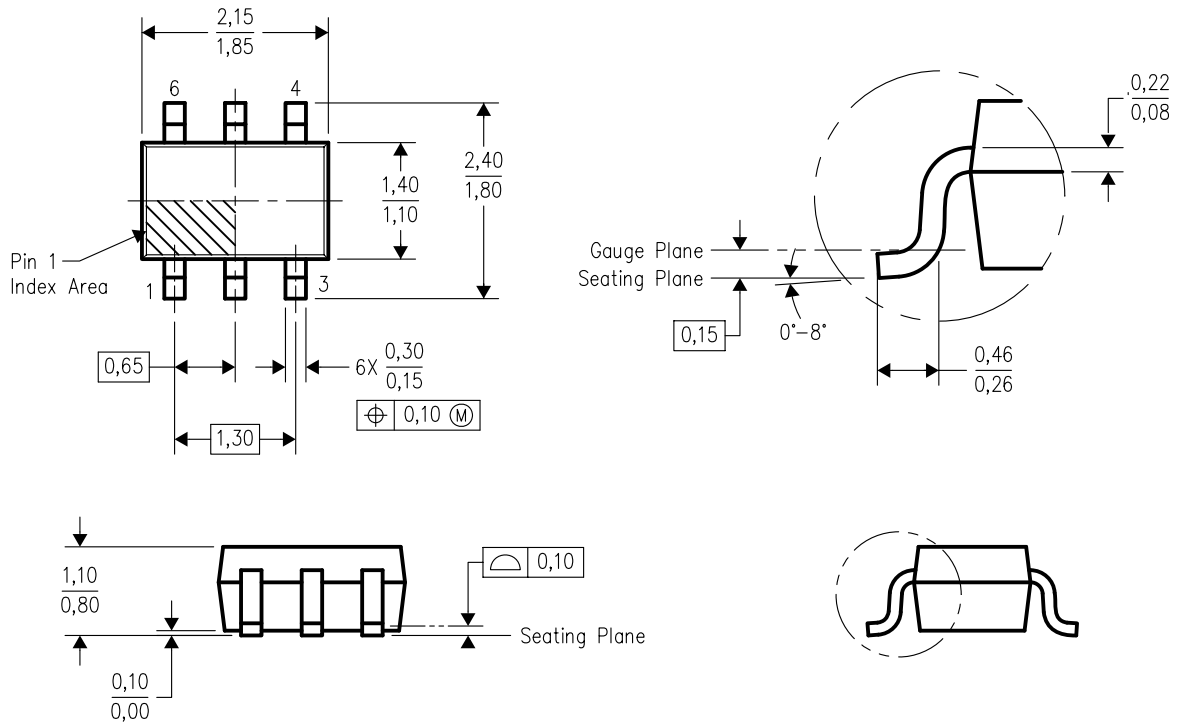
[Link to Package Drawing](#)



3.13 6-pin SC70 (TI: DCK) | 2.15 mm × 1.4 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD4E1B06	4	bidirectional	±5.5	0.7	12
TPD4E1U06	4	unidirectional	5.5	0.8	15
TPD4S009	4	unidirectional	5.5	0.8	8
TPD4E001	4	unidirectional	5.5	1.5	8

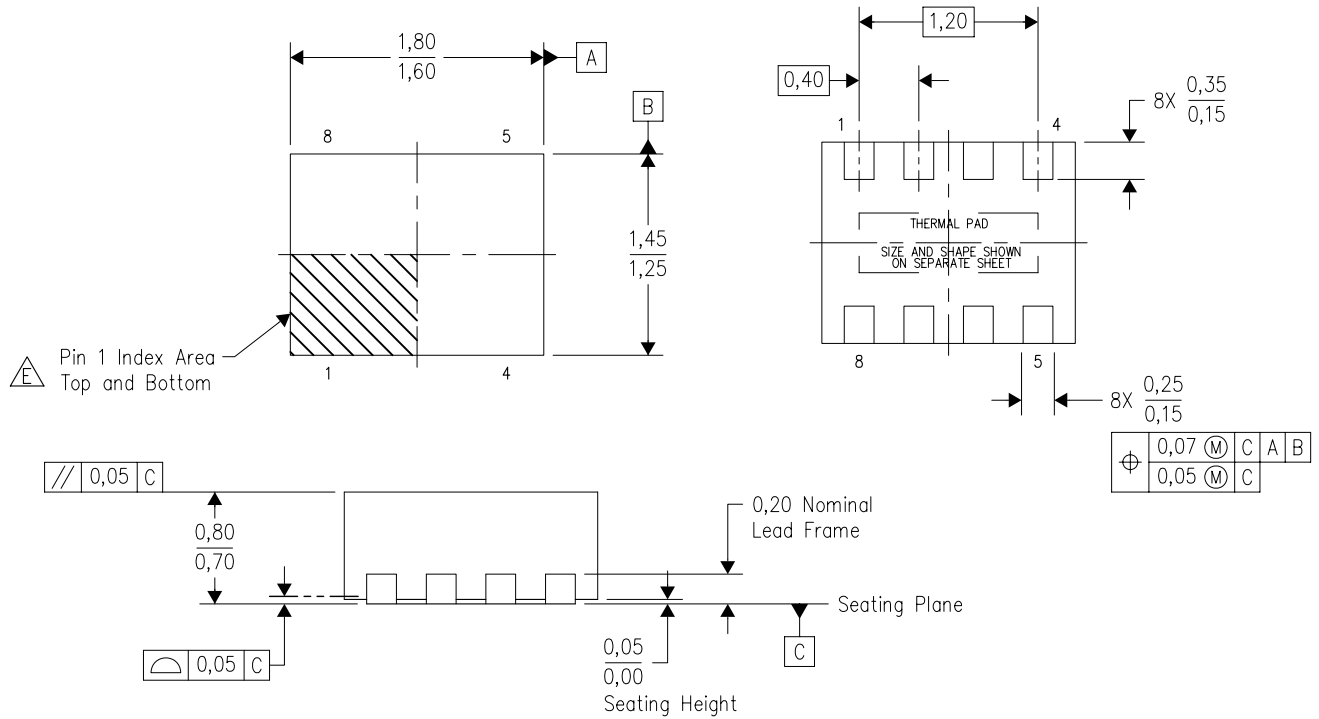
[Link to Package Drawing](#)



3.14 8-pin SON (TI: DQD) | 1.35 mm × 1.7 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD3F303	3	bidirectional	±5.5	20	15
TPD4F003	4	unidirectional	5.5	17	12
TPD8E003	8	unidirectional	5.5	9	12

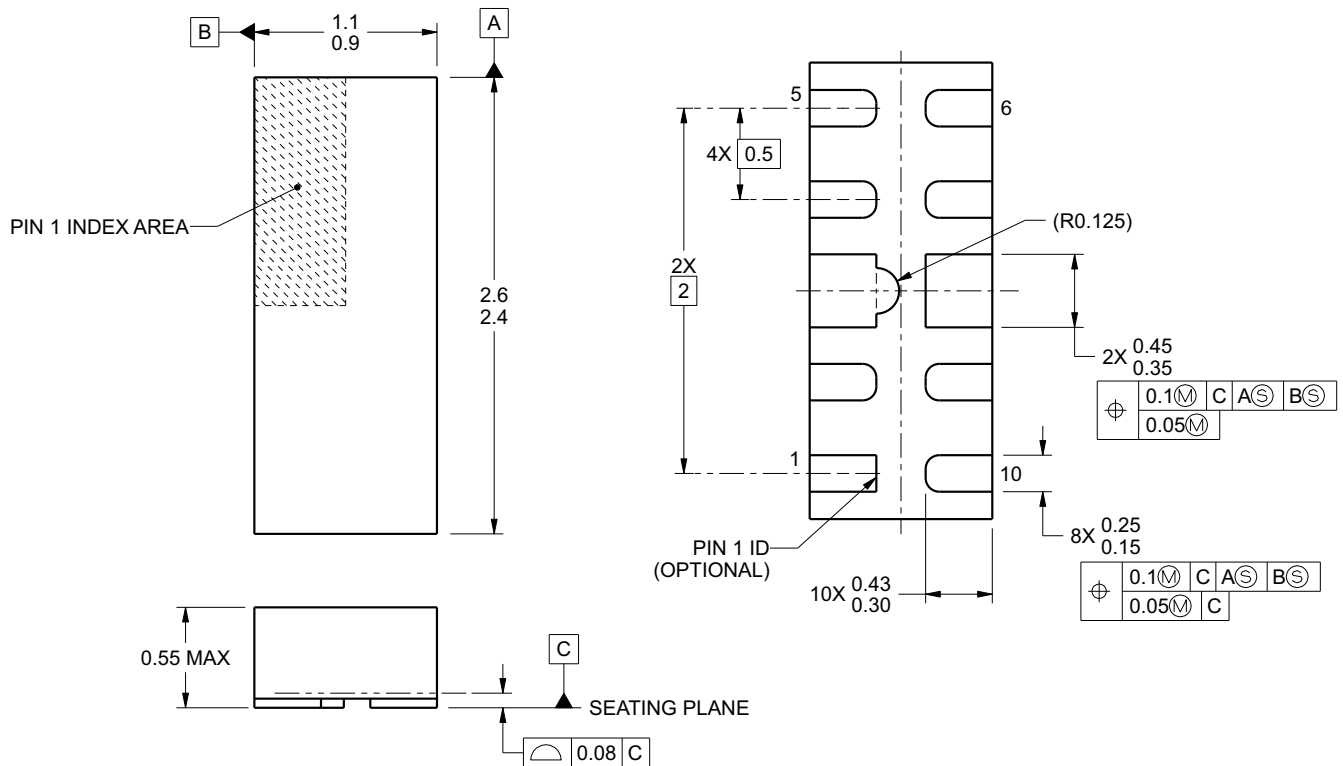
[Link to Package Drawing](#)



3.15 10-pin SON (TI: DQA) | 1 mm × 2.5 mm

Device Name	Number of Channels	Directional	Working Voltage (V)	Capacitance (pF)	ESD Rating (kV)
TPD4E02B04 (Q1)	4	bidirectional	±3.6	0.25	12
ESD224	4	bidirectional	±3.6	0.5	12
ESD204	4	bidirectional	±3.6	0.55	30
TPD4E05U06 (Q1)	4	unidirectional	5.5	0.5	12
TPD4EUSB30	4	unidirectional	5.5	0.8	8
TPD4S010	4	unidirectional	5.5	0.8	8

[Link to Package Drawing](#)



4 References

- Texas Instruments, [System-Level ESD Protection Guide, Marketing Selection Guide](#)
- Texas Instruments, [ESD Protection Layout Guide Application Report](#)

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2022) to Revision B (August 2022) Page

- Updated packages layout and added current parts to each of the packages.....6
 - Added 3-pin SOT23 (TI:DBZ) | 3.04 mm × 2.64 mm topic..... 11
-

Changes from Revision * (August 2020) to Revision A (April 2022) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
 - Added 2-pin SOD-523 1.2-mm x 0.8-mm (TI: DYA) topic.....8
-

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