User’s Guide

# DLP2021LEQ1EVM Evaluation Module


## ABSTRACT

TI's DLP® technology offers a fully programmable and high-resolution solution for automotive dynamic ground projection (DGP) applications. With an effective input resolution of 588 × 330, DLP technology exceeds the resolution of existing ground projections technologies. Dynamic ground projection technology, with the ability to display any static or video pattern within the same module, can re-invent consumers’ perceptions on small projector lighting by providing new, innovative lighting capabilities. Examples include automotive light “carpets” that can illuminate the surrounding area outside a vehicle or project vehicle information such as the EV charge level and range remaining, tire pressure warnings, traffic warnings, turn signaling, check engine light warning, gas level/range, etc. from a side mirror. Ground projection has other enhancement features to help cars communicate with drivers and pedestrians, including corner lighting, reverse lighting, vehicle customization, and parking indicators.

The DLP2021LEQ1EVM is the DLP2021-Q1 Light Engine Evaluation Module (EVM) that allows for accelerated evaluation of the DLP2021-Q1 chipset with the inclusion of a DLP2021-Q1 light engine. This module brings together a set of components including the DLP2021-Q1 DMD, the FPGA based DMD controller, and the TPS65100 PMIC to provide an efficient system for evaluation of dynamic ground projection technology. The DLP2021LEQ1EVM includes RGB LEDs, while the DLP2021LEWQ1EVM includes a single white LED. When combined with a computer for GUI control, the evaluation module can be used in a laboratory setting to demonstrate features such as:


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# 1 DLP2021-Q1 Electronics EVM Overview

This user's guide presents an overview of the DLP2021-Q1 electronics EVM, a general description of the main features and functions, and quick start procedure for out-of-box evaluation. TI recommends users to first read the *Dynamic Ground Projection Application Requirements* (DLPA116) and *DLP3021-Q1 Dynamic Ground Projection System Design* (DLPA086) reports to become familiar with the terminology, variables, application considerations, and system design requirements for dynamic ground projection as they relate to the DLP2021-Q1 chipset.

**Note**

This document makes multiples references to documentation titled with the DLP3021-Q1. The DLP3021-Q1 system concepts are also applicable to the DLP2021-Q1. The DLP2021-Q1 has been derived from the DLP3021-Q1.

## 1.1 Introduction

The DLP2021LEQ1EVM Evaluation Module (EVM) is a complete electronic and optical subsystem designed to control and interface with the DLP2021-Q1 chipset. The DLP2021-Q1 interfaces with an FPGA based DMD controller. This chipset is combined with illumination and projection optics, and RGB or White LEDs to create a projector that offers brightness of approximately 30 lumens with full motion video playback in a small volume form factor. The DLP2021LEQ1EVM is not a production design, and is intended for evaluation only.

## 1.2 What is in the DLP2021-Q1 Light Engine EVM

The DLP2021-Q1 Light Engine EVM consists of three subsystems and two boards:

- DLP2021LEQ1EVM unit:
  - Formatter — Includes the DLP2021-Q1 DMD, FPGA based DMD controller, the MSP430G2553-Q1 MCU, external NOR flash memory, and the TPS65100-Q1 PMIC.
  - Illumination Driver — Includes illumination drivers and FETs.
  - Light Engine — Compact light engine designed to display images from the formatter. Two light engine variants are available:
    - DLP2021LEQ1EVM:
      - "EVM-T02DGPC" = Color/RGB LEDs
        - Green LED: Luminus SFT-03X-CG
        - Red/Blue LED: Luminus SFM-03X-RB
    - DLP2021LEWQ1EVM:
      - "EVM-T02DGPW" = White LED: Luminus SFT-03X-W
- FTDI C232HM-DDHSL-0 USB to MPSSE serial cable for 3.3V logical level SPI communication with the FPGA based DMD controller and external flash memory. The Cheetah™ USB-to-SPI interface can be used as a faster alternative for USB-to-SPI communication, but must be purchased separately.
- SPI Adapter board — intermediate board between the FTDI USB-to-SPI cable and DLP2021LEQ1EVM electronics board required for *Host Mute* and *Flash Programming* operating modes. Includes toggle switches to change the operating mode of the EVM.

Figure 1-1 shows the block diagram of the DLP2021LEQ1EVM.

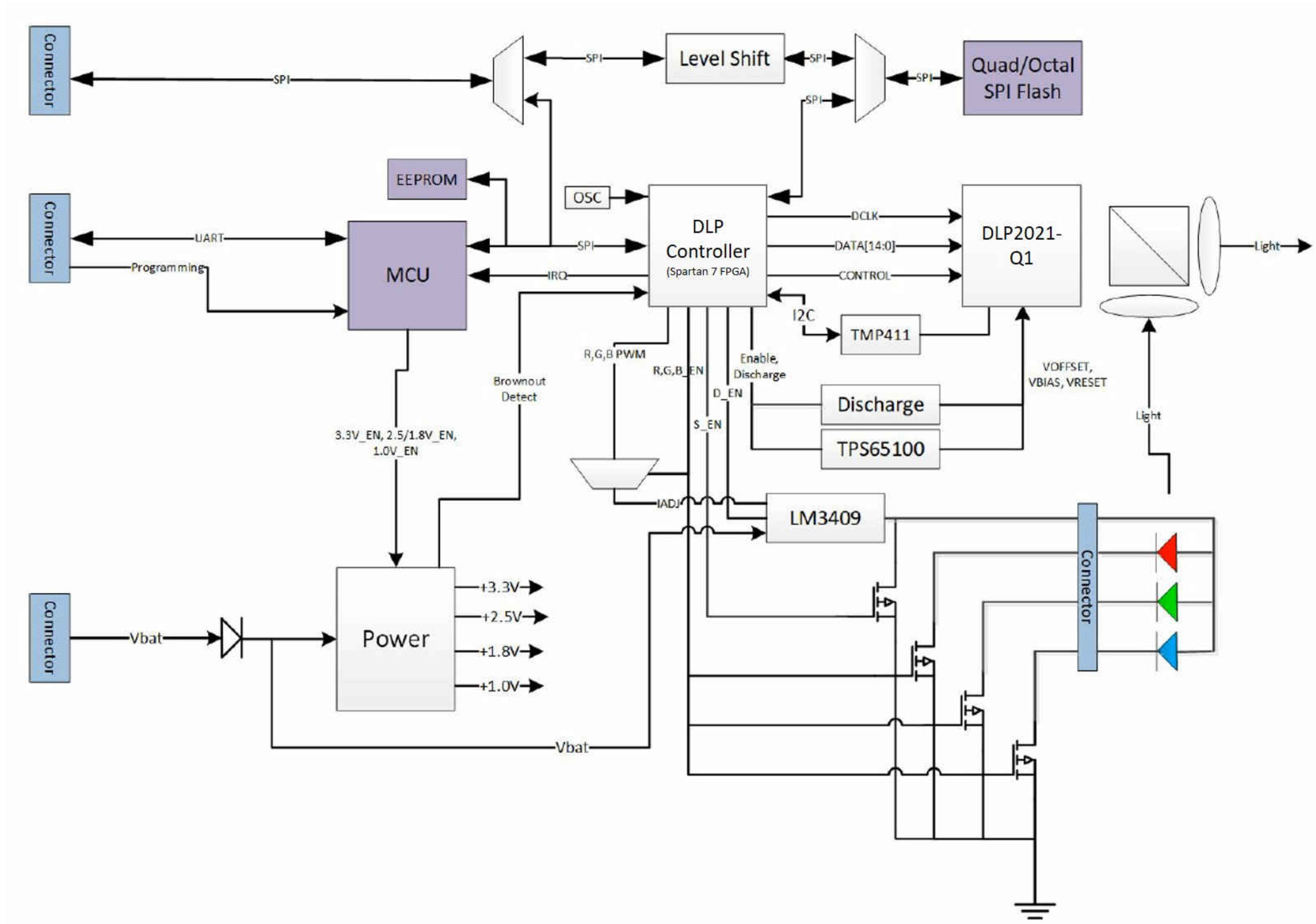



**Figure 1-1. DLP2021LEQ1EVM Block Diagram**

Figure 1-2 shows the assembled DLP2021LEQ1EVM Unit.

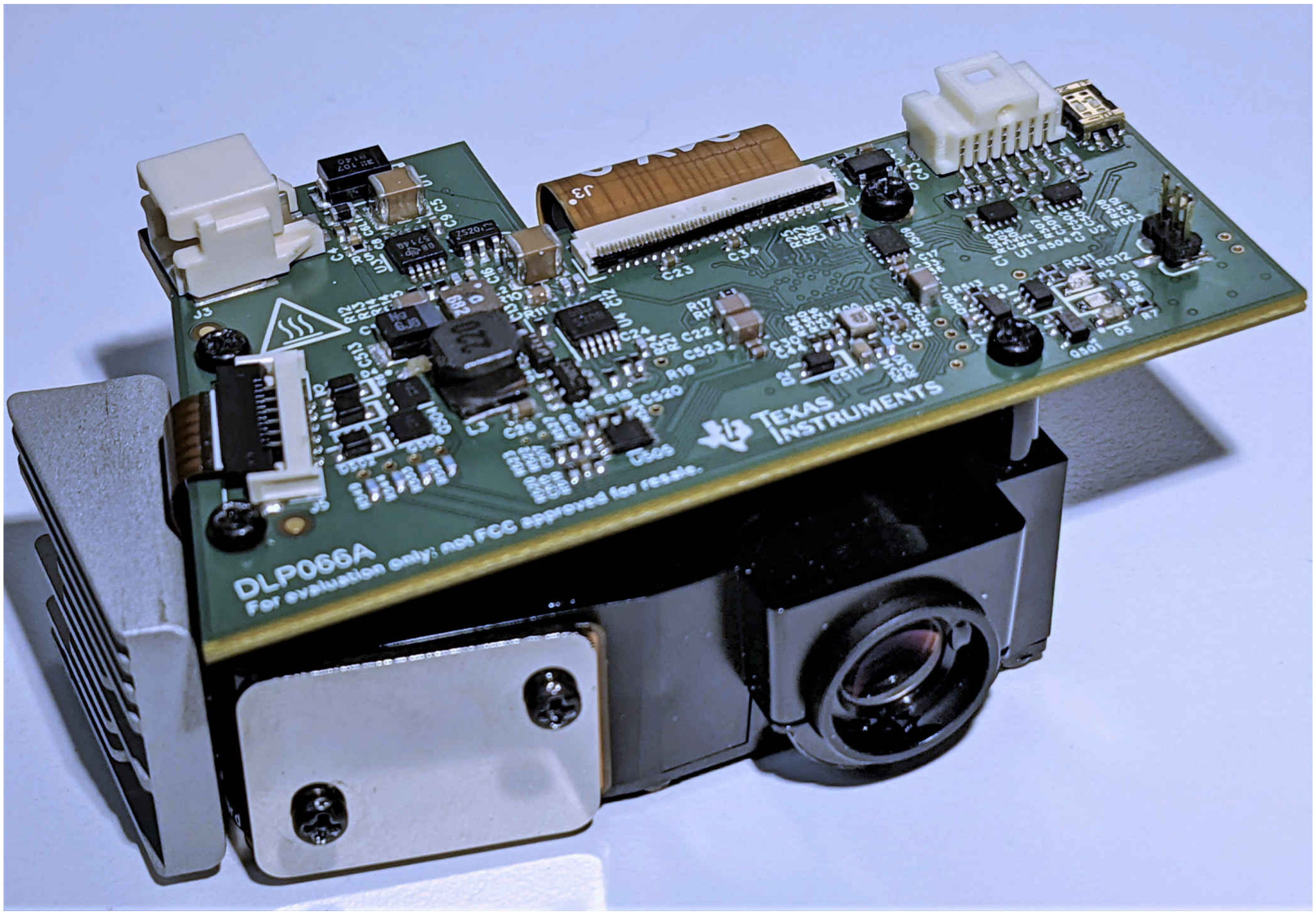



**Figure 1-2. DLP2021LEQ1EVM Unit with Heat Sink**

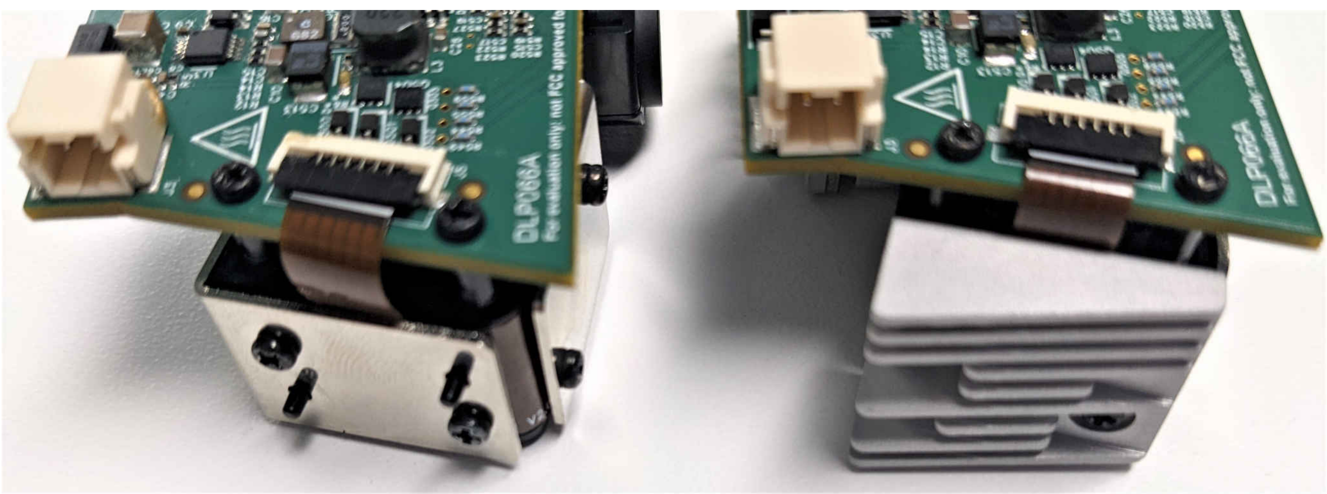


**Figure 1-3. DLP2021LEQ1EVM Cooling Plate for RGB LEDs (Left) and Heat Sink for White LED (Right)**

**CAUTION**

Projection Lamp

May be harmful to the eyes.

Do not stare at the operating lamp.

**CAUTION**

Hot Surface

Contact may cause burns.

Do not touch.

### 1.2.1 Formatter Subsystem

The formatter subsystem converts and translates image/video data stored in external flash memory through the FPGA based DMD controller into the Double Data Rate (DDR) interface format compatible with the DLP2021-Q1 data bus. The EVM offers two operating modes to specify what and how the image/video content is to be displayed: in a closed-loop stand-alone mode using the on-board MSP430 MCU, or through an external controller (such as the FTDI USB-to-SPI cable or Cheetah™ SPI Host Adapter) for GUI operation.

A DIP two-position switch at S1 on the DLP2021L1Q1EVM allows the user to physically set the operating mode of the formatter subsystem. The SPI Adapter board also has two physical switches (S1 and S2) to set the same operating modes. Figure 1-4 and Figure 1-5 show the default S1 switch state for *Host Control* operating mode for stand-alone operation, and the default switch state for *Host Mute* operating mode when the SPI Adapter Board is connected.

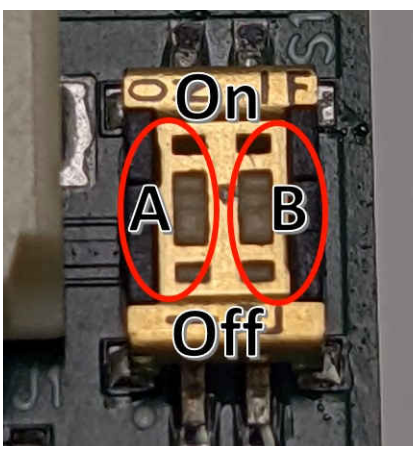



**Figure 1-4. Operating Mode Switches: Electronics Board S1-A and S1-B Switches**

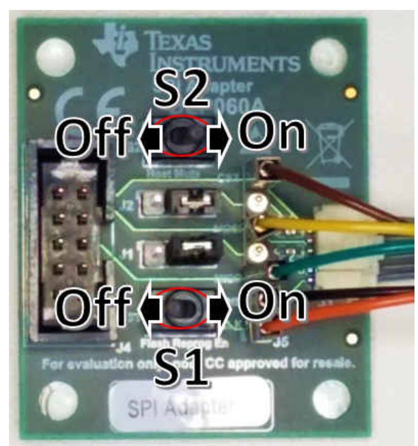



**Figure 1-5. Operating Mode Switches: SPI Adapter Board S1 and S2 Switches**

See Table 1-1 for the switch positions required of each operating mode.

**Table 1-1. DLP2021LEQ1 EVM Operating Mode Switch Positions**

| Operating Mode | DLP2021LEQ1EVM | | SPI Adapter Board | | LED State |
|---|---|---|---|---|---|
| | S1-A | S1-B | S1 | S2 | |
| Host Mute | OFF | ON | OFF | ON | Blue = ON, Amber = OFF, Green = ON |
| Local Host Control | OFF | OFF | OFF | OFF | Blue = OFF, Amber = OFF, Green = ON |
| FPGA Programming | ON | ON | ON | ON | Blue = ON, Amber = ON, Green = OFF |
| Undefined | ON | OFF | ON | OFF | Blue = OFF, Amber = ON, Green = OFF |

A brief description of each operating mode is provided as follows:

***Host Mute:*** This mode allows direct read/writes to the DMD controller parameters. This is the recommended operation mode of the EVM for initial development and debug purposes. The FTDI cable and SPI Adapter board are required to run the EVM in this mode and bypass the MSP430G2553-Q1 MCU on-board host controller. The DLP Control Program is the GUI used to configure the DMD control parameters in this mode.

***Local Host Control:*** This mode allows the MSP430G2553-Q1 MCU on-board host controller to locally read/ write to the DMD controller. No additional hardware or GUI is required to run the EVM in this mode because command execution by the MCU automatically starts after the EVM is powered-up. This mode is recommended for demonstration purposes or system testing to emulate the end-product module. The SPI Adapter board and FTDI cable are not required for this operation mode.

***FPGA Programming:*** This mode allows the DMD controller to be reprogrammed using the DLP Composer GUI. The FTDI cable and SPI Adapter board are required to run the EVM in this mode because the flash program binary is uploaded from the PC to EVM through the FTDI cable. The light engine will be disabled so that no content is displayed while the EVM is in this mode. See Section 4.1.7 for details on Flash Programming.

***Undefined:*** This mode is unsupported by the EVM and should not be used.

To allow the SPI Adapter board to set the operating mode, TI recommends the DLP2021LEQ1EVM electronics board S1 switches always be set to *Local Host Control* mode. This is because the On-state of either board will always override the Off-state of the other board. This setup will enable the use the more easily accessible S1 and S2 toggle switches of the SPI Adapter board to set the operating modes. When the SPI Adapter board is detached, the EVM will automatically start-up in the Local Host Control mode to allow the MSP430 to configure and run the EVM without intervention from an external controller such as the FTDI cable. When switching between operating modes, TI recommends that the EVM be fully power cycled to reset and apply the most recently set operating mode.

### 1.2.2 Illumination Subsystem

The illumination subsystem includes the LED driver circuit and RGB LEDs or a White LED. The FPGA has three PWM outputs which typically correspond to red, green, and blue illumination colors. The PWM duty cycles can be adjusted to set a reference voltage to an external illumination driver circuit as needed to balance colors and adjust output brightness. Typical illumination configurations for the DLP2021Q1EVM:

- Optimal Color for RGB: PWM=450 with duty cycles of Red=30%, Green=55%, Blue=15%
- Single/Monochromatic: PWM=450 with duty cycles of Red=0%, Green=100%, Blue=0%

The PWM is a 10-bit value that is initialized to the Default Register Configuration value of DLP Composer, but can be modified in real-time during display operation. The duty cycle of each RGB can only be configured in DLP Composer as part of a list of Sequence Settings.

### 1.2.3 Light Engine

The light engine included with the DLP2021LEQ1EVM can expect to achieve the specifications listed in Table 1-2.

**Table 1-2. Light Engine Performance Specifications**

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Lumionus Flux | RGB LEDs(1) | White ANSI | | 29.04 | | Lumen |
| | | Black ANSI | | 0.066 | | |
| | White LED(2) | White ANSI | | 39.66 | | |
| | | Black ANSI | | 0.109 | | |
| Full On/Off Contrast | RGB LEDs(1) | | | 442 | | |
| | White LED(2) | | | 366 | | |
| Field of View (FOV), Horizontal × Vertical | | | | 23 × 13 | | Degrees |

(1) LED PWM = 450; duty cycles: R30%, G55%, B15%
(2) LED PWM = 450; duty cycles: R0%, G100%, B0%

### 1.2.4 Cables

The DLP2021LEQ1EVM kit contains the following cables shown in Figure 1-6.

**Table 1-3. DLP2021LEQ1EVM Cables**

| NAME | REFERENCE | QUANTITY |
|---|---|---|
| FTDI USB-to-SPI Cable | A | 1 |
| Host SPI Adapter Cable | B | 1 |
| Input Power Cable | C | 1 |
| DMD Signal Flex PCB Cable(1) | D | 1 |
| LED Driver Flex PCB Cable(1) | E | 1 |
| Cheetah™ SPI Host Adapter(2) | F | 0 |
| USB Type-A to Type-B Cable for Cheetah™(2) | G | 0 |
| MSP-FET MSP MCU Programmer and Debugger(2) | H | 0 |

(1) Connected locally at DLP2021LEQ1EVM electronics board.
(2) Sold separately and not required for evaluation.

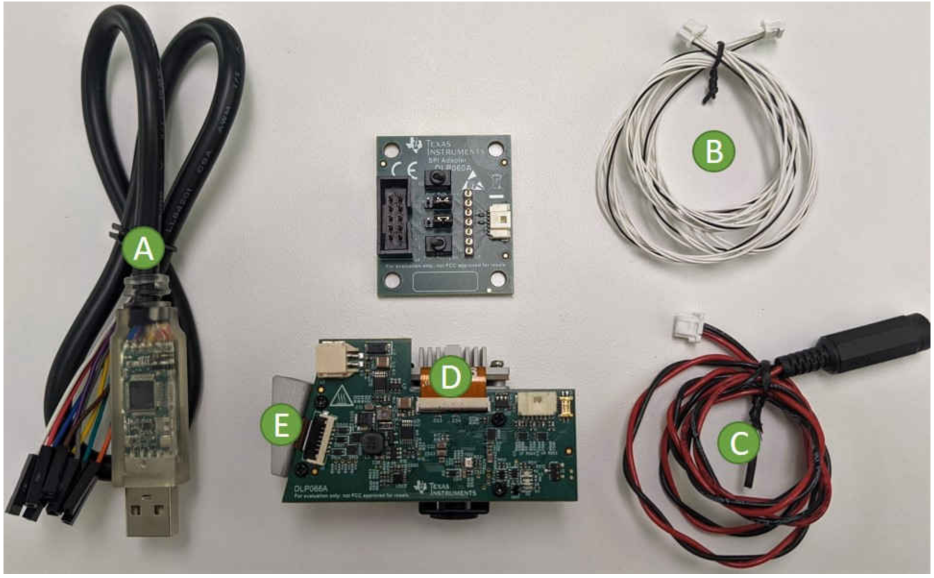



**Figure 1-6. Cables Included in DLP2021LEQ1EVM for FTDI**

## 1.3 Non-Optical Specifications

### 1.3.1 Electrical Specifications

**Table 1-4. Electrical Specifications**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Voltage | | 10.5 | 12 | 18 | V |
| Power (PWM Enabled) | RGB LEDs(1) | | 2.76 | | W |
| | White LED(2) | | 1.80 | | |
| Power (PWM Disabled) | RGB LEDs(1) | | 1.0 | | |
| | White LED(2) | | 1.0 | | |
| **LED DRIVER** | | | | | |
| Light Engine Efficiency(4) | RGB LEDs(1) | | 23.1 | | % |
| | White LED(2) | | 29.5 | | |
| LED Power | RGB LEDs(1) | | 1.34 | | W |
| | White LED(2) | | 1.31 | | |
| Efficacy(5) | RGB LEDs(1) | | 21.6 | | lm / W |
| | White LED(2) | | 30.1 | | |
| **TEMPERATURE** | | | | | |
| Operating DMD Temperature | | –40 | 25 | 105(3) | °C |

(1) LED PWM = 450; duty cycles: R30%, G55%, B15%.
(2) LED PWM = 450; duty cycles: R0%, G100%, B0%.
(3) Some components are only rated to 85°C.
(4) Efficiency defined as: *(Luminous Flux × 100%) / Calculated Raw Lumens*.
(5) Efficacy defined as: *White ANSI Lumen / LED Power*.

### 1.3.2 Component Temperature Ratings

The board and most of the board components are rated to operate between –40°C to 105°C, including the DLP2021-Q1, MSP430 MCU, and FPGA DMD controller. Some components on board, such as switches, connectors, and indicator LEDs, do not meet this temperature rating. Please refer to the EVM bill of materials to review the temperature specifications of all components used in the EVM design.

### 1.3.3 LED Driver Design

The DLP2021-Q1 chipset, used with LED illumination, includes illumination modulation based on the LM3904-Q1 P-FET buck controller for high-power LEDs. This illumination modulation turns off the light output during micromirror reset, which improves system contrast. For the system timing specifications of the DLP2021LEQ1EVM, see Figure 1-7.

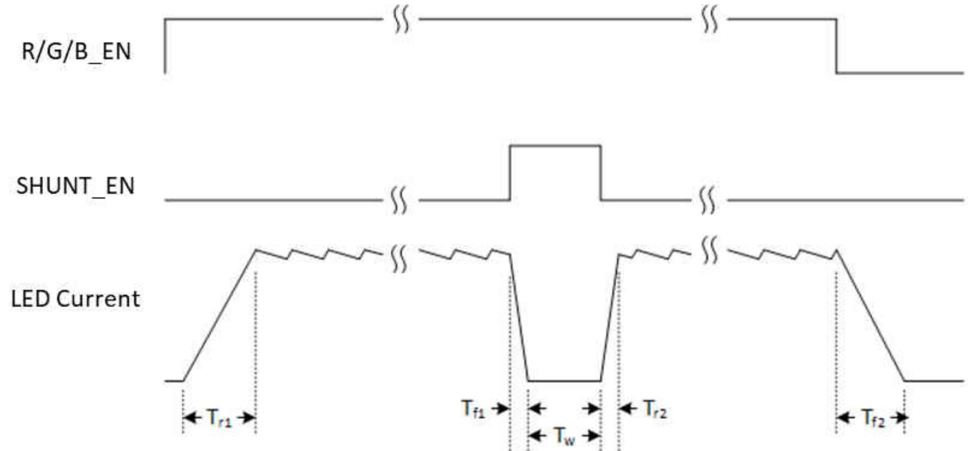



**Figure 1-7. LED Driver Timing Specifications**

The timing specifications are shown in Table 1-5.

**Table 1-5. LED Driver Timing Specifications**

| PARAMETER | VALUE |
|---|---|
| $T_{r1}$, $T_{f2}$ | < 50 µs |
| $T_{f1}$, $T_{r2}$ | < 2 µs |
| $T_w$ | minimum = 1 µs |

### 1.3.4 Video Specification

In this architecture, video content is compressed and stored in external flash memory. Low speed SPI commands are sent from the MSP430 MCU in Local Host Control operating mode or FTDI interface in Host Mute operating mode to the DMD controller to indicate what image/video content to read from the external 2Gb flash memory. Storing the image/video content in memory removes the need for a high-speed video interface to the module which improves compatibility with typical vehicle infrastructures. It also decreases overall system size and cost by removing graphics generation and interfaces. The controller decompresses each bit plane of the video data (416 × 468 resolution) and displays them on the DMD in rapid succession to create the full video image at a frame rate of 25 Hz. A frame rate of 25 Hz is recommended due to memory constraints, but the DLP2021-Q1 can support a maximum frame rate of 60 Hz. Due to the diamond format of the DMD pixels, the output image has an effective resolution of 588× 330. The controller synchronizes the DMD bit plane data with the RGB enable timing for the LED color controller and driver circuit.

## 2 Quick Start

Use the following instruction to setup your DLP2021-Q1 Light Engine EVM and PC.

### 2.1 Kit Assembly Instructions

The DLP2021-Q1 Light Engine EVM electronics board is shipped as a fully assembled unit. A diagram of all cable connections is shown in Figure 2-1.

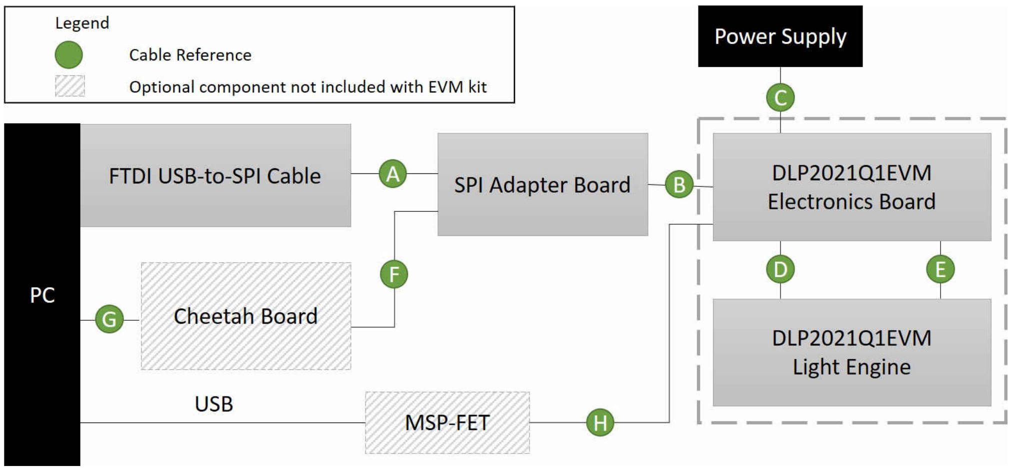



**Figure 2-1. Cable Connections**

**Table 2-1. FTDI C232HM MPSSE Cable to SPI Adapter Board Connections**

| FTDI Wire Signal (Pin) | FTDI Wire Color | SPI Adapter Board FTDI Header Pin |
|---|---|---|
| TCK (2) | Orange | J5-1 |
| GND (10) | Black | J5-2 |
| TDO (4) | Green | J5-3 |
| TDI (3) | Yellow | J5-5 |
| TMS (5) | Brown | J5-7 |

### 2.2 Software Installation

Download and install the following software from TI:

- DLP2021-Q1 Composer Project and FPGA Configuration (*DLPC153*): https://www.ti.com/lit/zip/dlpc153
- DLP Control Program for the DLP2021-Q1 DMD (*DLPC136*): https://www.ti.com/lit/zip/dlpc136
- DLP Composer for DLP2021-Q1 (*DLPC137*): https://www.ti.com/lit/zip/dlpc137
- MSP430 Example Code (*DLPC138*): https://www.ti.com/lit/zip/dlpc138

Download and install the following from third-parties:

- The C232HM MPSSE cable requires USB device drivers, available free from http://www.ftdichip.com. The D2XX driver is used with application software to directly access the FT232H in the cable though a DLL.
- Optional: Total Phase Cheetah™ USB adapter: http://www.totalphase.com/products/usb-driverswindows

### 2.3 Power-Up

Follow these steps to properly supply power to the EVM:

1. Connect the input power cable to a power supply that meets input power specifications defined in Section 1.3.1. A 12-V supply with a 0.5-A limit is recommended for out-of-box evaluation. The red cable for the V+ terminal and black cable for the V– terminal. A red LED will illuminate on the electronics board to indicate the EVM is receiving power.
2. Set the operation mode switches to the *Local Host Control* operating mode as defined in Section 1.2.1. The EVM is already flash programmed with TI demo image/video content when shipped for out-of-box evaluation.

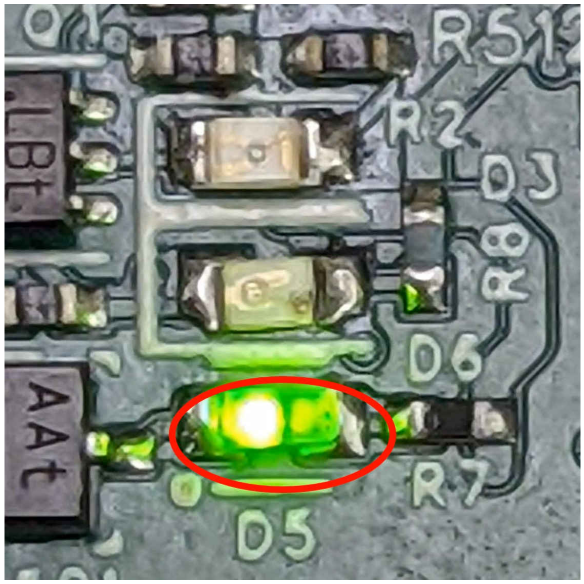



**Figure 2-2. Local Host Operating Mode LED Status**

3. Turn on the supply power, and the EVM will immediately begin to display content.

## 2.4 Select Display Content

Follow these steps to run the DGP software to change the display content and settings:

1. Turn off the supply power.
2. Set the operation mode switches to the *Host Mute* operating mode as defined in Section 1.2.1.
3. Turn on the supply power. Figure 2-3 shows the LED status of the EVM when in the *Host Mute* operation mode.

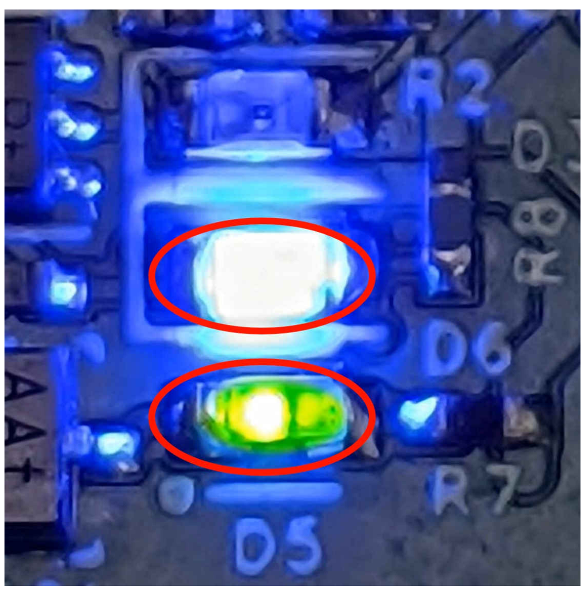



**Figure 2-3. Host Mute Operating Mode LED Status**

4. At start-up in *Host Mute* operation mode, the default content projected is a static image of vertical color bars.
5. Confirm the FTDI cable is connected to the PC. While running DLP Control Program, click on the *Connection* list. If the FTDI cable is not already connected, click the *Connect* button. Note, the Connection settings must be a clock rate of 5 MHz and timeout of 500 ms.

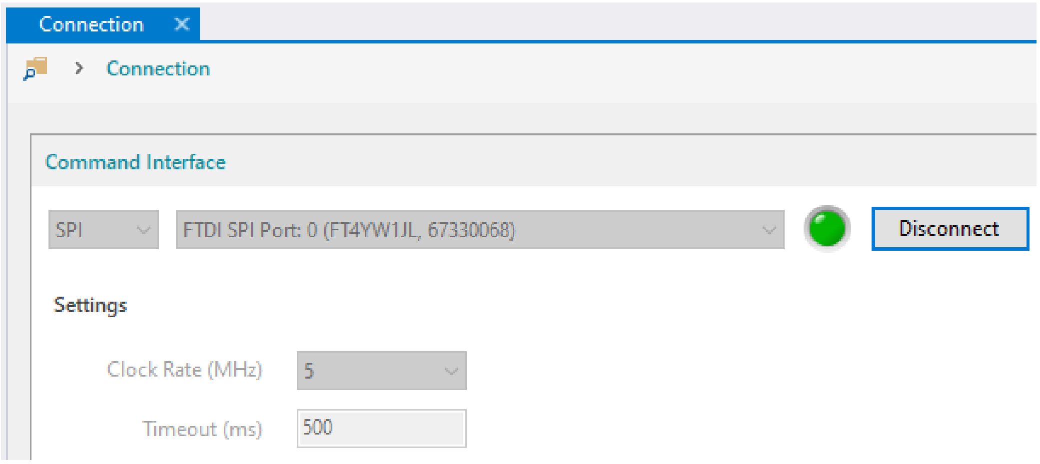



**Figure 2-4. Successful FTDI Cable Connection Established in GUI**

6. Python scripts can be run from the *Scripting* window. The script shown below can be used to select one of the pre-programmed test patterns of the DLP2021-Q1 DGP composer project. Press the green button to run the script, and the projected content toggles between a static image and video.
7. 

```
from dgp.commands import *
#-------------------------------------------------------
#Uncomment one static test pattern
#-------------------------------------------------------
#WriteVideoStartAddress1(0x85980) # Color Bars
#WriteVideoStartAddress1(0x95F64)  # Color Bars Gradient
#WriteVideoStartAddress1(0xC2734) # Solid Black
#WriteVideoStartAddress1(0xD3830) # Solid Red
#WriteVideoStartAddress1(0xE3E14) # Solid Green
#WriteVideoStartAddress1(0xF43F8) # Solid Blue
#WriteVideoStartAddress1(0x1049DC) # Solid White
#WriteVideoStartAddress1(0x114FC0) # Black to White Gradient
#WriteVideoStartAddress1(0x1546C8) # Checkerboard
#WriteVideoStartAddress1(0x179F3C) # MTF Chart
WriteVideoStartAddress1(0x1A2280) # Bird
WriteVideoConfiguration1(1,30)
#-------------------------------------------------------
#Uncomment the desired video test pattern
#-------------------------------------------------------
WriteVideoStartAddress2(0x20A98C) # Race Car
WriteVideoConfiguration2(220,1)
#-------------------------------------------------------
# Configure and run video control
#-------------------------------------------------------
VideoControl = VideoControl()
VideoControl.Play = True
VideoControl.Stop = False
VideoControl.Autostop = False
VideoControl.BufPtr = 0
VideoControl.LoopConfigs = True
VideoControl.ToggleConfigs = True
WriteVideoControl(VideoControl)
```

8. Before closing the GUI, click the *Disconnect* button in the *Connection* window to properly disconnect the FTDI cable interface. If the EVM is power cycled, repeat steps *c* and *d* to select and display content again.

## 2.5 LED Driver

The LED brightness can be controlled through PWM output from DMD controller. Using the DLP Control Program "General" tab, the PWM input text boxes (RPWM DC, GPWM DC, and BPWM DC) control the current through each LED driver channel. Note that the PWM control may exceed the maximum current specification of some LEDs in certain LED configurations. Table 2-2 provides reference conversions from PWM level to drive current for commonly used current levels.

**Table 2-2. LED PWM Drive Current Conversion Reference**

| PWM LEVEL (10-bit) | DRIVER CURRENT (mA) |
|---|---|
| 0 | ≈ 0[(1)] |
| 128 | 142 |
| 256 | 284 |
| 384 | 426 |
| 450 | 500 |
| 512 | 568 |
| 640 | 710 |
| 768 | 852 |
| 896 | 995 |
| 1024 | 1137 |

(1) Some current will continue to flow through the LED with a PWM level of 0 and light output may still be visible. To fully remove LED current, the DMD controller must be set to disable the PWM outputs.

**Note**

The RGB LEDs included with the DLP2021LEQ1EVM have maximum continuous forward current ratings of 0.5 A, and maximum forward current pulsed ratings of up to 1 A. Though the LED driver of the EVM is capable of driving above 1 A per channel, TI does not recommend driving beyond 500 mA for extended periods to prevent damage to the EVM due to individual component temperature ratings and thermal management limitations.

# 3 Optics and Mechanics

Both optics and recommended heat sinks (DMD and LED) are included with the DLP2021-Q1 Light Engine EVM. These heat sinks have been designed to operate the DLP2021-Q1 DMD and LEDs within their data sheet specifications.

# 4 Software

## 4.1 DLP Composer

DLP Composer for DLP2021-Q1 is a software tool that allows users to configure and generate firmware flash data for the DMD controller of the EVM. In the case of the DLP2021LEQ1EVM, the firmware file generated is specific to the FPGA based DMD controller, and loaded into external SPI flash memory. The DMD controller executes commands to read image/video content from the SPI flash memory, and processes the content into the Data Rate (DDR) interface format compatible with the DLP2021-Q1 data bus. The image/video content must be flashed into the external SPI flash memory prior to running the GUI. Image/video content cannot be uploaded or streamed in real-time to the DMD controller.

The DLP Composer DGP process is explained with more detail in the *DLP3021-Q1 Dynamic Ground Projection System Design* (DLPA086) report.

### 4.1.1 Default Register Configuration

This page determines the default start-up conditions of select DMD controller registers. Certain registers enable read and write permissions during typical operation to allow settings to be changed after flash programming, while certain registers only allow read permissions after flash programming during typical operation. See the *DLP3021-Q1 FPGA User's Guide* (DLPU100) for details on each register.

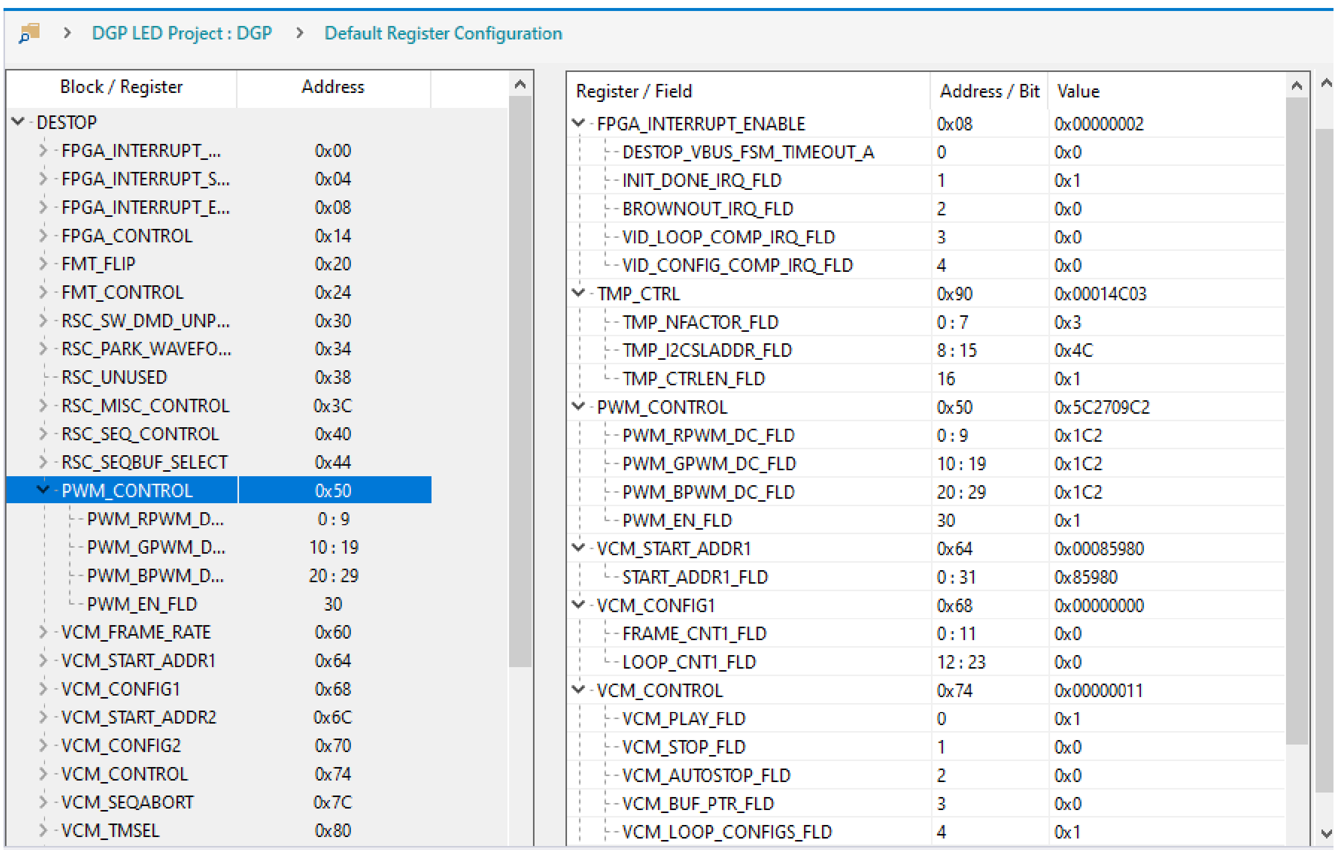


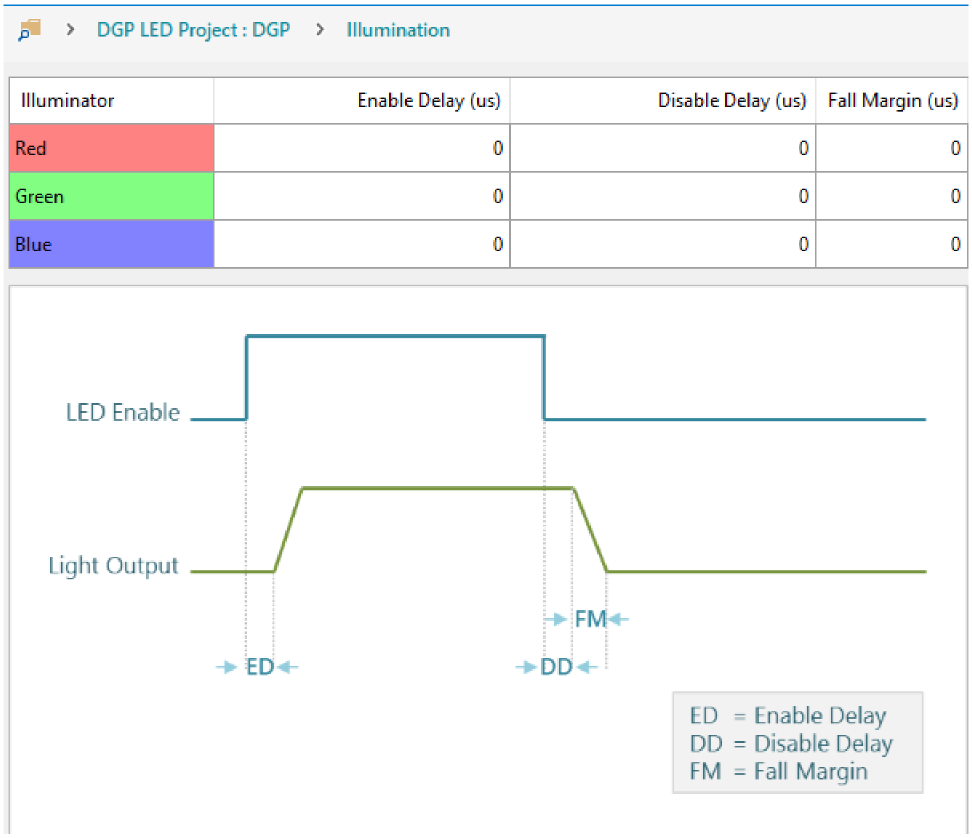

**Figure 4-1. DLP Composer - Default Register Configuration**

Key settings to configure on this page include:

- whether or not content should be displayed immediately after power-up.
- the ready state default display content immediately after power-up.
- the PWM and duty cycle of each LED driver, and the PWM enable state.

### 4.1.2 Illumination

This page allows the DMD controller to introduce additional enable delay, disable delay, and fall margin to the LED illumination transition states. Though not always required, some LEDs or applications may require this additional delay for power budget optimization, more precise LED on/off timing, calibration, dimming, or other LED driver related countermeasures. To prioritize brightness, the delays should be disabled or kept as short as possible.



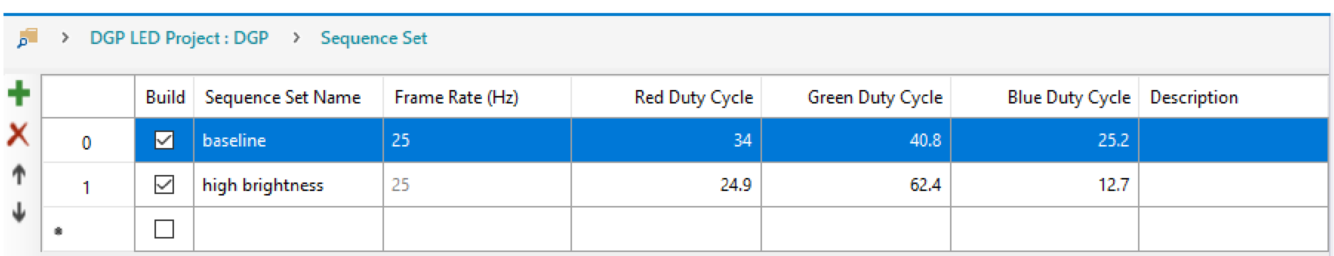

| Illuminator | Enable Delay (us) | Disable Delay (us) | Fall Margin (us) |
|---|---|---|---|
| Red | 0 | 0 | 0 |
| Green | 0 | 0 | 0 |
| Blue | 0 | 0 | 0 |

**Figure 4-2. DLP Composer - Illumination**

### 4.1.3 Sequence Set

The sequence sets determine the frame rate and duty cycle partition of each RGB color. The recommended frame rate is 25 Hz. Ideally, the duty cycle of the three color (red, green, and blue) would be split equally at 33% each; however, a larger green duty cycle is recommended to achieve a higher brightness output.

For a single color or monochromatic LED, set the duty cycle of a single channel to 100%, and the other two channels to 0%. In the case of the White LED variant of the EVM, the green channel must be used.




| | Build | Sequence Set Name | Frame Rate (Hz) | Red Duty Cycle | Green Duty Cycle | Blue Duty Cycle | Description |
|---|---|---|---|---|---|---|---|
| 0 | ☑ | baseline | 25 | 34 | 40.8 | 25.2 | |
| 1 | ☑ | high brightness | 25 | 24.9 | 62.4 | 12.7 | |
| * | ☐ | | | | | | |

**Figure 4-3. DLP Composer - Sequence Set**

The TI created project will include two sequences: baseline and high brightness. TI recommends using the baseline sequence for optimal color, and only using the high brightness sequence to maximize the lumens output.

The duty cycling of each color is made possible through the use of a multiplexer with active channel selection by the PWM_SEL_0 and PWM_SEL_1 pins of the FPGA. This, in combination with the overall LED driver, PWM of each color, and shunt enable, gives the ability to select different current limits for each of the colors, which is important for color calibration and dimming the image for thermal derating.

### 4.1.4 Degamma Curves

This page allows the use to select one of five different gamma profile curves that apply identically to all three RGB channels:

- *enhanced.dgm* – Enhanced: More bits allocated to low light levels where steps in brightness are more noticeable to human perception. Recommended for full range of brightness intensities.
- *enhphoto.dgm* – Enhanced Photo: Same as Enhanced with a more linear mapping in the high brightness range.
- *linear.dgm* – Linear: Pass through of input to out pixel intensity where pixel intensity remains unchanged. Recommended for high brightness content.
- *maxbright.dgm* – Same as enhanced, but steeper slope to reach high brightness content saturation sooner. Recommended for binary content that is a combination of very low and high brightness content as middle range resolution is reduced.
- *photo.dgm* – Photo: More bits allocated to low and medium light levels. Recommended for content where high brightness is less of a priority.

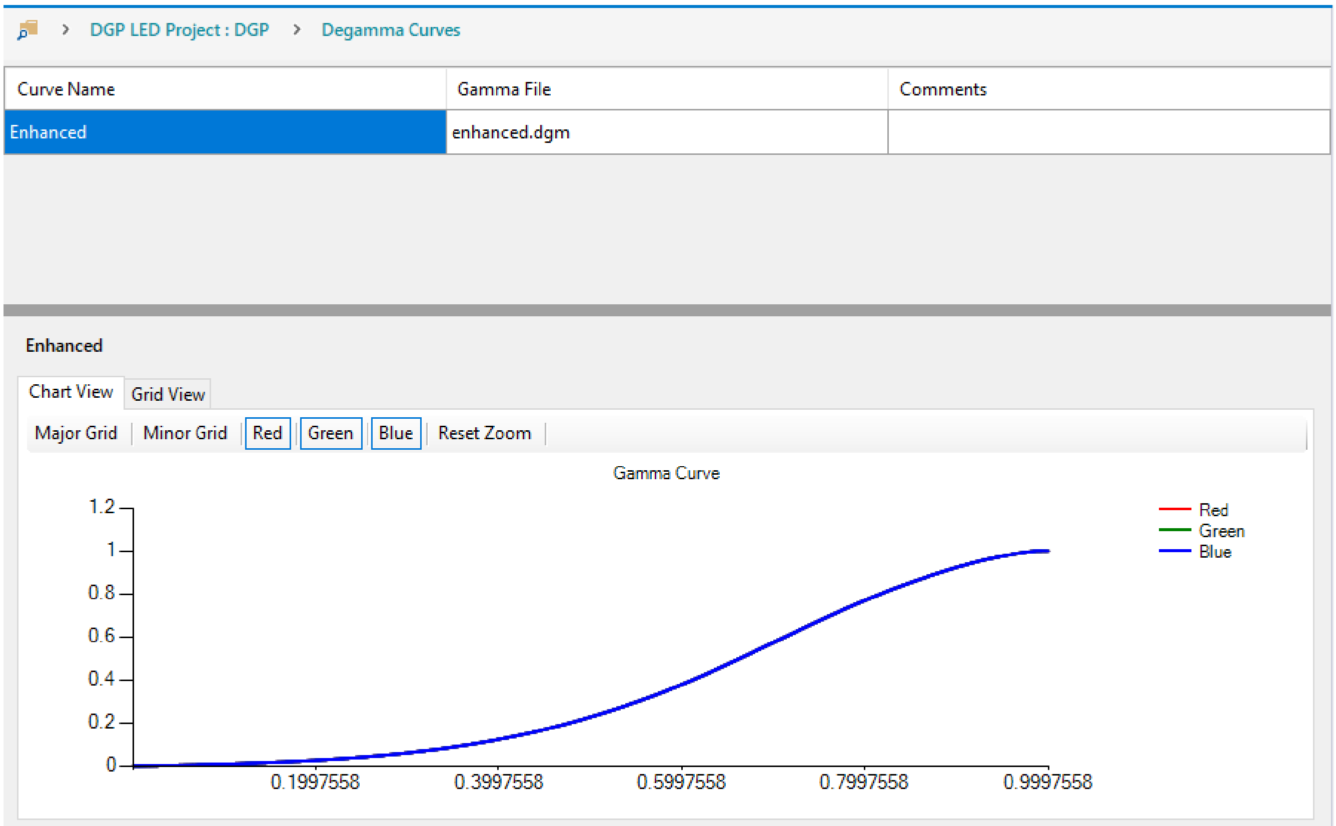


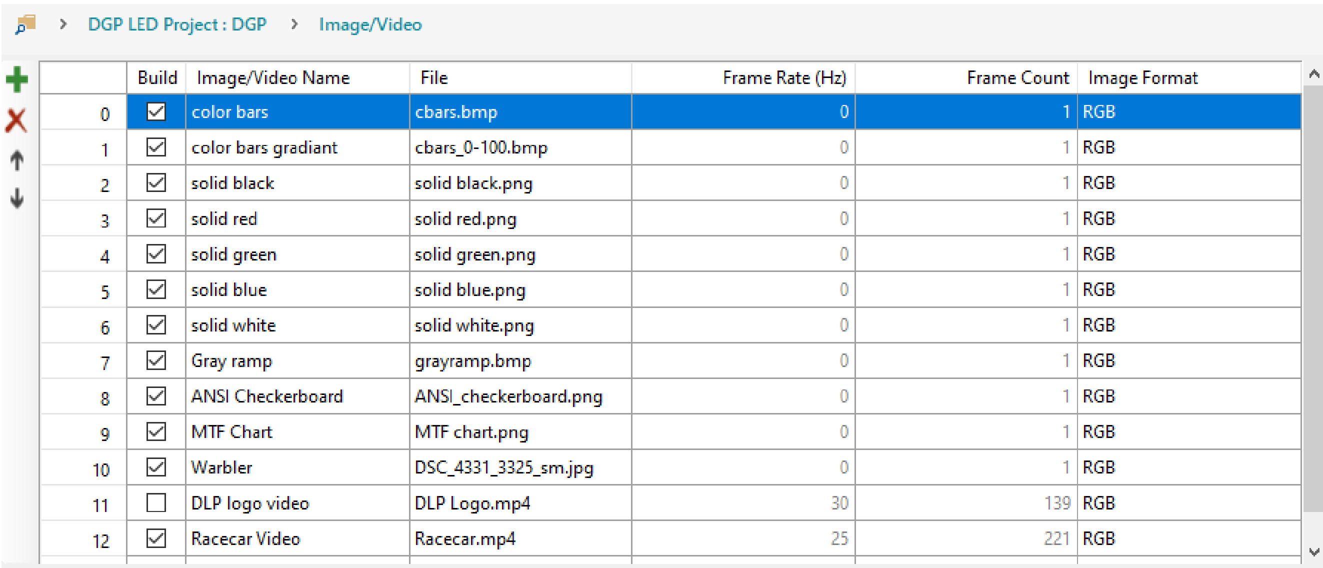

**Figure 4-4. DLP Composer - Degamma Curves**

Gamma correction is a method of adjusting the mapping of input to output pixel intensity levels that is generally used to account for visual perception of brightness. This process is common to most display and camera systems. The human visual system does not perceive light intensity linearly. Humans are more capable of perceiving fine brightness differences in low light intensity levels than they are in bright intensity levels. Therefore, source video content is typically gamma encoded to optimize bit allocation by providing more bits to low light levels where steps in brightness will be most noticeable. Then, the display will apply a corresponding de-gamma curve to decode the input bits into corresponding display brightness.

See the *DLP5531-Q1 Chipset Video Processing for Light Control Applications* (DLPA101) for additional details on the effects of gamma curves.

### 4.1.5 Image/Video

This page allows the user to select the image/video content that is to be programmed into the SPI flash memory. For the content to be a selectable option, the image/video file must be available in the following directory DLP Composer project: "*(dgp_project_root)\Inputs\Videos*". Check the *Build* check box for the contented to included or excluded from the firmware build.




| | Build | Image/Video Name | File | Frame Rate (Hz) | Frame Count | Image Format |
|---|---|---|---|---|---|---|
| 0 | ☑ | color bars | cbars.bmp | 0 | 1 | RGB |
| 1 | ☑ | color bars gradiant | cbars_0-100.bmp | 0 | 1 | RGB |
| 2 | ☑ | solid black | solid black.png | 0 | 1 | RGB |
| 3 | ☑ | solid red | solid red.png | 0 | 1 | RGB |
| 4 | ☑ | solid green | solid green.png | 0 | 1 | RGB |
| 5 | ☑ | solid blue | solid blue.png | 0 | 1 | RGB |
| 6 | ☑ | solid white | solid white.png | 0 | 1 | RGB |
| 7 | ☑ | Gray ramp | grayramp.bmp | 0 | 1 | RGB |
| 8 | ☑ | ANSI Checkerboard | ANSI_checkerboard.png | 0 | 1 | RGB |
| 9 | ☑ | MTF Chart | MTF chart.png | 0 | 1 | RGB |
| 10 | ☑ | Warbler | DSC_4331_3325_sm.jpg | 0 | 1 | RGB |
| 11 | ☐ | DLP logo video | DLP Logo.mp4 | 30 | 139 | RGB |
| 12 | ☑ | Racecar Video | Racecar.mp4 | 25 | 221 | RGB |

**Figure 4-5. DLP Composer - Image/Video**

This EVM allows users to store approximately twenty seconds of full-color content in the 2-Gb SPI flash device. However, content duration can be increased by optimizing content and setting the correct illumination (RGB or single color) to match the type of content being displayed. The video content must be in .MP4 format to be compatible with DLP Composer.

### 4.1.6 Flash Blocks

The flash memory for the DGP system is divided into five major blocks. Creation of the flash binary is handled entirely by DLP Composer. The FPGA Configuration for the Xilinx XA7S15-1CPGA196Q Spartan®-7 FPGA is already compiled and included with the example project provided by Texas Instruments.

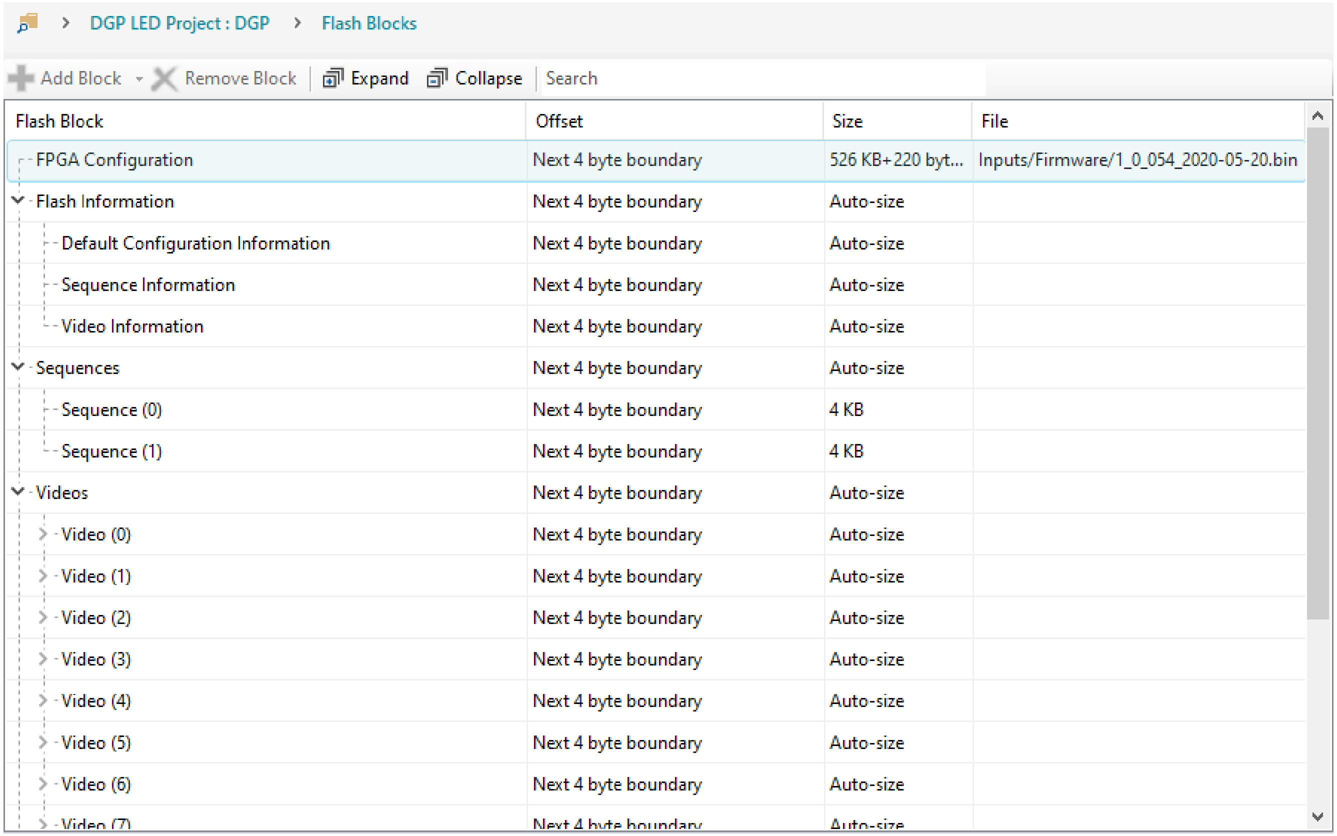



**Figure 4-6. DLP Composer - Flash Blocks**

**Table 4-1. Top Level Flash Structure**

| DATA | ADDRESS | LENGTH |
|---|---|---|
| FPGA Configuration | 0x0 | 0x838DC |
| Flash Information | 0x83900 | Variable |
| Default Configuration (Defconfig) | Variable | Variable |
| Sequence 1 | Variable | 0x1000 |
| Sequence 2 | Variable | 0x1000 |
| Sequence … | Variable | 0x1000 |
| Sequence n | Variable | 0x1000 |
| Video / Image 1 | Variable | Variable |
| Video / Image 2 | Variable | Variable |
| Video / Image … | Variable | Variable |
| Video / Image n | Variable | Variable |

*FPGA Configuration*

The FPGA configuration block is always located at address 0x0, and is always a fixed size of 0x838DC bytes. This size is derived from the Xilinx XA7S15 specification for maximum configuration length. See the Xilinx UG470 (https://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf) for additional details.

*Flash Information*

The flash information block provides metadata regarding the contents of the flash. This is intended to allow an external MCU or software tool understand the contents of the flash. For example, it defines the locations of the videos within flash so that they can be loaded dynamically by an MCU, such as the MSP430G2553-Q1 on the EVM. The flash information block is divided into four main sections as shown in Table 4-2. Information such as the number of sequences is provided so that software can navigate the flash block and determine the correct offset for the data of interest. The number of sequence and video entries in the information block is variable, but each entry is a fixed size.

**Table 4-2. Flash Information Block**

| Offset (HEX) | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 00 | Major | Minor | Patch | |
| 04 | "D" | "E" | "F" | "C" |
| 08 | Block Address | | | |
| 0C | Count (Number of Register Writes) | | | |
| 10 | "S" | "E" | "Q" | "L" |
| 14 | Size (of Sequence Block) | | | |
| 18 | Count (Number of Sequences) | | | |
| 1C | Sequence 0 Address | | | |
| 20 | Seq 0 Red Duty Cycle | | Seq 0 Green Duty Cycle | |
| 24 | Seq 0 Blue Duty Cycle | | Seq 0 Frame Rate | |
| 28 | Sequence 1 Address | | | |
| 2C | Seq 1 Red Duty Cycle | | Seq 1 Red Duty Cycle | |
| 30 | Seq 1 Blue Duty Cycle | | Seq 1 Blue Duty Cycle | |
| 34 | Sequence … Address | | | |
| 38 | Seq … Red Duty Cycle | | Seq … Red Duty Cycle | |
| 3C | Seq … Blue Duty Cycle | | Seq … Blue Duty Cycle | |
| Variable | "V" | "I" | "D" | "E" |
| Variable | Size (of Video Block) | | | |
| Variable | Count (Number of Videos) | | | |
| Variable | Video 0 Address | | | |
| Variable | Video 0 Frame Rate | | Video 0 Frame Count | |
| Variable | Video 1 Address | | | |
| Variable | Video 1 Frame Rate | | Video 1 Frame Rate | |
| Variable | Video … Address | | | |
| Variable | Video … Frame Rate | | Video … Frame Rate | |

*Sequences*

Sequences are generated by DLP Composer based on the duty cycle selection. Each sequence entry is reserved 4kB in flash.

*Videos*

Videos and still image content are an input to a dynamic ground projection project in DLP Composer. Composer takes the content, scales it, converts it to a sequence of DMD native format bit-planes, and compresses it using run length encoding (RLE) for storage in flash. When a video or still image is to be shown, the FPGA decompresses each bit-plane and displays in the order and with the timings specified by the sequence.

*Default Configuration*

The default configuration block is the set of values for each of the FPGA registers. This information is loaded by the FPGA after the completion of the FPGA configuration. These values supersede the power-on default values described in the *DLP2021-Q1 FPGA User's Guide*. Default configuration values can be set using DLP Composer on the *Default Register Configuration* page.

### 4.1.7 Flash Programming

After the DLP Composer project is configured as desired, use the *Flash Programming* page to program and verify the flash binary onto the SPI flash memory of the EVM.

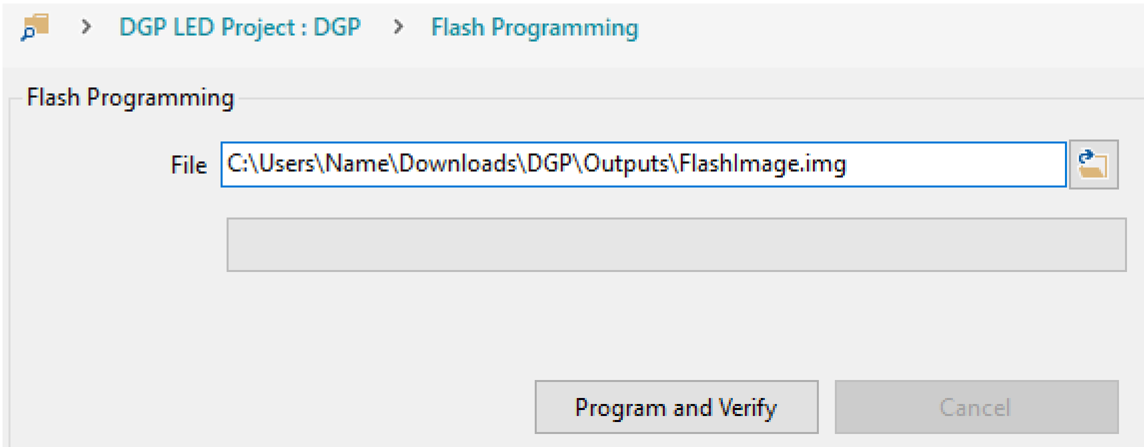



**Figure 4-7. DLP Composer - Flash Programming**

Follow these steps to flash program the EVM:

1. Start with the EVM powered-off.
2. Set the SPI Adapter board to the *Flash Programming* operating mode.
3. Connect the FTDI cable interface to the SPI Adapter Board and PC.
4. Power-on the EVM. Figure 4-8 shows the LED status of the EVM when in the *Flash Programming* operation mode.

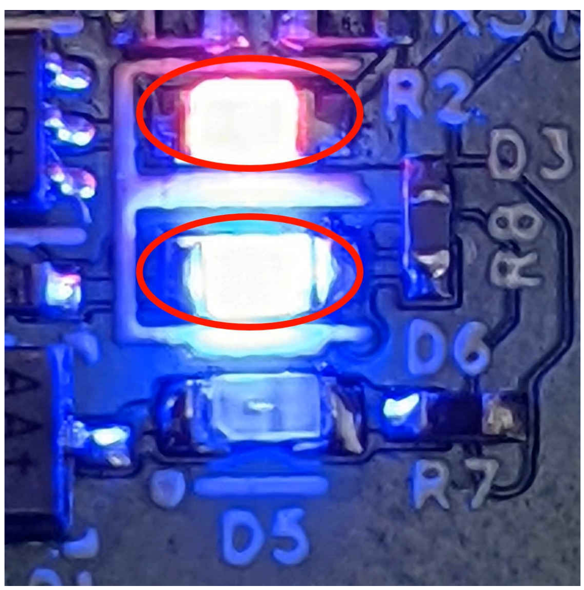



**Figure 4-8. Flash Programming Operating Mode LED Status**

5. Import and open the DLP2021LEQ1EVM DGP project in DLP Composer.
6. Navigate to the Connections tab. Set to *SPI* and *FTDI SPI Port*, then click the *Connect* button. The virtual green LED should illuminate to indicate a successful connection as shown in Figure 4-9.

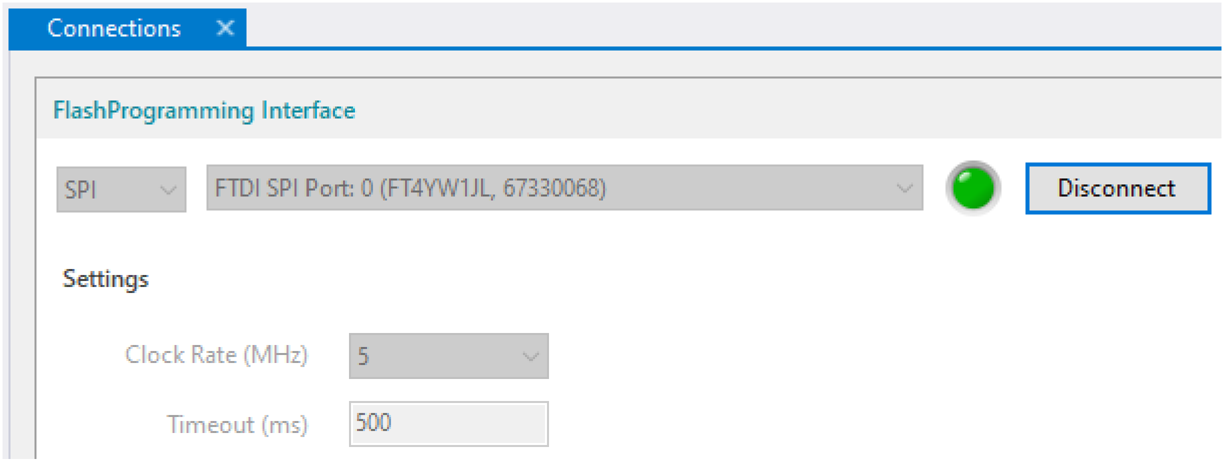



**Figure 4-9. DLP Composer - Connections**

7. Build the DLP Composer project using the *Project* → *Build* from the menu bar. Ensure the build is completed and successful before proceeding. Note, the build time will vary and can take up to several minutes depending on the size of the image/video content block.
8. Navigate to the *Flash Programming* page, and browse to select the flash image file from the following directory: "*(dgp_project_root)\Outputs\FlashImage.img*".
9. Click the *Program and Verify* button to flash program the EVM. Note, the flash programming time will vary and can take up to several minutes depending on the size of the image/video content block.

## 4.2 DLP Control Program

DLP Control Program for the DLP2021-Q1 allows users to use the FTDI cable to issue commands to the FPGA via SPI to read/write registers, enable video playback, change videos, read DMD temperature via the TMP411, or adjust current levels to the LEDs.

To change the DLP Control Program window and pages for DLP2021LEQ1EVM support, navigate to *Product* → *Dynamic Ground Projection for Automotive* in the menu bar.

### 4.2.1 Connection

The first step in running the GUI requires the user to establish connection to the FTDI cable. The GUI will attempt to automatically connect to the FTDI cable at start-up. To manually connect the FTDI cable, navigate to the *Connection* page. With the FTDI cable selected from the drop-down interface list, click the *Connect* button. Note, the Connection settings must be a clock rate of 5 MHz and timeout of 500 ms. When using the Cheetah™ interface, the clock rate can be increased to 16 MHz in SPI Mode 0 and MSB first bit order.

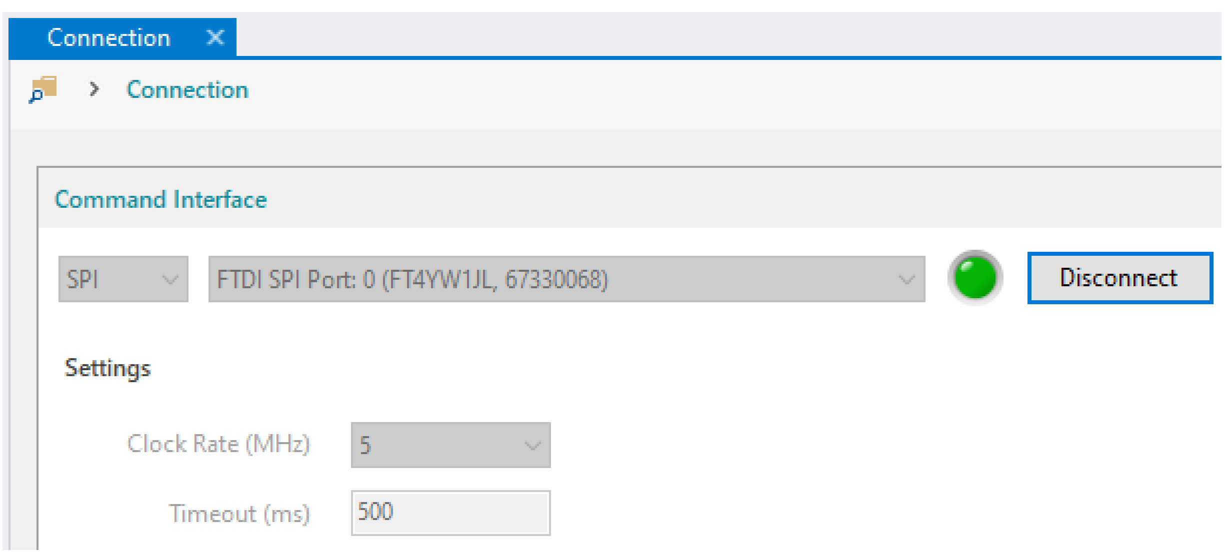



**Figure 4-10. DLP Control Program - Connection**

**Note**

The FTDI cable must be disconnected/released from DLP Composer if DLP Composer was previously used to flash program the EVM. The FTDI cable cannot be shared simultaneously between DLP Composer and DLP Control Program.

### 4.2.2 Scripting

The Scripting page allows for the automated execution of a custom list of SPI-to-FPGA commands to sweep and run a variety of tests. The scripting terminal uses the Python programming language. For example, the Python script can be used to cycle through all the image/video content in a loop for demo purposes.

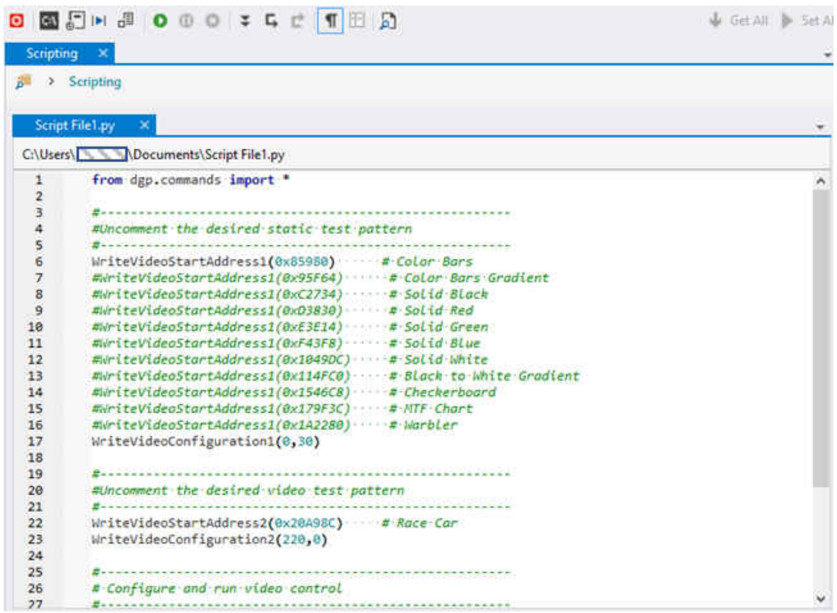



**Figure 4-11. DLP Control Program - Scripting**

To run the Python script, click the green *Run Script* button at the top of the page. If the Python script is not programmed to automatically end, the script can be stopped at any point by clicking the red *Stop Script* button at the top of the page.

For a list of the available functions that the Python script tool can call, navigate to *Help → Scripting Reference* in the menu bar to open the Scripting Reference manual. Each function includes a description and the input/output parameter details.

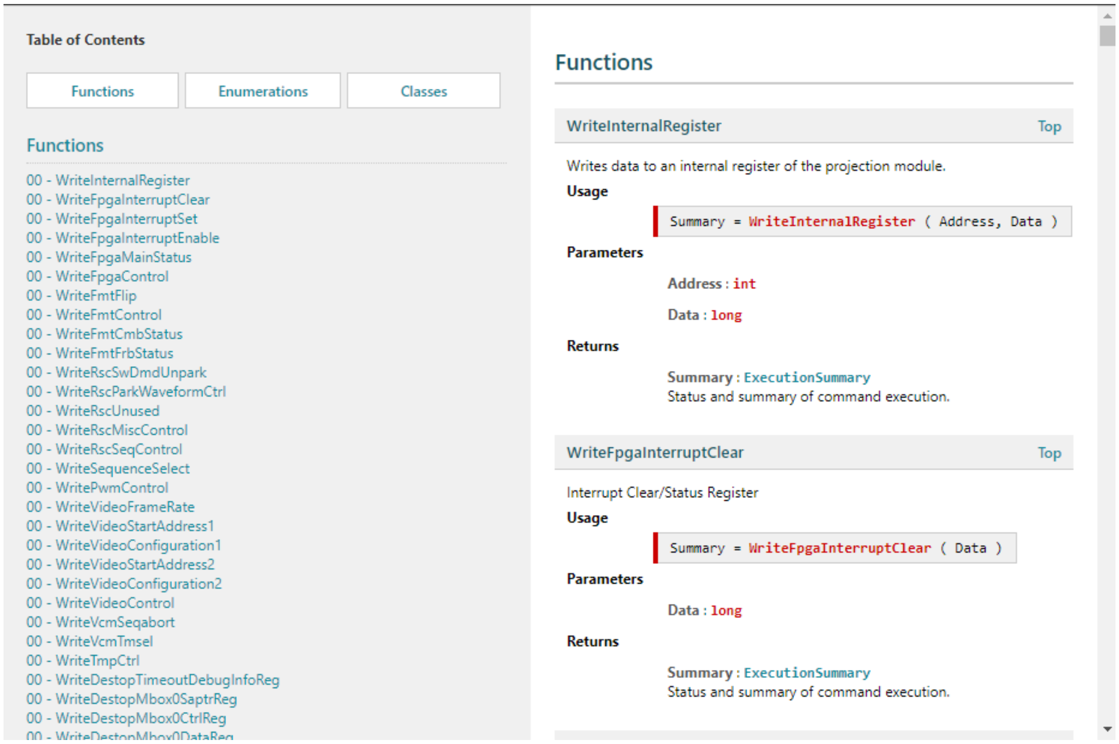



**Figure 4-12. DLP Control Program - Scripting Reference**

### 4.2.3 Registers

The Registers page allows users to perform individual read/writes of the block, register, or bit fields of the FPGA registers.

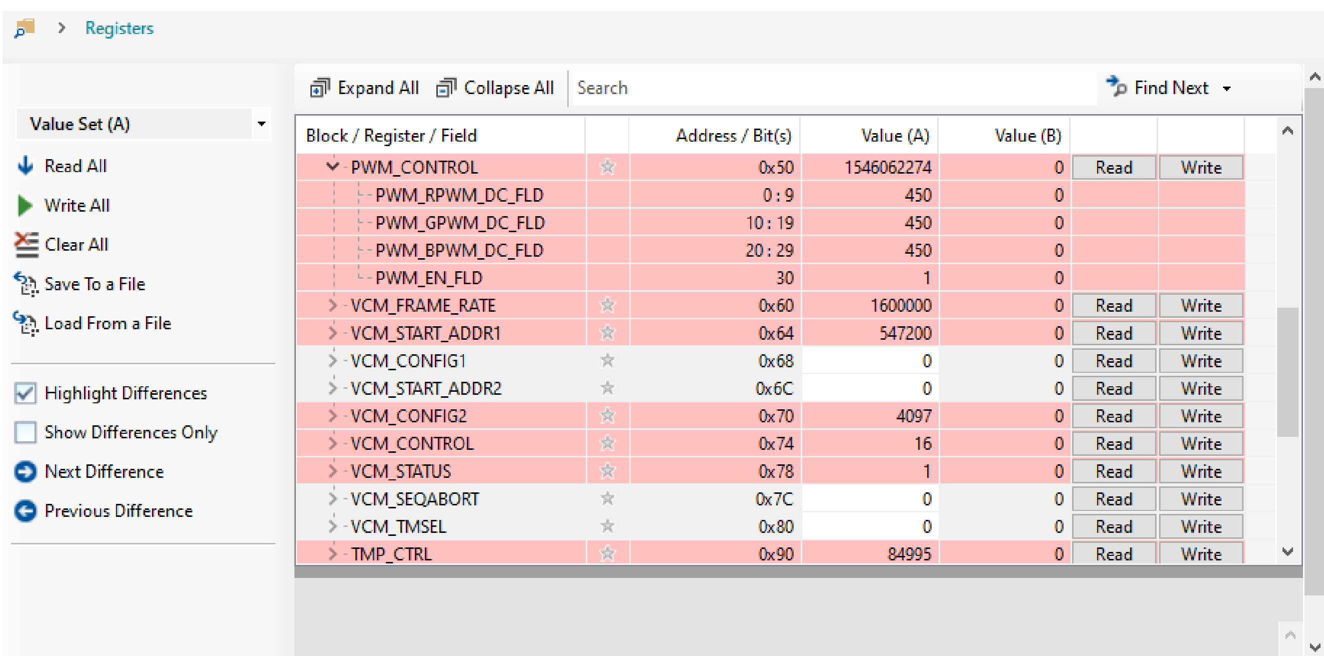



**Figure 4-13. DLP Control Program - Registers**

### 4.2.4 Commands

The commands page allows users to read/write settings in a grouped format. To read the currently set values, click the *Get* button. For commands that enable writes, update the command fields, then click the *Set* button for the values to immediately take effect.

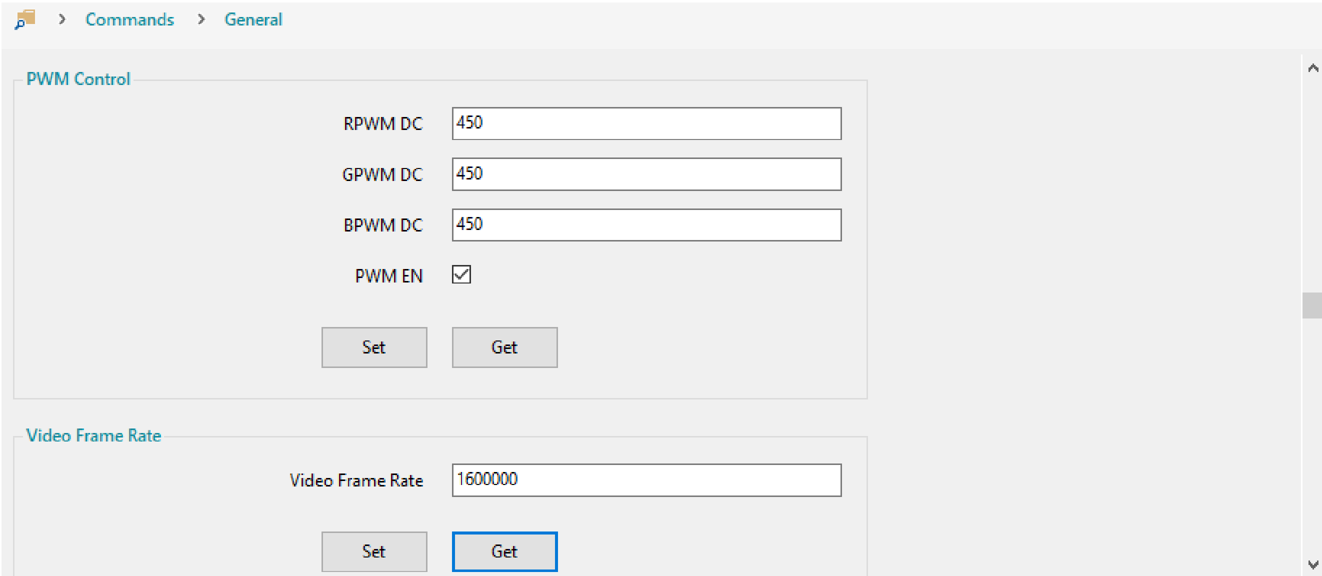



**Figure 4-14. DLP Composer - Commands**

## 4.3 MSP430 Example Code

When power is applied to the system, the FPGA configuration is loaded to the FPGA. Depending on the default configuration, the FPGA begins loading bit-planes to the DMD and sequencing the LED enables for each bit plane loaded. Alternatively, a microcontroller such as the MSP430G2553-Q1 on the EVM, can issue commands to the FPGA via SPI to enable video playback, change videos, read DMD temperature via the TMP411, or adjust current levels to the LEDs. The *MSP430 Example Code* (DLPC138) is a Code Composer Studio example project available for users to edit and refer to for a custom *Local Host Control* operation mode implementation.

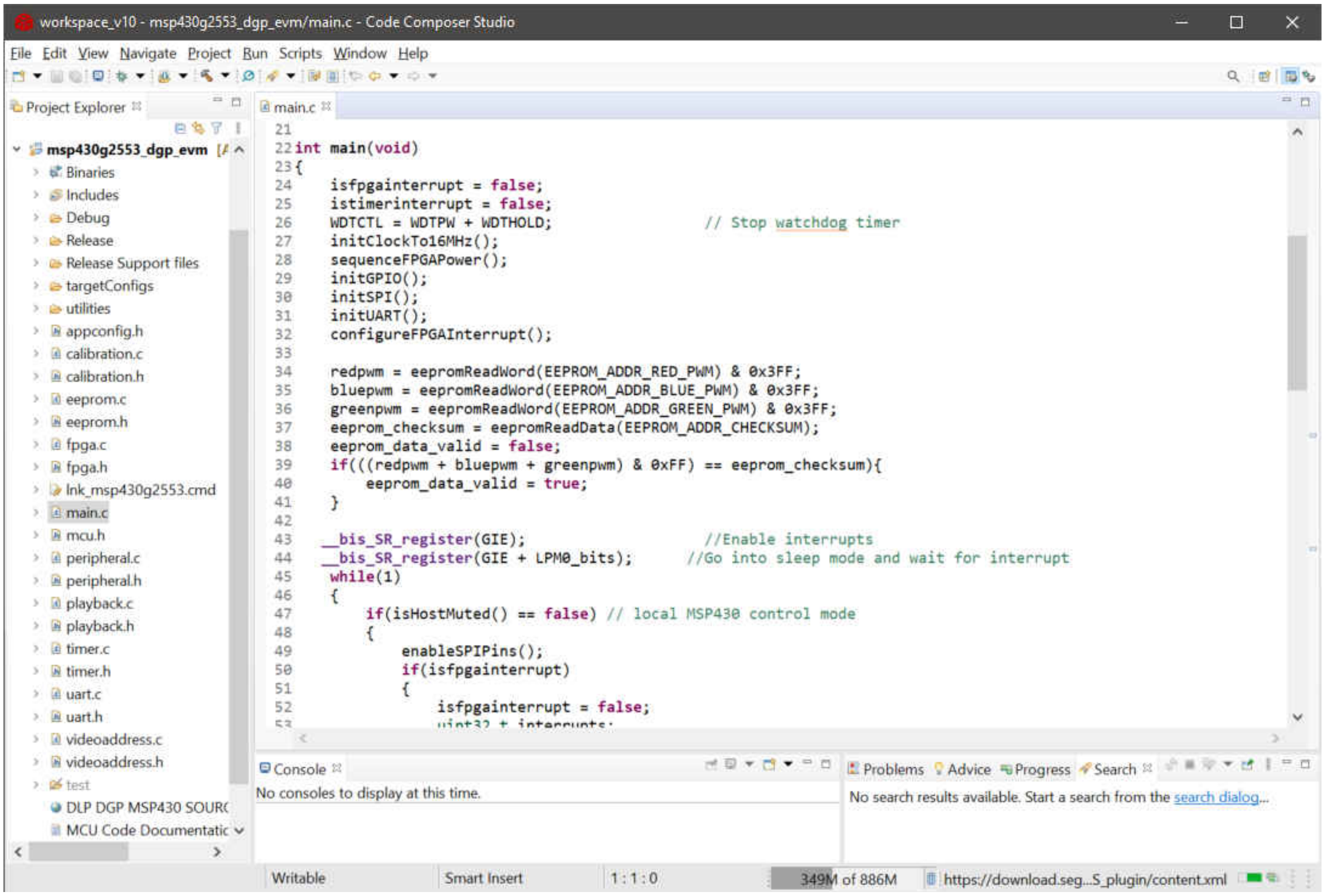



**Figure 4-15. MSP430G2553-Q1 Code Composer Example Project for DGP EVM**

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (December 2021) to Revision A (April 2022) | Page |
|---|---|
| • Added image of EVM showing cooling plate and heat sink variants | 3 |
| • Changed LED States for Table 1-1 | 6 |
| • Changed Light Engine Performance specifications | 8 |
| • Changed LED Driver specifications | 9 |