EVM User's Guide: DLPLCRC964EVM DLPLCR99EVM DLPLCR99UVEVM

DLPC964 and DLP991U/DLP991UUV Evaluation Modules

Description

The DLP® LightCrafter™ DLPC964 evaluation module (EVM) offers a reference design to enable faster development of the DLPC964 controller architecture in support of the DLP991U and DLP991UUV DMDs. This platform receives high-speed bitplane data from an external source through the AMD Aurora 64B/66B interface and formats the bitplane data before loading the data into a DLPLCR99EVM or DLPLCR99UVEVM for display on the DLP991U or DLP991UUV DMD.

Get Started

1. To order the DLPLCRC964EVM, visit the DLPLCRC964EVM Product Page.
2. Refer to the TI E2E DLP products forum for more assistance.

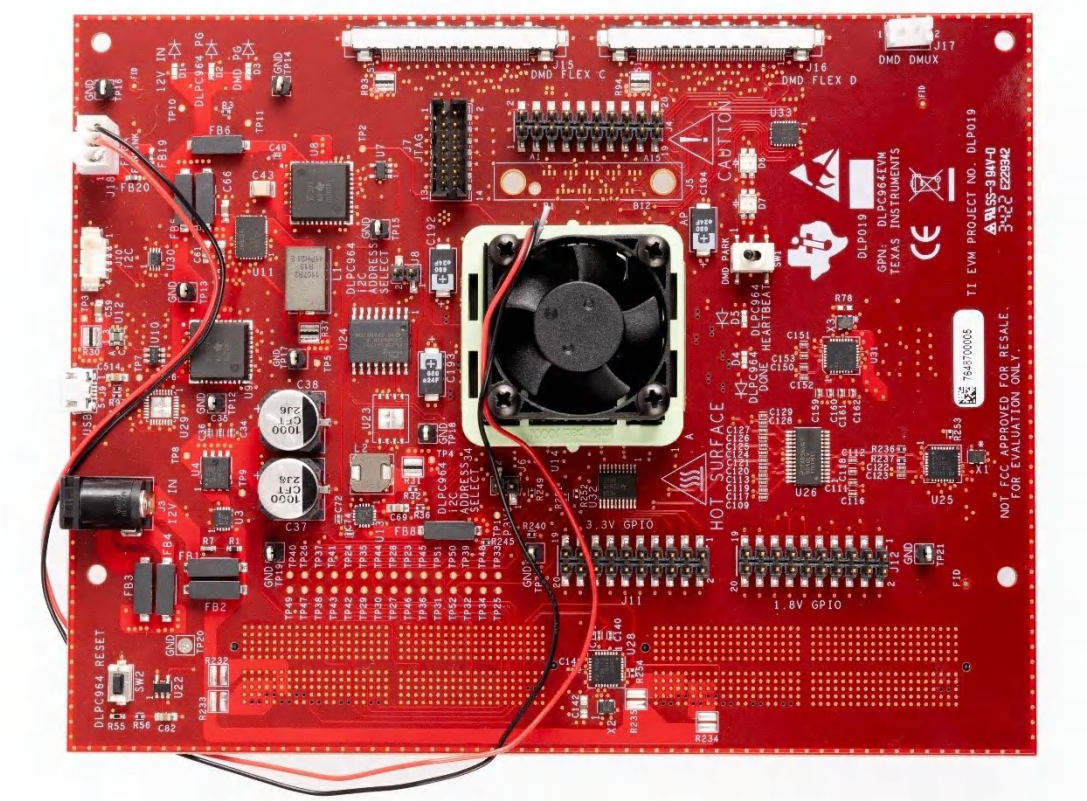
Features

- Controller EVM for the DLPLCR99EVM and DLPLCR99UVEVM
- 12 HSS input Aurora 64B/66B data lanes at 10Gbps per lane
- 32 HSS DMD output data lanes at 3.6Gbps per data lane

Applications

- Digital direct imaging (LDI)
- Maskless lithography
- Additive manufacturing and 3D printing
- Industrial printing
- Dynamic grayscale marking and coding
- High-speed imaging and display

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DLP LightCrafter DLPC964 Evaluation Module

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1 Evaluation Module Overview

1.1 Introduction

The TI DLP DLPC964 GUI enables evaluating the DLPLCRC964EVM (DLPC964 controller board), DLPLCR99EVM (DLP991U DMD board), DLPLCR99UVEVM (DLP991UUV DMD board), and Apps FPGA (AMD EVM) application. The DLPLCRC964EVM contains fixed internal test patterns that can be loaded into DLP991U or DLP991UUV DMD, providing the necessary interfaces for displaying these patterns on the supported DMD. The front-end AMD EVM interfaces with the DLPC964 controller to send high-speed pattern data to the supported DMD EVM (DLPLCR99EVM or DLPLCR99UVEVM).

This guide explains the hardware and software features of the DLP LightCrafter DLPC964 EVM system. The EVM architecture and connectors are described along with a quick start guide on how to assemble a supporting DMD EVM and an AMD Xilinx™ Evaluation board to the DLPLCRC964EVM to display and run test patterns. This guide also explains how to operate the DLP LightCrafter DLPLCRC964EVM using a Graphical User Interface (GUI). Specific details for each DLP component can be found in Section 6.

Note

The DLPLCR99EVM (DMD EVM), DLPLCR99UVEVM (DMD EVM), AMD Xilinx UltraScale+™ Evaluation board (Apps FPGA), optics, illumination source, and power supply are sold separately from the DLPLCRC964EVM kit.

1.2 Kit Contents

The DLPLCRC964EVM is a flexible, ready-to-use evaluation module. When the DLPLCRC964EVM is coupled with the DLPLCR99EVM or DLPLCR99UVEVM with an Apps FPGA board, the DLPLCRC964EVM enables the capability of sending customer-created patterns to the DLPC964 Controller and then to the attached DLP991U or DLP991UUV DMD for display. The DLP LightCrafter DLPC964EVM and supported DLP991U or DLP991UUV DMD EVM are offered for purchase separately so that customers can determine which elements are needed for the application.

The following items are not included with the EVM and need to be purchased separately if needed for evaluation:

- Supported DMD EVM board (DLPLCR99EVM or DLPLCR99UVEVM)
- APPS FPGA board: example: AMD Evaluation Board (with separate power supply)
- Power supply: see Section 2.1.1 for more details
- USB cable: Type A to Micro-B USB cable

1.3 Specification

The DLPLCRC964EVM contains the electronics capable of controlling the supported DLP991U DMD. This EVM offers several interface options including USB, I^2C, HPC FMC connectors, and Flex Cables connectors. Figure 1-1 shows the EVM Hardware Block diagram of the DLPLCRC964EVM.

The major components of DLPLCRC964EVM are:

- DLPC964 Digital DMD Controller
- Power Management Unit to support the DLPC964 subsystem
- DLPC964 configuration Flash memory
- USB 2.0 interface
- Flex Cables: Four are needed to support the DLP991U DMD EVM board
- HPC FMC Connectors: Two for an attached Apps FPGA or other front-end board

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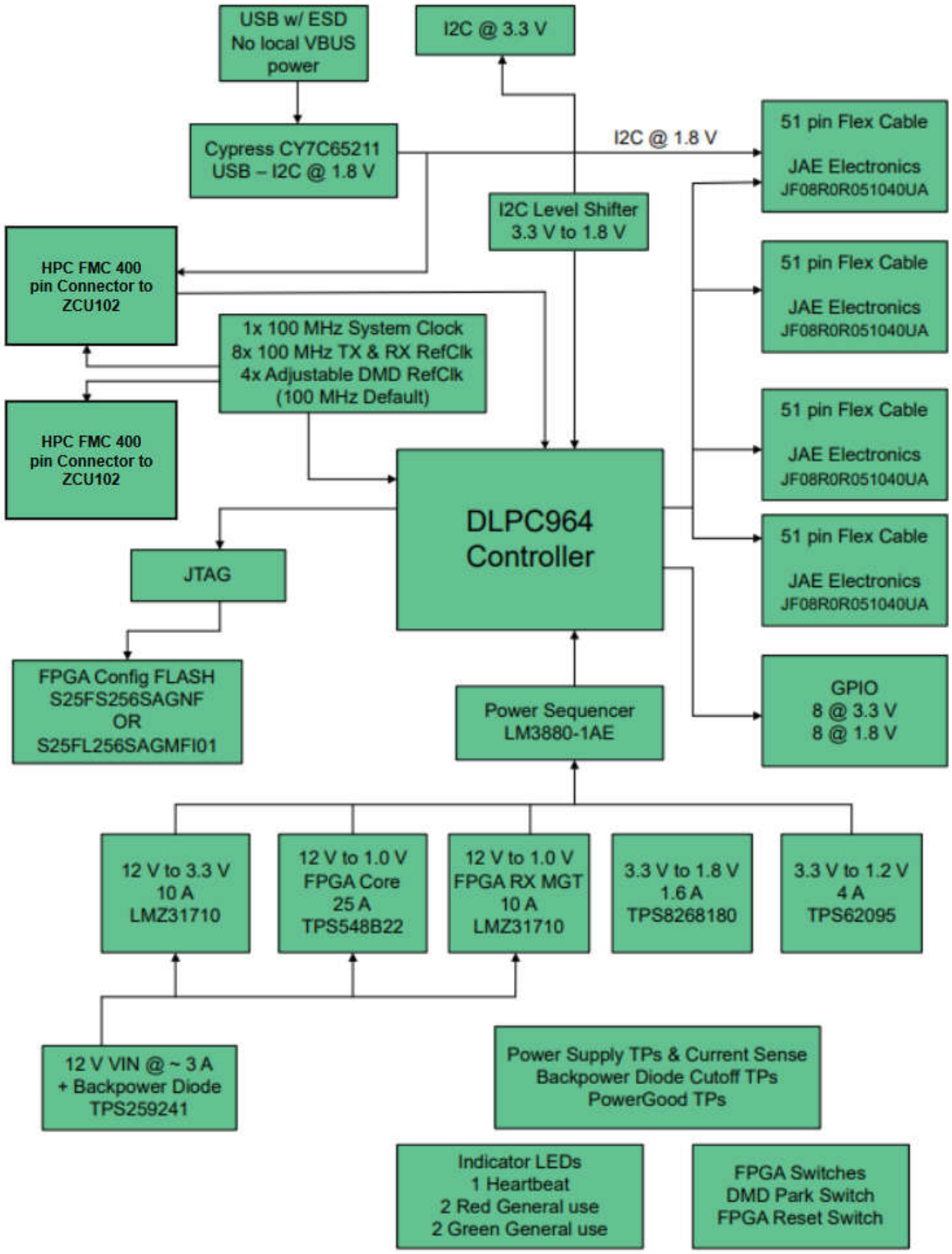


Figure 1-1. DLP LightCrafter DLPC964 EVM Block Diagram

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1.4 Device Information

The DLP LightCrafter DLPC964 EVM is one-third of a complete DMD imaging electronics subsystem. The DLP LightCrafter DLPC964 EVM consists of the DLPC964 board which includes a DLPC964 Digital Controller, USB interface, power management circuits, and supported digital logic.

Also needed to complete the imaging subsystem is a compatible DLPLCR99EVM or DLPLCR99UVEVM. Both DMD EVMs are compatible with the DLPLCRC964EVM and the AMD Xilinx UltraScale+ EVM or other front end to send patterns to the DLPC964 controller. The DLPLCR99EVM and DLPLCR99UVEVM consist of a DMD, a DMD board (PCB) containing on-board DMD power circuits, DMD mounting hardware, and Flex Cables for connections to the DLPLCRC964EVM and DLPLCR99EVM or DLPLCR99UVEVM.

Figure 1-2 outlines the major hardware components of a DLPLCRC964EVM System Hardware.

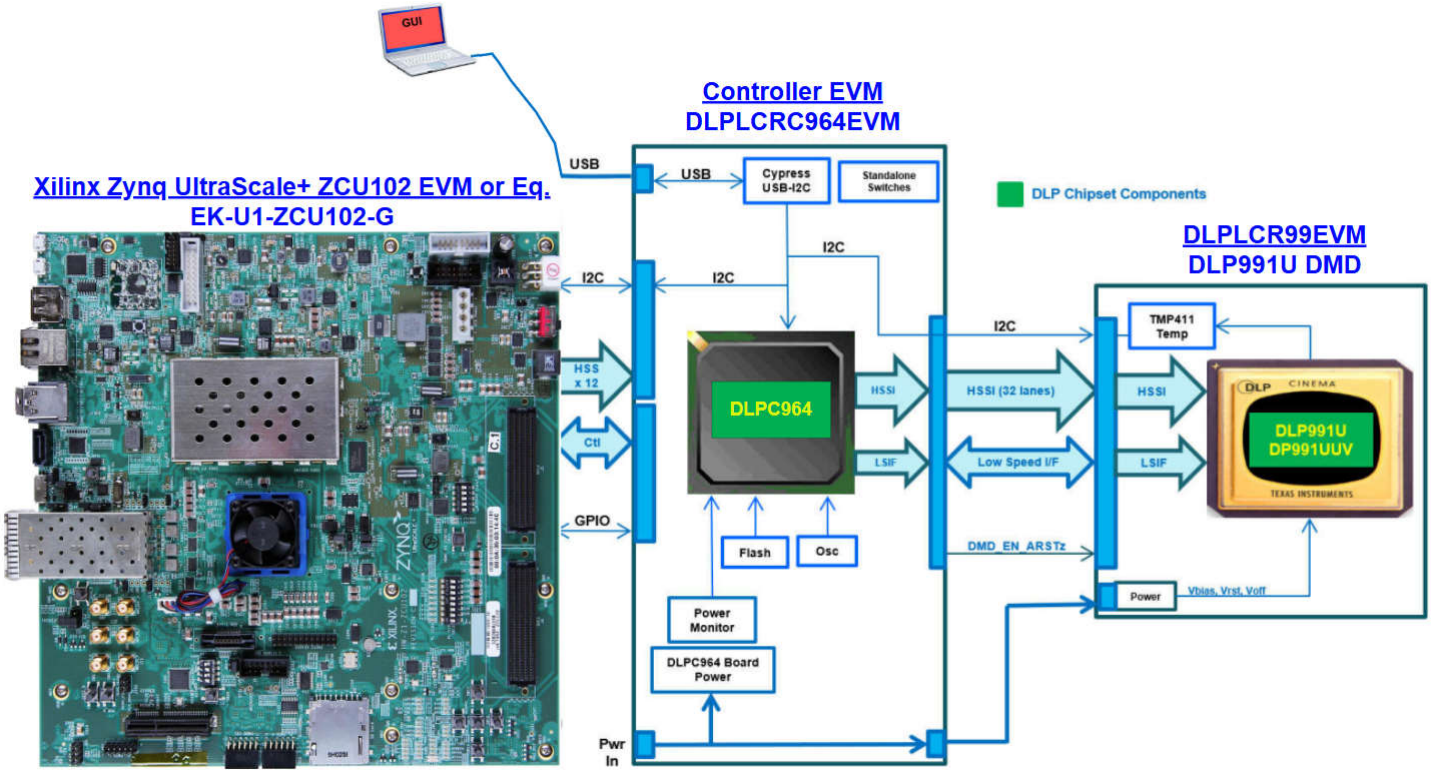


Figure 1-2. DLPLCRC964EVM Hardware Components

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2 Hardware

2.1 DLPLCRC964EVM Power Supply Requirements

2.1.1 External Power Supply Requirements

The DLP LightCrafter DLPC964 EVM does not include a power supply. The external power supply requirements are:

- Nominal voltage: 12V DC -5%/+10%
- Current: 5A
- DC connector size:
  - Inner diameter: 2.5mm
  - Outer diameter: 5.5mm
  - Shaft: 9.5mm socket, center positive
- A recommended power supply is Digi-Key part number 102-3811-ND or equivalent.

Note

External Power Supply Regulatory Compliance Certifications: TI recommends selecting and using an external power supply that meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory and safety certification requirements such as UL, CSA, VDE, CCC, and PSE.

2.2 DLPLCRC964EVM Connections

Figure 2-1 depicts the DLPLCRC964EVM switches and connectors with the respective locations.

Note

The DLPLCR99EVM, DLPLCR99UVEVM, Apps FPGA, power supply, and USB cable are NOT included with the module.

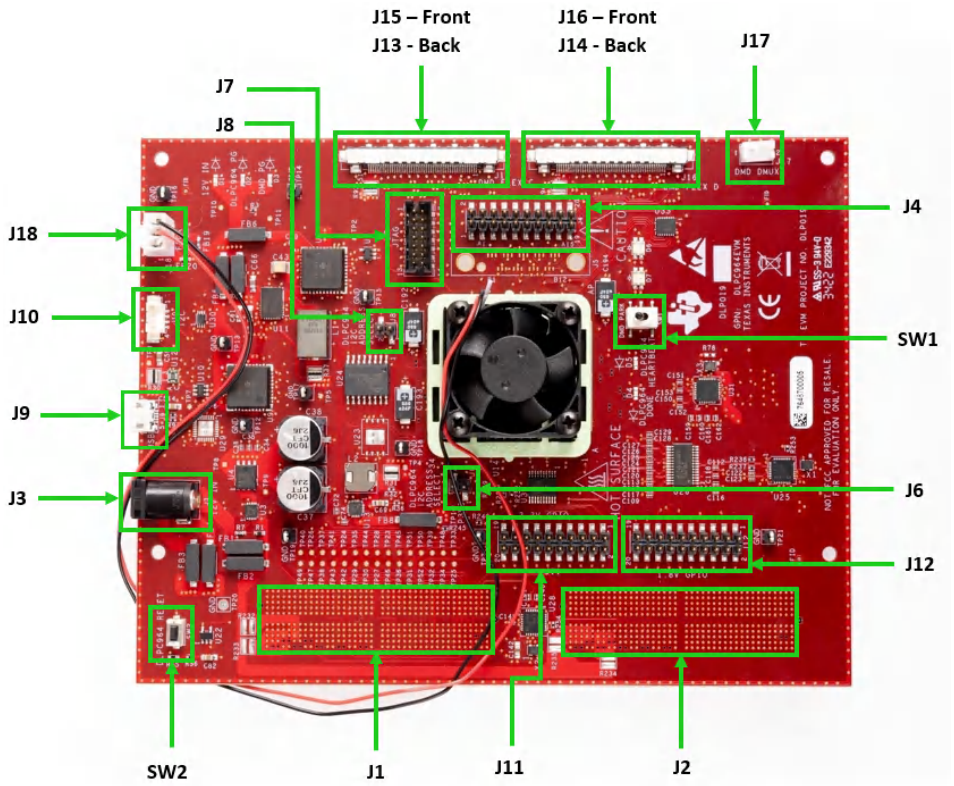


Figure 2-1. DLPLCRC964EVM Connectors (Top View)

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2.2.1 J1, J2—HPC FMC Connector (Plug)

The 400 position HPC FMC plug connectors J1 and J2 are used to connect a front-end Apps FPGA (AMD Evaluation Board) to the DLPLCRC964EVM Board. The Apps FPGA is used to help enable customers with interfacing to the DLPC964 Controller for sending high-speed pattern data to the DLP991U DMD.

The matching part numbers are:

- Samtec part number: SEAF-40-05.0-S-10-2-A-K-TR
- Digi-Key part number: SAM8009CT-ND

If using ribbon cables to connect between the front-end Apps FPGA and DLPLCRC964EVM Board, the matching part numbers are:

- Samtec part number: ASP-134488-01 or ASP-134602-01
- Digi-Key part number: SAM8730-ND or 612-ASP-134602-01CT-ND

2.2.2 J3—Input Power

Connecter J3 accepts a +12 VDC input power to the DLPLCRC964EVM board. The power socket J3 pins are shown in Table 2-1.

The matching part numbers are:

- CUI Devices part number: PP3-002A
- Digi-Key part number: CP3-1000-ND

Note

The power supply and cable are not included inside the DLPLCRC964EVM kit and needs to be purchased separately. Please see Section 2.1.1 for more details.

Table 2-1. Power Connector Pins

Description	Pin	Supply Range
Input supply	1	12+ V DC –5%/+10%
Ground	2	0V
Ground	3	0V

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2.2.3 J4—TestMux Connector

The TESTMUX connector J4 pins are shown in Table 2-2.

Table 2-2. TESTMUX Connector Pins

Description	Pin	Supply Range
Ground	1	0V
Ground	2	0V
TESTMUX_0	3	1.8V
TESTMUX_8	4	1.8V
TESTMUX_1	5	1.8V
TESTMUX_9	6	1.8V
TESTMUX_2	7	1.8V
TESTMUX_10	8	1.8V
TESTMUX_3	9	1.8V
TESTMUX_11	10	1.8V
TESTMUX_4	11	1.8V
TESTMUX_12	12	1.8V
TESTMUX_5	13	1.8V
TESTMUX_13	14	1.8V
TESTMUX_6	15	1.8V
TESTMUX_14	16	1.8V
TESTMUX_7	17	1.8V
TESTMUX_15	18	1.8V
Ground	19	0V
Ground	20	0V

2.2.4 J6, J8—I^2C Address Selectors

The I^2C_ADDR_SEL[1:0] input pins allow the user to select the DLPC964 I^2C Secondary address. Table 2-3 describes the relationship between the I2C_ADDR_SEL[1:0] pins and the DLPC964 I2C Secondary address.

Note

If pins are left unconnected, the default I^2C address is 0x0C.

Table 2-3. DLPC964 I^2C Secondary Address Selection Table

I^2C_ADDR_SEL[1]	I^2C_ADDR_SEL[0]	I^2C Secondary Address
0	0	0x0F
0	1	0x0E
1	0	0x0D
1	1	0x0C

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2.2.5 J7—JTAG Boundary Scan

Connector J7 provides a direct connection for an AMD JTAG programming cable. J7 is used when customers want to load firmware configuration files into the FPGA (DLPC964 Controller). The JTAG Boundary connector J7 pins on the DLPLCRC964EVM pins are listed in Table 2-4.

Two matching fourteen position connector part numbers are:

- Molex part number: 051110-1451
- Digi-Key part number: WM18047-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 087396-8051
- Digi-Key part number: WM23602CT-ND

Note

For instructions on programming the DLPC964 Controller, see Section 3.1.5.2 for more details.

Table 2-4. JTAG Boundary Scan Connector Pins

Description	Pin	Supply Range
Ground	1	0V
Supply Voltage	2	1.8V
Ground	3	0V
TMS	4	1.8V
Ground	5	0V
TCK	6	1.8V
Ground	7	0V
TDO	8	1.8V
Ground	9	0V
TDI	10	1.8V
Ground	11	0V
NC	12	N/A
Ground	13	0V
NC	14	N/A

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2.2.6 J9—Micro-B USB Connector

Connector J9 is used to connect the USB cable from users PC running the DLPC964 GUI. The Micro-B USB connector J9 pins are shown in Table 2-5.

Note

The USB Micro-B to USB type A cable is not included inside the DLPLCRC964EVM kit and needs to be purchased separately.

Table 2-5. Micro-B USB Receptacle Connector Pins

Description	Pin	Supply Range
VBUS	1	5.0V
DMINUS	2	5.0V
DPLUS	3	5.0V
NC	4	0V
Ground	5	0V
Ground	6	0V
Ground	7	0V
Ground	8	0V
Ground	9	0V

2.2.7 J10—I^2C Connector

The connector J10 is used for 3.3V external I^2C operations. The I^2C connector J10 pins are shown in Table 2-6.

Two matching four-pin, 1.25mm connector part numbers are:

- Molex part number: 0510210400
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 0500798100
- Digi-Key part number: 0500798100

Table 2-6. I^2C Connector Pins

Description	Pin	Supply Range
I^2C SCL	1	3.3V
I^2C SDA	2	3.3V
3.3V supply	3	3.3V
Ground	4	0V
Ground	5	0V
Ground	6	0V

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2.2.8 J11—3.3V GPIO Connector

The pins for J11 are available for customers definition. The 3.3V GPIO connector J11 pins are shown in Table 2-7.

Table 2-7. 3.3V GPIO Connector Pins

Description	Pin	Supply Range
GPIO_3P3_0	1	3.3V
Ground	2	0V
GPIO_3P3_1	3	3.3V
Ground	4	0V
GPIO_3P3_2	5	3.3V
Ground	6	0V
GPIO_3P3_3	7	3.3V
Ground	8	0V
GPIO_3P3_4	9	3.3V
Ground	10	0V
GPIO_3P3_5	11	3.3V
Ground	12	0V
GPIO_3P3_6	13	3.3V
Ground	14	0V
GPIO_3P3_7	15	3.3V
Ground	16	0V
3.3V Supply	17	3.3V
Ground	18	0V
3.3V Supply	19	3.3V
Ground	20	0V

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2.2.9 J12—1.8V GPIO Connector

The pins for J12 are available for customers definition. The 1.8V GPIO connector J12 pins are shown in Table 2-8.

Table 2-8. 1.8V GPIO Connector Pins

Description	Pin	Supply Range
GPIO_1P8_0	1	1.8V
Ground	2	0V
GPIO_1P8_1	3	1.8V
Ground	4	0V
GPIO_1P8_2	5	1.8V
Ground	6	0V
GPIO_1P8_3	7	1.8V
Ground	8	0V
GPIO_1P8_4	9	1.8V
Ground	10	0V
GPIO_1P8_5	11	1.8V
Ground	12	0V
GPIO_1P8_6	13	1.8V
Ground	14	0V
GPIO_1P8_7	15	1.8V
Ground	16	0V
1.8V Supply	17	1.8V
Ground	18	0V
1.8V Supply	19	1.8V
Ground	20	0V

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2.2.10 J13, J14, J15, J16—DMD EVM Board Flex Cable Connectors

Connectors J13, J14, J15, and J16 are used to connect the DLPLCRC964EVM to the DLPLCR99EVM or DLPLCR99UVEVM. All four Flex Cables must be connected so there can be a proper data interface to the DMD board and DMD.

Two matching fifty-one position connector part numbers are:

- JAE Electronics part number: FI-RE51HL
- Digi-Key part number: 670-1205-ND

The corresponding terminal (crimp) part numbers are:

- JAE Electronics part number: FI-RC3-1A-1E-15000
- Digi-Key part number: 670-1195-1-ND

2.2.11 J17—DMD_DMux Connector

The DMD_DMux connector J17 is connected to the DMUX_LATCHED signal on the DLP991U DMD EVM board. The J17 connector pins are shown in Table 2-9.

Two matching two-pin, 2.5mm connector part numbers are:

- JST Sales America Inc. part number: EHR-2
- Digi-Key part number: 455-1000-ND

The corresponding terminal (crimp) part numbers are:

- JST Sales America Inc. part number: SEH-001T-P0.6
- Digi-Key part number: 455-1042-1-ND

Table 2-9. DMD_DMUX Connector Pins

Description	Pin	Supply Range
DMD_DMUX	1	3.3V
Ground	2	0V

2.2.12 J18—FanSink Connector

Connector J18 is a 3-pin +12 VDC fan connector used to control the temperature of the DLPC964 controller from overheating. The FanSink connector J18 pins on the DLPLCRC964EVM are listed in Table 2-10.

Two matching three-pin, 2.54mm connector part numbers are:

- Molex part number: 0022013037
- Digi-Key part number: 900-0022013037-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 0008650804
- Digi-Key part number: WM2756CT-ND

Note

Before powering on the DLPLCRC964EVM, make sure J18 is connected to the FanSink to prevent damaging the DLPC964 Controller.

Table 2-10. Fan Connector Pins

Description	Pin	Supply Range
Ground	1	0V
Power	2	12V
Power	3	NC

2.2.13 Switches

This section describes the switches on the DLPLCRC964EVM with the respective locations.

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2.2.13.1 SW1—DMD Park (PARK_Z)

SW1 is a toggle switch that issues a park command to the DMD that stops the DLPC964 logic. When ON, SW1 forces the DMD micromirrors to the parked state.

Note

TI highly recommends switching SW1 ON prior to removing power through J3 to prevent damage to the EVM board. Please see Section 2.4.2 for more information.

Table 2-11. SW1 ON/OFF State

SW1 State	Description
ON (facing toward DLPC964 controller)	Sets PARK_Z low and unparks the attached DMD
OFF (facing away from DLPC964 controller)	Sets PARK_Z high and issues a park on the DMD micromirrors

2.2.13.2 SW2—DLPC964 Reset

SW2 is a contact switch that resets the DLPC964 controller code running on the DLPLCRC964EVM. When SW2 is released, the DLPC964 controller boots from reset.

2.2.14 DLP LightCrafter DLPC964 LEDs

This section describes the power and status LEDs of the DLPLCRC964EVM.

2.2.14.1 DLPLCRC964EVM Power and Status LEDs

Figure 2-2 depicts the DLPLCRC964EVM LEDs with the respective locations.

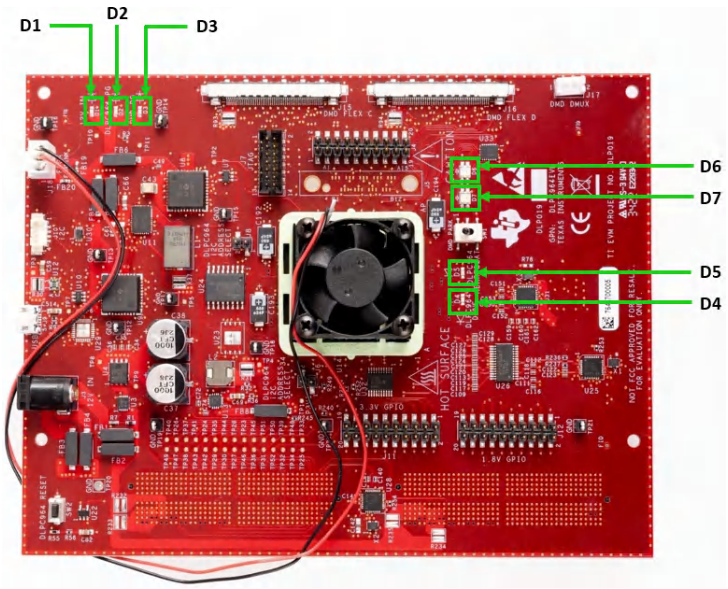


Figure 2-2. DLPLCRC964EVM LEDs (Top View)

Table 2-12. DLP LightCrafter DLPC964 EVM LED Reference

Connector Reference	EVM Function	Description or Use
D1	12V Power	External +12 VDC present.
D2	DLPC964 Power Good (PG)	All voltages are stable and present from the controller board.
D3	DMD Power Good (PG)	All voltages are stable and present from the DMD board.
D4	DLPC964 Done	DLPC964 initialization is complete.
D5	DLPC964 Heartbeat (Flashing)	Flashes when the DLPC964 is running.
D6	Phased-Locked Loop (PLL)	The indicator that the phase-locked loop (PLL) clock circuity of the controller is locked.
D7	DMD HSSI sync error	The indicator on whether a DMD HSSI sync error is detected.

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2.3 EVM Assembly

This section describes how to assemble the EVM hardware.

2.3.1 DLPLCRC964EVM and DMD EVM Assembly

This section explains how to assemble the standalone DLPLCRC964EVM and DLPLCR99EVM and DLPLCR99UVEVM.

The DLPLCRC964EVM requires a DLPLCR99EVM or DLPLCR99UVEVM and four flex cables for assembling standalone system.

- The flex cable connectors are labeled J13, J14, J15, and J16, which can be seen in Figure 2-1.
- The flex cable connectors are going to be connected between the EVM boards.
- The ends of each flex cable are identical.
- Either end can be connected to the connector ports J13, J14, J15, and J16 of the DLPLCRC964EVM. The other end of the flex cable is going to be connected to the DLPLCR99EVM or DLPLCR99UVEVM.

The flex cables that come with the DLPLCR99EVM and DLPLCR99UVEVM kit have a length of 16 inches. If desired, then there are shorter flex cables offered by JAE Electronics. Please see the other two flex cable connector options below:

- JF08R0R051030UA : 12-inch cable length
- JF08R0R051020UA: 8-inch cable length

Figure 2-3 depicts how to successfully connect the flex cables between the DLPLCRC964EVM and DLPLCR99EVM and DLPLCR99UVEVM.



Figure 2-3. Standalone DLPLCRC964EVM and DLPLCR99EVM / DLPLCR99UVEVM

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2.3.2 Connecting an Apps FPGA Board to the DLPLCRC964EVM

This section explains how to assemble the Apps FPGA front end to the DLPLCRC964EVM and DLPLCR99EVM and DLPLCR99UVEVM.

If desired, customers can connect a front-end board (AMD EVM) to the DLPLCRC964EVM board to send fast test patterns to the DLPC964 controller.

Locate the AMD EVM socket HPC FMC connectors and the DLPLCRC964EVM HPC FMC connectors (J1 and J2). Please line up both HPC FMC connectors and verify that the connectors are lined up correctly before applying pressure to connect the boards together as shown in Figure 2-6.

Note

After initially applying pressure to connect both boards, apply pressure at one end and then the other to verify the connectors are fully connected together.

The 300mm Samtec® HPC FMC ribbon cables (HDR-169468-01) are an alternative for these connections. Two cables are needed.

- Attach the HPC FMC socket connector end of the cables to the plug HPC FMC connectors on the DLPLCRC964EVM board.
- Attach the HPC FMC plug connector end of the cables to the socket HPC FMC connectors on the Apps FPGA board.

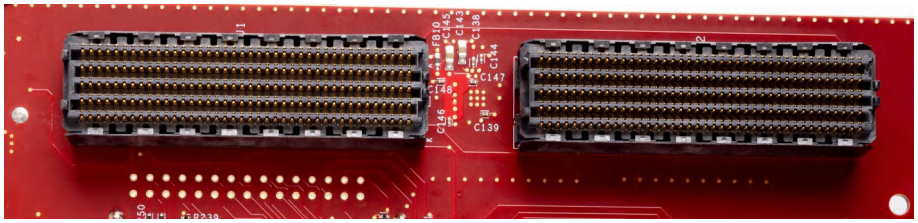


Figure 2-4. DLPLCRC964EVM Socket HPC FMC Connector

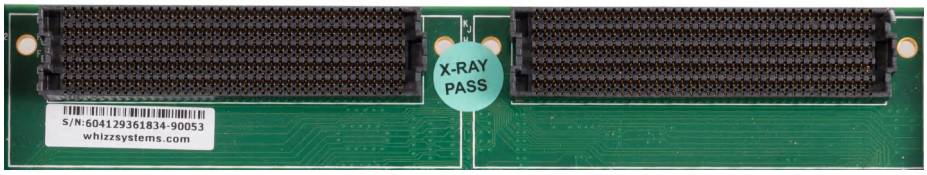


Figure 2-5. AMD EVM Socket HPC FMC Connector



Figure 2-6. Fully Assembled DLPLCRC964EVM with AMD EVM

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2.4 Quick Start

This chapter explains how to properly power up and power down the DLPLCRC964EVM.

2.4.1 Powering Up the DLPLCRC964EVM

The DLPLCRC964EVM is ready to use after assembling with a supported DMD EVM and a front-end board such as the AMD ZCU102 EVM. The following steps show how to power, display an image, and connect the EVM to a PC.

Before powering up the DLPLCRC964EVM and AMD EVM board, follow the instructions on programming the configuration PROM for either the standalone system or the AMD EVM and standalone system.

- Programming the DLPC964 Controller
- Programming the Apps FPGA (AMD EVM)

Power-Up Instructions:

1. Verify that switch SW1 is OFF and facing away from the DLPC964 Controller [DMD in parked state].
2. Power on the AMD EVM.

Note

Allow sufficient time for the AMD EVM board to configure (DS1 and DS10 illuminates, indicating successful power-up on the Apps FPGA).

3. Connect a 12V, 5A DC power supply to the barrel jack connector J3 shown in Figure 1-3.
4. Flip SW1 ON to face toward the DLPC964 Controller (DMD in unparked state).
5. 12V power (D1), DLPC964 Power Good (D2), and DMD Power Good (D3) LEDs illuminate indicating that power is present on the DLPLCRC964EVM and DLPLCR99EVM / DLPLCR99UVEVM boards.
6. DLPC964 Done (D4) illuminates indicating that the DLPC964 has completed initialization.
7. Phased-Locked Loop (D6) & DMD HSSI sync error (D7) illuminate indicating that there are no DMD HSSI sync errors and that the DLPC964 PLL is locked.
8. DLPC964 heartbeat (D5) flashes on and off indicating that the DLPLCRC964EVM is running.

Note

The DLPLCR99EVM and DLPLCR99UVEVM DMD board or a properly configured AMD EVM board must be present for the DLPC964 to initialize.

9. Connect a USB cable from a PC to connector J9 on the DLPLCRC964EVM, as seen in Figure 1-3. The first time the cable is connected on a PC, the DLPLCRC964EVM enumerates. The required drivers are installed as part of the DLPLCRC964EVM GUI installation.
10. Open and run the DLP LightCrafter DLPC964 GUI. When the GUI application opens, look at the bottom left. The GUI is going to display *Hardware Connected*.
11. The DLPLCRC964EVM can be controlled through the GUI software available for download from the DLPLCRC964EVM Tools Folder.

2.4.2 Powering Down the DLPLCRC964EVM

Follow steps 1 through 3 to properly power down the DLPLCRC964EVM:

1. Flip switch SW1 so the switch is facing away from the DLPC964 Controller [DMD in the parked state]
2. Remove power from the barrel jack connector J3 of the DLPLCRC964EVM
3. Power off the AMD EVM (if connected)

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3 Software

This chapter introduces the Windows DLPC964 GUI software used to control the DLPLCRC964EVM.

3.1 Operating the DLPLCRC964EVM

3.1.1 DLPLCRC964EVM GUI and Apps FPGA Software

The DLPLCRC964EVM-SW includes a DLPC964 GUI application to control the DLPC964 Controller, Apps FPGA, GUI source code, and Apps FPGA VHDL source code.

For details on the Apps FPGA VHDL source code, please see DLPC964 Apps FPGA User's Guide.

3.1.2 PC Software

Upon execution of the DLPC964 GUI application, the panel shown in Figure 3-1 is displayed. The GUI interface contains the following:

- Menu Bar (top)
- Main window with five sub-windows
- Hardware Connected—information bar (bottom)
- Log window (bottom)
- Online Resources

The five sub-windows are:

- Start Page
- DLPC964 Tab
- DLPC964 Registers Tab
- Apps FPGA Tab
- Apps FPGA Registers Tab

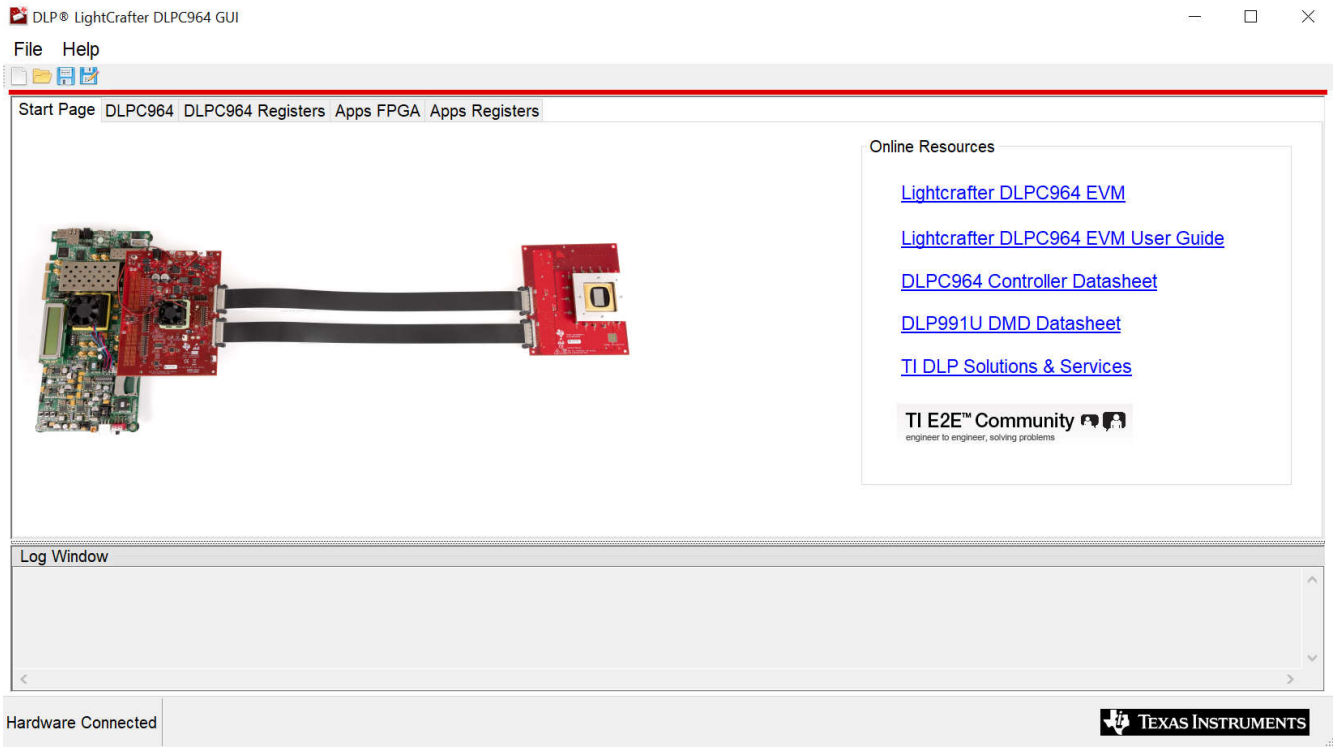


Figure 3-1. DLPC964 GUI

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3.1.3 Menu Bar

The DLPC964 GUI Menu bar consists of two items:

1. File Menu
   - *New Log* empties the Status sub-window to record a new command log sequence.
   - *Open Log* opens a dialog box to select an existing command log sequence file from the disk.
   - *Save Log* saves the current contents of the Status sub-window to the current script file. If the file is not yet saved the save as dialog opens.
   - *Save Log As* opens a dialog box to save the current command log sequence with a new name.

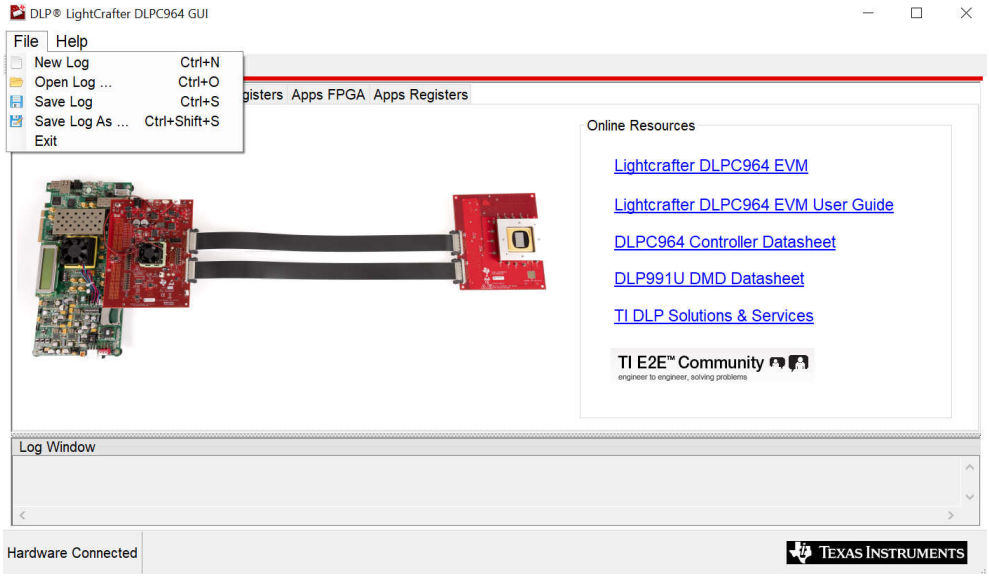


Figure 3-2. Menu Log Items

2. Help Menu
   - About DLP® LightCrafter DLPC964 GUI displays the Software Version (X.X.X) and USB DLL Version information box:

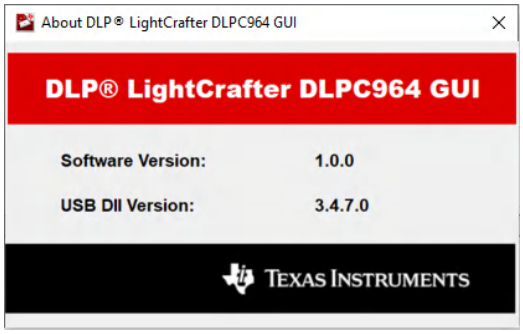


Figure 3-3. DLPC964 GUI About Box

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3.1.4 Main Window

The main window consists of five sub-windows.

3.1.4.1 Start Page

The Start Page is the first window that users see upon executing the DLPC964 GUI.

This window has the image of a standard setup for the Apps FPGA (AMD EVM) with DLPLCRC964EVM and DLPLCR99EVM and DLPLCR99UVEVM.

There are also online resources to help enable customers to get evaluation module kits started.

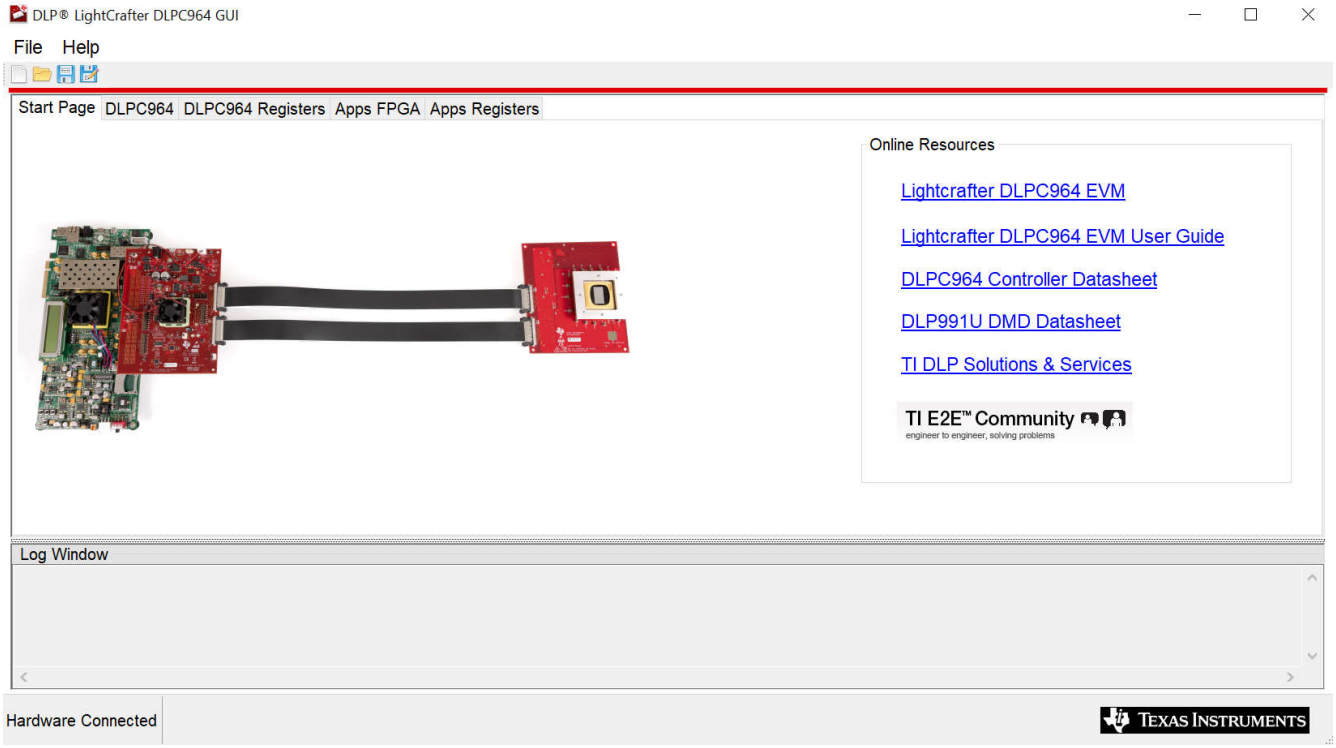


Figure 3-4. DLPC964 GUI Start Window

If the DLPC964 GUI states that Hardware is not connected, then check:

- The USB connection on J9 and/or the USB connection through the user's PC.
- The DLPC964 driver in Device Manager with the .inf file provided from the GUI software installation.

Note

The .inf file is located under: C:\Program Files\Texas Instruments\DLPC964REF-SW-VX.X.XX\Driver\Win10\x64.

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3.1.4.2 DLPC964 Tab

The *DLPC964 tab* read the status of the DLPC964 features and functions. HSSI, HSS, PLL, select test patterns and configure test pattern settings.

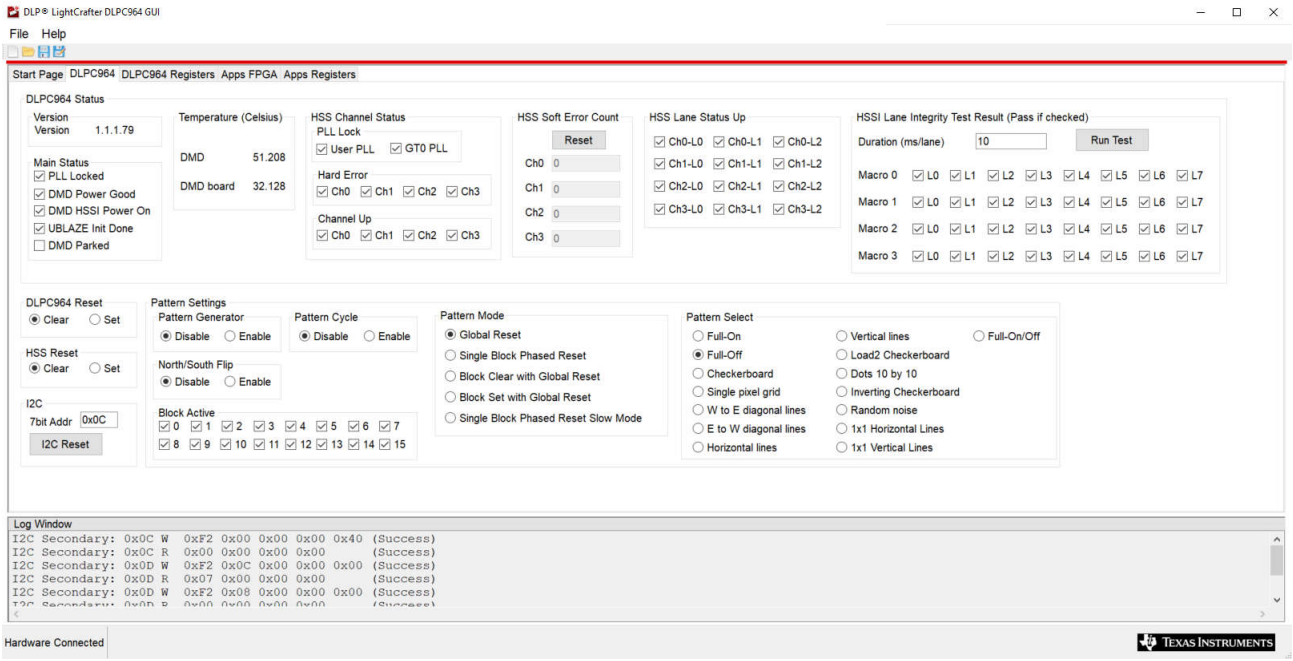


Figure 3-5. DLPC964 Tab

3.1.4.2.1 DLPC964 Status

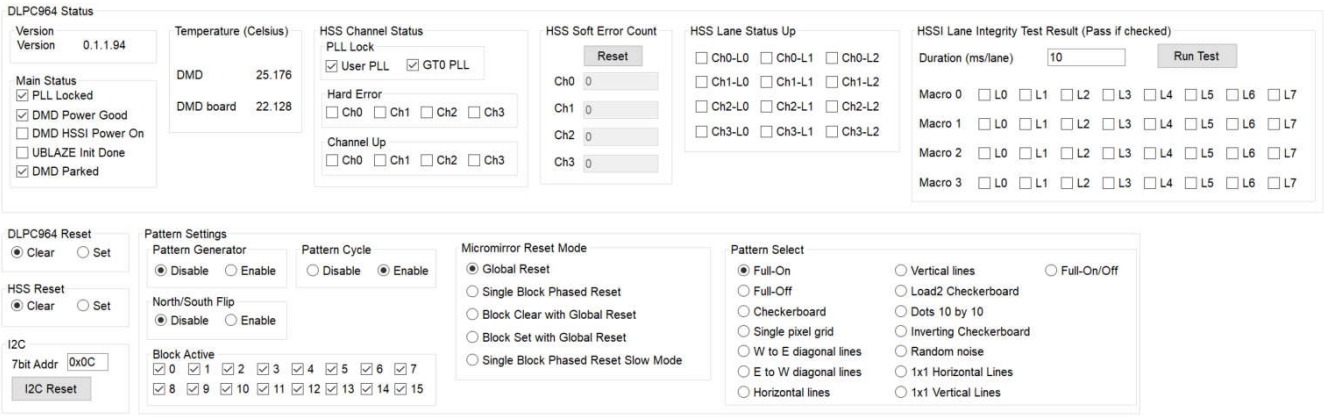


Figure 3-6. DLPC964 Status

- DLPC964 Version: contains the build number and version information for the DLPC964 Firmware.
- DLPC964 Temperature: displays the temperature of the DMD in Celsius
  - DMD: DMD internal temperature
  - DMD Board: surface temperature of physical DMD board
- Main Status: contains the status of the DLPC964 PLL Lock, DMD POWERGOOD, DMD High-Speed Interface, UBLAZE, and DMD Parked.
- HSS Channel Status: indicates the status of the Aurora 64B/66B inputs to the DLPC964 Controller.
  - PLL Lock
    - User PLL: when unchecked, the user clock is not lock. When checked, user clock is locked.
    - GT0 PLL: the source for the MMCM to generate the user clock and determines if the PLL is lock.
  - Hard Error: indicates if the HSS requires a reset to recover from a hard error condition.
  - Channel Up: determines if the Aurora Channels 0-3 are up and running.

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- HSS Soft Error Count: contains the Aurora 64B/66B Channel 0-3 total soft error count.
- HSS Lane Status Up: indicates the status of each individual lane of the Aurora 64B/66B input to the DLPC964 Controller.
- HSSI Lane Integrity Test Results: the Lane Integrity Test contains the testing results of DMD High Speed Serial Interface for Channels 0-3. Each lane for this interface (7:0) can be checked for passing results.

Note

If the Channels are not passing, this results in a DMD Interface D-Sync Error.

3.1.4.2.2 DLPC964 Reset



Figure 3-7. DLPC964 Reset

The *DLPC964 Reset* command causes the mirrors to change from the current state to the state of that in memory. The contents of memory are determined by the pattern that is currently selected from Pattern Select. You can choose to reset all the blocks (*Global*), or you can choose to reset blocks individually using single block mode.

3.1.4.2.3 HSS Reset



Figure 3-8. HSS Reset

The *HSS Reset* command causes the HSS input and output buses to reset the data going to the DLPC964.

3.1.4.2.4 I^2C 7-Bit Addr

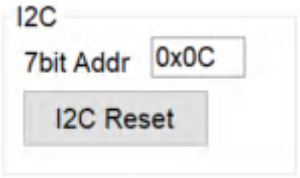


Figure 3-9. DLPC641 I^2C 7-Bit Addr

This allows for an alternate I^2C address to be reset.

Note

When J6 and J8 are left unconnected, the default I^2C address is 0x0C. To communicate with the alternate I2C addresses, please see Table 2-3 for information regarding the jumpers that must be populated.

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3.1.4.2.5 Pattern Settings

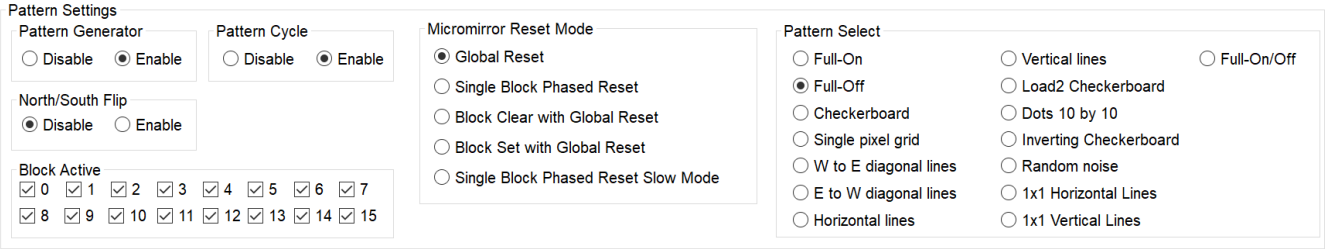


Figure 3-10. DLPC964 Pattern Settings

- Pattern Generator: when enabled, patterns are displayed on the DMD. When disabled, no patterns are going to be displayed on DMD.
- Pattern Cycle: when enabled, the DMD cycles through the first eight predefined patterns, each being displayed every two seconds. When disabled, a single selected pattern is sent to the DMD.
- North/South Flip: having this enabled flips the image being displayed on the DMD vertically.
- Pattern Select
  - Full-On: full white background where all mirrors on the DMD are going to be in the on position.
  - Full-Off: full black background where all mirrors on the DMD are going to be in the off position.
  - Checkerboard: black and white checkerboard (64 pixels × 64 pixels).
  - Single pixel grid: the border is on to help visualize the extent of the DMD array.
  - W to E diagonal lines: used to check for row data issues.
  - E to W diagonal lines: used to check for row data issues.
  - Horizontal lines: used to check for issues with row loads.
  - Vertical lines: used to check for issues with data bus lines.
  - Load2 Checkboard: a black and white checkerboard pattern (32 pixels × 32 pixels).
  - Dots 10 by 10: single white pixels are spaced 10 pixels evenly in the X and Y directions.
  - Inverting Checkerboard: inverted version of the checkerboard pattern.
  - Random Noise: randomized noise pattern for customer tilt angle testing.
  - 1x1 Horizontal lines (every row alternating black/white): used to check for issues with row loads.
  - 1x1 Vertical lines (every column alternating black/white): used to check for issues with data bus lines.
  - Full-On/Off: toggles between the Full-On and Full-Off pattern.
- Micromirror Reset Mode
  - Global Reset: in global reset mode, all enabled blocks are going to be loaded with data sequentially. Once all blocks have been loaded, the MCP_Start signal resets all the blocks at the same time.
  - Single Block Phased Reset: in single reset mode, a single block is loaded at a time and once the DLPC964 has loaded the DMD with the data sent, the MCP_Start signal resets that single block.
  - Block Clear with Global Reset: this mode shows how the Clear block load type is used in the DLPC964 system. A clear load type does not require any data since the block puts all of the mirrors in the off state (0). Since the clear load type does not have any data to be sent after, the command valid signal is not needed so only the DMD load signal is sent. The MCP_Start signal follows the same pattern as Global Mode.
  - Block Set with Global Reset: this mode shows how the Set block load type is used in the DLPC964 system. A set load type does the opposite of the clear load type and also does not require any data. The set load type sets all the mirrors in the on state (1). Just like the clear load type, there is no need for the command valid signal, only the DMD load signal. The MCP_Start signal follows the same pattern as Global Mode.
  - Single Block Phased Reset Slow Mode: slow mode (or disabling the fast mode) causes the DLPC964 to receive data across a single channel only (4x 10Gbps lanes compared to 12x). To do this, each segment of a block must be sent sequentially across 1 Aurora 64B/66B channel instead of parallel. The segments must be sent in the following order: D (0x3) C (0x2) B (0x1) A (0x0). Once all four segments are sent, the MCP_Start signal can be issued. The MCP_Start signal behaves the same as in Single Mode.
- Block Active: there are 16 blocks [0-15] in the DLP991U DMD. The blocks that are checked inside the GUI are going to determine what blocks are going to be reset and loaded with new data from the DMD.

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3.1.4.3 DLPC964 Registers Tab

The DLPC964 Registers tab uses the I^{2}C Interface to communicate with the DLPC964 controller registers. This tab shows the DLPC964 controller register list and settings for each register which use Get/Set buttons to read/write to specific registers.

Note

Access to the DLPC964 registers must not begin until INIT_DONE has transitioned high (logic 1).

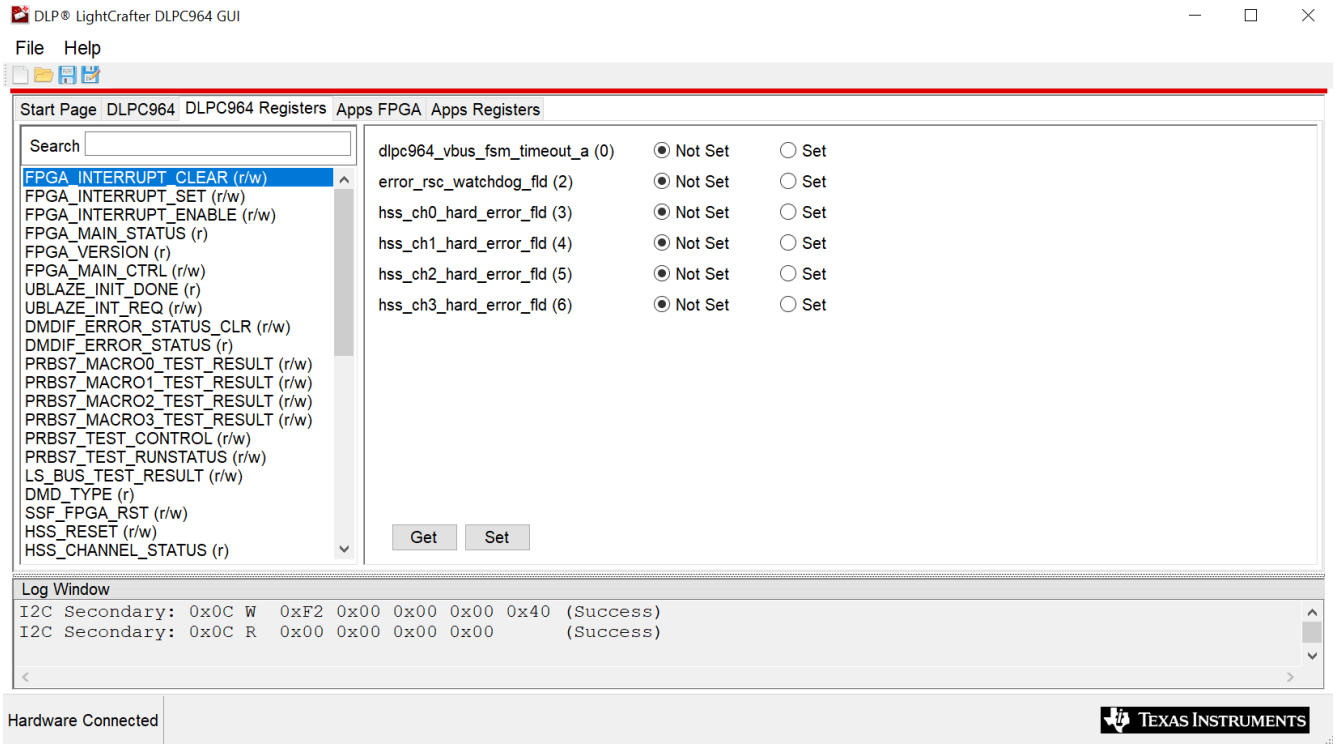


Figure 3-11. DLPC964 Register List

Register Definitions

The following designations are used throughout this section of the document:

- R—designates read-only
- W—designates write-only
- R/W—designates read and write
- S—designates status of register
- I—designates interrupt only
- P—designates pulse only

Please visit the DLPC964 datasheet for detailed descriptions of each DLPC964 register offered in the DLPC964 GUI.

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3.1.4.4 Apps FPGA Tab

The *Apps FPGA tab* reads the status of Apps FPGA features and functions, select test patterns and configure pattern settings.

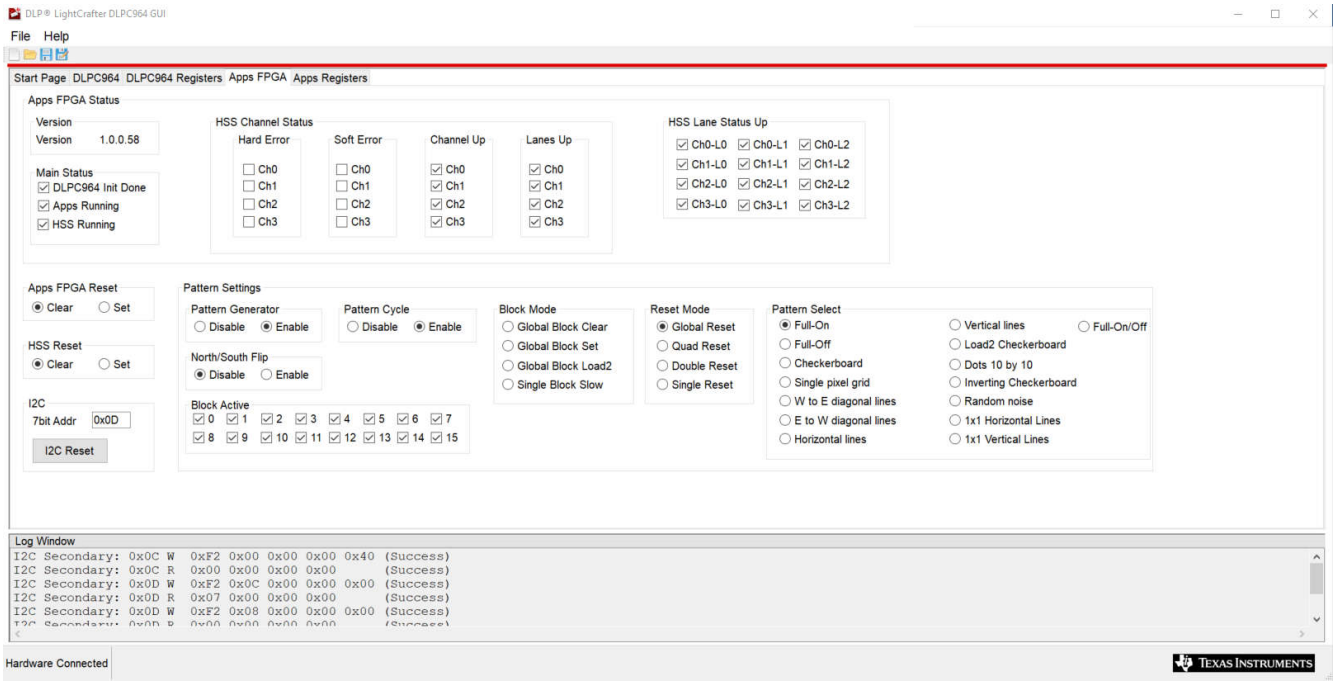


Figure 3-12. Apps FPGA Tab

3.1.4.4.1 Apps FPGA Status

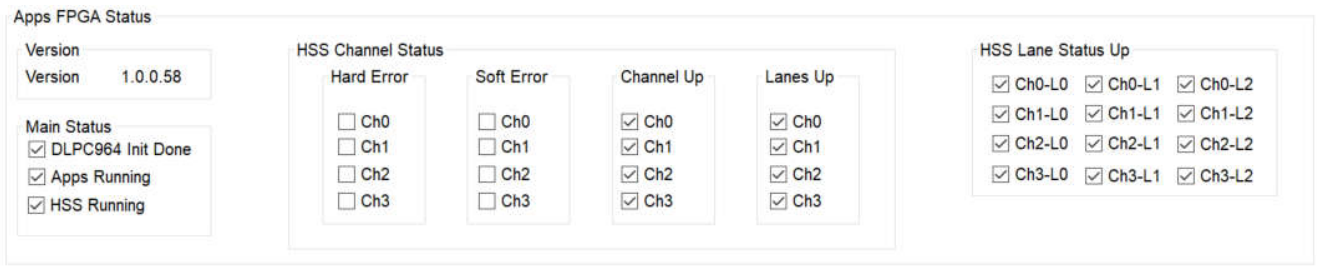


Figure 3-13. Apps FPGA Status

- Apps FPGA Version: contains the build number and version information for the Apps FPGA Firmware.
- Main Status: this contains the status for the DLPC964, Apps FPGA, and HSS status determining if each one is up and running.
- HSS Channel Status: HSS Channel Status indicates the status of the Aurora 64B/66B inputs to the DLPC964 Controller.
  - Hard Error: input Aurora Channel 0-3 hard error and indicate failure in the GTH.
  - Soft Error: the HSS Soft Error Count indicates corrupted data received on each individual channel.
  - Channel Up: determines if the HSS Aurora Channels 0-3 are initialized.
  - Lanes Up: determines if the HSS Aurora Lane Channels 0-3 are initialized.
- HSS Lane Status Up: the HSS Lane Status Up indicates the status of each individual lane of the Aurora 64B/66B input to the DLPC964 Controller.

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3.1.4.4.2 Apps FPGA Reset

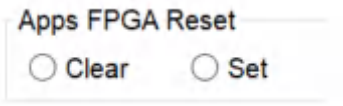


Figure 3-14. Apps FPGA Reset

The *Apps FPGA Reset* command causes the mirrors to change from the current state to the state of that in memory. The contents of memory are determined by the pattern that is currently selected from Pattern Select. You can choose to reset all the blocks (*Global*), or you can choose to reset blocks individually using single block mode.

3.1.4.4.3 HSS Reset (Apps)

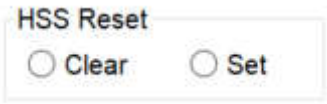


Figure 3-15. HSS Reset

The HSS Reset command causes the HSS input and output buses to reset the data of the Aurora 64B/66B interface.

3.1.4.4.4 Apps I²C 7-Bit Addr



Figure 3-16. DLPC964 I2C 7-Bit Addr

This allows for an alternate I²C address to be reset.

Note

When J6 and J8 are left unconnected, the default I²C address is 0x0D. To communicate with the alternate I2C addresses, please see Table 2-3 for information regarding the jumpers that must be populated.

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3.1.4.4.5 Pattern Settings (Apps)

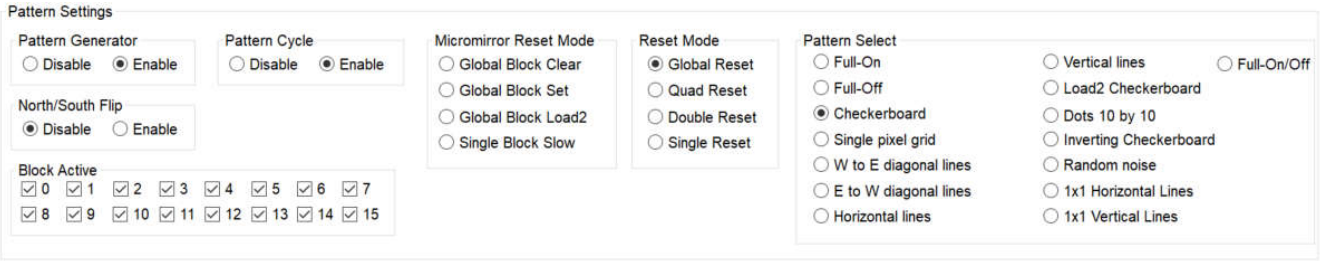


Figure 3-17. Apps FPGA Pattern Settings

- Pattern Generator: when enabled, patterns are displayed onto the DMD. When disabled, no patterns are going to be displayed on DMD.
- Pattern Cycle: when enabled, the DMD cycles through the first eight predefined patterns, each being displayed every two seconds. When disabled, a single selected pattern is sent to the DMD.
- North/South Flip: having this enabled flips the image being displayed on the DMD vertically.
- Pattern Select
  - Full-On: full white background where all mirrors on the DMD are going to be in the on position.
  - Full-Off: full black background where all mirrors on the DMD are going to be in the off position.
  - Checkerboard: black and white checkerboard (64 pixels × 64 pixels).
  - Single pixel grid: the border is on to help visualize the extent of the DMD array.
  - W to E diagonal lines: used to check for row data issues.
  - E to W diagonal lines: used to check for row data issues.
  - Horizontal lines: used to check for issues with row loads.
  - Vertical lines: used to check for issues with data bus lines.
  - Load2 Checkboard: a black and white checkerboard pattern (32 pixels × 32 pixels).
  - Dots 10 by 10: single white pixels are spaced 10 pixels evenly in the X and Y direction.
  - Inverting Checkerboard: inverted version of the checkerboard pattern.
  - Random Noise: randomized noise pattern for customer tilt angle testing.
  - 1x1 Horizontal lines (every row alternating black/white): used to check for issues with row loads.
  - 1x1 Vertical lines (every column alternating black/white): used to check for issues with data bus lines.
  - Full-On/Off: toggles between the Full-On and Full-Off pattern.
- Micromirror Reset Mode
  - Global Block Clear: this mode shows how the Clear block load type is used in the DLPC964 system. A clear load type does not require any data since the block puts all of the mirrors in the off state (0). Since the clear load type does not have any data to be sent, the command valid signal is not needed so only the DMD load signal is sent. The MCP_Start signal follows the same pattern as Global Mode.
  - Global Block Set: this mode shows how the Set block load type is used in the DLPC964 system. A set load type does the opposite of the clear load type and also does not require any data. The set load type sets all the mirrors in the on state (1). Just like the clear load type, there is no need for the command valid signal, only the DMD load signal. The MCP_Start signal follows the same pattern as Global Mode.
  - Global Block Load2: enabling the Load2 operation tells the DMD to load 1 line of data received into 2 rows of the DMD. The role of the DLPC964 Apps FPGA during a Load2 operation is to verify that 68 lines, at most, are sent over the Aurora HSSI channels. Asserting LOAD2 causes the DLPC964 controller and attached DMD to load 2 rows for every row of data sent, reducing the pattern load time to half of a full DMD load. This function does not reduce the MCP timing.
  - Single Block Slow: slow mode (or disabling the fast mode) causes the DLPC964 Apps FPGA to send data across a single Aurora 64B/66B channel only (4x 10Gbps lanes compared to 12x). To do this, each segment of a block must be sent sequentially across 1 channel instead of parallel. The segments must be sent in the following order: D (0x3) C (0x2) B (0x1) A (0x0). Once all four segments are sent, the MCP_Start signal can be issued. The MCP_Start signal behaves the same as in Single Mode.
- Block Active: there are 16 blocks [0-15] in the DLP991U DMD. The blocks that are checked inside the GUI are going to determine what blocks are going to be reset and loaded with new data to the DMD.

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3.1.4.5 Apps FPGA Registers Tab

The Apps FPGA Registers tab uses the I²C Interface to communicate with the Apps FPGA registers. This tab shows the Apps FPGA register list and settings for each register that use Get/Set buttons to read/write to specific registers.

Note

Access to the Apps FPGA registers must not begin until INIT_DONE has transitioned high (logic 1).

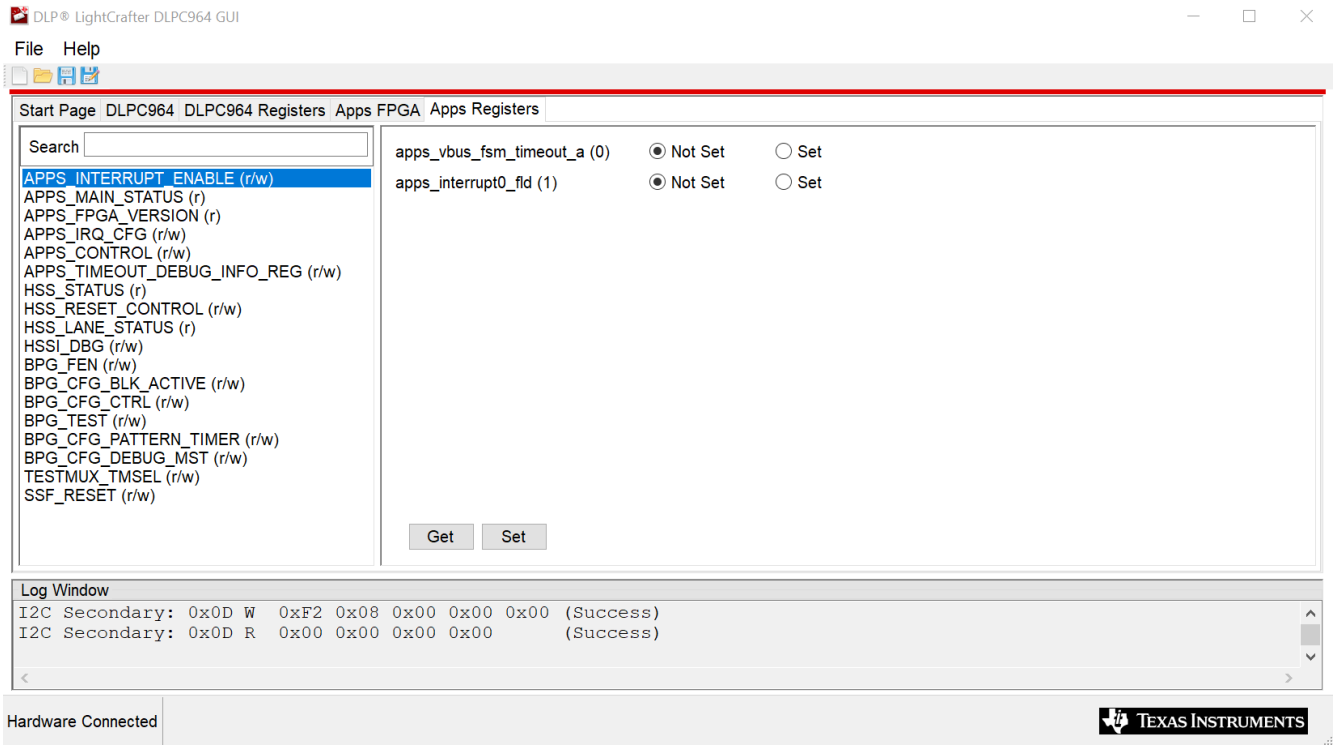


Figure 3-18. Apps FPGA Register List

Register Definitions

The following designations are used throughout this section of the document:

- R—designates read-only
- W—designates write-only
- R/W—designates read and write
- S—designates status of register
- I—designates interrupt only
- P—designates pulse only

Please visit the DLPC964 datasheet for detailed descriptions of each Apps FPGA register offered in the DLPC964 GUI.

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3.1.5 Programming Firmware

3.1.5.1 Connecting to the DLPC964 GUI

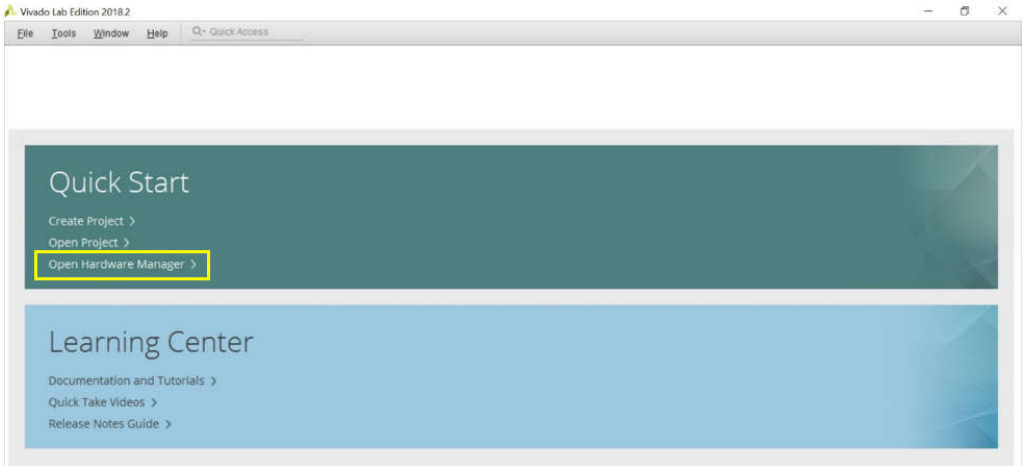
1. Connect the boards as shown in previous slides. There are two configurations:
   a. Apps FPGA with DLPC964 controller board and DLP991U DMD board.
   b. Standalone DLPC964 controller board with DLP991U DMD board.
2. Power DLPC964 controller board using 12V DC input.
3. Power on AMD EVM (if present).
4. Connect USB from DLPC964 controller board to PC.
5. Run TI DLP DLPC964 GUI.
6. GUI displays *Hardware Connected* message in bottom left corner of status bar.

3.1.5.2 Programming the DLPC964 Controller

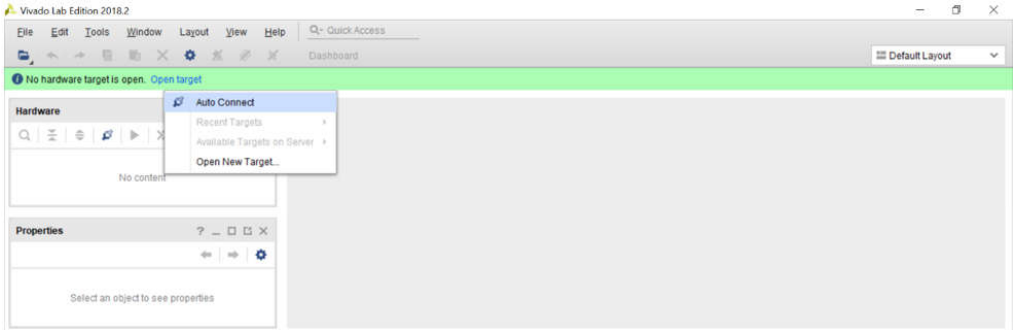
1. Launch the Vivado Lab Solutions 2024.2 application. Once the application opens, select *Open Hardware Manager* from the main window.

Note

Click the link above to download Vivado Lab Solutions 2024.2 Once the web page is loaded, find the archived 2024.2 folder and then navigate to the Vivado Lab Solutions 2024.2 downloadable link and download the installation.

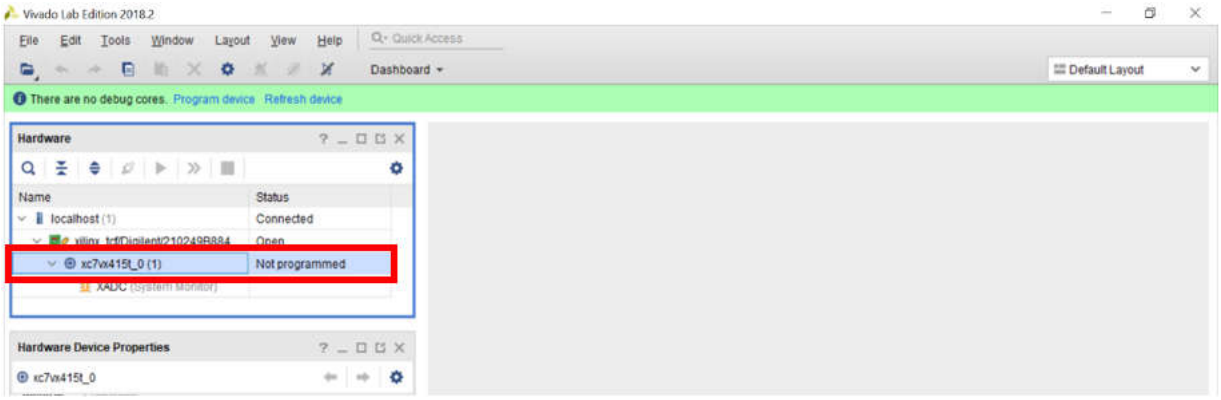


2. Once the Hardware Manager is open, check that the JTAG is connected to jumper J7 on the DLPLCRC964EVM board and that the port is connected to a PC. Once JTAG is properly connected, plug the 12V DC power supply into the barrel jack on the board and power on.
3. Once JTAG is properly connected and the board is powered on, the next step is selecting the target device that is going to be programmed.
4. In the *Hardware Manager* window, select *Open Target* > *Auto Connect* to find the target device being programmed.

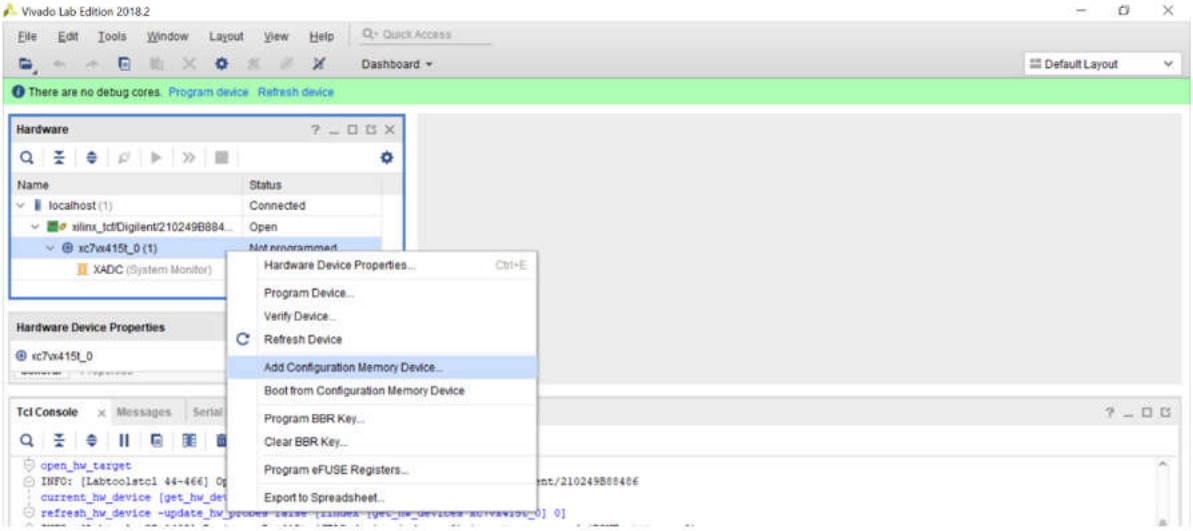


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5. Once the target device is detected, the target device is going to be displayed in the bottom left corner, showing current status of device.



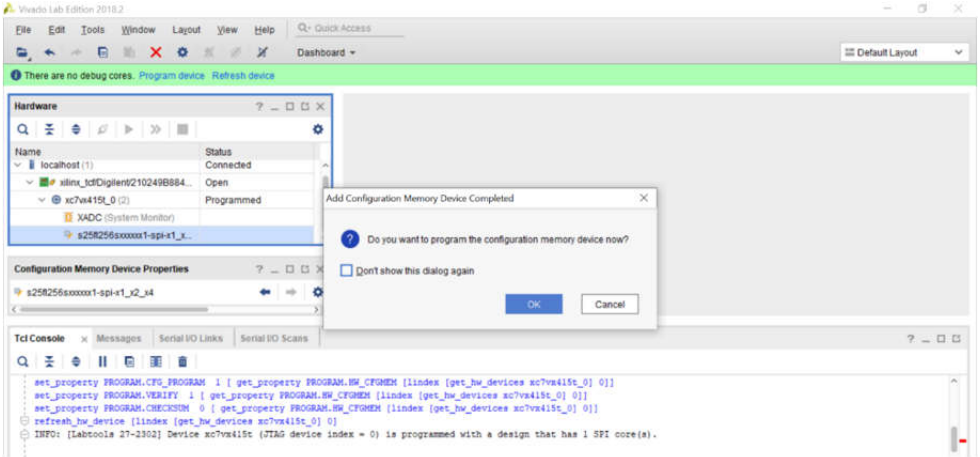
6. Right-click on the FPGA and select "*Add Configuration Memory Device*."



7. Select the correct flash device that is connected to the FPGA device on the DLPLCRC964EVM board. Input the parameters below to select the correct flash device.

Manufacturer = Spansion	Type = SPI
Density = 256Mb	Width = x1_x2_x4
Part Number = s25fl256sxxxxxx1	

8. Once the appropriate flash device is selected, a dialog box is going to pop up asking if the user wants to program the configuration device (SPI Flash). Click *OK*.



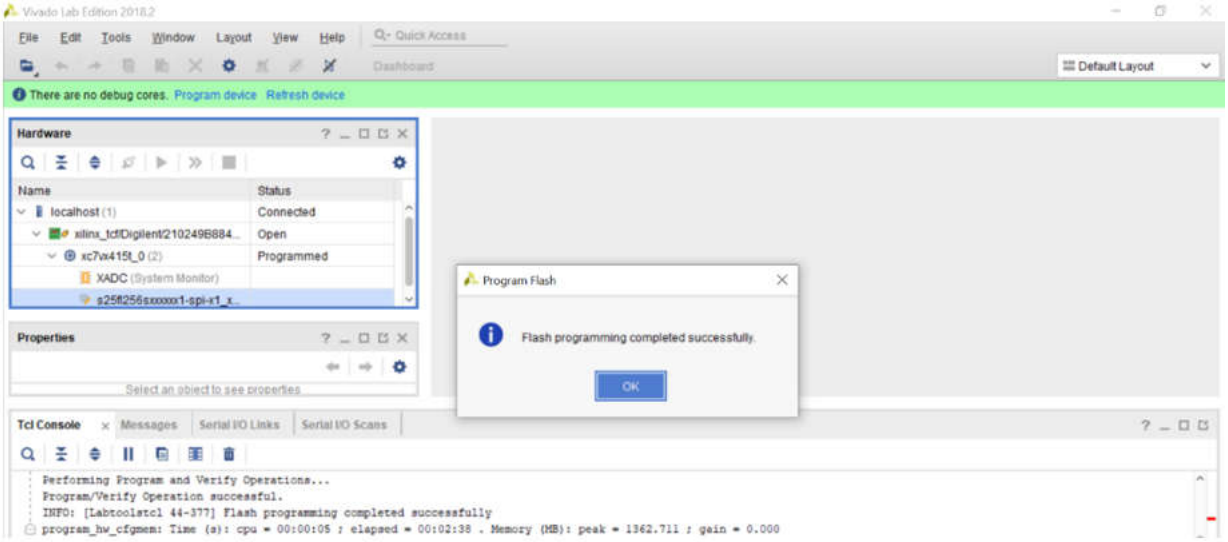
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9. Go to the Configuration file and select the appropriate `.mcs` file needed to program the flash device.

Note

The `.mcs` can be downloaded from the DLPLCRC964EVM Tool Page. Locate and download the DLPR964-FW package which includes the appropriate `.mcs` to program the DLPC964 Controller.

10. After clicking *OK*, the Vivado Hardware Manager programs the flash of the board and verifies that the flash was programmed successfully.



11. Complete a power cycle on the DLPLCRC964EVM board. Unplug power from the barrel jack connector J3 and then plug power back into the barrel jack connector. After the FPGA is programmed successfully, DLPC964 Done (D4) is going to illuminate green and the DLPC964 Heartbeat (D5) has a heartbeat that flashes on and off.

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3.1.5.3 Programming the Apps FPGA (AMD EVM)

3.1.5.3.1 Programming the Apps FPGA with Bitstream Loading

Follow the instructions below for loading the DLPC964 Apps binary onto the FPGA through a bitstream using Vivado Lab Solutions 2024.2:

Note

Click the link above to download Vivado Lab Solutions 2024.2. Once the web page is loaded, find the archived 2024.2 folder and then navigate to the Vivado Lab Solutions 2024.2 downloadable link and download the installation.

Note

The FPGA needs to be reloaded each time power is lost or disconnected from the AMD EVM.

1. Plug the Micro-B USB cable into the side of the ZCU102 and the other end into the computer running Vivado.
2. Start Vivado Lab Solutions 2024.2 on the computer.
3. Select *Open Hardware Manager* from the main window.
4. Click *open target* located in the top left of the hardware manager then *Auto Connect*.
   a. If the AMD EVM is the only FPGA plugged into the computer, then Vivado automatically connects to the AMD EVM.
5. Right-click on the FPGA and select *Program Device*.
6. Navigate to the appstop.mcs file and select *Program*.

3.1.5.3.2 Programming Apps FPGA by Flash

Follow the instructions below for loading the DLPC964 Apps binary onto the flash through a bitstream using Vivado Lab Solutions 2024.2:

Note

Click the link above to download Vivado Lab Solutions 2024.2. Once the web page is loaded, find the archived 2024.2 folder and then navigate to the Vivado Lab Solutions 2024.2 downloadable link and download the installation.

Note

The bitstream is always loaded onto the FPGA upon power-up of the AMD EVM.

1. Plug the micro USB into the side of the AMD EVM and the other end into the computer running Vivado.
2. Verify that boot mode is set to JTAG by setting SW6 to 0000 (Switches 4 →1, right to left, toward the ON arrow) corresponding to Mode Pins [3:0] = 0000.

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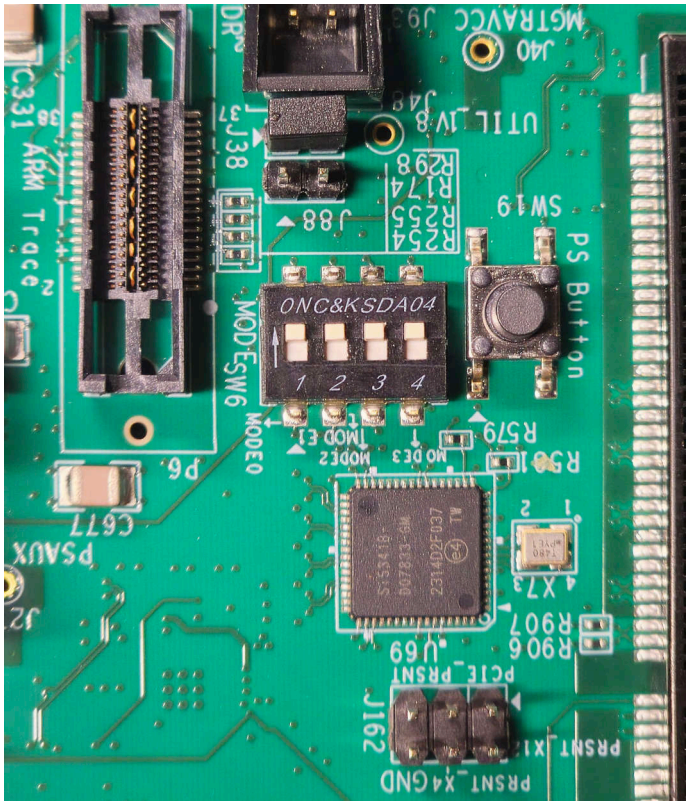


Figure 3-19. FPGA Configuration Mode 1 (JTAG)

3. Start Vivado Lab Studios 2024.2 on the computer.
4. Select *Open Hardware Manager* from the main window.
5. Click *open target* located in the top left of the hardware manager then *Auto Connect*.
   a. If the AMD EVM is the only FPGA plugged into the computer, then Vivado automatically connects to the AMD EVM. Otherwise, the process is slightly more involved.
6. Right-click on the FPGA and select *Add Configuration Memory Device*.
7. Find the Flash name mt25qu512-qspi-x8-dual_parallel and click *OK*.
8. Select *OK* again and select the configuration file (appstop.mcs).
   a. Make sure all other settings match.
9. Once setup is complete, click *OK*. The programming can take a few minutes.
10. After programming is complete, power off the FPGA.
11. Enter QSPI mode by setting SW6 to 0010 (Switches 4 →1, right to left, toward the ON arrow) corresponding to Mode Pins [3:0] = 0010.
12. Once completed, power cycle the AMD EVM, and the DLPC964 Apps Bitstream automatically loads onto the AMD EVM. This can be verified by the heartbeat led located on DS44.

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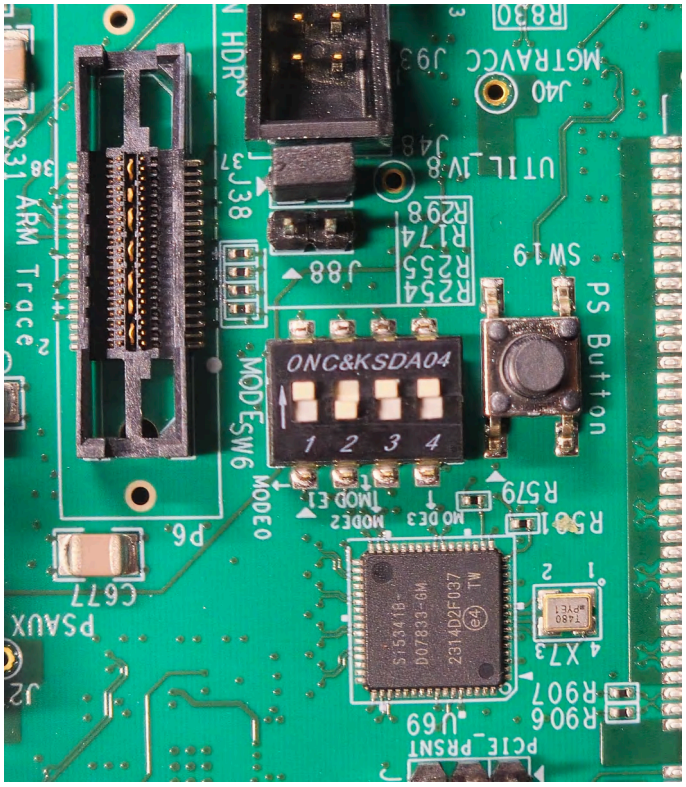


Figure 3-20. FPGA Configuration Mode 2 (QSPI)

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4 Hardware Design Files

4.1 Schematics

The schematics are available for download on the DLPLCRC964EVM Tool Folder.

4.2 PCB Layout

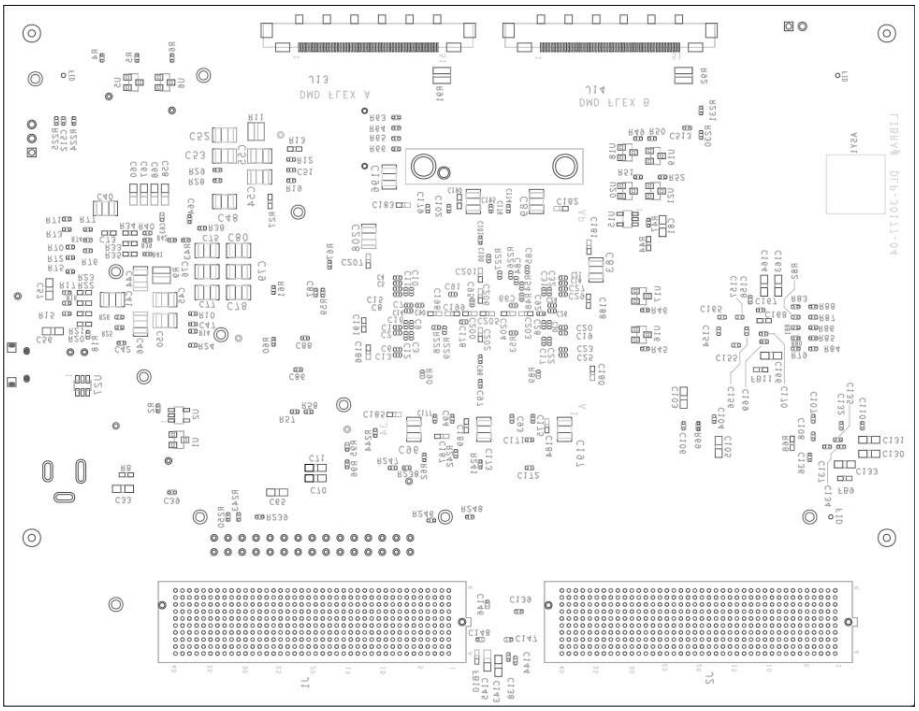


Figure 4-1. DLPLCRC964EVM PCB (Front)

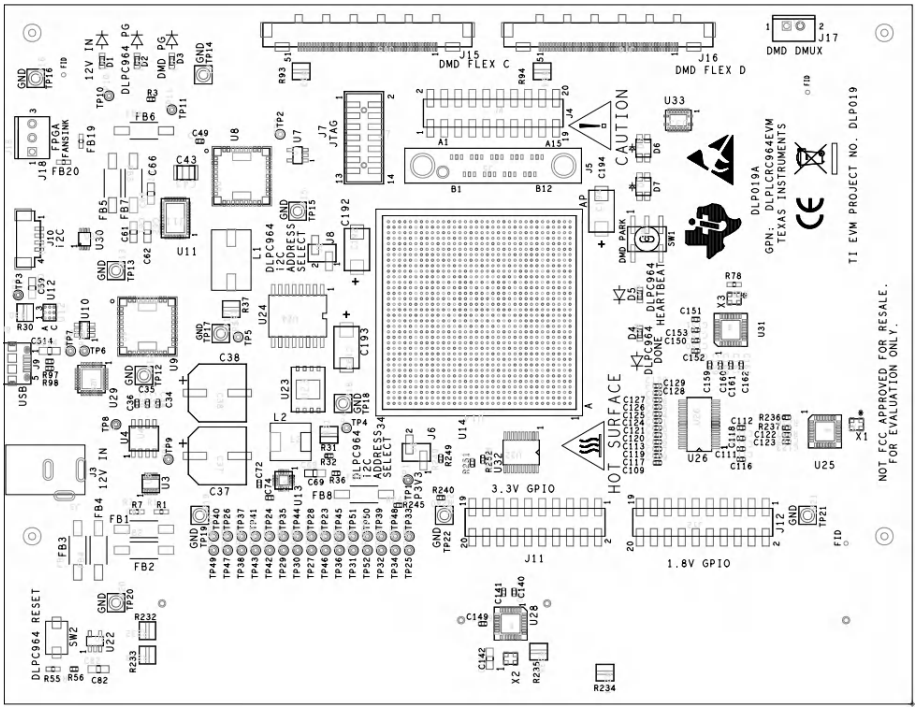


Figure 4-2. DLPLCRC964EVM PCB (Back)

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4.3 Bill of Materials (BOM)

Table 4-1 lists the Bill of Materials for the DLPLCRC964EVM.

Table 4-1. DLPLCRC964EVM Bill of Materials

Reference	Quantity	Part	MFG	MFG Part Number
C1,C2,C3,C4,C5,C6,C7,C8,C9,C10, C11,C12,C13,C14,C15,C16,C17,C18, C19,C20,C21,C22,C23,C24,C25,C26, C27,C28,C29,C30,C31,C32	32	0.1µ	American Technical Ceramics	530L104KT16T
C33	1	22µ	Samsung	CL21A226MOCLRNC
C34,C35,C36,C39,C42,C49,C64,C84, C85,C86,C87,C88,C90,C91,C92,C93, C94,C95,C97,C98,C99,C100,C101, C102,C104,C106,C107,C108,C109, C111,C112,C113,C116,C117,C118, C119,C120,C121,C122,C123,C124, C125,C126,C127,C128,C129,C132, C134,C135,C136,C139,C140,C141, C144,C146,C147,C148,C150,C151, C152,C153,C154,C155,C156,C157, C159,C160,C161,C162,C165,C167, C168,C169,C171,C172,C174,C175, C176,C177,C178,C179,C513	82	0.1µ	Samsung	CL05A104KA5NNNC
C37,C38	2	1000µ	Panasonic	EEE-FT1C102GP
C40,C45,C46,C48,C50,C52,C53, C54,C77,C78,C79,C80,C89,C96, C173,C196,C197	17	100µ	Cal-Chip Electronics	GMC32X5R107M16NT
C41,C43,C83,C195	4	47µ	KEMET	C1210C476M4PACTU
C44,C55	2	220µ	Murata	GRM32ER60J227ME05L
C47,C51	2	0.01µ	KEMET	C0402C103K5RACTU
C56,C57,C58,C69,C81,C82,C514	7	1µ	Yageo	CC0805KKX7R9BB105
C59,C60,C61,C62,C65, C66,C67,C68,C70,C71	10	22µ	Samsung	CL21A226MOCLRNC
C63	1	2200p	Yageo	AC0402KRX7R8BB222
C72,C110,C138,C158	4	0.01µ	KEMET	C0402C103K5RACTU
C73,C180,C181,C182,C183,C184, C185,C186,C187,C188,C189,C190, C191,C198,C199,C200,C201,C202, C203,C204,C205,C206,C207	23	4.7µ	Murata	GRM188R61E475KE11D
C74	1	3900p	Kyocera	KGM05AR71H392JH
C75,C76,C208	3	330u	Murata	GRM32ER60G337ME05L
C103,C105,C130,C131,C133,C142, C143,C145,C163,C164,C166	11	10µ	Samsung	CL21A106KAYNNNE
C137,C149,C170	3	0.047u	Murata	GRM155C71H473KE19D
C192,C193,C194	3	680µ	Panasonic	2R5TPF680M6L
C512	1	36p	Yageo	CC0402JRNPO9BN360
D1,D2,D3	3	LED_BLUE_SMT	Lite-On	LTST-C193TBKT-5A
D4,D5	2	LED_GREEN_SMT	Lite-On	LTST-C193KGKT-5A
D6,D7	2	DUAL_LED_GRN_RED_SMT	Lite-On	LTST-C155GEKT
FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8	8	FB	Laird	35F0121-1SR-10

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Table 4-1. DLPLCRC964EVM Bill of Materials (continued)

Reference	Quantity	Part	MFG	MFG Part Number
FB9,FB10,FB11,FB19,FB20	5	FB	Laird	HI0603P600R-10
J1,J2	2	FMC 400POS CONNECTOR	SAMTEC	SEAM-40-11.0-S-10-2-A-K-TR
J3	1	PJ-002AH	CUI	PJ-002AH
J4,J11,J12	3	TSM-110-01-L-DV-P	Samtec	TSM-110-01-L-DV-P
J6,J8	2	TSM-102-01-L-SV	Samtec	TSM-102-01-L-SV
J7	1	JTAG	Molex	878321420
J9	1	10118194-0001LF	Amphenol	10118194-0001LF
J10	1	53398-0471	Molex	533980471
J13,J14,J15,J16	4	FI-RE51S-HF-R1500	JAE	FI-RE51S-HF-R1500
J17	1	B2B-EH	JST	B2B-EH-A(LF)(SN)
J18	1	22-23-2031	Molex	22232031
L1	1	150n	Eaton	FP1107R2-R15-R
L2	1	1µH	TDK	SPM6530T-1R0M120
R1,R27	2	1 Meg	Vishay Dale	CRCW06031M00DHEAP
R2,R47,R56,R62,R67,R238,R239,R240, R241,R242,R243,R244,R245, R246,R247,R248,R249,R250	18	10k	Samsung	RC1005F103CS
R3,R15,R16,R17,R18,R57,R76,R77	8	2.2K	Panasonic	ERJ-2RKF2201X
R4,R5,R6	3	1.8K	Panasonic	ERJ-2GEJ185X
R7	1	150k	Panasonic	ERJ-3EKF1503V
R8	1	130K	Yageo	RC0603FR-07130KL
R9,R11,R30,R31,R37,R91,R92,R93,R94	9	10m	Rohm	LTR18EZPFU10L0
R10,R12,R38,R72,R73,R74,R81,R83, R84,R85,R87,R97,R98,R230, R231,R236,R237	17	0	Samsung	RC1005J000CS
R13,R21,R22,R23,R78	5	100K	TE Connectivity	CRG0603F100K
R14	1	316	Vishay Dale	CRCW0402316RFKED
R19	1	2.15K	Panasonic	ERJ-2RKF2151X
R20,R33,R34,R35,R68	5	100K	TE Connectivity	CRG0603F100K
R24,R39	2	90.9K	Panasonic	ERJ-2RKF9092X
R25,R26,R28,R29,R43,R70,R71,R75, R79,R80,R82,R86,R88	13	0	Samsung	RC1005J000CS
R32	1	80.6K	Panasonic	ERJ-2RKF8062X
R36	1	160k	Panasonic	ERJ-2GEJ164X
R40	1	133k	Yageo	AC0402FR-07133KL
R41	1	42.2K	Panasonic	ERJ-2RKF4222X
R42	1	61.9K	Panasonic	ERJ-2RKF6192X
R44,R55	2	20K	Yageo	ERJ-3EKF2002V
R45,R46,R49,R50,R51,R52	6	270	Panasonic	ERJ-2RKF2700X
R48,R53,R63,R64,R65,R66	6	4.7K	Samsung	RC1005J472CS
R54	1	330	Panasonic	ERJ-2RKF3300X
R58,R61,R224,R225	4	22	Panasonic	ERJ-2GEJ220X
R59,R60	2	2.2K	Panasonic	ERJ-2RKF2201X
R69,R89,R90,R226,R227, R228,R229,R251	8	100	Samsung	RC1005F101CS
R95	1	80.6K	Panasonic	ERJ-2RKF8062X

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Table 4-1. DLPLCRC964EVM Bill of Materials (continued)

Reference	Quantity	Part	MFG	MFG Part Number
R96	1	160k	Panasonic	ERJ-2GEJ164X
R232,R233,R234,R235	4	10m	Rohm	LTR18EZPFU10L0
R252	1	100	Samsung	RC1005F101CS
SW1	1	SW SPST	C&K COMPONENTS	GT12MSCBE
SW2	1	EVQ-PE105K	Panasonic	EVQ-PE105K
TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8, TP9,TP10,TP11,TP23,TP24,TP25, TP26,TP27,TP28,TP29,TP30,TP31, TP32,TP33,TP34,TP35,TP36,TP37, TP38,TP39,TP40,TP41,TP42,TP43, TP44,TP45,TP46,TP47,TP48,TP49, TP50,TP51,TP52	41	Testpoint		
TP12,TP13,TP14,TP15,TP16, TP17,TP18,TP19,TP21,TP22	10	GND Testpoint	Keystone	5006
TP20	1	GND Testpoint	Keystone	5006
U1	1	N-CHANNEL MOSFET	Diodes Inc	DMN67D8L
U2,U7	2	SN74LVC1G07	Texas Instruments	SN74LVC1G07DBVR
U3	1	TPS259241	Texas Instruments	TPS259241DRCT
U4	1	CSD17579	Texas Instruments	CSD17579Q5AT
U5,U6,U16,U17,U18,U19,U20,U21	8	N-CHANNEL MOSFET	FAIRCHILD SEMI	FDV303N
U8,U9	2	LMZ31710	Texas Instruments	LMZ31710RVQR
U10	1	LM3880-1AE	Texas Instruments	LM3880QMFE-1AE/NOPB
U11	1	TPS548B22	Texas Instruments	TPS548B22RVFT
U12	1	TPS8268180	Texas Instruments	TPS8268180SIPT
U13	1	TPS62095	Texas Instruments	TPS62095RGTR
U14	1	DLPC964ZUM	DLP	DLPC964ZUM
U15,U22	2	SN74LVC1G17	Texas Instruments	SN74LVC1G17DBVRG4
U23	1	S25FS256SAGNF	Cypress	S25FS256SAGNFI000
U24	1	S25FL256SAGMFI01	Cypress	S25FL256SAGMFI011
U25	1	CDCM61002	Texas Instruments	CDCM61002RHBR
U26	1	DS90LV110T	Texas Instruments	DS90LV110TMTC/NOPB
U27	1	TPD4E1U06	Texas Instruments	TPD4E1U06DBVR
U28	1	CDCM61001	Texas Instruments	CDCM61001RHBT
U29	1	CY7C65215	Cypress	CY7C65215-32LTXI
U30	1	TCA9406	Texas Instruments	TCA9406DCUR
U31	1	CDCM61004	Texas Instruments	CDCM61004RHBT
U32	1	TXB0108PWR	Texas Instruments	TXB0108PWR
U33	1	SN74AUC245	Texas Instruments	SN74AUC245RGYR
X1,X2	2	ASDMB-25.000MHZ	Abracon	ASDMB-25.000MHZ-LY-T
X3	1	DSC6111JE1A-PROGRAMMABLE	Microchip	DSC6111JE1A-PROGRAMMABLE

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5 Additional Information

5.1 Abbreviations and Acronyms

The following lists abbreviations and acronyms used in this manual:

Apps FPGA	AMD Xilinx UltraScale+ FPGA on the ZCU102 EVM or similar board for customer applications
BOM	Bill of Materials
BPG	Bitplane Pattern Generator
DLL	Dynamic Link Library
DMD	Digital Micromirror Device
EVM	Evaluation Module (Board)
FMC	FPGA Mezzanine Connector
FPGA	Field Programmable Gate Array
FW	Firmware
GPIO	General Purpose Input Output
GUI	Graphical User Interface
HPC	High Pin Count
HSS	High Speed Serial
HSSI	High Speed Serial Interface
HW	Hardware
I^2C	Inter-Integrated Circuit
LED	Light Emitting Diode
MCP	Mirror Clocking Pulse
NC	Not Connected
PC	Personal Computer
PCB	Printed Circuit Board
PG	Power Good
PLL	Phase-Locked Loop
PROM	Programmable Read-Only Memory
SW	Switch
USB	Universal Serial Bus
VHDL	Verification and Hardware Description Language

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5.3 References

1. Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit Quick Start Guide
2. ZCU102 Evaluation Board User Guide
3. DLPC964 Apps FPGA User's Guide

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5.4 Safety

5.4.1 Caution Labels

CAUTION



To minimize the risk of fire or equipment damage, make sure that air is allowed to circulate freely around the DLPLCRC964EVM controller board while operating.

CAUTION



The DLPLCRC964EVM contains ESD-sensitive components. Handle with care to prevent permanent damage.

CAUTION



When choosing your LED or laser component (not included with this EVM) the end user must consult the data sheet supplied by the manufacturer of the illuminator to identify the EN62471 Risk Group Rating and review any potential eye hazards associated with the illuminator chosen. Always consider and implement the use of effective light filtering and darkening protective eye wear and be fully aware of surrounding laboratory-type set-ups when viewing intense light sources that can be required to minimize or eliminate such risks to avoid accidents related to temporary blindness.

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6 Related Documentation from Texas Instruments

Component data sheets, technical documents, design documents, and ordering information can be found at the following links:

DLPC964 Digital Controller Product Folder

DLP LightCrafter DLPC964 EVM Tool Folder

DLP991UFLV DMD Product Folder

DLP LightCrafter DLP991UFLV DMD EVM Product Folder

DLPC964 Apps FPGA Guide

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2026) to Revision E (November 2026)	Page
• Document title updated	0

Changes from Revision C (July 2026) to Revision D (August 2026)	Page
• Changed use of the term "female" to "socket" to avoid unnecessary gendered language	6
• Changed use of the term "male" to "plug" to avoid unnecessary gendered language	7
• Changed use of the term "male" to "plug" and "female" to "socket" to avoid unnecessary gendered language	16
• Updating all link references to point to the version of Vivado utilized for the Apps FPGA Design	32
• Added *Programming Apps FPGA by Flash* section	32
• Updating Version of Vivado used to match development version and validation supported version	32

Changes from Revision B (February 2025) to Revision C (July 2026)	Page
• Updated reference to FPGA to UltraScale+; Images needs to be updated to reflect the change	5
• Updated reference from VC-707 to ZCU102	17
• Updated to match vivado version used for development and validations	29
•	39
• Updating References & links from VC707 to ZCU102; needs to be updated with updated dlpu133b version, when that is complete	39

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