XTR105 4-20mA Current Transmitter With Sensor Excitation and Linearization

1 Features

- Low unadjusted error
- Two precision current sources: 800μA each
- Linearization
- 2-wire or 3-wire RTD operation
- Low offset drift: 0.4μV/°C
- Low output current noise: $30nA_{PP}$
- High PSRR: 110dB minimum
- High CMRR: 86dB minimum
- Wide supply range: 7.5V to 36V
- Packages: DIP-14 and SOIC-14

2 Applications

- Field transmitter and sensor
- Factory automation
- Temperature transmitter
- Pressure transmitter
- Industrial PLC systems
- SCADA remote data acquisition
- Compatible with HART modem

3 Description

The XTR105 is a monolithic 4mA to 20mA, 2-wire current transmitter with two precision current sources. This device provides complete current excitation for platinum RTD temperature sensors and bridges, instrumentation amplifiers, and current output circuitry on a single integrated circuit.

Versatile linearization circuitry provides a 2nd-order correction to the RTD, typically achieving a 40:1 improvement in linearity.

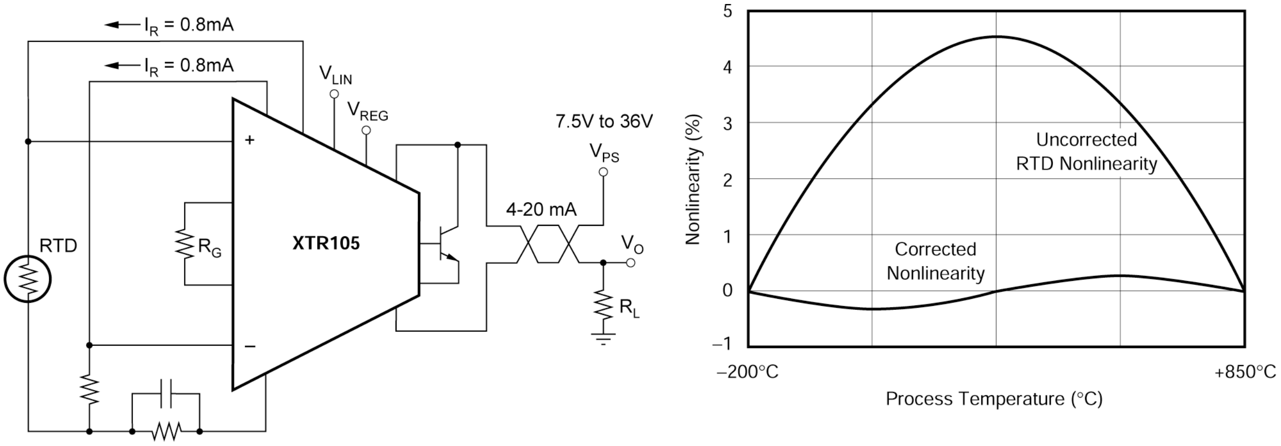
Instrumentation amplifier gain can be configured for a wide range of temperature or pressure measurements. Total unadjusted error of the complete current transmitter is low enough to permit use without adjustment in many applications. This includes zero output current drift, span drift, and nonlinearity. The XTR105 operates on loop power-supply voltages down to 7.5V.

The XTR105 is available in DIP-14 and SOIC-14 surface-mount packages and is specified for the industrial temperature range of –40°C to +85°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
XTR105	D (SOIC, 14)	8.65mm × 6mm
	N (PDIP, 14)	19.3mm × 9.4mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable



Pt100 Nonlinearity Correction Using the XTR105

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4 Pin Configuration and Functions

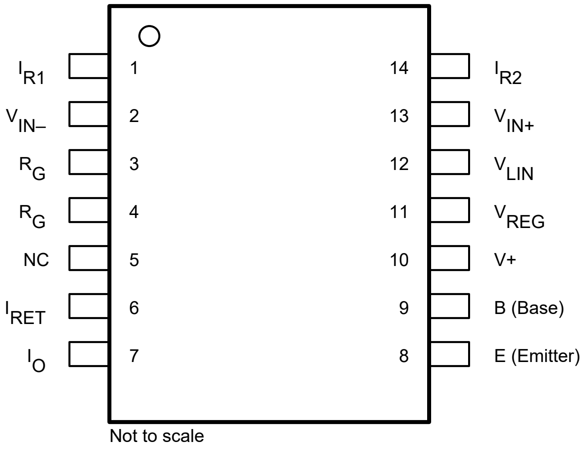


Figure 4-1. D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
B (Base)	9	Output	Base connection for external transistor
E (Emitter)	8	Input	Emitter connection for external transistor
I_O	7	Output	Regulated 4mA to 20mA current loop output
I_{R1}	1	Output	800μA reference current output, channel 1
I_{R2}	14	Output	800μA reference current output, channel 2
I_{RET}	6	Input	*Local ground* return pin for V_{REG}, V_{LIN}, I_{R1}, and I_{R2}
NC	5	—	Not internally connected
R_G	3, 4	—	Input stage gain setting pins. The resistance R_G between pins 3 and 4 sets the gain of the voltage-to-current transfer function
V+	10	Power	Loop power supply
$V_{IN–}$	2	Input	Negative (inverting) differential voltage input
V_{IN+}	13	Input	Positive (noninverting) differential voltage input
V_{LIN}	12	Output	Linearity correction voltage output
V_{REG}	11	Output	5.1V regulator voltage output

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 8.1.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V+	Power supply (referenced to the I_O pin)		40	V
V_{IN}	Input voltage, $V_{IN+} – V_{IN–}$ (referenced to the I_O pin)	0	V+	V
	Output current limit		Continuous	
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		165	°C
T_{stg}	Storage temperature	–55	125	°C
	Lead temperature (soldering, 10s)		300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Power supply (referenced to the I_O pin)	7.5	24	36	V
T_A	Specified temperature	−40		85	°C

5.3 Thermal Information

THERMAL METRICS(1)		XTR105		UNIT
		D (SOIC)	N (PDIP)	
		14 PINS		
$R_{θJA}$	Junction-to-ambient thermal resistance	87.3	54.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	47.3	31.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	46.6	25.8	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	9.9	9.6	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	46.1	25.3	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

5.4 Electrical Characteristics

at T_A = +25°C, V+ = 24V, TIP29C external transistor, and all chip site origin (CSO), (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
OUTPUT							
Output current equation	V_{IN} in volts, R_G in ohms			$I_O = V_{IN} \times (40 / R_G) + 4mA$			
Output current, specified range				4		20	mA
Overscale limit				24	27	30	mA
Underscale limit	I_{REG} = 0V			1.8	2.2	2.6	mA
ZERO OUTPUT (1)	V_{IN} = 0V, R_G = ∞				4		mA
Initial error	XTR105P, XTR105U				±5	±25	μA
	XTR105PA, XTR105UA				±5	±50	
vs temperature	T_A = –40°C to +85°C	XTR105P, XTR105U			±0.07	±0.5	μA/°C
		XTR105PA, XTR105UA			±0.07	±0.9	
vs supply voltage, V+	V+ = 7.5V to 36V				0.04	0.2	μA/V
vs common-mode voltage	V_{CM} = 1.25V to 3.5V(2)				0.02		μA/V
vs V_{REG} output current					0.3		μA/mA
Noise, 0.1Hz to 10Hz					0.03		μA_{PP}
SPAN							
Span equation (transconductance)					S = $40/R_G$		A/V
Initial error(3)	Full-scale (V_{IN}) = 50mV	XTR105P, XTR105U			±0.05	±0.2	%
		XTR105PA, XTR105UA			±0.05	±0.4	
vs temperature(3)	T_A = –40°C to +85°C				±3	±25	ppm/°C
Nonlinearity, ideal input(4)	Full-scale (V_{IN}) = 50mV				0.003	0.01	%
INPUT (5)							
Offset voltage	V_{CM} = 2V	CSO: SHE	XTR105P, XTR105U		±50	±100	μV
			XTR105PA, XTR105UA		±50	±250	
		CSO: TID			±7		
vs temperature	T_A = –40°C to +85°C	CSO: SHE	XTR105P, XTR105U		±0.4	±1.5	μV/°C
			XTR105PA, XTR105UA		±0.4	±3	
		CSO: TID			±0.1		
vs supply voltage, V+	V+ = 7.5V to 36V				±0.3	±3	μV/V
vs common-mode voltage, RTI (CMRR)	V_{CM} = 1.25V to 3.5V(2)	XTR105P, XTR105U			±10	±50	μV/V
		XTR105PA, XTR105UA			±10	±100	
Common-mode input range(2)				1.25		3.5	V
Input bias current	CSO: SHE	XTR105P, XTR105U			5	25	nA
		XTR105PA, XTR105UA			5	50	
	CSO: TID				0.9	8	
vs temperature	T_A = –40°C to +85°C	CSO:SHE			20		pA/°C
		CSO: TID			1		
Input offset current	XTR105P, XTR105U				±0.2	±3	nA
	XTR105PA, XTR105UA				±0.2	±10	
vs temperature	T_A = –40°C to +85°C	CSO: SHE			5		pA/°C
		CSO: TID			±1		

5.4 Electrical Characteristics (continued)

at T_A = +25°C, V+ = 24V, TIP29C external transistor, and all chip site origin (CSO), (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Impedance, differential				0.1 || 1		GΩ || pF
Common-mode				5 || 10		GΩ || pF
Noise	f = 0.1Hz to 10Hz			0.6		μA_{PP}
CURRENT SOURCES (6)						
Current				800		µA
Accuracy	XTR105P, XTR105U			±0.05	±0.2	%
	XTR105PA, XTR105UA			±0.05	±0.4	
vs temperature	T_A = –40°C to +85°C	XTR105P, XTR105U		±15	±35	ppm/°C
		XTR105PA, XTR105UA		±15	±75	
vs power supply, V+	V+ = 7.5V to 36V	CSO: SHE		±10	±25	ppm/V
		CSO: TID		±2	±15	
Matching	XTR105P, XTR105U			±0.02	±0.1	%
	XTR105PA, XTR105UA			±0.02	±0.2	
vs temperature	T_A = –40°C to +85°C	XTR105P, XTR105U		±3	±15	ppm/°C
		XTR105PA, XTR105UA		±3	±30	
vs power supply, V+	V+ = 7.5V to 36V			1	10	ppm/V
Compliance voltage	Positive		(V+) − 3	(V+) − 2.5		V
	Negative(2)		0	−0.2		
Output impedance				150		MΩ
Noise	f = 0.1Hz to 10Hz			0.003		μA_{PP}
V_{REG} (2)				5.1		V
Accuracy				±0.02	±0.1	V
vs temperature	T_A = –40°C to +85°C			±0.5		mV/°C
vs supply voltage, V+				1		mV/V
Output current				±1		mA
Output impedance				75		Ω
LINEARIZATION						
R_{LIN} (internal)				1		kΩ
Accuracy	XTR105P, XTR105U			±0.2	±0.5	%
	XTR105PA, XTR105UA			±0.2	±1	
vs temperature	T_A = –40°C to +85°C			±25	±100	ppm/°C

(1) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero.
(2) Voltage measured with respect to I_{RET} pin.
(3) Does not include initial error or TCR of gain-setting resistor, R_G.
(4) Increasing the full-scale input range improves nonlinearity.
(5) Does not include zero output initial error.
(6) Current source output voltage V_O = 2V, with respect to I_{RET} pin.

5.5 Typical Characteristics

at T_A = +25°C and V+ = 24V, and all chip site origin (CSO), (unless otherwise noted)

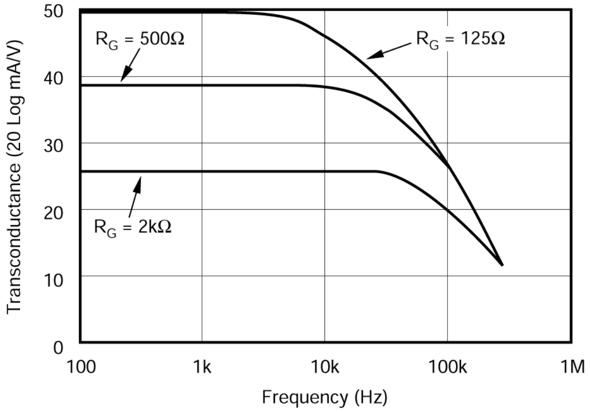
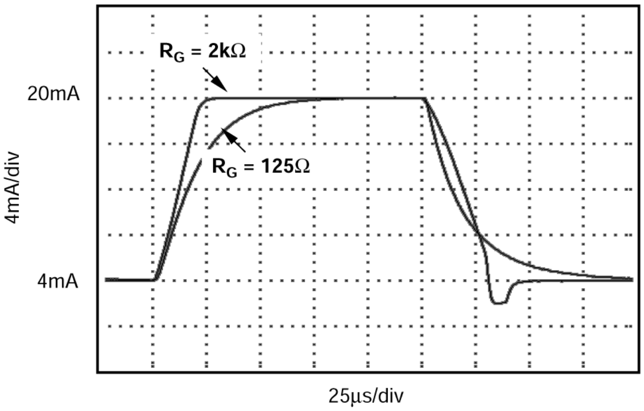
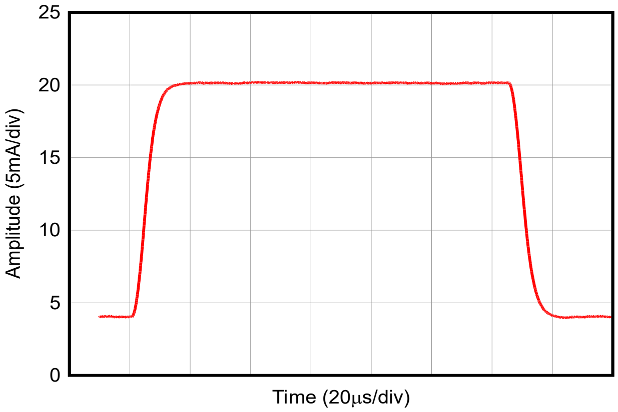


Figure 5-1. Transconductance vs Frequency



CSO: SHE

Figure 5-2. Step Response



CSO: TID

Figure 5-3. Step Response, R_G = 125Ω, 2kΩ

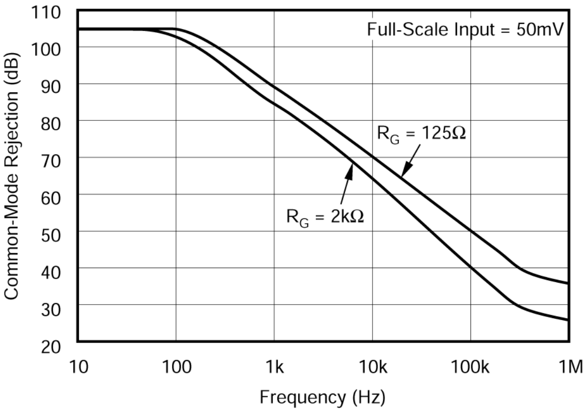


Figure 5-4. Common-Mode Rejection vs Frequency

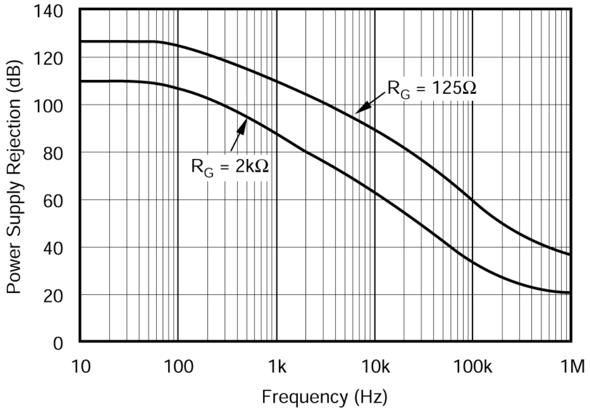
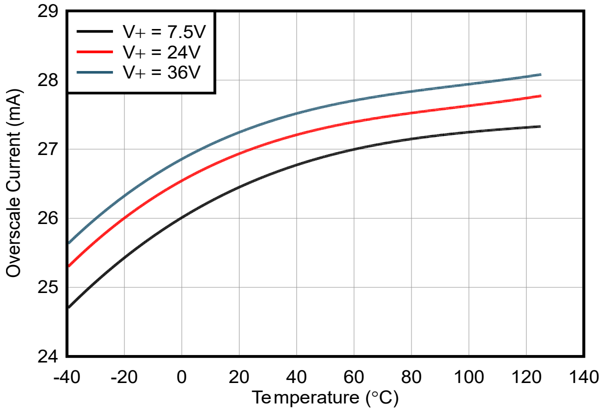


Figure 5-5. Power-Supply Rejection vs Frequency



With external transistor

Figure 5-6. Overscale Current vs Temperature

5.5 Typical Characteristics (continued)

at T_A = +25°C and V+ = 24V, and all chip site origin (CSO), (unless otherwise noted)

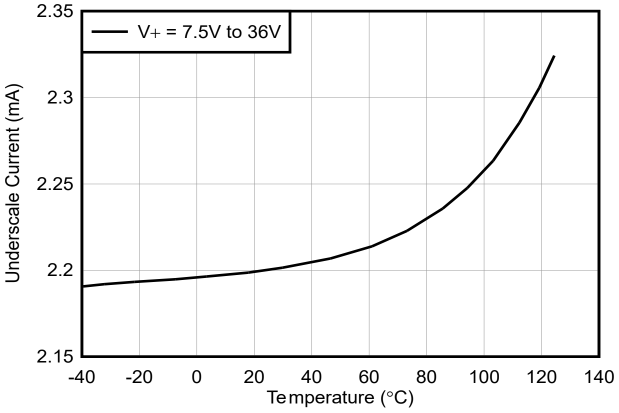


Figure 5-7. Underscale Current vs Temperature

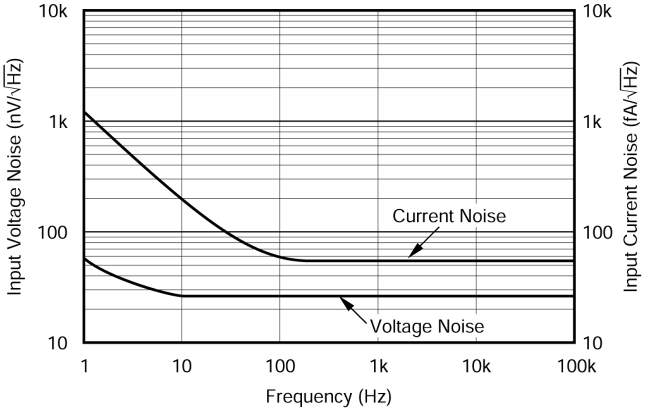


Figure 5-8. Input Voltage and Current Noise Density vs Frequency

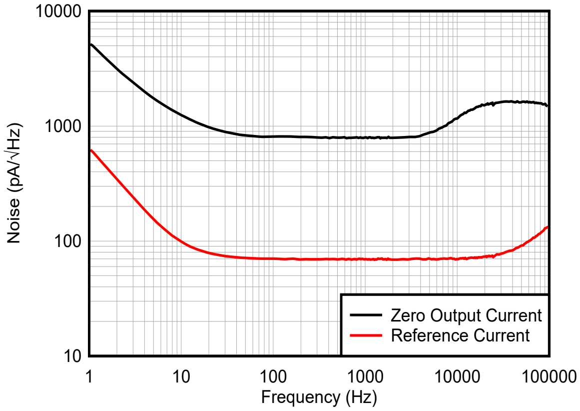
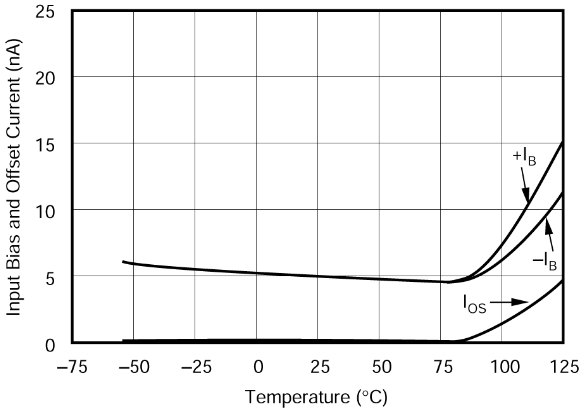
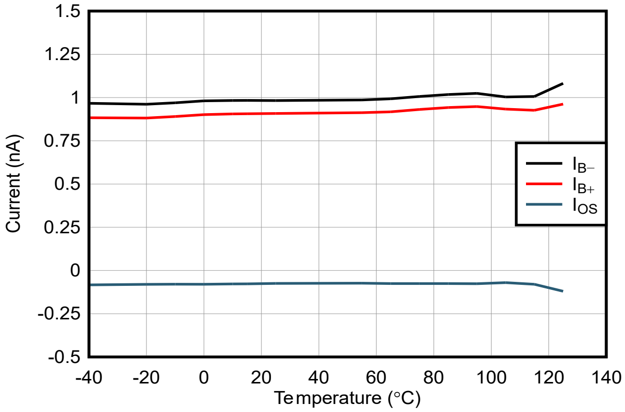


Figure 5-9. Zero Output and Reference Current Noise vs Frequency



CSO: SHE

Figure 5-10. Input Bias and Offset Current vs Temperature



CSO: TID

Figure 5-11. Input Bias and Offset Current vs Temperature

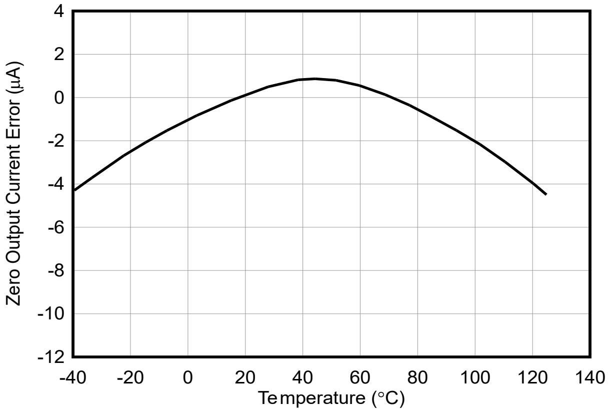
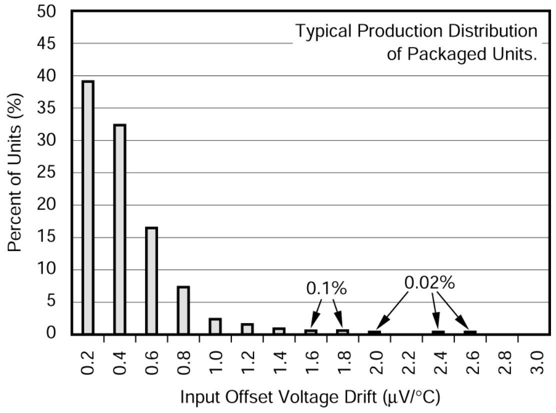


Figure 5-12. Zero Output Current Error vs Temperature

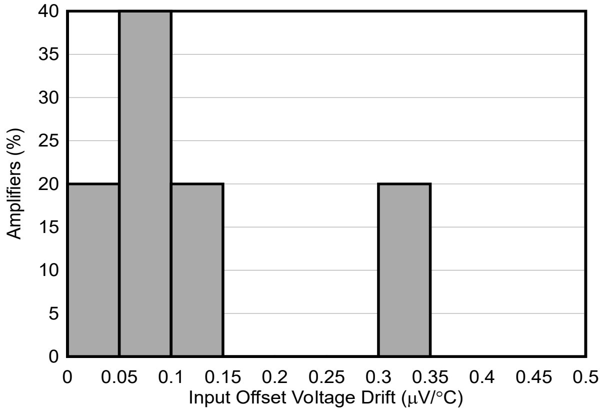
5.5 Typical Characteristics (continued)

at T_A = +25°C and V+ = 24V, and all chip site origin (CSO), (unless otherwise noted)



CSO: SHE

Figure 5-13. Input Offset Voltage Drift Production Distribution



CSO: TID

Figure 5-14. Input Offset Voltage Drift Production Distribution

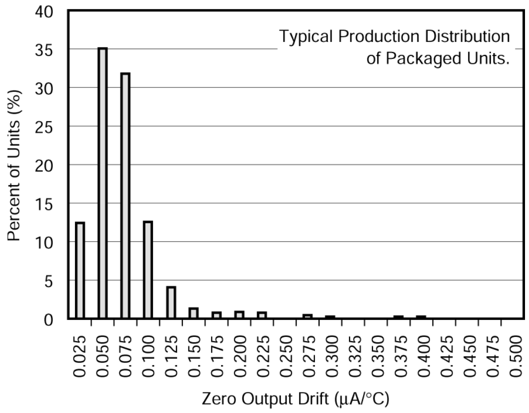


Figure 5-15. Zero Output Drift Production Distribution

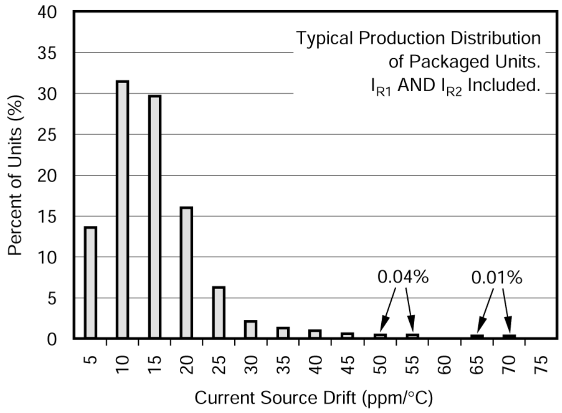


Figure 5-16. Current Source Drift Production Distribution

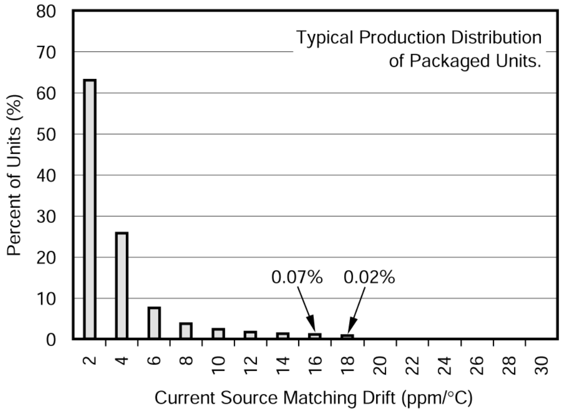
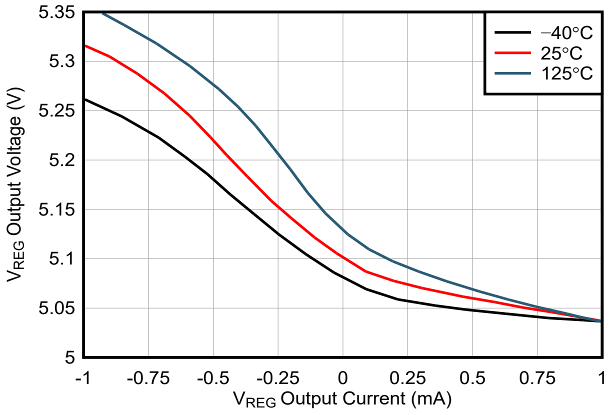


Figure 5-17. Current Source Matching Drift Production Distribution



Above 1mA, zero output degrades

Figure 5-18. V_{REG} Output Voltage vs v_{REG} Output Current

5.5 Typical Characteristics (continued)

at T_A = +25°C and V+ = 24V, and all chip site origin (CSO), (unless otherwise noted)

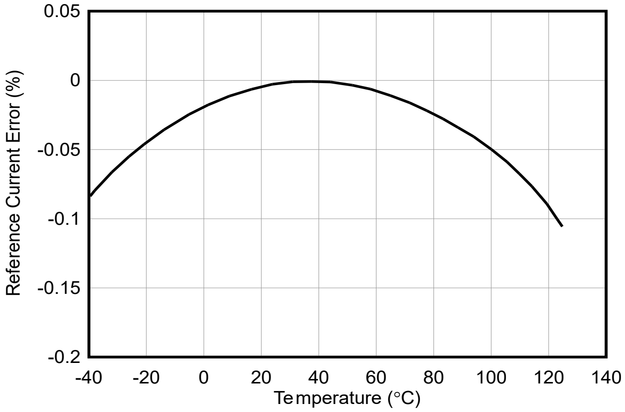


Figure 5-19. Reference Current Error vs Temperature

6 Detailed Description

6.1 Overview

The XTR105 is a monolithic 4mA to 20mA, 2-wire current transmitter with a differential voltage input. Figure 6-1 shows the simplified schematic of the XTR105. The loop power supply, V_+, provides power for all circuitry. The output loop current is modulated by the XTR105 and is typically measured as a voltage across a series load resistor (R_L).

The instrumentation amplifier input of the XTR105 measures the voltage difference between the noninverting and inverting inputs. This difference is then gained up according to the value of R_G, and expressed as a regulated current output.

The two matched 0.8mA current sources are typically used to drive an RTD and zero-setting resistor (R_Z). R_Z determines the static offset of the current output and can be adjusted to correct for offset errors. A linearity correction feature is provided to further improve the RTD response. An additional 5.1V voltage regulator output is provided to power external circuitry such as buffer amplifiers.

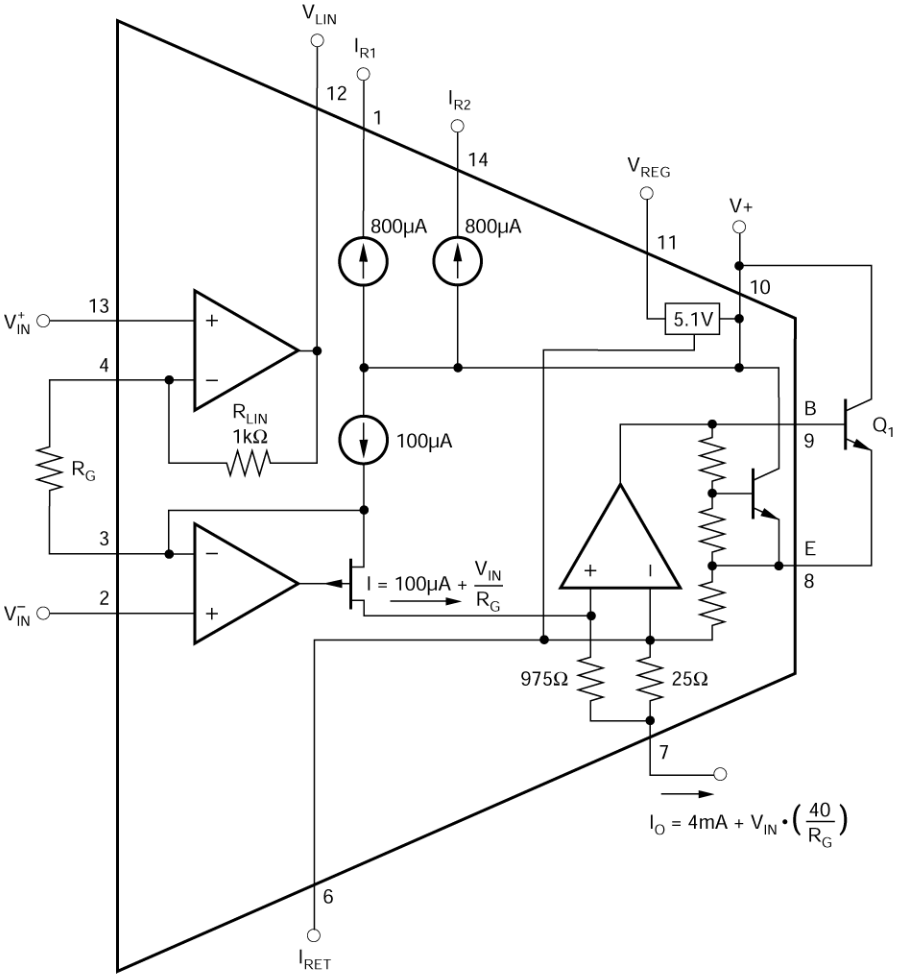
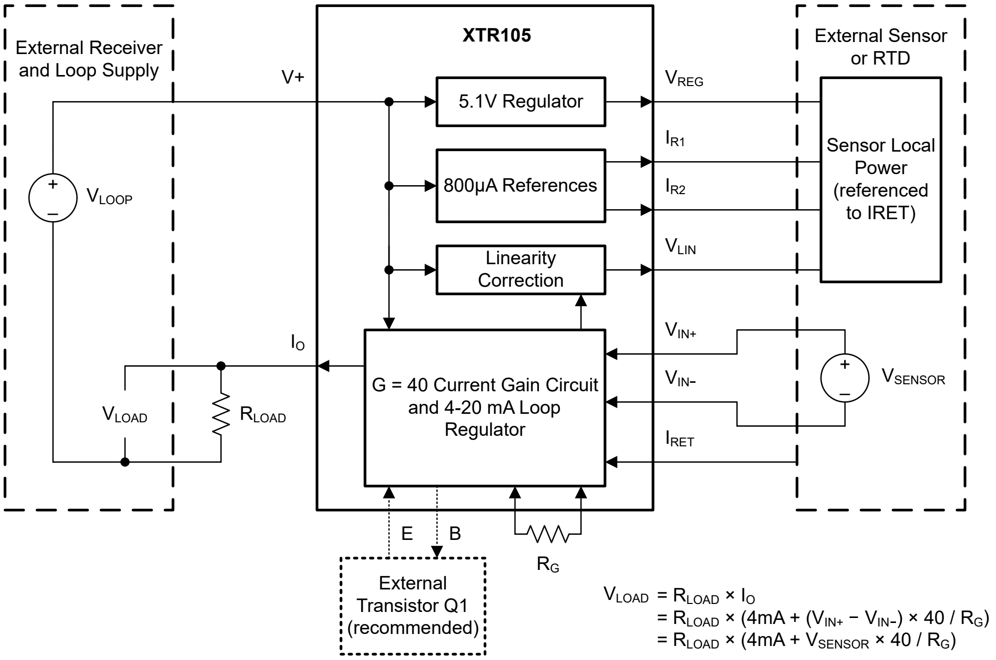


Figure 6-1. Simplified Schematic

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Linearization

RTD temperature sensors are inherently (but predictably) nonlinear. With the addition of one or two external resistors, R_{LIN1} and R_{LIN2}, compensation is possible for most of this nonlinearity by using the V_{LIN} linearity correction feature of the XTR105. This results in a 40:1 improvement in linearity over the uncompensated output.

See Figure 7-1 for a typical 2-wire RTD application with linearization. Resistor R_{LIN1} provides positive feedback and controls linearity correction. R_{LIN1} is chosen according to the desired temperature range. An equation is given in Figure 7-1.

In 3-wire RTD connections, an additional resistor, R_{LIN2}, is required. As with the 2-wire RTD application, R_{LIN1} provides positive feedback for linearization. R_{LIN2} provides an offset canceling current to compensate for wiring resistance encountered in remotely located RTDs. R_{LIN1} and R_{LIN2} are chosen such that the currents are equal. This makes the voltage drop in the wiring resistance to the RTD a common-mode signal that is rejected by the XTR105. The nearest standard 1% resistor values for R_{LIN1} and R_{LIN2} are adequate for most applications. Table 7-1 provides the 1% resistor values for a 3-wire Pt100 RTD connection.

If no linearity correction is desired, leave the V_{LIN} pin open. With no linearization, R_G = 2500m × V_{FS}, where V_{FS} = full-scale input range.

6.3.1.1 High-Resistance RTDs

The text and figures thus far have assumed a Pt100 RTD. With higher resistance RTDs, evaluate the temperature range and input voltage variation to maintain proper common-mode biasing of the inputs. As mentioned previously, R_{CM} can be adjusted to provide an additional voltage drop to bias the inputs of the XTR105 within the common-mode input range.

6.3.2 Voltage Regulator

The V_{REG} pin provides an on-chip voltage source of approximately 5.1V and is designed for powering external input circuitry (as shown in Figure 6-2). This source is a moderately accurate voltage reference, and is not the same reference used to set the 800µA current references. V_{REG} is capable of sourcing approximately 1mA of current. Exceeding 1mA can affect the 4mA zero output.

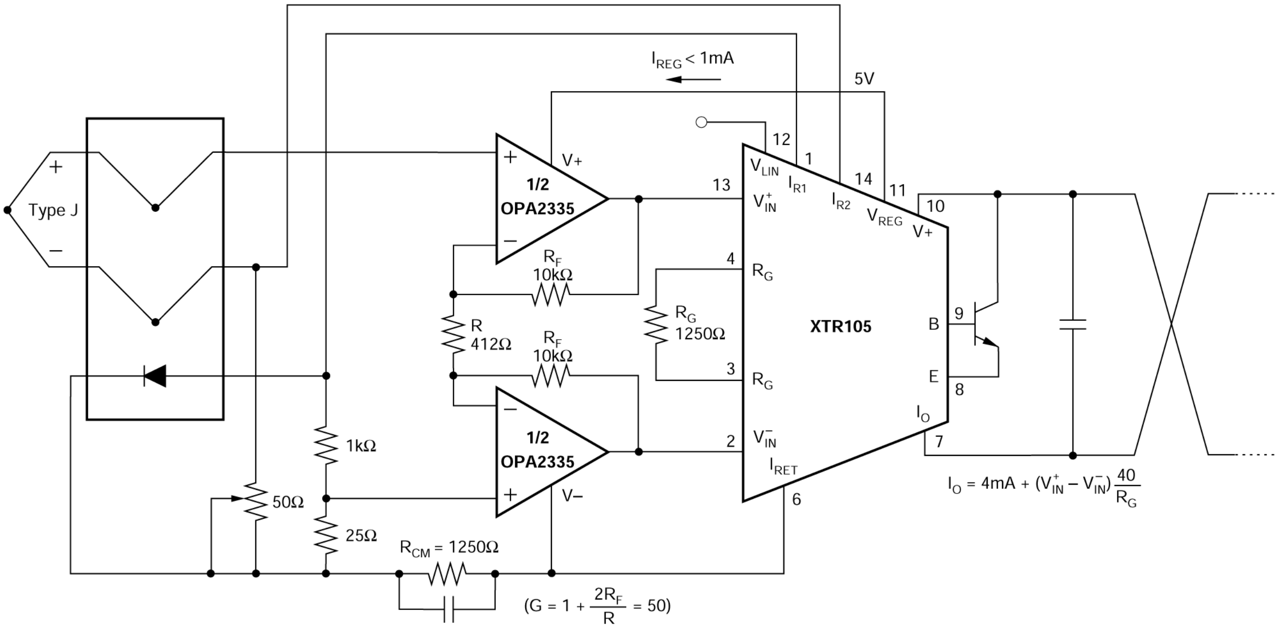
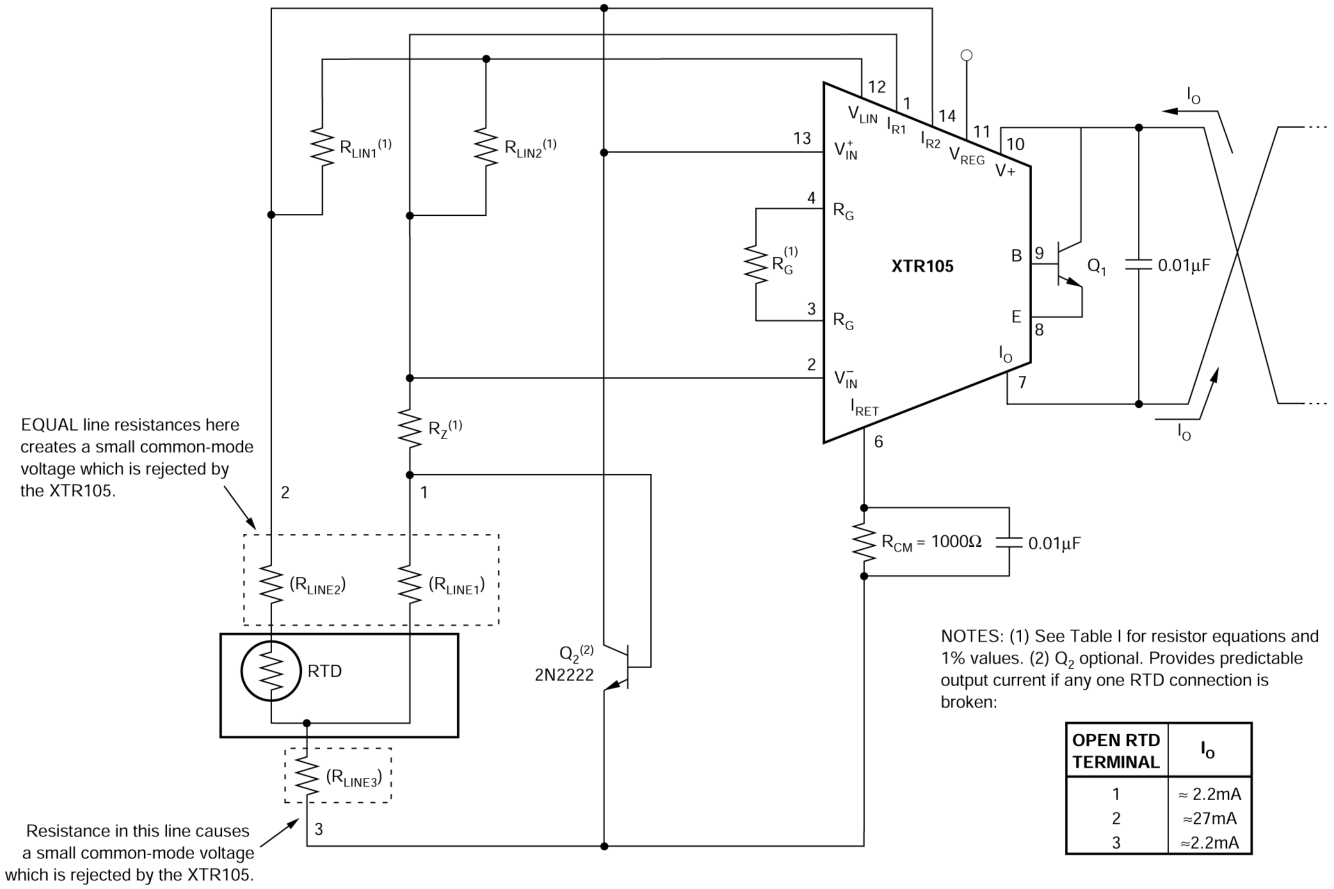


Figure 6-2. Thermocouple Low Offset, Low Drift Loop Measurement With Diode Cold Junction Compensation

6.3.3 Open-Circuit Protection

Optional transistor Q_2 in Figure 6-3 provides predictable behavior with open-circuit RTD connections. If any one of the three RTD connections is broken, the XTR105 output current goes to either the high current limit (≅ 27mA) or low current limit (≅ 2.2mA). This state is easily detected as an out-of-range condition.



EQUAL line resistances here creates a small common-mode voltage which is rejected by the XTR105.

Resistance in this line causes a small common-mode voltage which is rejected by the XTR105.

NOTES: (1) See Table I for resistor equations and 1% values. (2) Q_2 optional. Provides predictable output current if any one RTD connection is broken:

OPEN RTD TERMINAL	I_O
1	≈ 2.2mA
2	≈27mA
3	≈2.2mA

Figure 6-3. Remotely Located RTDs With a 3-Wire Connection

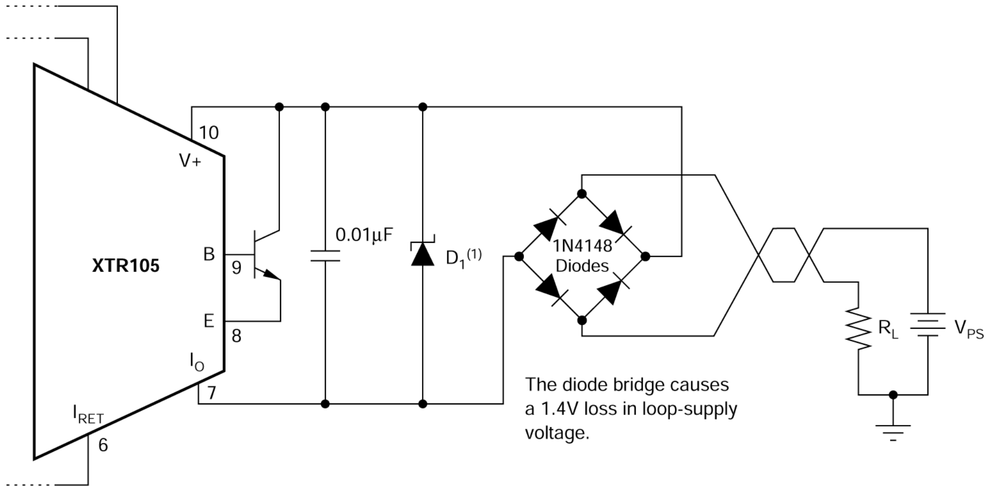
6.3.4 Reverse-Voltage Protection

The XTR105 low compliance rating (7.5V) permits the use of various voltage protection methods without compromising operating range. Figure 6-4 shows a diode bridge circuit that allows normal operation even when the voltage connection lines are reversed. The bridge causes a two diode drop (approximately 1.4V) loss in loop-supply voltage. This results in a compliance voltage of approximately 9V—satisfactory for most applications. If a 1.4V drop in loop supply is too much, a diode can be inserted in series with the loop-supply voltage and the V+ pin. This protects against reverse output connection lines with only a 0.7V loss in loop-supply voltage.

6.3.5 Surge Protection

Remote connections to current transmitters are sometimes subjected to voltage surges. Limit the maximum surge voltage applied to the XTR105 to the lowest practical value. Various zener diodes and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. For example, a 36V protection diode allows proper transmitter operation at normal loop voltages, yet provides an appropriate level of protection against voltage surges. The XTR105 is specified to an absolute maximum loop voltage of 40V.

Most surge protection zener diodes have a diode characteristic in the forward direction that conducts excessive current, possibly damaging receiving-side circuitry, if the loop connections are reversed. If a surge protection diode is used, use a series diode or diode bridge for protection against reversed connections.



The diode bridge causes a 1.4V loss in loop-supply voltage.

Maximum V_{PS} must be less than minimum voltage rating of zener diode.

(1) 36V Zener diode, such as 1N4753A or P6KE39A. Use lower-voltage Zener diodes with loop power-supply voltages < 30V for increased protection.

Figure 6-4. Reverse Voltage Operation and Overvoltage Surge Protection

6.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Figure 7-1 shows the basic connection diagram for the XTR105. The loop power supply, V_{PS}, provides power for all circuitry. Output loop current is measured as a voltage across the series load resistor, R_L.

Two matched 0.8mA current sources drive the RTD and zero-setting resistor, R_Z. The instrumentation amplifier input of the XTR105 measures the voltage difference between the RTD and R_Z. The value of R_Z is chosen to be equal to the resistance of the RTD at the low-scale (minimum) measurement temperature. R_Z can be adjusted to achieve 4mA output at the minimum measurement temperature to correct for input offset voltage and reference current mismatch of the XTR105.

R_{CM} provides an additional voltage drop to bias the inputs of the XTR105 within the common-mode input range. Bypass R_{CM} with a 0.01µF capacitor to minimize common-mode noise. Resistor R_G sets the gain of the instrumentation amplifier according to the desired temperature range. R_{LIN1} provides 2nd-order linearization correction to the RTD, typically achieving a 40:1 improvement in linearity. An additional resistor is required for 3-wire RTD connections (see Figure 6-3).

The transfer function through the complete instrumentation amplifier and voltage-to-current converter is:

$I_O = 4mA + V_{IN} \times (40 / R_G)$

(V_{IN} in volts, R_G in ohms)

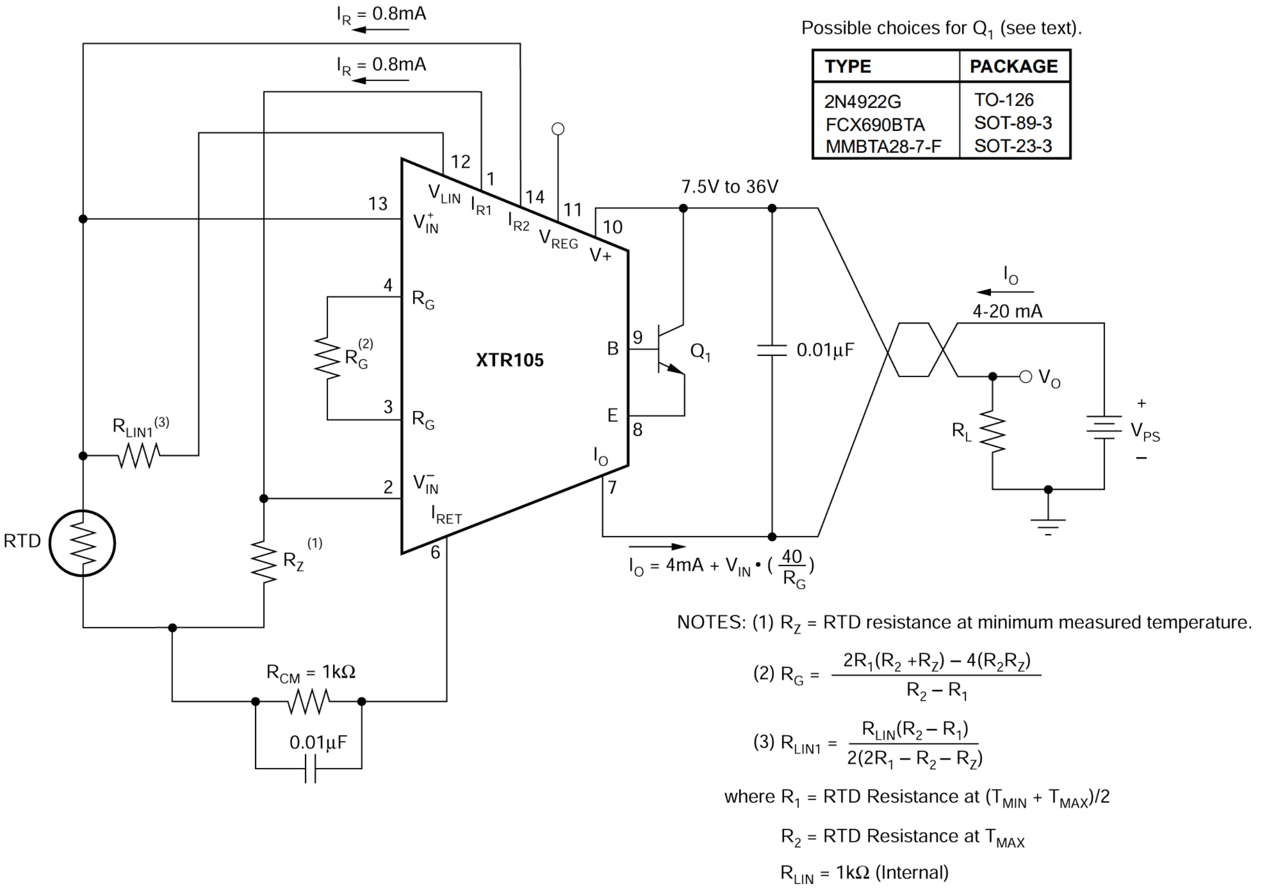
where V_{IN} is the differential input voltage.

A negative input voltage, V_{IN}, causes the output current to be less than 4mA. Increasingly negative V_{IN} causes the output current to limit at approximately 2.2mA. See also typical characteristic *Under-Scale Current vs Temperature*.

Increasingly positive input voltage (greater than the full-scale input) produces increasing output current according to the transfer function, up to the output current limit of approximately 27mA. See also typical characteristic *Over-Scale Current vs Temperature*.

As evident from the transfer function, if no R_G is used the gain is zero and the output is simply the XTR105's zero current. The value of R_G varies slightly for 2-wire RTD and 3-wire RTD connections with linearization. R_G can be calculated from the equations given in Figure 7-1 (2-wire RTD connection) and Table 7-1 (3-wire RTD connection).

The I_{RET} pin is the return path for all current from the current sources and V_{REG}. The I_{RET} pin allows any current used in external circuitry to be sensed by the XTR105 and to be included in the output current without causing an error.



Possible choices for Q_1 (see text).

TYPE	PACKAGE
2N4922G	TO-126
FCX690BTA	SOT-89-3
MMBTA28-7-F	SOT-23-3

NOTES: (1) R_Z = RTD resistance at minimum measured temperature.

(2) $R_G = \frac{2R_1(R_2 + R_Z) - 4(R_2R_Z)}{R_2 - R_1}$

(3) $R_{LIN1} = \frac{R_{LIN}(R_2 - R_1)}{2(2R_1 - R_2 - R_Z)}$

where R_1 = RTD Resistance at $(T_{MIN} + T_{MAX})/2$

R_2 = RTD Resistance at T_{MAX}

R_{LIN} = 1kΩ (Internal)

Figure 7-1. Basic 2-Wire RTD Temperature Measurement Circuit With Linearization

Table 7-1. R_Z, R_G, R_{LIN1}, and R_{LIN2} Standard 1% Resistor Values for 3-Wire Pt100 RTD Connection With Linearization

MEASUREMENT TEMPERATURE SPAN ΔT (°C)

T_{MIN}	100°C	200°C	300°C	400°C	500°C	600°C	700°C	800°C	900°C	1000°C
–200°C	18.7/86.6 15000 16500	18.7/169 9760 11500	18.7/255 8060 10000	18.7/340 6650 8870	18.7/422 5620 7870	18.7/511 4750 7150	18.7/590 4020 6420	18.7/665 3480 5900	18.7/750 3090 5360	18.7/845 2740 4990
–100°C	60.4/80.6 27400 29400	60.4/162 15400 17800	60.4/243 10500 13000	60.4/324 7870 10200	60.4/402 6040 8660	60.4/487 4990 7500	60.4/562 4220 6490	60.4/649 3570 5900	60.4/732 3090 5360	
0°C	100/78.7 33200 35700	100/158 16200 18700	100/237 10500 13000	100/316 7680 10000	100/392 6040 8250	100/475 4870 7150	100/549 4020 6340	100/634 3480 5620		
100°C	137/75 31600 34000	137/150 15400 17800	137/226 10200 12400	137/301 7500 9760	137/383 5760 8060	137/453 4750 6810	137/536 3920 6040			
200°C	174/73.2 30900 33200	174/147 15000 17400	174/221 9760 12100	174/294 7150 9310	174/365 5620 7680	174/442 4530 6490				
300°C	210/71.5 30100 32400	210/143 14700 16500	210/215 9530 11500	210/287 6980 8870	210/357 5360 7320					
400°C	249/68.1 28700 30900	249/137 14000 16200	249/205 9090 11000	249/274 6650 8450						
500°C	280/66.5 28000 30100	280/133 13700 15400	280/200 8870 10500							
600°C	316/64.9 26700 28700	313/130 13000 14700								
700°C	348/61.9 26100 27400									
800°C	374/60.4 24900 26700									

R_Z/R_G
R_{LIN1}
R_{LIN2}

NOTE: The values listed in this table are 1% resistors (in Ω). Exact values may be calculated from the following equations:

R_Z = RTD resistance at minimum measured temperature.

$$R_G = \frac{2(R_2 - R_Z)(R_1 - R_Z)}{(R_2 - R_1)}$$

$$R_{LIN1} = \frac{R_{LIN}(R_2 - R_1)}{2(2R_1 - R_2 - R_Z)}$$

$$R_{LIN2} = \frac{(R_{LIN} + R_G)(R_2 - R_1)}{2(2R_1 - R_2 - R_Z)}$$

where: R_1 = RTD resistance at $(T_{MIN} + T_{MAX})/2$

R_2 = RTD resistance at T_{MAX}

R_{LIN} = 1kΩ (Internal)

EXAMPLE:

The measurement range is –100°C to +200°C for a 3-wire Pt100 RTD connection. Determine the values for R_S, R_G, R_{LIN1}, and R_{LIN2}. Look up the values from the chart or calculate the values according to the equations provided.

METHOD 1: TABLE LOOK UP

For T_{MIN} = –100°C and ΔT = –300°C, the 1% values are:

R_Z = 60.4Ω R_{LIN1} = 10.5kΩ
R_G = 243Ω R_{LIN2} = 13kΩ

METHOD 2: CALCULATION

Step 1: Determine R_Z, R_1, and R_2.

R_Z is the RTD resistance at the minimum measured temperature,T_{MIN} = –100°C. Using Equation 1 at right gives R_Z = 60.25Ω (1% value is 60.4Ω).

R_2 is the RTD resistance at the maximum measured temperature, T_{MAX} = 200°C. Using Equation 2 at right gives R_2 = 175.84Ω.

R_1 is the RTD resistance at the midpoint measured temperature, $T_{MID} = (T_{MIN} + T_{MAX})/2$ = 50°C. R_1 is NOT the average of R_Z and R_2. Using Equation 2 at right gives R_1 = 119.40Ω.

Step 2: Calculate R_G, R_{LIN1}, and R_{LIN2} using equations above.

R_G = 242.3Ω (1% value is 243Ω)
R_{LIN1} = 10.413kΩ (1% value is 10.5kΩ)
R_{LIN2} = 12.936kΩ (1% value is 13kΩ)

Calculation of Pt100 Resistance Values
(according to DIN IEC 751)

(Equation 1) Temperature range from –200°C to 0°C:

$$R_{(T)} = 100\ [1 + 3.90802 \cdot 10^{-3} \cdot T - 0.5802 \cdot 10^{-6} \cdot T^2 - 4.27350 \cdot 10^{-12}\ (T - 100)\ T^3]$$

(Equation 2) Temperature range from 0°C to +850°C:

$$R_{(T)} = 100\ (1 + 3.90802 \cdot 10^{-3} \cdot T - 0.5802 \cdot 10^{-6} \cdot T_2)$$

where: $R_{(T)}$ is the resistance in Ω at temperature T.
T is the temperature in °C.

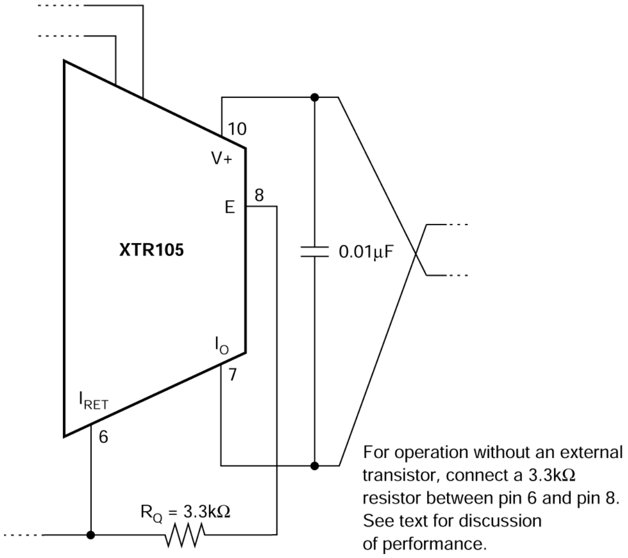
NOTE: Most RTD manufacturers provide reference tables for resistance values at various temperatures.

7.1.1 External Transistor

Transistor Q_1 conducts the majority of the signal-dependent 4-20mA loop current. Using an external transistor isolates the majority of the power dissipation from the precision input and reference circuitry of the XTR105, maintaining excellent accuracy.

The external transistor is inside a feedback loop; therefore, the transistor characteristics are not critical. Requirements are: V_{CEO} = 45V min, β = 40 min, and P_D = 800mW. Power dissipation requirements can be lower if the loop power-supply voltage is less than 36V. Some possible choices for Q_1 are listed in Figure 7-1.

The XTR105 operates without this external transistor; however, accuracy is somewhat degraded as a result of the internal power dissipation and resulting self-heating. Operation without Q_1 is not recommended for extended temperature ranges. A resistor (R = 3.3kΩ) connected between the I_{RET} pin and the E (emitter) pin is advised for operation below 0°C without Q_1 to support the full 20mA full-scale output, especially with V+ near 7.5V.



For operation without an external transistor, connect a 3.3kΩ resistor between pin 6 and pin 8. See text for discussion of performance.

Figure 7-2. Operation Without an External Transistor

7.1.2 Loop Power Supply

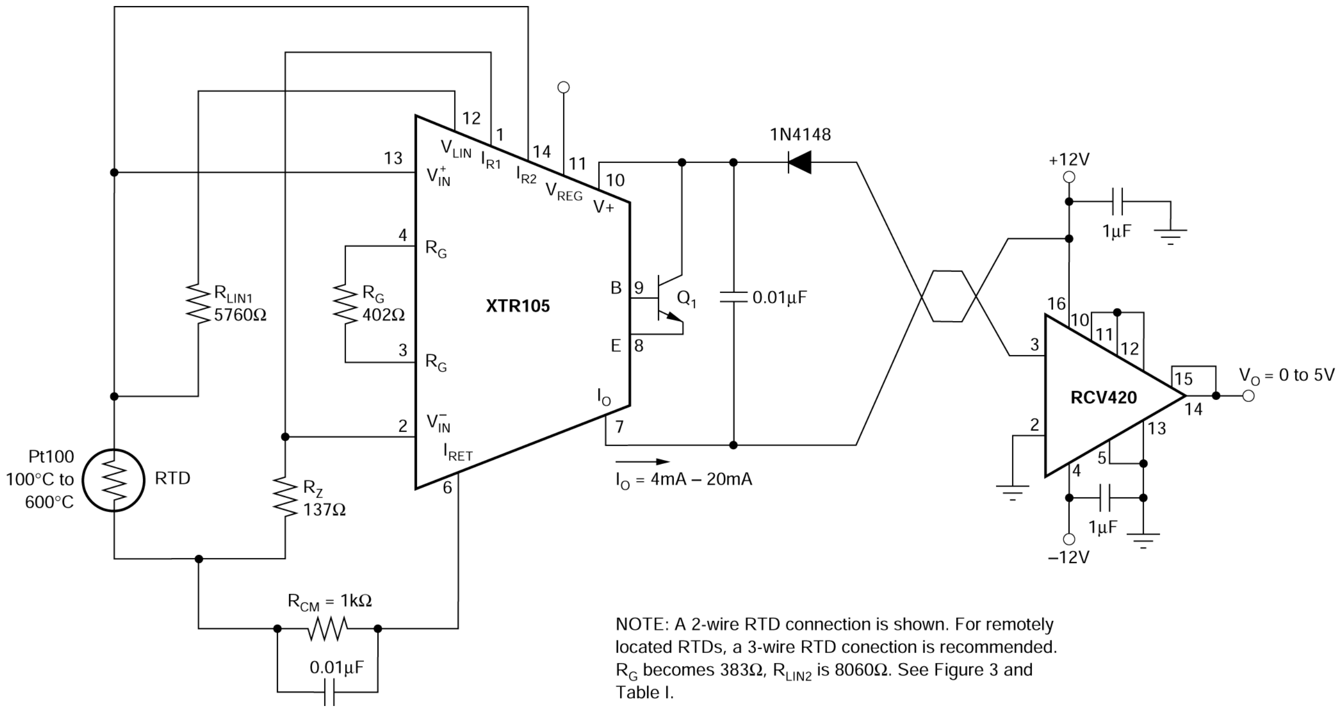
The voltage applied to the XTR105, V+, is measured with respect to the I_O connection, pin 7. V+ can range from 7.5V to 36V. The loop-supply voltage, V_{PS}, differs from the voltage applied to the XTR105 according to the voltage drop on the current sensing resistor, R_L (plus any other voltage drop in the line).

If a low loop-supply voltage is used, R_L (including the loop wiring resistance) must be made a relatively low value so that V+ remains 7.5V or greater for the maximum loop current of 20mA:

$$R_L \max = \left(\frac{(V+) - 7.5V}{20mA}\right) - R_{WIRING}$$

For loop currents up to 30mA, design for V+ equal or greater than 7.5V to allow for out-of-range input conditions.

The low operating voltage (7.5V) of the XTR105 allows operation directly from personal computer power supplies (12V ±5%). When used with the RCV420 current loop receiver (see Figure 7-3), the load resistor voltage drop is limited to 3V.



NOTE: A 2-wire RTD connection is shown. For remotely located RTDs, a 3-wire RTD conection is recommended. R_G becomes 383Ω, R_{LIN2} is 8060Ω. See Figure 3 and Table I.

Figure 7-3. ±12V Powered Transmitter-Receiver Loop

7.1.3 2-Wire and 3-Wire RTD Connections

In Figure 7-1, the RTD can be located remotely simply by extending the two connections to the RTD. With this remote 2-wire connection to the RTD, line resistance introduces error. This error can be partially corrected by adjusting the values of R_Z, R_G, and R_{LIN1}.

A better method for remotely located RTDs is the 3-wire RTD connection (see Figure 6-3). This circuit offers improved accuracy. R_Z's current is routed through a third wire to the RTD. Assuming line resistance is equal in RTD lines 1 and 2, this produces a small common-mode voltage that is rejected by the XTR105. A second resistor, R_{LIN2}, is required for linearization.

Note that although the 2-wire and 3-wire RTD connection circuits are very similar, the gain-setting resistor, R_G, has slightly different equations:

2-wire:

$$R_G = \frac{2R_1(R_2 + R_Z) - 4(R_2R_Z)}{R_2 - R_1}$$

3-wire:

$$R_G = \frac{2(R_2 - R_Z)(R_1 - R_Z)}{R_2 - R_1}$$

where

- R_Z = RTD resistance at T_{MIN}
- R_1 = RTD resistance at $(T_{MIN} + T_{MAX}) / 2$
- R_2 = RTD resistance at T_{MAX}

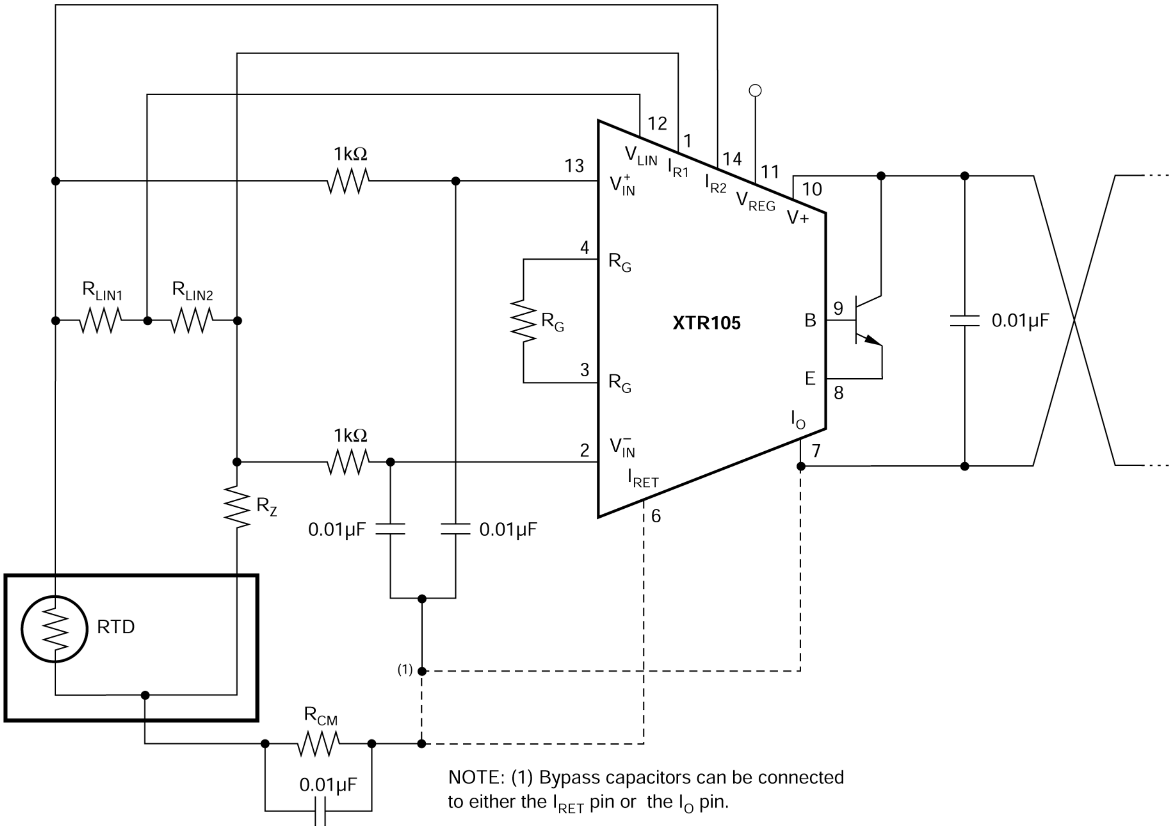
To maintain good accuracy, use at least 1% (or better) resistors for R_G. Table 7-1 provides standard 1% R_G resistor values for a 3-wire Pt100 RTD connection with linearization.

7.1.4 Radio Frequency Interference

The long wire lengths of current loops invite radio frequency (RF) interference. RF can be rectified by the sensitive input circuitry of the XTR105, causing errors. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the RTD sensor is remotely located, the interference can enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current loop connections.

Bypass capacitors on the input reduce or eliminate this input interference. Connect these bypass capacitors to the I_{RET} terminal (see Figure 7-4). Although the dc voltage at the I_{RET} terminal is not equal to 0V (at the loop supply, V_{PS}), this circuit point can be considered the transmitter *ground*. The 0.01µF capacitor connected between V+ and I_O can help minimize output interference.



NOTE: (1) Bypass capacitors can be connected to either the I_{RET} pin or the I_O pin.

Figure 7-4. Input Bypassing Technique With Linearization

7.1.5 Error Analysis

Many applications require adjustment of initial errors. Input offset and reference current mismatch errors can be corrected by adjustment of the zero resistor, R_Z. Adjusting the gain-setting resistor, R_G, corrects any errors associated with gain.

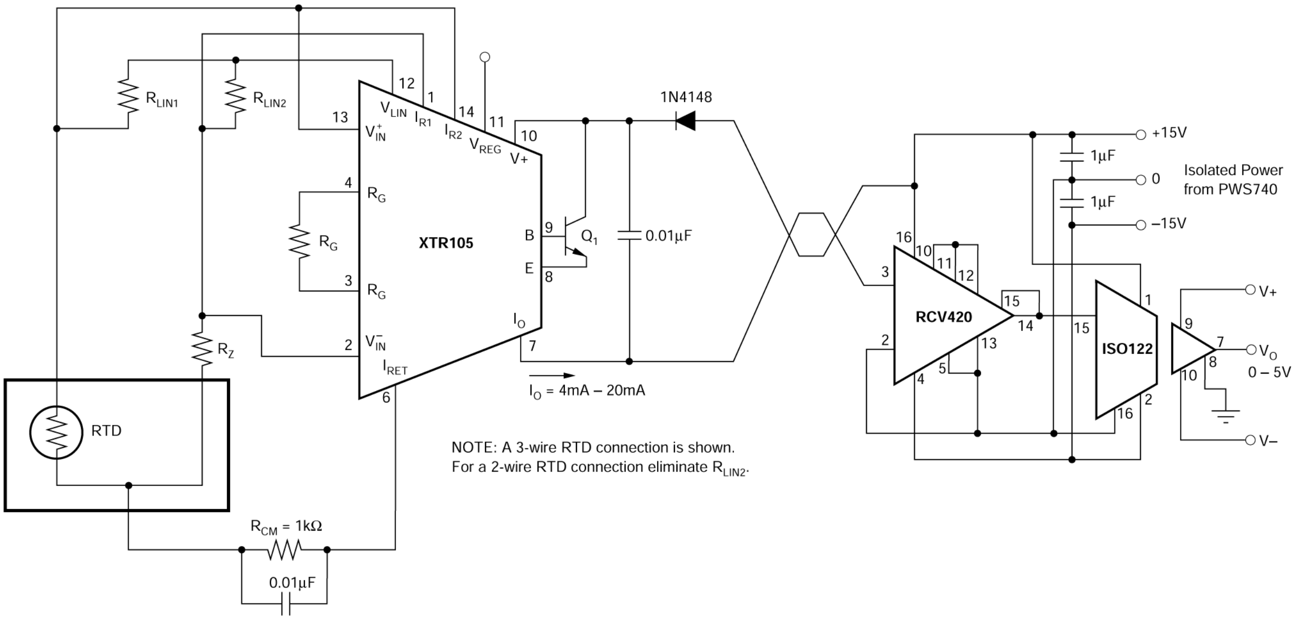
Table 7-2 shows how to calculate the effect of various error sources on the circuit accuracy. A sample error calculation for a typical RTD measurement circuit (Pt100 RTD, 200°C measurement span) is provided. The results reveal the XTR105 excellent accuracy, in this case 1.1% unadjusted. Adjusting resistors R_G and R_Z for gain and offset errors improves circuit accuracy to 0.32%. These are worst-case errors; maximum values were used in the calculations and all errors were assumed to be positive (additive). The XTR105 achieves performance that is difficult to obtain with discrete circuitry and requires less space.

Table 7-2. Error Calculation

SAMPLE ERROR CALCULATION				
RTD value at 4mA output ($R_{RTD\ MIN}$): 100Ω				
RTD measurement range: 200°C				
Ambient temperature range (ΔT_A): 20°C				
Supply voltage change (ΔV+): 5V				
Common-mode voltage change (ΔCM): 0.1V				
			ERROR (ppm of Full Scale)	
ERROR SOURCE	**ERROR EQUATION**	**SAMPLE ERROR CALCULATION(1)**	**UNADJ.**	**ADJUST.**
INPUT				
Input offset voltage	V_{OS} / ($V_{IN\ MAX}$) × 10^6	100µV / (800µA × 0.38Ω/°C × 200°C) × 10^6	1645	0
vs common-mode	CMRR · ΔCM/($V_{IN\ MAX}$) × 10^6	50µV/V × 0.1V / (800µA × 0.38Ω/°C × 200°C) × 10^6	82	82
Input bias current	I_B / I_{REF} × 10^6	0.025µA / 800µA × 10^6	31	0
Input offset current	I_{OS}× $R_{RTD\ MIN}$ / ($V_{IN\ MAX}$) × 10^6	3nA × 100Ω / (800µA × 0.38Ω/°C × 200°C) × 10^6	5	0
		Total Input Error:	**1763**	**82**
EXCITATION				
Current reference accuracy	I_{REF} accuracy (%) / 100% × 10^6	0.2% / 100% × 10^6	2000	0
vs supply	(I_{REF} vs V+) × ΔV+	25ppm/V × 5V	125	125
Current reference matching	I_{REF} matching (%) / 100% × 800µA × $R_{RTD\ MIN}$ / ($V_{IN\ MAX}$) × 10^6	0.1% / 100% × 800µA × 100Ω / (800µA × 0.38Ω/°C × 200°C) × 10^6	1316	0
vs supply	(I_{REF} matching vs V+) × ΔV+ × $R_{RTD\ MIN}$ / ($V_{IN\ MAX}$)	10ppm/V × 5V × 800µA × 100Ω / (800µA × 0.38Ω/°C × 200°C)	66	66
		Total Excitation Error:	**3507**	**191**
GAIN				
Span	Span error (%) / 100% × 10^6	0.2% / 100% × 10^6	2000	0
Nonlinearity	Nonlinearity (%) / 100% × 10^6	0.01% / 100% × 10^6	100	100
		Total Gain Error:	**2100**	**100**
OUTPUT				
Zero output	(I_{ZERO} – 4mA) / 16000µA × 10^6	25µA / 16000µA × 10^6	1563	0
vs supply	(I_{ZERO} vs V+) × ΔV+ / 16000µA × 10^6	0.2µA/V × 5V / 16000µA × 10^6	63	63
		Total Output Error:	**1626**	**63**
DRIFT (ΔT_A = 20°C)				
Input offset voltage	Drift × ΔT_A / ($V_{IN\ MAX}$) × 10^6	1.5µV/°C × 20°C / (800µA × 0.38Ω/°C × 200°C) × 10^6	493	493
Input bias current (typical)	Drift × ΔT_A / 800µA × 10^6	20pA/°C × 20°C / 800µA × 10^6	0.5	0.5
Input offset current (typical)	Drift × ΔT_A × $R_{RTD\ MIN}$ / ($V_{IN\ MAX}$) × 10^6	5pA/°C × 20°C × 100W / (800µA × 0.38Ω/°C × 200°C) × 10^6	0.2	0.2
Current reference accuracy	Drift · ΔT_A	35ppm/°C × 20°C	700	700
Current reference matching	Drift × ΔT_A × 800µA × $R_{RTD\ MIN}$ / ($V_{IN\ MAX}$)	15ppm/°C × 20°C × 800µA × 100Ω / (800µA × 0.38Ω/°C × 200°C)	395	395
Span	Drift × ΔT_A	25ppm/°C × 20°C	500	500
Zero output	Drift × ΔT_A / 16000µA × 10^6	0.5µA/°C × 20°C / 16000µA × 10^6	626	626
		Total Drift Error:	**2715**	**2715**
NOISE (0.1Hz to 10Hz, typical)				
Input offset voltage	v_n / ($V_{IN\ MAX}$) × 10^6	0.6µV / (800µA × 0.38Ω/°C × 200°C) × 10^6	10	10
Current reference	I_{REF} noise × $R_{RTD\ MIN}$ / ($V_{IN\ MAX}$) × 10^6	3nA × 100Ω / (800µA × 0.38Ω/°C × 200°C) × 10^6	5	5
Zero output	I_{ZERO} noise / 16000µA × 10^6	0.03µA / 16000µA × 10^6	2	2
		Total Noise Error:	**17**	**17**
		TOTAL ERROR:	**11728** **(1.17%)**	**3168** **(0.32%)**

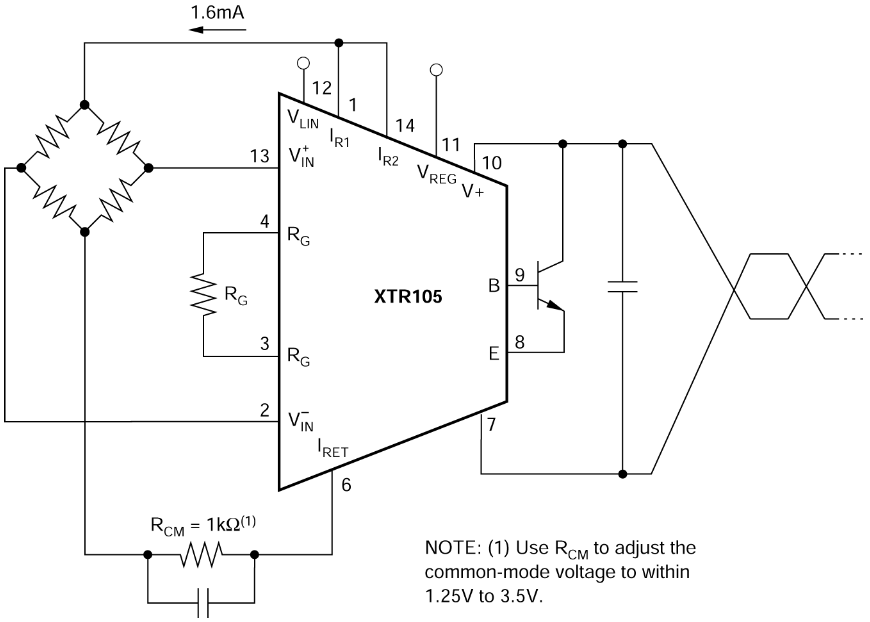
(1) All errors are minimum and maximum, and referred to input, unless otherwise stated.

7.2 Typical Applications



NOTE: A 3-wire RTD connection is shown.
For a 2-wire RTD connection eliminate R_{LIN2}.

Figure 7-5. Isolated Transmitter-Receiver Loop



NOTE: (1) Use R_{CM} to adjust the common-mode voltage to within 1.25V to 3.5V.

Figure 7-6. Bridge Input, Current Excitation

7.3 Layout

7.3.1 Layout Guidelines

The XTR105 is typically used with an external transistor (Q_1) to regulate the power dissipation of the 4-20mA loop. This allows the resulting localized self-heating to be distanced from the precision circuitry of the XTR105 and reduces over-temperature drift errors.

The XTR105 can be used without the Q_1 transistor if the application requirements do not lead to violation of the device *Absolute Maximum Requirements*, such as the maximum junction temperature. Calculate the peak power dissipation and multiply by thermal resistance to determine the associated junction temperature rise. Minimize overheat conditions for reliable long-term operation.

Place supply bypass capacitors close to the package and make connections with low-impedance conductors. Reduce trace lengths for R_G to minimize coupled environmental noise. If the loop power supply is electrically noisy, implement filtering using decoupling capacitors and small resistors or dampening inductors in series with V+.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Device Support

8.1.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

Part Number	Definition
XTR105UA/2K5	The die is manufactured in CSO:SHE or CSO:TID.
XTR105P XTR105PA XTR105U XTR105UA	The die is manufactured in CSO:SHE.

8.1.2 Related Documentation

For related documentation see the following:

- Texas Instruments, *Special Function Amplifiers* Precision Labs video series on Current Loop Transmitters
- Texas Instruments, *Analog Linearized 3-Wire PT100 RTD to 2-Wire 4-20mA Current Loop Transmitter reference design* with XTR105
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* technical article
- Texas Instruments, *A Basic Guide to RTD Measurements* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2024) to Revision D (December 2025)	**Page**
• Updated end equipment links in *Applications*	1
• Added description of device flow information in *Specifications*	4
• Added all chip site origin (CSO) to typical test conditions in *Electrical Characteristics*	5
• Added additional fabrication process specification for Input Bias Current and Input Bias Current vs temperature in *Electrical Characteristics* table	5
• Added additional fabrication process specification for Input Offset Current vs temperature in *Electrical Characteristics* table	5
• Added additional fabrication process specification for Offset Voltage and Offset Voltage vs temperature in *Electrical Characteristics* table	5
• Added additional fabrication process specification for Current Source Accuracy vs Power Supply, V+ in *Electrical Characteristics* table	5
• Added all chip site origin (CSO) to typical test conditions in *Typical Characteristics*	7
• Added additional fabrication process curve for Step Response, Input Bias and Offset Current vs Temperature, and Input Offset Voltage Drift in *Typical Characteristics*	7
• Updated Overscale Current vs Temperature, Underscale Current vs Temperature, Zero Output Current Error vs Temperature, V_{REG} Output Voltage vs V_{REG} Output Current, and Reference Current Error vs Temperature to align with absolute maximum temperature rating in *Typical Characteristics*	7
• Added part number fabrication process information table in *Device Support*	25

Changes from Revision B (August 2004) to Revision C (October 2024)	**Page**
• Added the *Pin Configuration and Functions*, *Specifications*, *ESD Ratings*, *Recommended Operating Conditions*, *Thermal Information*, *Detailed Description*, *Overview*, *Functional Block Diagram*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Typical Applications*, *Layout*, *Layout Guidelines*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Added end equipments in *Applications*	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Pin Functions* table	3
• Moved operating and storage temperature parameters from *Electrical Characteristics* to *Absolute Maximum Ratings*	4
• Changed minimum operating temperature from −55°C to −40°C in *Absolute Maximum Ratings*	4
• Moved specified temperature and power-supply parameters from *Electrical Characteristics* to *Recommended Operating Conditions*	4
• Deleted thermal resistance, θ_{JA} parameters in *Electrical Characteristics* and replaced with detailed thermal model parameters in *Thermal Information*	4
• Updated formatting of *Electrical Characteristics* table	5
• Changed Voltage accuracy vs temperature typical specification from ±0.2mV/°C to ±0.5mV/°C in *Electrical Characteristics*	5
• Updated Figure 5-2, *Step Response*	7
• Updated Figure 5-8, *Zero Output and Reference Current Noise vs Frequency*	7
• Changed description of maximum loop-supply voltage to specified absolute maximum rating in *Surge Protection*	15
• Updated suggested Zener diode part numbers in Figure 6-4, *Reverse Voltage Operation and Overvoltage Surge Protection*	15
• Updated suggested transistor part numbers in Figure 7-1, *Basic 2-Wire RTD Temperature Measurement Circuit with Linearization*	16

- Moved *Adjusting Initial Errors* into *Error Analysis* section 21

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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