INA117 High Common-Mode Voltage Difference Amplifier

1 Features

- Common-mode input range: ±200V (V_S = ±15V)
- Protected inputs:
  - ±500V Common-mode
  - ±500V Differential
- Unity gain: 0.05% gain error maximum
- Nonlinearity: 0.001% maximum
- CMRR: 70dB minimum

2 Applications

- Single multi axis servo drives
- Industrial machine and machine tools
- Semiconductor test and ATE
- Ultrasound scanner

3 Description

The INA117 is a precision unity-gain difference amplifier with very high common-mode input voltage range. The INA117 is a single monolithic IC consisting of a precision op amp and integrated thin-film resistor network. The device can accurately measure small differential voltages in the presence of common-mode signals up to ±200V. The INA117 inputs are protected from momentary common-mode or differential overloads up to ±500V.

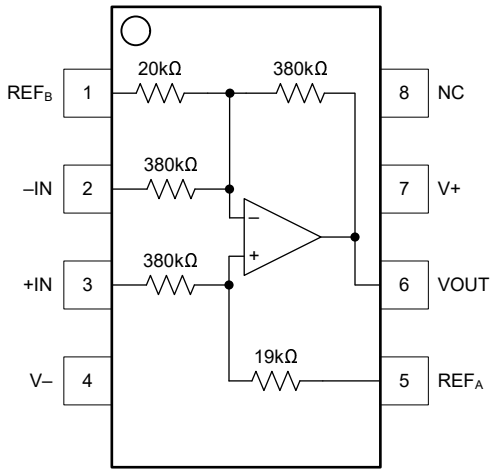
In many applications, where galvanic isolation is not essential, the INA117 can replace isolation amplifiers. This design can eliminate costly isolated input-side power supplies and the associated ripple, noise, and quiescent current. The INA117 offers low nonlinearity of 0.001% and a wide bandwidth of 200kHz (CSO: SHE) or 500kHz (CSO: TID) (see specification note in Section 5).

The INA117 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –40°C to 85°C temperature range.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA117P	P (DIP, 8)	6.35mm × 9.81mm
INA117KU	D (SOIC, 8)	3.91mm × 4.9mm
INA117KU/2K5		

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



INA117 D Package Top View

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4 Pin Configuration and Functions

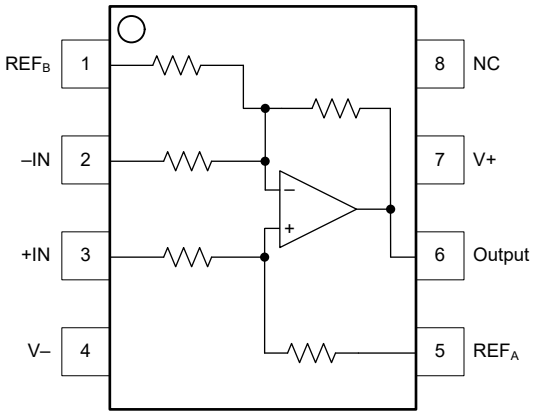


Figure 4-1. DIP/SO
INA117P, KU
Top View

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
-In	2	I	Inverting input.
+In	3	I	Non-inverting input.
NC	8	_	No internal connection. Can be grounded or disconnected.
Output	6	O	Output of the amplifier.
Ref_A	5	I	Reference A.
Ref_B	1	I	Reference B.
V-	4	P	Negative power supply.
V+	7	P	Positive power supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 8.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S		Dual supply, V_S = (V+) – (V–)		±22	V
	Signal input pins	Continuous		±200	V
		Peak (0.1s)		±500	V
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–40	85	°C
T_{stg}	Storage temperature		–55	125	°C
	Junction temperature			150	°C
	Lead temperature (soldering, 10s)			300	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	10	30	36	V
		Dual-supply	±5	±15	±18	
T_A	Specified temperature		–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA117 D (SOIC) 8 PINS	INA117 P (PDIP) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	150	80	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ, V_{REF} = 0V, V_{CM} = V_S/2, and G = 1, all chips site origins (CSO) (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage	RTO (P package)	CSO: SHE			120	1000	µV
			CSO: TID			350	1000	
		RTO (KU package)	CSO: SHE			600	2000	
			CSO: TID			350	2000	
	Offset voltage drift	RTO, T_A = –40°C to 85°C	CSO: SHE			8.5		µV/°C
			CSO: TID			3		
	Long term drift					200		µV/mo
PSRR	Power-supply rejection ratio	RTO, V_S = ±5V to ±18V			74	90		dB
	Common-mode voltage (1)				–200		200	V
	Differential voltage				–10		10	V
CMRR	Common-mode voltage rejection	DC, V_{CM} = –200V to 200V	CSO: SHE		70	80		dB
				T_A = –40°C to 85°C		75		
			CSO: TID		70	100		
				T_A = –40°C to 85°C	70			
		AC, V_{CM} = –200V to 200V	CSO: SHE	60 Hz	66	80		
			CSO: TID	500 Hz	90			
				1 kHz		90		
	Differential input impedance					800		kΩ
	Common-mode input impedance	CSO: SHE				400		kΩ
		CSO: TID				200		kΩ
NOISE								
e_N	Voltage noise	RTO, f_B = 0.1Hz to 10Hz				25		$µV_{PP}$
		RTO, f = 1kHz				550		$nV/\sqrt{Hz}$
GAIN								
GE	Gain error					±0.01	±0.05	%
	Gain error drift	T_A = –40°C to 85°C				±2		ppm/°C
	Gain nonlinearity(2)	CSO: SHE				±0.0002	±0.001	% of FSR
		CSO: TID				±0.0005	±0.001	
OUTPUT								
	Output voltage	I_O = 20mA, –5mA	CSO: SHE		10	12		V
		I_O = ±6.75mA	CSO: TID		13.5	13.7		
	Output impedance					0.01		Ω
C_L	Load capacitance	Stable operation	CSO: SHE			1		nF
			CSO: TID			10		
	Short-circuit current	Continuous to V_S/2	CSO: SHE			49, –13		mA
			CSO: TID			16, –25		

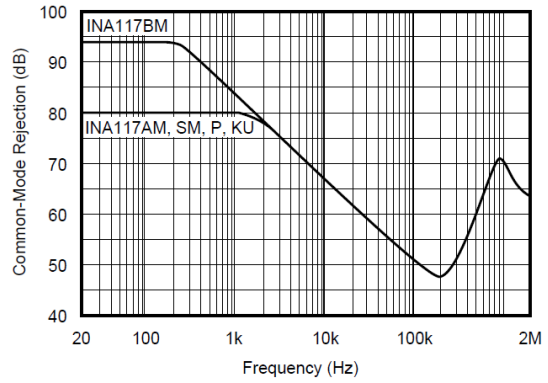
at T_A = 25°C, V_S = ±15V, R_L = 10kΩ, V_{REF} = 0V, V_{CM} = V_S/2, and G = 1, all chips site origins (CSO) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	CSO: SHE			200		kHz
		CSO: TID			500		
	Full power bandwidth	V_O = 20V_{pp}	CSO: SHE	30			kHz
		V_O = 2V_{pp}	CSO: TID		32		
SR	Slew rate	CSO: SHE		1.7	2.6		V/µs
		CSO: TID		1.7	5		
t_S	Settling time	To 0.1%,	V_O = 10V step		6.5		µs
		To 0.01%	V_O = 10V step		10		
			V_{CM} = 10V step, V_{DIFF} = 0V		4.5		
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0V	CSO: SHE		1.5	±2	mA
			CSO: TID		0.8	±2	

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

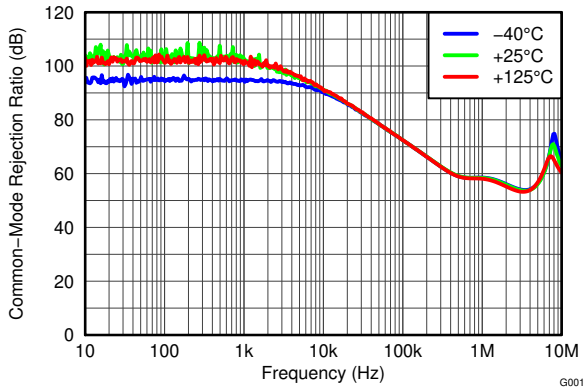
6 Typical Characteristics

at T_A = 25°C, V_S = ±15V, all chips site origins (CSO) (unless otherwise noted)



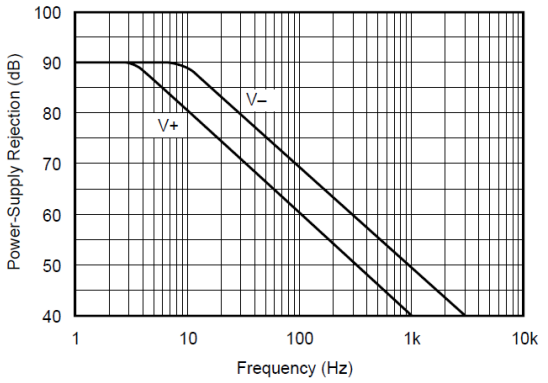
CSO: SHE

Figure 6-1. Common-mode Rejection vs Frequency



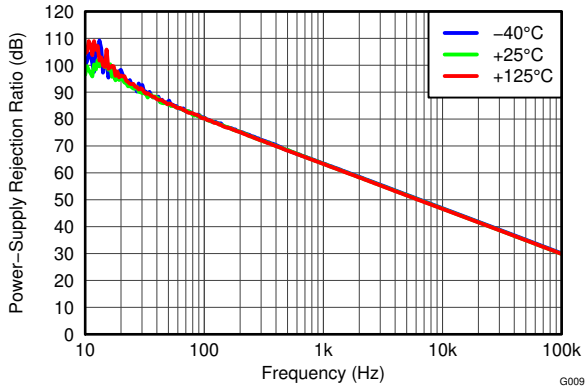
CSO: TID R_L = 2kΩ connected to ground

Figure 6-2. Common-mode Rejection vs Frequency



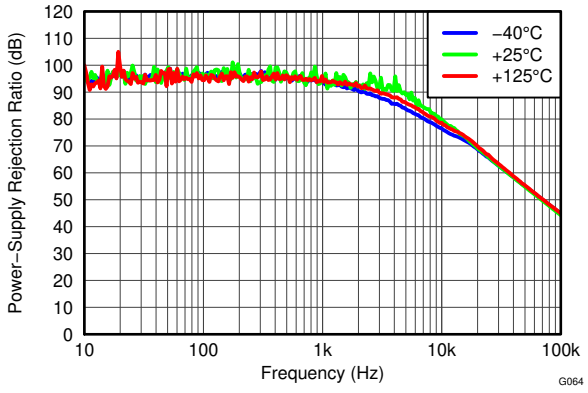
CSO: SHE

Figure 6-3. Power-supply Rejection vs Frequency



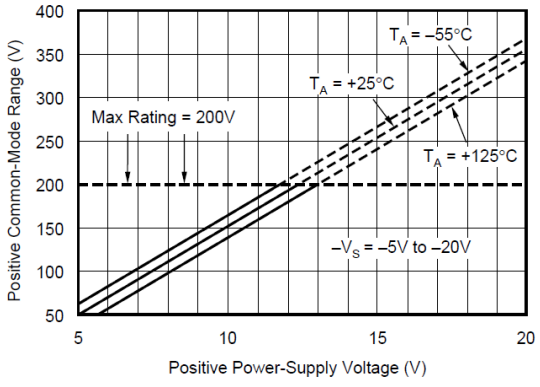
CSO: TID R_L = 2kΩ connected to ground

Figure 6-4. Positive Power-supply Rejection vs Frequency



CSO: TID R_L = 2kΩ connected to ground

Figure 6-5. Negative Power-supply Rejection vs Frequency

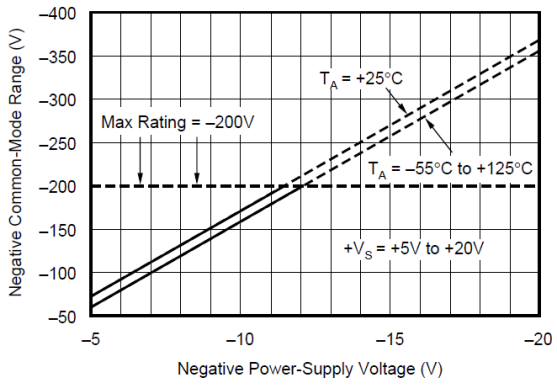


CSO: SHE

Figure 6-6. Positive Common-mode Voltage Range vs Positive Power-supply Voltage

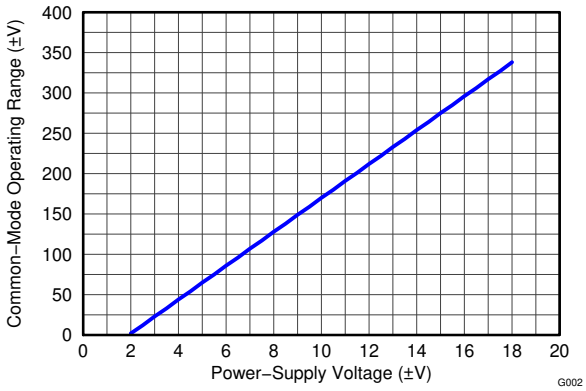
6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, all chips site origins (CSO) (unless otherwise noted)



CSO: SHE

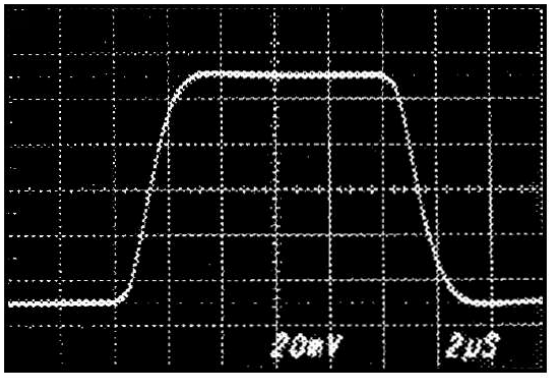
Figure 6-7. Negative Common-mode Voltage Range vs Negative Power-supply Voltage



CSO: TID

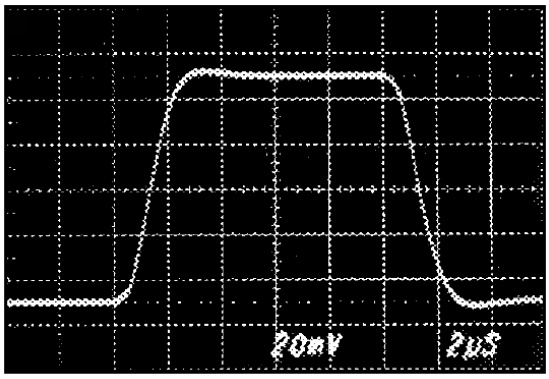
R_L = 2kΩ connected to ground

Figure 6-8. Common-mode Voltage Range vs Power-supply Voltage



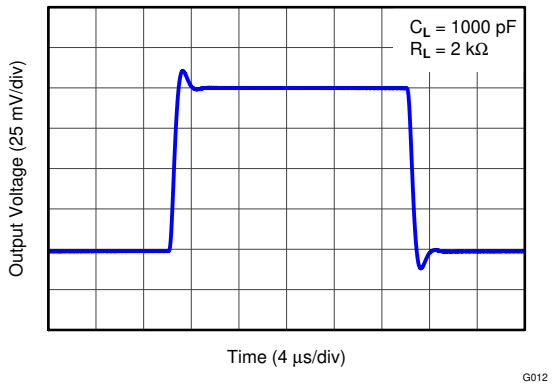
CSO: SHE

Figure 6-9. Small Signal Step Response C_L = 0pF



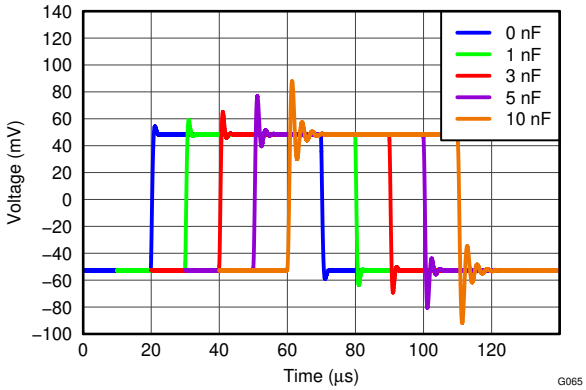
CSO: SHE

Figure 6-10. Small Signal Step Response C_L = 1000pF



CSO: TID

Figure 6-11. Small Signal Step Response



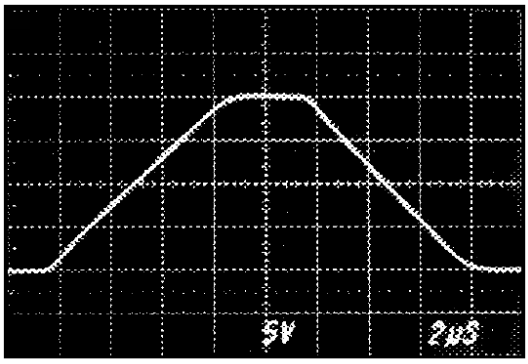
CSO: TID

R_L = 2kΩ connected to ground

Figure 6-12. Small Signal Step Response vs Capacitive Load

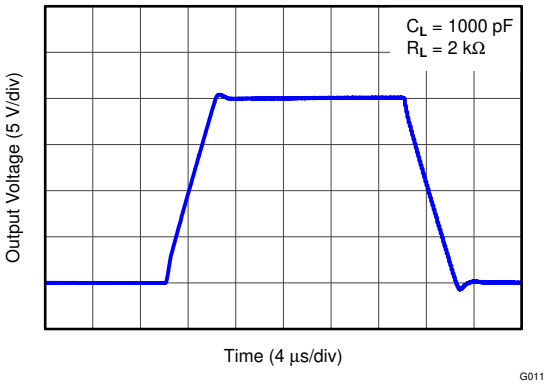
6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, all chips site origins (CSO) (unless otherwise noted)



CSO: SHE

Figure 6-13. Large Signal Step Response



CSO: TID

Figure 6-14. Large Signal Step Response

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Figure 7-1 shows the basic connections required for operation.

Applications with noisy or high-impedance power-supply lines can require decoupling capacitors close to the device pins.

The output voltage is equal to the differential input voltage between pins 2 and 3. The common mode input voltage is rejected.

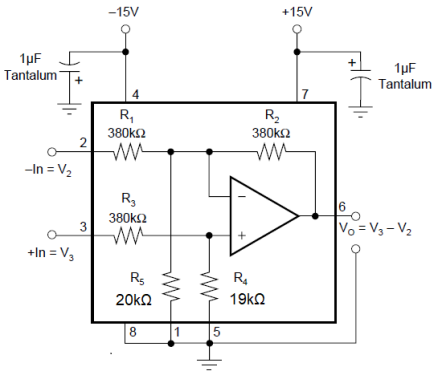


Figure 7-1. Basic Power and Signal Connections

7.1.1 Common-mode Rejection

Common-mode rejection (CMR) of the INA117 is dependent on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, having low source impedances is important for driving the two inputs. A 75Ω resistance in series with pin 2 or 3 decreases CMR from 86dB to 72dB.

Resistance in series with the reference pins also degrades CMR. A 4Ω resistance in series with pin 1 or 5 decreases CMRR from 86dB to 72dB.

Most applications do not require trimming. Figure 7-2 and Figure 7-3 show optional circuits that can be used for trimming offset voltage and common-mode rejection.

7.1.2 Transfer Function

Most applications use the INA117 as a simple unity-gain difference amplifier. The transfer function is:

$V_0 = V_3 – V_2$

V_3 and V_2 are the voltages at pins 3 and 2.

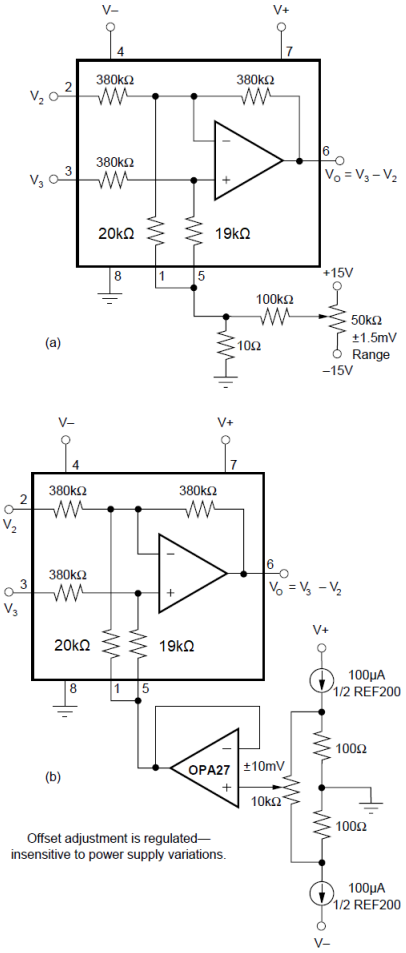


Figure 7-2. Offset Voltage Trim Circuits

Some applications, however, apply voltages to the reference terminals (pins 1 and 5). A more complete transfer function is:

$V_0 = V_3 – V_2 + 20 \times V_5 – 19 \times V_1$

V_5 and V_1 are the voltages at pins 5 and 1.

7.1.3 Measuring Current

The INA117 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 7-4 shows the INA117 used to measure the supply currents of a device under test. The circuit in Figure 7-5 measures the output current of a power supply. If the power supply has a sense connection, the power supply can be connected to the output side of R_S to eliminate the voltage-drop error. Another common application is current-to-voltage conversion, as shown in Figure 7-6.

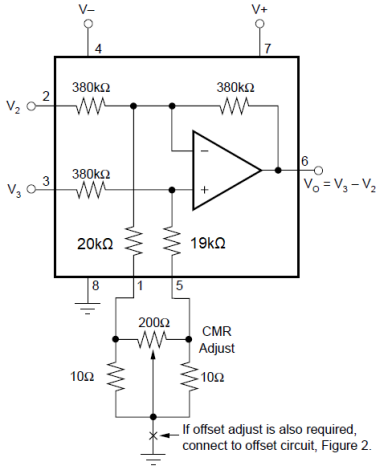


Figure 7-3. CMR Trim Circuit

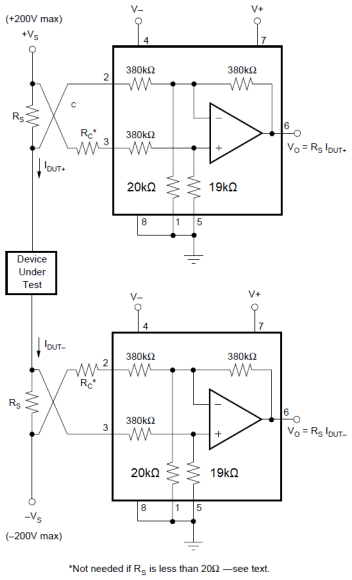
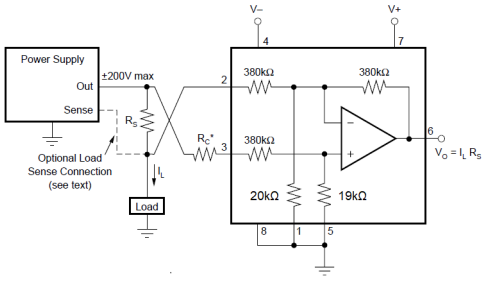


Figure 7-4. Measuring Supply Currents of Device Under Test



*R_C not needed if R_S is less than 20Ω – see text.

Figure 7-5. Measuring Power Supply Output Current

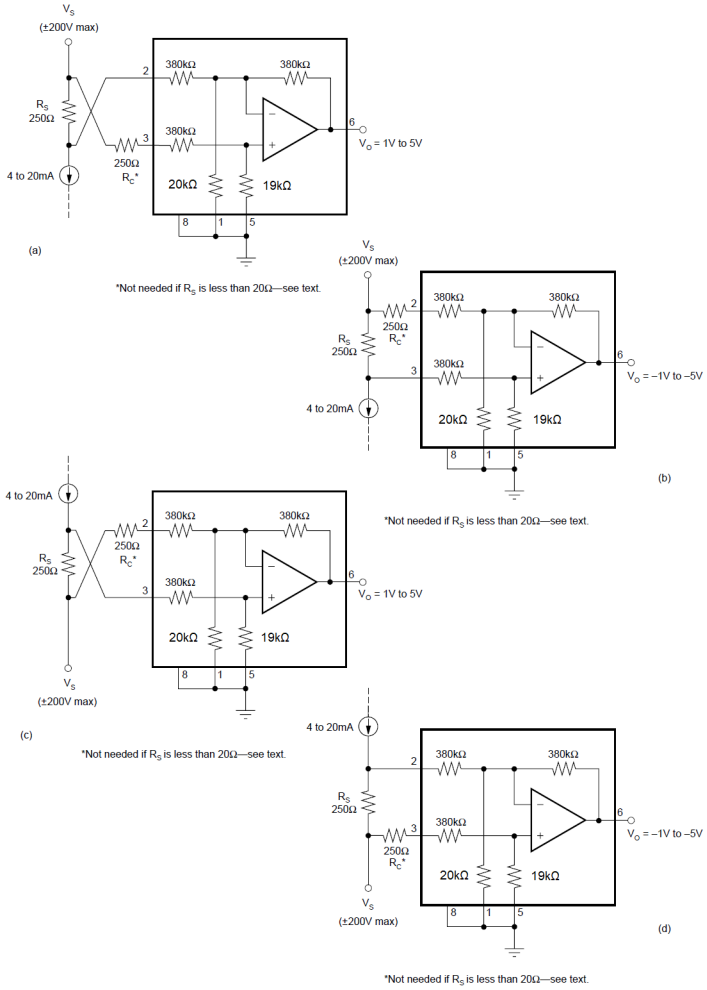


Figure 7-6. Current to Voltage Converter

In all cases, the sense resistor imbalances the input resistor matching of the INA117, degrading the CMR. Also, the input impedance of the INA117 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor, R_C, equal in value to R_S as shown in Figure 7-4, Figure 7-5, and Figure 7-6. If R_S is less than 20Ω, the degradation in CMR is negligible and R_C can be omitted. If R_S is larger than approximately 2kΩ, trimming R_C can be required to achieve greater than 86dB CMR. This trim is because the actual INA117 input impedances have 1% typical mismatch. If R_S is more than approximately 100Ω, the gain error is greater than the 0.05% specification of the INA117. This gain error can be corrected by slightly increasing the value of R_S. The corrected value, R_S', can be calculated by:

$$R_S' = \frac{R_S \times 380k\Omega}{380k\Omega - R_S} \quad (1)$$

Example: For a 1V/mA transfer function, the nominal, uncorrected value for R_S is 1kΩ. A slightly larger value, R_S' = 1002.6Ω, compensates for the gain error due to loading.

The 380kΩ term in the equation for R_S' has a tolerance of ±25%, so sense resistors above approximately 400Ω can require trimming to achieve gain accuracy better than 0.05%.

Of course, if a buffer amplifier is added as shown in Figure 7-7, both inputs see a low source impedance, and the sense resistor is not loaded. As a result, there is no gain error or CMR degradation. The buffer amplifier

can operate as a unity gain buffer or as an amplifier with non-inverting gain. Gain added ahead of the INA117 improves both CMR and signal-to-noise. Added gain also allows a lower voltage drop across the sense resistor. The OPA1013 is a good choice for the buffer amplifier since both the input and output can swing close to the negative power supply.

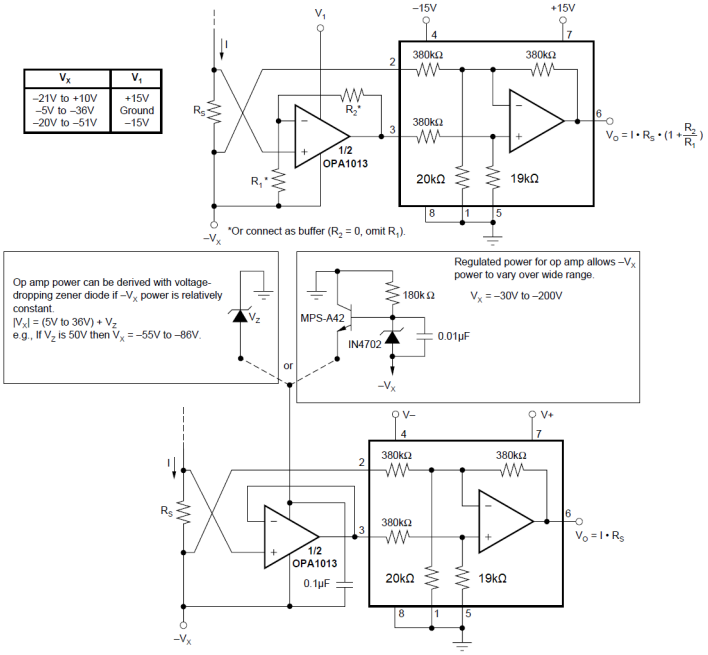


Figure 7-7. Current Sensing With Input Buffer

Figure 7-8 shows very high input impedance buffer used to measure low leakage currents. Here, the buffer operational amplifier is powered with an isolated, split-voltage power supply. Using an isolated power supply allows full ±200V common-mode input range.

7.1.4 Noise Performance

The noise performance of the INA117 is dominated by the internal resistor network. The thermal or Johnson noise of these resistors produces approximately 550nV/√Hz noise. The internal op amp contributes virtually no excess noise at frequencies above 100Hz.

Many applications can be satisfied with less than the full 200kHz bandwidth of the INA117. In these cases, the noise can be reduced with a low-pass filter on the output. The two- pole filter shown in Figure 7-9 limits bandwidth to 1kHz and reduces noise by more than 15:1. Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, a cutoff frequency below 100Hz does not further reduce noise.

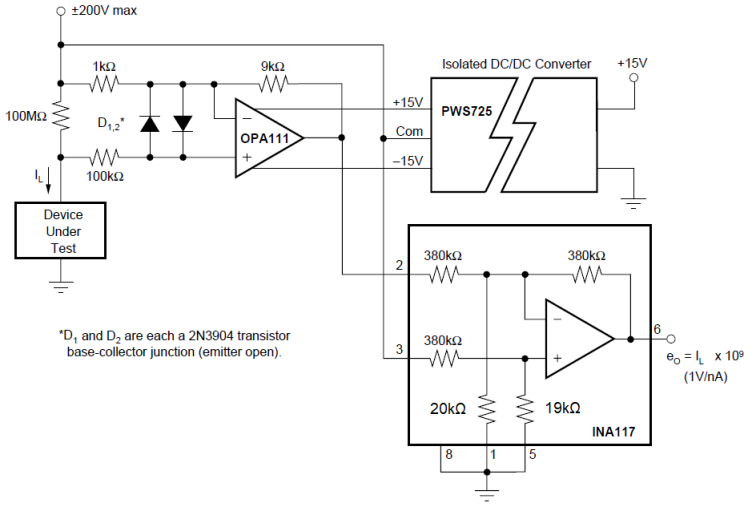
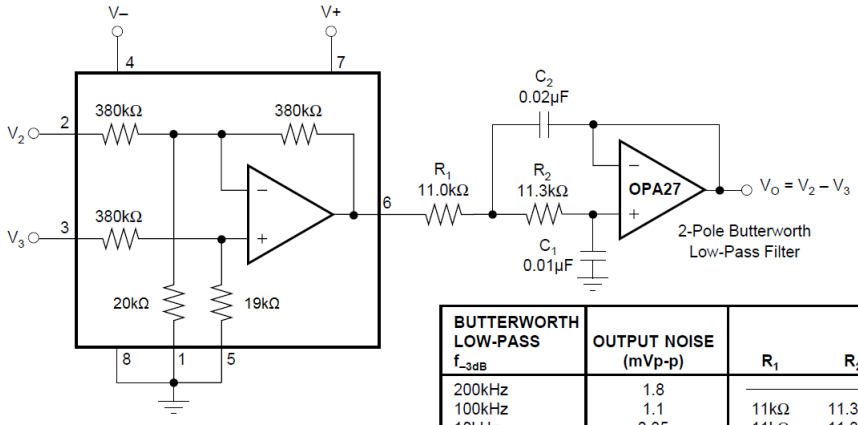


Figure 7-8. Leakage Current Measurement Circuit



BUTTERWORTH LOW-PASS f_{-3dB}	OUTPUT NOISE (mVp-p)	R_1	R_2	C_1	C_2
200kHz	1.8	No Filter			
100kHz	1.1	11kΩ	11.3kΩ	100pF	200pF
10kHz	0.35	11kΩ	11.3kΩ	1nF	2nF
1kHz	0.11	11kΩ	11.3kΩ	10nF	20nF
≤100Hz(1)	0.05	11kΩ	11.3kΩ	0.1µF	0.2µF

See Application Bulletin AB-017 for other filters.

NOTE: (1) Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, bandwidth reduction below this frequency will not significantly reduce noise.

Figure 7-9. Output Filter for Noise Reduction

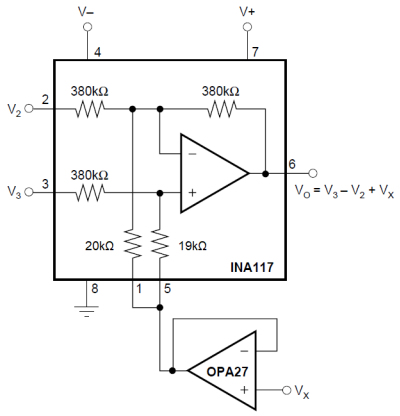


Figure 7-10. Summing V_X in Output

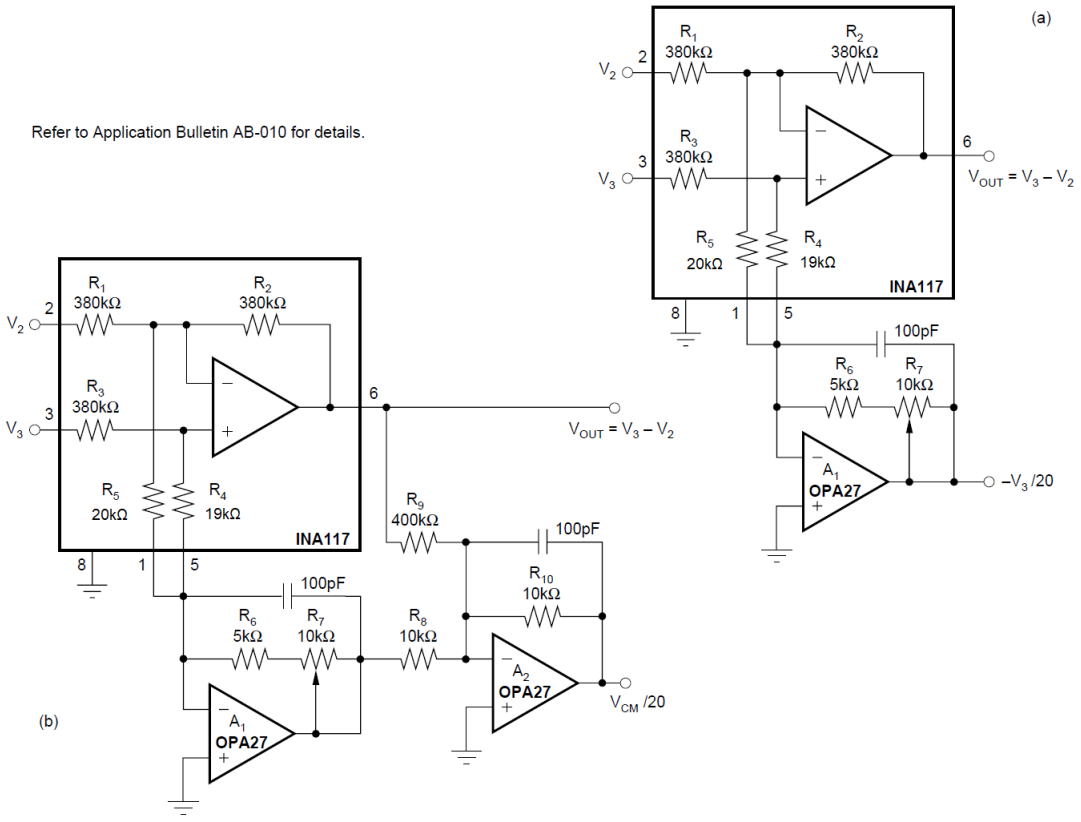


Figure 7-11. Common-mode Voltage Monitoring

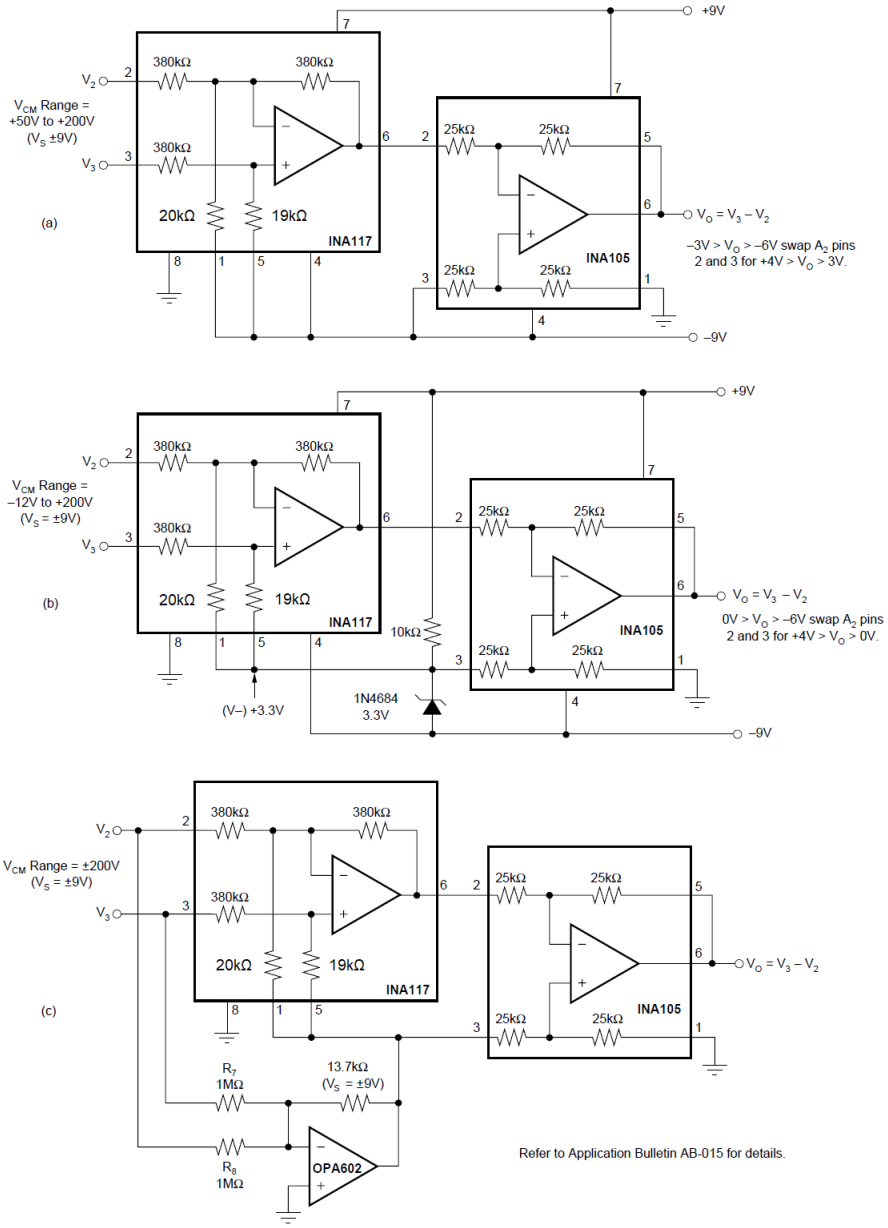


Figure 7-12. Offsetting or Boosting Common-mode Voltage Range for Reduced Power-supply Voltage Operation

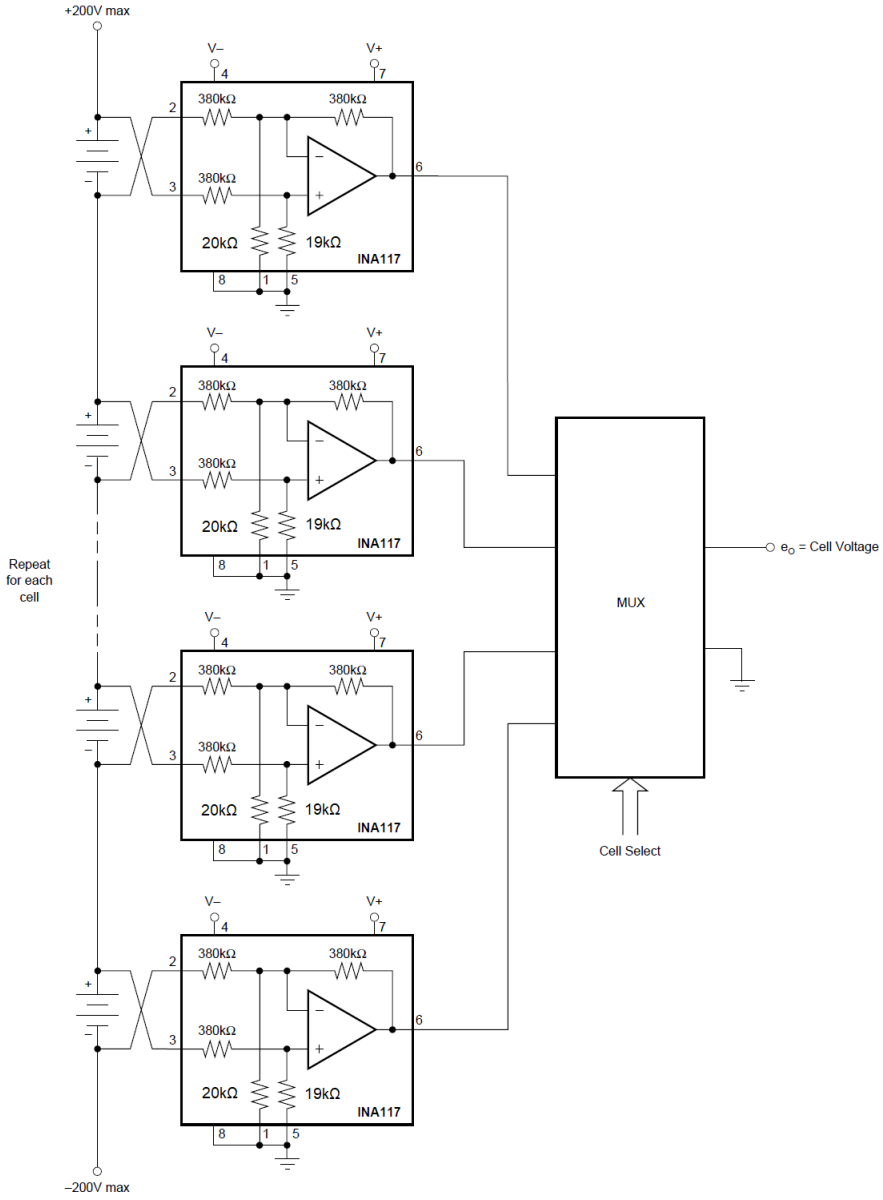


Figure 7-13. Battery Cell Voltage Monitor

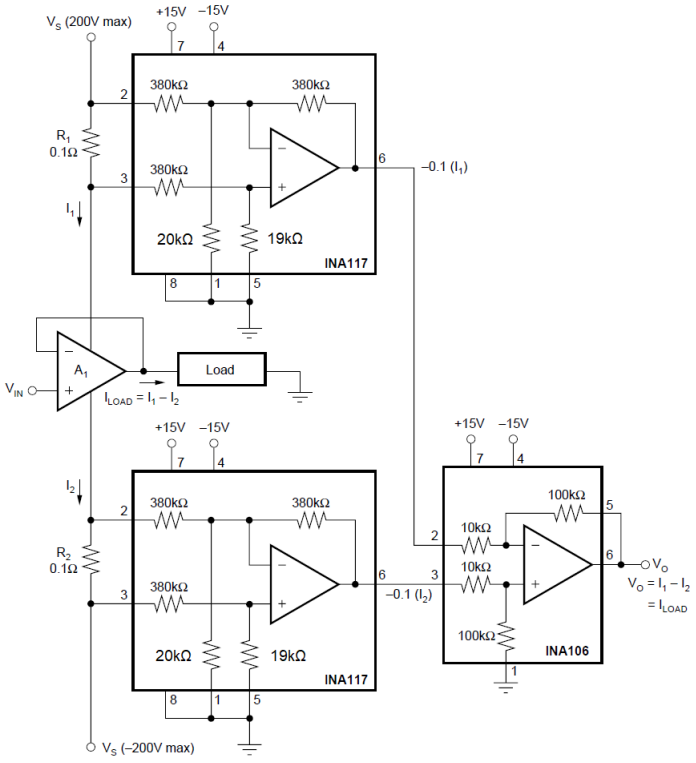


Figure 7-14. Measuring Amplifier Load Current

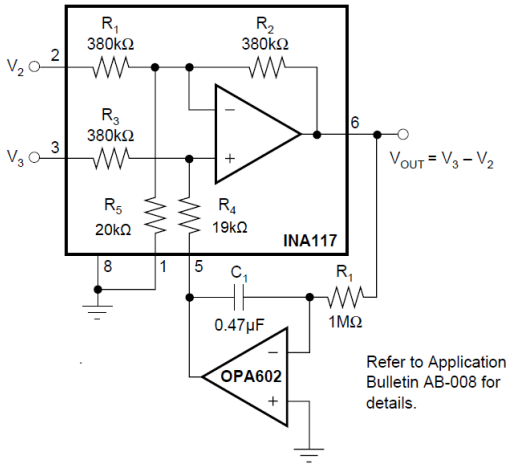


Figure 7-15. AC-coupled INA117

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Nomenclature

Table 8-1. Device Nomenclature

Part Number	Definition
INA117KU INA117KU/2K5 INA117P	The die is manufactured in CSO: SHE or CSO: TID.
INA117AM INA117BM INA117SM INA117SMQ	The die is manufactured in CSO: SHE.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *Precision labs series: Instrumentation amplifier*, videos
- Texas Instruments, *INA149 High common mode voltage difference amplifier*, data sheet
- Texas Instruments, *Supporting High Voltage Common Mode Using Difference Amplifier*, application brief

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2024) to Revision C (January 2026) **Page**

- Added different fabrication process specifications for Bandwidth, –3dB to the *Description* section....1
- Added description of device flow information in the *Specifications* 3
- Added different fabrication process specifications for Offset voltage in the *Electrical Characteristics* 4
- Added all chips site origins (CSO) condition to the typical test conditions in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Offset voltage drift in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Common-mode voltage rejection in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Common-mode input impedance in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Gain nonlinearity in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Output voltage in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Load capacitance in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Short-circuit current in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Bandwidth, -3dB in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Full power bandwidth in the *Electrical Characteristics* ..4
- Added different fabrication process specifications for Slew rate in the *Electrical Characteristics* 4
- Added different fabrication process specifications for Quiescent current in the *Electrical Characteristics* 4
- Added typical test conditions in the *Typical Characteristics* 6
- Added all *chips site origins (CSO)* condition to the typical test conditions in the *Typical Characteristics* 6
- Added CSO: SHE to *Common-mode Rejection vs Frequency*, *Power-supply Rejection vs Frequency*, *Positive Common-mode Voltage Range vs Positive Power-supply Voltage*, *Negative Common-mode Voltage Range vs Negative Power-supply Voltage*, *Small Signal Step Response*, and*Large Signal Step Response* curves in the *Typical Characteristics* 6
- Added *Common-mode Rejection vs Frequency*, *Positive Power-supply Rejection vs Frequency*, *Negative Power-supply Rejection vs Frequency*, *Common-mode Voltage Range vs Power-supply Voltage*, *Small Signal Step Response*, *Small Signal Step Response vs Capacitive Load*, and *Large Signal Step Response* curves for CSO: TID in the *Typical Characteristics* 6
- Added Part Number flow information table to the *Device Nomenclature* 19

Changes from Revision A (November 2000) to Revision B (April 2024) **Page**

- Updated the formatting for tables, figures, and cross-references throughout the document....1
- Deleted information about the INA117AM and INA117SM variants throughout this document....1
- Changed pin 8 from "Comp" to "NC" in the *Description* and *Pin Configuration and Functions* sections....1
- Added *Package Information* table to the *Description* section....1
- Added *Pin Functions* table....2
- Added ESD Ratings table....3
- Added single supply specification to *Recommended Operating Conditions* 3
- Added specified temperature range to *Recommended Operating Conditions* 3
- Added VREF = 0V, VCM = VS/2, and G = 1 to "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity....4
- Changed parameter from "Offset voltage vs Temperature" to "Offset voltage drift" in *Electrical Characteristics* 4
- Added test condition of "TA = –40°C to +85°C" for "Offset voltage drift" in *Electrical Characteristics* 4
- Changed parameter from "Offset Voltage vs Power Supply" to "Power-supply rejection ratio" in *Electrical Characteristics* 4
- Added test condition of "TA = –40°C to +85°C" for "CMRR" in *Electrical Characteristics* 4

- Changed "Common-mode input impedance" typical value from 400kΩ to 200kΩ in *Electrical Characteristics* 4
- Added test condition "TA = –40°C to +85°C" for "Gain error vs temperature" in *Electrical Characteristics* and renamed to "Gain error drift" for clarity....4
- Changed "Gain nonlinearity" typical value from 0.0002% to 0.0005% in *Electrical Characteristics* 4
- Added test condition "Continuous to V_S/2" to Short-circuit current specification in *Electrical Characteristics* for clarity....4
- Change minimum Slew rate from 2V/µs to 1.7V/µs in *Electrical Characteristics* 4
- Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics* 4
- Deleted *Reducing Differential Gain* application circuit figure 13
- Added *Documentation Support* and *Related Documentation* sections....19

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA117AM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	INA117AM
INA117AM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	INA117AM
INA117BM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	INA117BM
INA117BM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	INA117BM
INA117KU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 117KU
INA117KU.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 117KU
INA117KU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 117KU
INA117KU/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 117KU
INA117P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	Call TI | Nipdau	N/A for Pkg Type	-40 to 85	INA117P
INA117P.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA117P
INA117SM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-40 to 85	INA117SM
INA117SM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-40 to 85	INA117SM
INA117SMQ	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-40 to 85	INA117SMQ
INA117SMQ.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-40 to 85	INA117SMQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

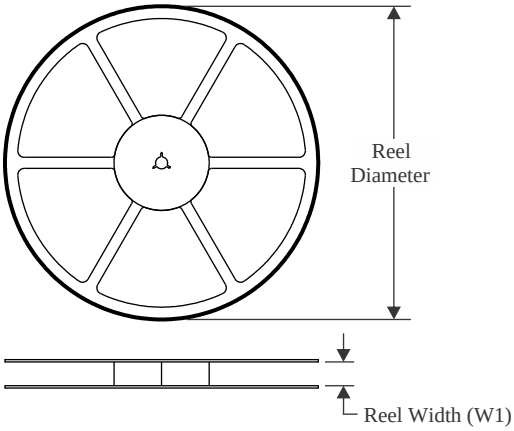
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

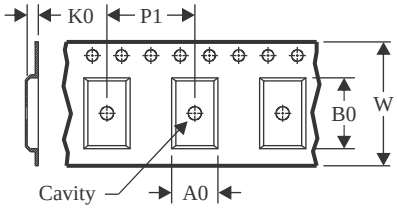
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

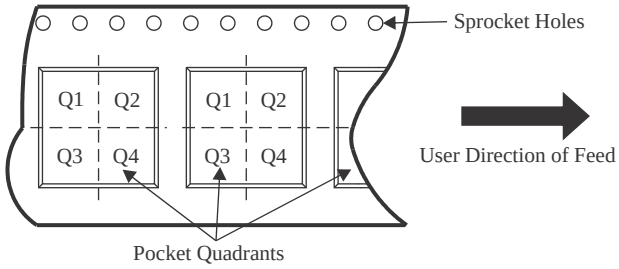


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

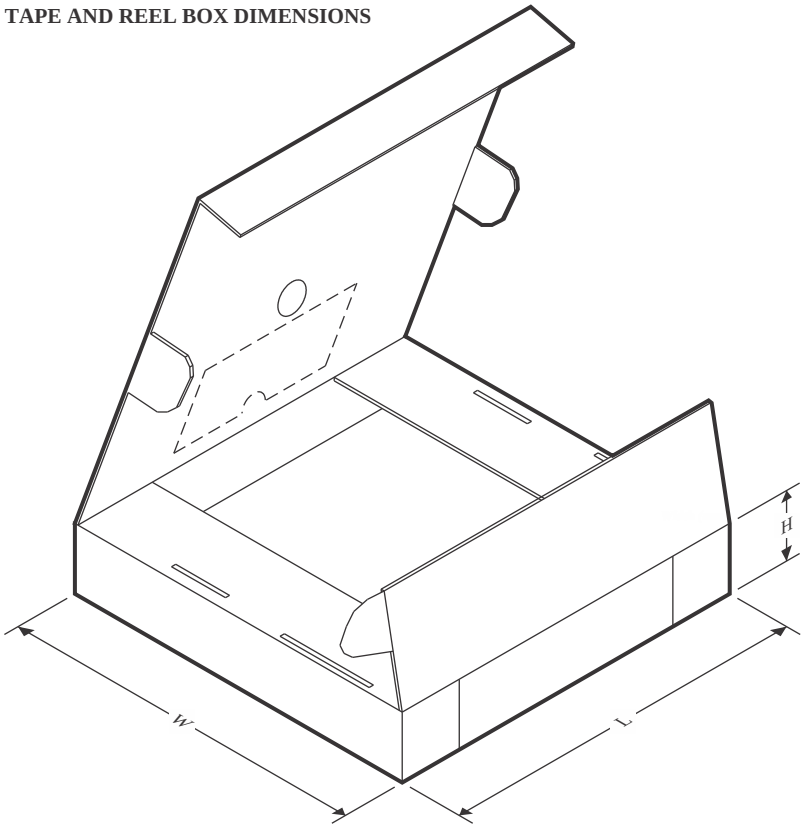
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA117KU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

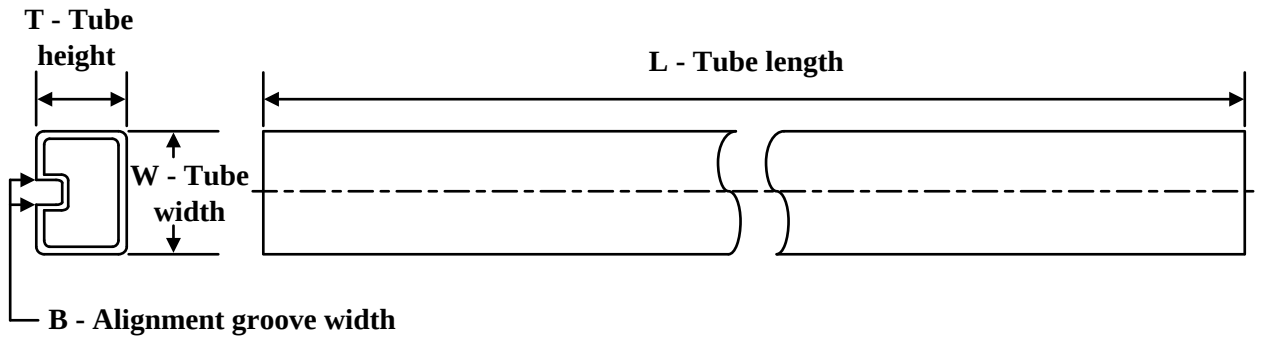
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA117KU/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

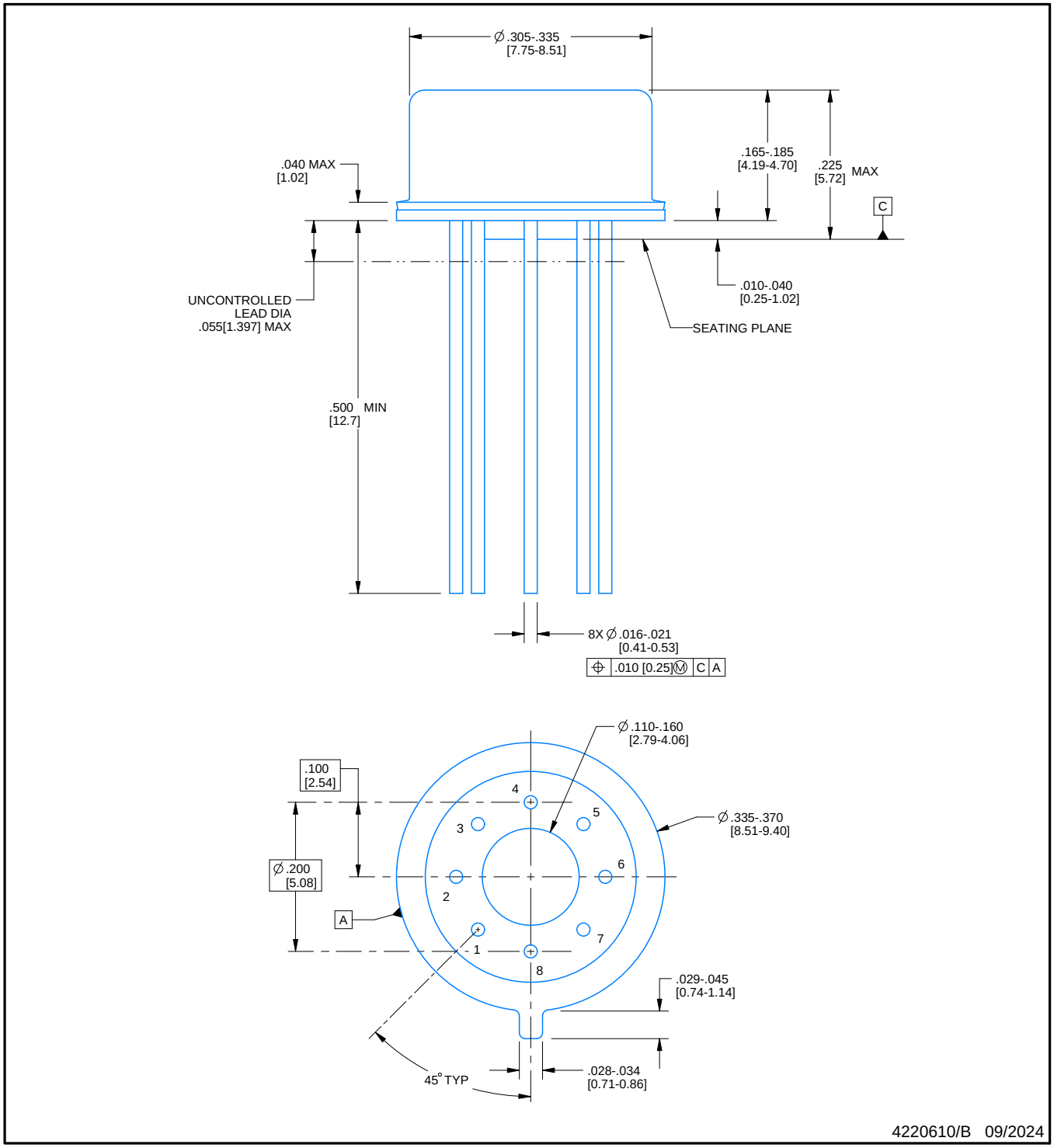
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA117AM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117AM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117BM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117BM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117KU	D	SOIC	8	75	506.6	8	3940	4.32
INA117KU.B	D	SOIC	8	75	506.6	8	3940	4.32
INA117P	P	PDIP	8	50	506	13.97	11230	4.32
INA117P.B	P	PDIP	8	50	506	13.97	11230	4.32
INA117SM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117SM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117SMQ	LMC	TO-CAN	8	20	532.13	21.59	889	NA
INA117SMQ.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA

PACKAGE OUTLINE

LMC0008A

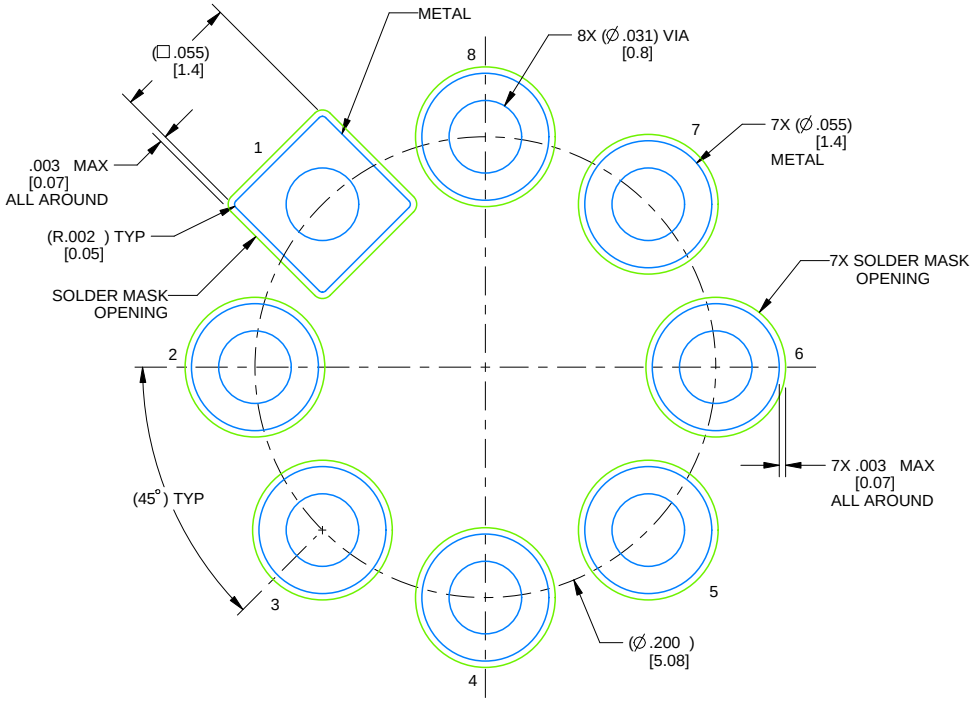
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



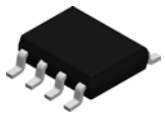
NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

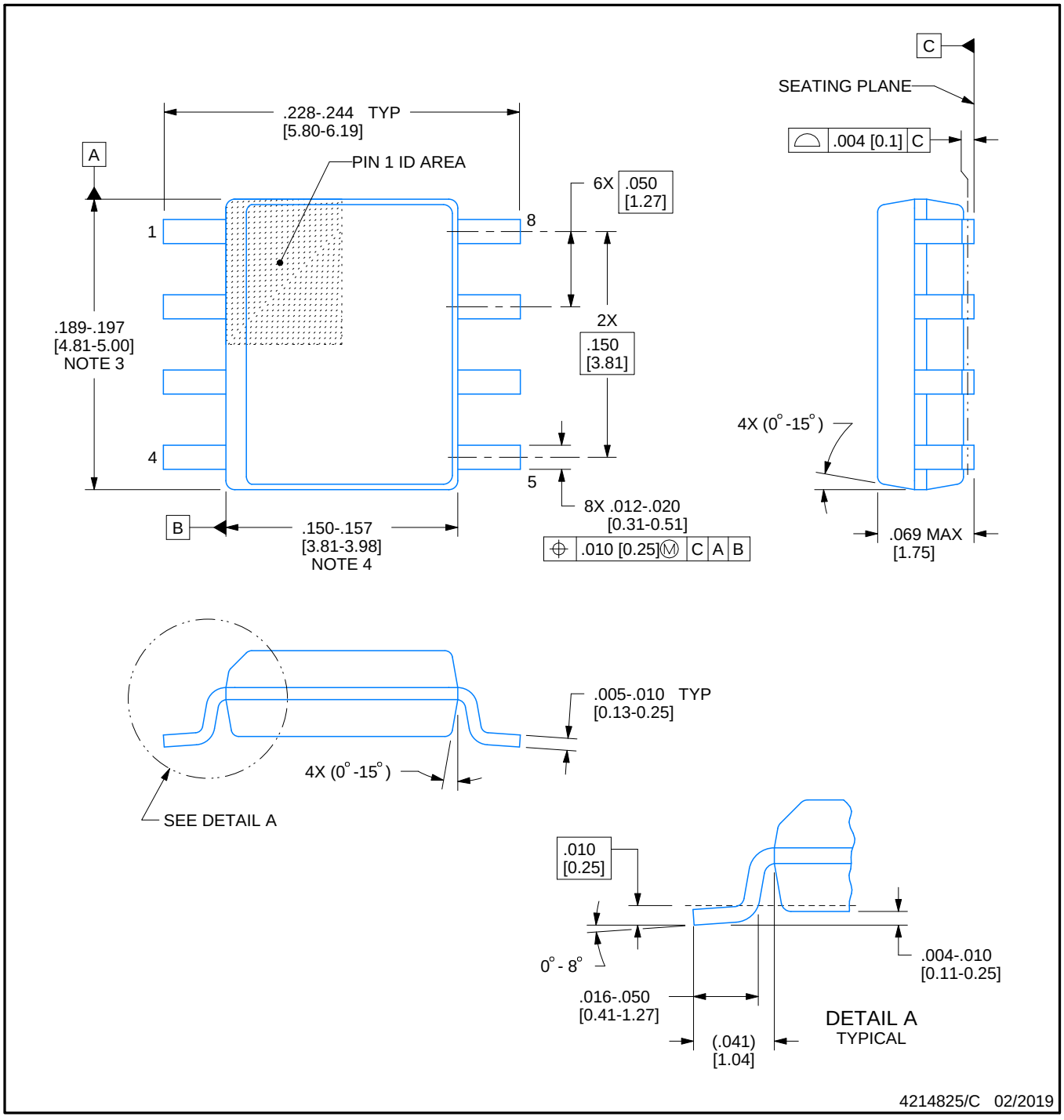


PACKAGE OUTLINE

D0008A

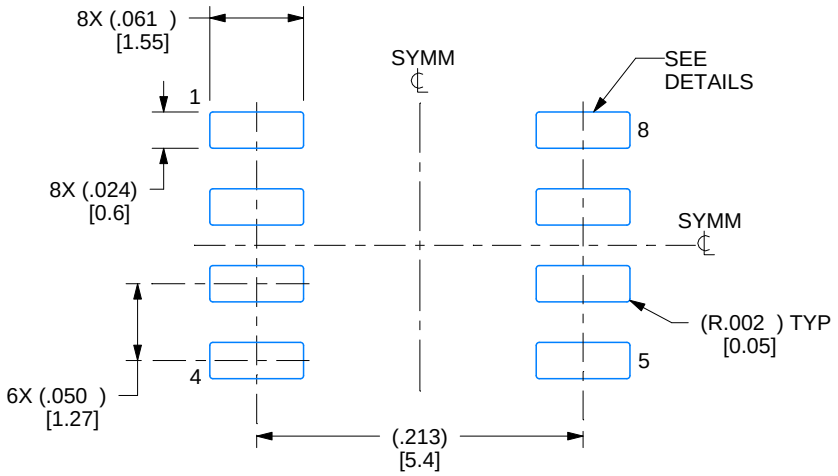
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

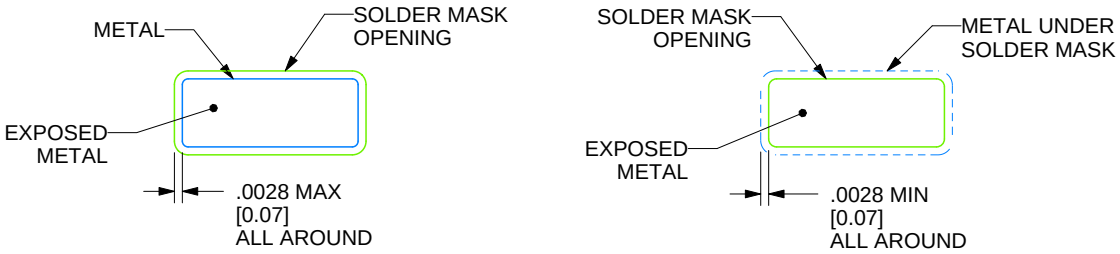


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

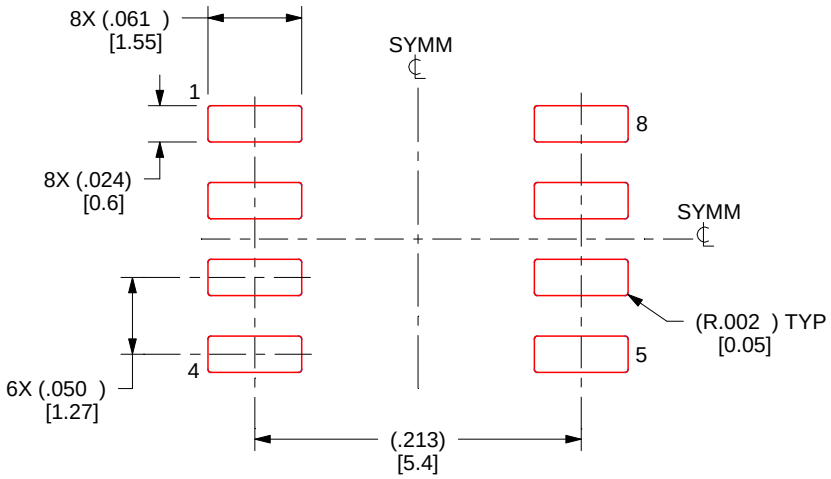
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



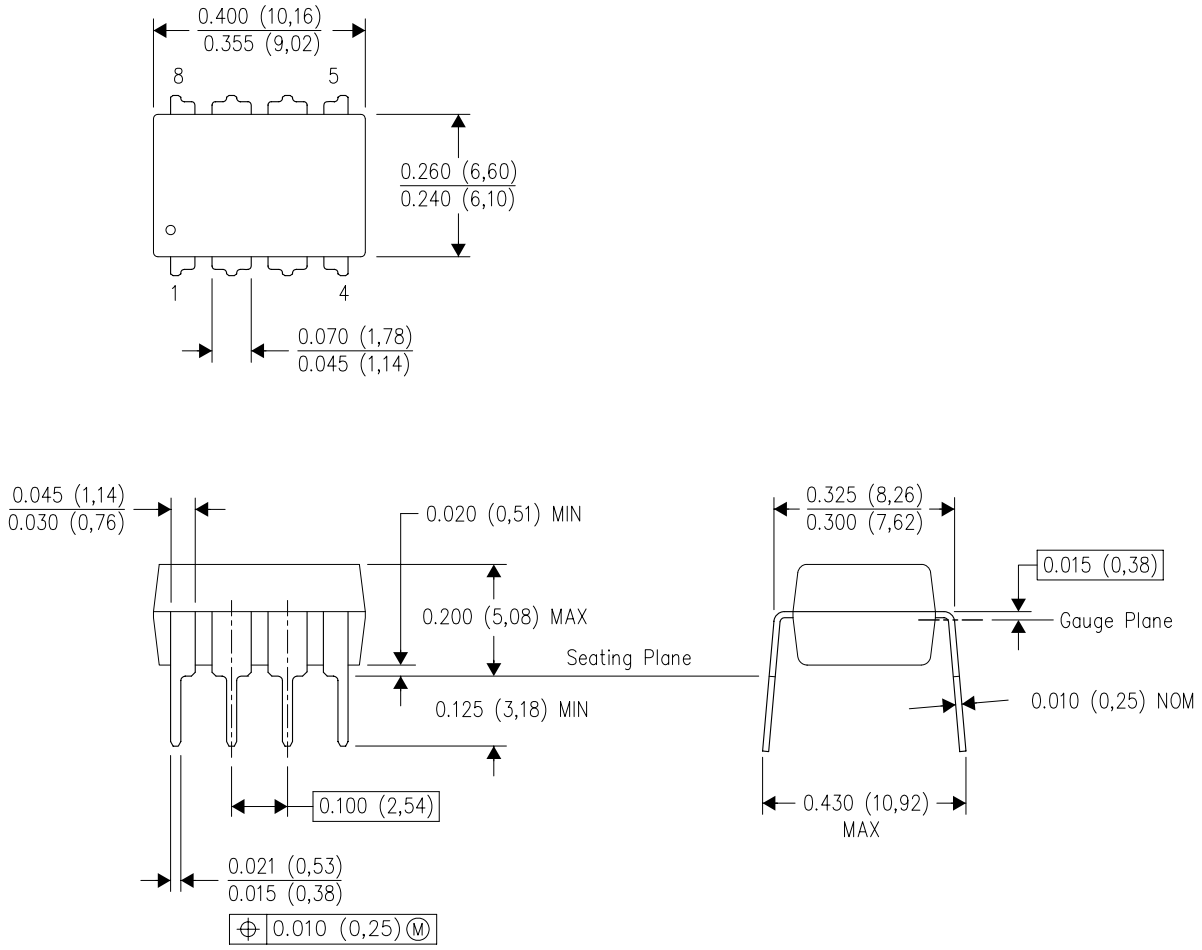
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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