EVM User's Guide: TLV755EVM-087

TLV755EVM-087 Evaluation Module

Description

The TLV755 evaluation module (EVM) helps design engineers evaluate the operation and performance of the TLV755 linear regulator for use in circuit applications. The configuration of the TLV755EVM-087 contains a single low-I_Q, small-size, linear regulator for a wide range of applications. The regulator is capable of delivering up to 500mA.

Get Started

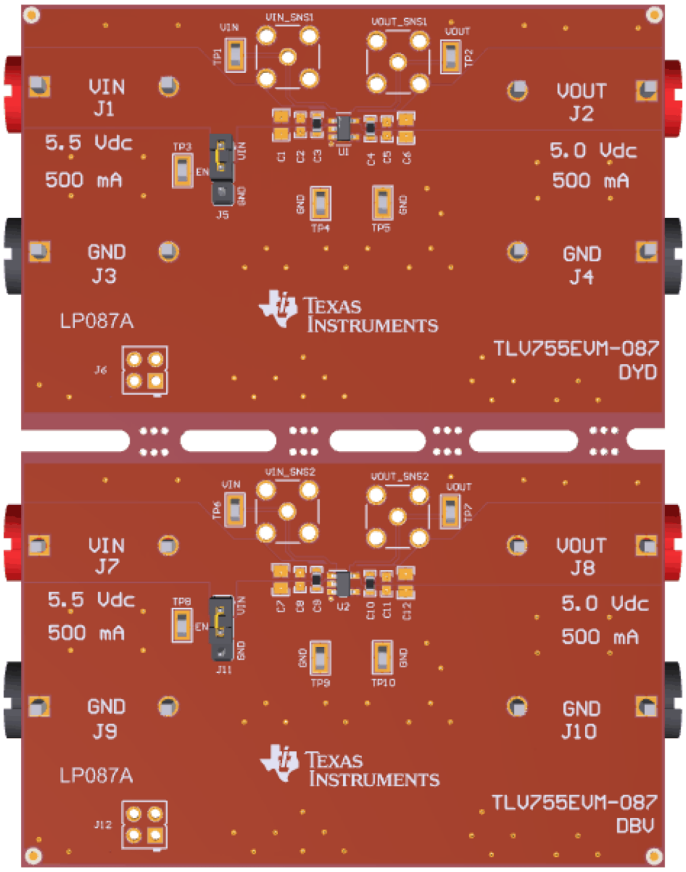
1. Order the TLV755EVM-087 Evaluation Module
2. Download the TLV755EVM-087 Evaluation Module User's Guide

Features

- 1% accuracy over load, line, and temperature
- Available in fixed-output voltages: 0.7V to 3.3V
- Improved thermal performance over JEDEC standards
- Active output discharge

Applications

- Personal electronics and gaming
- PC and notebooks
- Tablets
- Appliances
- Grid infrastructure and protection relays
- Advanced Driver Assistance Systems (ADAS) and sensor fusion



TLV755EVM-087 Hardware Board

1 Evaluation Module Overview

1.1 Introduction

The Texas Instruments' TLV755EVM-087 evaluation module (EVM) helps designers evaluate the operation and performance of the TLV755 LDO voltage regulator. The TLV755EVM-087 offers the capability to evaluate the TLV755 in DBV and DYD package options, each one electrically isolated from the other through tab routing. The boards can be easily separated if desired. As shown in Table 1-1, the TLV755EVM-087 contains two TLV755 LDO voltage regulator in the DBV and DYD packages.

This user's guide describes the operational use of the TLV755EVM-087 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TLV755 low-dropout linear regulator (LDO). Included in this user's guide are setup and operating instructions, thermal and layout guidelines, a printed-circuit board (PCB) layout, a schematic diagram, and a bill of materials (BOM). Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the TLV755EVM-087.

Table 1-1. Device Information

EVM ORDERABLE NUMBER	V_{OUT}	PART NAME	PACKAGE
TLV755EVM-087	1.8V	TLV75518PDYDR	DYD
	1.8V	TLV75518PDBVR	DBV

1.2 Kit Contents

The package includes:

1. TLV755EVM-087 evaluation module (EVM) version 1.0, which has tab-routed DYD and DBV layouts.
2. EVM Disclaimer Read Me
3. Antistatic foam

What is Not Included

A TLV755EVM-087 Evaluation User's Module. This PDF is available on ti.com.

1.3 Specification

The evaluation module provides banana cable input and output; along with SMA connections for LDO Input and Output sense. Power supplies for VIN and VENABLE must be rated to meet the data sheet specifications. A electronic load is not recommended for testing because the load can negatively interfere with LDO compensation loops.

1.4 Device Information

Table 1-2. Device Information

EVM ORDERABLE NUMBER	V_{OUT}	PART NAME	PACKAGE
TLV755EVM-087	1.8V	TLV75518PDBVR	SOT-23 (5)
	1.8V	TLV75518PDYDR	SOT-23 with pad (5)

2 Hardware

2.1 Setup

This section describes the jumpers and connectors on the EVM, and how to properly connect, set up, and use the TLV755EVM-087. LDO Input/Output Connector Descriptions and TLV755 LDO Operation describe the test setup and operation for the TLV755 LDO.

2.1.1 LDO Input/Output Connector Descriptions

2.1.1.1 VIN and GND

VIN and GND are the connection terminals for the input supply. The VIN terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection. Apply a voltage between V_{OUT}+0.5V and 5.5V

2.1.1.2 VOUT and GND

VOUT and GND are the connection terminals for the output load. The VOUT terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.1.1.3 EN

EN is a 3-pin header used to enable or disable the TLV755. The center pin of the 3-pin header is tied to the TLV755 EN input. When the 2-pin shunt is placed across the top two pins of the header, VIN is shorted to EN, and the TLV755 is enabled. When the 2-pin shunt is placed across the bottom two pins of the header, GND is shorted to EN, and the TLV755 is disabled. When driving the EN terminal with an off-board supply or signal generator, the applied voltage must be kept between 0V and 5.5V

2.1.2 TLV755 LDO Operation

The TLV755EVM-087 evaluation module contains the TLV755 LDO with input and output capacitors installed. These two components provide the minimum required solution-size. Additional pads are available to test the LDO with additional input and output capacitors beyond what is already installed on the EVM. The TLV755 LDO can be enabled or disabled by using the J5 3-pin header for the DYD package option and the J11 3-pin header for the DBV package option.

1. Place a 2-pin shunt across the header to tie VIN to EN to enable the device.
2. Place a 2-pin shunt across the header to tie GND to EN to disable the device.

Alternatively, by connecting an external function generator to TP3 (EN for DYD) or TP8 (EN for DBV) and a nearby GND, the user can enable or disable the TLV755 LDO after VIN is applied. Figure 2-1shows the result of the TLV755EVM-087 during turn on. The pink trace is the enable voltage, and the green trace is the output voltage.

Figure 2-1. TLV755EVM-087 Turn On

3 Hardware Design Files

3.1 TLV755EVM-087 Schematics

Figure 3-1 shows a schematic for the TLV755EVM-087, DYD package.

Figure 3-2shows a schematic for the TLV755EVM-087, DBV package.

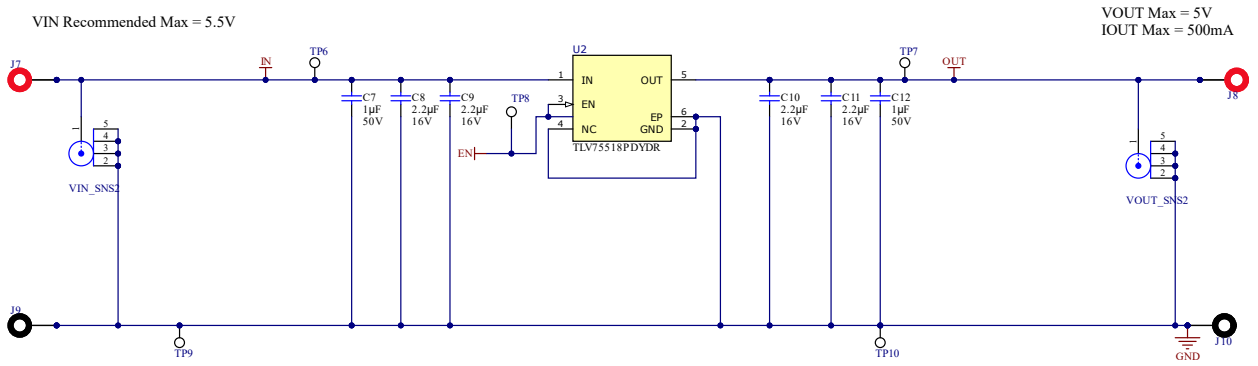


Figure 3-1. DYD Schematic

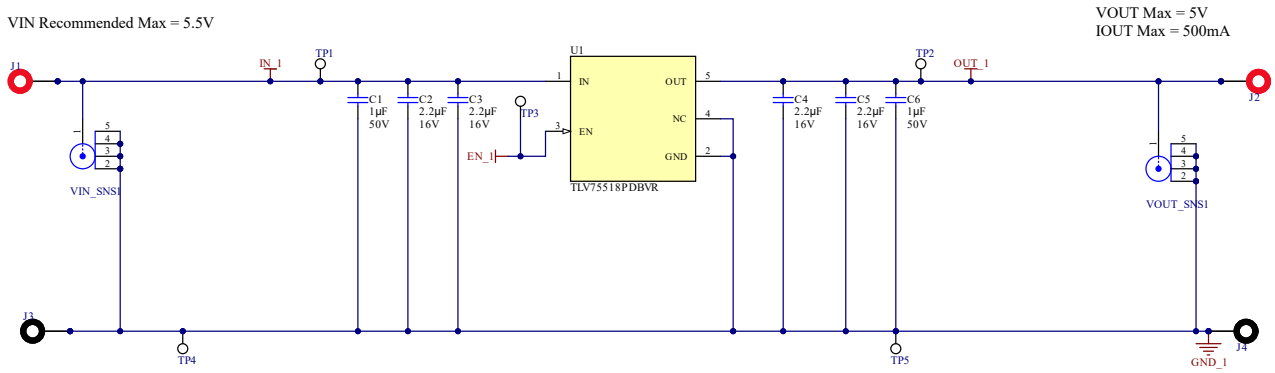


Figure 3-2. DBV Schematic

3.2 PCB Layouts

Figure 3-3 through Figure 3-8 illustrate the board layout for the TLV755EVM-087 PCB

The TLV755EVM-087 PCB dissipates power, which can cause some components to experience an increase in temperature. The LDO can become hot to the touch during normal operation; see the thermal impedance discussion in the TLV755P data sheet.

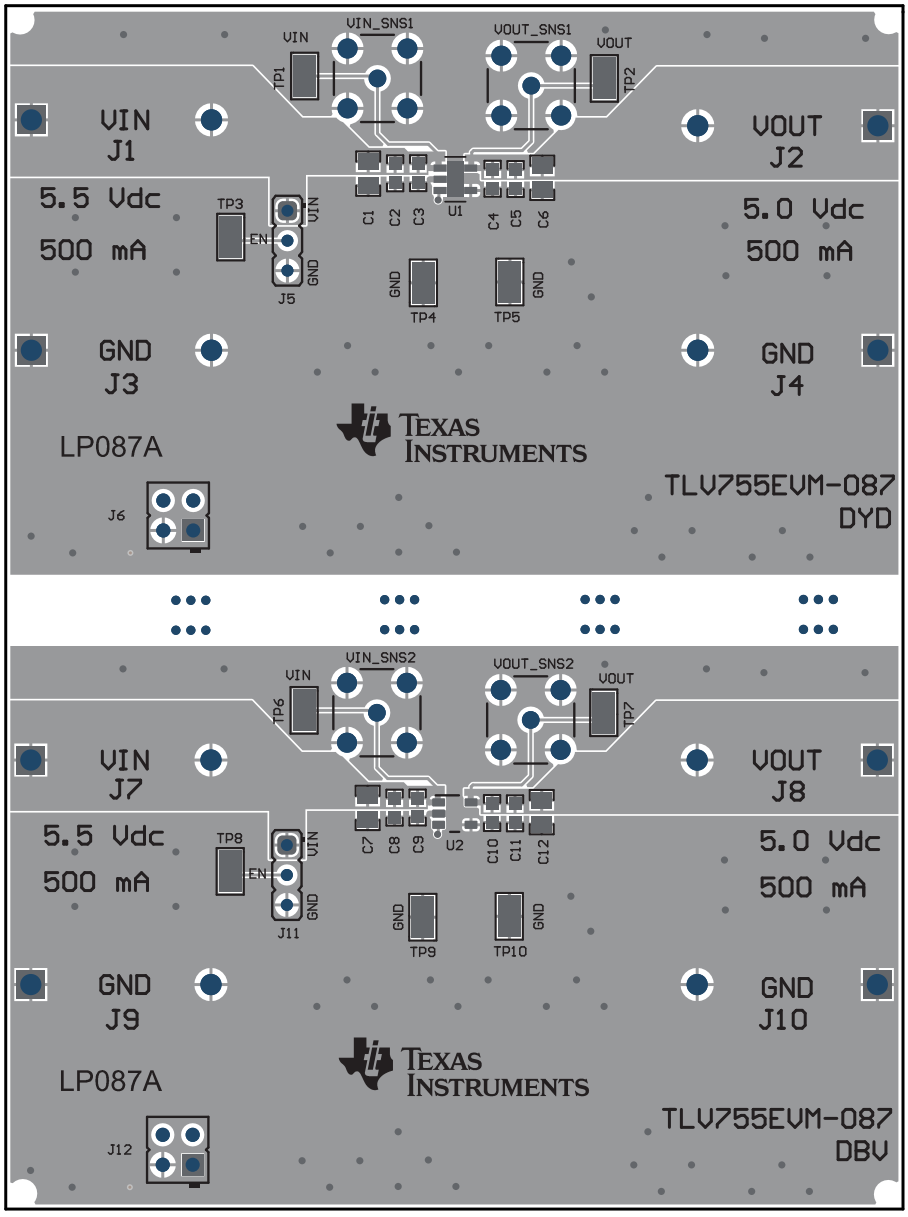


Figure 3-3. Top Assembly Layer and Silkscreen

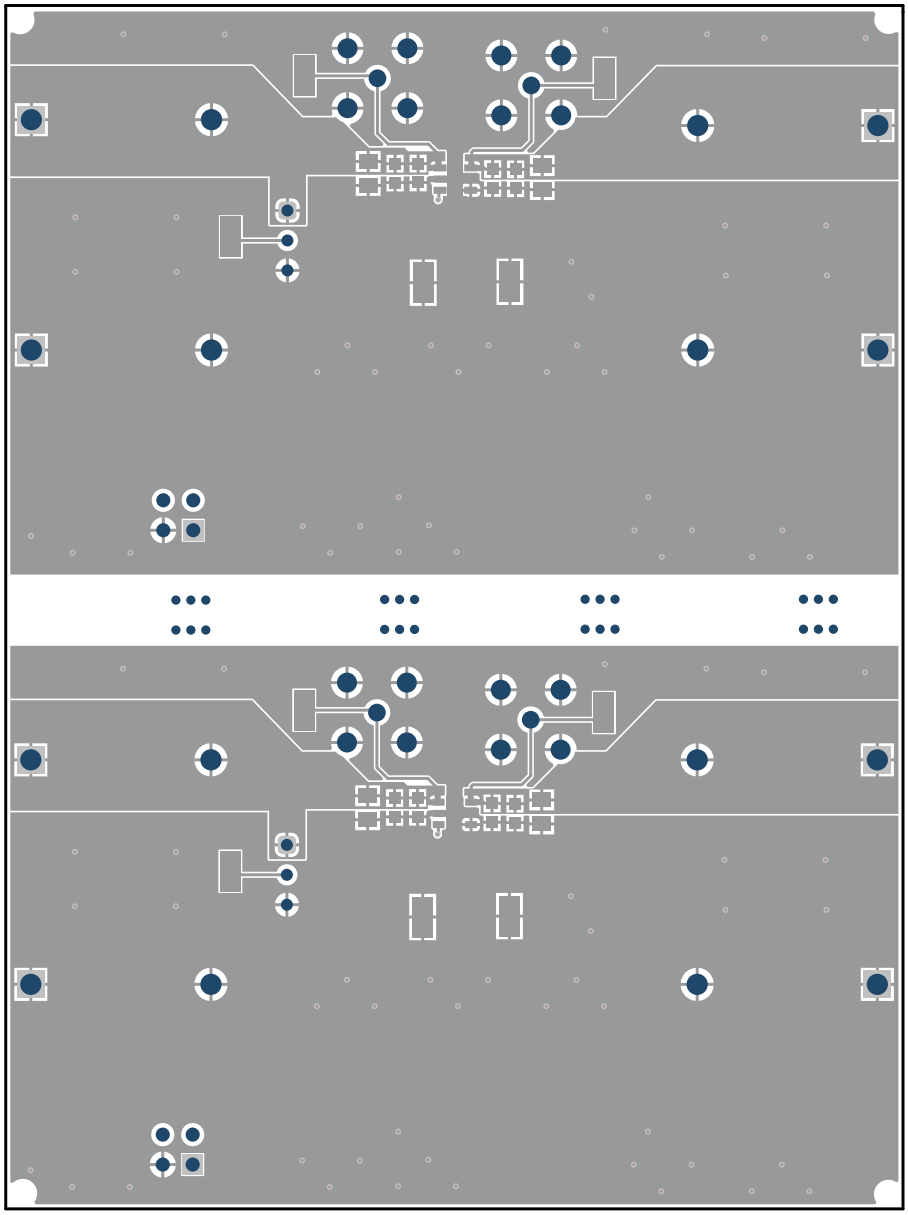


Figure 3-4. Top Layer Routing

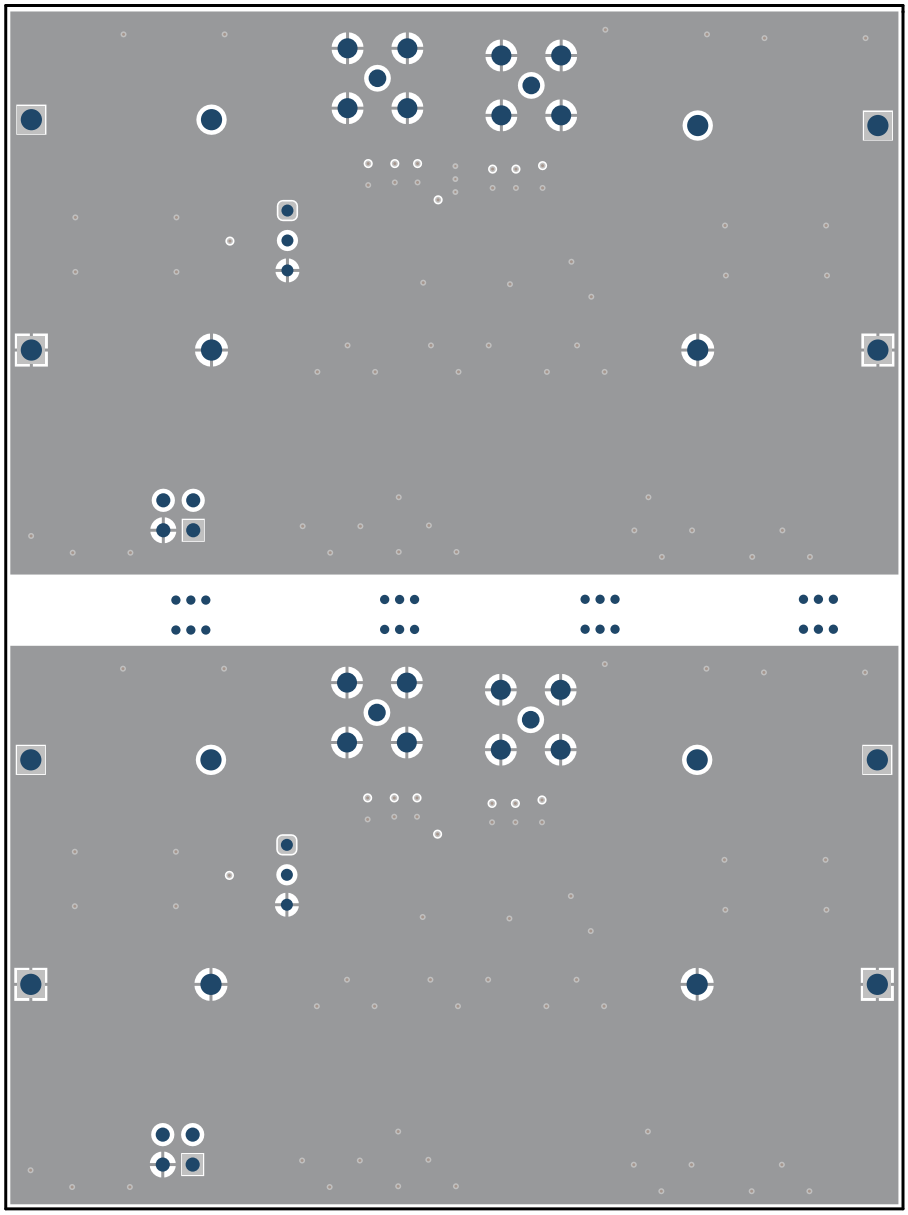


Figure 3-5. Layer 2

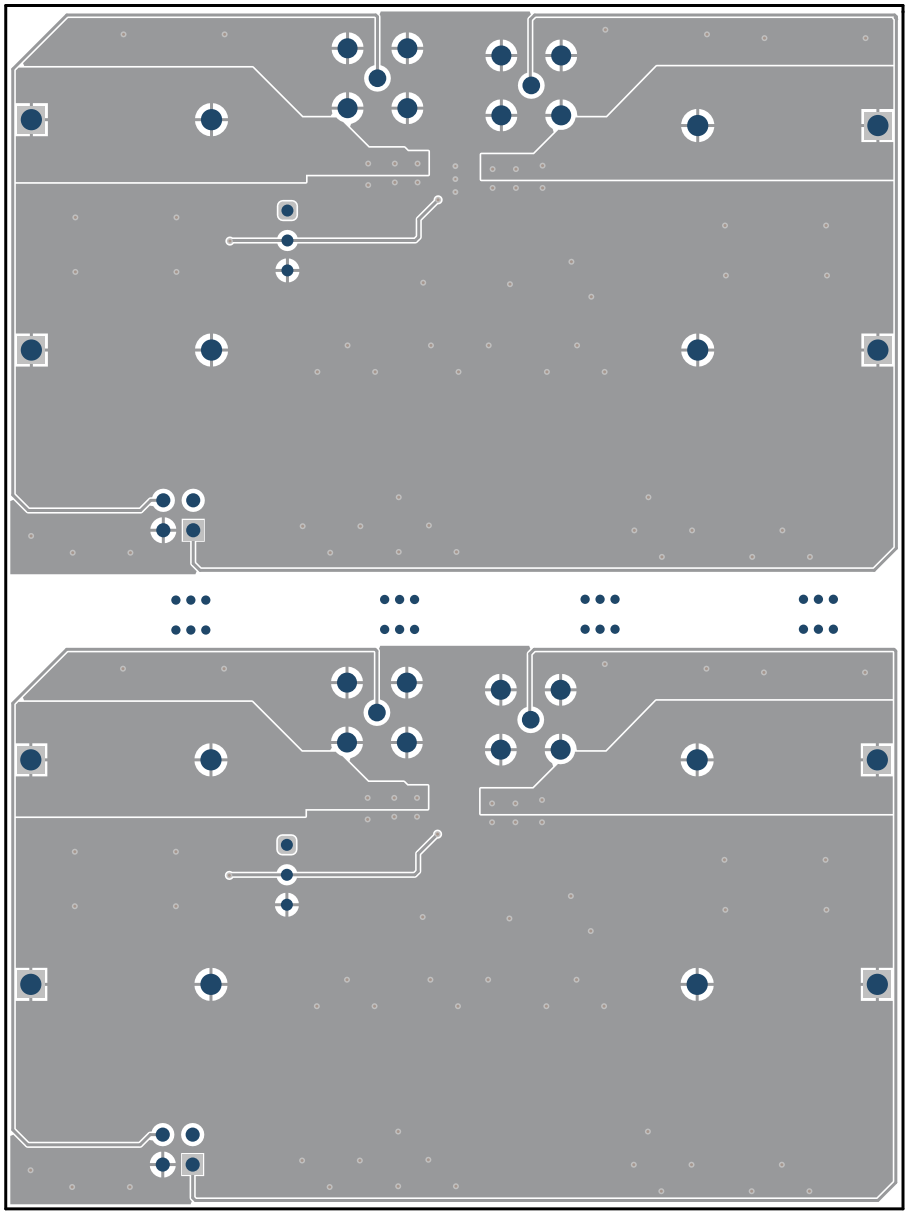


Figure 3-6. Layer 3

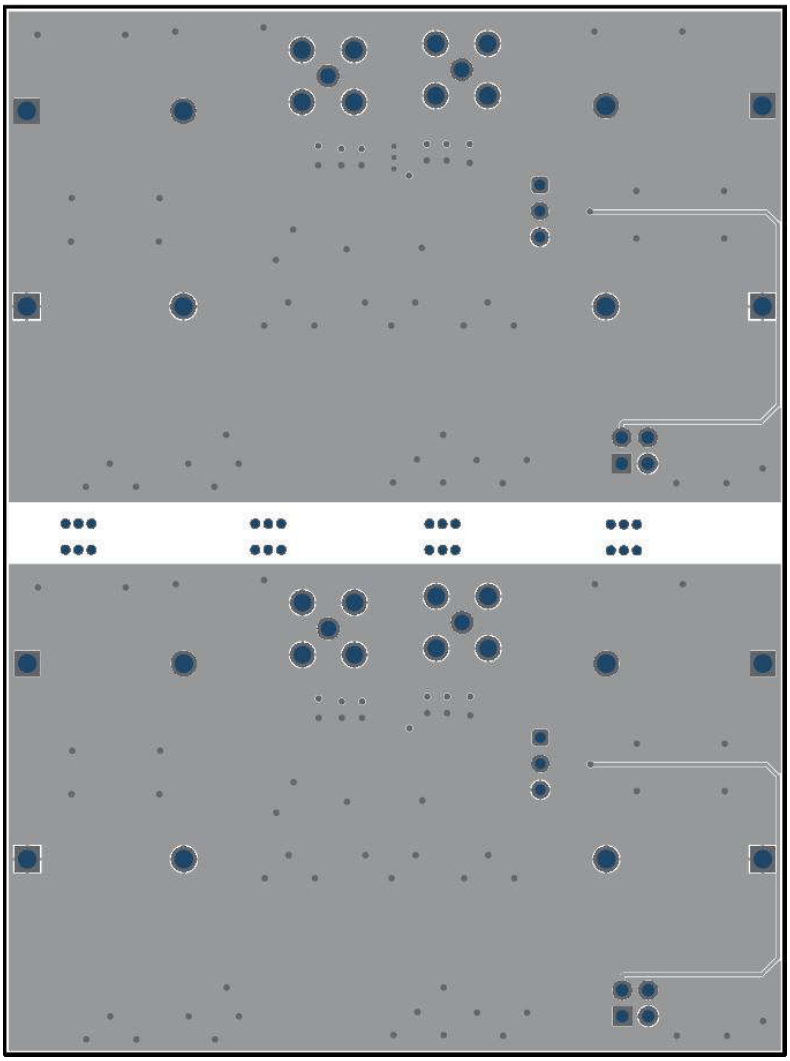


Figure 3-7. Bottom Layer Routing

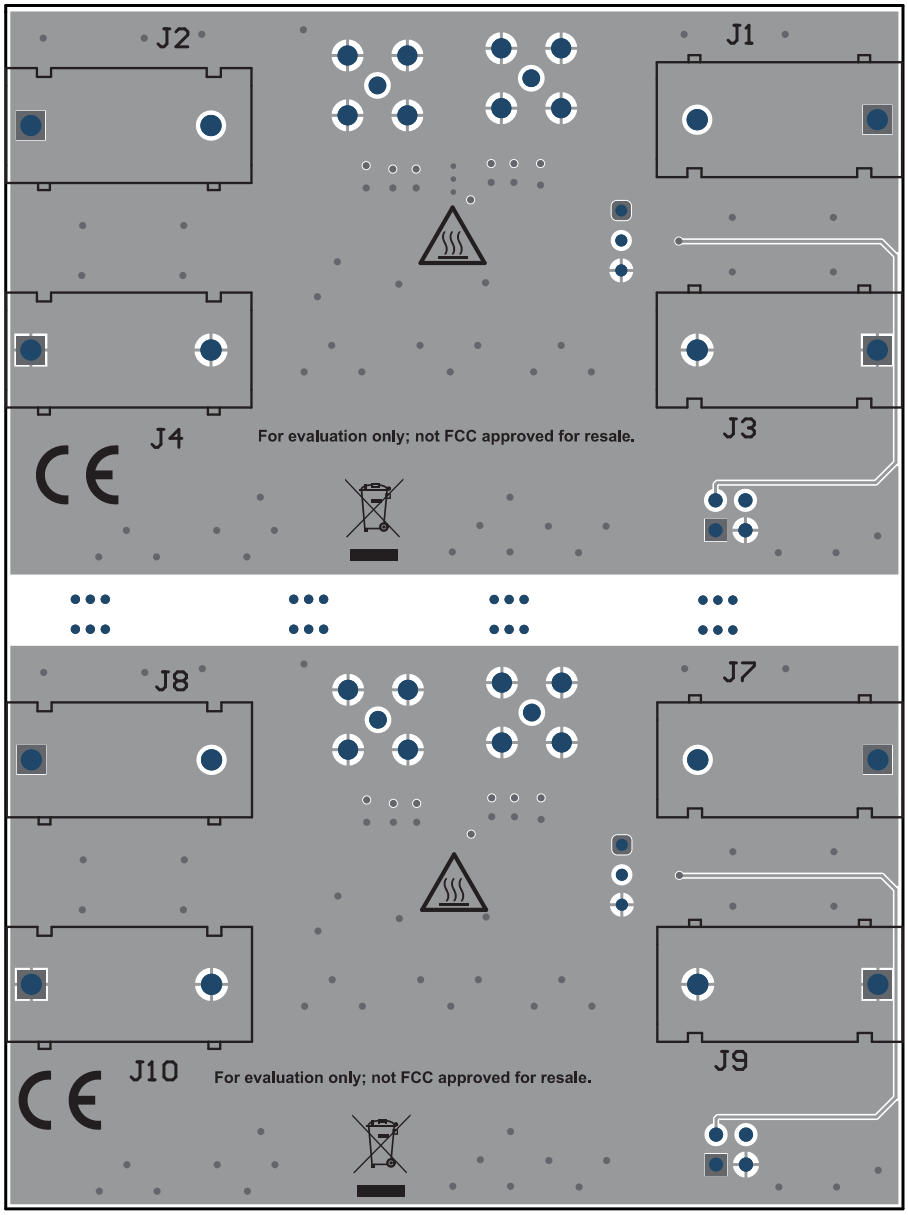


Figure 3-8. Bottom Assembly Layer and Silkscreen

3.3 Bill of Materials (BOM)

Table 3-1 lists the bill of materials (BOM) for the TLV755EVM-087.

Table 3-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		LP087	Any
C3, C4, C9, C10	4	2.2uF	CAP CER 2.2UF 16V X7R 0603	0603	CC0603KRX7R7BB225	Yageo America
J1, J2, J7, J8	4		Standard Banana Jack, Insulated, 10A, Red	571-0500	571-0500	DEM Manufacturing
J3, J4, J9, J10	4		Standard Banana Jack, Insulated, 10A, Black	571-0100	571-0100	DEM Manufacturing
J5, J11	2		Header, 2.54mm, 3x1, Tin, TH	Header, 2.54mm, 3x1, Tin, TH	2.2E+07	Molex
SH-J1, SH-J2	2	1x2	CONN SHUNT 2POS	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10		PC TEST POINT MINIATURE	Testpoint_Keystone_Miniature	5015	Keystone
U1	1		IC REG LINEAR 1.8V 500MA SOT23-5	DBV0005A	TLV75518PDBVR	Texas Instruments
U2	1		TLV75518PDYDR	SOT23-5	TLV75518PDYDR	Texas Instruments

4 Additional Information

4.1 Trademarks

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