SN74LVC244A Octal Buffer or Driver With 3-State Outputs

1 Features

- Operates from 1.65V to 3.6V
- Inputs accept voltages to 5.5V
- Specified from –40°C to +85°C and –40°C to +125°C
- Maximum t_{pd} of 5.9ns at 3.3V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_A = 25°C
- Supports mixed-mode signal operation on all ports (5V input or output voltage with 3.3V V_{CC})
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Can be used as a down translator to translate inputs from a maximum of 5.5V down to the V_{CC} level
- Available in ultra small logic QFN package (0.5mm maximum height)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Servers
- LED displays
- Network switches
- Telecom infrastructure
- Motor drivers
- I/O expanders
- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

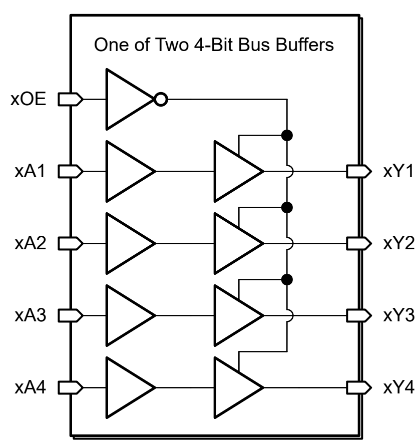
3 Description

These octal bus buffers are designed for 1.65V to 3.6V V_{CC} operation. The SN74LVC244A devices are designed for asynchronous communication between data buses.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC244A	RKS (VQFN, 20)	4.50mm × 2.50mm	4.50mm × 2.50mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	NS (SOP, 20)	12.60mm × 7.8mm	12.60mm × 5.30mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.30mm
	DGV (TVSOP, 20)	5.00mm × 6.4mm	5.00mm × 4.4mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm
	RGY (VQFN, 20)	4.50mm × 3.50mm	4.50mm × 3.50mm
	ZQN (BGA, 20)	4.00mm × 3.00mm	4.00mm × 3.00mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm
	RWP (X1QFN, 20)	3.30mm × 2.50mm	3.30mm × 2.50mm
	DGS (VSSOP, 20)	5.10mm × 4.90mm	5.10mm × 3.00mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

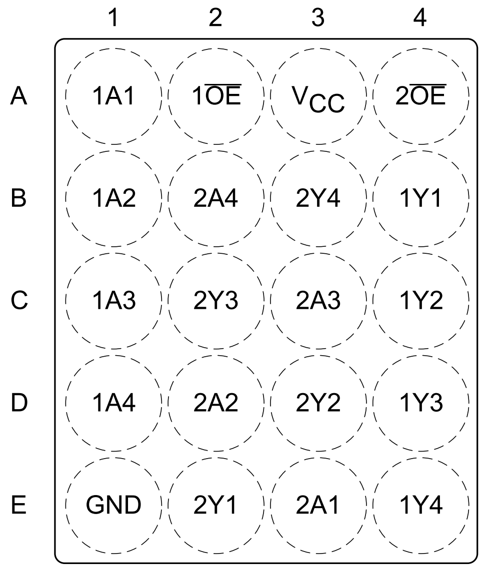

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Figure 4-1. ZQN Package 20-Pin BGA Top View

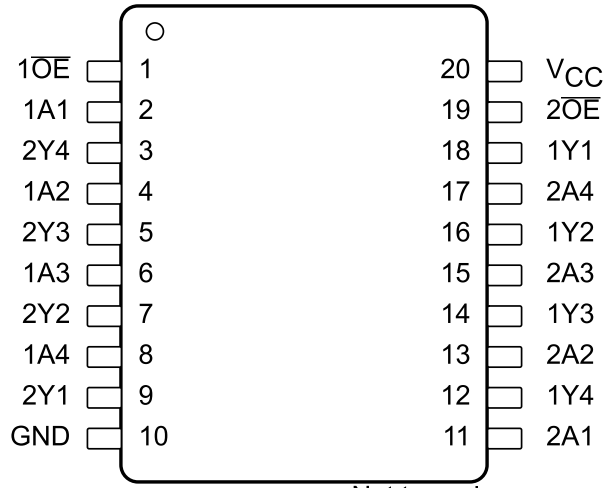

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Figure 4-2. DB, DGV,DW, N, NS, DGS and PW Packages 20-Pin SSOP, TVSOP, SOIC, PDIP, SO,VSSOP and TSSOP Front View

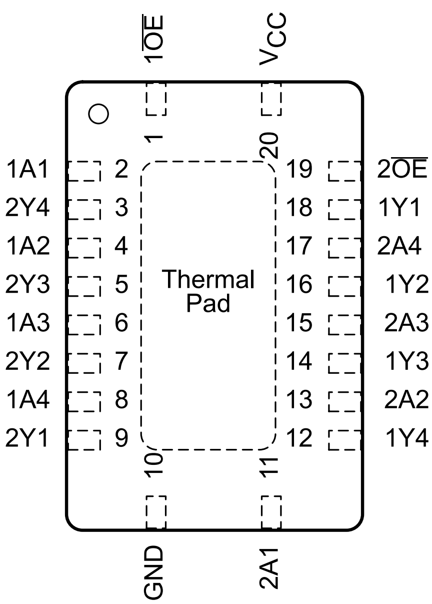

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Figure 4-3. RGY and RKS Packages 20-Pin VQFN Top View

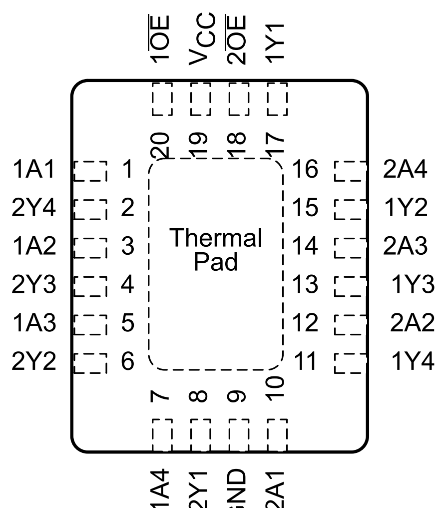

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Figure 4-4. RWP Package 20-Pin X1QFN Top View

Table 4-1. Pin Functions

PIN				TYPE[(1)]	DESCRIPTION
NAME	DB, DGV, DW, N, NS, PW, RGY, DGS and RKS	ZQN	RWP		
1A1	2	A1	1	I	Port 1A1 input

Table 4-1. Pin Functions (continued)

PIN				TYPE[1]	DESCRIPTION
NAME	DB, DGV, DW, N, NS, PW, RGY, DGS and RKS	ZQN	RWP		
1A2	4	B1	3	I	Port 1A2 input
1A3	6	C1	5	I	Port 1A3 input
1A4	8	D1	7	I	Port 1A4 input
1 $\overline{OE}$	1	A2	20	I	Output enable
1Y1	18	B4	17	O	Port 1Y1 output
1Y2	16	C4	15	O	Port 1Y2 output
1Y3	14	D4	13	O	Port 1Y3 output
1Y4	12	E4	11	O	Port 1Y4 output
2A1	11	E3	10	I	Port 2A1 input
2A2	13	D2	12	I	Port 2A2 input
2A3	15	C3	14	I	Port 2A3 input
2A4	17	B2	16	I	Port 2A4 input
2 $\overline{OE}$	19	A4	18	I	Output enable
2Y1	9	E2	8	O	Port 2Y1 output
2Y2	7	D3	6	O	Port 2Y2 output
2Y3	5	C2	4	O	Port 2Y3 output
2Y4	3	B3	2	O	Port 2Y4 output
GND	10	E1	9	—	Ground
V_{CC}	20	A3	19	—	Power pin

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2] [3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
P_{tot}	Power dissipation	T_A = –40°C to +125°C[4] [5]		500	mW
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Section 5.3* table.
(4) For the DW package: above 70°C the value of P_{tot} derates linearly with 8mW/K.
(5) For the DB, DGV, N, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)[1]

			T_A = 25°C		–40 TO +85°C		–40 TO +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 1.95V	0.65 × V_{CC}		0.65 × V_{CC}		0.65 × V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		1.7		1.7		
		V_{CC} = 2.7V to 3.6V	2		2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65V to 1.95V		0.35 × V_{CC}		0.35 × V_{CC}		0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7		0.7		0.7	
		V_{CC} = 2.7V to 3.6V		0.8		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4		–4		–4	mA
		V_{CC} = 2.3V		–8		–8		–8	
		V_{CC} = 2.7V		–12		–12		–12	
		V_{CC} = 3V		–24		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4		4		4	mA
		V_{CC} = 2.3V		8		8		8	
		V_{CC} = 2.7V		12		12		12	
		V_{CC} = 3V		24		24		24	
T_A	Ambient temperature	BGA package			–40	85			°C
		All other packages					–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to verify proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC[1]						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	20	120.3	62.5	82.4	16.0	81.5	N/A	°C/W
DGS (VSSOP)	20	124.5	62.9	79.2	7.8	78.7	N/A	°C/W
RKS (VQFN)	20	87.2	93.4	59.8	24.9	59.6	44.3	°C/W
DB (SSOP)	20	121.7	86.8	87.8	44.7	87.0	N/A	°C/W
DW (SOIC)	20	114.8	84.1	88.8	55.8	87.8	N/A	°C/W
NS (SOP)	20	116.3	82.4	86.2	43.9	85.5	N/A	°C/W
RGY (VQFN)	20	82.84	88.73	56.81	32.37	56.62	42.09	°C/W
N (PDIP)	20	61.6	46.5	42.5	34.6	42.4	N/A	°C/W
NS (SO)	20	90.1	56.4	57.7	28.4	57.2	N/A	°C/W
RWP (X1QFN)	20	79.9	63.2	46.4	2.6	46.3	N/A	°C/W
DGV (TVSOP)	20	128.7	43.7	70.2	3.1	69.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40 TO +85°C		–40 TO +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –100μA	1.65V to 3.6V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.3		V
	I_{OH} = –4mA	1.65V	1.29			1.2		1.05		
	I_{OH} = –8mA	2.3V	1.9			1.7		1.55		
	I_{OH} = –12mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
	I_{OH} = –24mA	3V	2.3			2.2		2		
V_{OL}	I_{OL} = 100μA	1.65V to 3.6V			0.1		0.2		0.3	V
	I_{OL} = 4mA	1.65V			0.24		0.45		0.6	
	I_{OL} = 8mA	2.3V			0.3		0.7		0.75	
	I_{OL} = 12mA	2.7V			0.4		0.4		0.6	
	I_{OL} = 24mA	3V			0.55		0.55		0.8	
I_I	V_I = 5.5V or GND	3.6V			±1		±5		±20	μA
I_{off}	V_I or V_O = 5.5V	0			±1		±10		±20	μA
I_{OZ}	V_O = 0 to 5.5V	3.6V			±1		±10		±20	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V			1		10		40	μA
	3.6V ≤ V_I ≤ 5.5V(1), I_O = 0				1		10		40	
ΔI_{CC}	One input at V_{CC} – 0.6V, Other inputs at V_{CC} or GND	2.7V to 3.6V			500		500		5000	μA
C_i	V_I = V_{CC} or GND	3.3V		4						pF
C_o	V_O = V_{CC} or GND	3.3V		5.5						pF

(1) This applies in the disabled state only.

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			–40 TO +85°C		–40 TO +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.5V		7	14.4		14.9		16.4	ns
			1.8V ± 0.15V		5.9	10.4		10.9		12.4	
			2.5V ± 0.2V		4.2	7.4		7.9		10	
			2.7V		4.2	6.7		6.9		8.2	
			3.3V ±0.3V		3.9	5.7		5.9		7.2	
t_{en}	$\overline{OE}$	Y	1.5V		8.3	17.8		18.3		19.8	ns
			1.8V ±0.15V		6.4	12.1		12.6		14.1	
			2.5V ±0.2V		4.6	9.1		9.6		11.7	
			2.7V		5	8.4		8.6		10.3	
			3.3V ±0.3V		4.5	7.4		7.6		9.4	
t_{dis}	$\overline{OE}$	Y	1.5V		7.2	15.6		16.1		17.6	ns
			1.8V ±0.15V		5.8	11.6		12.1		13.6	
			2.5V ±0.2V		3.7	7.3		7.8		9.9	
			2.7V		3.8	6.6		6.8		8.6	
			3.3V ±0.3V		3.8	6.3		6.5		8	
$t_{sk(o)}$			3.3V ±0.3V					1		1.5	ns

5.7 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10MHz	1.8V	43	pF
				2.5V	43	
				3.3V	44	
		Outputs disabled	f = 10MHz	1.8V	1	
				2.5V	1	
				3.3V	2	

5.8 Typical Characteristics

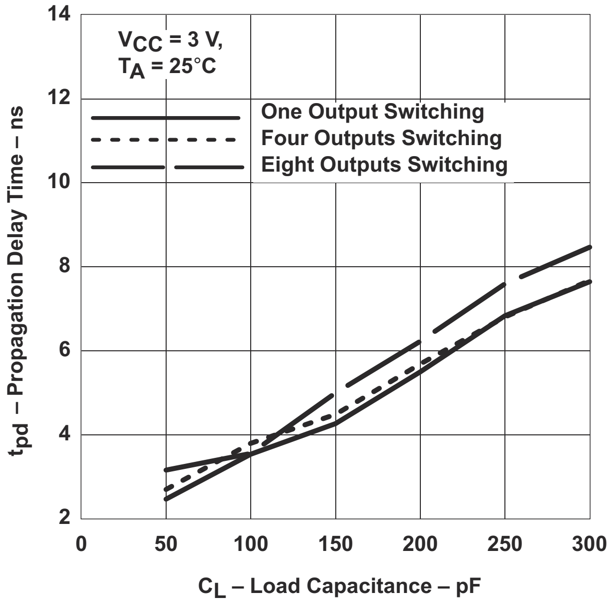


Figure 5-1. Propagation Delay (Low to High Transition) vs Load Capacitance

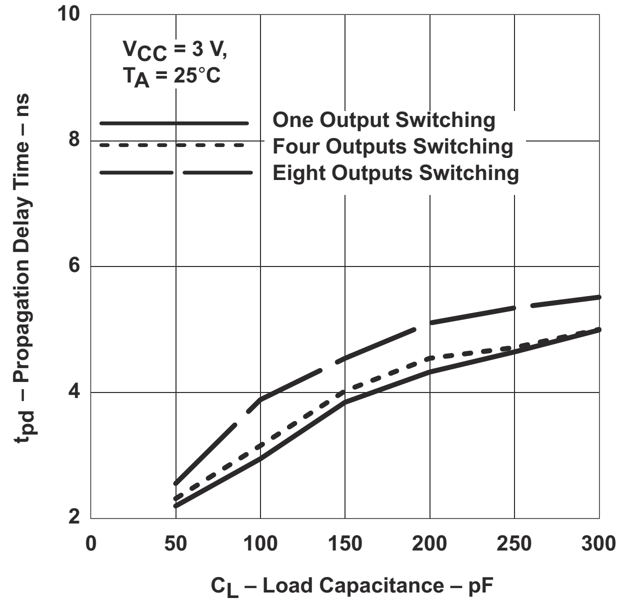
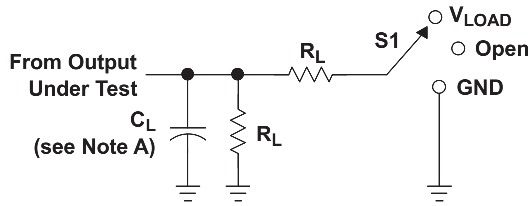


Figure 5-2. Propagation Delay (High to Low Transition) vs Load Capacitance

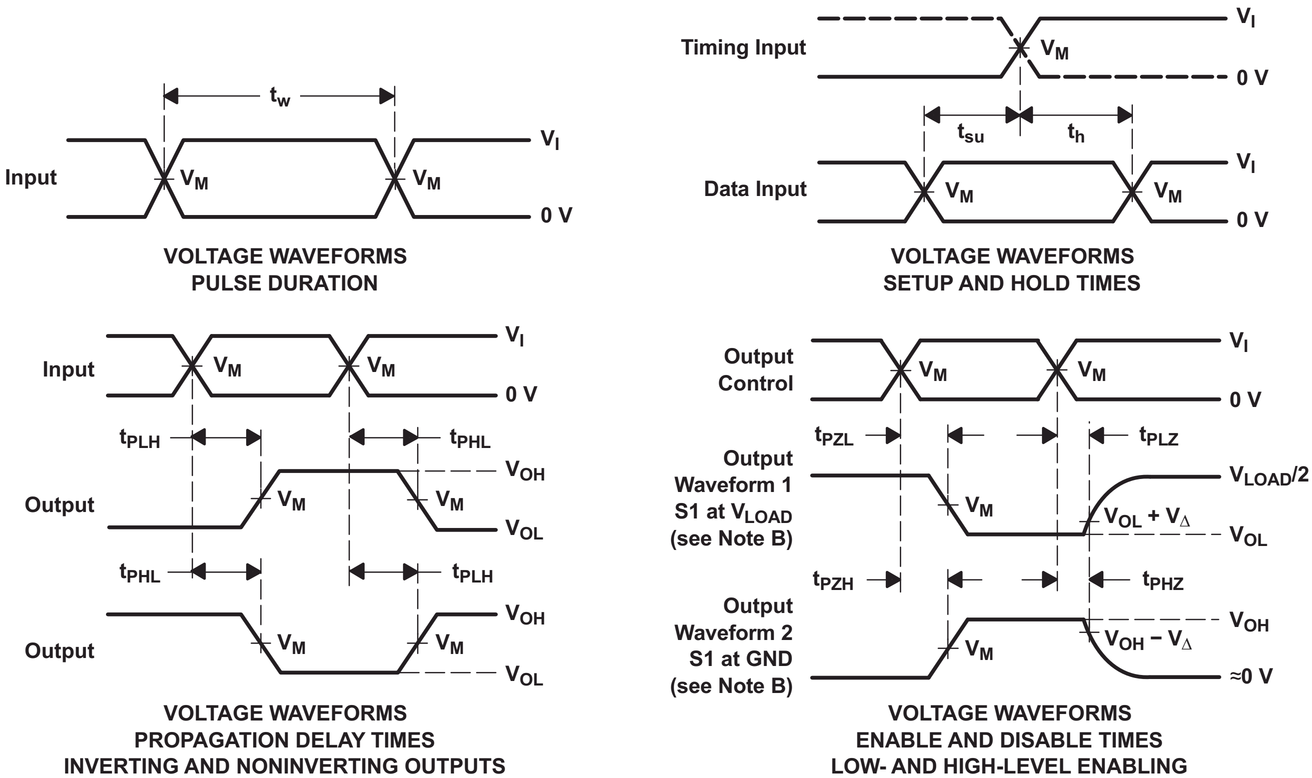
6 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.5 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC244A contains 8 individual high speed CMOS buffers organized as two 4-bit buffers/line drives with 3-state outputs.

Each buffer performs the boolean logic function xYn = xAn, with *x* being the bank number and *n* being the channel number.

Each output enable ($x\overline{OE}$) controls four buffers. When the $x\overline{OE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the $x\overline{OE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both $\overline{OE}$ pins to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

7.2 Functional Block Diagram

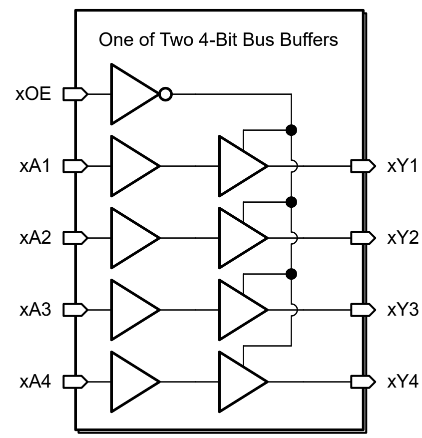


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.3.4 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION
Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

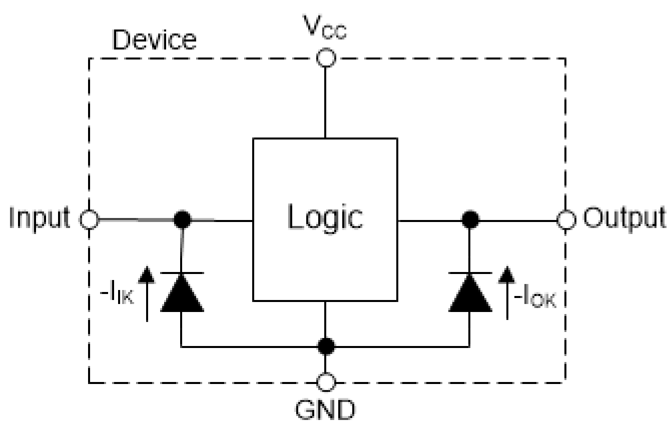


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC244A.

Table 7-1. Function Table

INPUTS[(1)]		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H

Table 7-1. Function Table (continued)

INPUTS(1)		OUTPUTS
$\overline{OE}$	A	Y
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74LVC244A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

8.2 Typical Application

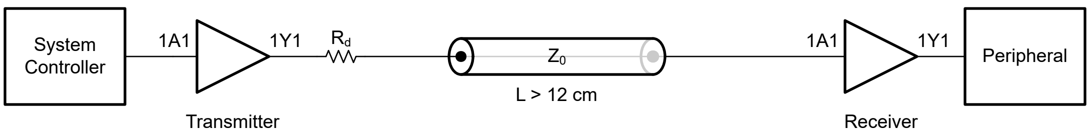


Figure 8-1. Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specification, see (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended maximum Output Conditions:
   - Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs must not be pulled above V_{CC}.

8.2.3 Application Curves

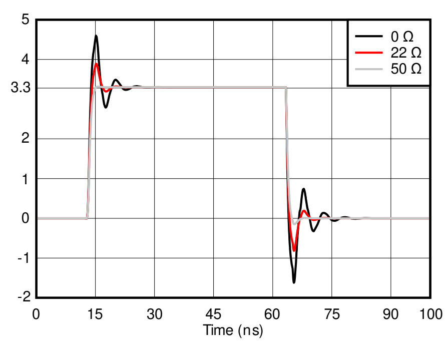


Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

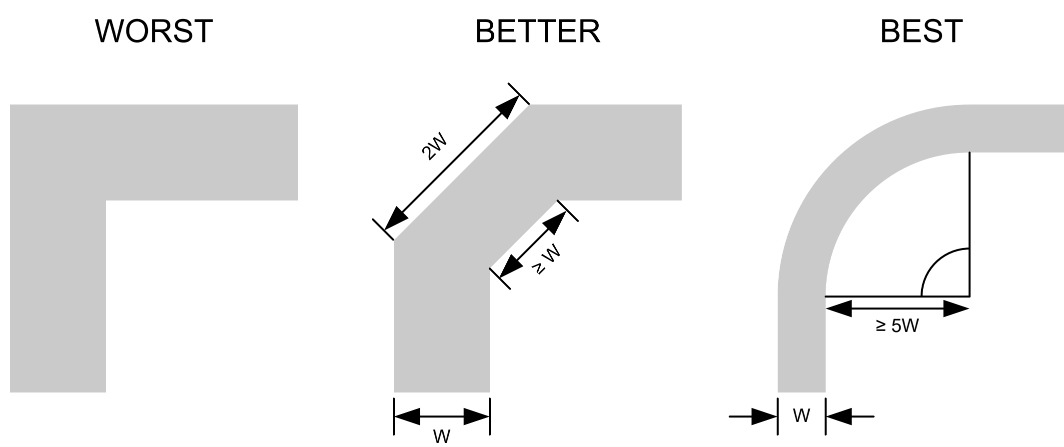


Figure 8-3. Example Trace Corners for Improved Signal Integrity

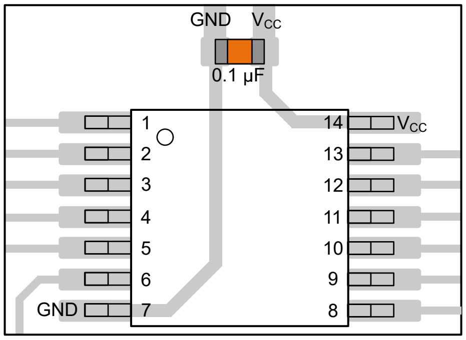


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

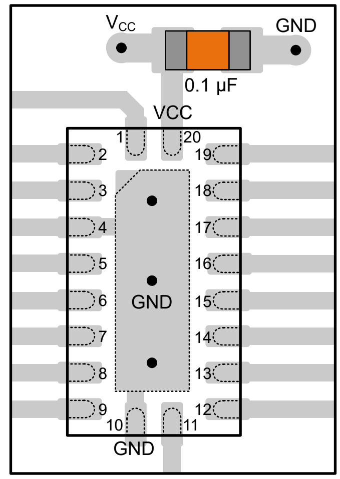


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

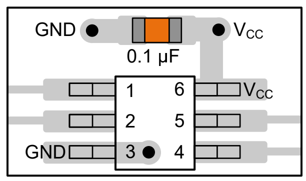


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

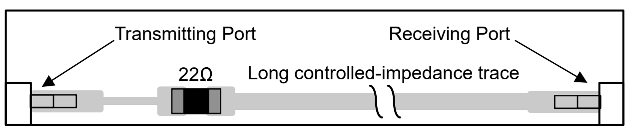


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 2, 2026 to June 26, 2026 (from Revision AF (February 2026) to Revision AG (June 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................ 1
- Changed RθJA for DB package from: 108.1°C/W to: 121.7°C/W... 6
- Changed RθJC(top) for DB package from: 70.2°C/W to: 86.8°C/W..6
- Changed ΨJT for DB package from: 63.3°C/W to: 87.8°C/W..6
- Changed ΨJB for DB package from: 30.6°C/W to: 44.7°C/W..6
- Changed RθJA for DW package from: 90.9°C/W to: 114.8°C/W...6
- Changed RθJC(top) for DW package from: 55.3°C/W to: 84.1°C/W...6
- Changed ΨJT for DW package from: 58.8°C/W to: 88.8°C/W...6
- Changed ΨJB for DW package from: 29.1°C/W to: 55.8°C/W...6

Changes from Revision AE (August 2025) to Revision AF (February 2026) **Page**

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.