TAS5828M 50W Stereo, Digital Input, High Efficiency Closed-Loop Class-D Amplifier with Hybrid-Pro Algorithm

1 Features

- Flexible audio I/O:
  - Supports 32, 44.1, 48, 88.2, 96, 192kHz sample rates
  - I^2S, LJ, RJ, TDM, SDOUT for audio monitoring, sub-channel or echo cancellation
  - Supports 3-wire digital audio interface (no MCLK required)
- High-efficiency Class-D modulation
  - > 90% power efficiency, 90mΩ R_{DS}on
- Supports multiple output configurations
  - 2 × 50W, 2.0 Mode (4Ω, 23V, THD+N=1%)
  - 2 × 40W, 2.0 Mode (6Ω, 24V, THD+N=1%)
  - 1 × 100W, 1.0 Mode (2Ω, 23V, THD+N=1%)
  - 1 × 80W, 1.0 Mode (3Ω, 24V, THD+N=1%)
- Excellent audio performance:
  - THD+N ≤ 0.03% at 1W, 1kHz, PVDD = 12V
  - SNR ≥ 110dB (A-weighted), ICN ≤ 40μVRMS
- Flexible processing features
  - 12 BQs per channel, level meter
  - 3-Band advanced DRC +2 BQs + AGL + 2 BQs
    - In 48kHz processor sampling mode
  - 48kHz, 96kHz, 192kHz processor sampling
  - Mixer, volume, dynamic EQ, output cross bar
  - PVDD sensing and hybrid-pro algorithm audio signal tracking
- Flexible power supply configurations
  - PVDD: 4.5V to 26.4V
  - DVDD and I/O: 1.8V or 3.3V
- Excellent integrated self-protection:
  - Over-current error (OCE)
  - Cycle-by-cycle current limit
  - Over-temperature warning (OTW)
  - Over-temperature error (OTE)
  - Under and over-voltage lock-out (UVLO/OVLO)
  - PVDD voltage drop detection
- Easy system integration
  - I^2C Software or Hardware Control Mode
  - Fewer passive required compared with open-loop devices

2 Applications

- Battery-powered speaker
- Wireless, Bluetooth speakers
- Soundbars and subwoofers
- Heat or efficiency sensitive audio system

3 Description

The TAS5828M is a stereo high-performance, closed-loop Class-D with integrated audio processor with up to 192kHz architecture.

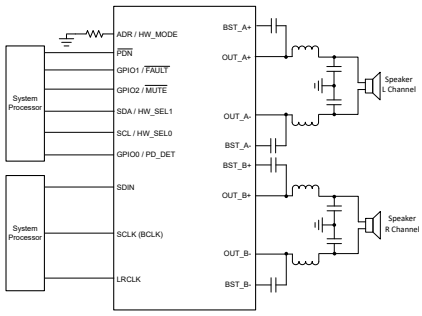
After startup with Software Control Mode, TAS5828M not only implements classic BQs, 3-Band DRC, and AGL, but also a proprietary algorithm called Hybrid-Pro. The Hybrid-Pro algorithm detects the upcoming audio power demand and provides a PWM format control signal for the former DC-DC converter via the Hybrid-Pro feedback pin (HPFB). The TAS5828M supports up to 4ms of delay buffer of audio signal for predictable envelop tracking, which significantly helps to prevent audio clipping due to DC-DC voltage adjustment.

While setting into Hardware control mode, TAS5828M supports switching frequency, analog gain, BTL/PBTL mode and cycle by cycle current limit threshold through pin configuration. This mode is especially designed to eliminate end system software driver integration efforts.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TAS5828M	DAD (TSSOP, 32)	11.00mm × 6.20mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

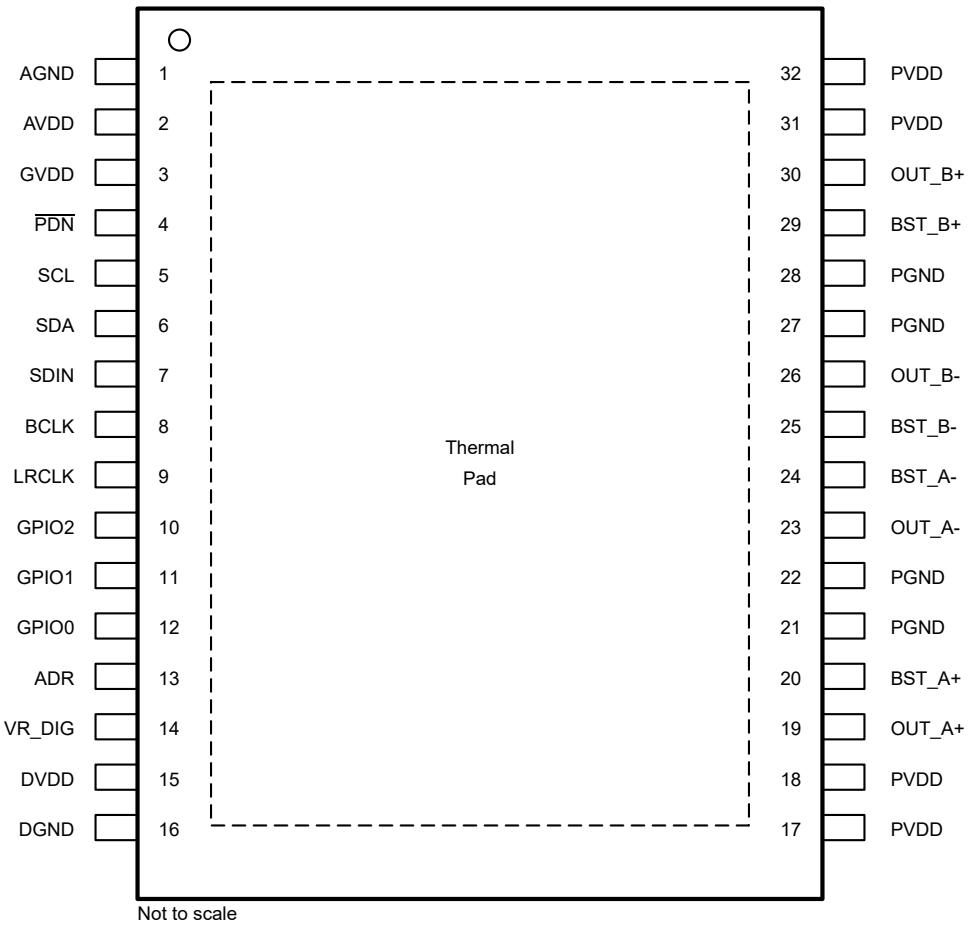

Figure 4-1. DAD (TSSOP) Package, 32-Pin PadUp, Software Mode, Top View

Table 4-1. Pin Functions - Software Mode

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog ground.
AVDD	2	P	Internally regulated 5V analog supply voltage. This pin must not be used to drive external devices.
GVDD	3	P	Gate drive internal regulator output. This pin must not be used to drive external devices.
$\overline{PDN}$	4	DI	Power down, active-low. $\overline{PDN}$ place the amplifier in Shutdown, turn off all internal regulators.
SCL	5	DI	I^2C serial control clock input.
SDA	6	DI/O	I^2C serial control data interface input/output.
SDIN	7	DI	Data line to the serial data port.
BCLK	8	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
LRCLK	9	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
GPIO2	10	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x62h). Can be configured to be open drain output or push-pull output.
GPIO1	11	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x61h). Can be configured to be open drain output or push-pull output.
GPIO0	12	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x63h). Can be configured to be open drain output or push-pull output.
ADR	13	AI	A table of resistor value (Pull down to GND) decides the device I2C address. See Table 7-7.
VR_DIG	14	P	Internally regulated 1.5V digital supply voltage. This pin must not be used to drive external devices.

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Table 4-1. Pin Functions - Software Mode (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DVDD	15	P	3.3V or 1.8V digital power supply.
DGND	16	G	Digital ground.
PVDD	17	P	PVDD voltage input.
	18	P	
	31	P	
	32	P	
PGND	21	G	Ground reference for power device circuitry. Connect this pin to system ground.
	22	G	
	27	G	
	28	G	
OUT_A+	19	PO	Positive pin for differential speaker amplifier output A.
BST_A+	20	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+.
OUT_A-	23	PO	Negative pin for differential speaker amplifier output A.
BST_A-	24	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-.
BST_B-	25	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-.
OUT_B-	26	PO	Negative pin for differential speaker amplifier output B.
BST_B+	29	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+.
OUT_B+	30	PO	Positive pin for differential speaker amplifier output B.
PowerPAD™		P	Ground, connect to grounded heat sink for best system performance.

(1) AI = Analog input, PO = Power output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0V)

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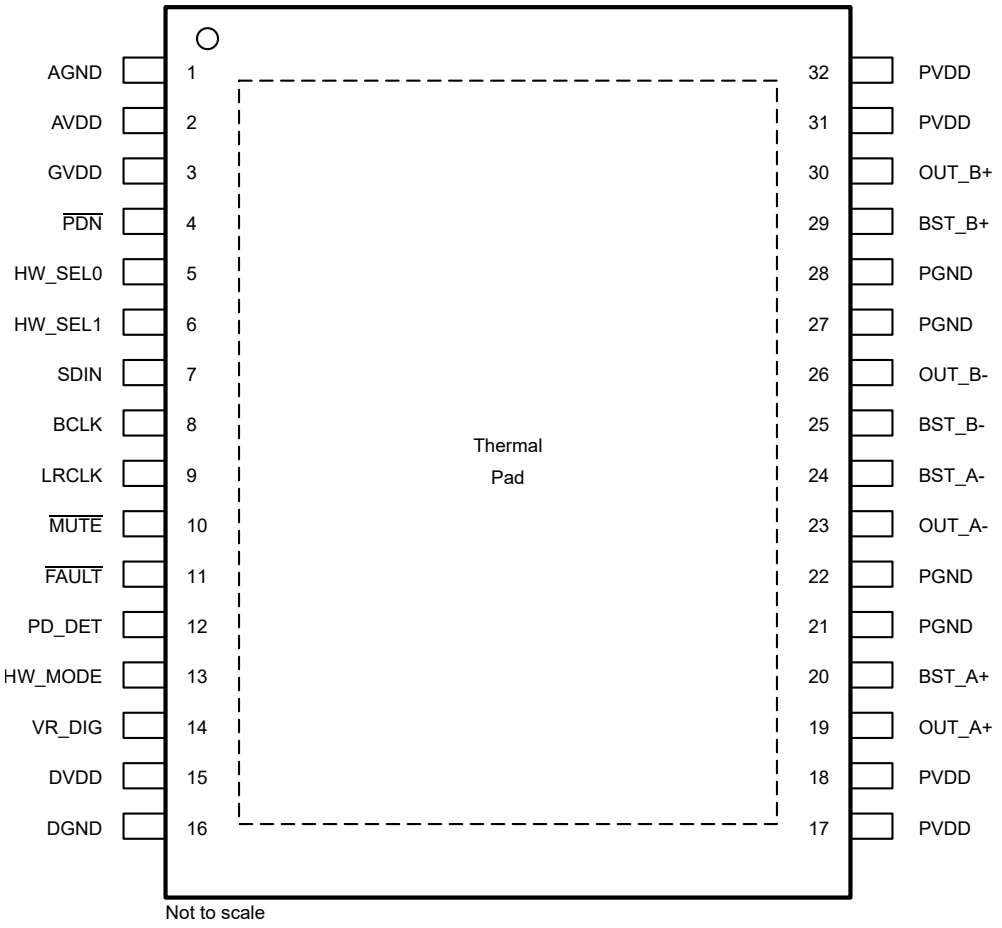

Figure 4-2. DAD (TSSOP) Package, 32-Pin PadUp, Hardware Mode,Top View

Table 4-2. Pin Functions - Hardware Mode

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog ground.
AVDD	2	P	Internally regulated 5V analog supply voltage. This pin must not be used to drive external devices.
GVDD	3	P	Gate drive internal regulator output. This pin must not be used to drive external devices.
PDN	4	DI	Power down, active-low. PDN place the amplifier in Shutdown, turn off all internal regulators.
HW_SEL0	5	DI	Analog gain and BTL/PBTL mode selection in Hardware Mode . Pull up to DVDD or Pull down to ground with different resistor. See Table 7-6.
HW_SEL1	6	DI	PWM Switching Frequency and Spread Spectrum Enable/Disable selection in Hardware Mode. Pull up to DVDD or Pull down to ground with different resistor. See Table 7-5.
SDIN	7	DI	Data line to the serial data port.
BCLK	8	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
LRCLK	9	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
MUTE	10	DI	Speaker amplifier Mute. Which must be pulled low (connect to DGND) to MUTE the device and pulled high (connected to DVDD) to exit MUTE state. In Mute state, device output keep in Hi-Z state.
FAULT	11	DO	Fault terminal,which is pulled LOW when an internal fault occurs.
PD_DET	12	DO	PVDD Drop detection, which is pulled LOW when the PVDD drop below 8V.
HW_MODE	13	AI	Connect to DVDD directly to maintain device enter into Hardware Control Mode.
VR_DIG	14	P	Internally regulated 1.5V digital supply voltage. This pin must not be used to drive external devices.
DVDD	15	P	3.3V or 1.8V digital power supply.

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Table 4-2. Pin Functions - Hardware Mode (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DGND	16	G	Digital ground.
PVDD	17	P	PVDD voltage input.
	18	P	
	31	P	
	32	P	
PGND	21	G	Ground reference for power device circuitry. Connect this pin to system ground.
	22	G	
	27	G	
	28	G	
OUT_A+	19	PO	Positive pin for differential speaker amplifier output A.
BST_A+	20	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+.
OUT_A-	23	PO	Negative pin for differential speaker amplifier output A.
BST_A-	24	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-.
BST_B-	25	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-.
OUT_B-	26	PO	Negative pin for differential speaker amplifier output B.
BST_B+	29	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+.
OUT_B+	30	PO	Positive pin for differential speaker amplifier output B.
PowerPAD™		P	Ground, connect to grounded heat sink for best system performance.

(1) AI = Analog input, PO = Power output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0V)

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5 Specifications

5.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	30	V
$V_{I(DigIn)}$	DVDD referenced digital inputs(2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
T_A	Ambient operating temperature	–40	85	°C
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SDIN, SDOUT, SCL, SDA, $\overline{\text{PDN}}$

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002.(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	PVDD	4.5		26.4	V
		DVDD	1.62		3.63	V
R_{SPK}	Minimum Speaker Load	4.5V-24V Operating PVDD Range, BTL Mode	3.2			Ω
		4.5V-24V Operating PVDD Range, PBTL Mode	1.6			Ω
$V_{IH(DigIn)}$	Input logic high for DVDD referenced digital inputs		0.9 × V_{DVDD}		DVDD	V
$V_{IL(DigIn)}$	Input logic low for DVDD referenced digital inputs				0.1 × V_{DVDD}	V
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1			µH

5.4 Thermal Information

THERMAL METRIC(1)		TSSOP32 (DAD) - 32 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
$R_{\theta JA(top)}$	Junction-to-case (top) thermal resistance	62.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.5	°C/W
$R_{\theta JB(top)}$	Junction-to-board thermal resistance	33.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = V_{DVDD}$			10	uA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = 0V$			–10	uA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	I_{OH} = 4mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	I_{OH} = –4mA			20%	V_{DVDD}
I^2C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I^2C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required LRCLK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		192	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
AMPLIFIER OPERATING MODE AND DC PRAMETERS						
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2V, DVDD = 3.3V, Play mode, General Audio Process flow with full DSP running		23		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2V, DVDD = 3.3V,Sleep mode		1		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2V, DVDD = 3.3V,Deep Sleep mode		1		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 0.8V, DVDD = 3.3V,Shutdown mode		16		uA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2V, PVDD = 18V, No Load, LC filter = 10μH + 0.68μF, FSW = 384kHz, 1SPW Modulation, Play Mode		39		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2V, PVDD = 18V, No Load, LC filter = 10μH + 0.68μF, FSW = 384kHz, Output Hiz Mode		11		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2V, PVDD = 18V, No Load, LC filter = 10μH + 0.68μF, FSW = 384kHz, Sleep Mode		7.5		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2V, PVDD = 18V, No Load, LC filter = 10μH + 0.68μF, FSW = 384kHz, Deep Sleep Mode		10		uA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2V, PVDD = 18V, No Load, LC filter = 10μH + 0.68μF, FSW = 384kHz, Shutdown Mode		10		uA
$A_{V(SPK_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD. Measured at 0dB input(1FS)	13.75		29.4	dBV
$\Delta A_{V(SPK_AMP)}$	Amplifier gain error	Gain = 26.4dBV		0.5		dB

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5.5 Electrical Characteristics (continued)

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Software Mode		384		kHz
				480		kHz
				768		kHz
		Hardware Mode		480		kHz
				768		kHz
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization. V_{PVDD}=24V, $I_{(OUT)}$=500mA, T_J=25℃		90		mΩ
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold (Speaker current)	Speaker Output Current (Post LC filter), Speaker current, LC Filter=10uH+0.68uF, BTL Mode	7.5	8	8.5	A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold		3.7	4	4.2	V
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold		27	28.1	29.2	V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		1.7		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		570		ms
OTE_{THRES}	Over temperature error threshold			165		℃
$OTE_{Hystersis}$	Over temperature error hysteresis			10		℃
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit0		112		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit1		122		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit2		134		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit3		146		°C

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5.5 Electrical Characteristics (continued)

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMACNE (STEREO BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4dBV analog gain, V_{PVDD} range:12V~24V	–5		5	mV
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 18V, LC Filter=10uH+0.68uF, R_{SPK} = 4Ω, f = 1 KHz, THD+N = 10%		43		W
		V_{PVDD} = 18V, LC Filter=10uH+0.68uF, R_{SPK} = 4Ω, f = 1 KHz, THD+N = 1%		35		W
		V_{PVDD} = 18V, LC Filter=10uH+0.68uF, R_{SPK} = 6Ω, f = 1 KHz, THD+N = 10%		31		W
		V_{PVDD} = 18V, LC Filter=10uH+0.68uF, R_{SPK} = 6Ω, f = 1 KHz, THD+N = 1%		25		W
		V_{PVDD} = 21V, LC Filter=10uH+0.68uF, R_{SPK} = 4Ω, f = 1 KHz, THD+N = 10%		55		W
		V_{PVDD} = 21V, LC Filter=10uH+0.68uF, R_{SPK} = 4Ω, f = 1 KHz, THD+N = 1%		44		W
		V_{PVDD} = 24V, LC Filter=10uH+0.68uF, R_{SPK} = 6Ω, f = 1 KHz, THD+N = 10%		54		W
		V_{PVDD} = 24V, LC Filter=10uH+0.68uF, R_{SPK} = 6Ω, f = 1 KHz, THD+N = 1%		43		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1W, f = 1 KHz)	V_{PVDD} = 18V,LC Filter=10uH+0.68uF, Load=4Ω		0.08		%
		V_{PVDD} = 24V,LC Filter=10uH+0.68uF,Load=6Ω		0.06		%
$ICN_{(SPK)}$	Idle channel noise(Aweighted, AES17)	V_{PVDD} = 18V, LC Filter=10uH+0.68uF, Load=4Ω, Fsw=768kHz, BD Modulation		40		μVrms
		V_{PVDD} = 18V, LC Filter=10uH+0.68uF,Load=4Ω, Fsw=384kHz, 1SPW Modulation		35		μVrms
		V_{PVDD} = 24V, LC Filter=10uH+0.68uF,,Load=6Ω, Fsw=768kHz, BD Modulation		35		μVrms
		V_{PVDD} = 24V, LC Filter=10uH+0.68uF, Load=6Ω, Fsw=384kHz, 1SPW Modulation		35		μVrms
DR	Dynamic range	A-Weighted, -60dBFS method. V_{PVDD} = 24V, Load = 6Ω Analog Gain = 29.4dBV		111		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=24V, load=6Ω		111		dB
		A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=18V, Load=4Ω		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 Vrms, V_{PVDD} = 24V, input audio signal = digital zero		72		dB
$X\text{-}talk_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 KHz, based on Inductor (DFEG7030D-4R7) from Murata		100		dB

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5.5 Electrical Characteristics (continued)

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE (MONO PBTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4dBV Analog gain, V_{PVDD} = 12V-24V range, 1SPW mode	–5		5	mV
$P_{O(SPK)}$	Output Power	V_{PVDD} = 24V, R_{SPK} = 3Ω, f = 1KHz, THD+N = 1%		84		W
		V_{PVDD} = 24V, R_{SPK} = 3Ω, f = 1KHz, THD+N = 10%		104		W
		V_{PVDD} = 18V, R_{SPK} = 2Ω, f = 1KHz, THD+N = 1%		67		W
		V_{PVDD} = 18V, R_{SPK} = 2Ω, f = 1KHz, THD+N = 10%		80		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1W, f = 1 KHz)	V_{PVDD} = 18V, LC-filter=10uH+0.68uF, R_{SPK} = 2Ω		0.07		%
		V_{PVDD} = 24V, LC-filter=10uH+0.68uF, R_{SPK} = 3Ω		0.05		%
DR	Dynamic range	A-Weighted, -60dBFS method, V_{PVDD}=24V, R_{SPK} = 3Ω.		111		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=24V, R_{SPK} = 3Ω		108		dB
		A-Weighted,referenced to 1% THD+N Output Level, V_{PVDD}=18V, R_{SPK} = 2Ω		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 Vrms,V_{PVDD} = 18V, input audio signal = digital zero		72		dB

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5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing - Target Mode					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCLK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I²C Bus Timing – Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			µs
t_{S-HD}	Hold time for (repeated) START condition	4			µs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		3450	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{P-SU}	Setup time for STOP condition	4			µs
C_b	Capacitive load for each bus line			400	pf
I²C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated)START condition	600			ns
t_{RS-HD}	Hold time for (repeated)START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_b	Capacitive load for each bus line			400	pf

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5.7 Typical Characteristics

5.7.1 Bridge Tied Load (BTL) Configuration Curves with BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Amplifier Loop Bandwidth, LC filter with 10µH / 0.68µF, unless otherwise noted.

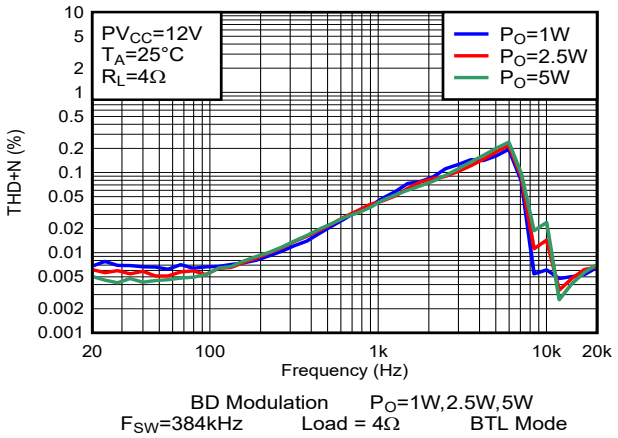

Figure 5-1. THD+N vs Frequency-BTL

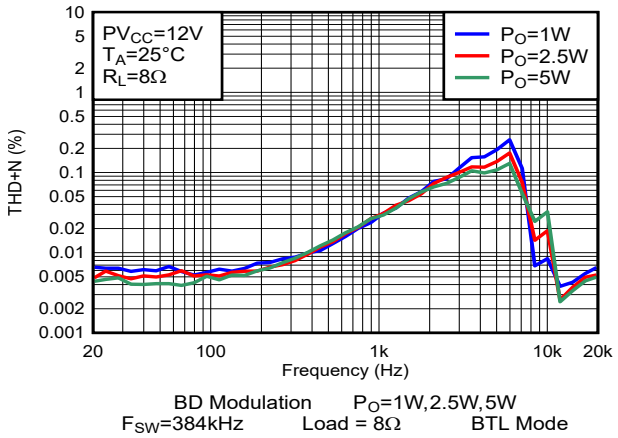

Figure 5-2. THD+N vs Frequency-BTL

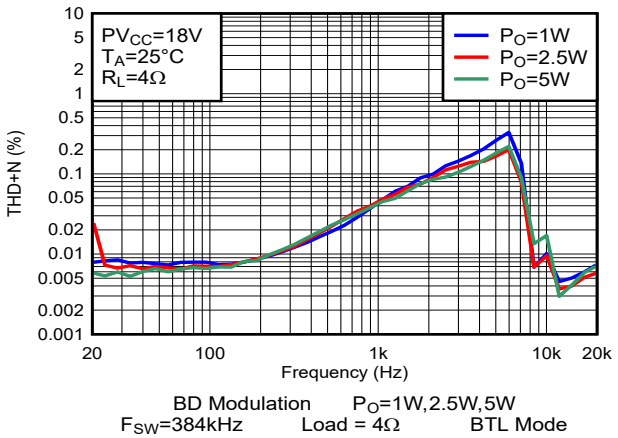

Figure 5-3. THD+N vs Frequency-BTL

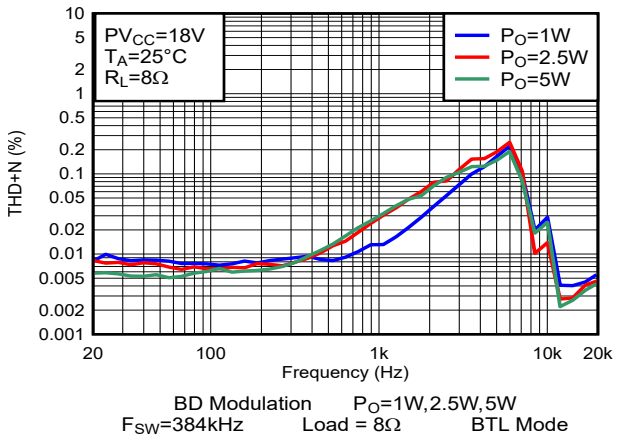

Figure 5-4. THD+N vs Frequency-BTL

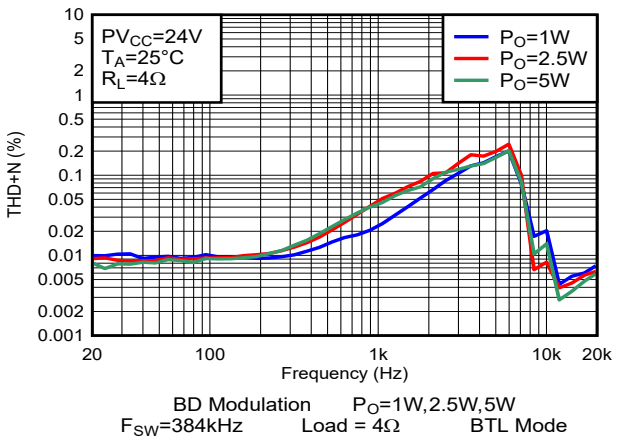

Figure 5-5. THD+N vs Frequency-BTL

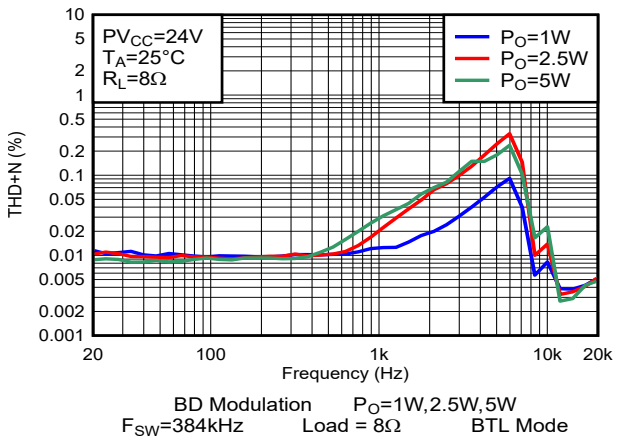

Figure 5-6. THD+N vs Frequency-BTL

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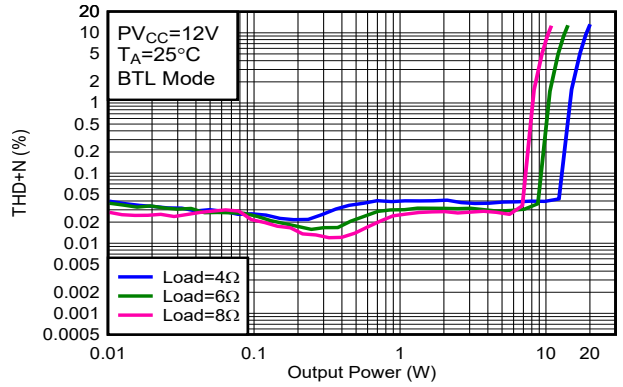

Figure 5-7. THD+N vs Output Power-BTL

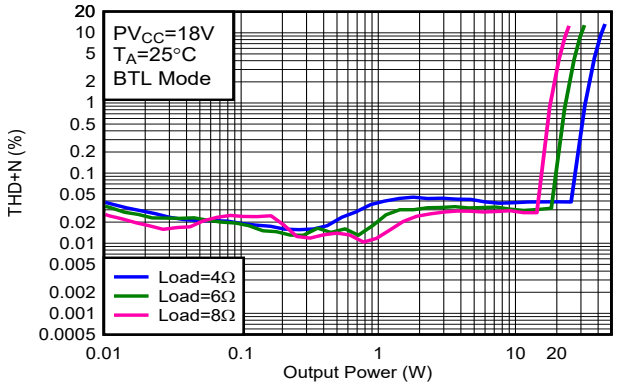

Figure 5-8. THD+N vs Output Power-BTL

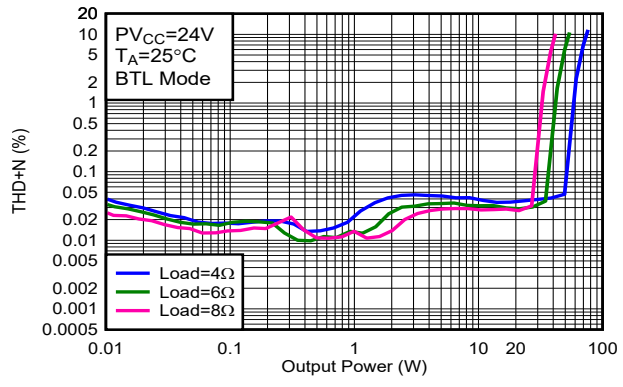

Figure 5-9. THD+N vs Output Power-BTL

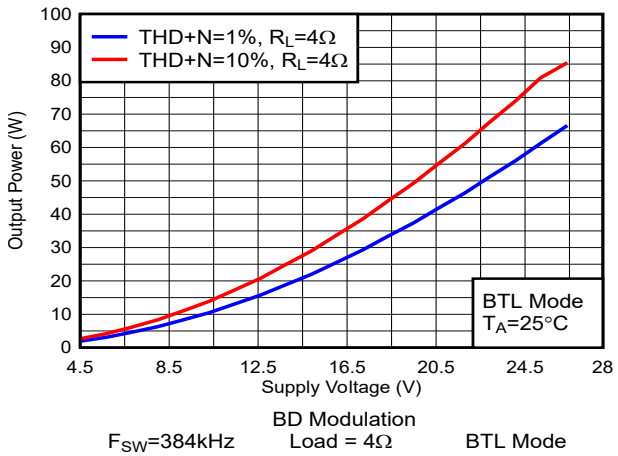

Figure 5-10. Output Power vs Supply Voltage

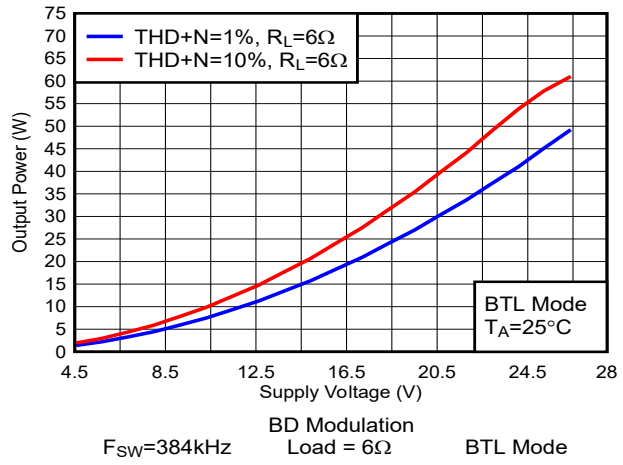

Figure 5-11. Output Power vs Supply Voltage

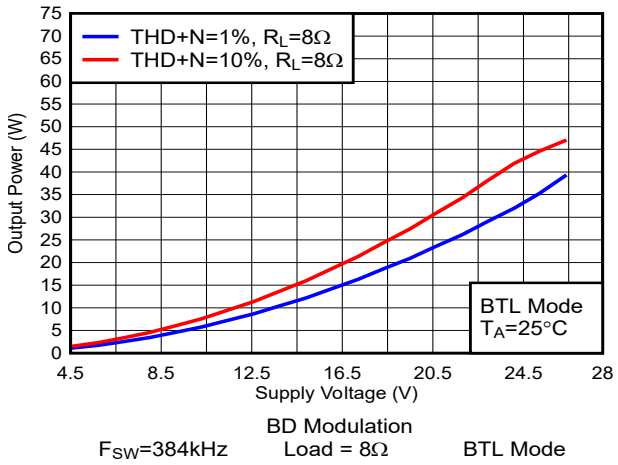

Figure 5-12. Output Power vs Supply Voltage

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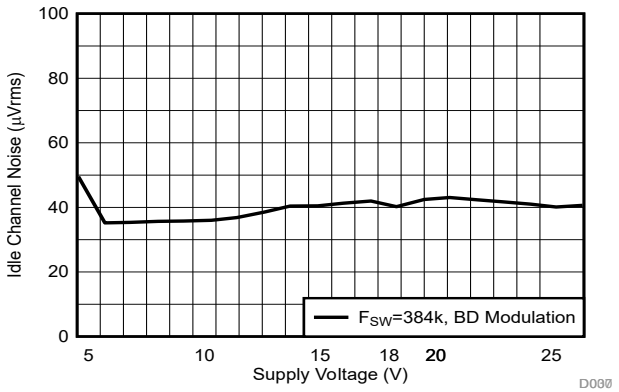
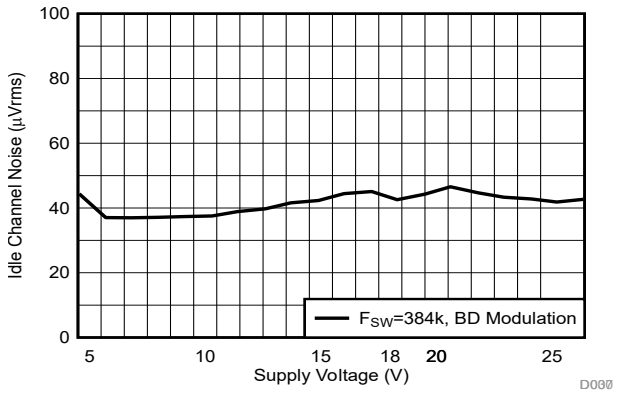


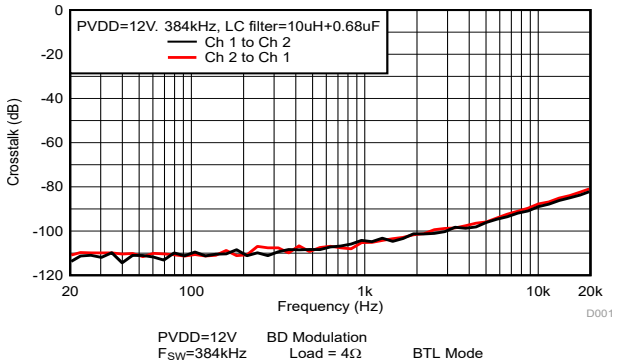
BD Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-13. Idle Channel Noise vs Supply Voltage



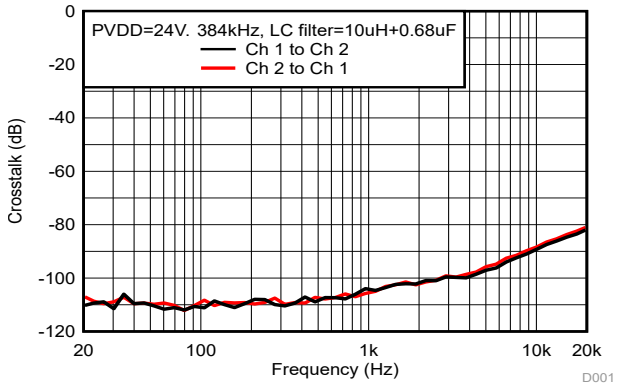
BD Modulation
F_{SW}=384kHz Load = 8Ω BTL Mode

Figure 5-14. Idle Channel Noise vs Supply Voltage



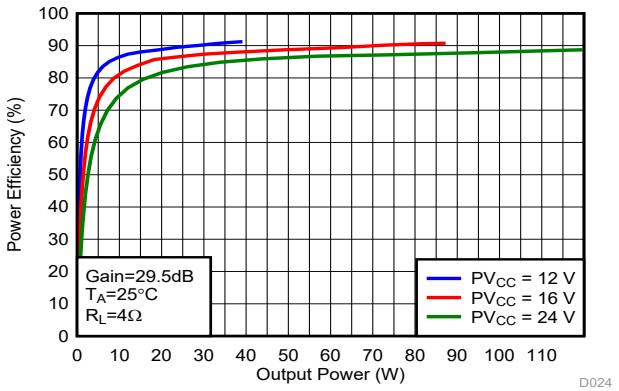
PVDD=12V BD Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-15. Crosstalk



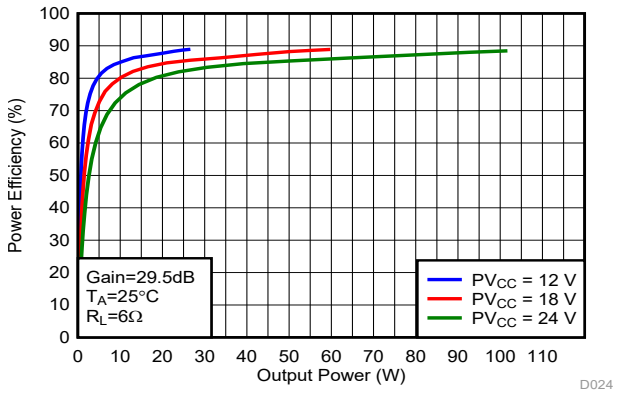
PVDD=24V BD Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-16. Crosstalk



BD Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-17. Efficiency vs Output Power



BD Modulation
F_{SW}=384kHz Load = 6Ω BTL Mode

Figure 5-18. Efficiency vs Output Power

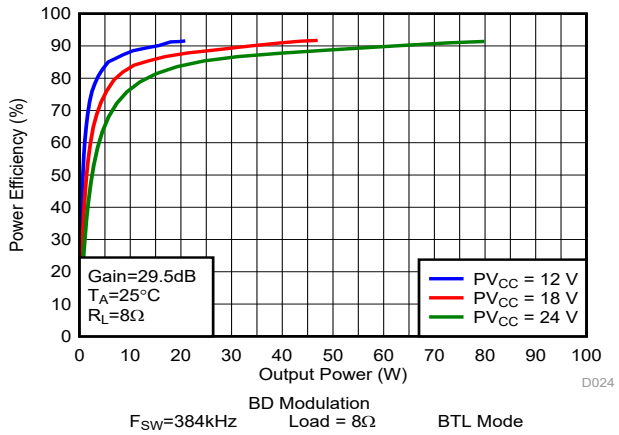


Figure 5-19. Efficiency vs Output Power

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5.7.2 Bridge Tied Load (BTL) Configuration Curves with 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Loop Bandwidth, the LC filter used was 10µH / 0.68µF, unless otherwise noted.

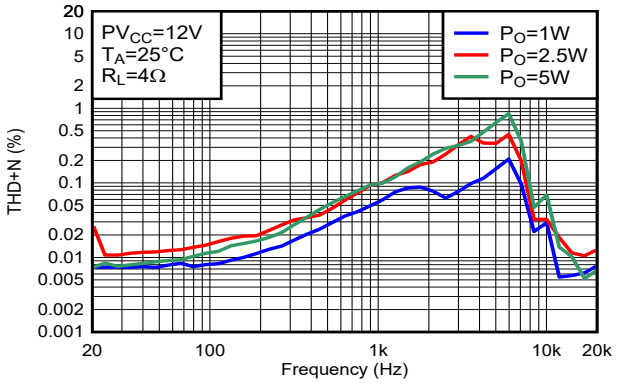

Figure 5-20. THD+N vs Frequency-BTL

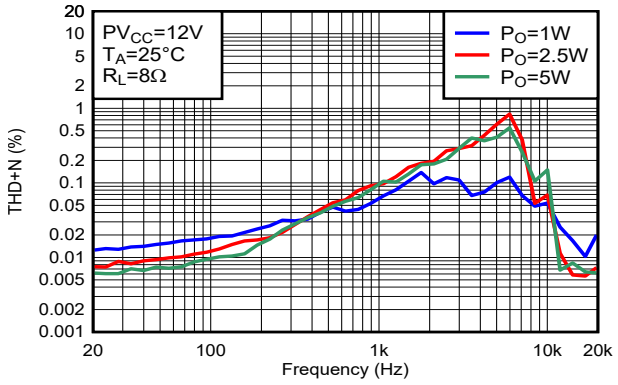

Figure 5-21. THD+N vs Frequency-BTL

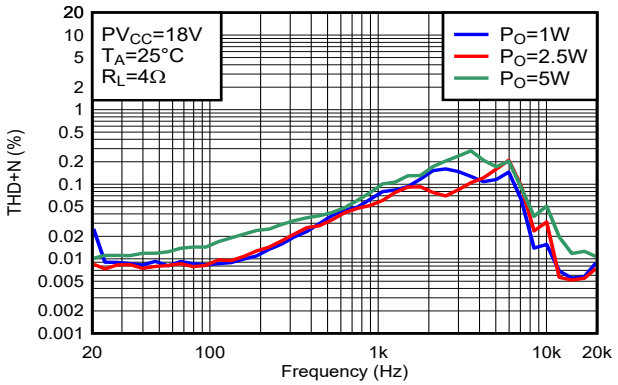

Figure 5-22. THD+N vs Frequency-BTL

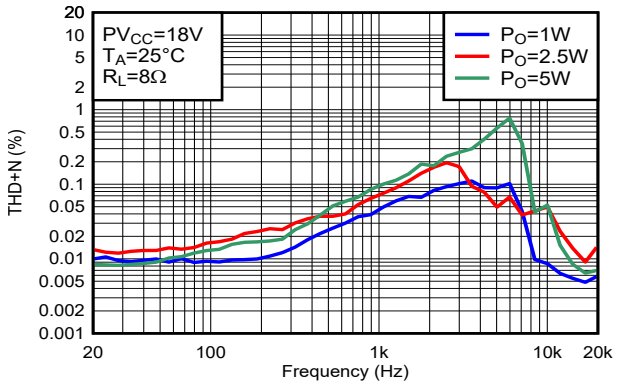

Figure 5-23. THD+N vs Frequency-BTL

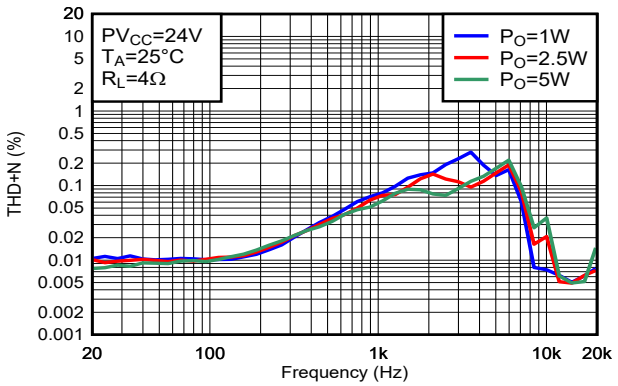

Figure 5-24. THD+N vs Frequency-BTL

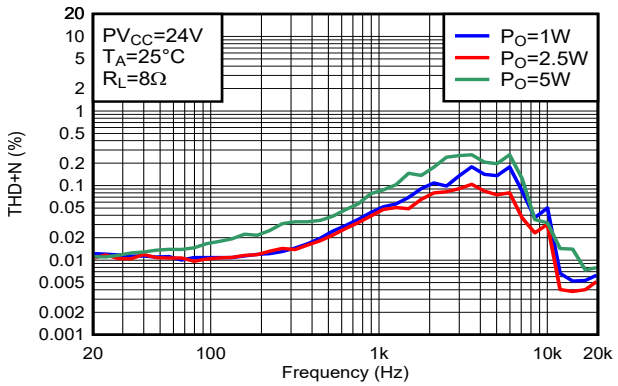

Figure 5-25. THD+N vs Frequency-BTL

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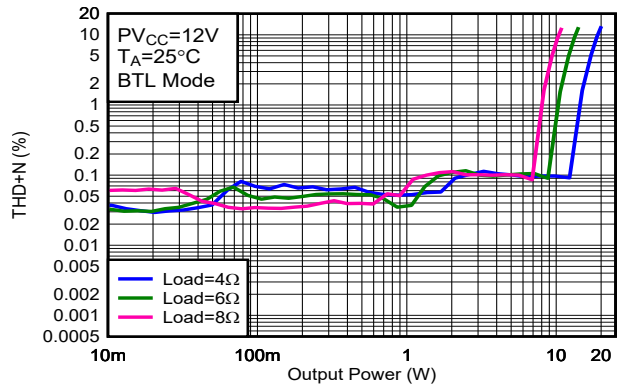

Figure 5-26. THD+N vs Output Power-BTL

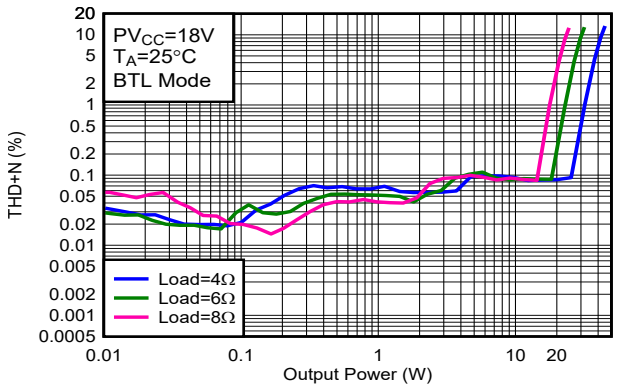

Figure 5-27. THD+N vs Output Power-BTL

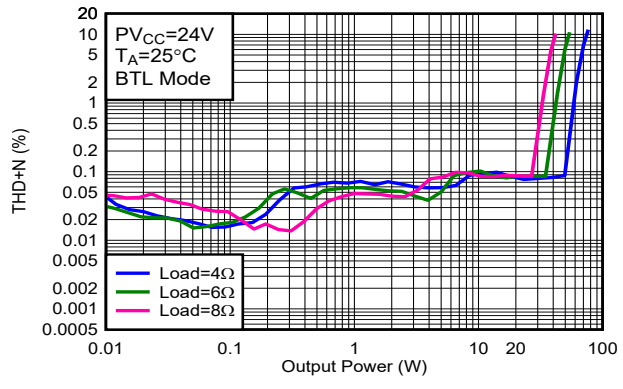

Figure 5-28. THD+N vs Output Power-BTL

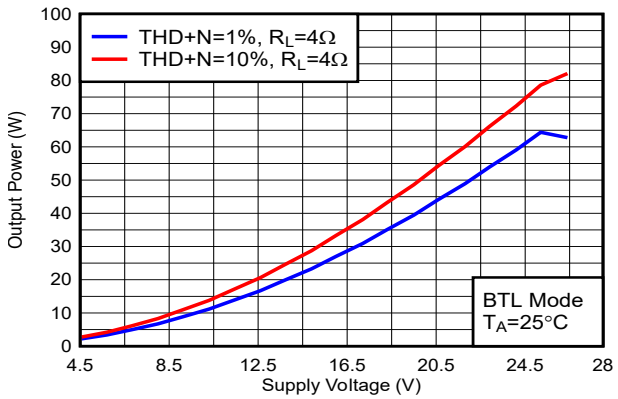

Figure 5-29. Output Power vs Supply Voltage

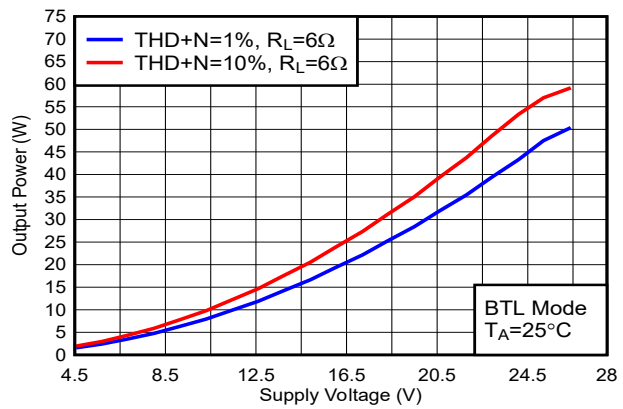

Figure 5-30. Output Power vs Supply Voltage

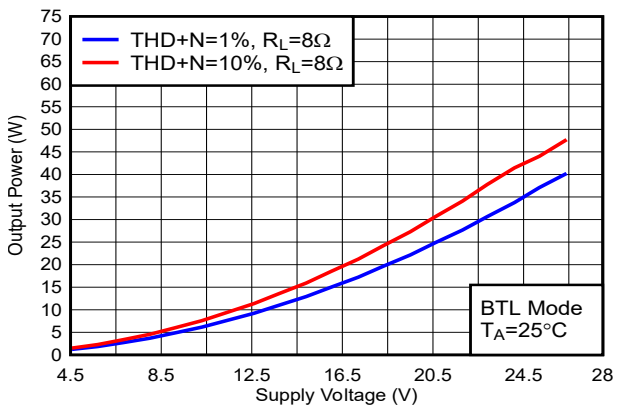

Figure 5-31. Output Power vs Supply Voltage

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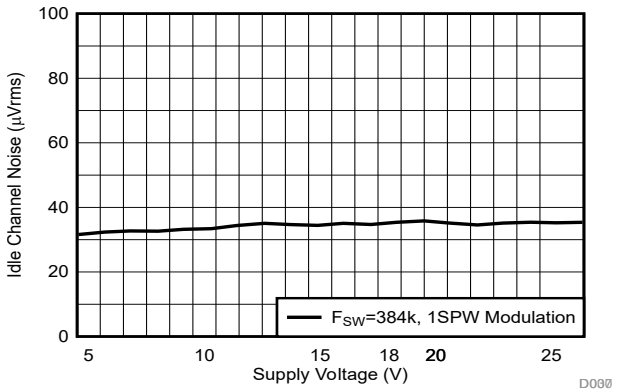
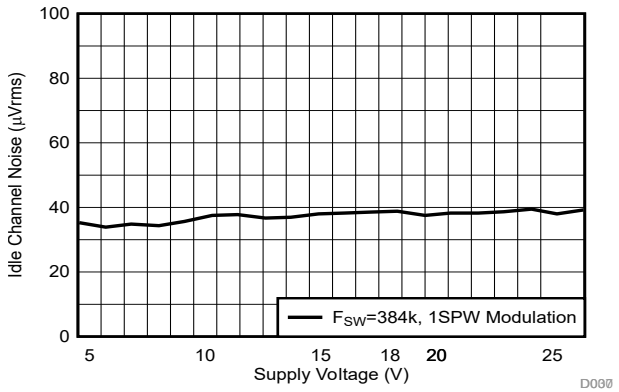


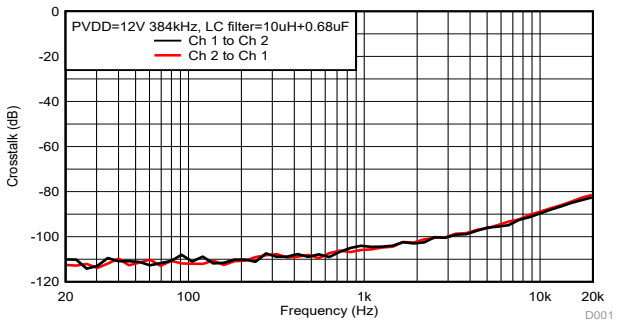
1SPW Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-32. Idle Channel Noise vs Supply Voltage



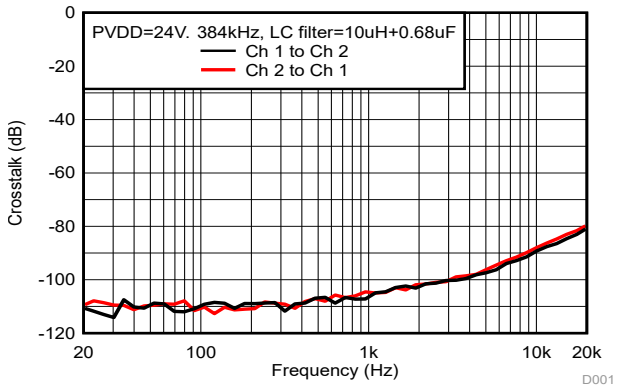
1SPW Modulation
F_{SW}=384kHz Load = 8Ω BTL Mode

Figure 5-33. Idle Channel Noise vs Supply Voltage



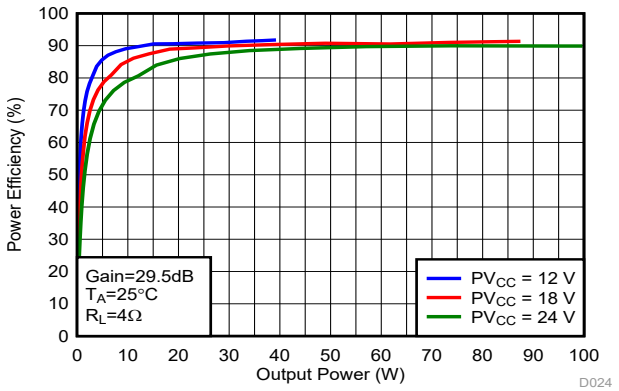
PVDD=12V 1SPW Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-34. Crosstalk



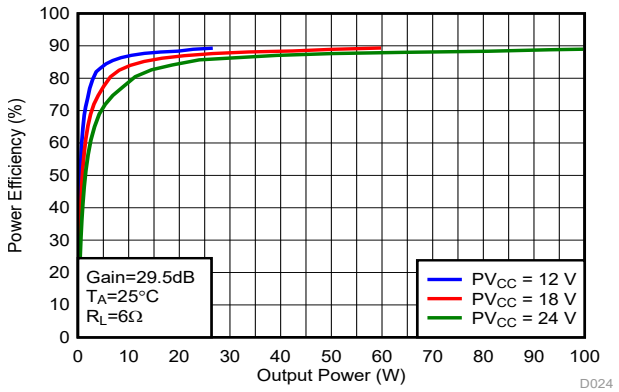
PVDD=24V 1SPW Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-35. Crosstalk - old



1SPW Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode

Figure 5-36. Efficiency vs Output Power



1SPW Modulation
F_{SW}=384kHz Load = 6Ω BTL Mode

Figure 5-37. Efficiency vs Output Power

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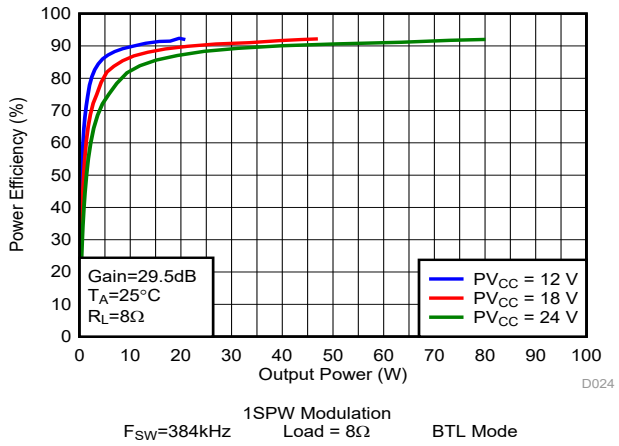

Figure 5-38. Efficiency vs Output Power

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5.7.3 Parallel Bridge Tied Load (PBTL) Configuration With BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Amplifier Loop Bandwidth, LC filter with 10µH / 0.68µF (Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see details in Section 9.2.4) , unless otherwise noted.

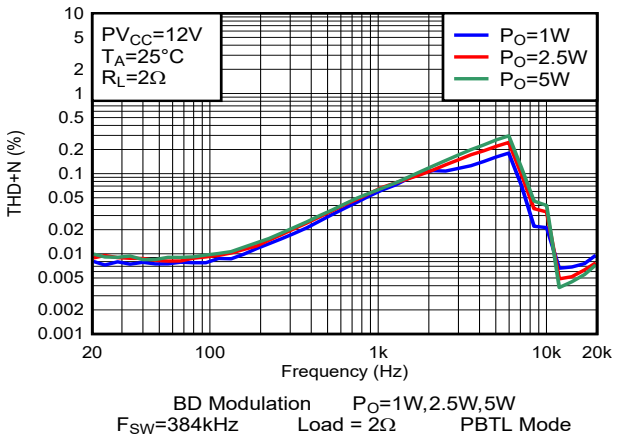

Figure 5-39. THD+N vs Frequency-PBTL

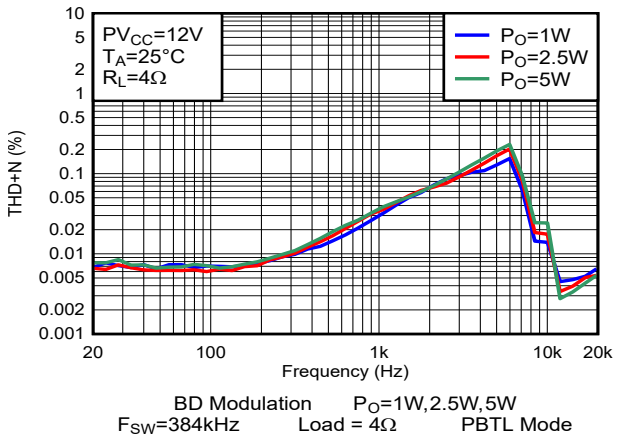

Figure 5-40. THD+N vs Frequency-PBTL

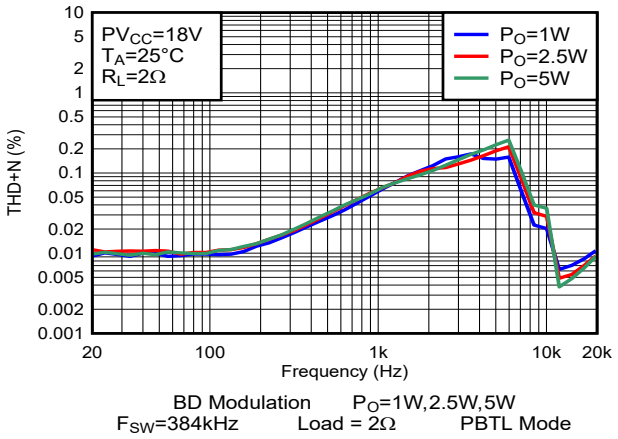

Figure 5-41. THD+N vs Frequency-PBTL

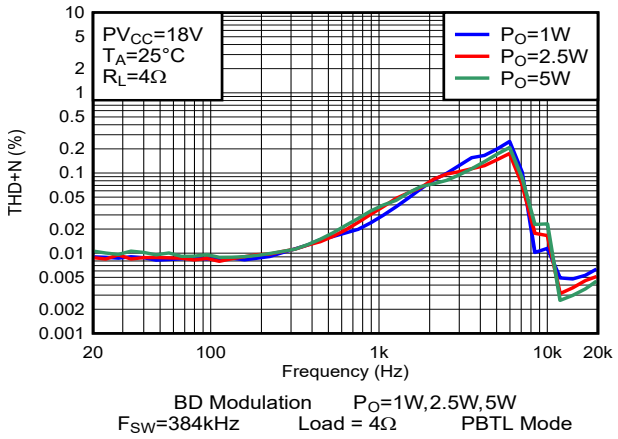

Figure 5-42. THD+N vs Frequency-PBTL

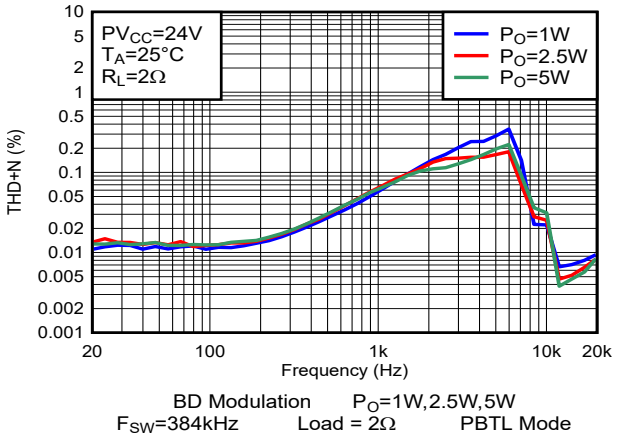

Figure 5-43. THD+N vs Frequency-PBTL

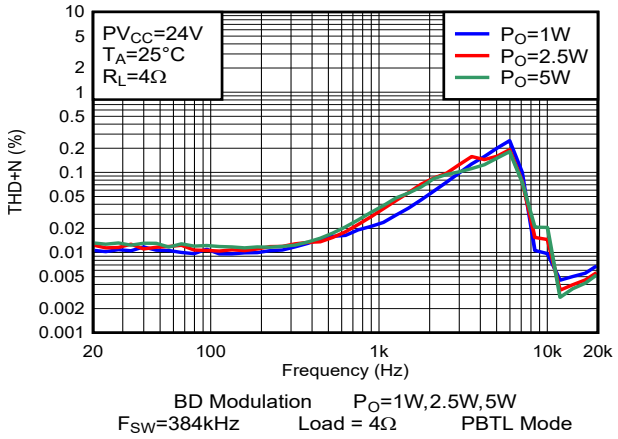

Figure 5-44. THD+N vs Frequency-PBTL

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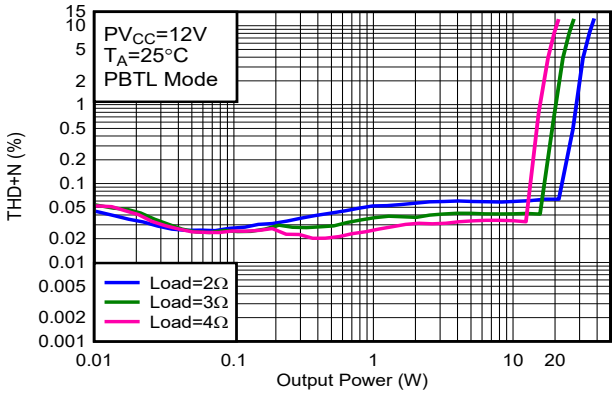

Figure 5-45. THD+N vs Output Power-PBTL

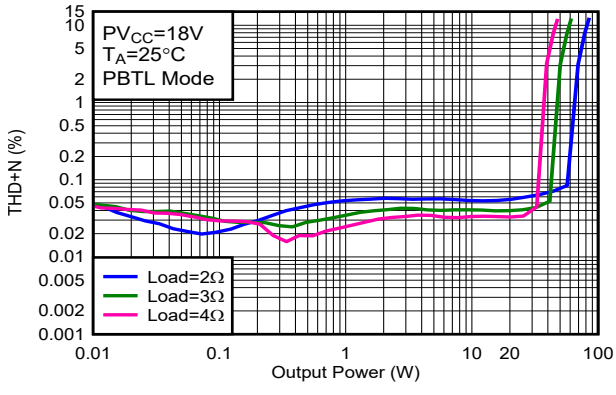

Figure 5-46. THD+N vs Output Power-PBTL

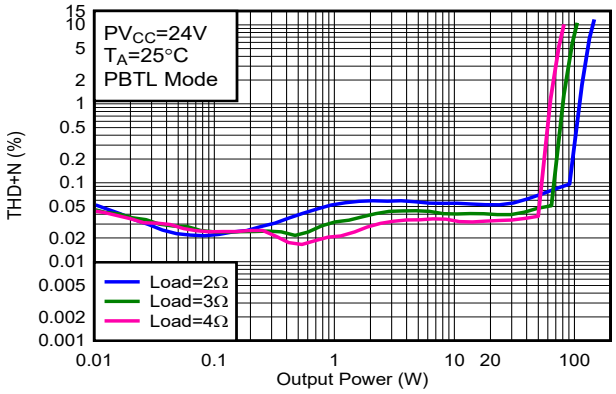

Figure 5-47. THD+N vs Output Power-PBTL

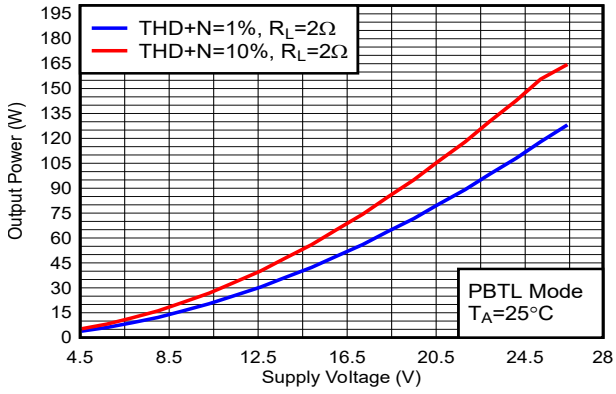

Figure 5-48. Output Power vs Supply Voltage

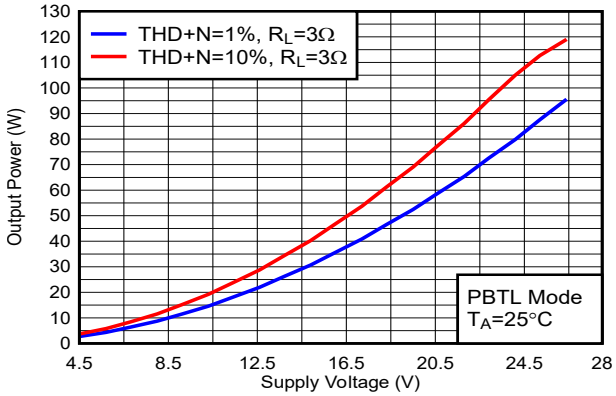

Figure 5-49. Output Power vs Supply Voltage

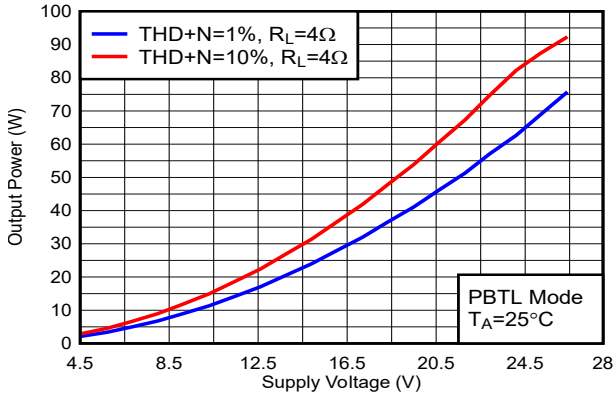

Figure 5-50. Output Power vs Supply Voltage

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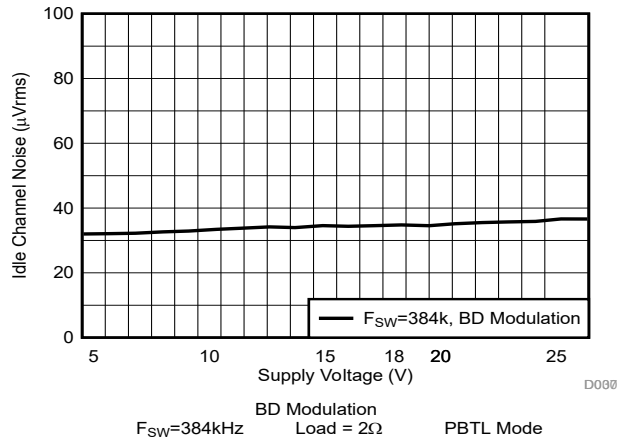
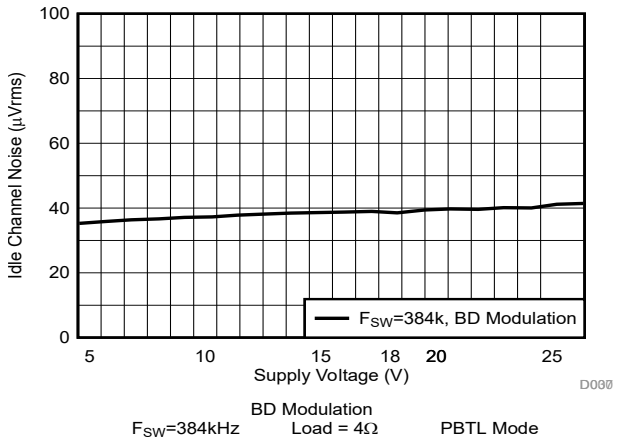


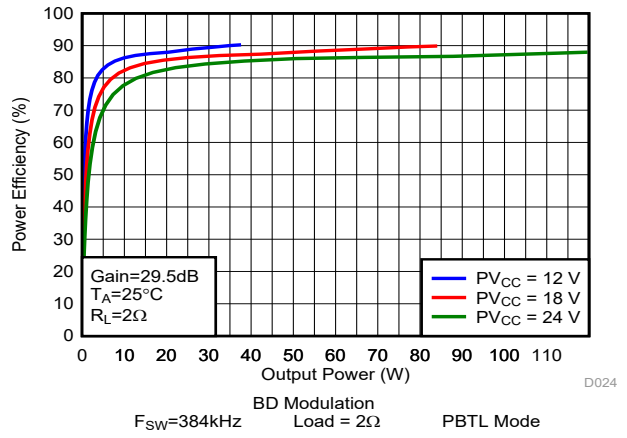
BD Modulation
F_{SW}=384kHz Load = 2Ω PBTL Mode

Figure 5-51. Idle Channel Noise vs Supply Voltage



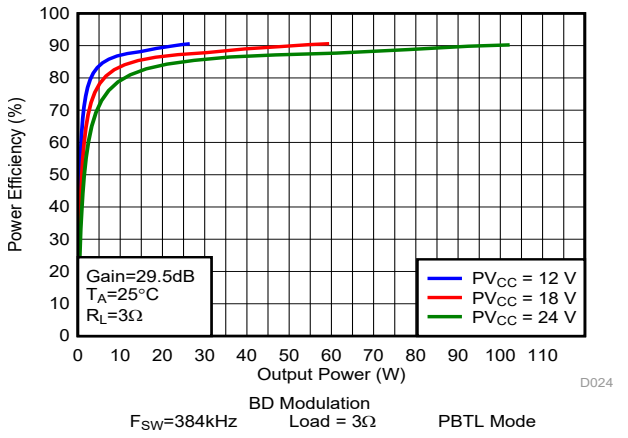
BD Modulation
F_{SW}=384kHz Load = 4Ω PBTL Mode

Figure 5-52. Idle Channel Noise vs Supply Voltage



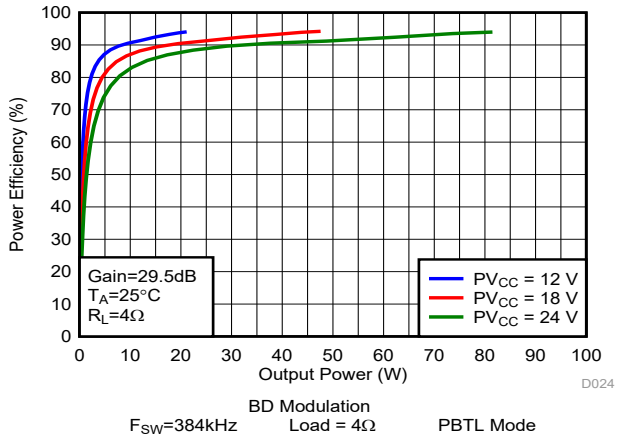
BD Modulation
F_{SW}=384kHz Load = 2Ω PBTL Mode

Figure 5-53. Efficiency vs Output Power



BD Modulation
F_{SW}=384kHz Load = 3Ω PBTL Mode

Figure 5-54. Efficiency vs Output Power



BD Modulation
F_{SW}=384kHz Load = 4Ω PBTL Mode

Figure 5-55. Efficiency vs Output Power

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5.7.4 Parallel Bridge Tied Load (PBTL) Configuration With 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 80kHz Class D Amplifier Loop Bandwidth, the LC filter used was 10µH / 0.68µF (Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see connect method in Section 9.2.4) , unless otherwise noted.

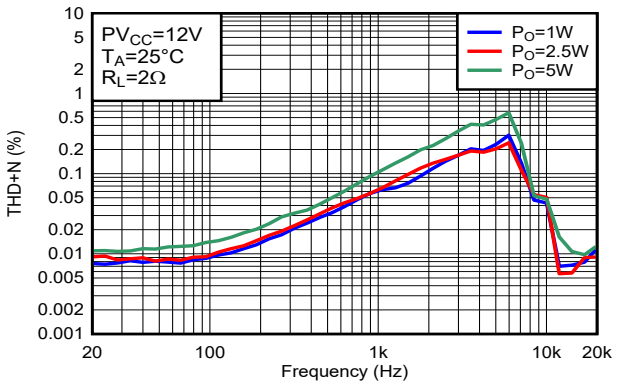

Figure 5-56. THD+N vs Frequency-PBTL

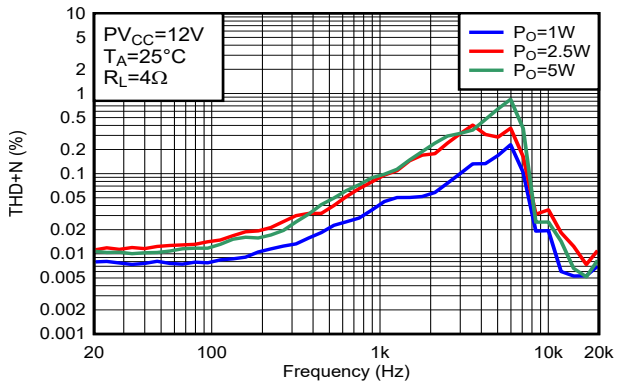

Figure 5-57. THD+N vs Frequency-PBTL

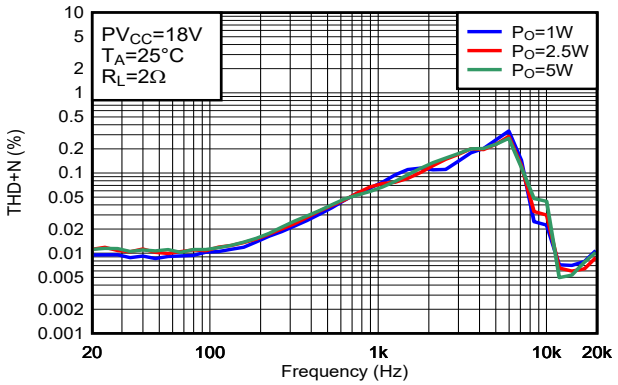

Figure 5-58. THD+N vs Frequency-PBTL

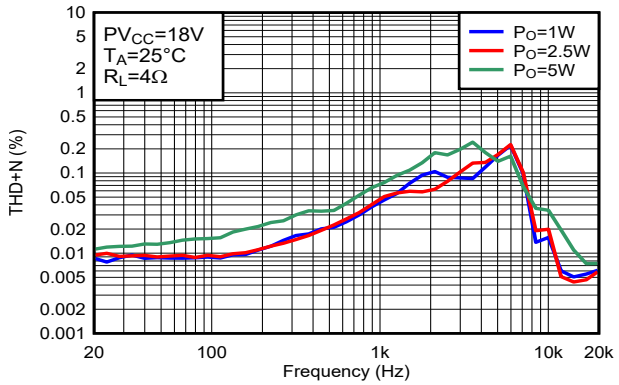

Figure 5-59. THD+N vs Frequency-PBTL

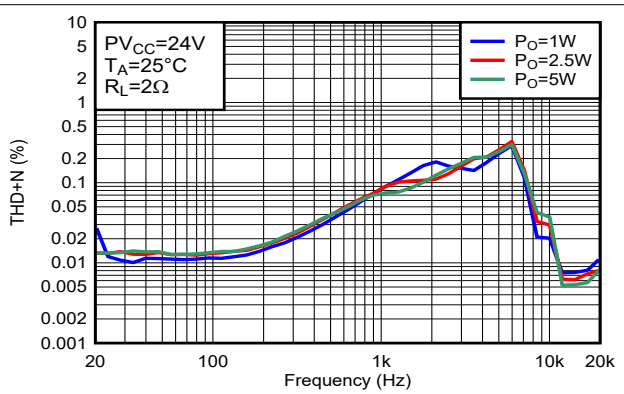

Figure 5-60. THD+N vs Frequency-PBTL

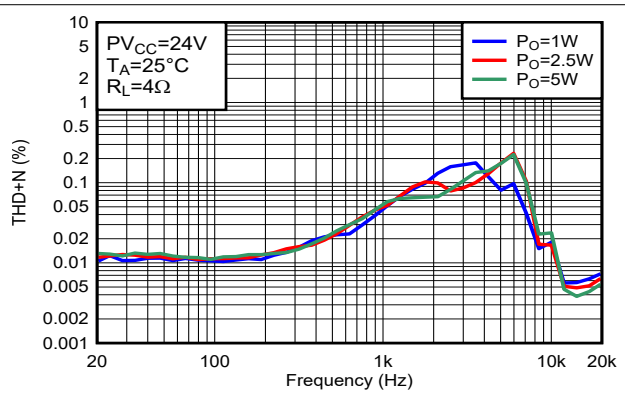

Figure 5-61. THD+N vs Frequency-PBTL

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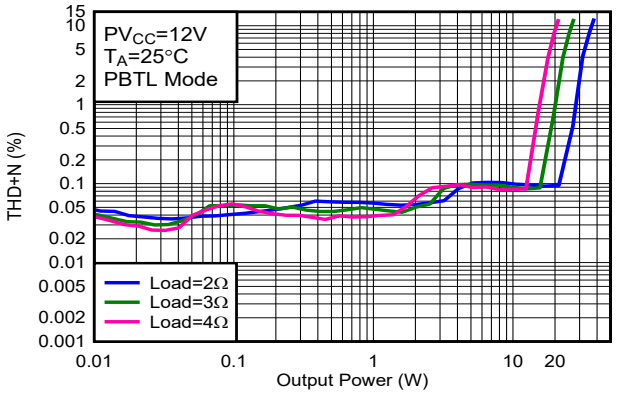

Figure 5-62. THD+N vs Output Power-PBTL

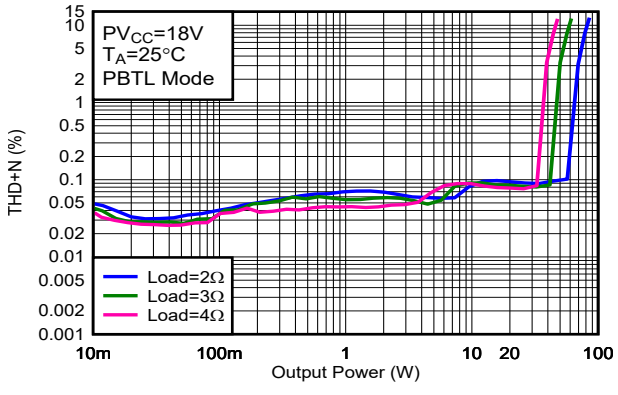

Figure 5-63. THD+N vs Output Power-PBTL

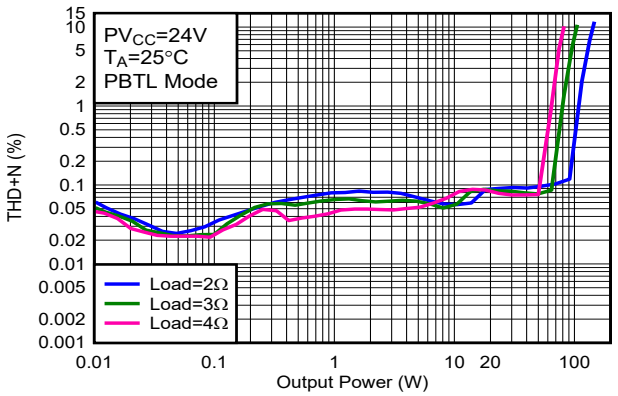

Figure 5-64. THD+N vs Output Power-PBTL

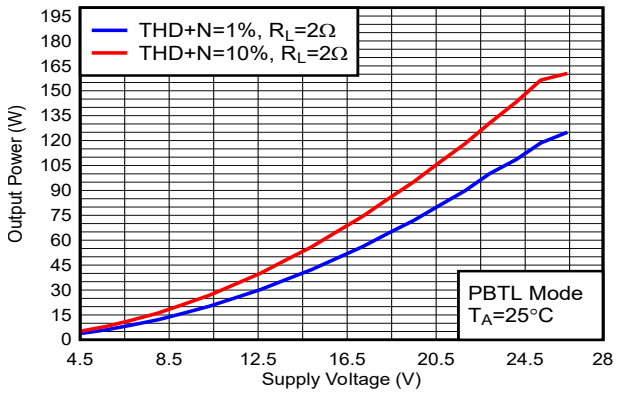

Figure 5-65. Output Power vs Supply Voltage

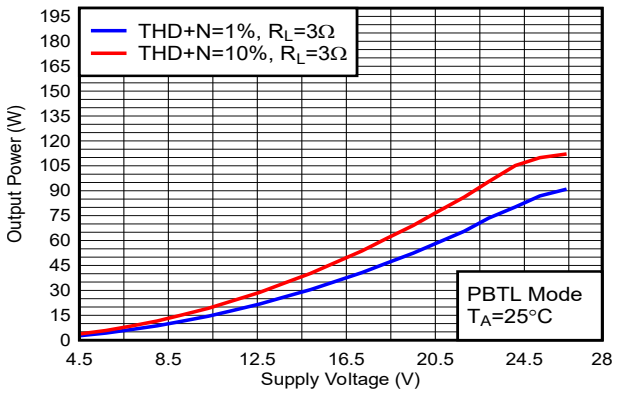

Figure 5-66. Output Power vs Supply Voltage

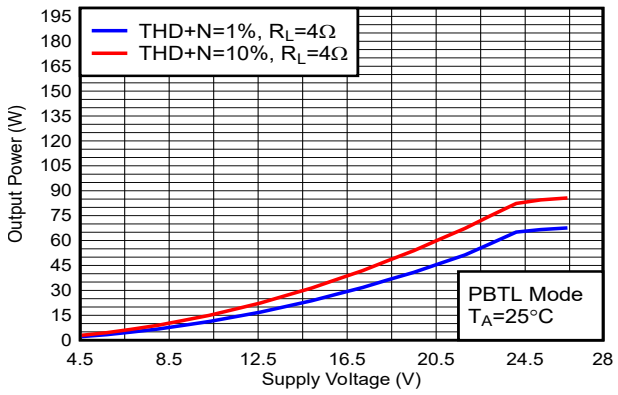

Figure 5-67. Output Power vs Supply Voltage

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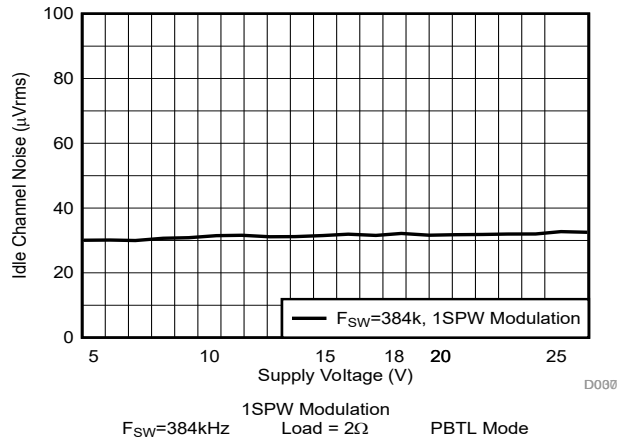
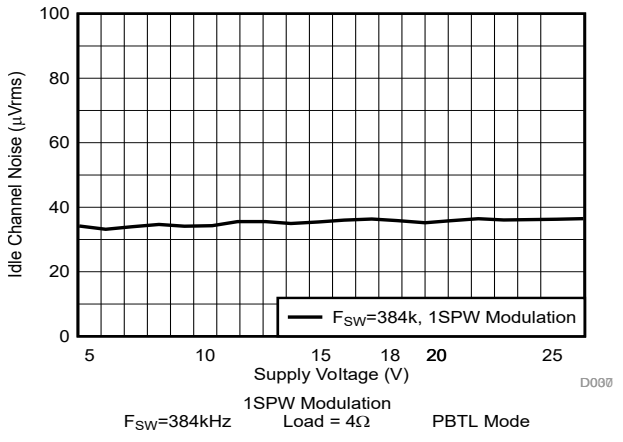


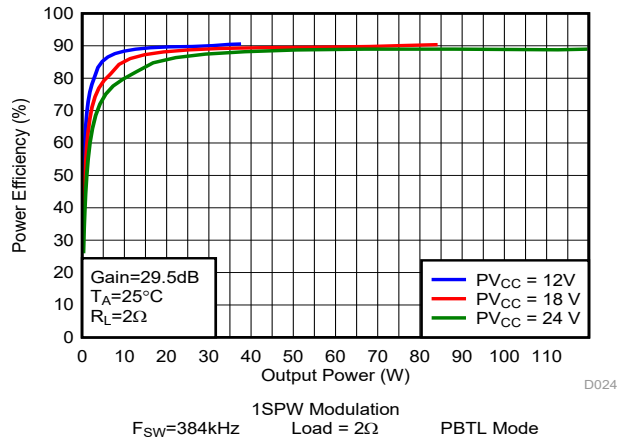
1SPW Modulation
F_{SW}=384kHz Load = 2Ω PBTL Mode

Figure 5-68. Idle Channel Noise vs Supply Voltage



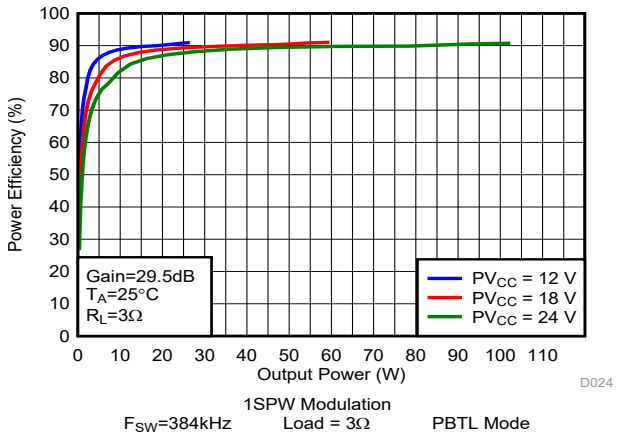
1SPW Modulation
F_{SW}=384kHz Load = 4Ω PBTL Mode

Figure 5-69. Idle Channel Noise vs Supply Voltage



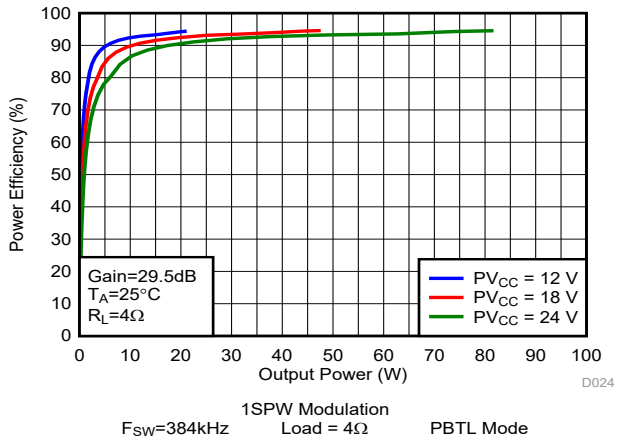
1SPW Modulation
F_{SW}=384kHz Load = 2Ω PBTL Mode

Figure 5-70. Efficiency vs Output Power



1SPW Modulation
F_{SW}=384kHz Load = 3Ω PBTL Mode

Figure 5-71. Efficiency vs Output Power



1SPW Modulation
F_{SW}=384kHz Load = 4Ω PBTL Mode

Figure 5-72. Efficiency vs Output Power

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6 Parameter Measurement Information

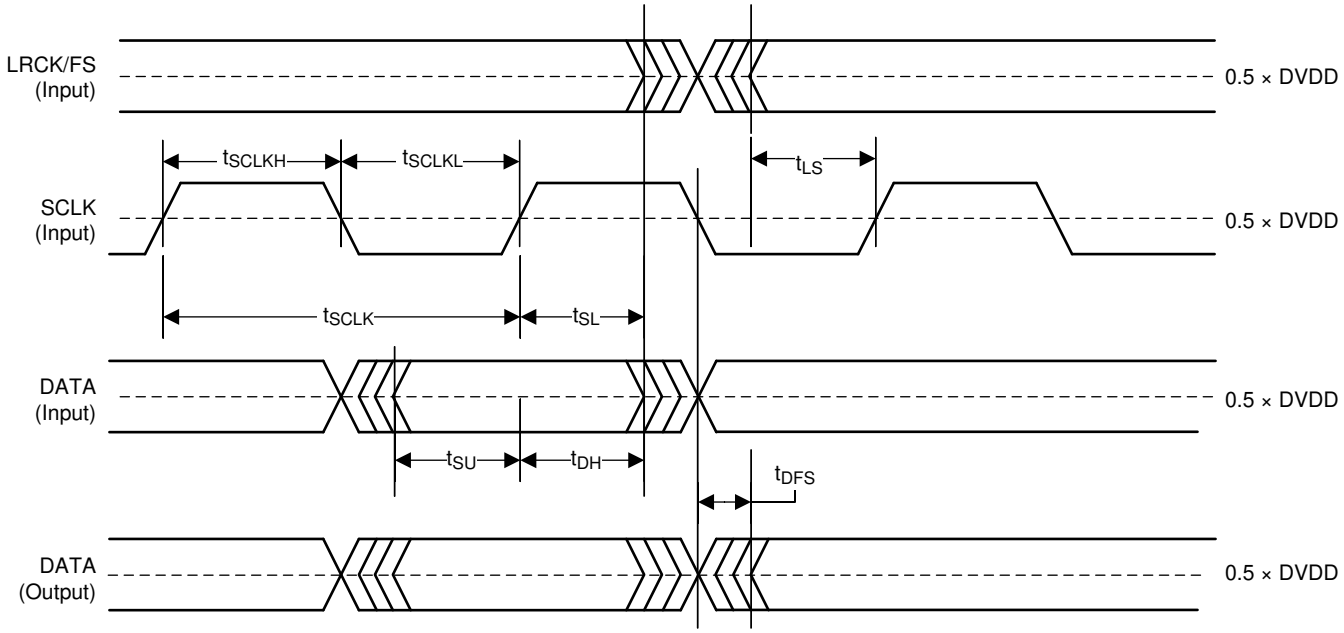


Figure 6-1. Serial Audio Port Timing in Target Mode

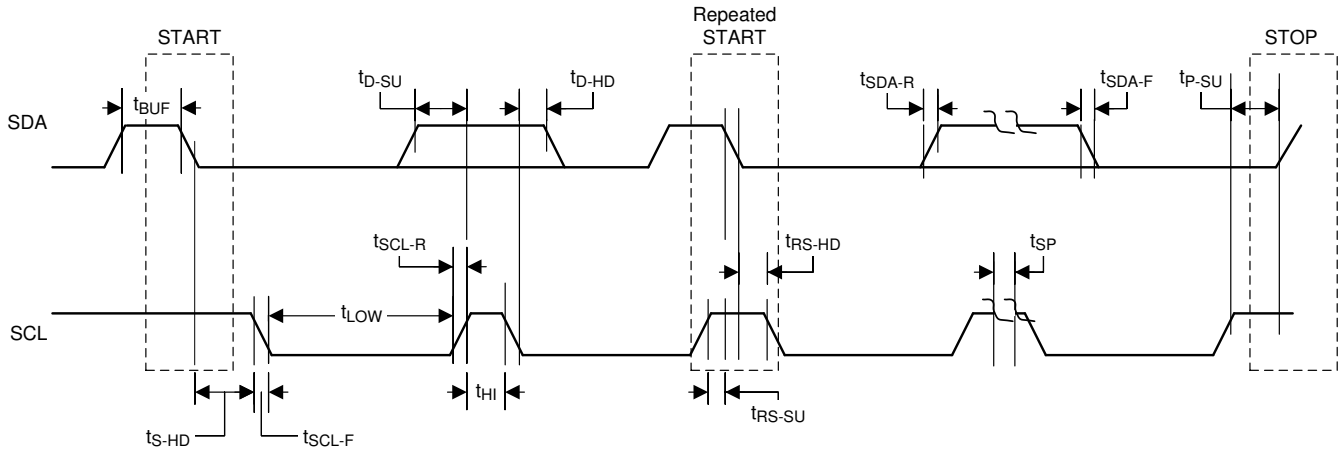


Figure 6-2. I²C Communication Port Timing Diagram

7 Detailed Description

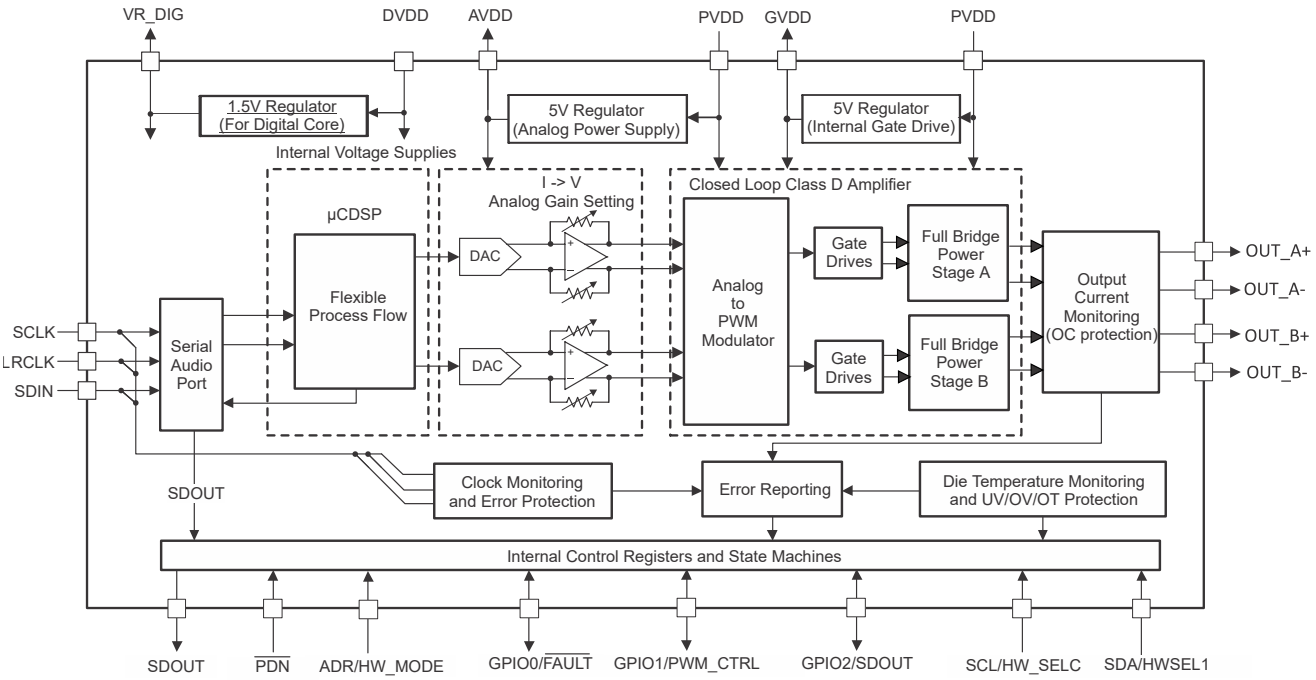
7.1 Overview

The TAS5828M device combines 4 main building blocks into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

- A stereo digital to PWM modulator.
- An Audio DSP subsystem.
- A flexible closed-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. Two internal LDOs convert PVDD to 5V for GVDD and AVDD and to 1.5V for DVDD respectively.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supplies

For system design, TAS5828M needs a 3.3V or 1.8V supply in addition to the (typical) 12V or 24V power-stage supply. Two internal voltage regulators provide voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs can result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (GVDD) are derived from the PVDD voltage. Pay special attention to placing all decoupling capacitors as close to the associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive

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regulator output pin (GVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a voltage supply for the high-side gate driver.

7.3.2 Device Clocking

The TAS5828M devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

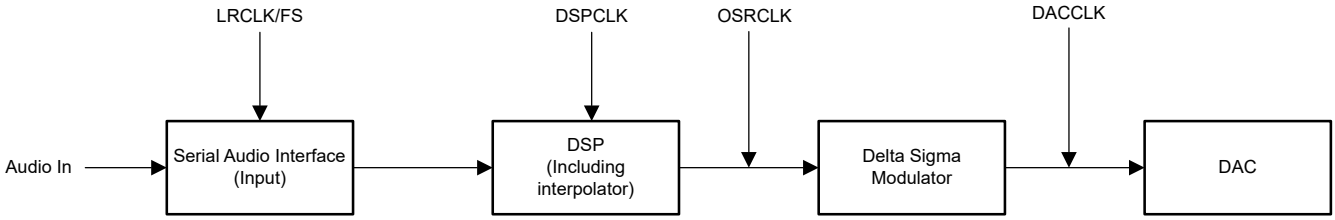

Figure 7-1. Audio Flow with Respective Clocks

Figure 7-1 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left/Right Word Clock or Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher rate clocks required by the DSP and the DAC clock.

The TAS5828M device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32kHz, 44.1kHz – 48kHz, 88.2kHz – 96kHz, 176.4kHz – 192kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

If the input LRCLK/SCLK stopped during music playing, the TAS5828M DSP switches to sleep state and waiting for the clock recovery (Class D output switches to Hiz automatically), once LRCLK/SCLK recovered, TAS5828M auto recovers to the play mode. There is no need to reload the DSP code.

7.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK , and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5828M device with SCLK. The LRCLK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Table 7-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	32 to 192	64, 32
TDM	32, 24, 20, 16	32	128
		44.1,48	128,256,512
		96	128,256
		192	128

When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

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7.3.4 Clock Halt Auto-recovery

Some of host processor Halt the I^{2}S clock when there is no audio playing. When Clock halt, the device puts all channels into the Hi-Z state and reports Clock Error in Register 113 (Register Address 0x71). After audio clocks recovery, the device automatically returns to the previous state.

7.3.5 Sample Rate on the Fly Change

TAS5828M supports LRCLK(FS) rate on the fly change. For example, change LCRLK from 32kHz to 48kHz or 96kHz or 192kHz, Host processor needs to put the LRCLK(FS)/SCLK to Halt state at least 100us before changing to the new sample rate.

7.3.6 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (Register Address 0x33h [5:4]). If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (Register Address 0x33h [3:2]) are set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 7-1. The data formats are detailed in Figure 7-2 through Figure 7-6. The word length are selected via Register (Register Address 0x33h [1:0]). The offsets of data are selected via Register (Register Address 0x33h [7]) and Register (Register Address 0x34h [7:0]). Default setting is I2S and 24 bit word length.

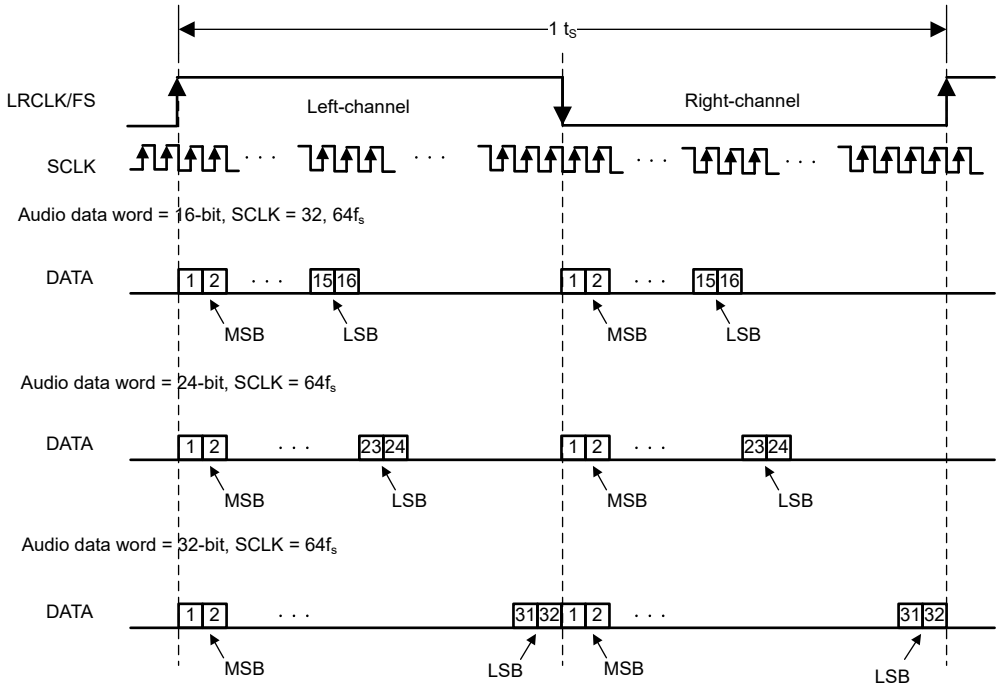

Figure 7-2. Left Justified Audio Data Format

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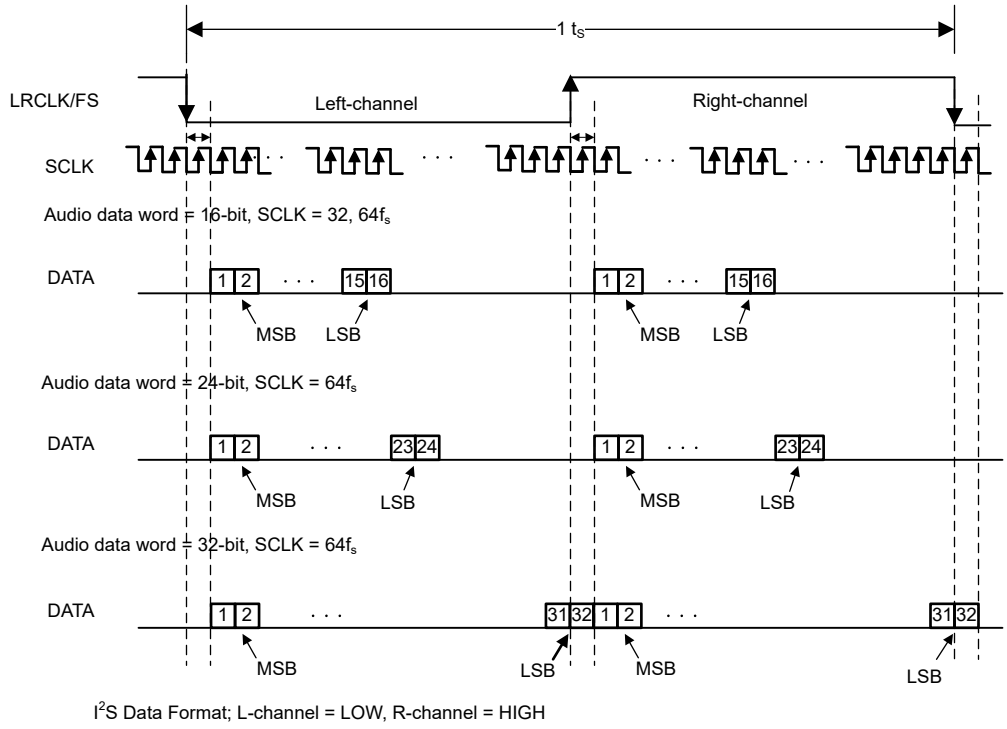
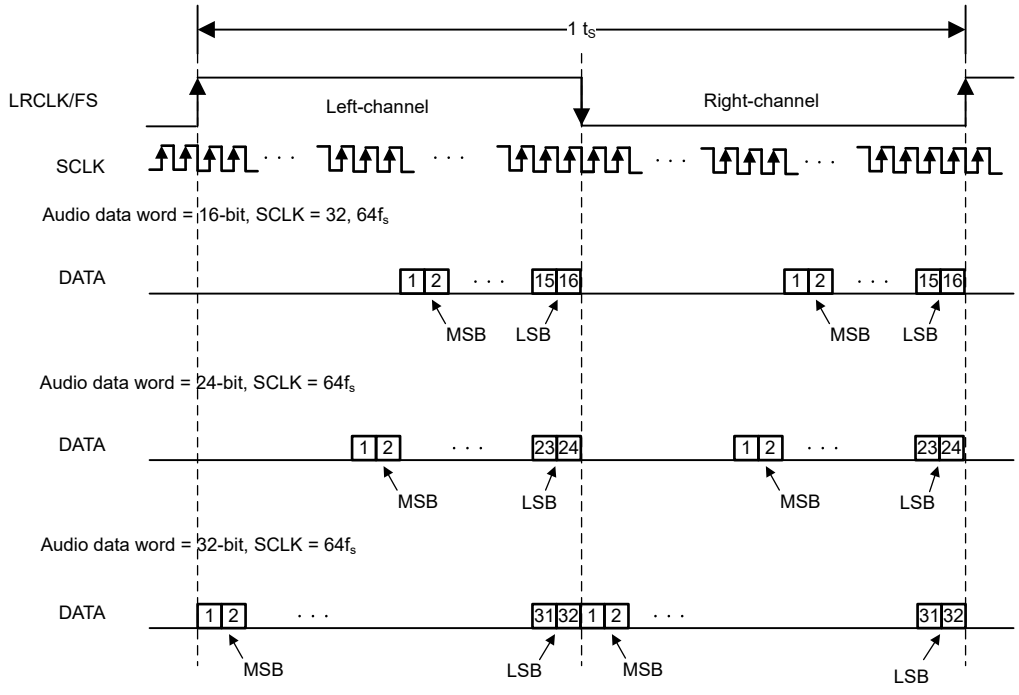


I²S Data Format; L-channel = LOW, R-channel = HIGH

I²S Data Format; L-channel = LOW, R-channel = HIGH

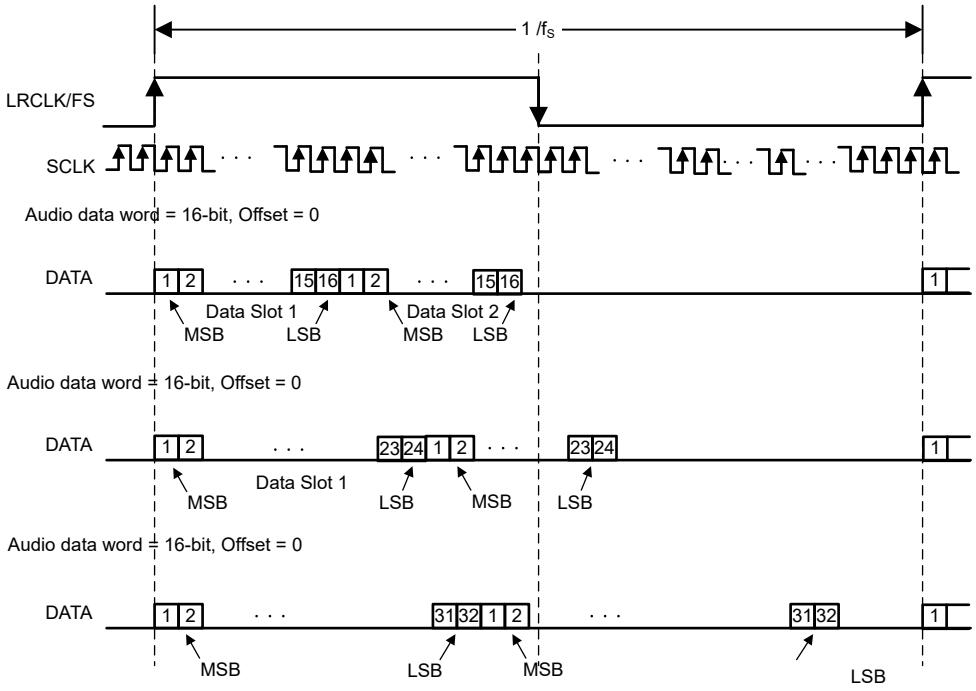
Figure 7-3. I²S Audio Data Format



Right-Justified Data Format; L-channel = HIGH, R-channel = LOW

Right Justified Data Format; L-channel = HIGH, R-channel = LOW

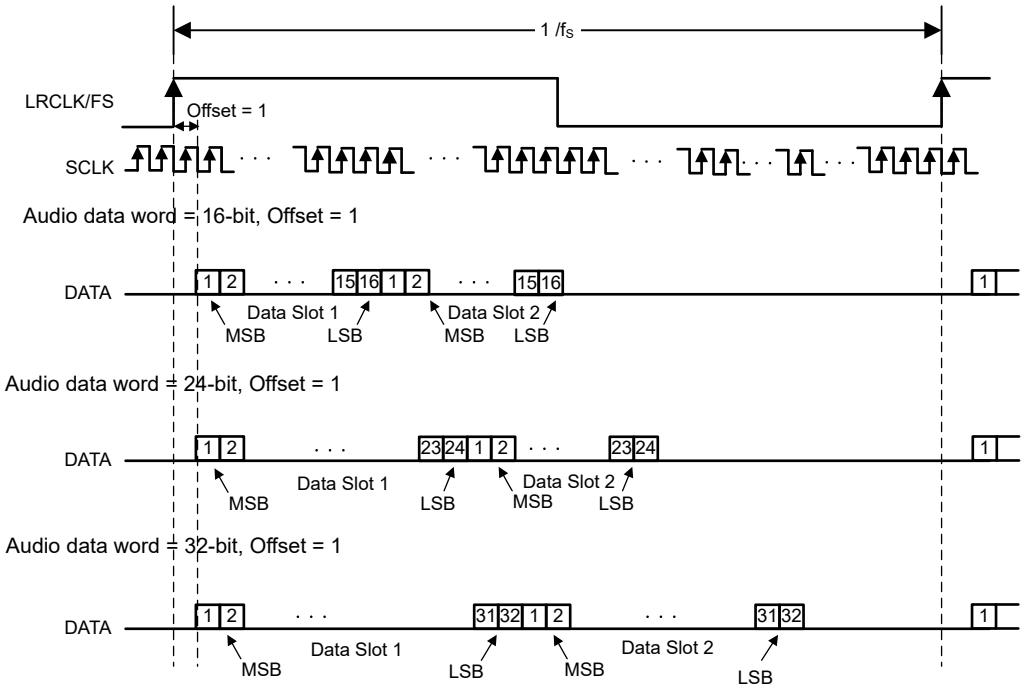
Figure 7-4. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS is 1x SCLK at minimum. Rising edge is considered frame start.

Figure 7-5. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS is 1x SCLK at minimum. Rising edge is considered frame start.

Figure 7-6. TDM 2 Audio Data Format

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7.3.7 Digital Audio Processing

TAS5828M digital audio processing includes three main functions: basic audio tuning blocks, Hybrid-Pro algorithm and advanced features.

For <192kHz processor sampling rates, basic audio tuning blocks are SRC (sample rate converter), stereo channel Input Mixer, 12 to 16 BQs for each channel (throughout the signal chain), pop click free Volume, multi-band DRC, and AGL. For 192kHz processor sampling rates, features are limited to the Hybrid-Pro algorithm and SRC. Detailed introduction of each block can be found with TAS5825M Process Flows.

Hybrid-Pro can be used in conjunction with Hybrid Modulation, which is a remarkable Class-D internal PWM modulation scheme to improve efficiency even more without compromising THD+N performance. Hybrid-Pro goes beyond Hybrid PWM modulation from system efficiency perspective, by tracking audio signal envelope with advanced look-ahead DSP structure, controlling the external PVDD supply voltage rail, and maintaining just enough margin to provide high dynamic range without clipping distortion to save as much power as possible. Refer TAS5828M User Guide for more configurable options:

- Optional 8 steps 384kHz PWM format or 16 steps 192kHz PWM format Hybrid-Pro control waveform for external DC-DC converter.
- Configurable max 4ms look-ahead audio signal delay buffer, which provides capability to fit various applications systems' DC-DC bandwidth and power supply coupling capacitance.
- Max 512 samples audio signal peak hold to optimize power supply voltage rail transition from large audio input to small level, which is useful to avoid clipping distortion.
- Hybrid-Pro Margin automatically adjusts audio signal trigger level and each step level. Fine tune the Hybrid-Pro Margin to achieve the balance between efficiency and envelope tracking speed.

Advanced features include PVDD Sensing (Dynamic Headroom Tracking), Thermal Foldback and Hybrid PWM modulation. Advanced features are implemented based on integrated 8-bit PVDD sense ADC and 4 level temperature sensor. Refer to application note:TAS5825M Advanced Features.

7.3.8 Class D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC maintain constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device. The gain structures are discussed in detail below for both Figure 7-7 and Table 7-2. The switching rate of the amplifier is configurable by register (Register Address 0x02h [6:4])

7.3.8.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in Figure 7-7, the audio path of the TAS5828M consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown in the digital audio path, the DAC gain, and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

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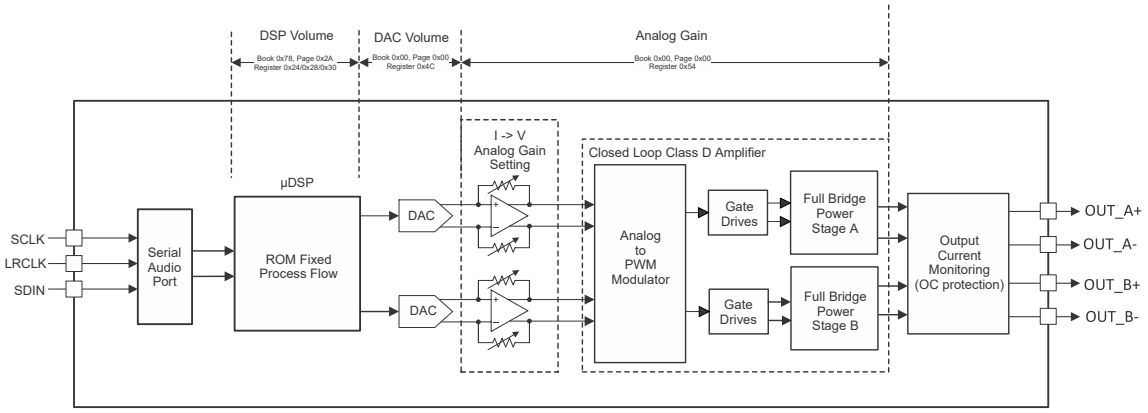

Figure 7-7. Speaker Amplifier Gain

As shown in Figure 7-7, the first gain stage for the speaker amplifier is present in the digital audio path. The digital audio path consists of the volume control (DSP Volume) and the DAC Volume. The volume control is set to 0dB by default. For all settings of the register 0x54, AGAIN[4:0], the digital volume blocks remain at 0dB. These gain settings maintain that the output signal is not clipping at different PVDD levels. 0dBFS output is 29.5V peak output voltage

Table 7-2. Analog Gain Setting

AGAIN <4:0>	GAIN (dBFS)	AMPLIFIER OUTPUT PEAK VOLTAGE (V_P/FS)	AMPLIFIER OUTPUT PEAK VOLTAGE (dBV_P/FS)
00000	0	29.5	29.4
00001	-0.5	27.85	28.9
00010	-1.0	26.29	28.4
00011	-1.5	24.82	27.9
…….	……..	…….	…….
11111	-15.5	4.95	13.9

7.3.8.2 Class D Loop Bandwidth and Switching Frequency Setting

TAS5828M closed loop structure provides Loop bandwidth setting option (Setting by register 83, Register address 0x53h [6-5]) to co-work with different switching frequency (Setting by register 2, Register address 0x02h [6-4]). Table 7-3 shows recommended settings for the Loop Bandwidth and Switching Frequency selection. Same Fsw, Better THD+N performance with higher BW.

Table 7-3. Loop Bandwidth and Switching Frequency Setting

Modulation Scheme	Fsw	BW (Loop Band Width)	Notes
Hybrid, 1SPW	384kHz	80kHz	Principle: Fsw (Switching Frequency) ≥ 4.2 × Loop Bandwidth
	480kHz	80kHz, 100kHz	
	576kHz	80kHz, 100kHz, 120kHz	
	768kHz	80kHz, 100kHz, 120kHz, 175kHz	
BD	384kHz	80kHz, 100kHz, 120kHz	Principle: Fsw (Switching Frequency) ≥ 3 × Loop Bandwidth
	480kHz	80kHz, 100kHz, 120kHz	
	576kHz	80kHz, 100kHz, 120kHz, 175kHz	
	768kHz	80kHz, 100kHz, 120kHz, 175kHz	

7.4 Device Functional Modes

7.4.1 Software Control

The TAS5828M device is configured via an I^2C communication port.

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The I2C Communication Protocol is detailed in the I²C Communication Port section. The I²C timing requirements are described in the Timing Requirements - I²C Bus Timing.

7.4.2 Speaker Amplifier Operating Modes

The TAS5828M device can be configured as two different amplifier configurations through Register 0x02h [2]:

- BTL Mode
- PBTL Mode

7.4.2.1 BTL Mode

In BTL mode, the TAS5828M amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-. The amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

7.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the TAS5828M device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the TAS5828M device, the input signal to the PBTL amplifier is left frame of I2S or TDM data.

7.4.3 Low EMI Modes

TAS5828M employs several modes to minimize EMI during playing audio, and these modes can be used based on different applications.

7.4.3.1 Spread Spectrum

Spread spectrum is used in some cases to minimize EMI noise. The TAS5828M supports Spread Spectrum with triangle and random mode.

User needs to configure register SS_CTRL0 (0x6B) to enable triangle mode and spread spectrum. User can select spread spectrum frequency and range with SS_CTRL1 (0x6C). For 768kHz F_{SW}, which is configured by DEVICE_CTRL1 (0x02), the spread spectrum frequencies and ranges are described in Table 7-4.

Table 7-4. Triangle Mode Spread Spectrum Frequency and Range Selection

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example: Central Switching Frequency is 768kHz, Triangle Frequency is 48kHz.

Register 0x02 = 0x41 // 768kHz Fsw, BTL Mode, 1SPW mode.

Register 0x6b = 0x03 // Enable Spread Spectrum

Register 0x6c = 0x03 // SS_CTRL[3:0]=0011, Triangle Frequency = 48kHz, Spread Spectrum Range is 10% (729kHz~807kHz)

7.4.3.2 Channel to Channel Phase Shift

This device supports channel to channel 180-degree PWM phase shift to minimize the EMI. Bit 0 of Register 0x53 can be used to disable or enable the phase shift.

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7.4.3.3 Multi-Devices PWM Phase Synchronization

TAS5828M support up to 4 phases selection for the multi devices application system. For example, when a system integrated 4 TAS5828M devices, user can select phase0/1/2/3 for each device by register PHASE_CTRL(0x6A), which means there is a 45 degree phase shift between each device to minimize the EMI.

There are two methods for Multi-Device PWM phase synchronization. Phase Synchronization With I^{2}S Clock In Startup Phase or Phase Synchronization With GPIO.

7.4.3.3.1 Phase Synchronization With I^{2}S Clock In Startup Phase

1. Step 1, Halt I^{2}S clock.
2. Step 2, Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A=0x03 for device 0; Register 0x6A=0x07 for device 1; Register 0x6A=0x0B for device 2; Register 0x6A=0x0F for device 3.
3. Step 3, Configure each device into HIZ mode.
4. Step 4, Provide I^{2}S to each device. Phase synchronization for all 4 devices is automatically done by internal sequence.
5. Step 5, Initialize the DSP code (This step can be skipped if only need to do the Phase Synchronization).
6. Step 6, Device to Device PWM phase shift is fixed with 45 degree.

7.4.3.3.2 Phase Synchronization With GPIO

1. Step 1, Connect GPIOx pin of each device to the SOC GPIO pin on PCB.
2. Step 2, Configure each device GPIOx as phase sync input usage by registers GPIO_CTRL (0X60) and GPIO_INPUT_SEL (0x64).
3. Step 3, Select different phase for each device and enable phase synchronization by register PHASE_CTRL (0x6A).
4. Step 4, Configure each device into PLAY mode by register DEVICE_CTRL2 (0x03) and monitor the POWER_STATE register (0x68) until device changed to HIZ state.
5. Step 5, Give a 0 to 1 toggle on SOC GPIO. Then all 4 devices enter into PLAY mode, and device-to-device PWM phase shift are fixed with 45 degree.
6. Step 6, Phase Synchronization has been finished. Configure the GPIOx pin to other function based on the application.

7.4.4 Thermal Foldback

The Thermal Foldback (TFB), is designed to protect TAS5828M from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. The TFB allows the TAS5828M to play as loud as possible without triggering unexpected thermal shutdown. TAS5828M has four over-temperature warning (OTW) thresholds, each threshold is indicated in I2C register 0x73 bits 0, 1, 2, and 3. An internal Automatic Gain Limiter (AGL) gradually reduces the digital gain when the OTW value increases in temperature from level 1 (lowest OTW temperature) to level 4 (highest OTW temperature). The gain attenuation applied is proportional to OTW level, with lower OTW levels resulting in lower attenuation and higher OTW levels resulting in higher attenuation. When die temperature decreases and the OTW level reduces, the digital signal gain gradually increases until the temperature falls below the OTW level and digital gain is restored to the original level. Both the attenuation gain and adjustable rate are programmable. The TFB gain regulation speed (attack rate and release rate) settings are the same as a regular AGL, which is also configurable with TAS5828M App in PurePath™ Console 3.

7.4.5 Device State Control

Other than Shutdown Mode, TAS5828M has other 4 states for different power dissipation: Deep Sleep, Sleep, HiZ, and Play mode. The power levels for each mode are listed in Electrical Characteristics.

- Writing register 0x03 [1:0]=00 places the device in Deep Sleep Mode. In this mode, I^2 C is active. This mode can be used to extend the battery lifetime in some portable speaker applications. Once the host processor stops playing audio, TAS5828M can be set to Deep Sleep Mode to minimize power dissipation until host

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processor starts playing audio again. The device can return back to Play Mode by setting Register 0x03 [1:0] to 11. Compared with Shutdown Mode (Pull $\overline{PDN}$ Low), Deep Sleep Mode keeps the DSP and I2C active.
- Writing register 0x03 [1:0]=01 places the device in Sleep Mode. In this mode, the I^2C block, Digital core, DSP Memory, and 5V Analog LDO are active.
- Writing register 0x03 [1:0]=10 places the device in HiZ Mode. In this mode, the driver outputs are set to the HiZ state, and all other blocks are operating normally.
- Writing register 0x03 [1:0]=11 places the device in Play Mode enabling the output path.

7.4.6 Device Modulation

TAS5828M has 3 modulation schemes: BD modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for TAS5828M with Register 0x02 [1:0]-DAMP_MOD.

7.4.6.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

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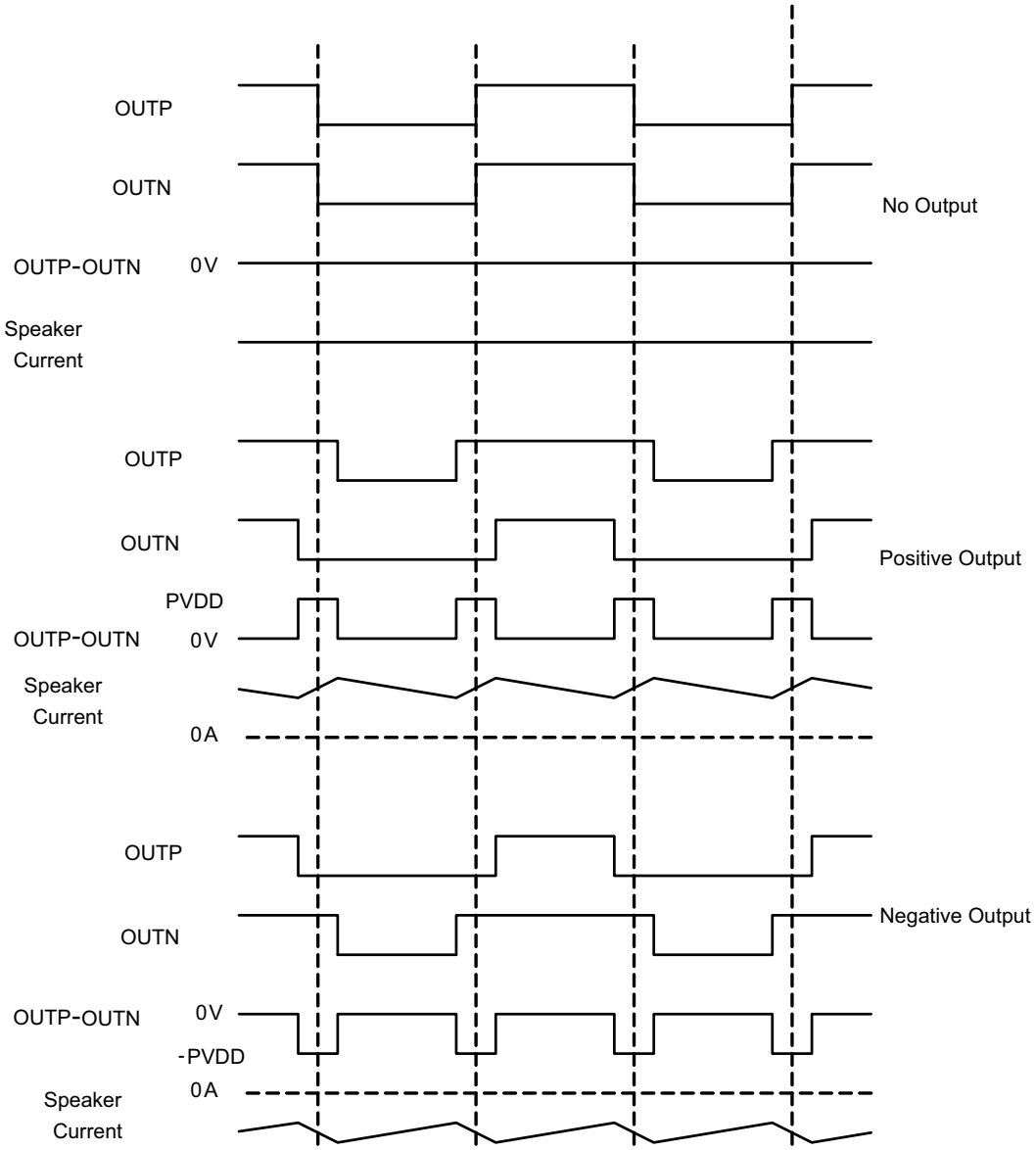

Figure 7-8. BD Mode Modulation

7.4.6.2 1SPW Modulation

The 1SPW mode alters the normal modulation scheme to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at approximately 17% modulation during idle conditions. When an audio signal is applied, one output decreases and one increases. The decreasing output signal rails to GND. At this point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

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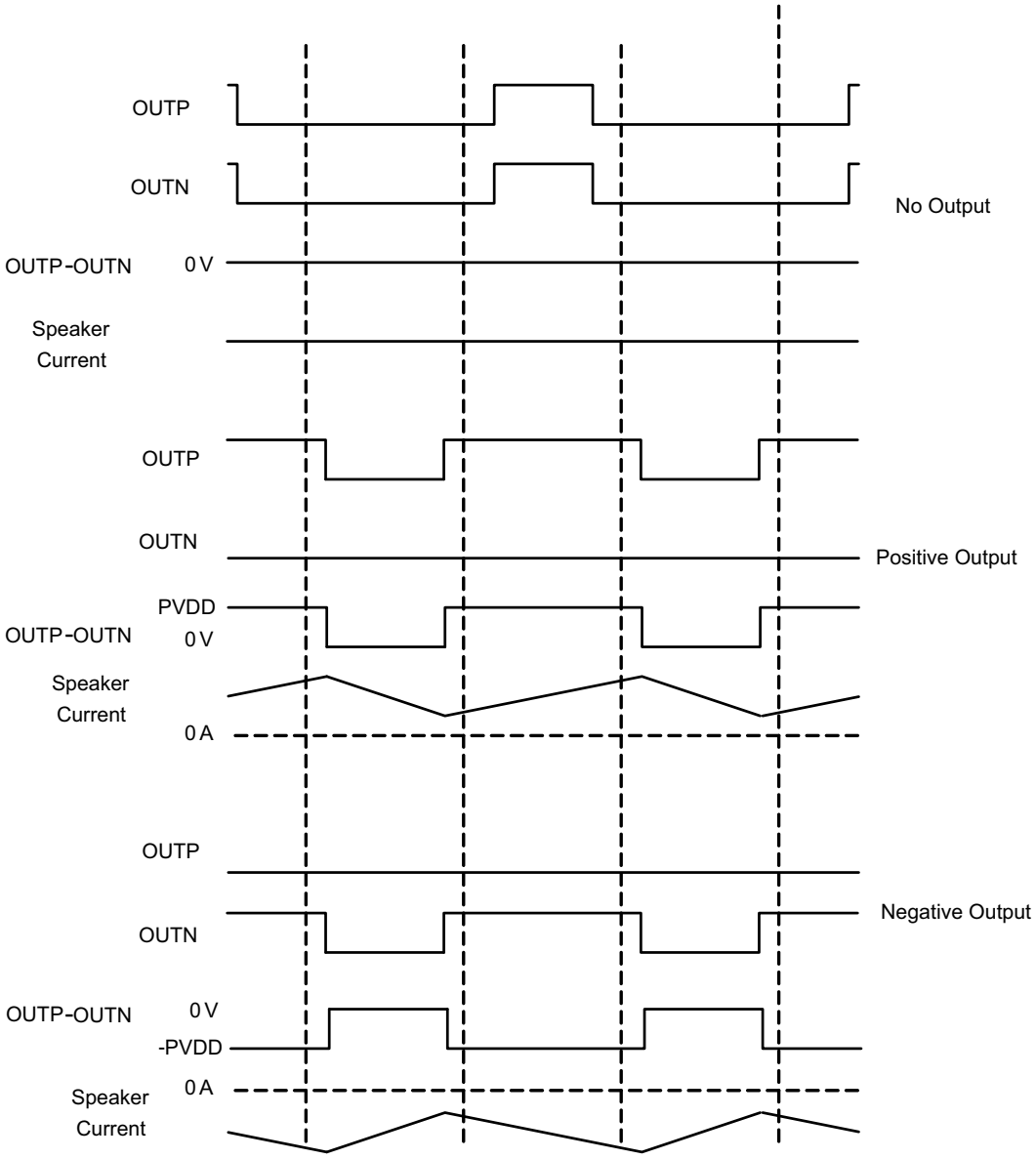

Figure 7-9. 1SPW Mode Modulation

7.4.6.3 Hybrid Modulation

Hybrid Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation, TAS5828M detects the input signal level and adjust PWM duty cycle dynamically from 1SPW to BD modulation based on the output level. Hybrid modulation achieves ultra low idle current and maintains the same audio performance level as the BD Modulation.

Note

As Hybrid Modulation need the internal DSP to detect the input signal level and adjust PWM duty cycle dynamically. To use the Hybrid Modulation, users need to select the corresponding process flows which support Hybrid Modulation in TAS5828M PPC3 App. Look into TAS5828M PPC3 App for more information about TAS5828M flexible audio process flows.

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7.5 Programming and Control

7.5.1 I² C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with I²C bus protocol and supports 100 and 400kHz data transfer rates for random and sequential write and read operations as a target device. Because the TAS5828M register map and DSP memory spans multiple pages and books, the user changes from book to book first and then page to page before writing individual register or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255. All registers listed in TAS5828M Data sheet belongs to Page 0.

7.5.2 Hardware Control Mode

For the system which does not require the advanced flexibility of the I²C registers control or does not have an available I²C host controller, the TAS5828M can be used in Hardware Control Mode. In Hardware mode, any changes are accomplished via the Hardware control pins. The audio performance between Hardware and Software Control mode with same configuration is identical, however more features are accessible under Software Control Mode through registers.

Several I/O's on the TAS5828M need to be took into consideration during schematic design for desired startup settings. The method going into Hardware Control Mode is to pull high HW_MODE, pin13, to DVDD.

The TAS5828M default Hardware configuration with optimized audio, thermal and BOM is BTL mode, 768kHz switching frequency, 1SPW modulation, 175kHz Class-D amplifier loop bandwidth, 29.5Vp/FS analog gain, CBC threshold with 80% of OCP threshold. The device requires the HW_SEL0, pin 5, and HW_SEL1, pin 6, directly tied low GND.

Table 7-5. Hardware Control - HW_SEL0 Pin5

Pin Configuration	Analog Gain	H-Bridge Output Configuration
0Ω to GND	29.5V_P/FS	BTL
1kΩ to GND	20.9V_P/FS	BTL
4.7kΩ to GND	14.7V_P/FS	BTL
15kΩ to GND	7.4V_P/FS	BTL
33kΩ to DVDD	7.4V_P/FS	PBTL
6.8kΩ to DVDD	14.7V_P/FS	PBTL
1.5kΩ to DVDD	20.9V_P/FS	PBTL
0Ω to DVDD	29.5V_P/FS	PBTL

Table 7-6. Hardware Control - HW_SEL1 Pin6

Pin Configuration	F_{SW}&Class D Loop Bandwidth	Cycle By Cycle Current Limit Threshold	Spread Spectrum	Modulation
0Ω to GND	768kHz F_{SW}, 175kHz BW	CBC Threshold = 80% OCP	Disable	1SPW
1kΩ to GND	768kHz F_{SW}, 175kHz BW	CBC Disable	Disable	1SPW
4.7kΩ to GND	768kHz F_{SW}, 175kHz BW	CBC Threshold = 40% OCP	Disable	1SPW
15kΩ to GND	768kHz F_{SW}, 175kHz BW	CBC Threshold = 60% OCP	Disable	1SPW
33kΩ to DVDD	480kHz F_{SW}, 100kHz BW	CBC Disable	Enable	BD
6.8kΩ to DVDD	480kHz F_{SW}, 100kHz BW	CBC Threshold = 80% OCP	Enable	BD
1.5kΩ to DVDD	480kHz F_{SW}, 100kHz BW	CBC Threshold = 40% OCP	Enable	BD
0Ω to DVDD	480kHz F_{SW}, 100kHz BW	CBC Threshold = 60% OCP	Enable	BD

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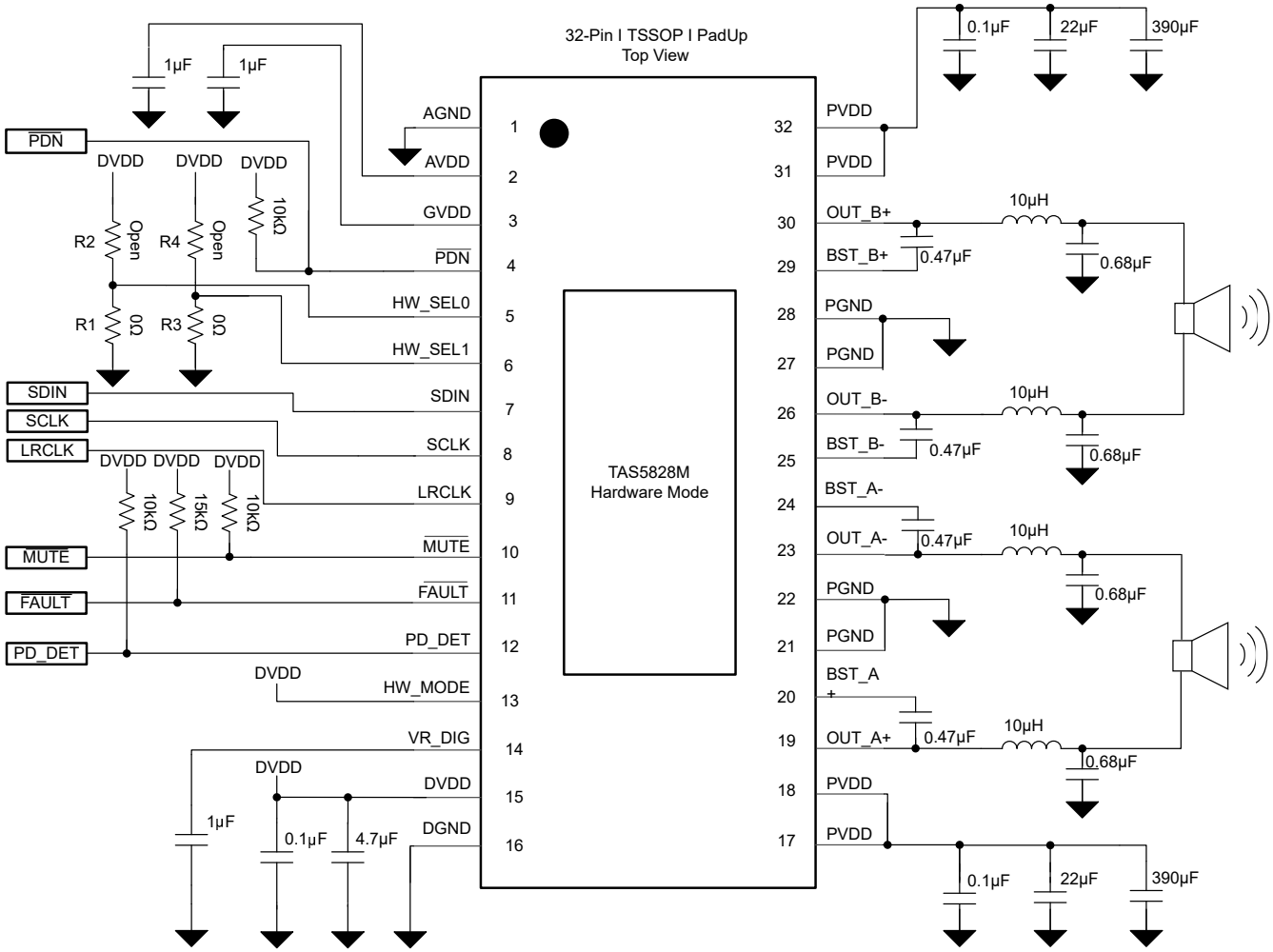
Example 1:

BTL Mode, FSW = 768kHz, 1 SPW Modulation, 175kHz Loop Bandwidth, CBC Threshold = 80% OCP, Analog Gain = 29.5V_P/FS, Spread spectrum disable.

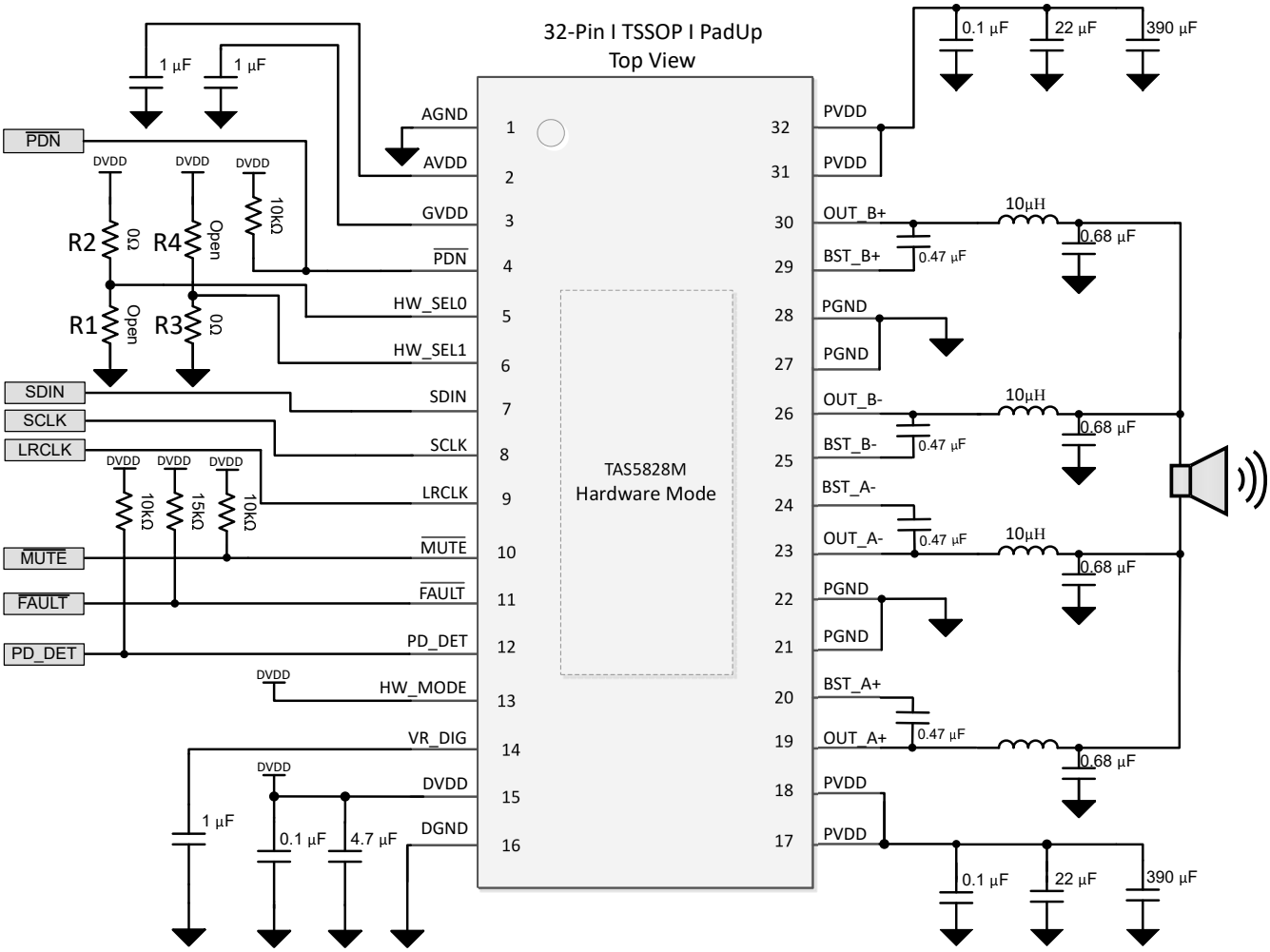
Figure 7-10. Typical Hardware Control Mode Application Schematic-BTL Mode



Example 2:

PBTL Mode, FSW = 768kHz, 1 SPW Modulation, 175kHz Loop Bandwidth, CBC Threshold = 80% OCP, Analog Gain = 29.5V_P/FS, Spread spectrum disable.

Figure 7-11. Typical Hardware Control Mode Application Schematic-PBTL Mode



7.5.3 I² C Target Address

The TAS5828M device has 7 bits for the target address. The user-defined address through ADR pin is listed in Table 7-7.

Table 7-7. I² C Target Address Configuration

ADR PIN Configuration	MSBs				User Define			LSB
0 Ω to GND	1	1	0	0	0	0	0	R/ $\overline{W}$
1kΩ to GND	1	1	0	0	0	0	1	R/ $\overline{W}$
4.7kΩ to GND	1	1	0	0	0	1	0	R/ $\overline{W}$
15kΩ to GND	1	1	0	0	0	1	1	R/ $\overline{W}$
33kΩ to DVDD	1	1	0	0	1	0	0	R/ $\overline{W}$
6.8kΩ to DVDD	1	1	0	0	1	0	1	R/ $\overline{W}$

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7.5.3.1 Random Write

As shown in Figure 7-12, a single-byte data-write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the controller transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the controller device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the controller device transmits a stop condition to complete the single-byte data-write transfer.

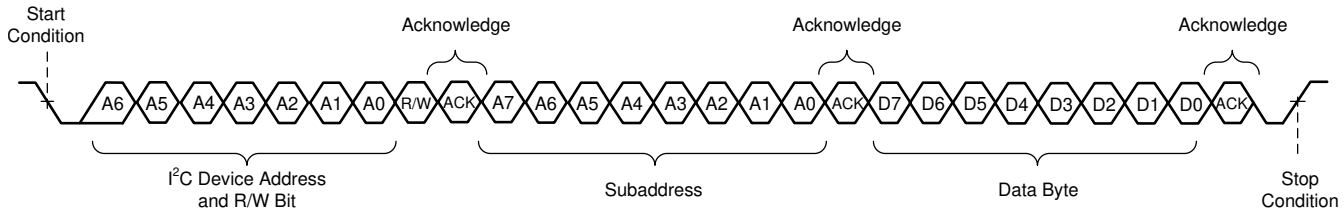

Figure 7-12. Random Write Transfer

7.5.3.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the controller to the device as shown in Figure 7-13. After receiving each data byte, the device responds with an acknowledge bit and the I² subaddress is automatically incremented by one.

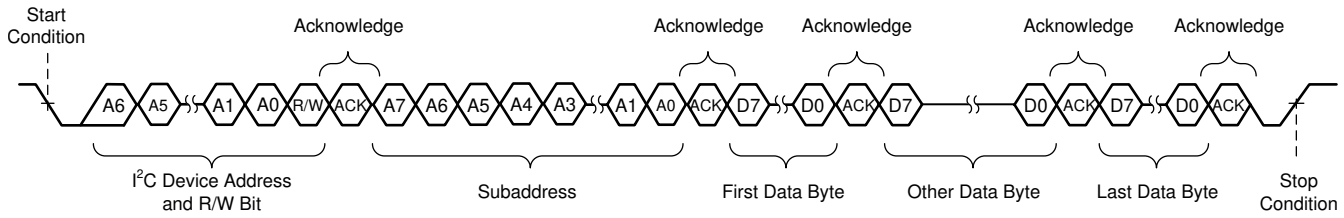

Figure 7-13. Sequential Write Transfer

7.5.3.3 Random Read

As shown in Figure 7-14, a single-byte data-read transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the controller device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

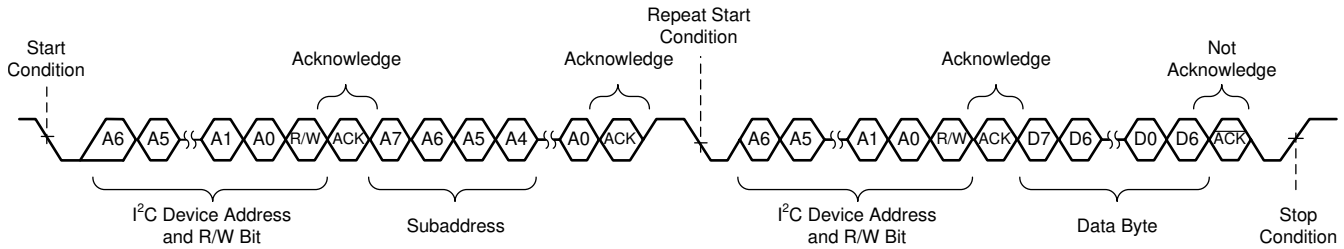

Figure 7-14. Random Read Transfer

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7.5.3.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the controller device as shown in Figure 7-15. Except for the last data byte, the controller device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C sub address by one. After receiving the last data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the transfer.

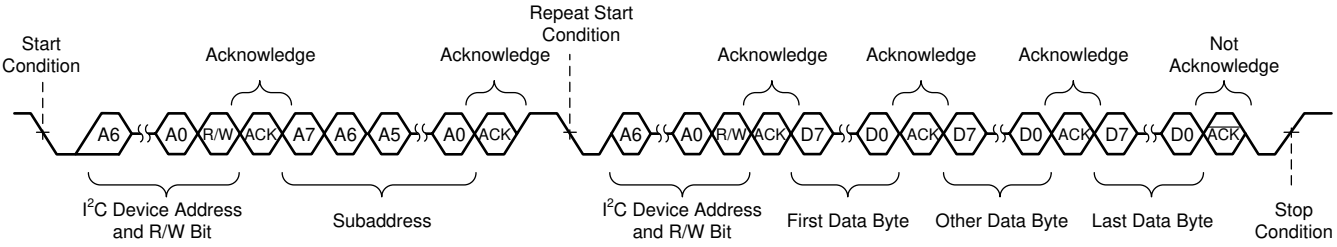

Figure 7-15. Sequential Read Transfer

7.5.3.5 DSP Memory Book, Page and BQ update

On Page 0x00 of each book, Register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a Page first write 0x00 to Register 0x00 to switch to Page 0 then write the book number to Register 0x7f on Page 0. To switch between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in book 0xAA. The five coefficients of every Biquad Filter are written entirely and sequentially from the lowest address to the highest address.

7.5.3.6 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers changes the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (for example 0x 00 00 00 00) to the checksums respective 4-byte register locations.

7.5.3.6.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1 + x1 + x2 + x8)). A major advantage of the CRC checksum is that CRC checksum is input order sensitive. The CRC supports all I²C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

7.5.3.6.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. The checksum performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR checksum can be reset by writing 0x00 to the same register location where 0x00 is read.

7.5.4 Control via Software

- Startup Procedures
- Shutdown Procedures

7.5.4.1 Startup Procedures

1. Configure ADR pin with proper setting for I²C device address or Hardware Mode with proper HW_SEL0 and HW_SEL1 settings.
2. Bring up power supplies (does not matter if PVDD or DVDD comes up first).

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3. Once power supplies are stable, wait at least 100µs, bring up $\overline{PDN}$ to High to enable internal LDO.
4. I^2C control port to configure desired settings. This process includes Deep Sleep to Hiz, register map configurations, DSP coefficients, and set into Play mode. Hardware Mode does not need this step I^2C writing.
5. Once I^2S clocks are stable, TAS5828M is going to normal operation music playing.

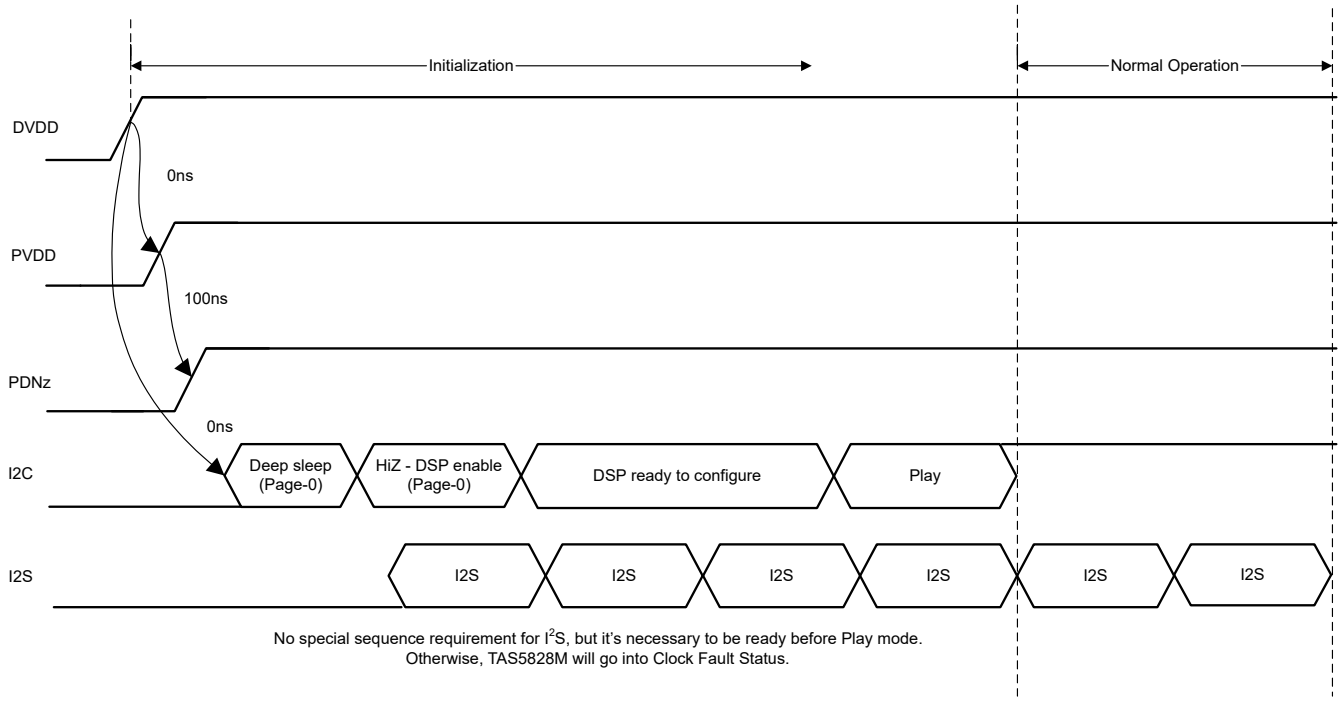
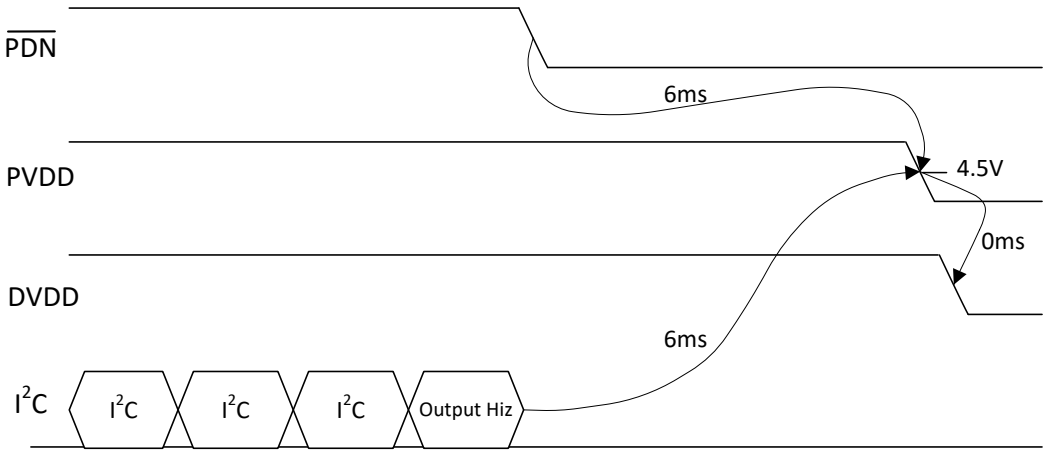


Figure 7-16. TAS5828M Startup Sequence

7.5.4.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register 0x03h [1:0]=10 (Hiz) via the I^2C control port or Pull $\overline{PDN}$ low.
3. Wait at least 6ms (this time depends on the LRCLK rate ,digital volume and digital volume ramp down rate).
4. Bring down power supplies.
5. The device is now fully shutdown and powered off.



- Before PVDD/DVDD power down, Class D Output driver needs to be disabled by $\overline{PDN}$ or by I^2C.
- At least 6ms delay needed based on LRCLK (Fs) = 48kHz,Digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume =24dB. Change the value of register 0x4C and 0x4E or change the LRCLK rate, the delay changes.

Figure 7-17. Power-Down Sequence

7.5.5 Protection and Monitoring

7.5.5.1 Overcurrent Limit (Cycle-By-Cycle)

In addition to direct Overcurrent Shutdown to mute audio output, TAS5828M provides CBC current limiting protection. The purpose is to reduce output current ahead of Overcurrent Shutdown level by insert pulse into PWM switching, and the threshold (list in Electrical Characteristics - OCE_{THRES}) is configurable through Register 0x77h [4:3] Reg_CBC_Level_Sel.

The overall effect on the audio is quite similar a voltage-clipping, which temporarily limits music signal peak power to maintain continues music playing without disruption on removal of the overload.

7.5.5.2 Overcurrent Shutdown (OCSD)

If there is severe short-circuit event, such as output short to PVDD or ground, the TAS5828M starts shutdown process less than 100ns once peak-current detector is over Overcurrent Threshold (list in Electrical Characteristics - OCE_{THRES}). The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency.

If an OCSD event occurs, the fault GPIO is pulled low and I^2C fault register fault status is reported, then outputs transfer to high impedance Hiz status, signifying a fault. This is a latched error, and the user needs to restart output via I^2C clear fault operation.

7.5.5.3 DC Detect Error

If the TAS5828M detects a DC offset in the output voltage cross speaker over DC error protection threshold DCR_{THRES}, and this status period is over T_{DCDET} (list in Electrical Characteristics - Protection), the FAULTZ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault. This latched DC Protection error requires I^2C clear fault operation to restart audio output.

7.5.5.4 Overtemperature Shutdown (OTSD)

The TAS5828M device continuously monitors die temperature to ensure it does not exceed the over temperature threshold specified in Electrical Characteristics - OCE_{THRES}. If an OTE event occurs, the fault GPIO is pulled low, I^2C fault status is reported, and the audio output transfers to high impedance, HiZ, mode, signifying a fault. This is a latched error and requires an I^2C clear fault operation to restart audio playing.

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7.5.5.5 PVDD Overvoltage and Undervoltage Error

If the voltage presented on the PVDD supply rises over the $OVE_{THRES(PVDD)}$ or drops below the $UVE_{THRES(PVDD)}$ listed in Electrical Characteristics - Protection, the fault GPIO is pulled to low and I^2C fault status is reported, then audio output transfers to high impedance Hiz mode. These are self-clearing error, which means that once PVDD level is back to normal operation, the device resumes audio playing.

7.5.5.6 PVDD Drop Detection

TAS5828M not only provides PVDD Undervoltage Shutdown protection, but also optional PVDD drop detection. Based on internal PVDD real-time sensing voltage, TAS5828M is able to be configured to expected behavior, which toggles pin10 PD_DET from high to low to indicate PVDD drops below specific level (default 8V), and whether TAS5828M automatically goes into Hiz mode to shutdown audio output. All these settings is accessible through Register 0x04h and 0x05h.

The purpose is to feedback PVDD voltage drop information through GPIO to user product control system, which is able to implement flexible protection strategy. For example, SOC starts audio volume fade out process once PD_DET pin goes to low. This process can provide effective pop-click free control shutdown.

7.5.5.7 Clock Fault

When a clock error is detected on incoming data clock, the TAS5828M device switches to an internal oscillator and continues to the driving DAC, which attenuates the data from the last known value. Once this process is completed, the DAC output is hard muted to ground and audio output stops. This non-latched clock fault status is reported via the I^2C fault status register, and the device automatically returns to play mode once the correct clock returns.

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8 Register Maps

8.1 CONTROL PORT Registers

Table 8-1 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in Table 8-1 are considered as reserved locations and the register contents are not to be modified.

Table 8-1. CONTROL PORT Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Register 1	Go
2h	DEVICE_CTRL1	Register 2	Go
3h	DEVICE_CTRL2	Register 3	Go
4h	PVDD_DROP_DETECTION_CTRL1	Register 4	Go
5h	PVDD_DROP_DETECTION_CTRL2	Register 5	Go
Fh	I2C_PAGE_AUTO_INC	Register 15	Go
28h	SIG_CH_CTRL	Register 40	Go
29h	CLOCK_DET_CTRL	Register 41	Go
30h	SDOUT_SEL	Register 48	Go
31h	I2S_CTRL	Register 49	Go
33h	SAP_CTRL1	Register 51	Go
34h	SAP_CTRL2	Register 52	Go
35h	SAP_CTRL3	Register 53	Go
37h	FS_MON	Register 55	Go
38h	BCK (SCLK)_MON	Register 56	Go
39h	CLKDET_STATUS	Register 57	Go
40h	DSP_PGM_MODE	Register 64	Go
46h	DSP_CTRL	Register 70	Go
4Ch	DAC_GAIN	Register 76	Go
4Eh	DIG_VOL_CTRL1	Register 78	Go
4Fh	DIG_VOL_CTRL2	Register 79	Go
50h	AUTO_MUTE_CTRL	Register 80	Go
51h	AUTO_MUTE_TIME	Register 81	Go
53h	ANA_CTRL	Register 83	Go
54h	AGAIN	Register 84	Go
5Eh	PVDD_ADC	Register 94	Go
60h	GPIO_CTRL	Register 96	Go
61h	GPIO1_SEL	Register 97	Go
62h	GPIO2_SEL	Register 98	Go
63h	GPIO0_SEL	Register 99	Go
64h	GPIO_INPUT_SEL	Register 100	Go
65h	GPIO_OUT	Register 101	Go
66h	GPIO_OUT_INV	Register 102	Go
67h	DIE_ID	Register 103	Go
68h	POWER_STATE	Register 104	Go
69h	AUTOMUTE_STATE	Register 105	Go
6Ah	PHASE_CTRL	Register 106	Go
6Bh	SS_CTRL0	Register 107	Go
6Ch	SS_CTRL1	Register 108	Go
6Dh	SS_CTRL2	Register 109	Go

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Table 8-1. CONTROL PORT Registers (continued)

Offset	Acronym	Register Name	Section
6Eh	SS_CTRL3	Register 110	Go
6Fh	SS_CTRL4	Register 111	Go
70h	CHAN_FAULT	Register 112	Go
71h	GLOBAL_FAULT1	Register 113	Go
72h	GLOBAL_FAULT2	Register 114	Go
73h	WARNING	Register 115	Go
74h	PIN_CONTROL1	Register 116	Go
75h	PIN_CONTROL2	Register 117	Go
76h	MISC_CONTROL	Register 118	Go
77h	CBC_CONTROL	Register 119	Go
78h	FAULT_CLEAR	Register 120	Go

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. CONTROL PORT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 RESET_CTRL Register (Offset = 1h) [reset = 0x00]

RESET_CTRL is shown in Figure 8-1 and described in Table 8-3.

Return to Summary Table.

Figure 8-1. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
R/W			W	R			W

Table 8-3. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	RST_DIG_CORE	W	0	WRITE CLEAR BIT Reset DIG_CORE WRITE CLEAR BIT Reset Full Digital Core. This bit resets the Full Digital Signal Path (Include DSP coefficient RAM and I2C Control Port Registers), Since the DSP is also reset, the coeffient RAM content is also cleared by the DSP. 0: Normal 1: Reset Full Digital Signal Path
3-1	RESERVED	R	000	This bit is reserved
0	RST_REG	W	0	WRITE CLEAR BIT Reset Registers This bit resets the mode registers back to the initial values. Only reset Control Port Registers, The RAM content is not cleared. 0: Normal 1: Reset I^2C Control Port Registers

8.1.2 DEVICE_CTRL_1 Register (Offset = 2h) [reset = 0x00]

DEVICE_CTRL_1 is shown in Figure 8-2 and described in Table 8-4.

Return to Summary Table.

Figure 8-2. DEVICE_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	DAMP_PBTL	DAMP_MOD	
R/W	R/W			R/W	R/W	R/W	

Table 8-4. DEVICE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	FSW_SEL	R/W	000	SELECT FSW 000:384K 010:480K 011:576K 100:768K 001:Reserved 101:Reserved 110:Reserved 111:Reserved
3	RESERVED	R/W	0	This bit is reserved

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Table 8-4. DEVICE_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DAMP_PBTL	R/W	0	0: SET DAMP TO BTL MODE 1:SET DAMP TO PBTL MODE
1-0	DAMP_MOD	R/W	00	00:BD MODE 01:1SPW MODE 10:HYBRID MODE

8.1.3 DEVICE_CTRL2 Register (Offset = 3h) [reset = 0x10]

DEVICE_CTRL2 is shown in Figure 8-3 and described in Table 8-5.

Return to Summary Table.

Figure 8-3. DEVICE_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED			DIS_DSP	MUTE_LEFT	RESERVED	CTRL_STATE	
R/W			R/W	R/W	R/W	R/W	

Table 8-5. DEVICE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	DIS_DSP	R/W	1	DSP reset When the bit is made 0, DSP starts powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
3	MUTE	R/W	0	Mute both Left and Right Channel This bit issues soft mute request for both left and right channel. The volume is smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	RESERVED	R/W	0	This bit is reserved
1-0	CTRL_STATE	R/W	00	device state control register 00: Deep Sleep 01: Sleep 10: Hiz, 11: PLAY

8.1.4 PVDD_DROP_DETECTION_CTRL1 Register (Offset = 4h) [reset = 0x00]

PVDD_DROP_DETECTION_CTRL1 is shown in Figure 8-4 and described in Table 8-6.

Return to Summary Table.

Figure 8-4. PVDD_DROP_DETECTION_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED				PVDD_DROP_DET_SEQUENCE	PVDD_DROP_DET_AVE_SAMPLES		PVDD_DROP_DET_BYPASS
R/W				R/W	R/W		R/W

Table 8-6. PVDD_DROP_DETECTION_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	000	This bit is reserved

Table 8-6. PVDD_DROP_DETECTION_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PVDD_DROP_DET_State_Control	R/W	0	This bit controls whether device automatically set into Hiz or still play once PVDD drop detection happens. 0: The device keeps in play mode even PVDD drops configured threshold 1: The device goes into Hiz once PVDD drops configured threshold
2-1	PVDD_DROP_DET_AVE_SAMPLES	R/W	00	PVDD sense average samples for drop detection This bit is used to set PVDD voltage sense average samples for drop detection. 00: 1 sample - cycle by cycle, no average 01: 16 samples 10: 32 samples 11: 64 samples
0	PVDD_DROP_DET_Enable	R/W	0	PVDD drop detection Enable This bit controls enable or bypass PVDD drop detection. 0: Bypass PVDD drop detection 1: Enable PVDD drop detection

8.1.5 PVDD_DROP_DETECTION_CTRL2 Register (Offset = 5h) [reset = 0x44]

PVDD_DROP_DETECTION_CTRL2 is shown in Figure 8-5 and described in Table 8-7.

Return to Summary Table.

Figure 8-5. PVDD_DROP_DETECTION_CTRL2 Register

7	6	5	4	3	2	1	0
PVDD Drop Detection Voltage Threshold							
R/W							

Table 8-7. PVDD_DROP_DETECTION_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PVDD Drop Detection Voltage Threshold	R/W	00000000	This bit is used to set PVDD Drop Detection Threshold. The radio to 0xFFh equals to full scale voltage 30V. For example, 8V threshold: 8V/30V = 0x44h/0xFFh. PVDD Drop Threshold is configured as: 00: 0V 01: 0.117V ... 44: 8V ... FF: 30V

8.1.6 I2C_PAGE_AUTO_INC Register (Offset = Fh) [reset = 0x00]

I2C_PAGE_AUTO_INC is shown in Figure 8-6 and described in Table 8-8.

Return to Summary Table.

Figure 8-6. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_AUTOINC_REG	RESERVED		
R/W				R/W	R/W		

Table 8-8. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved

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Table 8-8. I2C_PAGE_AUTO_INC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PAGE_AUTOINC_REG	R/W	0	Page auto increment disable Disable page auto increment mode. When this bit is 0 and the end of the page is reached, the I2C address auto-increments to 8th address location of next page. When this bit is 1 and the end of the page is reached, the I2C address returns to the 0th location of current page, like in older parts. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	RESERVED	R/W	000	This bit is reserved

8.1.7 SIG_CH_CTRL Register (Offset = 28h) [reset = 0x00]

SIG_CH_CTRL is shown in Figure 8-7 and described in Table 8-9.

Return to Summary Table.

Figure 8-7. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
SCLK_RATIO_CONFIGURE				FSMODE			
R/W				R/W			

Table 8-9. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SCLK_RATIO_CONFIGURE	R/W	0000	These bits indicate the configured SCLK ratio, the number of SCLK clocks in one audio frame. Device sets this ratio automatically. 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS
3-0	FSMODE	R/W	0	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. Need set the bit manually if the input FS is 44.1kHz/88.2kHz/176.4kHz. 4 'b0000 Auto detection 4 'b0100 Reserved 4 'b0110 32KHz 4 'b1000 44.1KHz 4 'b1001 48KHz 4'b1010 88.2KHz 4 'b1011 96KHz 4 'b1100 176.4KHz 4 'b1101 192KHz Others Reserved

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8.1.8 CLOCK_DET_CTRL Register (Offset = 29h) [reset = 0x00]

CLOCK_DET_CTRL is shown in Figure 8-8 and described in Table 8-10.

Return to Summary Table.

Figure 8-8. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DIS_DET_PLL	DIS_DET_SCLK_RANGE	DIS_DET_FS	DIS_DET_SCLK	DIS_DET_MISS	RESERVED	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-10. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	DIS_DET_PLL	R/W	0	Ignore PLL overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error is reported. When ignored, a PLL overrate error does not cause a clock error. 0: Regard PLL overrate detection 1: Ignore PLL overrate detection
5	DIS_DET_SCLK_RANGE	R/W	0	Ignore BCK Range Detection This bit controls whether to ignore the SCLK range detection. The SCLK must be stable between 256KHz and 50MHz or an error is reported. When ignored, a SCLK range error does not cause a clock error. 0: Regard BCK Range detection 1: Ignore BCK Range detection
4	DIS_DET_FS	R/W	0	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error does not cause a clock error.But CLKDET_STATUS reports fs error. 0: Regard FS detection 1: Ignore FS detection
3	DIS_DET_SCLK	R/W	0	Ignore SCLK Detection This bit controls whether to ignore the SCLK detection against LRCK. The SCLK must be stable between 32FS and 512FS inclusive or an error is reported. When ignored, a SCLK error does not cause a clock error. 0: Regard SCLK detection 1: Ignore SCLK detection
2	DIS_DET_MISS	R/W	0	Ignore SCLK Missing Detection This bit controls whether to ignore the SCLK missing detection. When ignored, an SCLK missing does not cause a clock error. 0: Regard SCLK missing detection 1: Ignore SCLKmissing detection
1	RESERVED	R/W	0	This bit is reserved
0	RESERVED	R/W	0	This bit is reserved

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8.1.9 SDOUT_SEL Register (Offset = 30h) [reset = 0x00]

SDOUT_SEL is shown in Figure 8-10 and described in Table 8-11.

Return to Summary Table.

Figure 8-9. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		SDOUT_SEL
R/W					R/W		R/W

Table 8-11. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	These bits are reserved
0	SDOUT_SEL	R/W	0	SDOUT Select. This bit selects what is being output as SDOUT pin. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

8.1.10 I2S_CTRL Register (Offset = 31h) [reset = 0x00]

I2S_CTRL is shown in Figure 8-10 and described in Table 8-12.

Return to Summary Table.

Figure 8-10. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		SCLK_INV	RESERVED	RESERVED	RESERVED		RESERVED
R/W		R/W	R/W	R	R		R/W

Table 8-12. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	SCLK_INV	R/W	0	SCLK Polarity This bit sets the inverted SCLK mode. In inverted SCLK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the SCLK. Normally the LRCK and DIN edges are assumed to be aligned to the falling edge of the SCLK 0: Normal SCLK mode 1: Inverted SCLK mode
4	RESERVED	R/W	0	This bit is reserved
3	RESERVED	R	0	This bit is reserved
2-1	RESERVED	R	00	These bits are reserved
0	RESERVED	R/W	0	This bit is reserved

8.1.11 SAP_CTRL1 Register (Offset = 33h) [reset = 0x02]

SAP_CTRL1 is shown in Figure 8-11 and described in Table 8-13.

Return to Summary Table.

Figure 8-11. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
I2S_SHIFT_MSB	RESERVED	DATA_FORMAT		I2S_LRCLK_PULSE		WORD_LENGTH	

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Figure 8-11. SAP_CTRL1 Register (continued)

R/W	R/W	R/W	R/W	R/W

Table 8-13. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2S_SHIFT_MSB	R/W	0	I2S Shift MSB
6	RESERVED	R/W	0	This bit is reserved
5-4	DATA_FORMAT	R/W	00	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_LRCLK_PULSE	R/W	00	01: LRCLK pulse < 8 SCLK
1-0	WORD_LENGTH	R/W	10	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

8.1.12 SAP_CTRL2 Register (Offset = 34h) [reset = 0x00]

SAP_CTRL2 is shown in Figure 8-12 and described in Table 8-14.

Return to Summary Table.

Figure 8-12. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
I2S_SHIFT							
R/W							

Table 8-14. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2S_SHIFT	R/W	00000000	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. MSB [8] locates in Section 8.1.11 000000000: offset = 0 SCLK (no offset) 000000001: offset = 1 SCLK 000000010: offset = 2 SCLKs and 111111111: offset = 512 SCLKs

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8.1.13 SAP_CTRL3 Register (Offset = 35h) [reset = 0x11]

SAP_CTRL3 is shown in Figure 8-13 and described in Table 8-15.

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Figure 8-13. SAP_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		LEFT_DAC_DPATH		RESERVED		RIGHT_DAC_DPATH	
R/W		R/W		R/W		R/W	

Table 8-15. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	These bits are reserved
5-4	LEFT_DAC_DPATH	R/W	01	Left DAC Data Path. These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
3-2	RESERVED	R/W	00	These bits are reserved
1-0	RIGHT_DAC_DPATH	R/W	01	Right DAC Data Path. These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

8.1.14 FS_MON Register (Offset = 37h) [reset = 0x00]

FS_MON is shown in Figure 8-14 and described in Table 8-16.

Return to Summary Table.

Figure 8-14. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		SCLK_RATIO_HIGH		FS			
R/W		R		R			

Table 8-16. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	SCLK_RATIO_HIGH	R	00	2 msbs of detected SCLK ratio
3-0	FS	R	0000	These bits indicate the currently detected audio sampling rate. 4 'b0000 FS Error 4 'b0100 16KHz 4 'b0110 32KHz 4 'b1000 Reserved 4 'b1001 48KHz 4 'b1011 96KHz 4 'b1101 192KHz Others Reserved

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8.1.15 BCK (SCLK)_MON Register (Offset = 38h) [reset = 0x00]

BCK_MON is shown in Figure 8-15 and described in Table 8-17.

Return to Summary Table.

Figure 8-15. BCK (SCLK)_MON Register

7	6	5	4	3	2	1	0
BCLK (SCLK)_RATIO_LOW							
R							

Table 8-17. BCK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLK (SCLK)_RATIO_LOW	R	00000000	These bits indicate the currently detected BCK (SCLK) ratio, the number of BCK (SCLK) clocks in one audio frame. BCK (SCLK) = 32 FS~512 FS

8.1.16 CLKDET_STATUS Register (Offset = 39h) [reset = 0x00]

CLKDET_STATUS is shown in Figure 8-16 and described in Table 8-18.

Return to Summary Table.

Figure 8-16. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		DET_STATUS					
R/W		R					

Table 8-18. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-0	DET_STATUS	R	000000	bit0: In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid or not. In non auto detection mode(reg_fsmode!=0), Fs error indicates that configured fs is different with detected fs. Even FS Error Detection Ignore is set, this flag is also asserted. bit1: This bit indicates whether the SCLK is valid or not. The SCLK ratio must be stable and in the range of 32-512FS to be valid. bit2: This bit indicates whether the SCLK is missing or not. bit3:This bit indicates whether the PLL is locked or not. The PLL is reported as unlocked when the bit is disabled. bits4:This bit indicates whether the PLL is overrate bits5:This bit indicates whether the SCLK is overrate or underrate

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8.1.17 DSP_PGM_MODE Register (Offset = 40h) [reset = 0x01]

DSP_PGM_MODE is shown in Figure 8-17 and described in Table 8-19.

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Figure 8-17. DSP_PGM_MODE Register

7	6	5	4	3	2	1	0
RESERVED				CH1_HIZ	CH2_HIZ	RESERVED	
				R/W	R/W		

Table 8-19. DSP_PGM_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3	CH1_HIZ	R/W	0	Hi-Z Mode Channel-1 Stops output switching and sets channel-1 to Hi-Z mode. 0: Normal Operation 1: Hi-Z state
2	CH2_HIZ	R/W	0	Hi-Z Mode Channel-2 Stops output switching and sets channel-2 to Hi-Z mode. 0: Normal Operation 1: Hi-Z state
1-0	RESERVED	R/W	01	This bit is reserved

8.1.18 DSP_CTRL Register (Offset = 46h) [reset = 0x01]

DSP_CTRL is shown in Figure 8-18 and described in Table 8-20.

Return to Summary Table.

Figure 8-18. DSP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			USER_DEFINED_PROCESSING_RATE		RESERVED	BOOT_FROM_IRAM	USE_DEFAULT_COEFFS
R/W			R/W		R	R/W	R/W

Table 8-20. DSP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-3	USER_DEFINED_PROCESSING_RATE	R/W	00	00:input 01:48k 10:96k 11:192k
2	RESERVED	R	0	This bit is reserved
1	RESERVED	R	0	This bit is reserved
0	RESERVED	R/W	1	This bit is reserved

8.1.19 DAC_GAIN Register (Offset = 4Ch) [reset = 30h]

DAC_GAIN is shown in Figure 8-19 and described in Table 8-21.

Return to Summary Table.

Figure 8-19. DAC_GAIN Register

7	6	5	4	3	2	1	0
DAC_GAIN							

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Figure 8-19. DAC_GAIN Register (continued)

R/W

Table 8-21. DAC_GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DAC GAIN	R/W	00110000	DAC GAIN These bits control both left and right channel digital volume. The digital volume is 24dB to -103dB in -0.5dB step. 00000000: +24.0dB 00000001: +23.5dB ..... and 00101111: +0.5dB 00110000: 0.0dB 00110001: -0.5dB ..... 11111110: -103dB 11111111: Mute

8.1.20 DIG_VOL_CTRL1 Register (Offset = 4Eh) [reset = 0x33]

DIG_VOL_CTRL1 is shown in Figure 8-20 and described in Table 8-22.

Return to Summary Table.

Figure 8-20. DIG_VOL_CTRL1 Register

7	6	5	4	3	2	1	0
PGA_RAMP_DOWN_SPEED		PGA_RAMP_DOWN_STEP		PGA_RAMP_UP_SPEED		PGA_RAMP_UP_STEP	
R/W		R/W		R/W		R/W	

Table 8-22. DIG_VOL_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGA_RAMP_DOWN_SPEED	R/W	00	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	PGA_RAMP_DOWN_STEP	R/W	11	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down. 00: Decrement by 4dB for each update 01: Decrement by 2dB for each update 10: Decrement by 1dB for each update 11: Decrement by 0.5dB for each update
3-2	PGA_RAMP_UP_SPEED	R/W	00	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	PGA_RAMP_UP_STEP	R/W	11	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up. 00: Increment by 4dB for each update e 01: Increment by 2dB for each update 10: Increment by 1dB for each update 11: Increment by 0.5dB for each update

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8.1.21 DIG_VOL_CTRL2 Register (Offset = 4Fh) [reset = 0x30]

DIG_VOL_CTRL2 is shown in Figure 8-21 and described in Table 8-23.

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Figure 8-21. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
FAST_RAMP_DOWN_SPEED		FAST_RAMP_DOWN_STEP		RESERVED			
R/W		R/W		R/W			

Table 8-23. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FAST_RAMP_DOWN_SPEED	R/W	00	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which typically needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	FAST_RAMP_DOWN_STEP	R/W	11	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which typically needs faster ramp down compared to normal soft mute. 00: Decrement by 4dB for each update 01: Decrement by 2dB for each update 10: Decrement by 1dB for each update 11: Decrement by 0.5dB for each update
3-0	RESERVED	R/W	0000	This bit is reserved

8.1.22 AUTO_MUTE_CTRL Register (Offset = 50h) [reset = 0x00]

AUTO_MUTE_CTRL is shown in Figure 8-22 and described in Table 8-24.

Return to Summary Table.

Figure 8-22. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					REG_AUTO_MUTE_CTRL		
R/W					R/W		

Table 8-24. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2-0	REG_AUTO_MUTE_CTRL	R/W	000	bit0: 0: Disable left channel auto mute 1: Enable left channel auto mute bit1: 0: Disable right channel auto mute 1: Enable right channel auto mute bit2: 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.

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8.1.23 AUTO_MUTE_TIME Register (Offset = 51h) [reset = 0x00]

AUTO_MUTE_TIME is shown in Figure 8-23 and described in Table 8-25.

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Figure 8-23. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	AUTOMUTE_TIME_LEFT			RESERVED	AUTOMUTE_TIME_RIGHT		
R/W	R/W			R/W	R/W		

Table 8-25. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	AUTOMUTE_TIME_LEFT	R/W	000	Auto Mute Time for Left Channel These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96kHz sampling rate and scales with other rates. 000: 11.5ms 001: 53ms 010: 106.5ms 011: 266.5ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0	This bit is reserved
2-0	AUTOMUTE_TIME_RIGHT	R/W	000	Auto Mute Time for Right Channel These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96kHz sampling rate and scales with other rates. 000: 11.5ms 001: 53ms 010: 106.5ms 011: 266.5ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

8.1.24 ANA_CTRL Register (Offset = 53h) [reset = 0h]

ANA_CTRL is shown inFigure 8-24 and described in Table 8-26

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Figure 8-24. ANA_CTRL Register

7	6	5	4	3	2	1	0
AMUTE_DLY							
R/W							

Table 8-26. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved

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Table 8-26. ANA_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	Class D bandwidth control	R/W	00	00: 100kHz 01: 80kHz 10: 120kHz 11:175kHz With Fsw=384kHz, 100kHz bandwidth is selected for high audio performance. With Fsw=768kHz, 175kHz bandwidth is selected for high audio performance.
4-1	RESERVED	R/W	0000	These bits are reserved
0	L and R PWM output phase control	R/W	0	0: out of phase 1: in phase

8.1.25 AGAIN Register (Offset = 54h) [reset = 0x00]

AGAIN is shown in Figure 8-25 and described in Table 8-27.

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Figure 8-25. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED			ANA_GAIN				
R/W			R/W				

Table 8-27. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control This bit controls the analog gain. 00000: 0dB (29.5V peak voltage) 00001:-0.5db 11111: -15.5dB

8.1.26 PVDD_ADC Register (Offset = 5Eh) [reset = 0h]

PVDD_ADC is shown in Figure 8-26 and described in Table 8-28.

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Figure 8-26. PVDD_ADC Register

7	6	5	4	3	2	1	0
ADC_DATA_OUT							
R							

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Table 8-28. PVDD_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PVDD_ADC[7:0]	R	00000000	PVDD Voltage = PVDD_ADC[7:0] / 8.428 (V) 223: 26.45V 222: 26.34V 221:26.22V ... 39: 4.63V 38: 4.51V 37: 4.39V

8.1.27 GPIO_CTRL Register (Offset = 60h) [reset = 0x00]

GPIO_CTRL is shown in Figure 8-27 and described in Table 8-29.

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Figure 8-27. GPIO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					GPIO0_OE	GPIO2_OE	GPIO1_OE
R/W					R/W	R/W	R/W

Table 8-29. GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0000	This bit is reserved
2	GPIO0_OE	R/W	0	GPIO0 Output Enable. This bit sets the direction of the GPIO0 pin 0: GPIO0 is input 1: GPIO0 is output
1	GPIO2_OE	R/W	0	GPIO2 Output Enable This bit sets the direction of the GPIO2 pin 0: GPIO2 is input 1: GPIO2 is output
0	GPIO1_OE	R/W	0	GPIO1 Output Enable This bit sets the direction of the GPIO1 pin 0: GPIO1 is input 1: GPIO1 is output

8.1.28 GPIO1_SEL Register (Offset = 61h) [reset = 0x00]

GPIO1_SEL is shown in Figure 8-28 and described in Table 8-30.

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Figure 8-28. GPIO1_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO1_SEL			
R/W				R/W			

Table 8-30. GPIO1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved

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Table 8-30. GPIO1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	GPIO1_SEL	R/W	0000	0000: off (low) 1000: GPIO1 as WARNZ output 1001: GPIO1 as Serial audio interface data output (SDOUT) 1011: GPIO1 as FAULTZ output 1100: GPIO1 as PVDD Drop Detection Flag 1101: GPIO1 as Class-H

8.1.29 GPIO2_SEL Register (Offset = 62h) [reset = 0x00]

GPIO2_SEL is shown in Figure 8-29 and described in Table 8-31.

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Figure 8-29. GPIO2_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO2_SEL			
R/W				R/W			

Table 8-31. GPIO2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-0	GPIO2_SEL	R/W	0000	0000: off (low) 1000: GPIO2 as WARNZ output 1001: GPIO2 as Serial audio interface data output (SDOUT) 1011: GPIO2 as FAULTZ output 1100: GPIO2 as PVDD Drop Detection Flag 1101: GPIO2 as Class-H

8.1.30 GPIO0_SEL Register (Offset = 63h) [reset = 0x00]

GPIO0_SEL is shown in Figure 8-30 and described in Table 8-32.

Return to Summary Table.

Figure 8-30. GPIO0_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO0_SEL			
R/W				R/W			

Table 8-32. GPIO0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-0	GPIO0_SEL	R/W	0000	0000: off (low) 1000: GPIO0 as WARNZ output 1001: GPIO0 as Serial audio interface data output (SDOUT) 1011: GPIO0 as FAULTZ output 1100: GPIO0 as PVDD Drop Detection Flag 1101: GPIO0 as Class-H

8.1.31 GPIO_INPUT_SEL Register (Offset = 64h) [reset = 0x00]

GPIO_INPUT_SEL is shown in Figure 8-31 and described in Table 8-33.

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Figure 8-31. GPIO_INPUT_SEL Register

7	6	5	4	3	2	1	0
GPIO_SPI_POCI_SEL		GPIO_PHASE_SYNC_SEL		GPIO_RESETZ_SEL		GPIO_MUTEZ_SEL	
R/W		R/W		R/W		R/W	

Table 8-33. GPIO_INPUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GPIO_SPI_POCI_SEL	R/W	00	00: N/A 01: GPIO1 10: GPIO2 11: GPIO0
5-4	GPIO_PHASE_SYNC_SEL	R/W	00	00: N/A 01: GPIO1 10: GPIO2 11: GPIO0
3-2	GPIO_RESETZ_SEL	R/W	00	00: N/A 01: GPIO1 10: GPIO2 11: GPIO0 can not be reset by GPIO reset
1-0	GPIO_MUTEZ_SEL	R/W	00	00: N/A 01: GPIO1 10: GPIO2 11: GPIO0 MUTEZ pin active-low, output driver is set to HiZ state, Class D amplifier's output stop switching.

8.1.32 GPIO_OUT Register (Offset = 65h) [reset = 0x00]

GPIO_OUT is shown in Figure 8-32 and described in Table 8-34.

Return to Summary Table.

Figure 8-32. GPIO_OUT Register

7	6	5	4	3	2	1	0
RESERVED					GPIO_OUT		
R/W					R/W		

Table 8-34. GPIO_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2-0	GPIO_OUT	R/W	000	bit0: GPIO1 output bit1: GPIO2 output bit2: GPIO0 output

8.1.33 GPIO_OUT_INV Register (Offset = 66h) [reset = 0x00]

GPIO_OUT_INV is shown in Figure 8-33 and described in Table 8-35.

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Figure 8-33. GPIO_OUT_INV Register

7	6	5	4	3	2	1	0
RESERVED					GPIO_OUT		

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Figure 8-33. GPIO_OUT_INV Register (continued)

R/W	R/W

Table 8-35. GPIO_OUT_INV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2-0	GPIO_OUT	R/W	000	bit0: GPIO1 output invert bit1: GPIO2 output invert bit2: GPIO0 output invert

8.1.34 DIE_ID Register (Offset = 67h) [reset = 95h]

DIE_ID is shown in Figure 8-34 and described in Table 8-36.

Return to Summary Table.

Figure 8-34. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R							

Table 8-36. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	10010101	DIE ID

8.1.35 POWER_STATE Register (Offset = 68h) [reset = 0x00]

POWER_STATE is shown in Figure 8-35 and described in Table 8-37.

Return to Summary Table.

Figure 8-35. POWER_STATE Register

7	6	5	4	3	2	1	0
STATE_RPT							
R							

Table 8-37. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STATE_RPT	R	00000000	0: Deep sleep 1: Seep 2: HIZ 3: Play Others: reserved

8.1.36 AUTOMUTE_STATE Register (Offset = 69h) [reset = 0x00]

AUTOMUTE_STATE is shown in Figure 8-36 and described in Table 8-38.

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Figure 8-36. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0

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Figure 8-36. AUTOMUTE_STATE Register (continued)

RESERVED	ZERO_RIGHT_MON	ZERO_LEFT_MON
R	R	R

Table 8-38. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	This bit is reserved
1	ZERO_RIGHT_MON	R	0	This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted
0	ZERO_LEFT_MON	R	0	This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted

8.1.37 PHASE_CTRL Register (Offset = 6Ah) [reset = 0]

PHASE_CTRL is shown in Figure 8-37 and described in Table 8-39.

Return to Summary Table.

Figure 8-37. PHASE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				RAMP_PHASE_SEL		PHASE_SYNC_SEL	PHASE_SYNC_EN
R/W				R/W		R/W	R/W

Table 8-39. PHASE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-2	RAMP_PHASE_SEL	R/W	00	select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, TI recommends to set all devices the same RAMP frequency and same spread spectrum. AMP frequency and spread spectrum must be set before driving device into PLAY mode if this feature is needed. 2'b00: phase 0 2'b01: phase 1 2'b10: phase 2 2'b11: phase 3 all of above have a 45 degree of phase shift
1	PHASE_SYNC_SEL	R/W	0	ramp phase sync sel, 0: is GPIO sync; 1: internal sync
0	PHASE_SYNC_EN	R/W	0	ramp phase sync enable

8.1.38 RAMP_SS_CTRL0 Register (Offset = 6Bh) [reset = 0x00]

RAMP_SS_CTRL0 is shown in Figure 8-38 and described in Table 8-40.

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Figure 8-38. SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	SS_PRE_DIV_SEL	SS_MANUAL_MODE	RESERVED		SS_RDM_EN	SS_TRI_EN

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Figure 8-38. SS_CTRL0 Register (continued)

R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-40. RAMP_SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	RESERVED	R/W	0	This bit is reserved
5	SS_PRE_DIV_SEL	R/W	0	Select pll clock divide 2 as source clock in manual mode
4	SS_MANUAL_MODE	R/W	0	Set ramp ss controller to manual mode
3-2	RESERVED	R/W	00	This bit is reserved
1	SS_RDM_EN	R/W	0	Random SS enable
0	SS_TRI_EN	R/W	0	Triangle SS enable

8.1.39 SS_CTRL1 Register (Offset = 6Ch) [reset = 0x00]

SS_CTRL1 is shown in Figure 8-39 and described in Table 8-41.

Return to Summary Table.

Figure 8-39. SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	SS_RDM_CTRL			SS_TRI_CTRL			
R/W	R/W			R/W			

Table 8-41. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	SS_RDM_CTRL	R/W	000	Add Dither
3-0	SS_TRI_CTRL	R/W	0000	Triangle SS frequency and range control

8.1.40 SS_CTRL2 Register (Offset = 6Dh) [reset = 0xA0]

SS_CTRL2 is shown in Figure 8-40 and described in Table 8-42.

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Figure 8-40. SS_CTRL2 Register

7	6	5	4	3	2	1	0
TM_FREQ_CTRL							
R/W							

Table 8-42. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TM_FREQ_CTRL	R/W	10100000	Control ramp frequency in manual mode, F=61440000/N

8.1.41 SS_CTRL3 Register (Offset = 6Eh) [reset = 0x11]

SS_CTRL3 is shown in Figure 8-41 and described in Table 8-43.

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Figure 8-41. SS_CTRL3 Register

7	6	5	4	3	2	1	0
TM_DSTEP_CTRL				TM_USTEP_CTRL			
R/W				R/W			

Table 8-43. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SS_TM_DSTEP_CTRL	R/W	0001	Control triangle mode spread spectrum fall step in ramp ss manual mode
3-0	SS_TM_USTEP_CTRL	R/W	0001	Control triangle mode spread spectrum rise step in ramp ss manual mode

8.1.42 SS_CTRL4 Register (Offset = 6Fh) [reset = 0x24]

SS_CTRL4 is shown in Figure 8-42 and described in Table 8-44.

Return to Summary Table.

Figure 8-42. SS_CTRL4 Register

7	6	5	4	3	2	1	0
RESERVED	TM_AMP_CTRL		SS_TM_PERIOD_BOUNDRY				
R/W	R/W		R/W				

Table 8-44. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	TM_AMP_CTRL	R/W	01	Control ramp amp ctrl in ramp ss manual model
4-0	SS_TM_PERIOD_BOUNDRY	R/W	00100	Control triangle mode spread spectrum boundary in ramp ss manual mode

8.1.43 CHAN_FAULT Register (Offset = 70h) [reset = 0x00]

CHAN_FAULT is shown in Figure 8-43 and described in Table 8-45.

Return to Summary Table.

Figure 8-43. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1_DC_1	CH2_DC_1	CH1_OC_I	CH2_OC_I
R				R	R	R	R

Table 8-45. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	This bit is reserved
3	CH1_DC_1	R	0	Left channel DC fault. Once there is a DC fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.

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Table 8-45. CHAN_FAULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CH2_DC_1	R	0	Right channel DC fault. Once there is a DC fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.
1	CH1_OC_I	R	0	Left channel over current fault. Once there is a OC fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.
0	CH2_OC_I	R	0	Right channel over current fault. Once there is a OC fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.

8.1.44 GLOBAL_FAULT1 Register (Offset = 71h) [reset = 0h]

GLOBAL_FAULT1 is shown in Figure 8-44 and described in Table 8-46.

Return to Summary Table.

Figure 8-44. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
OTP_CRC_ERROR	BQ_WR_ERROR	LOAD_EEPROM_ERROR	RESERVED	RESERVED	CLK_FAULT_I	PVDD_OV_I	PVDD_UV_I
R	R	R	R	R	R	R	R

Table 8-46. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTP_CRC_ERROR	R	0	Indicate OTP CRC check error.
6	BQ_WR_ERROR	R	0	The recent BQ is written failed
5	LOAD_EEPROM_ERROR	R	0	0: EEPROM boot load is done successfully 1: EEPROM boot load is done unsuccessfully
4	RESERVED	R	0	This bit is reserved
3	RESERVED	R	0	This bit is reserved
2	CLK_FAULT_I	R	0	Clock fault. Once there is a Clock fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). Clock fault works with an auto-recovery mode, once the clock error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.
1	PVDD_OV_I	R	0	PVDD OV fault. Once there is a OV fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.

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Table 8-46. GLOBAL_FAULT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PVDD_UV_I	R	0	PVDD UV fault. Once there is a UV fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.

8.1.45 GLOBAL_FAULT2 Register (Offset = 72h) [reset = 0h]

GLOBAL_FAULT2 is shown in Figure 8-45 and described in Table 8-47.

Return to Summary Table.

Figure 8-45. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED					CBC_FAULT_CH2_I	CBC_FAULT_CH1_I	OTSD_I
R					R	R	R

Table 8-47. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0000	This bit is reserved
2	CBC_FAULT_CH2_I	R	0	Right channel cycle by cycle over current fault
1	CBC_FAULT_CH1_I	R	0	Left channel cycle by cycle over current fault
0	OTSD_I	R	0	Over temperature shut down fault. Once there is an OT fault, this bit is set to be 1. Class D output is set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (GPIO). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Section 8.1.51 to 1 or this bit keeps 1.

8.1.46 WARNING Register (Offset = 73h) [reset = 0x00]

WARNING is shown in Figure 8-46 and described in Table 8-48.

Return to Summary Table.

Figure 8-46. WARNING Register

7	6	5	4	3	2	1	0
RESERVED		CBCW_CH1_I	CBCW_CH2_I	OTW_LEVEL4_I	OTW_LEVEL3_I	OTW_LEVEL2_I	OTW_LEVEL1_I
R		R	R	R	R	R	R

Table 8-48. WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0	This bit is reserved
5	CBCW_CH1_I	R	0	Left channel cycle by cycle over current warning
4	CBCW_CH2_I	R	0	Right channel cycle by cycle over current warning

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Table 8-48. WARNING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OTW_LEVEL4_I	R	0	Over temperature warning leve4, 146C
2	OTW_LEVEL3_I	R	0	Over temperature warning leve3, 134C
1	OTW_LEVEL2_I	R	0	Over temperature warning leve2, 122C
0	OTW_LEVEL1_I	R	0	Over temperature warning leve1, 112C

8.1.47 PIN_CONTROL1 Register (Offset = 74h) [reset = 0x00]

PIN_CONTROL1 is shown in Figure 8-47 and described in Table 8-49.

Return to Summary Table.

Figure 8-47. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDD_UV	MASK_DVDD_OV	MASK_CLK_FAULT	RESERVED	MASK_PVDD_UV	MASK_DC	MASK_OC
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Table 8-49. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0	Mask OTSD fault report
6	MASK_DVDD_UV	R/W	0	Mask DVDD UV fault report
5	MASK_DVDD_OV	R/W	0	Mask DVDD OV fault report
4	MASK_CLK_FAULT	R/W	0	Mask clock fault report
3	RESERVED	R	0	This bit is reserved
2	MASK_PVDD_UV	R/W	0	Mask PVDD UV fault report mask PVDD OV fault report
1	MASK_DC	R/W	0	Mask DC fault report
0	MASK_OC	R/W	0	Mask OC fault report

8.1.48 PIN_CONTROL2 Register (Offset = 75h) [reset = 0xF8]

PIN_CONTROL2 is shown in Figure 8-48 and described in Table 8-50.

Return to Summary Table.

Figure 8-48. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
CBC_FAULT_LATCH_EN	CBC_WARN_LATCH_EN	CLKFLT_LATCH_EN	OTSD_LATCH_EN	OTW_LATCH_EN	MASK_OTW	MASK_CBCW	MASK_CBC_FAULT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-50. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CBC_FAULT_LATCH_EN	R/W	1	Enable CBC fault latch by setting this bit to 1
6	CBC_WARN_LATCH_EN	R/W	1	Enable CBC warning latch by setting this bit to 1
5	CLKFLT_LATCH_EN	R/W	1	Enable clock fault latch by setting this bit to 1
4	OTSD_LATCH_EN	R/W	1	Enable OTSD fault latch by setting this bit to 1

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Table 8-50. PIN_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OTW_LATCH_EN	R/W	1	Enable OT warning latch by setting this bit to 1
2	MASK_OTW	R/W	0	Mask OT warning report by setting this bit to 1
1	MASK_CBCW	R/W	0	Mask CBC warning report by setting this bit to 1
0	MASK_CBC_FAULT	R/W	0	Mask CBC fault report by setting this bit to 1

8.1.49 MISC_CONTROL Register (Offset = 76h) [reset = 0x00]

MISC_CONTROL is shown in Figure 8-49 and described in Table 8-51.

Return to Summary Table.

Figure 8-49. MISC_CONTROL Register

7	6	5	4	3	2	1	0
DET_STATUS_LATCH	RESERVED		OTSD_AUTO_REC_EN	RESERVED			
R/W	R/W		R/W	R/W			

Table 8-51. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DET_STATUS_LATCH	R/W	0	1:Latch clock detection status 0:Don't latch clock detection status
6-5	RESERVED	R/W	00	These bits are reserved
4	OTSD_AUTO_REC_EN	R/W	0	OTSD auto recovery enable
3-0	RESERVED	R/W	0000	This bit is reserved

8.1.50 CBC_CONTROL Register (Offset = 77h) [reset = 0x00]

CBC_CONTROL is shown in Figure 8-50 and described in Table 8-52.

Return to Summary Table.

Figure 8-50. CBC_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED			CBC_LEVEL_SEL		CBC_EN	CBC_WARN_EN	CBC_FAULT_EN
R/W			R/W		R/W	R/W	R/W

Table 8-52. CBC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	These bits are reserved
4-3		CBC_LEVEL_SEL	00	This bit sets CBC level, which is percentage to Over-Current Threshold: 00: 80% 10: 60% 01: 40%
2	CBC_EN	R/W	0	Enable CBC function
1	CBC_WARN_EN	R/W	0	Enable CBC warning
0	CBC_FAULT_EN	R/W	0	Enable CBC fault

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8.1.51 FAULT_CLEAR Register (Offset = 78h) [reset = 0x00]

FAULT_CLEAR is shown in Figure 8-51 and described in Table 8-53.

Return to Summary Table.

Figure 8-51. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
ANALOG_FAULT_CLEAR	RESERVED						
W	R/W						

Table 8-53. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ANALOG_FAULT_CLEAR	W	0	WRITE CLEAR BIT once write this bit to 1, device clears analog fault
6-0	RESERVED	R/W	0000000	This bit is reserved

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5828M device into the larger system.

9.1.1 Inductor Selections

A requirement is that the peak current is smaller than the OCP (Over current protection) value which is 7.5A, there are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to θ. There is a start-up current which flow through inductor to set up the common mode voltage (PVDD×θ).

Note

θ = 0.5 (BD Modulation), 0.14 (1 SPW Modulation), 0.14 (Hybrid Modulation)

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping causes PWM duty cycle increase dramatically. This is the worst case and rarely happens.

$$I_{peak_clipping} \cong PVDD \times [1 - \theta] \div [F_{SW} \times L] \quad (1)$$

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak_output_power} \cong \sqrt{2 \times Max_Output_Power \div R_{speaker_Load}} \quad (2)$$

TI suggests that inductor saturation current I_{sat}, is larger than the amplifier peak current during power-up and play audio.

$$I_{SAT} \geq \max\left[I_{peak_power_up}, I_{peak_clipping}, I_{peak_output_power}\right] \quad (3)$$

Table 9-1. Inductor Requirements

PVDD (V)	Switching Frequency (kHz)	Minimum Inductance (L) (µH)
≤ 12	384	4.7
> 12	384	10

For higher switching frequencies (Fsw), select the inductors with minimum inductance to be 384kHz / Fsw × L. Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation.

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9.1.2 Bootstrap Capacitors

The output stage of the TAS5828M uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.47-µF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.47-µF capacitor between OUT_A and BST_A for bootstrapping the A channel. Similarly, connect another 0.47-µF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

9.1.3 Power Supply Decoupling

To maintain high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22µF. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1µF or 0.1µF capacitors as close as possible to the PVDD pins of the device.

9.1.4 Output EMI Filtering

The device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report Class-D LC Filter Design (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

For EMI performance and EMI Design consideration, reference to application report: TAS5825M Design Considerations for EMC.

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9.2 Typical Applications

9.2.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

Figure 9-1 shows the 2.0 (Stereo BTL) system application.

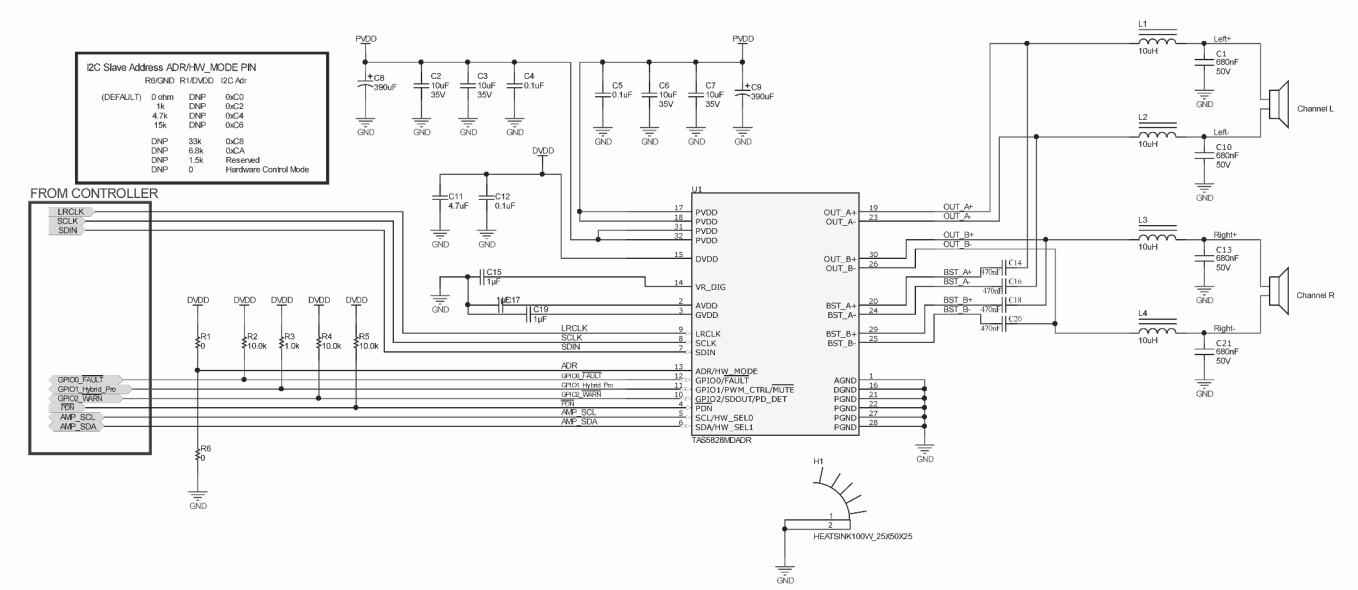

Figure 9-1. 2.0 (Stereo BTL) System Application Schematic

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9.2.2 Design Requirements

- Power supplies:
  - 3.3V supply
  - 5V to 24V supply
- Communication: host processor serving as I^2C compliant controller
- External memory (such as EEPROM and FLASH) used for coefficients.

The requirements for the supporting components for the TAS5828M device in a Stereo 2.0 (BTL) system is provide in Table 9-2.

Table 9-2. Supporting Component Requirements for Stereo 2.0 (BTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C8, C9	390µF	SMD	CAP, AL, 390uF, 35V, ± 20%, SMD
C4,C5	0.1µF	0402	CAP, CERM, 10uF, 35V, ± 10%, X5R, 0805
C2,C3, C6, C7	10µF	0805	CAP,CERM, 22µF, 35V, ±20%, JB, 0805
C11	4.7µF	0603	CAP,CERM, 4.7µF, 10V, ±10%, X5R, 0603
C12	0.1µF	0603	CAP,CERM, 0.1µF, 16V, ±10%, X7R, 0603
C15,C17, C19	1µF	0603	CAP,CERM, 1µF, 16V, ±10%, X5R, 0603
C14,C16, C18, C20	0.47µF	0603	CAP,CERM, 0.47µF, 16V, ±10%, X7R, 0603
C1,C10, C13, C21	0.68µF	0805	CAP,CERM, 0.68µF, 50V, ±10%, X7R, 0805
L1,L2, L3, L4	10µH		Inductor, Shielded Drum Core, Ferrite, 10uH, 7.1A, 0.01294ohm, SMD, 7447709100
R1, R6	0Ω	0402	RES,0, 5%, 0.063W, 0402
R2,R4, R5	10kΩ	0402	RES,10.0k, 1%, 0.063W, 0402
R3	1kΩ	0402	RES,1.0k, 1%, 0.063W, 0402

9.2.3 Detailed Design procedures

This Design procedures can be used for both Stereo 2.0, Advanced 2.1 and Mono Mode.

9.2.3.1 Step One: Hardware Integration

- Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout, and routing given in the example layout above, integrate the device and supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to maintain a given precedent as design trade-offs are made is recommended.
  - For questions and support go to the E2E forums (e2e.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

9.2.3.2 Step Two: Hardware Integration

Using the TAS5828MEVM evaluation module and the PPC3 app to configure the desired device settings.

9.2.3.3 Step Three: Software Integration

- Using the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

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9.2.4 MONO (PBTL) Systems

In MONO mode, TAS5828M can be used as PBTL mode to drive sub-woofer with more output power.

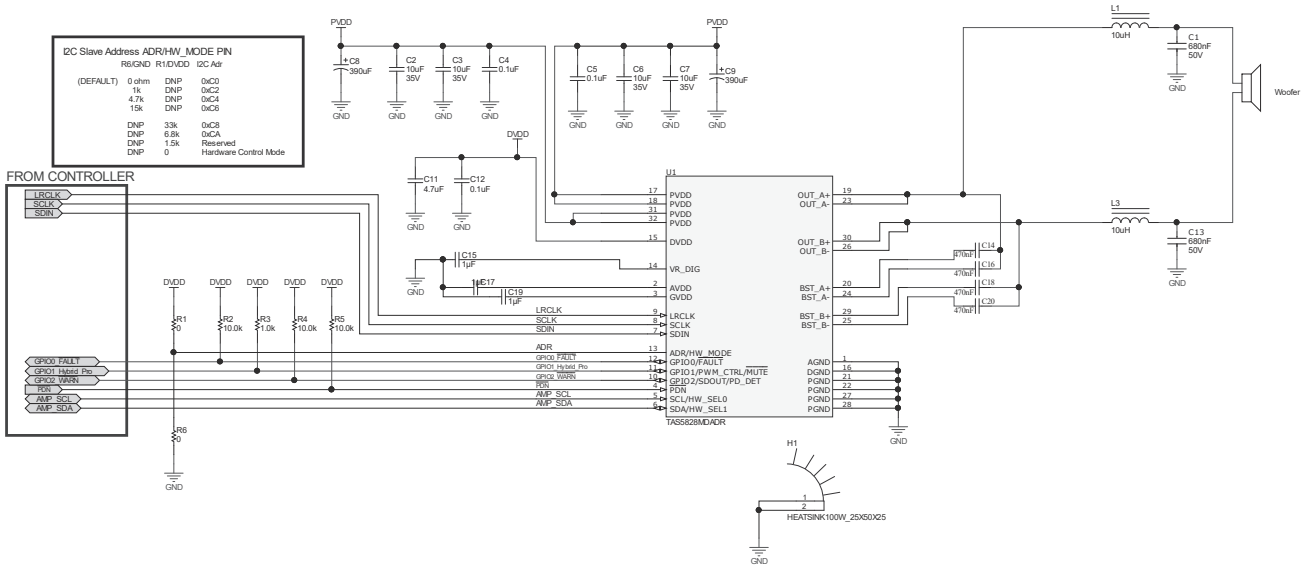

Figure 9-2. Sub-woofer (PBTL) Application Schematic

Table 9-3. Supporting Component Requirements for Sub-woofer (PBTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C8, C9	390μF	SMD	CAP, AL, 390uF, 35V, ± 20%, SMD
C4, C5	0.1μF	0402	CAP, CERM, 0.1uF, 35V, ± 10%, X5R, 0805
C2, C3, C6, C7	10μF	0805	CAP,CERM, 10μF, 35V, ±20%, JB, 0805
C11	4.7μF	0603	CAP,CERM, 4.7μF, 10V, ±10%, X5R, 0603
C12	0.1μF	0603	CAP,CERM, 0.1μF, 16V, ±10%, X7R, 0603
C15, C17, C19	1μF	0603	CAP,CERM, 1μF, 16V, ±10%, X5R, 0603
C14, C16, C18, C20	0.47μF	0603	CAP,CERM, 0.47μF, 16V, ±10%, X7R, 0603
C1, C13	0.68μF	0805	CAP,CERM, 0.68μF, 50V, ±10%, X7R, 0805
L1, L3	10μH		Inductor, Shielded Drum Core, Ferrite, 10uH, 7.1A, 0.01294Ω, SMD, 7447709100
R1, R6	0Ω	0402	RES, 0, 5%, 0.063W, 0402
R2, R4, R5	10kΩ	0402	RES, 10.0kΩ, 1%, 0.063W, 0402

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9.2.5 Advanced 2.1 System (Two TAS5828M Devices)

In higher performance systems, the subwoofer output can be enhanced using digital audio processing as was done in the high-frequency channels. To accomplish this, two TAS5828M devices are used - one for the high frequency left and right speakers and one for the mono subwoofer speaker. In this system, the audio signal can be sent from the TAS5828M device through the SDOUT pin. Alternatively, the subwoofer amplifier can accept the same digital input as the stereo, which can come from a central systems processor.Figure 9-3 shows the 2.1 (Stereo BTL with Two TAS5828M devices) system application.

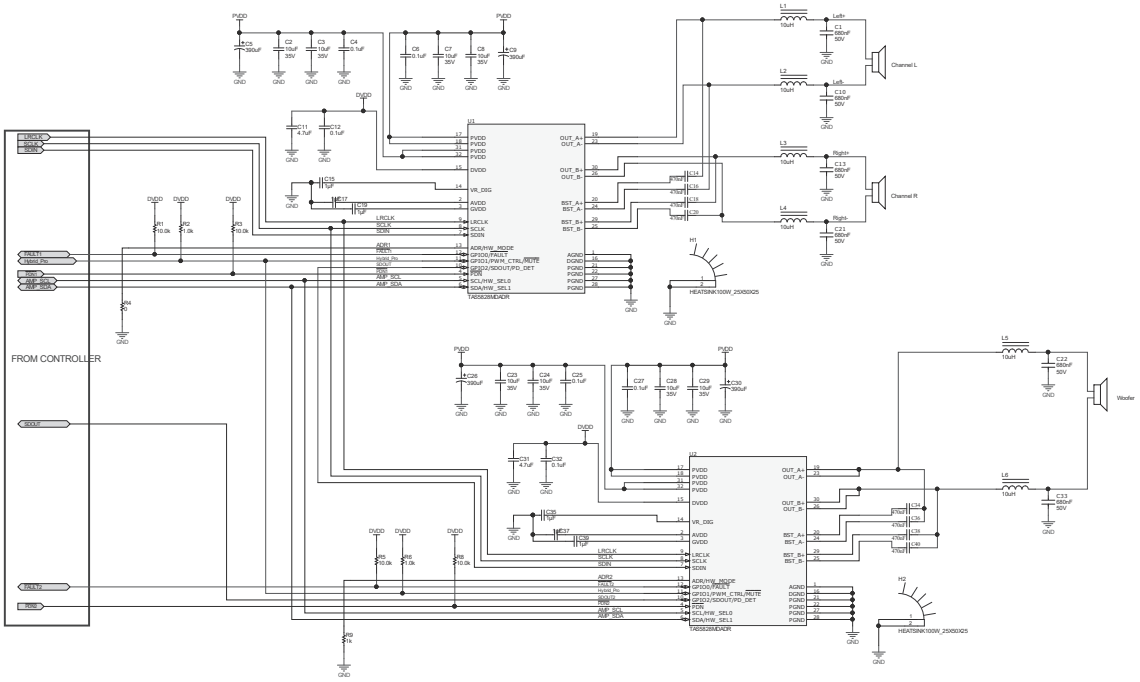

Figure 9-3. 2.1 (2.1 CH with Two TAS5828M Devices) Application Schematic

9.3 Power Supply Recommendations

The TAS5828M device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and the associated circuitry. Additionally, one low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the *Recommended Operating Conditions* table. The two power supplies do not have a required powerup sequence. The power supplies can be powered on in any order.

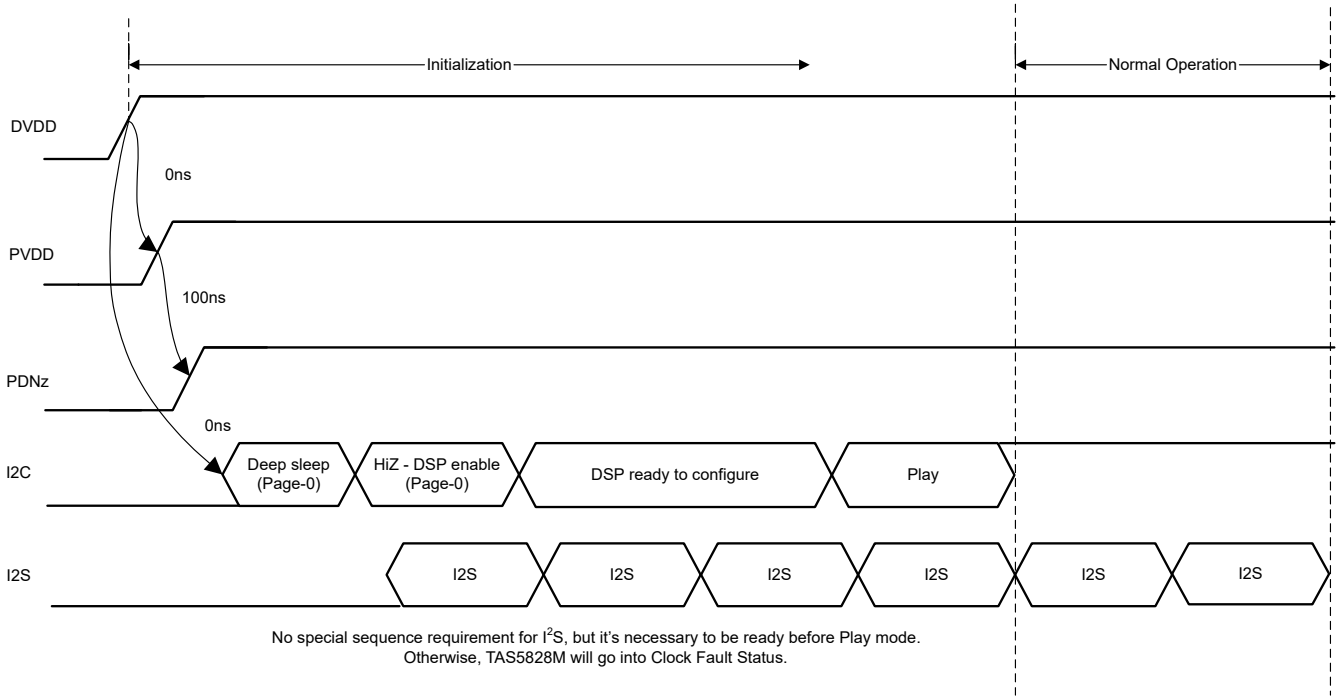

Figure 9-4. Power Supply Function Block Diagram

9.3.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in Figure 9-4, the DVDD supply provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the *Application and Implementation* section and the *Layout Example* section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5828M device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and the linear regulators output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. Note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and is not to be used to power any additional external circuity. Additional loading on this pin can cause the voltage to sag, negatively affecting the performance and operation of the device.

9.3.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5828MEVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, properly decoupling the output power stages in the manner described in the TAS5828M device *Application and Implementation* is particularly important. Lack of proper decoupling, like that shown in the *Application and Implementation*, results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. Noting that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and is not be used to power any additional external circuitry is important. Additional loading on this pin causes the voltage to sag, negatively affecting the performance and operation of the device.

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Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5828M internal circuitry. Noting that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry is important, and is not be used to power any additional external circuitry. Additional loading on this pin causes the voltage to sag, negatively affecting the performance and operation of the device.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to the audio amplifiers layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

The guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in the *Layout Example* section. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, design size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, TI recommends to start from the guidance shown in the *Layout Example* section and work with TI field application engineers or through the E2E community to modify the layout based upon the application specific goals.

9.4.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, GVDD and PVDD. However, the capacitors on the PVDD net for the TAS5828M device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only does placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5828M device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from the capacitors associated PVDD pins than what is shown in the example layouts in the *Layout Example* section.

9.4.1.3 Optimizing Thermal Performance

Follow the Layout Example section to achieve the best balance of design size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. The system designer maintains that the heat can get out of the device and into the ambient air surrounding the device. The TAS5828M device utilizes a TSSOP-DAD, pad up, package to maximize the thermal dissipation away from the device. Heat is transferred from the device to the ambient air through a low impedance heat sink path. The use of a heat sink is required. TI recommends using ATS-TI10P-519-C1-R3 from www.qats.com, shown in Figure 9-5. The size of the heat sink can deviate from the suggested heat sink in space constrained environments, but thermal performance can degrade.

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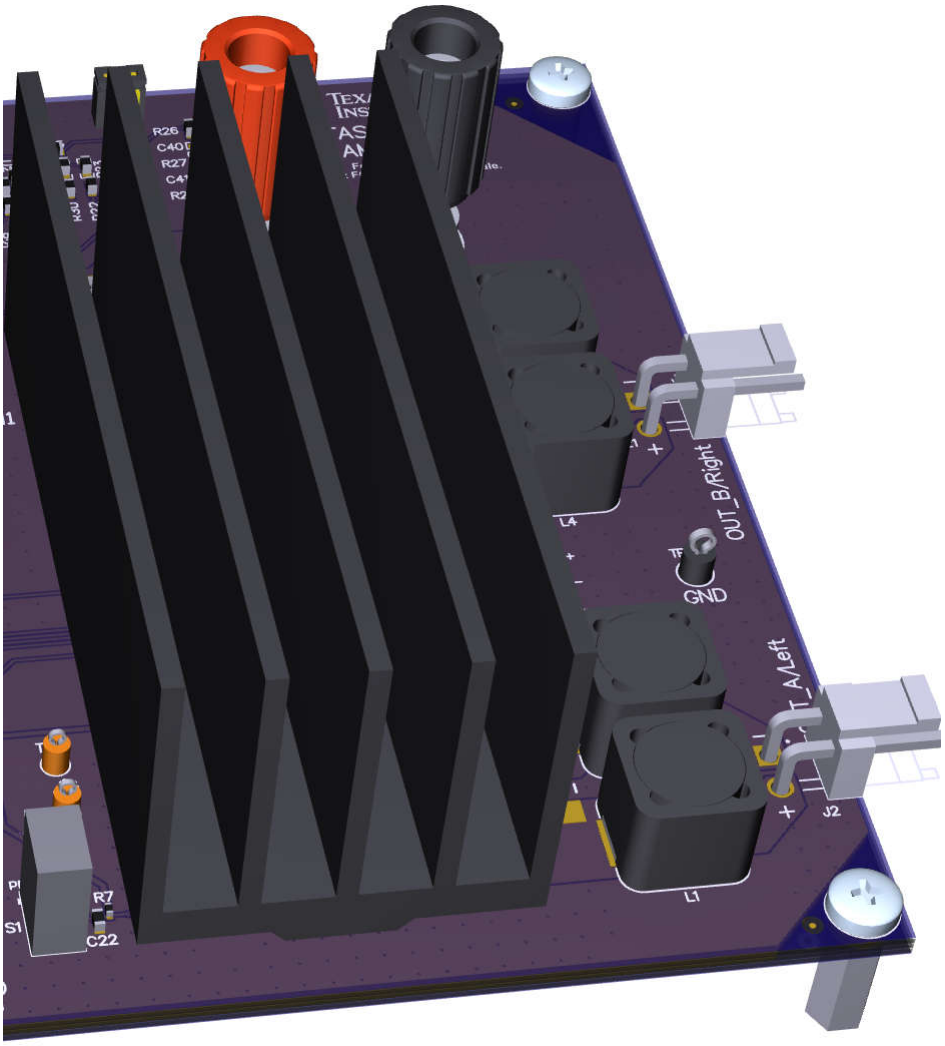

Figure 9-5. 2.0 (Stereo BTL) EVM 3D Top View with Heatsink

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9.4.2 Layout Example

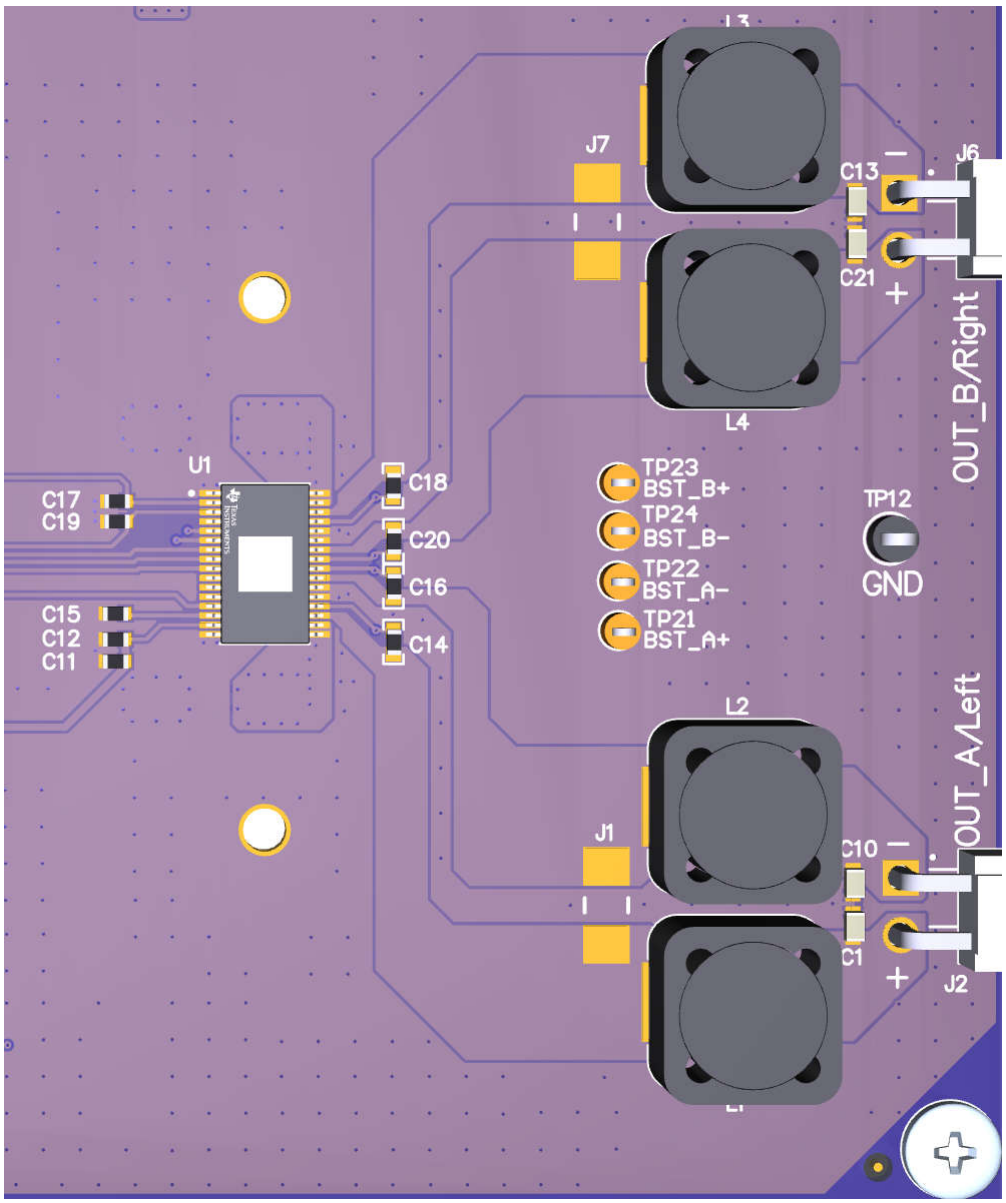
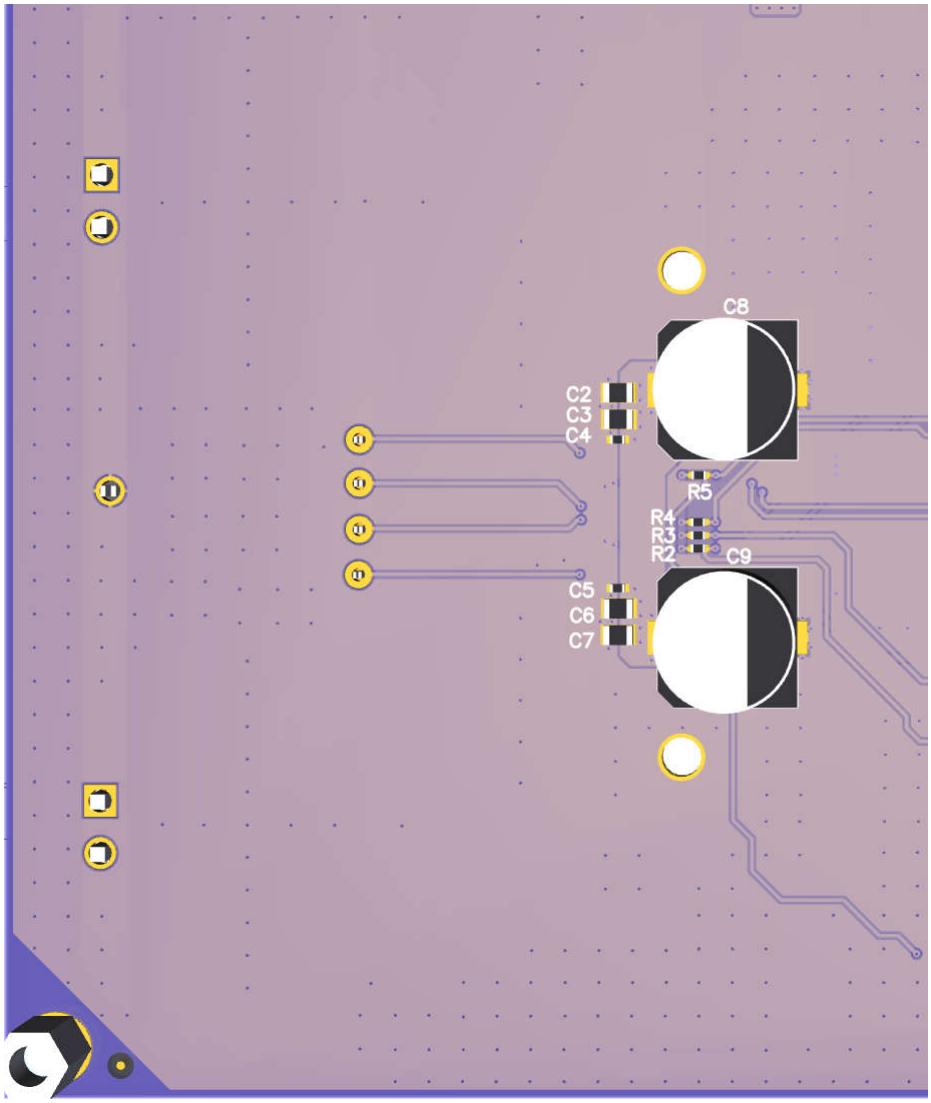


Figure 9-6. 2.0 (Stereo BTL) 3D Top View



Note

From bottom view. Flipped along Y-axis.

Figure 9-7. 2.0 (Stereo BTL) 3D Bottom View

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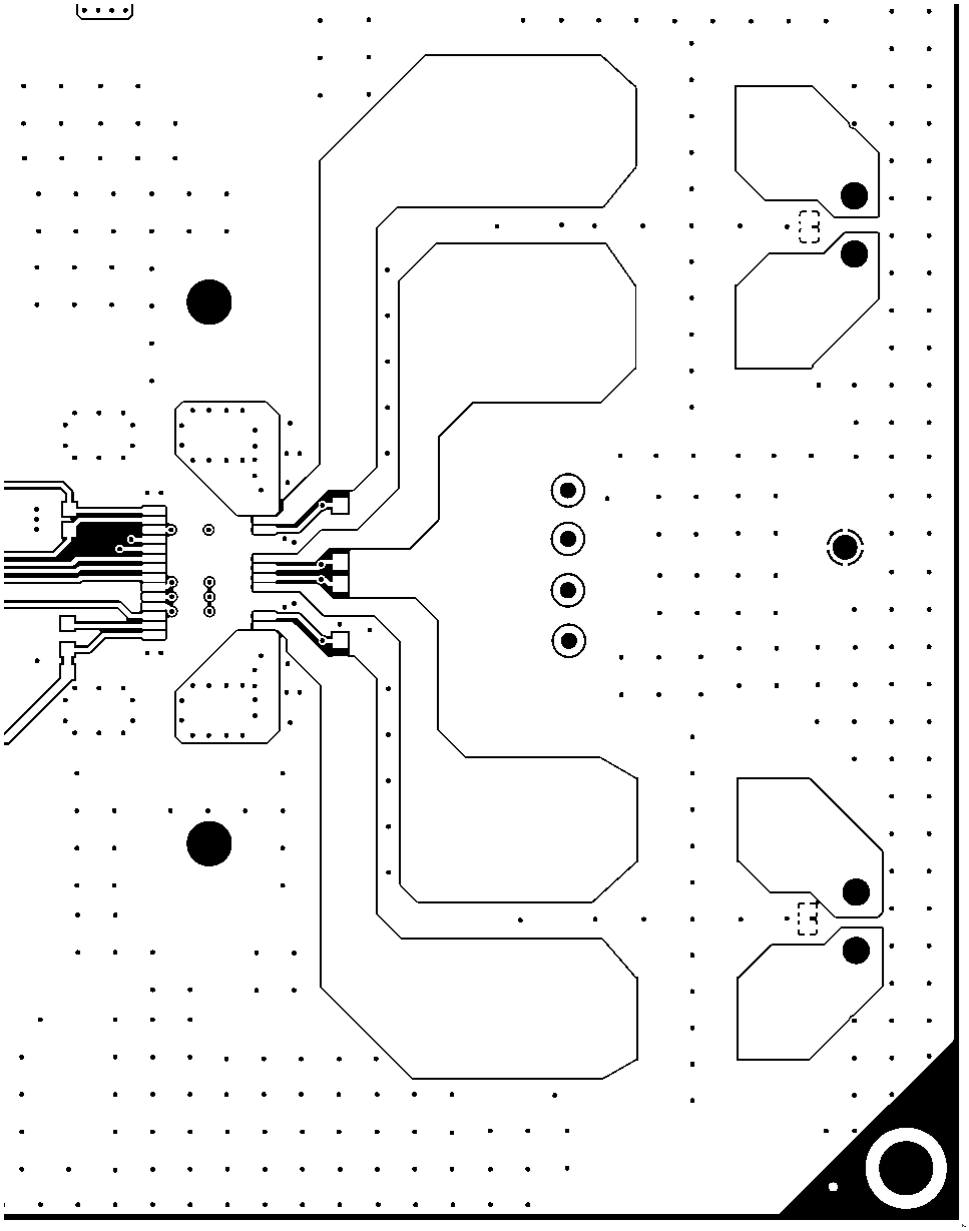

Figure 9-8. 2.0 (Stereo BTL) PCB Top Layer Plot (Top View)

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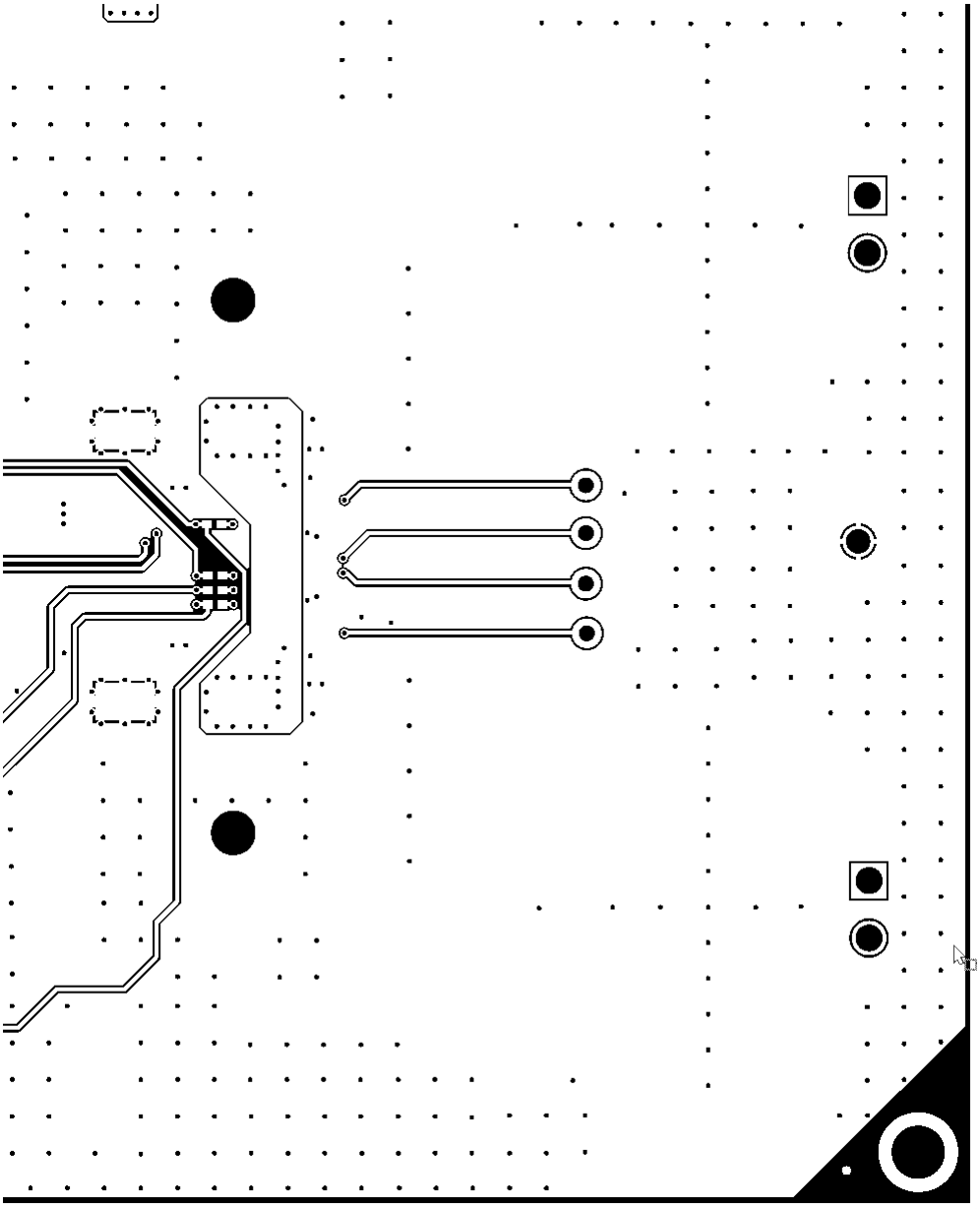

Figure 9-9. 2.0 (Stereo BTL) PCB Bottom Layer Plot (Top View)

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Device Nomenclature

The glossary section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplfier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin and is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to a device which serves as a central system controller, providing control information to connected devices as well as gathering audio source data from devices upstream from the device and distributing data to other devices. This device often configures the controls of the audio processing devices (like the TAS5828M) in the audio path to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that the amplifiers temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$r_{DS(on)}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

10.1.2 Development Support

For RDGUI software, please consult your local field support engineer.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2025) to Revision C (January 2026)	Page
• Updated thermal information	7
• Updated SIN_CH_CTRL Register	48
• Updated SIN_CH_CTRL Register Field Descriptions	48
• Updated Table 9-3	80

Changes from Revision A (December 2021) to Revision B (April 2025)	Page
• Change the Thermal Foldback description to be more clear	36
• Fixed DSP_PGM_MODE registers and other typos. Renamed DIG_VOL to DAC_GAIN	48
• Removed layout sections related to pad down packages	83
• Updated heat sink information and added image	83
• Updated layout images	85

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5828MDADR	Active	Production	HTSSOP (DAD) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TAS 5828M
TAS5828MDADR.A	Active	Production	HTSSOP (DAD) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TAS 5828M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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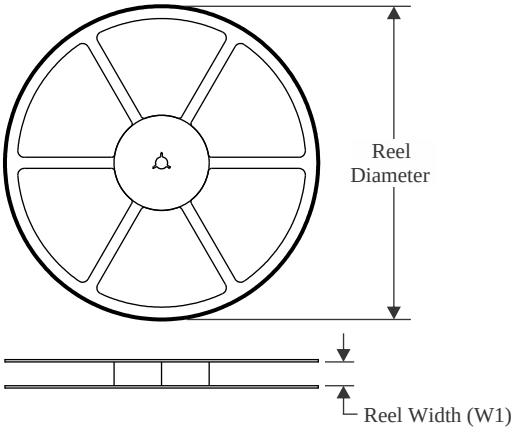
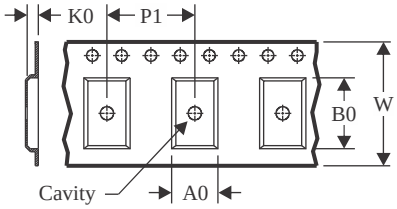
TAPE AND REEL INFORMATION

REEL DIMENSIONS

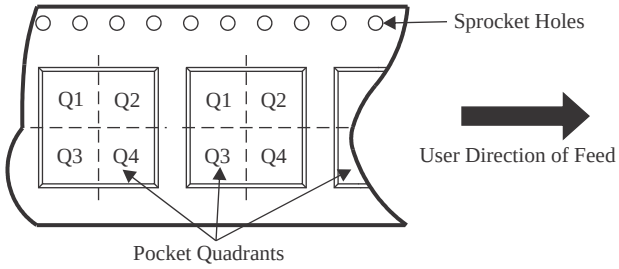


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

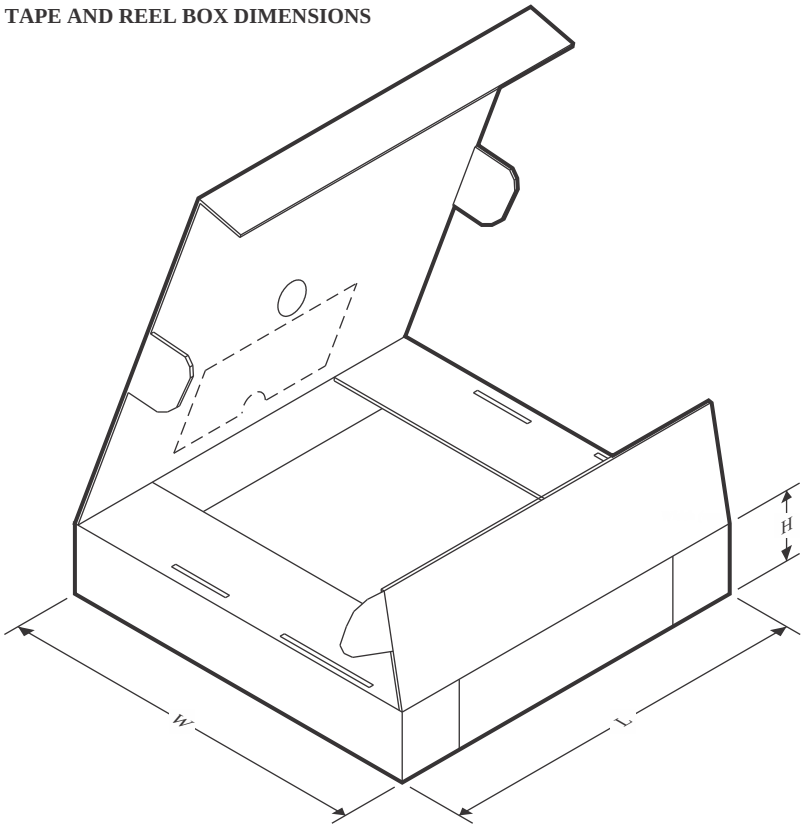
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5828MDADR	HTSSOP	DAD	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

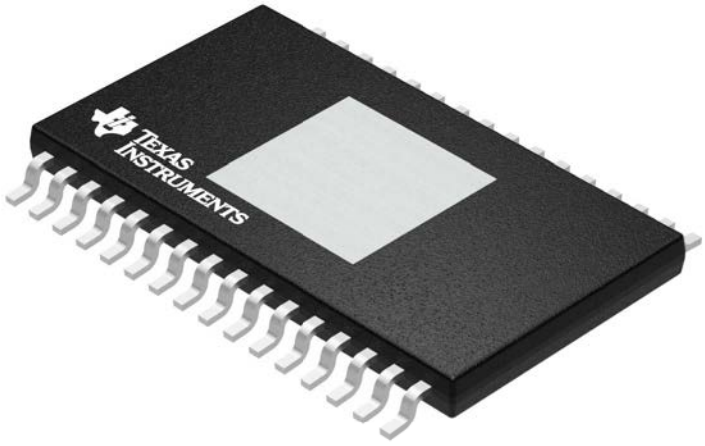


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5828MDADR	HTSSOP	DAD	32	2000	350.0	350.0	43.0

DAD 32 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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Last updated 10/2025