ISO1050 Isolated CAN Transceiver

1 Features

- Meets the requirements of ISO11898-2
- 5000-V_{RMS} isolation (ISO1050DW)
- 2500-V_{RMS} isolation (ISO1050DUB)
- Fail-safe outputs
- Low loop delay: 150 ns (typical), 210 ns (maximum)
- 50-kV/µs typical transient immunity
- Bus-fault protection of –27 V to 40 V
- Driver (TXD) dominant time-out function
- I/O voltage range supports 3.3 V and 5 V microprocessors
- Safety-related certifications
  - VDE approval per DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 approved
  - CSA approved for IEC 61010-1, IEC 60601-1
  - TUV Reinforced Insulation Approval for EN/UL/CSA 62368-1 (ISO1050DW-Only)
  - CQC reinforced insulation per GB4943.1 (ISO1050DW-only)
  - Typical 25-year life at rated working voltage (see application report SLLA197 and *Life Expectancy vs Working Voltage*)

2 Applications

- Industrial automation, control, sensors, and drive systems
- Building and climate control (HVAC) automation
- Security systems
- Transportation
- Medical
- Telecom
- CAN bus standards such as CANopen, DeviceNet, NMEA2000, ARINC825, ISO11783, CAN Kingdom, CANaerospace

3 Description

The ISO1050 is a galvanically isolated CAN transceiver that meets the specifications of the ISO11898-2 standard. The device has the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides galvanic isolation of up to 5000 V_{RMS} for ISO1050DW and 2500 V_{RMS} for ISO1050DUB. Used in conjunction with isolated power supplies, the device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

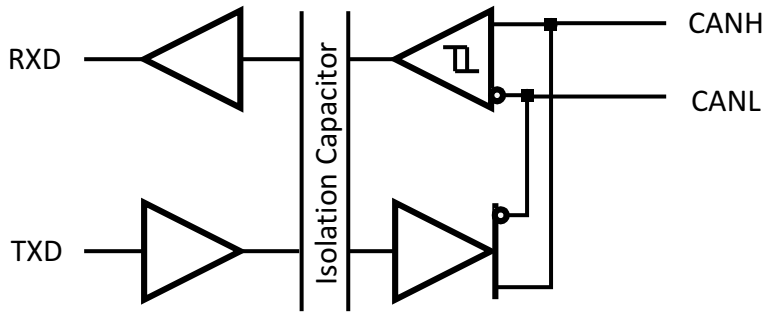
As a CAN transceiver, the device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). The device is designed for operation in especially harsh environments, and it features cross-wire, overvoltage and loss of ground protection from –27 V to 40 V and overtemperature shutdown, as well as –12V to 12V common-mode range.

The ISO1050 is characterized for operation over the ambient temperature range of –55°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE	PACKAGE SIZE ((2))
ISO1050	SOP (8)	9.5 mm × 10.4 mm
	SOIC (16)	10.3 mm × 10.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (August 2023) to Revision L (October 2023)	Page
• Updated Safety Related Certifications section	6
• Updated multiple Specifiaction sections	6

Changes from Revision J (September 2019) to Revision K (August 2023)	Page
• Changed VDE standard name to DIN EN IEC 60747-17 (VDE 0884-17), updated CSA standard to CSA 62368-1 and IEC 62368-1	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision I (September 2014) to Revision J (September 2019)	Page
• Changed VDE standard name From: DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 To: DIN VDE V 0884-11:2017-01 in Section 1	1
• Deleted 'Component Acceptance Notice 5 A' from CSA bullet in Section 1	1
• Changed inverting output label From: CANH To: CANL in Figure 7-10	14
• Changed VDE standard name From: DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 To: DIN VDE V 0884-11:2017-01 in INSULATION CHARACTERISTICS table	19
• Changed V_{ISO} PARAMETER description From: 'ISO1050DUB - Double Protection' To: 'ISO1050DUB - Single Protection' in INSULATION CHARACTERISTICS table	19
• Updated Regulatory Information in REGULATORY INFORMATION table	19
• Changed UL 1577 rating for ISO1050DUB From: '2500 V_{RMS} Double Protection' To: '2500 V_{RMS} Single Protection' in REGULATORY INFORMATION table	19
• Deleted UL 1577 'Double Protection' rating of 3500 V_{RMS} for ISO1050DW in REGULATORY INFORMATION table	19
• Added Section 10.2 section and SN6505 reference to Section 10	27
• Added SN6505x data sheet link to 'Transformer Driver for Isolated Power Supplies' in Section 12.1 section	29

Changes from Revision H (June 2013) to Revision I (September 2014) **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision G (March 2013) to Revision H (June 2013) **Page**

- Changed title From: LIFE EXPECTANCY vs WORKING VOLTAGE (ISO1050DW To: LIFE EXPECTANCY vs WORKING VOLTAGE (ISO1050DUB)..... 22

Changes from Revision F (January 2013) to Revision G (March 2013) **Page**

- Clarified clearance and creepage measurement method in ISOLATOR CHARACTERISTICS..... 19
- Clarified test methods for voltage ratings in INSULATION CHARACTERISTICS..... 19
- Changed UL Single Protection Certification pending to Single Protection in REGULATORY INFORMATION SECTION (certificate available)..... 19

Changes from Revision E (December 2011) to Revision F (January 2013) **Page**

- Deleted ISO1050L device..... 1
- Deleted ISO1050LDW from Features list..... 1
- Deleted ISO1050LDW in first paragraph of DESCRIPTION..... 1
- Added the PIN FUNCTIONS section..... 5
- Added Maximum impulse voltage (V_{IMP}) specification per DIN EN IEC 60747-17 (VDE 0884-17) 8
- Deleted ISO1050LDW from INSULATION CHARACTERISTICS..... 19
- Deleted ISO1050LDW from REGULATORY INFORMATION..... 19
- Added the FUNCTIONAL DESCRIPTION section..... 19
- Deleted ISO1050LDW from LIFE EXPECTANCY vs WORKING VOLTAGE 22
- Deleted 40V from the CANH and CANL input diagrams and output diagrams in the EQUIVALENT I/O SCHEMATICS 22
- Changed the APPLICATION INFORMATION section..... 24
- Changed the BUS LOADING, LENGTH AND NUMBER OF NODES section..... 24
- Added the CAN TERMINATION section..... 25

Changes from Revision D (June 2011) to Revision E (November 2011) **Page**

- Added device ISO1050L..... 1
- Changed (DW Package) in the Features list to (ISO1050DW)..... 1
- Changed (DUB Package) in the Features list to (ISO1050DUB and ISO1050LDW)..... 1
- Deleted IEC 60950-1 from the CSA Approvals Feature bullet..... 1
- From: IEC 60601-1 (Medical) and CSA Approvals Pending To: IEC 60601-1 (Medical) and CSA Approved ... 1
- Added Feature - 5 KVRMS Reinforced..... 1
- Changed DW Package to ISO105DW and DUB package to ISO1050DUB and ISO1050LDW in the first paragraph of DESCRIPTION..... 1
- Added Note 1 to the INSULATION CHARACTERISTICS table..... 19
- Changed V_{IORM} From: 8-DUB Package to ISO1050DUB and ISO1050LDW 19
- Changed V_{IORM} From: 16-DW to ISO1050DW 19
- Changed the V_{ISO} Isolation voltage per UL section of the INSULATION CHARACTERISTICS table..... 19
- Changed the IEC 60664-1 Ratings Table..... 19
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- Changed From: File Number: 220991 (Approval Pending) To: File Number: 220991..... 19
- Changed in note (1) 3000 to 2500 and 6000 to 5000..... 19
- Changed in LIFE EXPECTANCY vs WORKING VOLTAGE (8-DUB PACKAGE TO: LIFE.....(ISO1050DW and ISO1050LDW)..... 22

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- Changed the REGULATORY INFORMATION table.....19

Changes from Revision B (June 2010) to Revision C (July 2010) **Page**

- Changed the IEC 60747-5-2 Features bullet From: DW package Approval Pending To: VDE approved for both DUB and DW packages.....1
- Changed the Minimum Internal Gap value from 0.008 to 0.014 in the Isolator Characteristics table.....19
- Changed V_{IORM} Specification From: 1300 To: 1200 per VDE certification.....19
- Changed V_{PR} Specification From 2438 To: 2250.....19
- Added the Bus Loading paragraph to the Application Information section.....24

Changes from Revision A (Sept 2009) to Revision B (June 2010) **Page**

- Added information that IEC 60747-5-2 and IEC61010-1 have been approved.....1
- Changed DW package from preview to production data.....5
- Added Insulation Characteristics and IEC 60664-1 Ratings tables.....19
- Added IEC file number.....19

Changes from Revision * (June 2009) to Revision A (Sept 2009) **Page**

- Added Typical 25-Year Life at Rated Working Voltage to Features.....1
- Added LIFE EXPECTANCY vs WORKING VOLTAGE section.....22

5 Pin Configuration and Functions

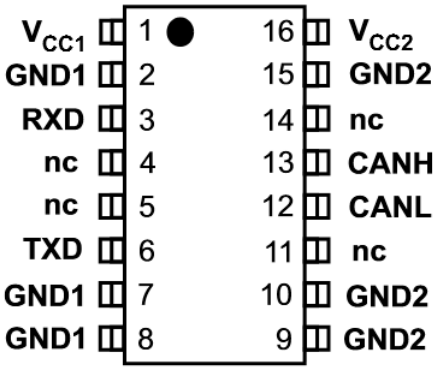


Figure 5-1. 16-Pin DW Package Top View

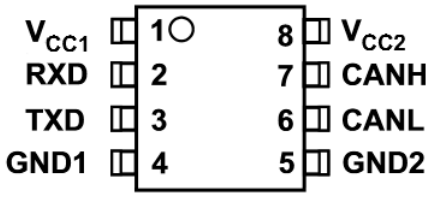


Figure 5-2. 8-Pin DUB Package Top View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DW	DUB		
V_{CC1}	1	1	Supply	Digital-side supply voltage (3 to 5.5 V)
GND1	2	—	Ground	Digital-side ground connection
RXD	3	2	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	4	—	NC	No connect
NC	5	—	NC	No connect
TXD	6	3	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND1	7	4	Ground	Digital-side ground connection
GND1	8	—	Ground	Digital-side ground connection
GND2	9	5	Ground	Transceiver-side ground connection
GND2	10	—	Ground	Transceiver-side ground connection
NC	11	—	NC	No connect
CANL	12	6	I/O	Low-level CAN bus line
CANH	13	7	I/O	High-level CAN bus line
NC	14	—	NC	No connect
GND2	15	—	Ground	Transceiver-side ground connection
V_{CC2}	16	8	Supply	Transceiver-side supply voltage (5 V)

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC1}	Supply voltage, side 1	-0.5	6	V
V_{CC2}	Supply voltage, side 2	-0.5	6	V
V_{IO}	Logic input voltage range (TXD)	-0.5	V_{CC1}+0.5(3)	V
V_{BUS}	Voltage on bus pins (CANH, CANL)	-27	40	V
I_O	Output current on RXD pin	-15	15	mA
T_J	Junction temperature	-55	150	℃
T_{STG}	Storage temperature	-65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins(1)	±4000	V
$V_{(ESD)}$	Electrostatic discharge Charged device model (CDM), per JEDEC specification JESD22-C101	All pins(2)	±1500	V
$V_{(ESD)}$	Electrostatic discharge Charged machine model, ANSI/ESDS5.2-1996	All pins(2)	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC1}	Supply Voltage, Side 1	3		5.5	V
V_{CC2}	Supply Voltage, Side 2	4.75		5.25	V
V_I or V_{IC}	Voltage at bus pins (separately or common mode)	-12		12	V
V_{IH}	High-level input voltage (TXD)	2		5.25	V
V_{IL}	Low-level input voltage (TXD)	0		0.8	V
V_{ID}	Differential input voltage	-7		7	V
I_{OH}	High-Level Output current, Driver	-70			mA
I_{OH}	High-Level Output current, Receiver	-4			mA
I_{OL}	Low-level output current, Driver			70	mA
I_{OL}	Low-level output current, Receiver			4	mA
T_A	Operating ambient temperature	-55		105	°C
T_J	Junction temperature	-55		125	°C
$T_{Jshutdown}$	Thermal shutdown temperature		190		°C

6.4 Thermal Information

THERMAL METRIC(1)		ISO1050		UNIT
		DW	DUB	
		16 PINS	8 PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	76.4	84.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	41	63.2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	47.7	43	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.2	27.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.2	42.7	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, R_L = 60 Ω TXD with 5V, 500kHz 50% duty square wave			200	mW
P_{D1}	Maximum power dissipation (side-1)	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, R_L = 60 Ω , TXD with 5V, 500kHz 50% duty square wave			25	mW
P_{D2}	Maximum power dissipation (side-2)	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, R_L = 60 Ω TXD with 5V, 500kHz 50% duty square wave			175	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS		UNIT
			DUB-8	DW-16	
IEC 60664-1					
CLR	External clearance(1)	Side 1 to side 2 distance through air	>6.1	>8	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	>6.8	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>13.5	>13.5	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	n/a	I-II	
		Rated mains voltage ≤ 848 V_{RMS}	n/a	I	
DIN V VDE V 0884-11:2017-01(2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	1200	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	395	848	V_{RMS}
		DC voltage	560	1200	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM} , t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	4000	4000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 x V_{IOSM} = 6.4 kV_{PK} (qualification)	4000	4000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} , t_m = 10 s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.3 × V_{IORM} , t_m = 10 s	≤ 5	≤ 5	
		Method b: At routine test (100% production) V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.5 x V_{IORM}, t_m = 1 s	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	1	1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 150°C	> 10^{11}	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	> 10^9	
	Pollution degree		2	2	
	Climatic category		40/125/21	40/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} , t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100% production)	2500	4243	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) ISO1044 is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 62368-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1 and EN 62368-1
Basic Insulation Transient Overvoltage, 4000 V_{PK} Surge Voltage, 4000 V_{PK} Maximum Working Voltage, 1200 V_{PK} (ISO1050DW) and 560 V_{PK} (ISO1050DUB)	ISO1050DW: 5000 V_{RMS} Reinforced Insulation Working voltage of 380 V_{RMS} per IEC 60950-1 2nd Ed.+A1+A2 and IEC 62368-1:2014 Working voltage of 300 V_{RMS} per IEC 61010-1 3rd Ed. ISO1050DUB: 2500 VRMS Basic Insulation Working voltage of 700 V_{RMS} per IEC 60950-1 2nd Ed.+A1+A2 Working voltage of 600 V_{RMS} per IEC 61010-1 3rd Ed. and IEC 62368-1:2014	ISO1050DUB: 2500 V_{RMS} Single Protection ISO1050DW: 4243 V_{RMS} Single Protection	ISO1050DW: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	ISO1050DW: 5000 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 5000 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage ISO1050DUB: 2500 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 2500 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage
Certificate number: 40047657	Client ID number: 77311	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109541

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DUB-8 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 84.3°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C. see Figure 6-1			269	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 84.3°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C. Figure 6-1			411	mA
T_S	Maximum safety temperature				150	°C
DW-16 Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 76.4°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C. Figure 6-2			297	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 76.4°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C. Figure 6-2			454	mA
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics - DC Specification

Typical specifications are at V_{CC1} = 3.3V, V_{CC2} = 5V, Min/Max are over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{CC1}	Supply current Side 1	V_I = 0 V or V_{CC1}, V_{CC1} = 3.3 V		1.8	3.6	mA
I_{CC1}	Supply current Side 1	V_I = 0 V or V_{CC1}, V_{CC1} = 5.0 V		2.3	3.6	mA
I_{CC2}	Supply current Side 2	V_I = 0 V, bus dominant, R_L = 60 Ω		52	73	mA
I_{CC2}	Supply current Side 2	V_I = V_{CC1}		8	12	mA
DRIVER ELECTRICAL CHARACTERISTICS						
$V_{O(DOM)}$	Bus output voltage(Dominant), CANH	See Figure 7-1 and Figure 7-2, V_I = 0 V, R_L = 60 Ω	2.9	3.5	4.5	V
	Bus output voltage(Dominant), CANL	See Figure 7-1 and Figure 7-2, V_I = 0 V, R_L = 60 Ω	0.8	1.2	1.78	V
$V_{O(REC)}$	Bus output voltage(recessive), CANH and CANL	See Figure 7-1 and Figure 7-2, V_I = 2 V, R_L = 60 Ω	2.0	2.3	3.0	V
$V_{OD(DOM)}$	Differential output voltage(dominant)	See Figure 7-1 and Figure 7-2, V_I = 0 V, R_L = 60 Ω	1.5		3.0	V
		See Figure 7-1 and Figure 7-2, V_I = 0 V, R_L = 45 Ω, VCC > 4.8 V	1.4		3.0	V
$V_{OD(REC)}$	Differential output voltage(recessive)	See Figure 7-1 and Figure 7-2, V_I = 3 V, R_L = 60 Ω	-120.0		12.0	mV
		V_I = 3 V, No Load	-500.0		50.0	mV
$V_{OC(DOM)}$	Common-mode output voltage (Dominant)	See Figure 7-8	2	2.3	3.0	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 7-8		0.3		V
I_{IH}	High level input leakage current	V_I = 2 V			5	uA
I_{IL}	Low level input leakage current	V_I = 0.8 V	-5			uA
$I_{O(off)}$	Power-off TXD leakage current	V_{CC1}, V_{CC2} at 0 V, TXD = 5 V			10	uA
$I_{OS(ss)}$	Short circuit current steady state output current, dominant	See Figure 7-11, CANH = –12 V, CANL Open	-105	-72		mA
		See Figure 7-11, VCANH = 12 V, CANL Open		0.36	6.2	mA
		See Figure 7-11, VCANL =–12 V, CANH Open	-1	-0.5		mA
		See Figure 7-11, VCANL = 12 V, CANH Open		71	105	mA
CMTI	Common-mode transient immunity	See Figure 7-13, V_I = V_{CC} or 0 V	25	50		kV/us
RECEIVER ELECTRICAL CHARACTERISTICS						
V_{IT+}	Positive-going bus input threshold voltage	See Table 1		750	900.0	mV
V_{IT-}	Negative-going bus input threshold voltage		500.0	650		mV
V_{HYS}	Hysteresis voltage for differential input threshold			150		mV
V_{OH}	High level output voltage with Vcc = 5 V	I_O = -4 mA, See Figure 7-6	Vcc - 0.8	4.6		V
		I_O = -20 uA, See Figure 7-6	Vcc - 0.1	5		V
V_{OH}	High level output voltage with Vcc1 = 3.3 V	I_O = 4 mA, See Figure 7-6	Vcc - 0.8	3.1		V
		I_O = 20 uA, See Figure 7-6	Vcc - 0.1	3.3		V
V_{OL}	Low level output voltage	I_O = 4 mA, See Figure 7-6		0.2	0.4	V
		I_O = 20 uA, See Figure 7-6		0	0.1	V

Typical specifications are at V_{CC1} = 3.3V, V_{CC2} = 5V, Min/Max are over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance to ground (CANH or CANL)	TXD = 3 V, V_I = 0.4 sin (4e6pi*t) + 2.5 V		12		pF
C_{ID}	Differential input capacitance	TXD = 3 V, V_I = 0.4 sin (4e6pi*t)		8		pF
R_{ID}	Differential input resistance	TXD = 3 V	40		90	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD = 3 V	20		45	kΩ
$R_{IN(M)}$	Input resistance matching: (1 - $R_{IN(CANH)}$/ $R_{IN(CANL)}$) x 100%	V_{CANH} = V_{CANL}	-3		3	%
CMTI	Common-mode transient immunity	See Figure 7-13, V_I = V_{CC} or 0 V	25	50		kV/us

6.10 Switching Characteristics

Typical specifications are at V_{CC1} = 3.3V, V_{CC2} = 5V, Min/Max are over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver RXD, recessive to dominant	See Figure 7-9	100	150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver RXD, dominant to recessive	See Figure 7-9	112	150	210	ns
DRIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, recessive-to-dominant output	See Figure 7-4		74	110	ns
t_{PHL}	Propagation delay time, dominant-to-recessive output			82	110	
t_R	Differential output signal rise time			20	50	
t_F	Differential output signal fall time			52	63	
t_{TXD_DTO}	Dominant time out	C_L = 100 pF, See Figure 7-10	1.2		4	ms
RECEIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high-level output	TXD at 3 V, See Figure 7-6	66	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		51	80	105	ns
t_R	Output signal rise time(RXD)			3	6	ns
t_F	Output signal fall time(RXD)			3	6	ns
t_{fs}	Fail-Safe output delay time from bus-side power loss	VCC1 at 5 V, See Figure 7-12		6		us

6.11 Insulation Characteristics Curves

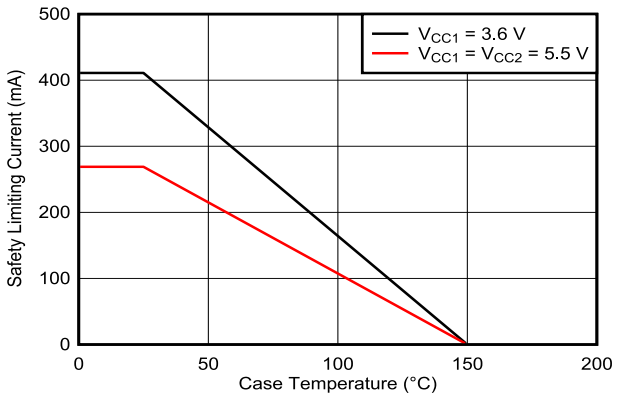


Figure 6-1. DUB-8 Thermal Derating Curve per VDE

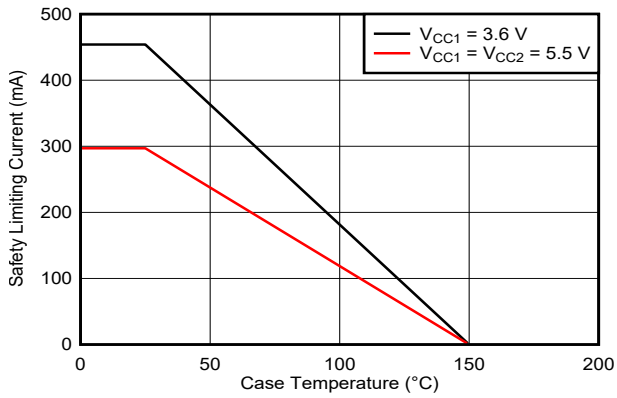


Figure 6-2. DW-16 Thermal Derating Curve per VDE

6.12 Typical Characteristics

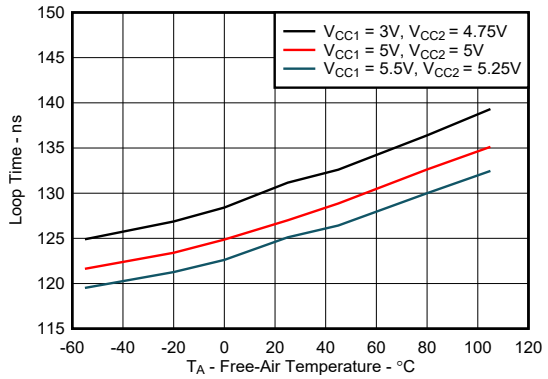


Figure 6-3. Recessive-to-Dominant Loop Time vs Free-Air Temperature (Across Vcc)

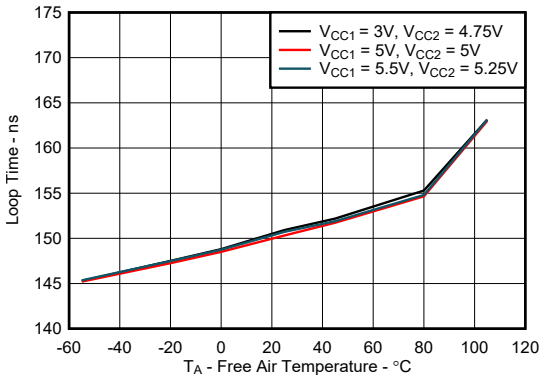


Figure 6-4. Dominant-to-Recessive Loop Time vs Free-Air Temperature (Across Vcc)

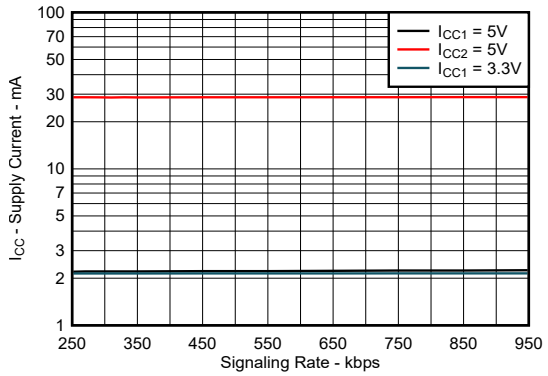


Figure 6-5. Supply Current (RMS) vs Signaling Rate (kbps)

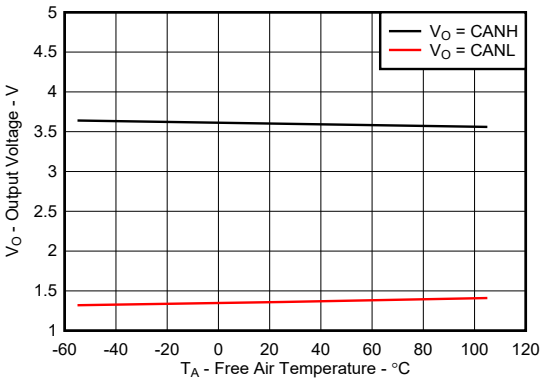


Figure 6-6. Driver Output Voltage vs Free-Air Temperature

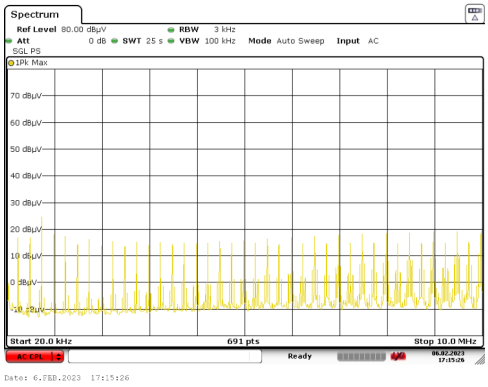


Figure 6-7. Emissions Spectrum to 10 MHz

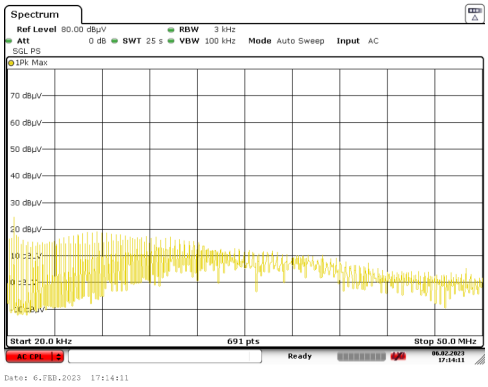


Figure 6-8. Emissions Spectrum to 50 MHz

7 Parameter Measurement Information

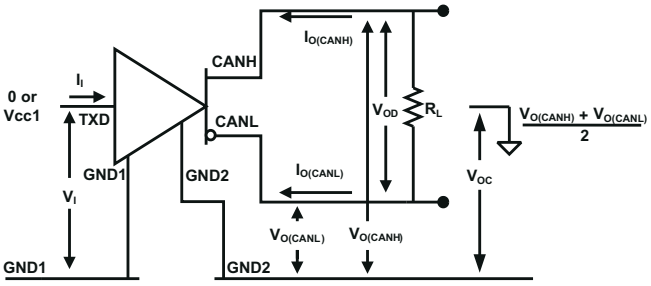


Figure 7-1. Driver Voltage, Current and Test Definitions

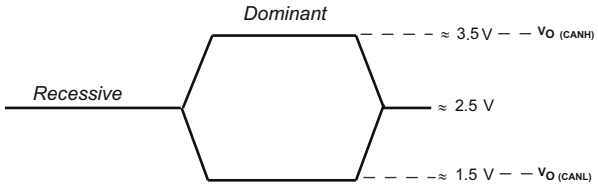


Figure 7-2. Bus Logic State Voltage Definitions

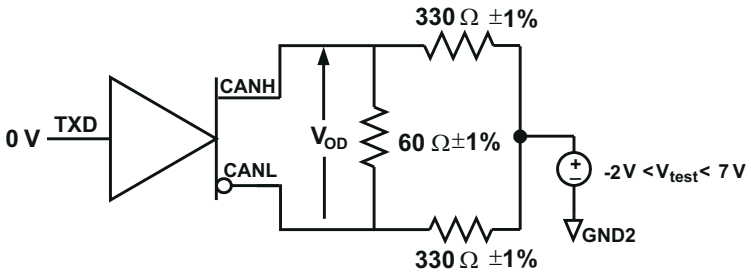
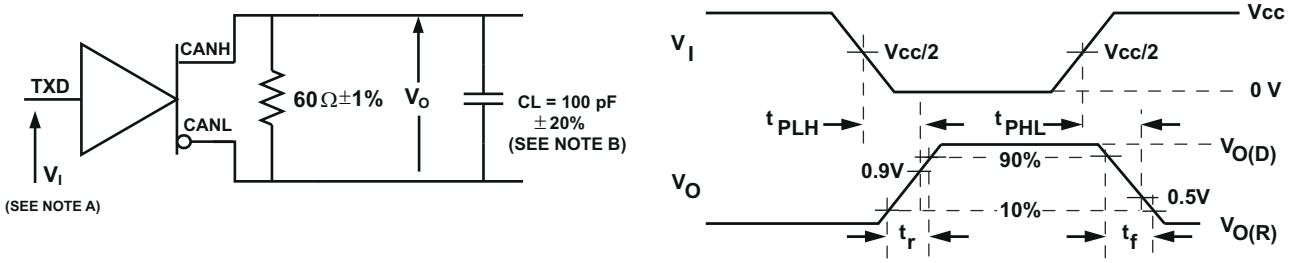


Figure 7-3. Driver V_{OD} With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7-4. Driver Test Circuit and Voltage Waveforms

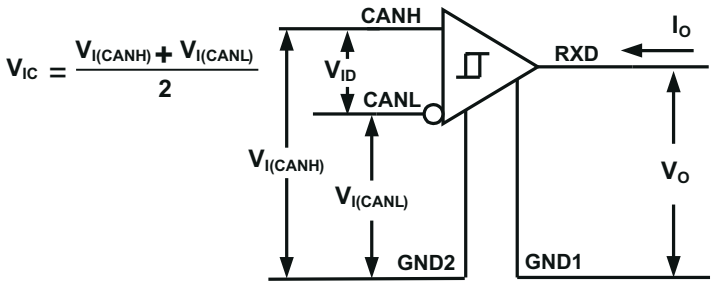
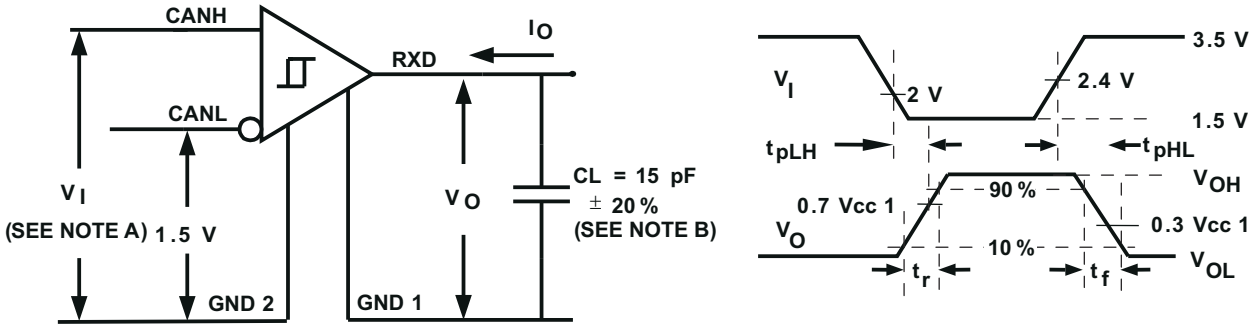


Figure 7-5. Receiver Voltage and Current Definitions



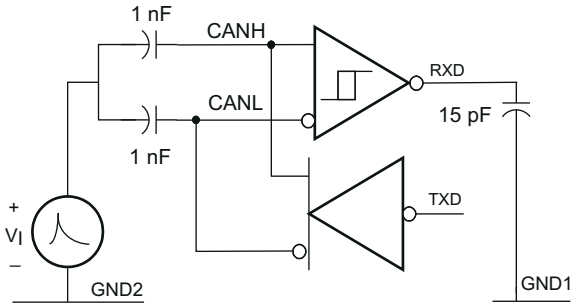
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7-6. Receiver Test Circuit and Voltage Waveforms

Table 7-1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	–6 V	H	
6 V	12 V	–6 V	H	
Open	Open	X	H	



The waveforms of the applied transients are in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b.

Figure 7-7. Transient Overvoltage Test Circuit

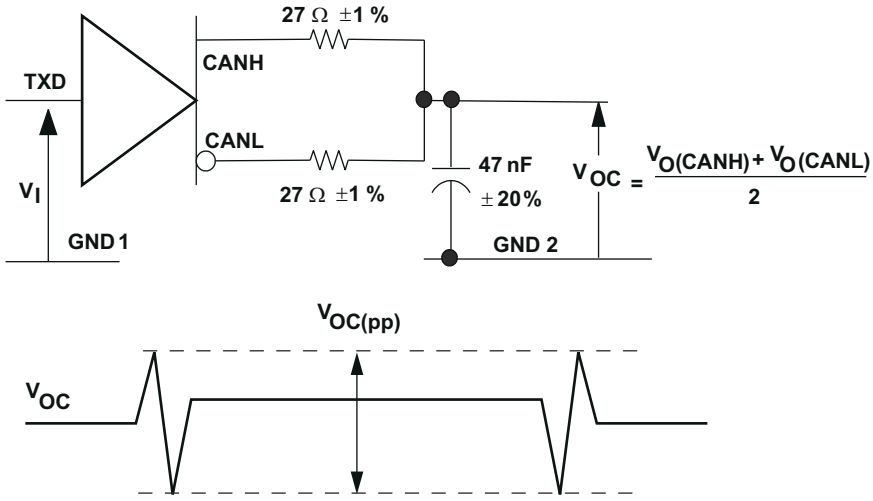


Figure 7-8. Peak-to-Peak Output Voltage Test Circuit and Waveform

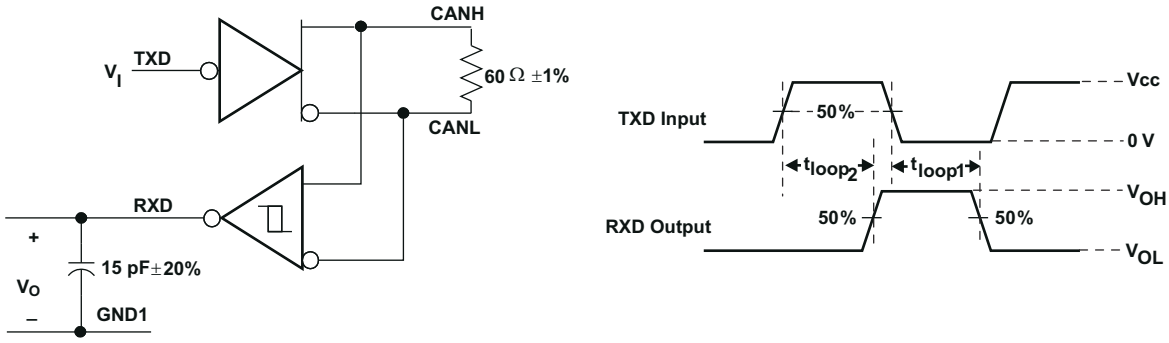
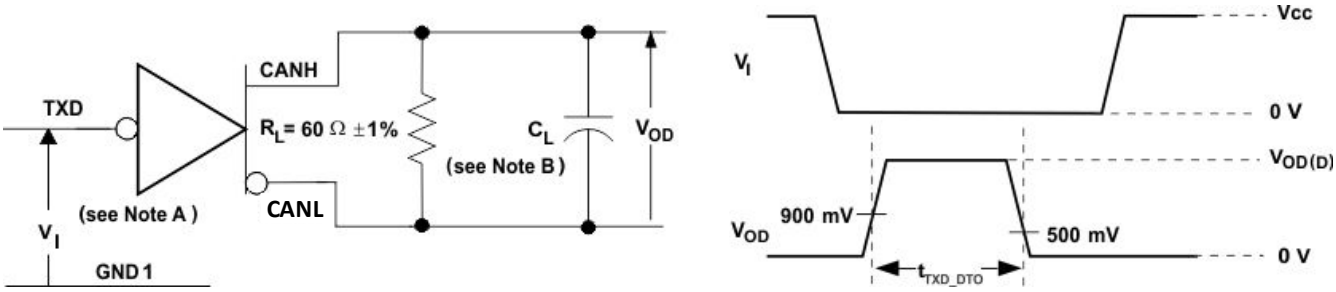


Figure 7-9. t_{LOOP} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7-10. Dominant Time-out Test Circuit and Voltage Waveforms

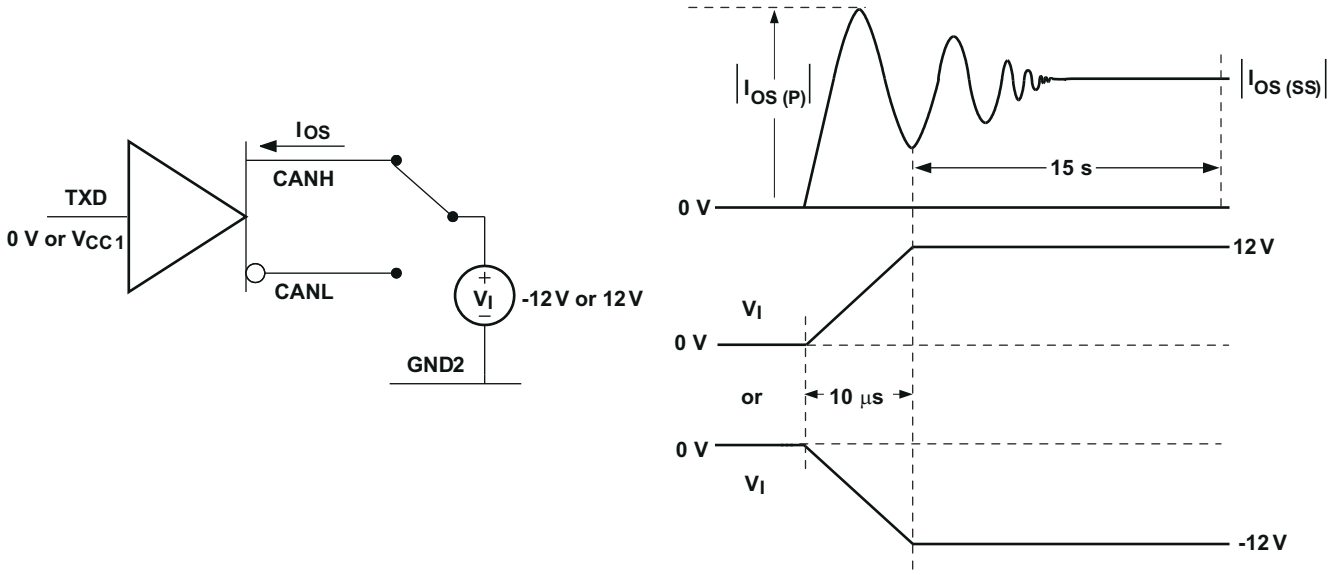


Figure 7-11. Driver Short-Circuit Current Test Circuit and Waveforms

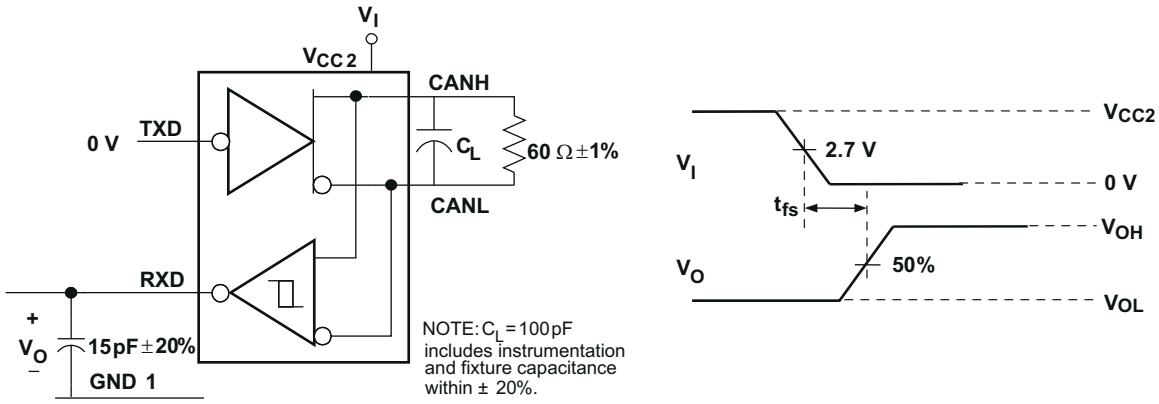


Figure 7-12. Fail-Safe Delay Time Test Circuit and Voltage Waveforms

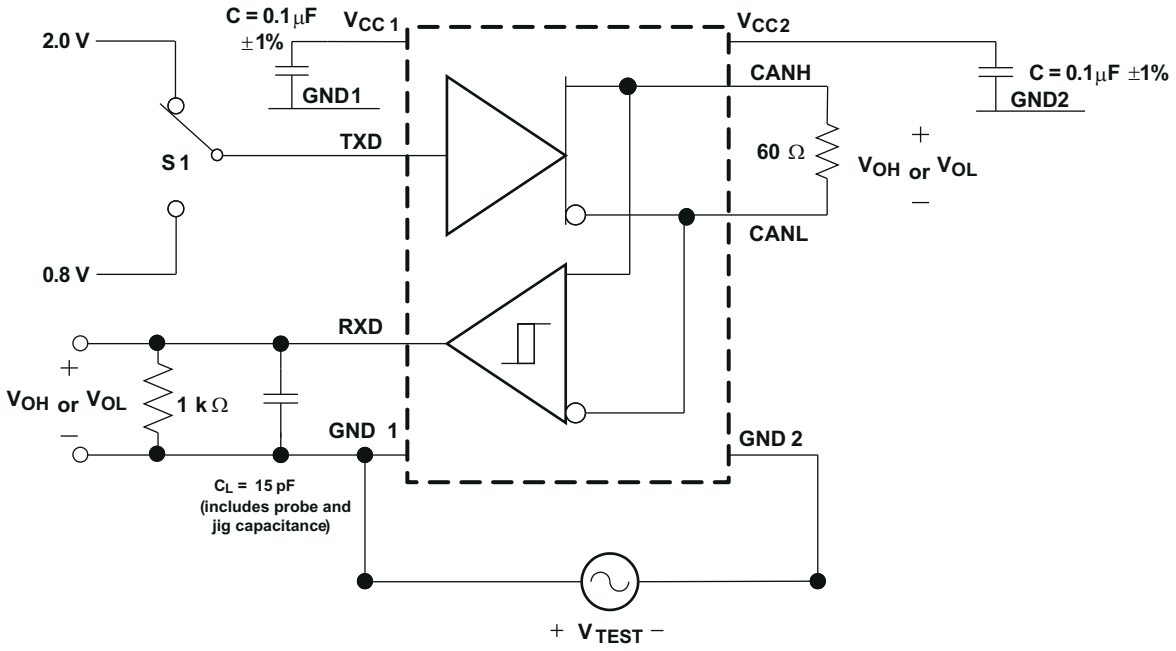


Figure 7-13. Common-Mode Transient Immunity Test Circuit

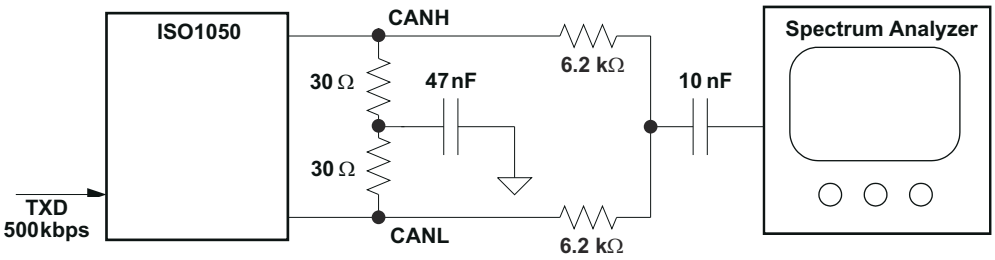


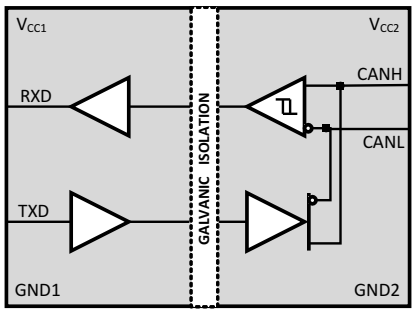
Figure 7-14. Electromagnetic Emissions Measurement Setup

8 Detailed Description

8.1 Overview

The ISO1050 is a digitally isolated CAN transceiver with a typical transient immunity of 50 kV/µs. The device can operate from 3.3-V supply on side 1 and 5-V supply on side 2. This is of particular advantage for applications operating in harsh industrial environments because the 3.3 V on side 1 enables the connection to low-volt microcontrollers for power preservation, whereas the 5 V on side 2 maintains a high signal-to-noise ratio of the bus signals.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 CAN Bus States

The CAN bus has two states during operation: *dominant* and *recessive*. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state is when the bus is biased to a common mode of V_{CC} / 2 through the high-resistance internal input resistors of the receiver, equivalent to a logic high. The host microprocessor of the CAN node will use the TXD pin to drive the bus and will receive data from the bus on the RXD pin. See Figure 8-1 and Figure 8-2.

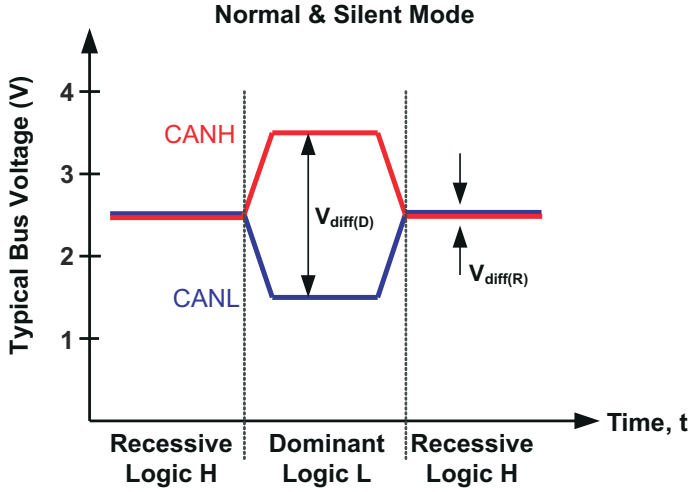


Figure 8-1. Bus States (Physical Bit Representation)

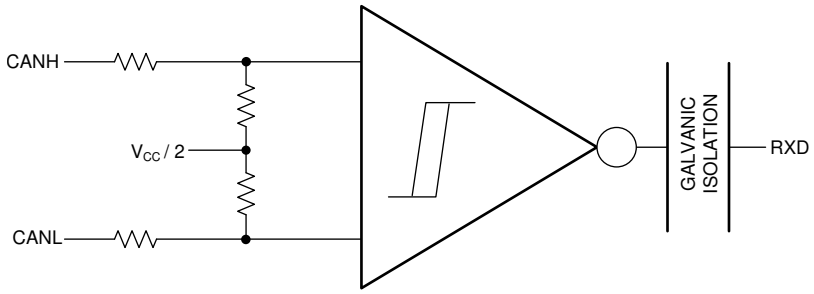


Figure 8-2. Simplified Recessive Common Mode Bias and Receiver

8.3.2 Digital Inputs and Outputs

TXD (Input) and RXD (Output):
V_{CC1} for the isolated digital input and output side of the device maybe supplied by a 3.3-V or 5-V supply and thus the digital inputs and outputs are 3.3-V and 5-V compatible.

Note

TXD is very weakly internally pulled up to V_{CC1}. An external pullup resistor should be used to make sure that TXD is biased to recessive (high) level to avoid issues on the bus if the microprocessor doesn't control the pin and TXD floats. TXD pullup strength and CAN bit timing require special consideration when the device is used with an open-drain TXD output on the CAN controller of the microprocessor. An adequate external pullup resistor must be used to ensure that the TXD output of the microprocessor maintains adequate bit timing input to the input on the transceiver.

8.3.3 Protection Features

8.3.3.1 TXD Dominant Time-Out (DTO)

TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. The TXD DTO circuit timer starts on a falling edge on TXD. The TXD DTO circuit disables the CAN bus driver if no rising edge is seen before the time-out period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD dominant time-out.

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

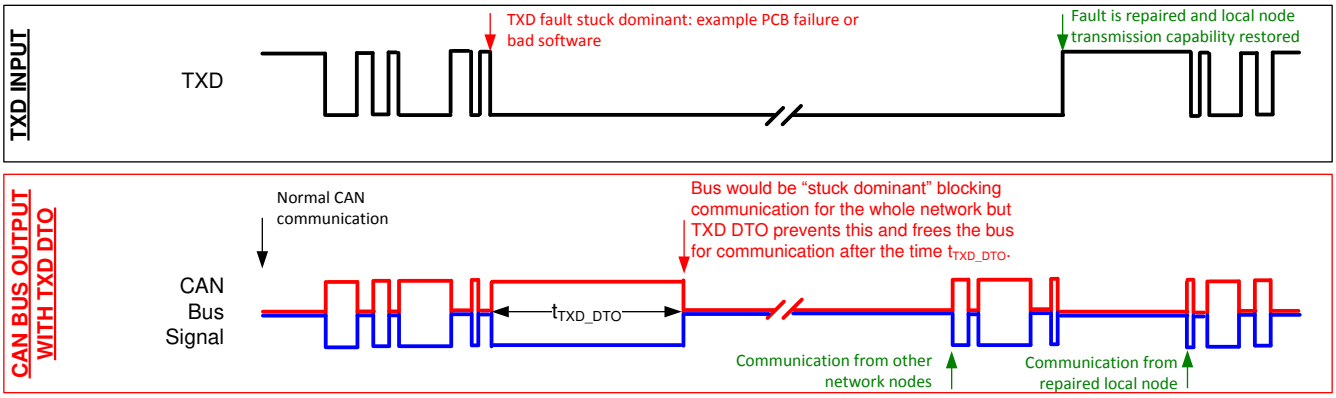


Figure 8-3. Example Timing Diagram for Devices With TXD DTO

8.3.3.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. If the fault condition is still present, the temperature may rise again and the device would enter thermal shut down again. Prolonged operation with thermal shutdown conditions may affect device reliability.

Note

During thermal shutdown the CAN bus drivers turn off; thus no transmission is possible from TXD to the bus. The CAN bus pins are biased to recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

8.3.3.3 Undervoltage Lockout and Fail-Safe

The supply pins have undervoltage detection that places the device in protected or fail-safe mode. This protects the bus during an undervoltage event on V_{CC1} or V_{CC2} supply pins. If the bus-side power supply V_{CC2} is lower than about 4 V, the power shutdown circuits in the ISO1050 will disable the transceiver to prevent false transmissions due to an unstable supply. If V_{CC1} is still active when this occurs, the receiver output (RXD) will go to a fail-safe HIGH (recessive) value in about 6 microseconds.

Table 8-1. Undervoltage Lockout and Fail-Safe

$V_{CC}1$	$V_{CC}2$	DEVICE STATE	BUS OUTPUT	RXD
GOOD	GOOD	Functional	Per Device State and TXD	Mirrors Bus
BAD	GOOD	Protected	Recessive	High Impedance (3-state)
GOOD	BAD	Protected	High Impedance	Recessive (Fail-Safe High)

Note

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300 µs

8.3.3.4 Floating Pins

Pullups and pulldowns should be used on critical pins to place the device into known states if the pins float. The TXD pin should be pulled up through a resistor to V_{CC1} to force a recessive input level if the microprocessor output to the pin floats.

8.3.3.5 CAN Bus Short-Circuit Current Limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include driver current limiting (dominant and recessive). The device has TXD dominant state time out to prevent permanent higher short-circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states with the data and control fields bits, thus the short-circuit current may be viewed either as the instantaneous current during each bus state, or as a DC average current. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short-circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit-stuffing
- Interframe space
- TXD dominant time-out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

Note

The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated with the following formula:

$I_{OS(AVG)}$ = %Transmit × [(%REC_Bits × $I_{OS(SS)\_REC}$) + (%DOM_Bits × $I_{OS(SS)\_DOM}$)] + [%Receive × $I_{OS(SS)\_REC}$]

Where

- $I_{OS(AVG)}$ is the average short-circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current.
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current.

Note

Consider the short-circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

8.4 Device Functional Modes

Table 8-2. Driver Function Table

INPUT	OUTPUTS		DRIVEN BUS STATE
TXD(1)	CANH(1)	CANL(1)	
L	H	L	Dominant
H	Z	Z	Recessive

(1) H = high level, L = low level, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 8-1 and Figure 8-2 for bus state and common mode bias information.

Table 8-3. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD PIN(1)
Normal or Silent	$V_{ID} \geq 0.9$ V	Dominant	L
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.

Table 8-4. Function Table

DRIVER				RECEIVER		
INPUTS	OUTPUTS		BUS STATE	DIFFERENTIAL INPUTS V_{ID} = CANH–CANL	OUTPUT RXD	BUS STATE
TXD	CANH	CANL				
L(1)	H	L	DOMINANT	$V_{ID} \geq 0.9$ V	L	DOMINANT
H	Z	Z	RECESSIVE	0.5 V < V_{ID} < 0.9 V	?	?
Open	Z	Z	RECESSIVE	$V_{ID} \leq 0.5$ V	H	RECESSIVE
X	Z	Z	RECESSIVE	Open	H	RECESSIVE

(1) Logic low pulses to prevent dominant time-out.

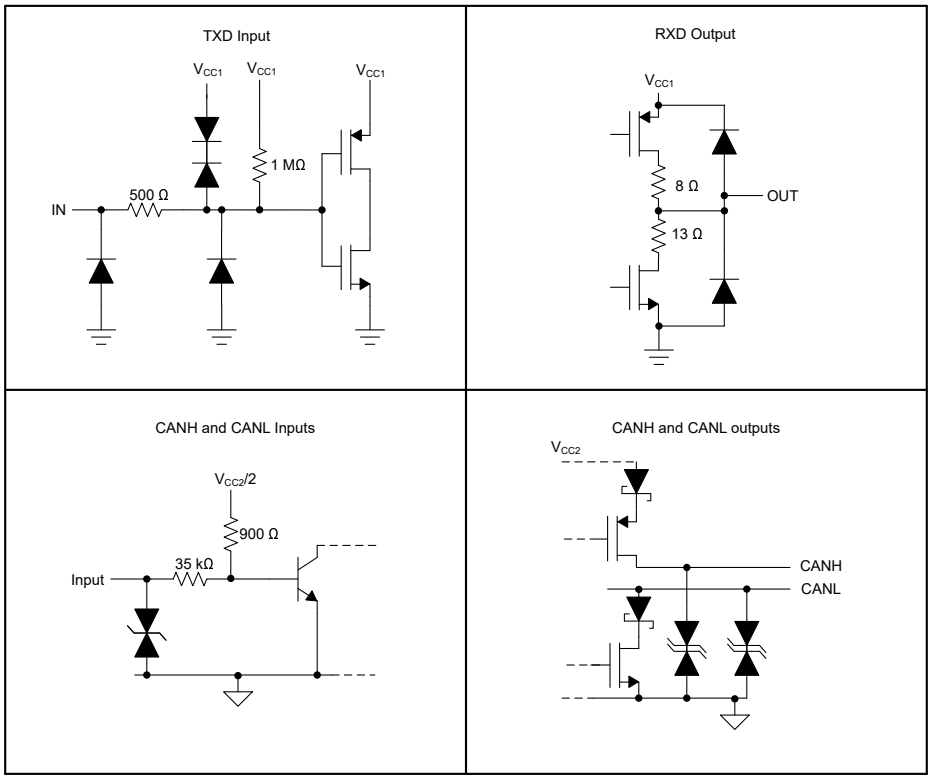


Figure 8-4. Equivalent I/O Schematics

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

ISO1050 can be used with other components from TI such as a microcontroller, a transformer driver, and a linear voltage regulator to form a fully isolated CAN interface.

9.2 Typical Application

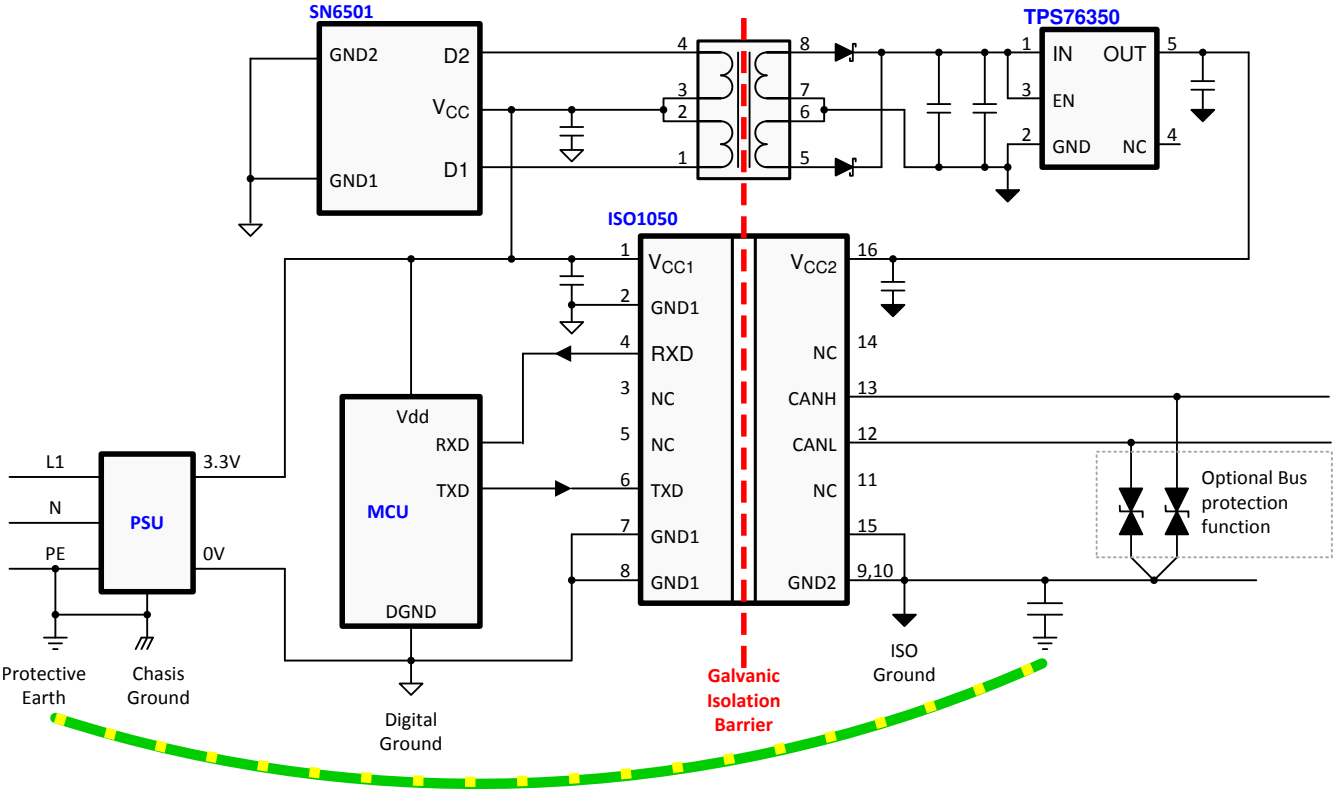


Figure 9-1. Application Circuit

9.2.1 Design Requirements

Unlike optocoupler-based solution, which needs several external components to improve performance, provide bias, or limit current, ISO1050 only needs two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

9.2.2.1 Bus Loading, Length and Number of Nodes

The ISO11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the ISO1050.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

A CAN network design is a series of tradeoffs, but these devices operate over wide –12-V to 12-V common-mode range. In ISO11898-2 the driver differential output is specified with a 60-Ω load (the two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The ISO1050 is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output of 1.4 V with a 45-Ω load. The differential input resistance of the ISO1050 is a minimum of 30 kΩ. If 167 ISO1050 transceivers are in parallel on a bus, this is equivalent to a 180-Ω differential load. That transceiver load of 180 Ω in parallel with the 60 Ω gives a total 45 Ω. Therefore, the ISO1050 theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2-V minimum differential input at each node. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CAN open network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design.

9.2.2.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

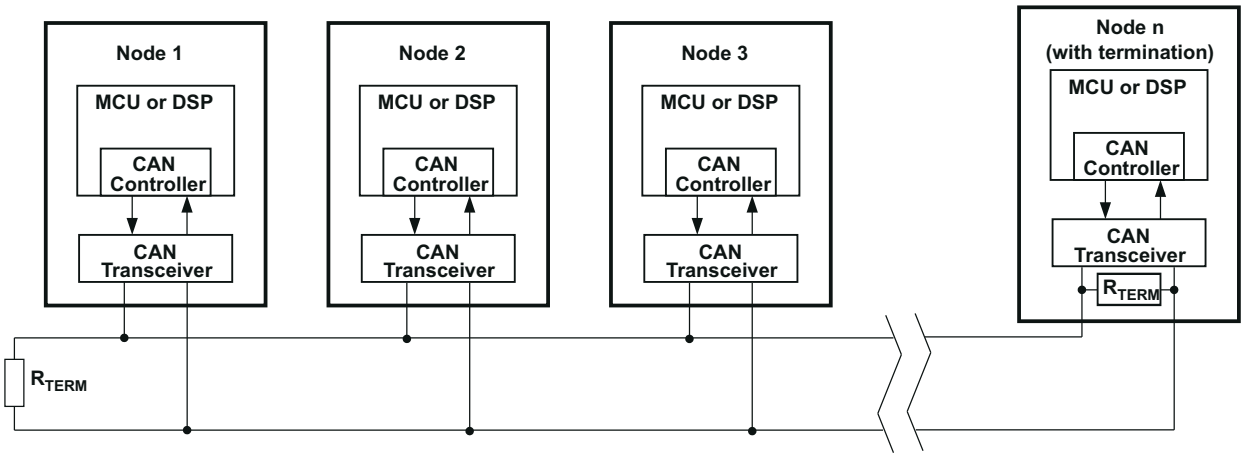


Figure 9-2. Typical CAN Bus

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 9-3). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

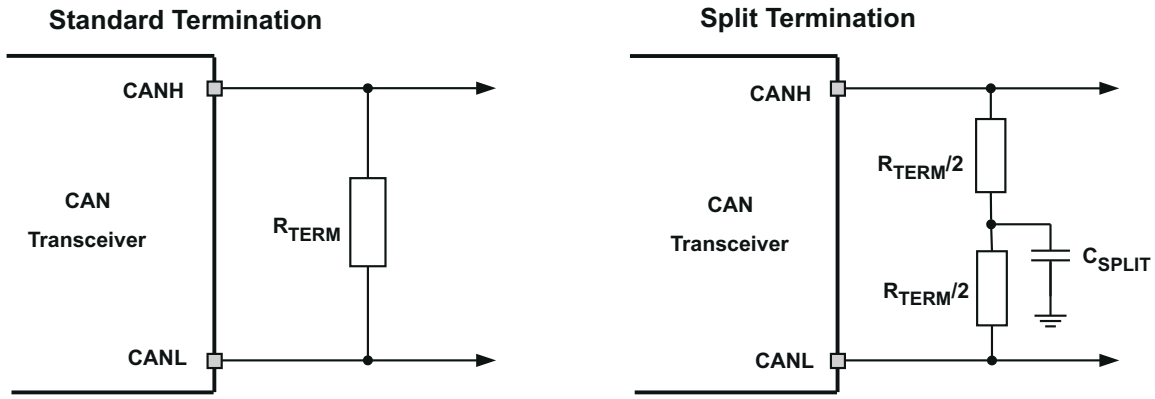


Figure 9-3. CAN Bus Termination Concepts

9.2.3 Application Curve

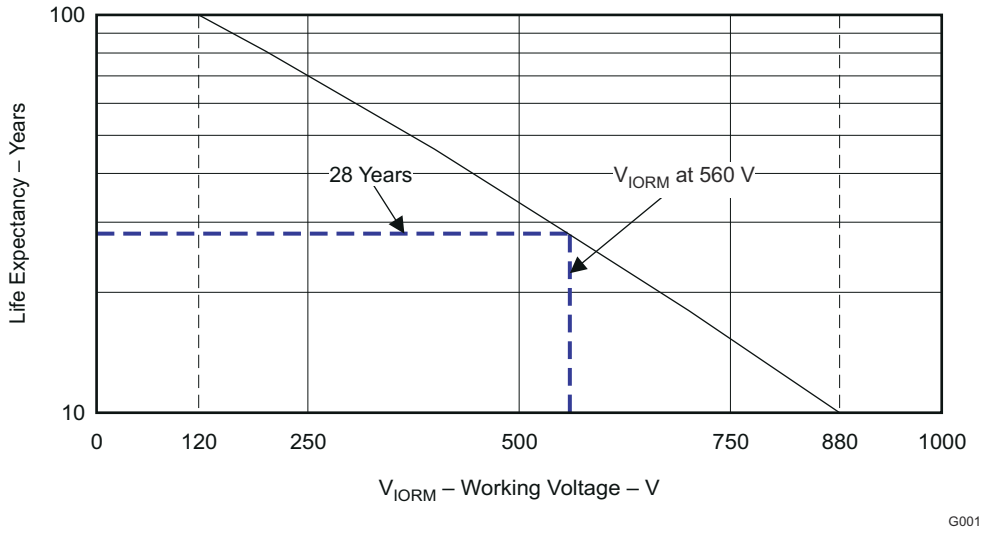


Figure 9-4. Life Expectancy vs Working Voltage (ISO1050DUB)

10 Power Supply Recommendations

10.1 General Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side using Texas Instruments' SN6505 and SN6501 based power supply solution. For such applications, detailed power supply design and transformer selection recommendations are available in SN6505 and SN6501 data sheets (SLLSEP9, SLLSEA0).

10.2 Power Supply Discharging

To ensure normal re-initialization time after a power down, the power supply for the ISO1050 needs to discharge below 0.3 V, and as closely to 0 V as possible, to ensure that a communication delay does not occur. Figure 10-1 illustrates various scenarios of power-supply ramp-down and its effect on the communication delay.

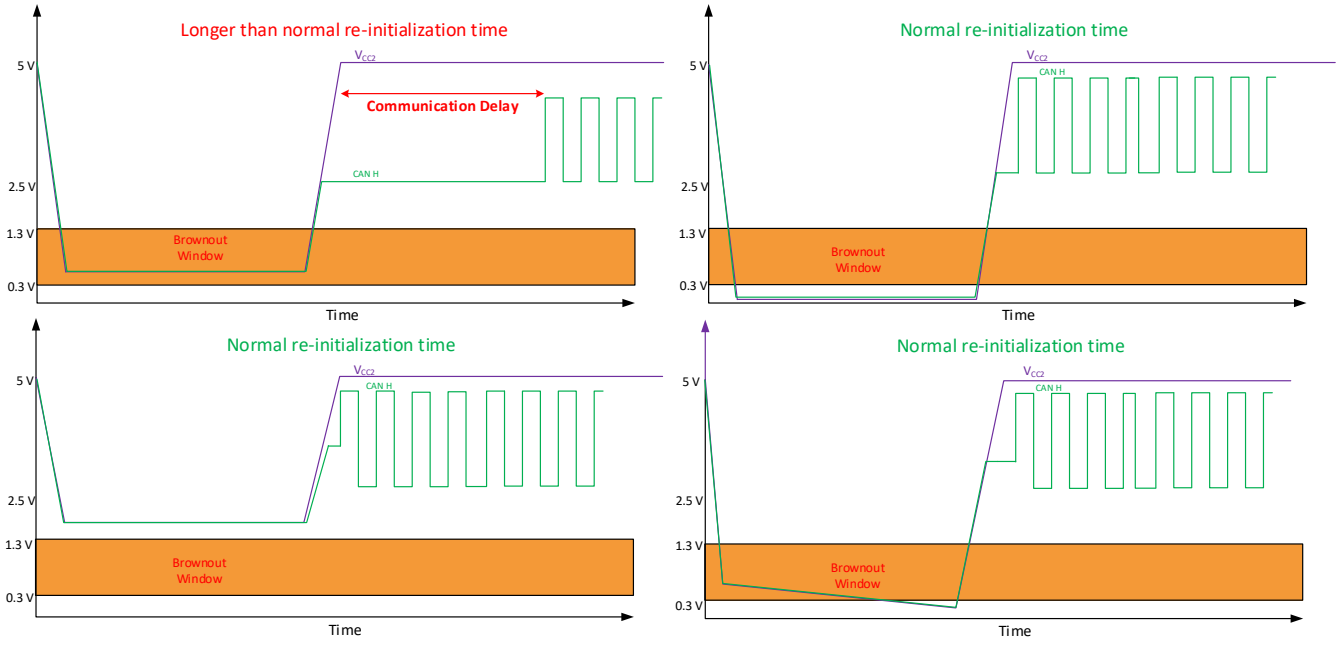


Figure 10-1. Power Supply Ramp-Down and Communication Delay Behavior

The brownout window, 0.3 V to 1.3 V (typical), represents the range of voltage in which a longer than normal re-initialization time may occur if V_{CC2} powers up from this voltage. The ISO1042, an upgraded device with higher isolation rating, CAN FD speeds of 5 Mbps, higher bus fault-protection voltage, stronger EMC performance, and smaller package options does not exhibit this behavior. For all new isolated CAN designs, it is recommended to use the ISO1042. If the ISO1050 must be used, ensure that V_{CC2} discharges to 0 V so that a longer than normal re-initialization time does not exist. If the power supplies cannot be configured in such a way that V_{CC2} discharge below 0.3 V on their own, implement a bleed resistor between V_{CC2} and GND2. The bleed resistor value should be selected such that it ensures V_{CC2} goes below the brownout window fast enough for any power interruption or power down sequence the system may permit. The lower the resistance, the faster V_{CC2} will discharge to 0V with the tradeoff of consuming power. For many systems, a bleed resistor value of 2 KΩ is sufficient.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

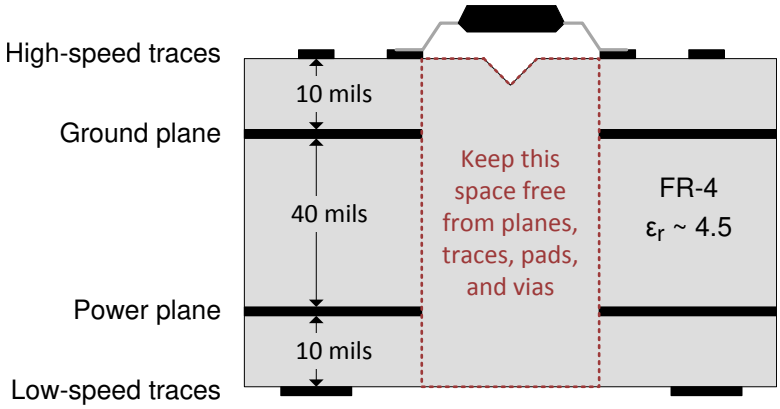


Figure 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- Texas Instruments, *High-Voltage Lifetime of the ISO72x Family of Digital Isolators*application report
- Texas Instruments, *SN6505x Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Isntruments, *Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *Digital Isolator Design Guide* application report
- Texas Instruments, *Isolation Glossary* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

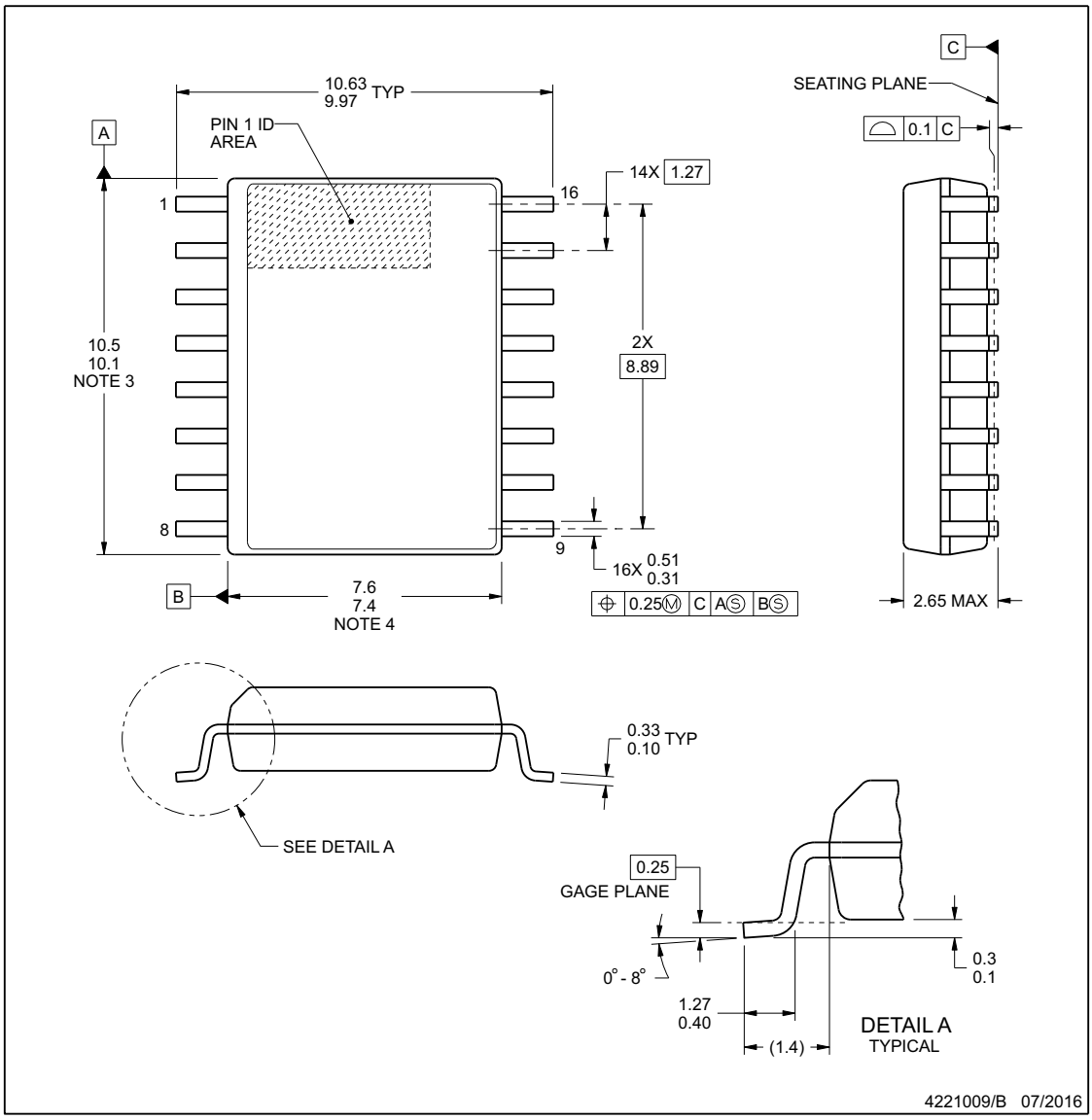
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

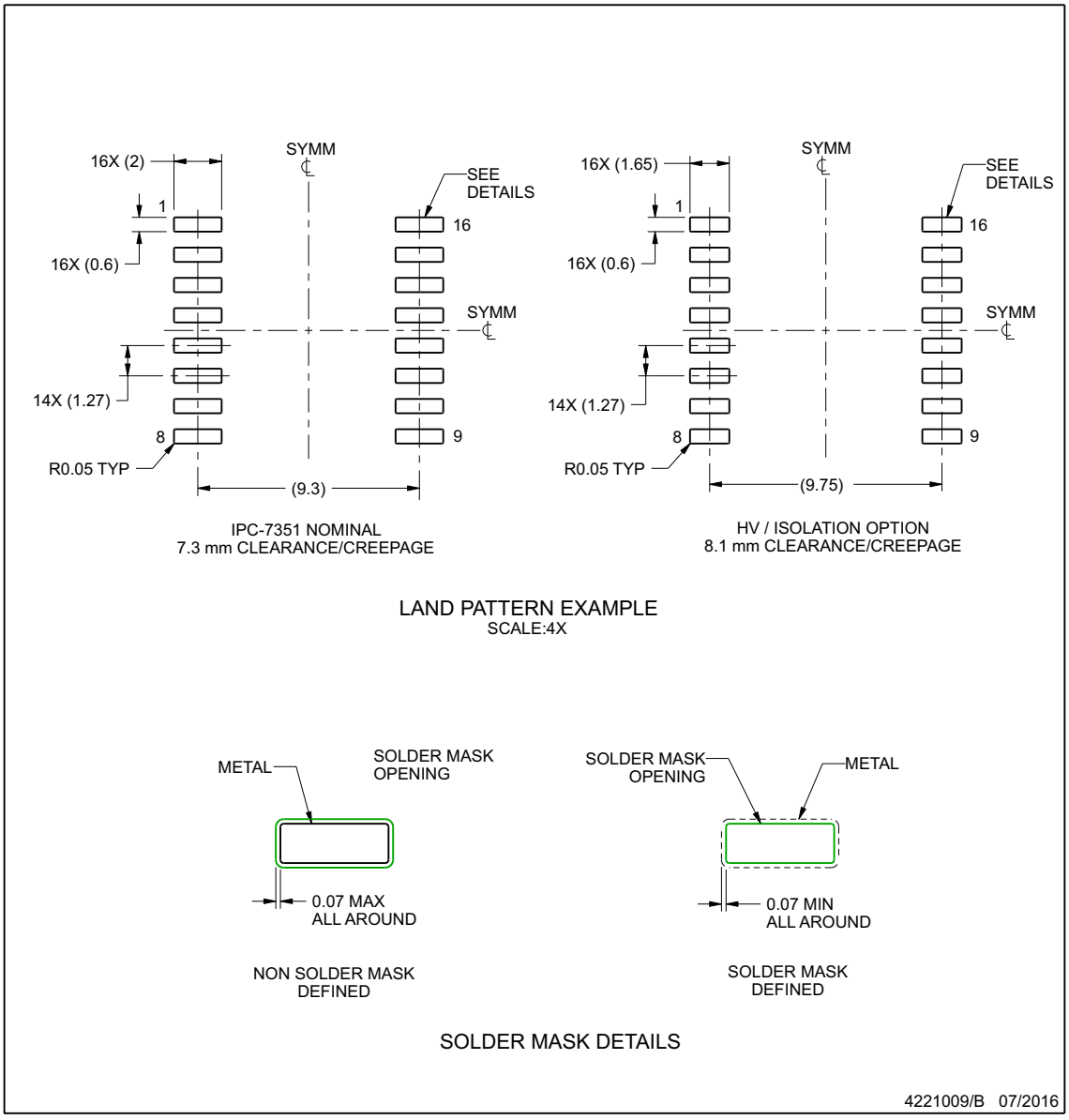
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

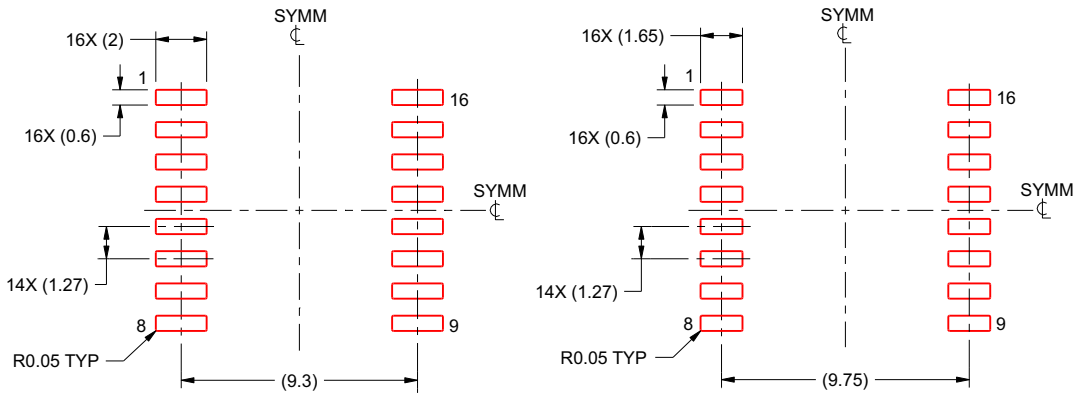
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1050DUB	OBSOLETE	SOP	DUB	8		TBD	Call TI	Call TI	-55 to 105	ISO1050	
ISO1050DUBR	ACTIVE	SOP	DUB	8	350	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-55 to 105	ISO1050	Samples
ISO1050DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-55 to 105	ISO1050	
ISO1050DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 105	ISO1050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

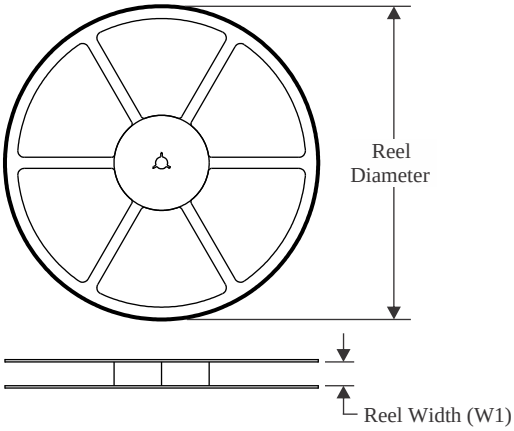
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

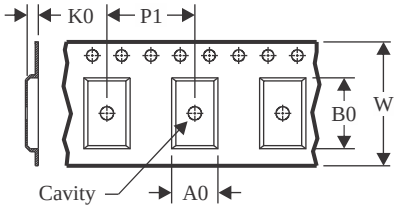
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

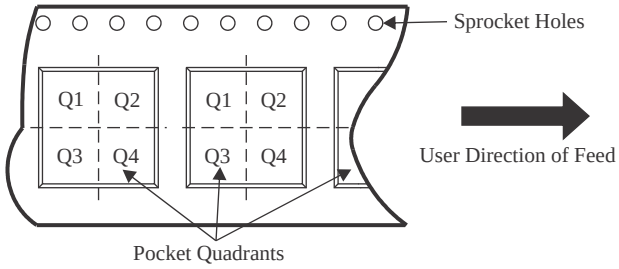


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

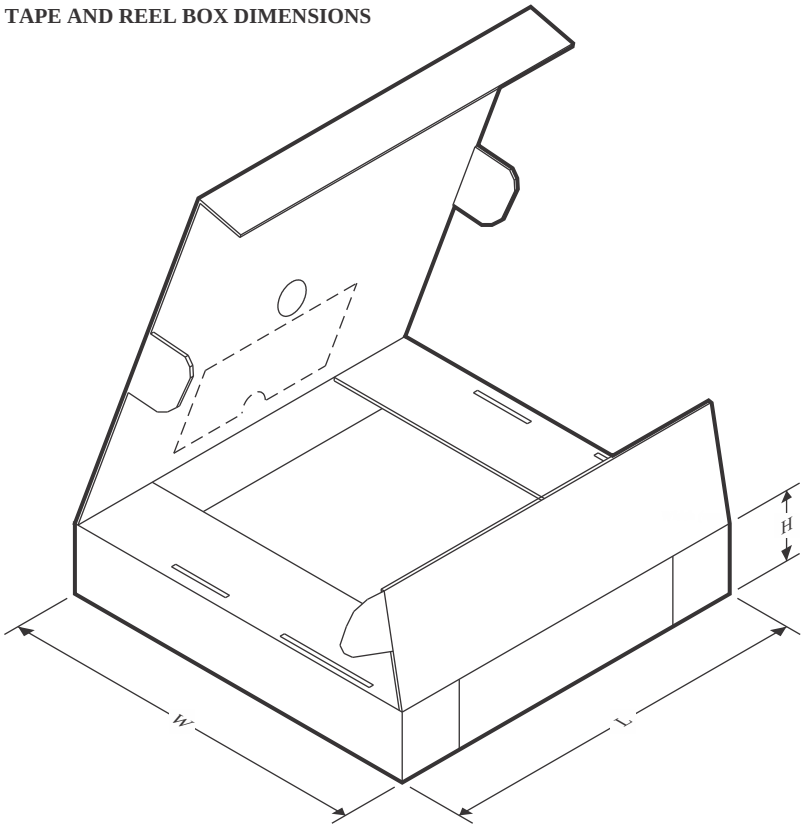
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1050DUBR	SOP	DUB	8	350	330.0	24.4	13.1	9.75	6.0	16.0	24.0	Q1
ISO1050DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

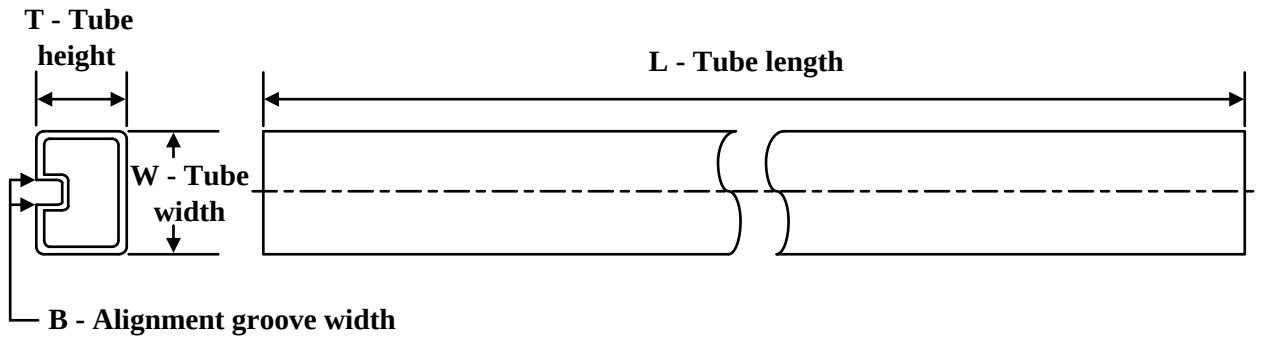
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1050DUBR	SOP	DUB	8	350	367.0	367.0	45.0
ISO1050DWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



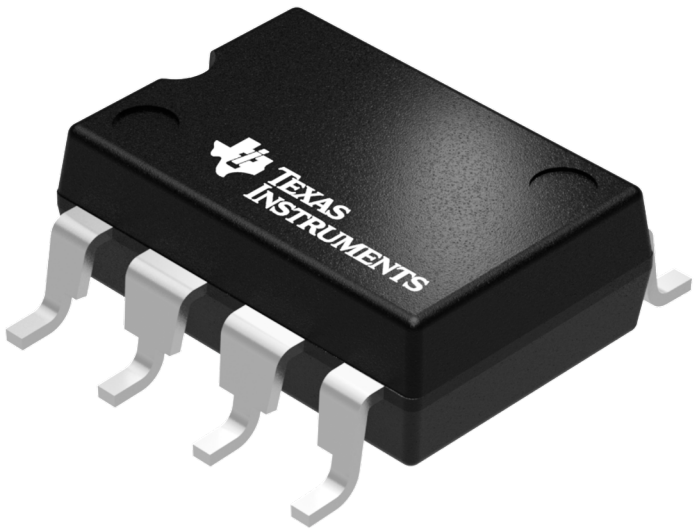
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO1050DUB	DUB	SOP	8	50	532.13	13	7300	6.6
ISO1050DUB	DUB	SOP	8	50	532.13	13.51	7.36	6.91
ISO1050DW	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

DUB 8 SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

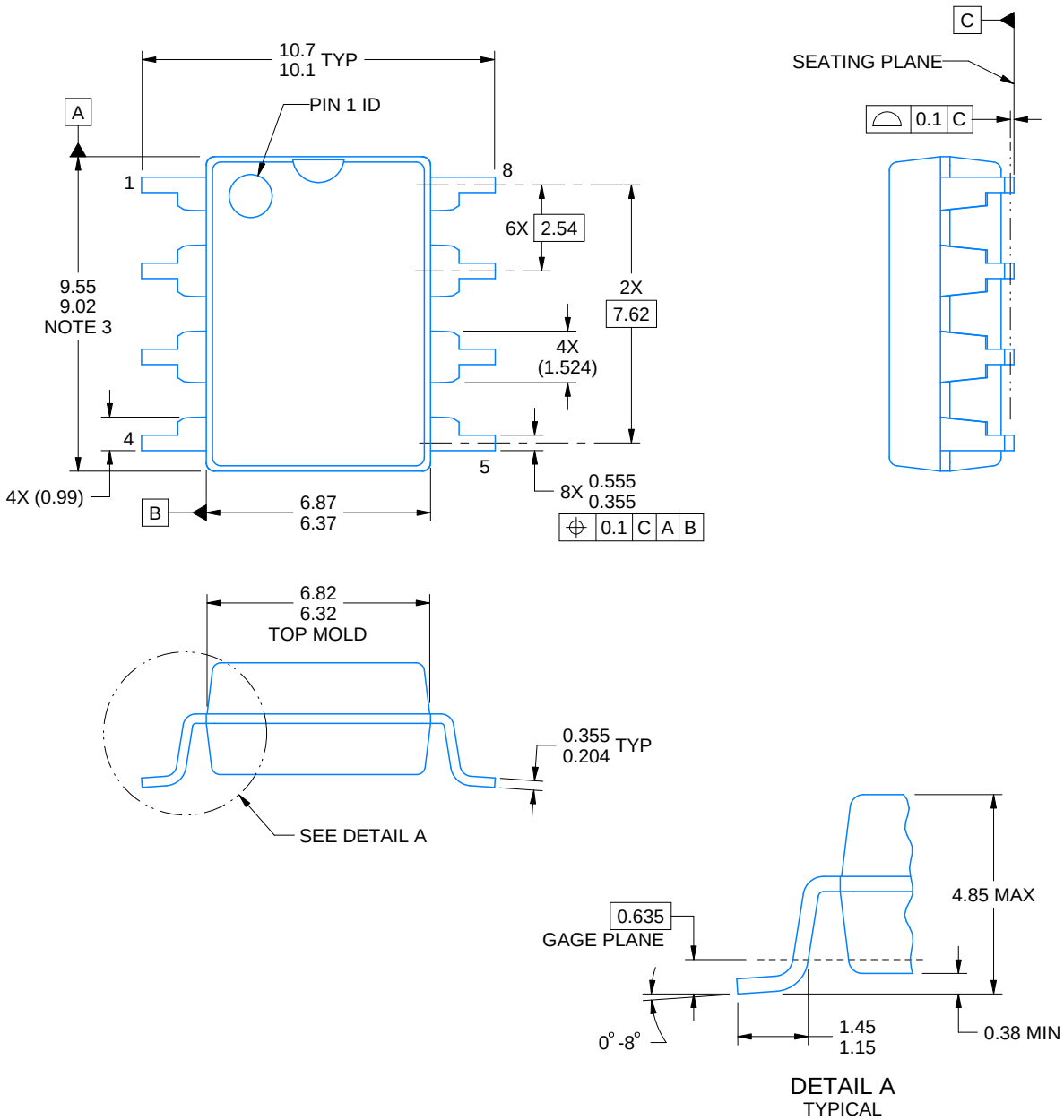
4207614/E

PACKAGE OUTLINE

DUB0008A

SOP - 4.85 mm max height

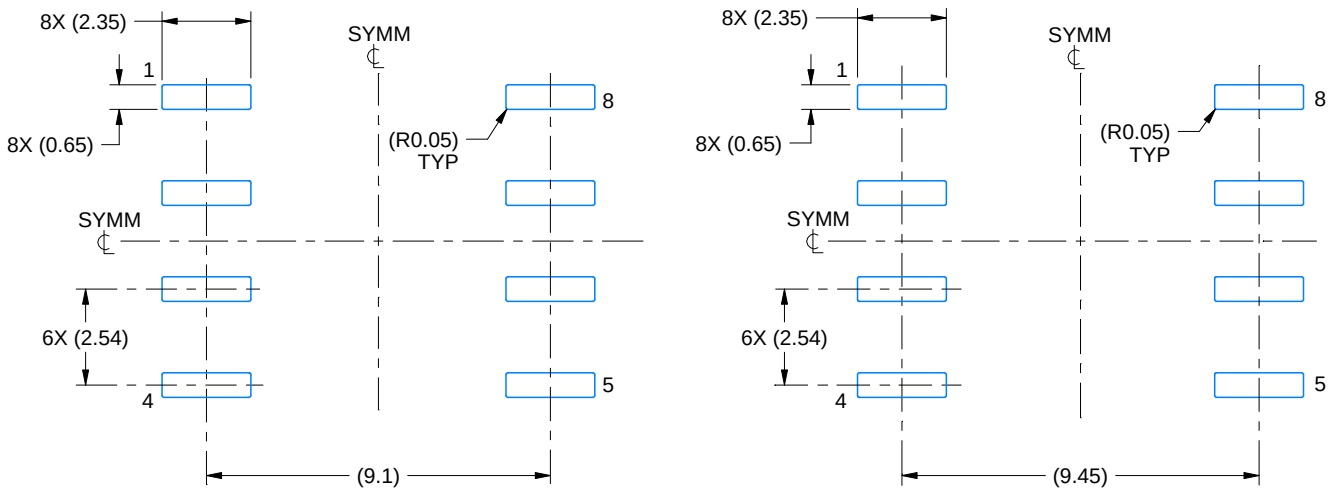
SMALL OUTLINE PACKAGE



4222355/G 04/2019

NOTES:

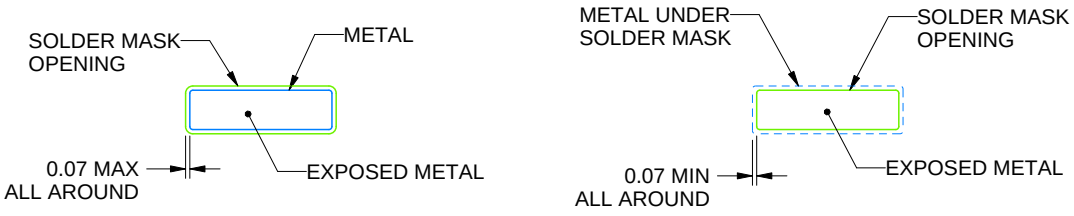
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.254 mm per side.



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE:5X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4222355/G 04/2019

NOTES: (continued)

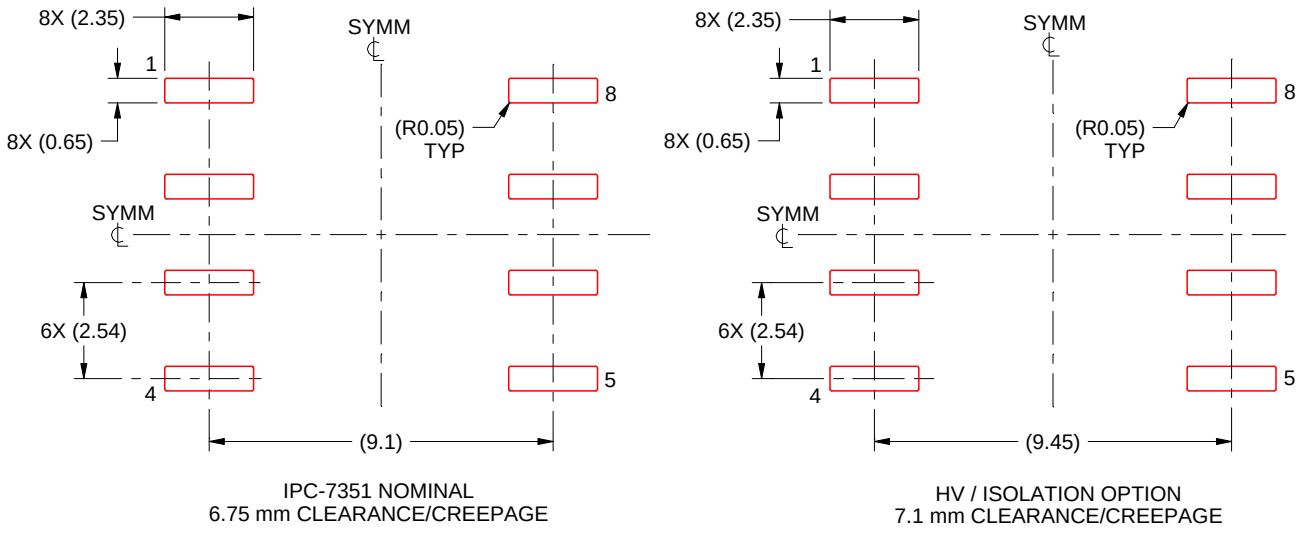
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DUB0008A

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:5X

4222355/G 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

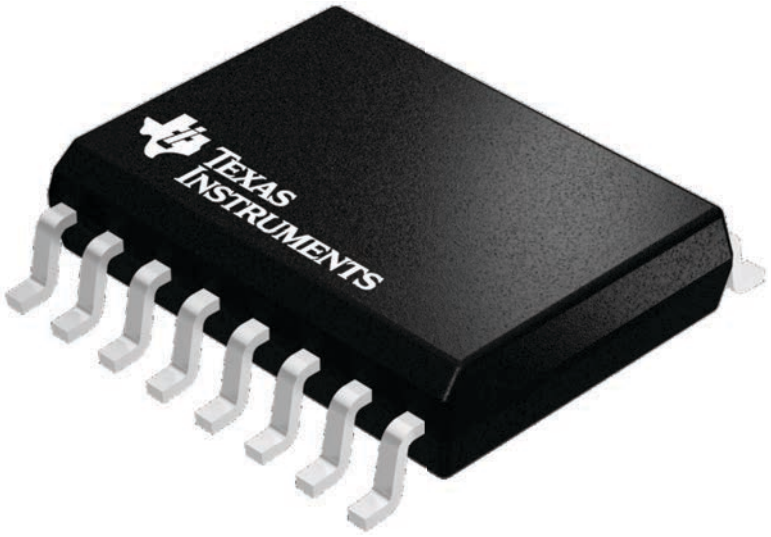
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

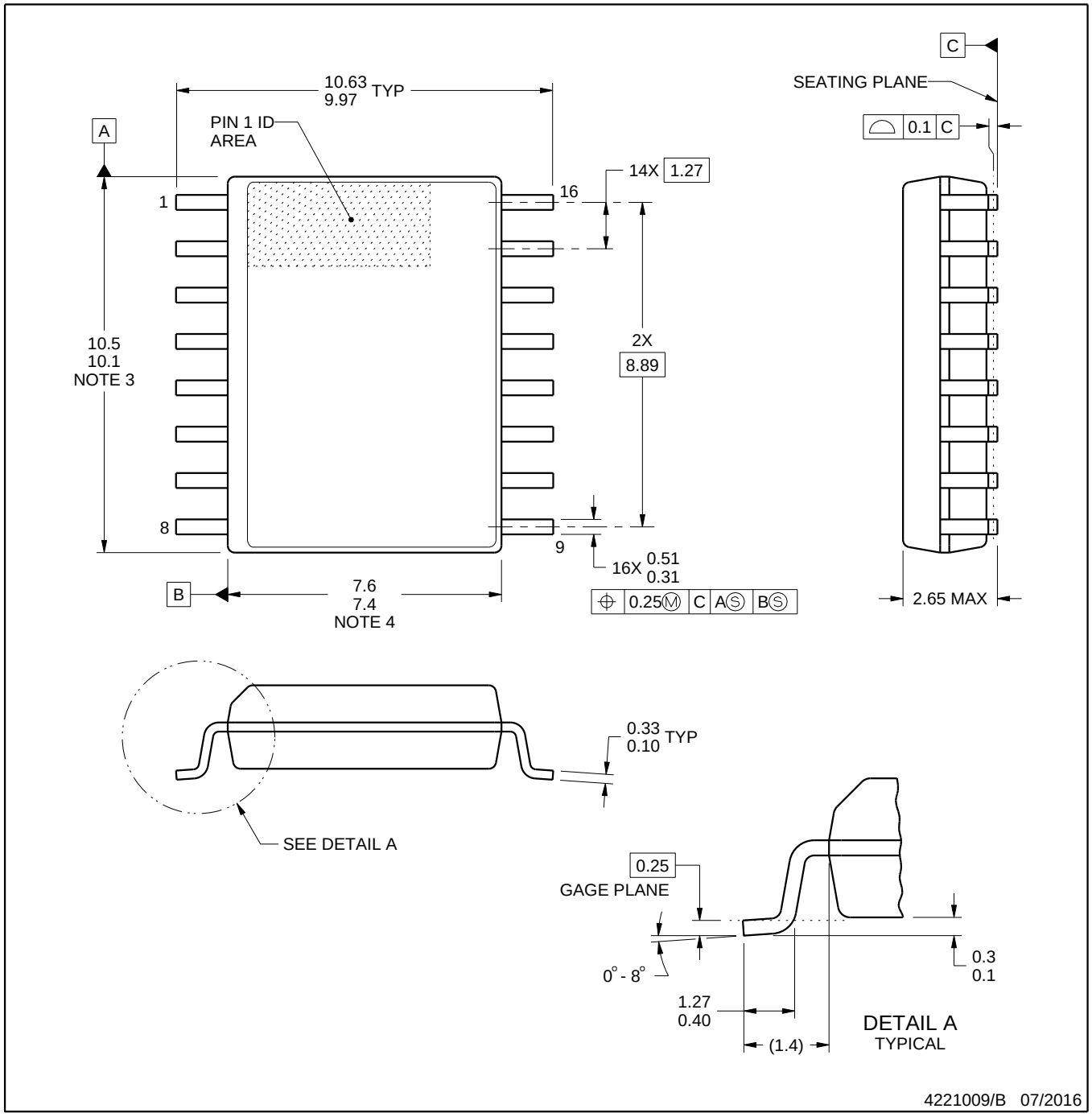
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



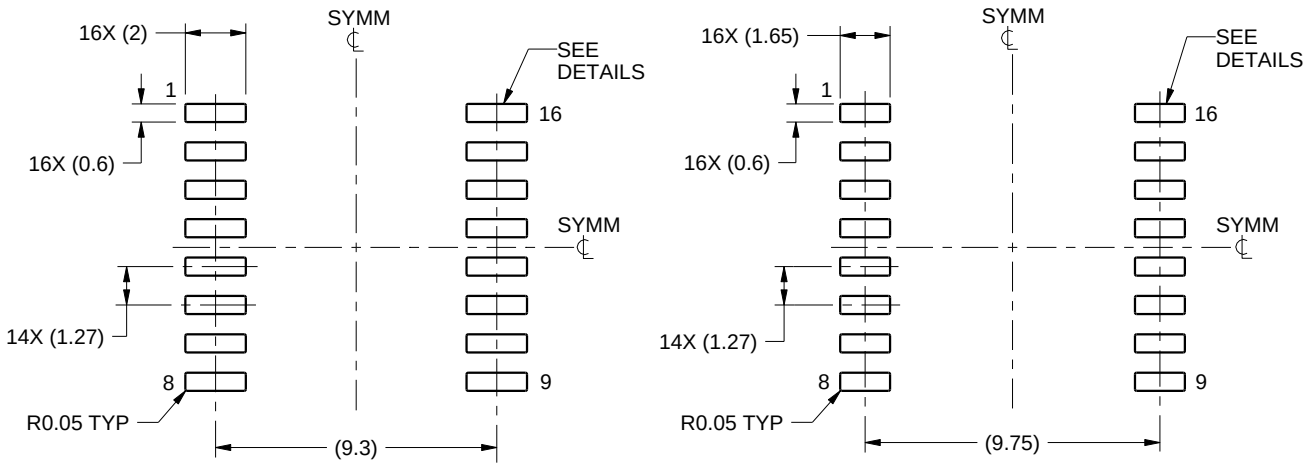
4224780/A

SOIC



NOTES:

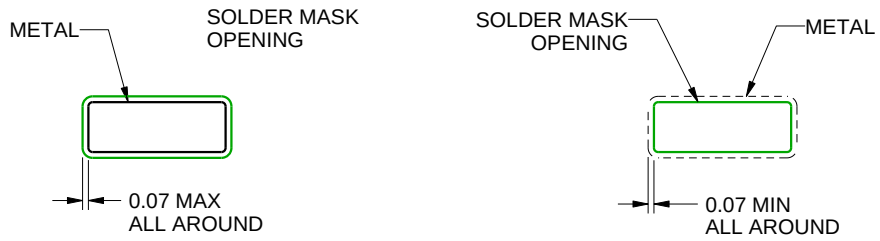
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

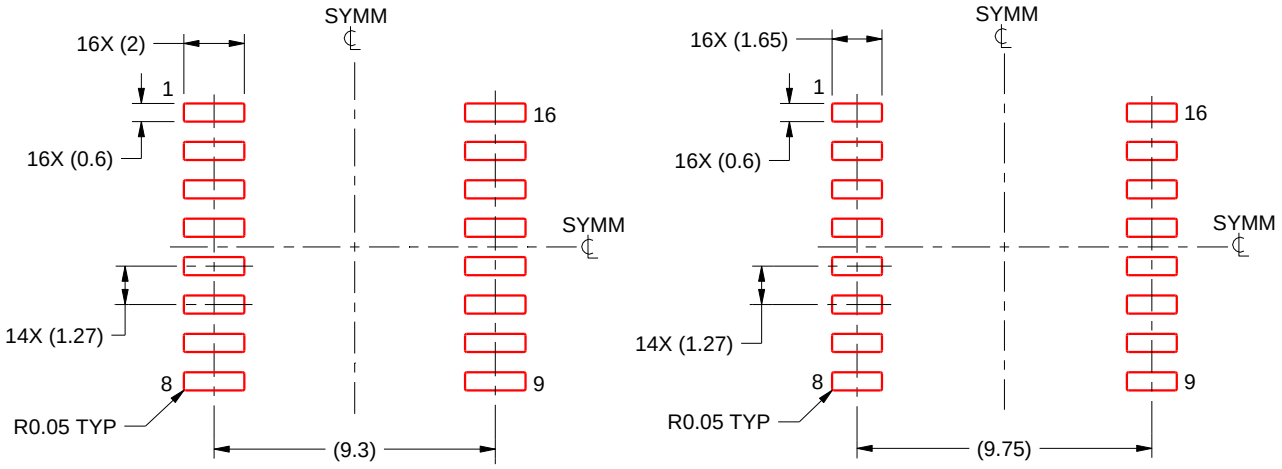
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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