ISO1042 Isolated CAN Transceiver With 70V Bus Fault Protection and Flexible Data Rate

1 Features

- Meets the ISO 11898-2:2016 physical layer standard
- Supports classic CAN up to 1Mbps and FD (Flexible Data Rate) up to 5Mbps
- Low loop delay: 152ns
- Protection features
  - DC bus fault protection voltage: ±70V
  - HBM ESD tolerance on bus pins: ±16kV
  - Driver Dominant Time Out (TXD DTO)
  - Undervoltage protection on V_{CC1} and V_{CC2}
- Common-Mode Voltage Range: ±30V
- Ideal passive, high-impedance bus terminals when unpowered
- High CMTI: 100kV/µs
- V_{CC1} voltage range: 1.71V to 5.5V
  - Supports 1.8V, 2.5V, 3.3V and 5.0V logic interface to the CAN controller
- V_{CC2} Voltage Range: 4.5V to 5.5V
- Robust Electromagnetic Compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Ambient Temperature Range: –40°C to +125°C
- 16-SOIC and 8-SOIC package options
- Automotive version available: ISO1042-Q1
- Safety-related certifications:
  - 7071V_{PK} V_{IOTM} and 1500V_{PK} V_{IORM} (Reinforced and Basic Options) per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5000V_{RMS} Isolation for 1 Minute per UL 1577
  - GB 4943.1, IEC 62368-1, IEC 60601-1 and IEC 61010-1 certifications
  - CQC, TUV and CSA certifications

2 Applications

- AC and servo drives
- Solar inverters
- PLC and DCS communication modules
- Elevators and escalators
- Industrial power supplies
- Battery charging and management

3 Description

The ISO1042 device is a galvanically-isolated controller area network (CAN) transceiver that meets the specifications of the ISO11898-2 (2016) standard. The ISO1042 device offers ±70V DC bus fault protection and ±30V common-mode voltage range. The device supports up to 5Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of 5000V_{RMS} and a working voltage of 1060V_{RMS}. Electromagnetic compatibility has been significantly enhanced to enable system-level ESD, EFT, surge, and emissions compliance. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. The ISO1042 device is available for both basic and reinforced isolation (see *Reinforced and Basic Isolation Options*). The ISO1042 device supports a wide ambient temperature range of –40°C to +125°C. The device is available in the SOIC-16 (DW) package and a smaller SOIC-8 (DWV) package.

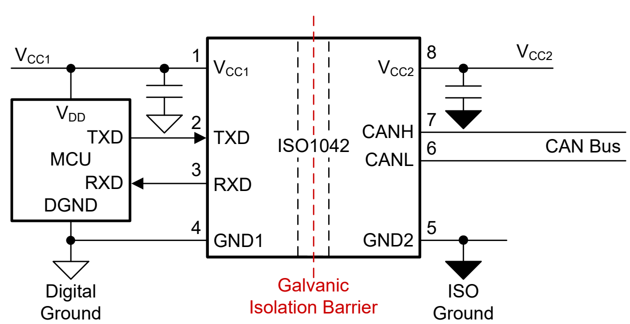
Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
ISO1042	DWV (SOIC, 8)	5.85mm × 11.50mm	5.85mm × 7.50mm
	DW (SOIC, 16)	10.30mm × 10.30mm	10.30mm × 7.50mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Reinforced and Basic Isolation Options

FEATURE	ISO1042x	ISO1042Bx
Protection Level	Reinforced	Basic
Surge Test Voltage	10000V_{PK}	6000V_{PK}
Isolation Rating	5000V_{RMS}	5000V_{RMS}
Working Voltage	1060V_{RMS} / 1500V_{PK}	1060V_{RMS} / 1500V_{PK}



Application Diagram

Table of Contents

4 Pin Configuration and Functions

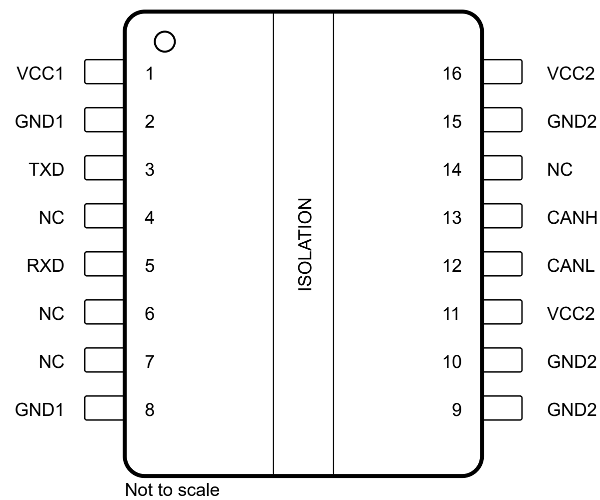


Figure 4-1. DW Package 16-Pin SOIC Top View

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_{CC1}	—	Digital-side supply voltage, Side 1
2	GND1	—	Digital-side ground connection, Side 1
3	TXD	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	NC	—	Not connected
5	RXD	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
6	NC	—	Not connected
7	NC	—	Not connected
8	GND1	—	Digital-side ground connection, Side 1

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
9	GND2	—	Transceiver-side ground connection, Side 2
10			
11	V_{CC2}	—	Transceiver-side supply voltage, Side 2. Must be externally connected to pin 16.
12	CANL	I/O	Low-level CAN bus line
13	CANH	I/O	High-level CAN bus line
14	NC	—	Not connected
15	GND2	—	Transceiver-side ground connection, Side 2
16	V_{CC2}	—	Transceiver-side supply voltage, Side 2. Must be externally connected to pin 11.

(1) I = Input; O = Output; I/O = Input or Output

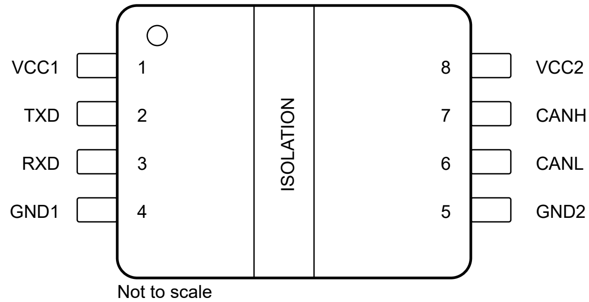


Figure 4-2. DWV Package 8-Pin SOIC Top View

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
1	V_{CC1}	—	Digital-side supply voltage, Side 1
2	TXD	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
3	RXD	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	GND1	—	Digital-side ground connection, Side 1
5	GND2	—	Transceiver-side ground connection, Side 2
6	CANL	I/O	Low-level CAN bus line
7	CANH	I/O	High-level CAN bus line
8	V_{CC2}	—	Transceiver-side supply voltage, Side 2

(1) I = Input; O = Output; I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
V_{CC1}	Supply voltage, side 1	-0.5	6	V
V_{CC2}	Supply voltage, side 2	-0.5	6	V
V_{IO}	Logic input and output voltage range (TXD and RXD)	-0.5	V_{CC1}+0.5[(3)]	V
I_O	Output current on RXD pin	-15	15	mA
V_{BUS}	Voltage on bus pins (CANH, CANL)	-70	70	V
V_{BUS_DIFF}	Differential voltage on bus pins (CANH-CANL)	-70	70	V
T_J	Junction temperature	-40	150	℃
T_{STG}	Storage temperature	-65	150	℃

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6V

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001	All pins[(1)]	±6000	V
		CANH and CANL to GND2[(1)]	±16000	V
	Electrostatic discharge Charged device model (CDM), per JEDEC specification JESD22-C101	All pins[(2)]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Transient Immunity

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{PULSE}	ISO7637-2 Transients according to GIFT - ICT CAN EMC test specification	Pulse 1; CAN bus terminals (CANH, CANL) to GND2	-100	V
		Pulse 2; CAN bus terminals (CANH, CANL) to GND2	75	V
		Pulse 3a; CAN bus terminals (CANH, CANL) to GND2	-150	V
		Pulse 3b; CAN bus terminals (CANH, CANL) to GND2	100	V

5.4 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC1}	Supply Voltage, Side 1, 1.8V operation	1.71	1.89	V
	Supply Voltage, Side 1, 2.5V, 3.3V and 5.5V operation	2.25	5.5	V
V_{CC2}	Supply Voltage, Side 2	4.5	5.5	V
T_A	Operating ambient temperature	-40	125	°C

5.5 Thermal Information

THERMAL METRIC[1]		ISO1042		UNIT
		DW (SOIC)	DWV (SOIC)	
		16 PINS	8 PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	69.9	100	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	40.8	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	29.0	51.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.2	16.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.6	49.8	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	See Figure 6-3, V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, R_L = 50Ω, A repetitive pattern on TXD with 1ms time period, 990µs LOW time, and 10µs HIGH time.			385	mW
P_{D1}	Maximum power dissipation (side-1)	See Figure 6-5, V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, R_L = 50Ω, Input a 2V pk-pk 2.5MHz 50% duty cycle differential square wave on CANH-CANL			25	mW
P_{D2}	Maximum power dissipation (side-2)	See Figure 6-3, V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, R_L = 50Ω, A repetitive pattern on TXD with 1ms time period, 990µs LOW time, and 10µs HIGH time.			360	mW

5.7 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS DW-16	SPECIFICATIONS DWV-8	UNIT
IEC 60664-1					
CLR	External clearance[(1)]	Side 1 to side 2 distance through air	>8.15	>8.5	mm
CPG	External Creepage[(1)]	Side 1 to side 2 distance across package surface	>8.15	>8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	
	Overvoltage category	Rated mains voltage ≤ $600V_{RMS}$	I-IV	I-IV	
		Rated mains voltage ≤ $1000V_{RMS}$	I-III	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) [(2)]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	1060	1060	V_{RMS}
		DC voltage	2121	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISO1042 [(3)]	Test method per IEC 62368-1, 1.2/50µs waveform	10000	10000	V_{PK}
	Maximum surge isolation voltage ISO1042B [(3)]	Test method per IEC 62368-1, 1.2/50µs waveform	6000	6000	V_{PK}
q_{pd}	Apparent charge[(4)]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; ISO1042: $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s ISO1042B: $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	≤ 5	
		At routine test (100% production), Method b1: $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; ISO1042: $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s ISO1042B: $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s, or Method b2: $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output[(5)]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1MHz	1	1	pF
R_{IO}	Insulation resistance, input to output[(5)]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 150°C	> 10^{11}	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^{9}	> 10^{9}	
	Pollution degree		2	2	
	Climatic category		40/125/21	40/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) ISO1042 is designed for *safe electrical insulation* and ISO1042B is designed for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of designed protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

5.8 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Certificates: Reinforced: 40040142 Basic: 40047657	Master contract number: 220991	File number: E181974	Certificate: CQC15001121716 (DW-16) CQC18001199096 (DWV-8)	Client ID number: 77311

5.9 Safety Limiting Values

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 69.9°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C, see Figure 5-1			325	mA
		$R_{\theta JA}$ = 69.9°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C, see Figure 5-1			496	
		$R_{\theta JA}$ = 69.9°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C, see Figure 5-1			650	
		$R_{\theta JA}$ = 69.9°C/W, V_I = 1.89V, T_J = 150°C, T_A = 25°C, see Figure 5-1			946	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 69.9°C/W, T_J = 150°C, T_A = 25°C, see Figure 5-3			1788	mW
T_S	Maximum safety temperature				150	°C
DWV-8 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 100°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C, see Figure 5-2			227	mA
		$R_{\theta JA}$ = 100°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C, see Figure 5-2			347	
		$R_{\theta JA}$ = 100°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C, see Figure 5-2			454	
		$R_{\theta JA}$ = 100°C/W, V_I = 1.89V, T_J = 150°C, T_A = 25°C, see Figure 5-2			661	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 100°C/W, T_J = 150°C, T_A = 25°C, see Figure 5-4			1250	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

5.10 Electrical Characteristics - DC Specification

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{CC1}	Supply current Side 1	V_{CC1} =1.71V to 1.89V, TXD = 0V, bus dominant		2.3	3.5	mA
		V_{CC1} = 2.25V to 5.5V, TXD = 0V, bus dominant		2.4	3.5	mA
		V_{CC1} = 1.71V to 1.89V, TXD = V_{CC1}, bus recessive		1.2	2.1	mA
		V_{CC1} = 2.25V to 5.5V, TXD = V_{CC1}, bus recessive		1.3	2.1	mA
I_{CC2}	Supply current Side 2	TXD = 0V, bus dominant, R_L = 60Ω		43	73.4	mA
		TXD = V_{CC1}, bus recessive, R_L = 60Ω		2.8	4.1	mA
UV_{VCC1}	Rising undervoltage detection, Side 1				1.7	V
UV_{VCC1}	Falling undervoltage detection, Side 1		1.0			V
$V_{HYS(UVCC1)}$	Hysteresis voltage on V_{CC1} undervoltage lock-out		75	125		mV
UV_{VCC2}	Rising undervoltage detection, side 2			4.2	4.45	V
UV_{VCC2}	Falling undervoltage detection, side 2		3.8	4.0	4.25	V
$V_{HYS(UVCC2)}$	Hysteresis voltage on V_{CC2} undervoltage lock-out			200		mV
TXD TERMINAL						
V_{IH}	High level input voltage		0.7 × V_{CC1}			V
V_{IL}	Low level input voltage				0.3 × V_{CC1}	V
I_{IH}	High level input leakage current	TXD = V_{CC1}			1	μA
I_{IL}	Low level input leakage current	TXD = 0V	-20			μA
C_I	Input capacitance	VIN = 0.4x sin(2 × π × 1E+6x t) + 2.5V, V_{CC1} = 5V		3		pF
RXD TERMINAL						
V_{OH} - V_{CC1}	High level output voltage	See Figure 6-4, I_O = -4mA for 4.5V ≤ V_{CC1} ≤ 5.5V	-0.4	-0.2		V
		See Figure 6-4, I_O = -2mA for 3.0V ≤ V_{CC1} ≤ 3.6V	-0.2	-0.07		V
		See Figure 6-4, I_O = -1mA for 2.25V ≤ V_{CC1} ≤ 2.75V	-0.1	-0.04		V
		See Figure 6-4, I_O = -1mA for 1.71V ≤ V_{CC1} ≤ 1.89V	-0.1	-0.045		V
V_{OL}	Low level output voltage	See Figure 6-4, I_O = 4mA for 4.5V ≤ V_{CC1} ≤ 5.5V		0.2	0.4	V
		See Figure 6-4, I_O = 2mA for 3.0V ≤ V_{CC1} ≤ 3.6V		0.07	0.2	V
		See Figure 6-4, I_O = 1mA for 2.25V ≤ V_{CC1} ≤ 2.75V		0.035	0.1	V
		See Figure 6-4, I_O = 1mA for 1.71V ≤ V_{CC1} ≤ 1.89V		0.04	0.1	V
DRIVER ELECTRICAL CHARACTERISTICS						

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(DOM)}$	Bus output voltage(Dominant), CANH	See Figure 6-1 and Figure 6-2, TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open	2.75		4.5	V
	Bus output voltage(Dominant), CANL	See Figure 6-1 and Figure 6-2, TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open	0.5		2.25	V
$V_{O(REC)}$	Bus output voltage(recessive), CANH and CANL	See Figure 6-1 and Figure 6-2, TXD = V_{CC1}, R_L = open	2.0	0.5 × VCC2	3.0	V
$V_{OD(DOM)}$	Differential output voltage, CANH-CANL (dominant)	See Figure 6-1 and Figure 6-2, TXD = 0V, 45Ω ≤ R_L ≤ 50Ω, C_L = open	1.4		3.0	V
	Differential output voltage, CANH-CANL (dominant)	See Figure 6-1 and Figure 6-2, TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open	1.5		3.0	V
	Differential output voltage, CANH-CANL (dominant)	See Figure 6-1 and Figure 6-2, TXD = 0V, R_L = 2240Ω, C_L = open	1.5		5.0	V
$V_{OD(REC)}$	Differential output voltage, CANH-CANL (recessive)	See Figure 6-1 and Figure 6-2, TXD = V_{CC1}, R_L = 60Ω, C_L = open	-120.0		12.0	mV
	Differential output voltage, CANH-CANL (recessive)	See Figure 6-1 and Figure 6-2, TXD = V_{CC1}, R_L = open, C_L = open	-50.0		50.0	mV
V_{SYM_DC}	DC Output symmetry (V_{CC2} - $V_{O(CANH)}$ - $V_{O(CANL)}$)	See Figure 6-1 and Figure 6-2, R_L = 60Ω, C_L = open, TXD = V_{CC1} or 0V	-400.0		400.0	mV
$I_{SO(SS\_DOM)}$	Short circuit current steady state output current, dominant	See Figure 6-9, VCANH = -5V to 40V, CANL = open, TXD = 0V	-100.0			mA
		See Figure 6-9, VCANL = -5V to 40V, CANH = open, TXD = 0V			100.0	mA
$I_{SO(SS\_REC)}$	Short circuit current steady state output current, recessive	See Figure 6-9, -27V ≤ VBUS ≤ 32V, VBUS = CANH = CANL, TXD = V_{CC1}	-5.0		5.0	mA
RECEIVER ELECTRICAL CHARACTERISTICS						
V_{IT}	Differential input threshold voltage	See Figure 6-4 and Table 6-1, |VCM| ≤ 20V	500.0		900.0	mV
	Differential input threshold voltage	See Figure 6-4 and Table 6-1, 20V ≤ |VCM| ≤ 30V	400.0		1000.0	
V_{HYS}	Hysteresis voltage for differential input threshold	See Figure 6-4 and Table 6-1		120		
V_{CM}	Input common mode range	See Figure 6-4 and Table 6-1	-30.0		30.0	V
$I_{OFF(LKG)}$	Power-off bus input leakage current	CANH = CANL = 5V, V_{CC2} to GND via 0Ω and 47kΩ resistor			4.8	μA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC1}		24.0	30	pF
C_{ID}	Differential input capacitance (CANH-CANL)	TXD = V_{CC1}		12.0	15	pF
R_{ID}	Differential input resistance	TXD = V_{CC1}; -30V ≤ VCM ≤ +30V	30.0		80.0	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD = V_{CC1}; -30V ≤ VCM ≤ +30V	15.0		40.0	kΩ
$R_{IN(M)}$	Input resistance matching: (1 - $R_{IN(CANH)}$/ $R_{IN(CANL)}$) x 100%	V_{CANH} = V_{CANL} = 5V	-2.0		2.0	%
THERMAL SHUTDOWN						
T_{TSD}	Thermal shutdown temperature			170		°C
T_{TSD_HYST}	Thermal shutdown hysteresis			5		°C

5.11 Switching Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver RXD, recessive to dominant	See Figure 6-6, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns; 1.71V ≤ V_{CC1} ≤ 1.89V	70	125	198.0	ns
		See Figure 6-6, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns; 2.25V ≤ V_{CC1} ≤ 5.5V	70	122	192.0	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver RXD, dominant to recessive	See Figure 6-6, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns; 1.71V ≤ V_{CC1} ≤ 1.89V	70	155	215.0	ns
		See Figure 6-6, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns; 2.25V ≤ V_{CC1} ≤ 5.5V	70	152	215.0	ns
$t_{UV\_RE\_ENABLE}$	Re-enable time after Undervoltage event	Time for device to return to normal operation from V_{CC1} or V_{CC2} undervoltage event			300.0	μs
CMTI	Common mode transient immunity	V_{CM} = 1200V_{PK}, See Figure 6-10	85	100		kV/μs
DRIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, HIGH TXD to driver recessive	See Figure 6-3, R_L = 60Ω and C_L = 100pF; input rise/fall time (10% to 90%) on TXD = 1ns		76	120	ns
t_{pLD}	Propagation delay time, LOW TXD to driver dominant			61	120	
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			14		
t_R	Differential output signal rise time			45		
t_F	Differential output signal fall time			45		
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC2}	See Figure 6-3 and Figure 8-4 , R_{TERM} = 60Ω, C_{SPLIT} = 4.7nF, C_L = open, R_L = open, TXD = 250kHz, 1MHz	0.9		1.1	V/V
t_{TXD_DTO}	Dominant time out	See Figure 6-8, R_L = 60Ω and C_L = open	1.2		3.8	ms
RECEIVER SWITCHING CHARACTERISTICS						
t_{pRH}	Propagation delay time, bus recessive input to RXD high output	See Figure 6-5, $C_{L(RXD)}$ = 15pF		75	130	ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output			63	130	ns
t_R	Output signal rise time(RXD)			1.4		ns
t_F	Output signal fall time(RXD)			1.8		ns
FD TIMING PARAMETERS						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500ns	See Figure 6-7, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns	435.0		530.0	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200ns	See Figure 6-7, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns	155.0		210.0	ns

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500ns	See Figure 6-7, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns	400		550.0	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200ns	See Figure 6-7, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns	120.0		220.0	ns
ΔtREC	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns	See Figure 6-7, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns; ΔtREC = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$	-65.0		40.0	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns	See Figure 6-7, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF; input rise/fall time (10% to 90%) on TXD = 1ns; ΔtREC = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$	-45.0		15.0	ns

5.12 Insulation Characteristics Curves

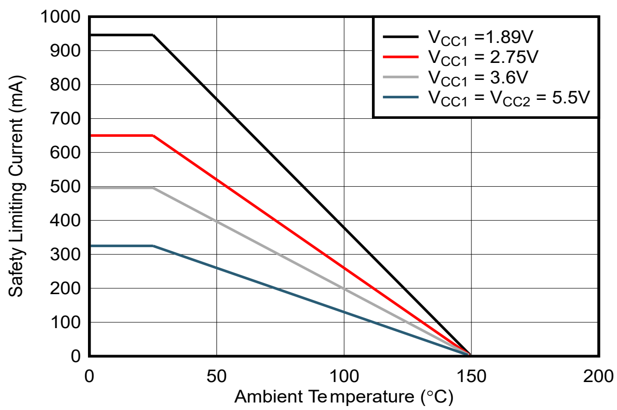


Figure 5-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

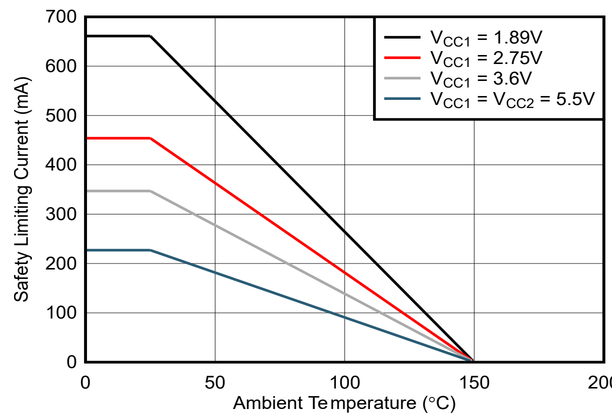


Figure 5-2. Thermal Derating Curve for Limiting Current per VDE for DWV-8 Package

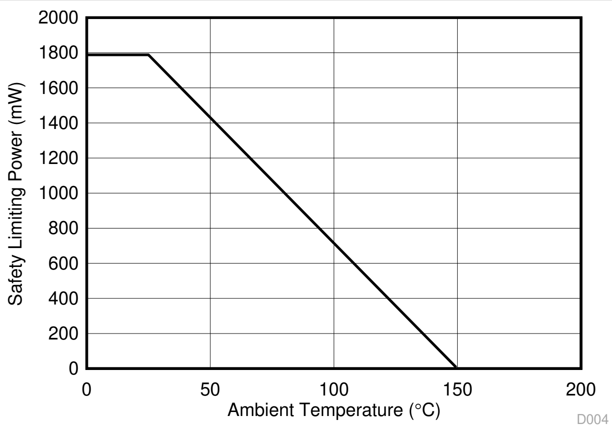


Figure 5-3. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

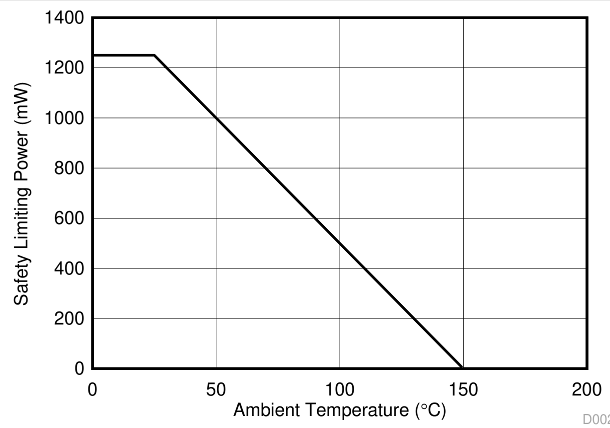
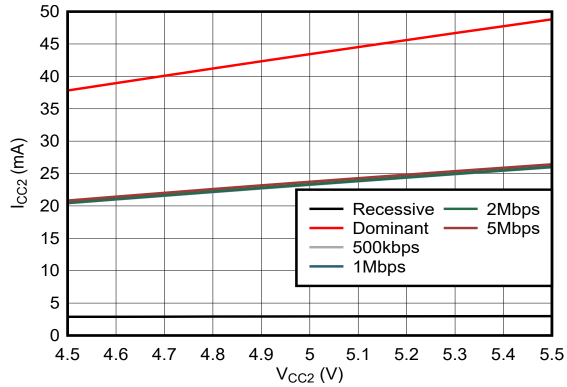


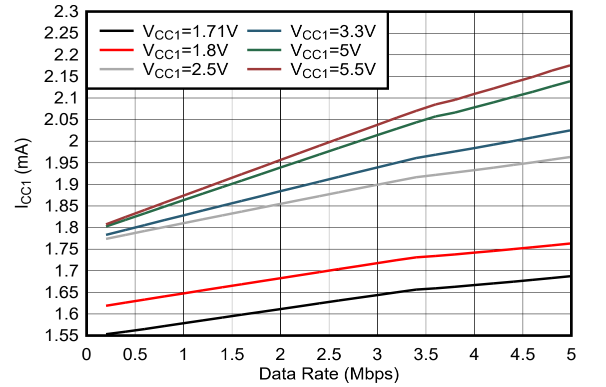
Figure 5-4. Thermal Derating Curve for Limiting Power per VDE for DWV-8 Package

5.13 Typical Characteristics



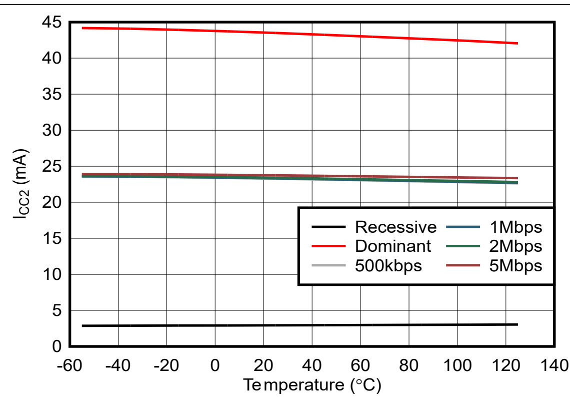
V_{CC1} = 5V R_L = 60Ω $C_{L(RXD)}$ = 15pF
Temp = 25°C

Figure 5-5. I_{CC2} vs V_{CC2} for Recessive, Dominant and Different CAN Datarates



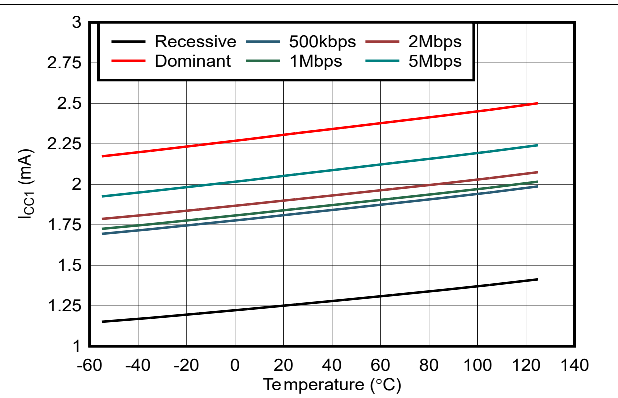
V_{CC2} = 5V R_L = 60Ω $C_{L(RXD)}$ = 15pF
Temp = 25°C

Figure 5-6. I_{CC1} vs Datarate



V_{CC1} = V_{CC2} = 5V R_L = 60Ω $C_{L(RXD)}$ = 15pF

Figure 5-7. I_{CC2} vs Ambient Temperature for Recessive, Dominant and Different CAN Datarates

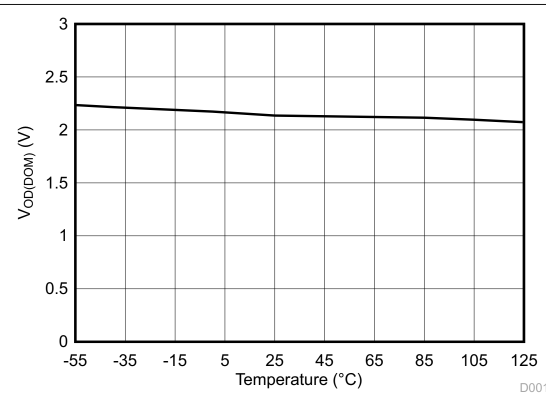


V_{CC1} = V_{CC2} = 5V R_L = 60Ω $C_{L(RXD)}$ = 15pF
Temp = 25°C

Figure 5-8. : ICC1 vs Ambient Temperature for Recessive, Dominant and Different CAN Datarates.

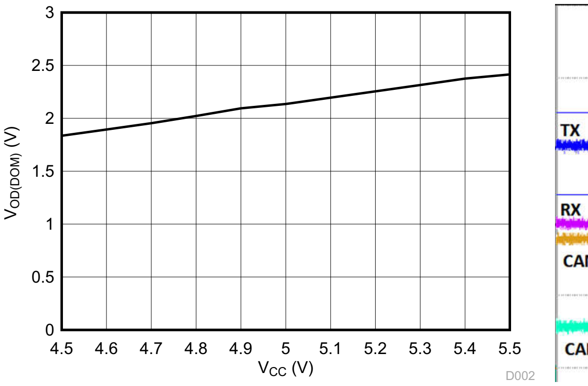
V_{CC1} = V_{CC2} = 5V R_L = 60Ω $C_{L(RXD)}$ = 15pF

Figure 5-9. Loop Delay vs Ambient Temperature



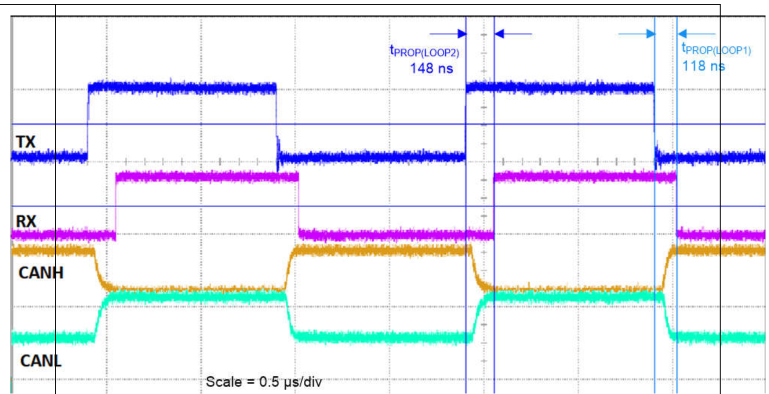
V_{CC} = 5V V_{CC1} = 5V R_L = 60Ω
C_L = Open

Figure 5-10. $V_{OD(DOM)}$ Over Temperature



V_{CC1} = 5V R_L = 60Ω
C_L = Open Temp = 25°C

Figure 5-11. $V_{OD(DOM)}$ Over V_{CC}

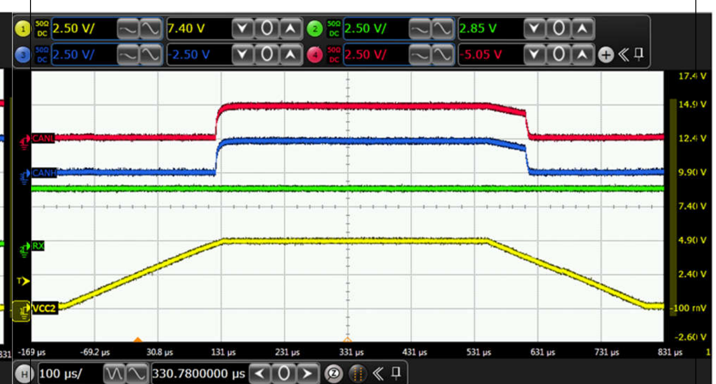


V_{CC1} = V_{CC2} = 5V R_L = 60Ω C_L = 100pF
$C_{L(RXD)}$ = 15pF

Figure 5-12. Typical TXD, RXD, CANH and CANL Waveforms at 1Mbps

TXD = V_{CC1} R_L = 60Ω V_{CC1} = V_{CC2} = 5V

Figure 5-13. Glitch Free Power Up on V_{CC1} – CAN Bus Remains Recessive



TXD = V_{CC1} R_L = 60Ω V_{CC1} = V_{CC2} = 5V

Figure 5-14. Glitch Free Power Up on V_{CC2} – CAN Bus Remains Recessive

6 Parameter Measurement Information

6.1 Test Circuits

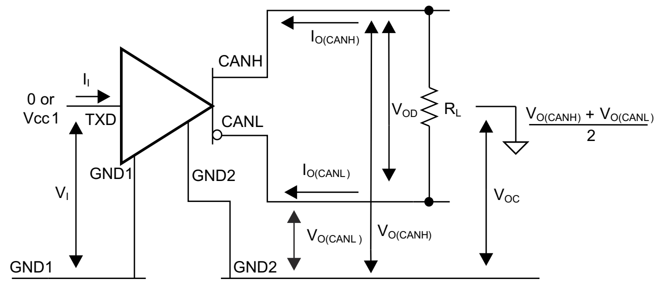


Figure 6-1. Driver Voltage, Current and Test Definitions

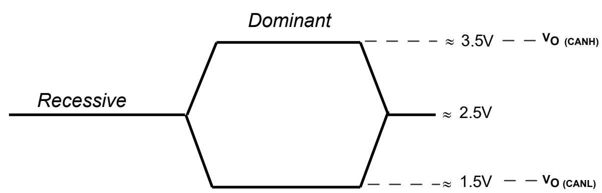
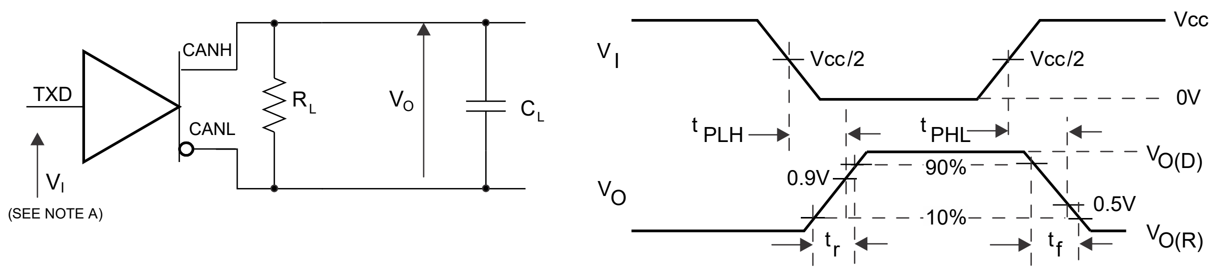


Figure 6-2. Bus Logic State Voltage Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-3. Driver Test Circuit and Voltage Waveforms

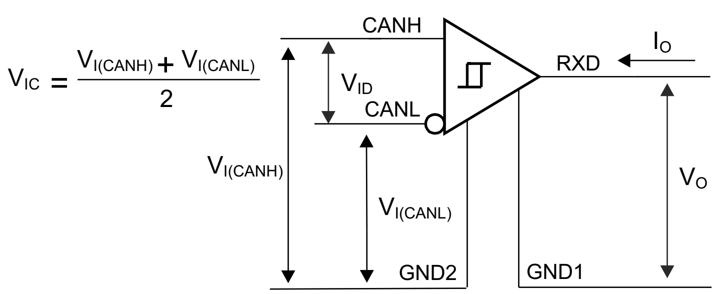
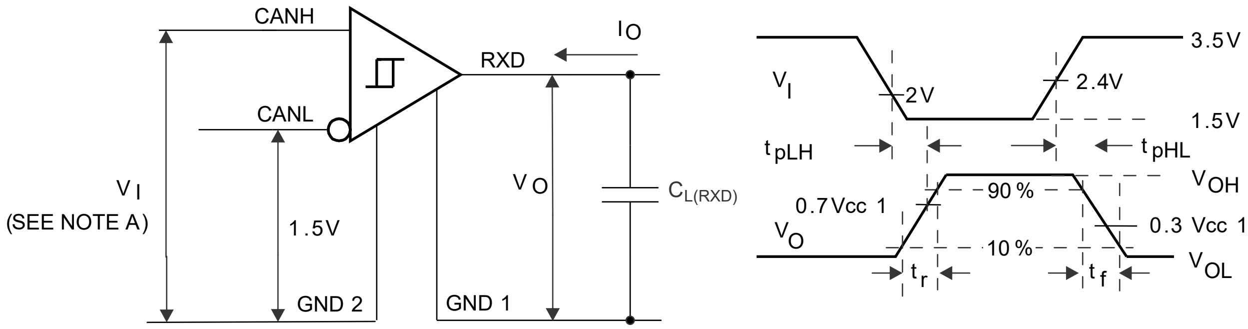


Figure 6-4. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-5. Receiver Test Circuit and Voltage Waveforms

Table 6-1. Receiver Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\|V_{ID}\|$	RXD	
-29.5V	-30.5V	1000mV	L	V_{OL}
30.5V	29.5V	1000mV	L	
-19.55V	-20.45V	900mV	L	
20.45V	19.55V	900mV	L	
-19.75V	-20.25V	500mV	H	V_{OH}
20.25V	19.75V	500mV	H	
-29.8V	-30.2V	400mV	H	
30.2V	29.8V	400mV	H	
Open	Open	X	H	

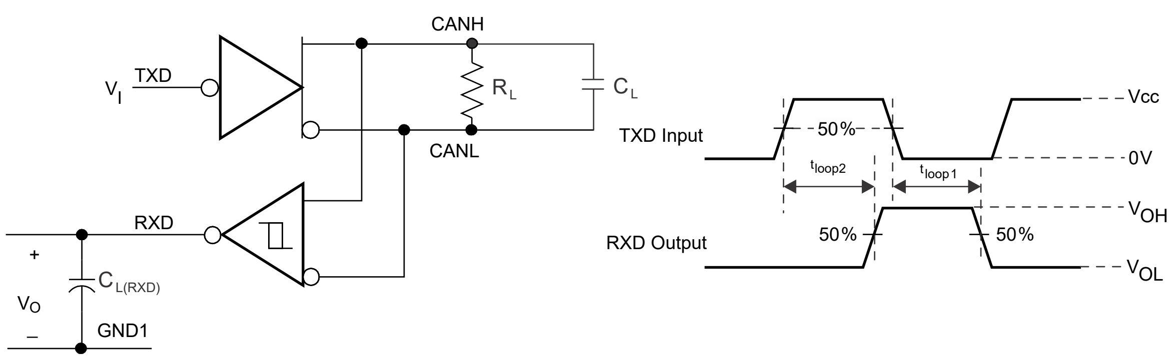


Figure 6-6. t_{LOOP} Test Circuit and Voltage Waveforms

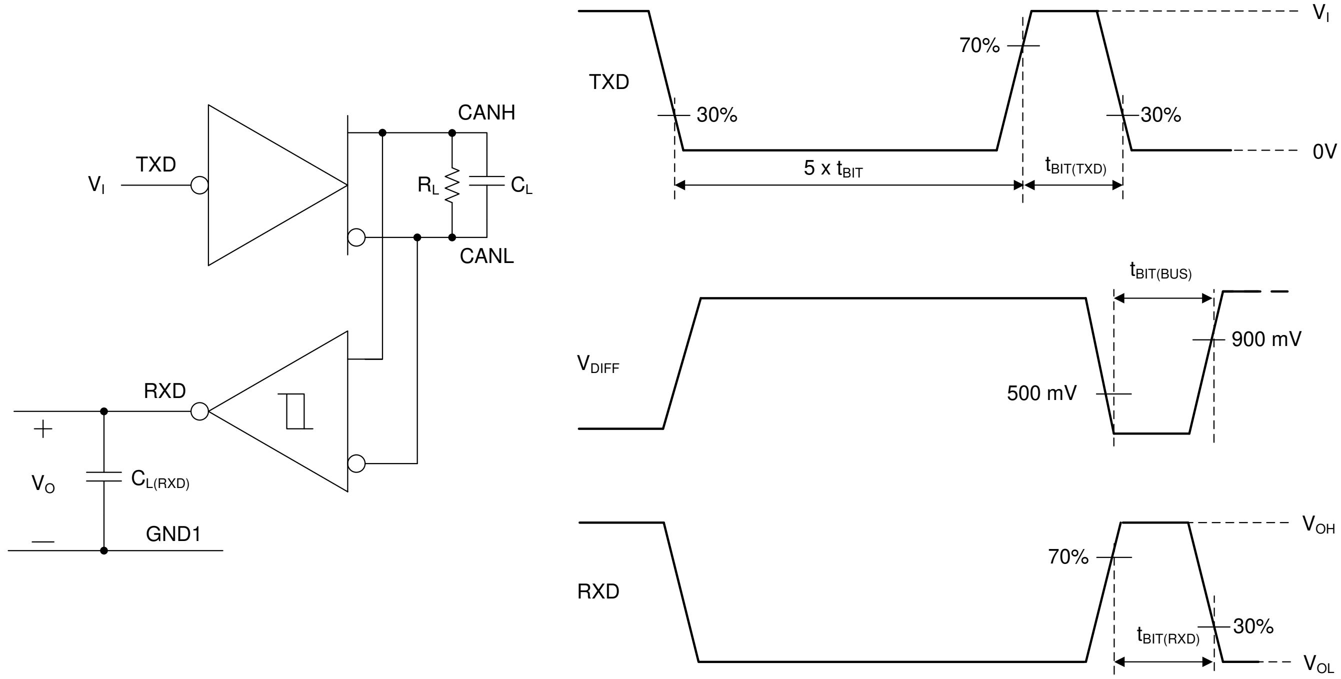
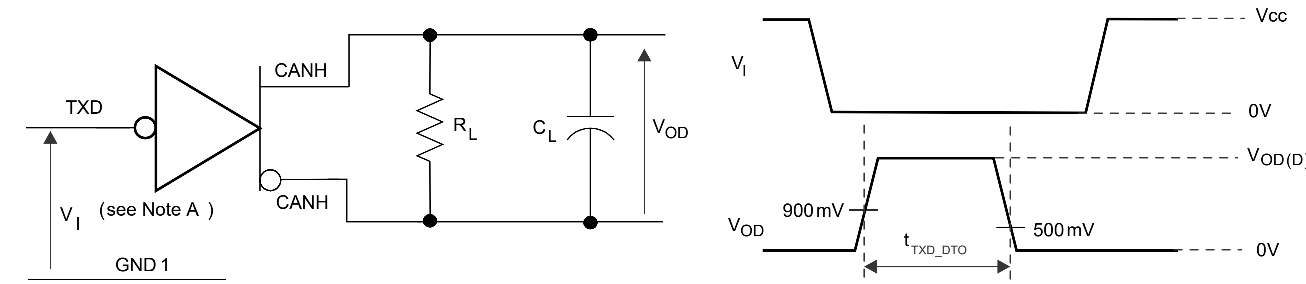


Figure 6-7. CAN FD Timing Parameter Measurement



A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 6ns$, $t_f \leq 6ns$, $Z_O = 50\Omega$.

Figure 6-8. Dominant Time-out Test Circuit and Voltage Waveforms

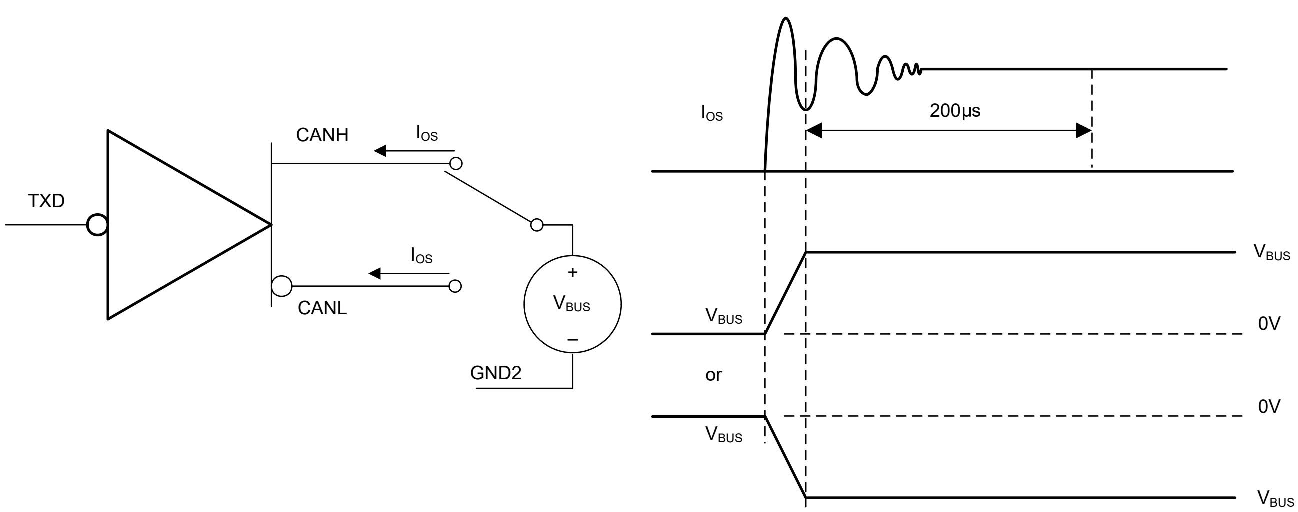


Figure 6-9. Driver Short-Circuit Current Test Circuit and Waveforms

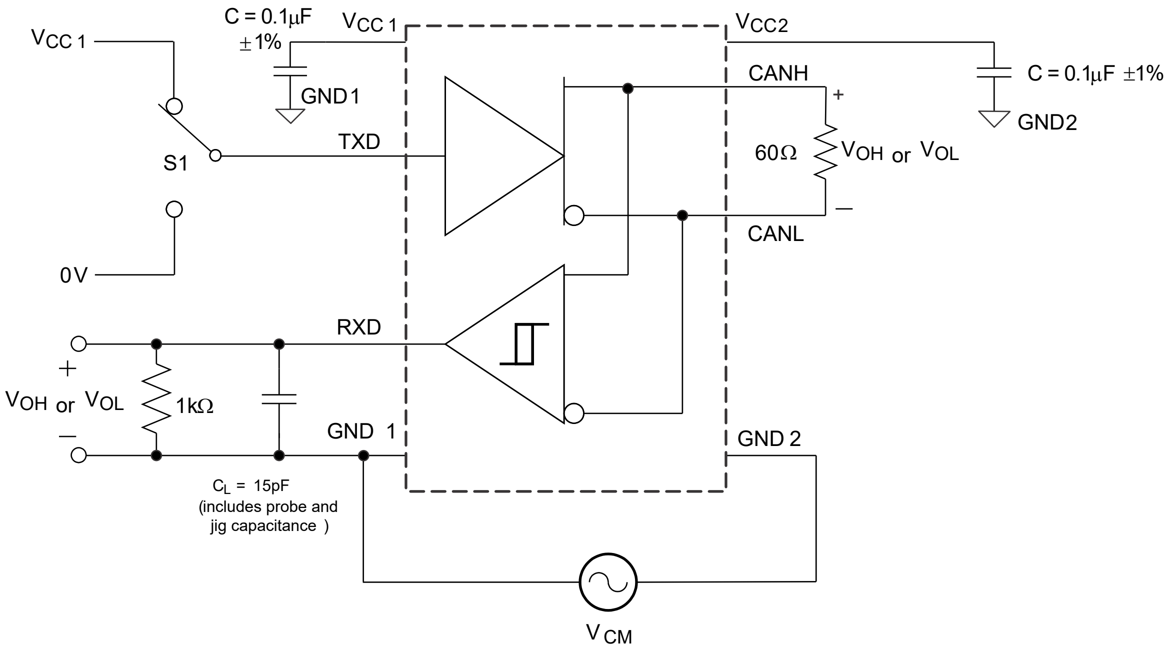


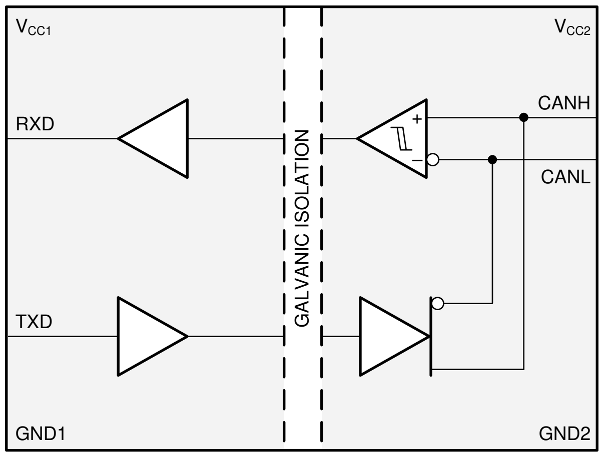
Figure 6-10. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO1042 device is a digitally isolated CAN transceiver that offers ±70V DC bus fault protection and ±30V common-mode voltage range. The device supports up to 5Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. The ISO1042 device has an isolation withstand voltage of 5000V_{RMS} and is available in basic and reinforced isolation with a surge test voltage of 6kV_{PK} and 10kV_{PK} respectively. The device can operate from 1.8V, 2.5V, 3.3V, and 5V supplies on side 1 and a 5V supply on side 2. This supply range is of particular advantage for applications operating in harsh industrial environments because the low voltage on side 1 enables the connection to low-voltage microcontrollers for power conservation, whereas the 5V on side 2 maintains a high signal-to-noise ratio of the bus signals.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 CAN Bus States

The CAN bus has two states during operation: *dominant* and *recessive*. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state is when the bus is biased to a common mode of V_{CC} / 2 through the high-resistance internal input resistors of the receiver, equivalent to a logic high. The host microprocessor of the CAN node uses the TXD pin to drive the bus and receives data from the bus on the RXD pin. See Figure 7-1 and Figure 7-2.

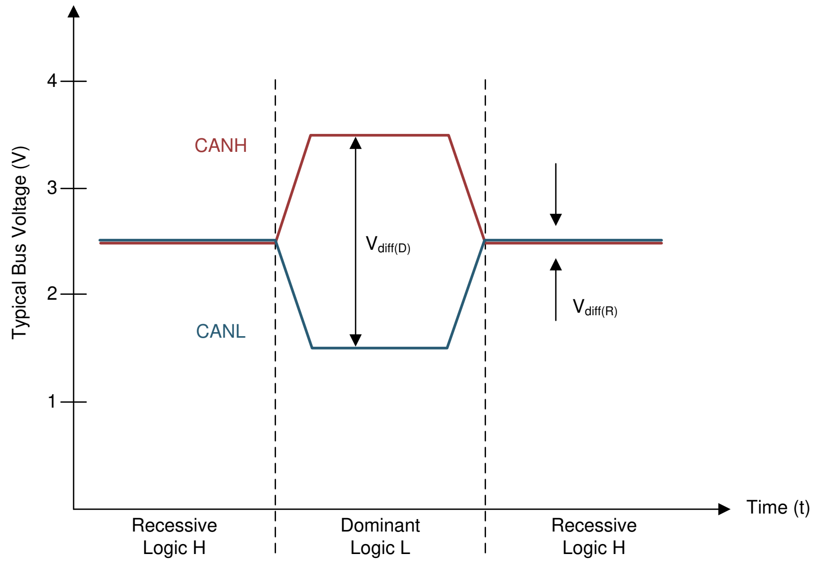


Figure 7-1. Bus States (Physical Bit Representation)

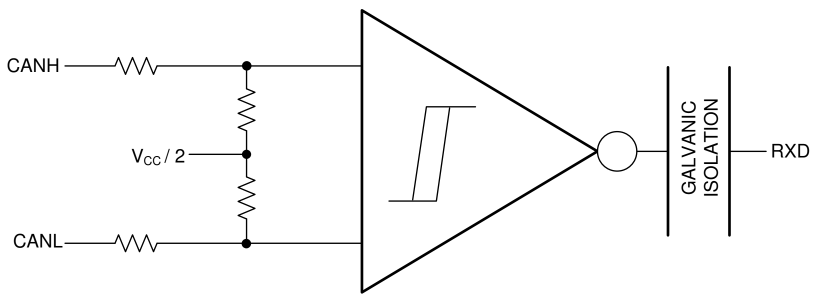


Figure 7-2. Simplified Recessive Common Mode Bias and Receiver

7.3.2 Digital Inputs and Outputs: TXD (Input) and RXD (Output)

The V_{CC1} supply for the isolated digital input and output side of the device can be supplied by 1.8V, 2.5V, 3.3V, and 5V supplies and therefore the digital inputs and outputs are 1.8V, 2.5V, 3.3V, and 5V compatible.

Note

The TXD pin is very weakly internally pulled up to V_{CC1}. An external pullup resistor must be used to make sure that the TXD pin is biased to recessive (high) level to avoid issues on the bus if the microprocessor does not control the pin and the TXD pin floats. The TXD pullup strength and CAN bit timing require special consideration when the device is used with an open-drain TXD output on the CAN controller of the microprocessor. An adequate external pullup resistor must be used to make sure that the TXD output of the microprocessor maintains adequate bit timing input to the input on the transceiver.

7.3.3 Protection Features

7.3.3.1 TXD Dominant Timeout (DTO)

The TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where the TXD pin is held dominant longer than the timeout period, t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on the TXD pin. The DTO circuit disables the CAN bus driver if no rising edge occurs before the timeout period expires, which frees the bus for communication between other nodes on the network. The CAN driver is activated again when a recessive signal occurs on the TXD pin, clearing the TXD

DTO condition. The receiver and RXD pin still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

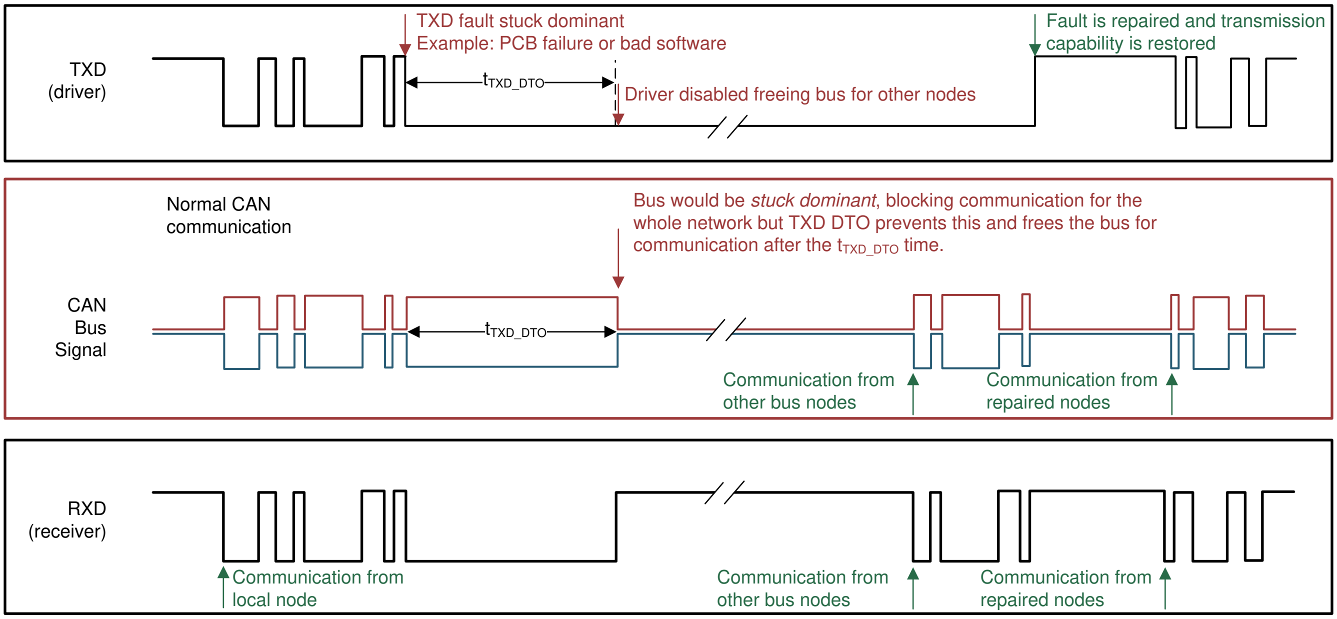


Figure 7-3. Example Timing Diagram for TXD DTO

Note

The minimum dominant TXD time (t_{TXD_DTO}) allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate with Equation 1.

$$\text{Minimum Data Rate} = 11 / t_{TXD\_DTO} \tag{1}$$

7.3.3.2 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold (T_{TSD}), the device turns off the CAN driver circuits, blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature (T_{TSD_HYST}) below the thermal shutdown temperature (T_{TSD}) of the device.

7.3.3.3 Undervoltage Lockout and Default State

The supply pins have undervoltage detection that places the device in protected or default mode which protects the bus during an undervoltage event on the V_{CC1} or V_{CC2} supply pins. If the bus-side power supply, V_{CC2}, is less than about 4V, the power shutdown circuits in the ISO1042 device disable the transceiver to prevent false transmissions because of an unstable supply. If the V_{CC1} supply is still active when this occurs, the receiver output (RXD) goes to a default HIGH (recessive) value. Table 7-1 summarizes the undervoltage lockout and fail-safe behavior.

Table 7-1. Undervoltage Lockout and Default State

V_{CC1}	V_{CC2}	DEVICE STATE	BUS OUTPUT	RXD
> UV_{VCC1}	> UV_{VCC2}	Functional	Per Device State and TXD	Mirrors Bus
<UV_{VCC1}	> UV_{VCC2}	Protected	Recessive	Undetermined

Table 7-1. Undervoltage Lockout and Default State (continued)

V_{CC1}	V_{CC2}	DEVICE STATE	BUS OUTPUT	RXD
$>UV_{VCC1}$	$< UV_{VCC2}$	Protected	High Impedance	Recessive (Default High)

Note

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300μs.

7.3.3.4 Floating Pins

Pullup and pulldown resistors must be used on critical pins to place the device into known states if the pins float. The TXD pin must be pulled up through a resistor to the V_{CC1} pin to force a recessive input level if the microprocessor output to the pin floats.

7.3.3.5 Unpowered Device

The device is designed to be *ideal passive* or *no load* to the CAN bus if the device is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus which is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

7.3.3.6 CAN Bus Short Circuit Current Limiting

The device has two protection features that limit the short circuit current when a CAN bus line has a short-circuit fault condition. The first protection feature is driver current limiting (both dominant and recessive states) and the second feature is TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states, therefore the short circuit current can be viewed either as the instantaneous current during each bus state or as an average current of the two states. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

These factors verify a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits. The short circuit current of the bus depends on the ratio of recessive to dominant bits and the respective short circuit currents. Use Equation 2 to calculate the average short circuit current.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (2)$$

where

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

Note

Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

7.4 Device Functional Modes

Table 7-2 and Table 7-3 list the driver and receiver functions. Table 7-4 lists the functional modes for the ISO1042 device.

Table 7-2. Driver Function Table

INPUT	OUTPUTS		DRIVEN BUS STATE
TXD[(1)]	CANH[(1)]	CANL[(1)]	
L	H	L	Dominant
H	Z	Z	Recessive

(1) H = high level, L = low-level, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 7-1 and Figure 7-2 for bus state and common mode bias information.

Table 7-3. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$ [(3)]	BUS STATE	RXD PIN[(1)]
Normal	$V_{ID} \geq V_{IT(MAX)}$	Dominant	L
	$V_{IT(MIN)} < V_{ID} < V_{IT(MAX)}$	?	?
	$V_{ID} \leq V_{IT(MIN)}$	Recessive	H
	Open ($V_{ID} \cong 0V$)	Open	H

(1) H = high level, L = low-level, ? = indeterminate.

Table 7-4. Function Table

DRIVER[(1)]				RECEIVER		
INPUTS	OUTPUTS		BUS STATE	DIFFERENTIAL INPUTS V_{ID} = CANH–CANL[(3)]	OUTPUT RXD	BUS STATE
TXD	CANH	CANL				
L[(2)]	H	L	DOMINANT	$V_{ID} \geq V_{IT(MAX)}$	L	DOMINANT
H	Z	Z	RECESSIVE	$V_{IT(MIN)} < V_{ID} < V_{IT(MAX)}$	?	?
Open	Z	Z	RECESSIVE	$V_{ID} \leq V_{IT(MIN)}$	H	RECESSIVE
X	Z	Z	RECESSIVE	Open ($V_{ID} \cong 0V$)	H	RECESSIVE

(1) H = high level; L = low-level; X = irrelevant; ? = indeterminate; Z = high-impedance
(2) Logic low pulses to prevent dominant time-out.
(3) See Receiver Electrical Characteristics section for input thresholds.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO1042 device can be used with other components from Texas Instruments such as a microcontroller, a transformer driver, and a linear voltage regulator to form a fully isolated CAN interface.

8.2 Typical Application

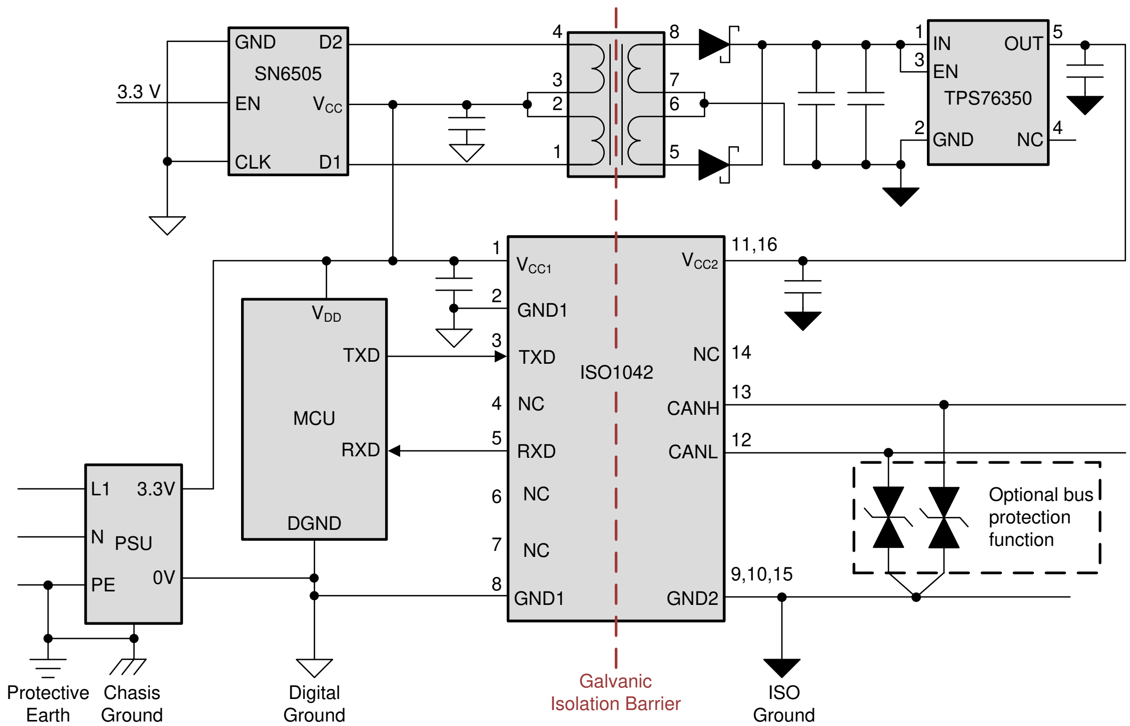


Figure 8-1. Application Circuit With ISO1042 in 16-SOIC Package

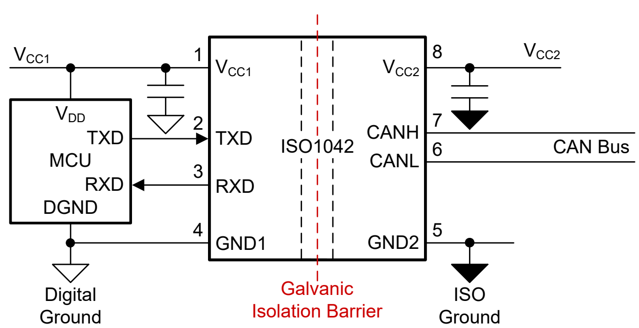


Figure 8-2. Application Circuit With ISO1042 in 8-SOIC Package

8.2.1 Design Requirements

Unlike an optocoupler-based design, which requires several external components to improve performance, provide bias, or limit current, the ISO1042 device only requires external bypass capacitors to operate.

8.2.2 Detailed Design Procedure

8.2.2.1 Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the ISO1042 transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 Standard. These organizations and standards have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet, and NMEA2000.

The ISO1042 device is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the ISO1042 device is a minimum of 30kΩ. If 100 ISO1042 transceivers are in parallel on a bus, this requirement is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the ISO1042 device theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity, therefore a practical maximum number of nodes is typically much lower. Bus length can also be extended beyond the original ISO 11898 standard of 40m by careful system design and data-rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes, and a significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. Using this flexibility requires the responsibility of good network design and balancing these tradeoffs.

8.2.2.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination can be in a node, but if nodes are removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

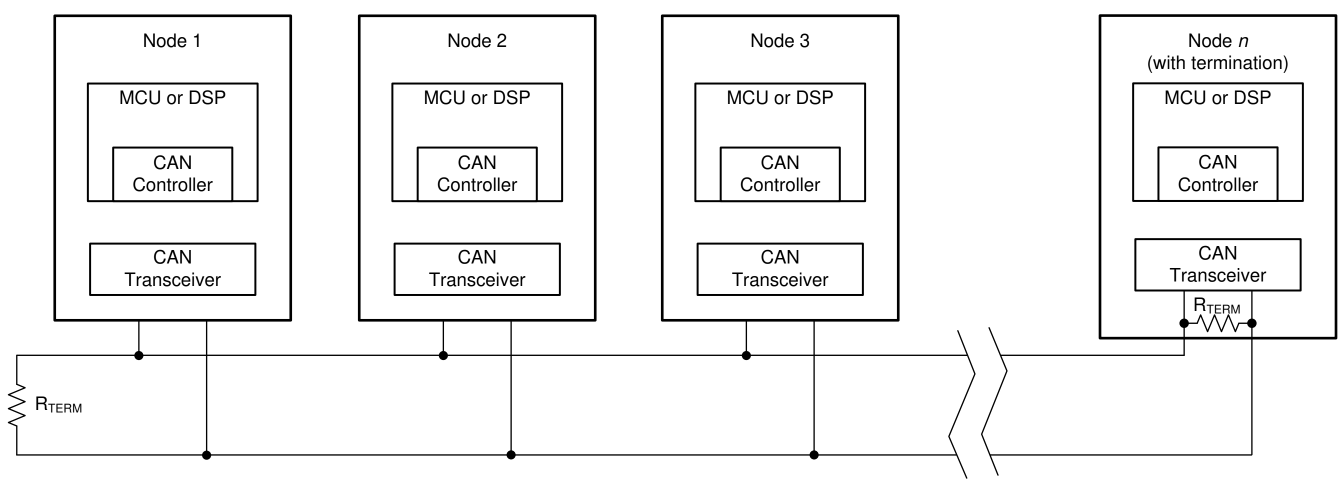


Figure 8-3. Typical CAN Bus

Termination can be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used. (See Figure 8-4). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

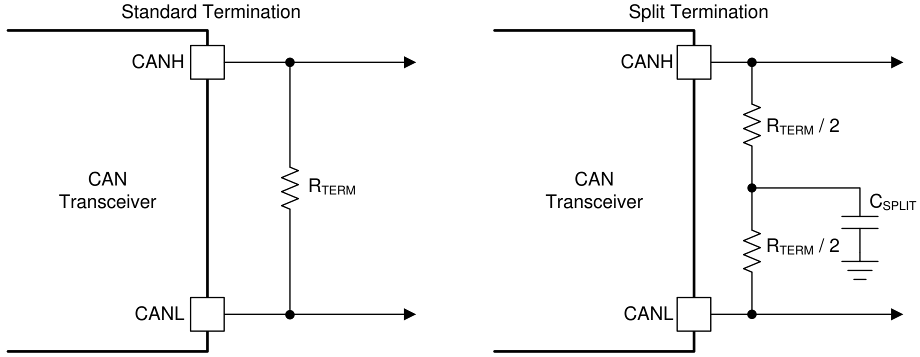


Figure 8-4. CAN Bus Termination Concepts

8.2.3 Application Curve

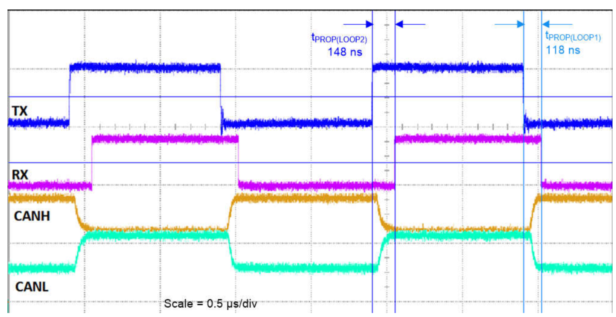


Figure 8-5. Typical TXD, RXD, CANH and CANL Waveforms at 1Mbps

8.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 8-6 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that is 20% higher than the specified value.

Figure 8-7 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is $1060V_{RMS}$ with a lifetime of 275 years. Other factors, such as package size, pollution degree, material group, and so forth, can further limit the working voltage of the component. The working voltage of DW-16 is specified up to $1060V_{RMS}$. At the lower working voltages, the corresponding insulation lifetime is much longer than 275 years.

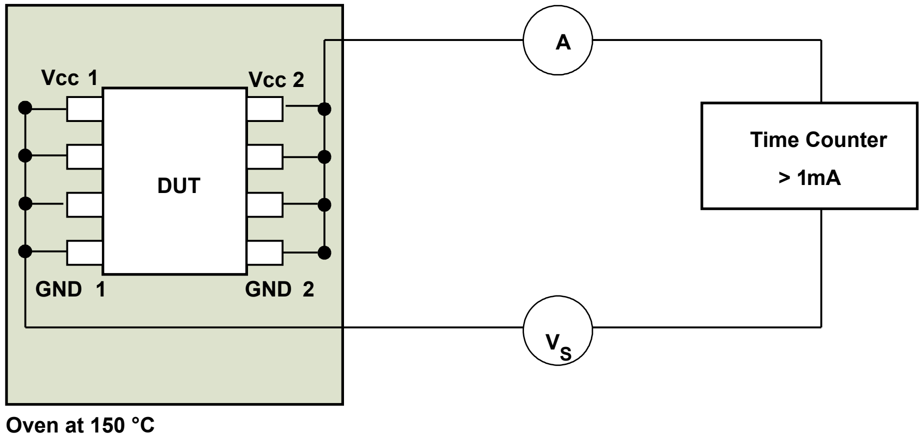


Figure 8-6. Test Setup for Insulation Lifetime Measurement

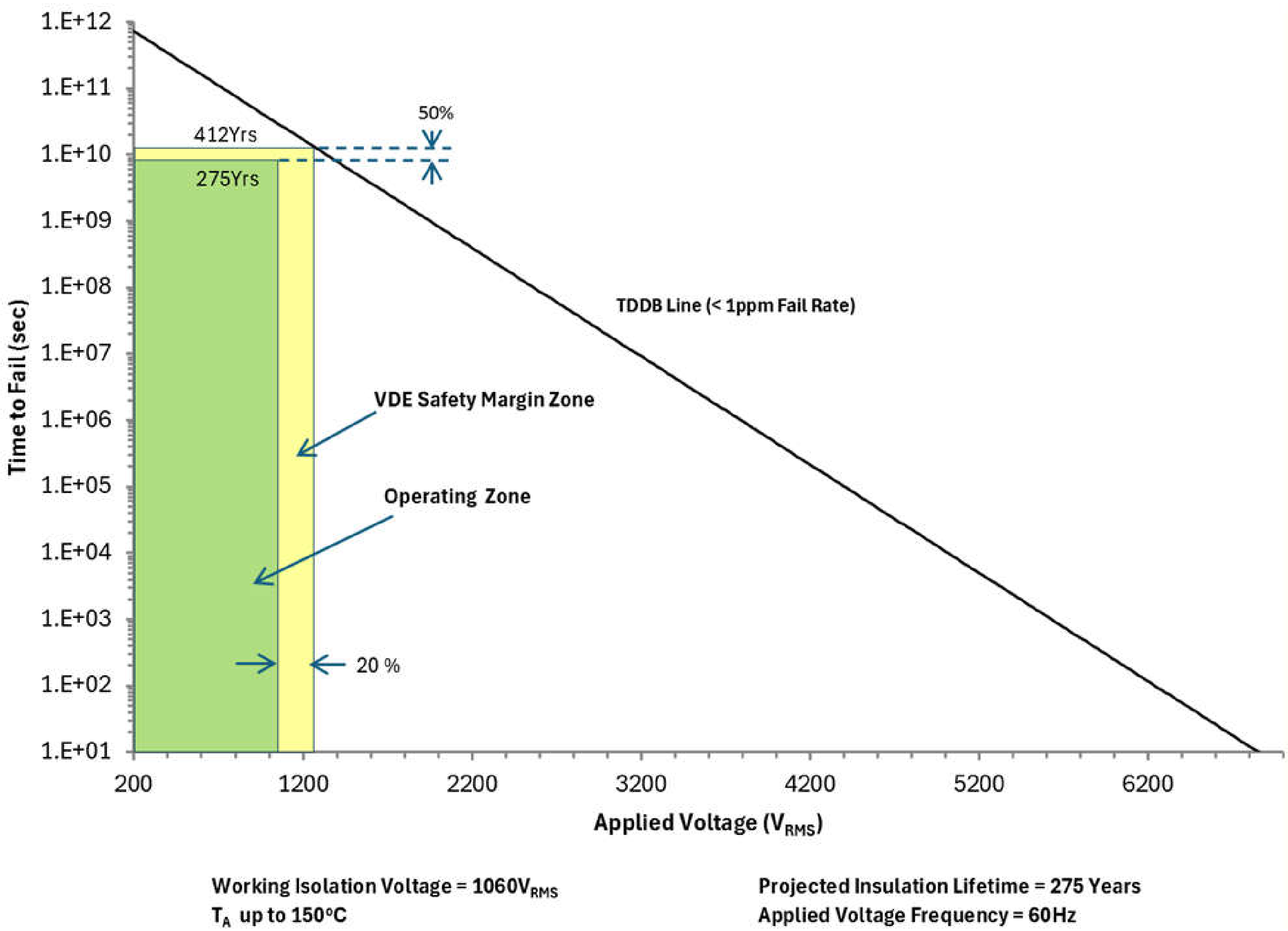


Figure 8-7. Insulation Lifetime Projection Data

8.3 DeviceNet Application

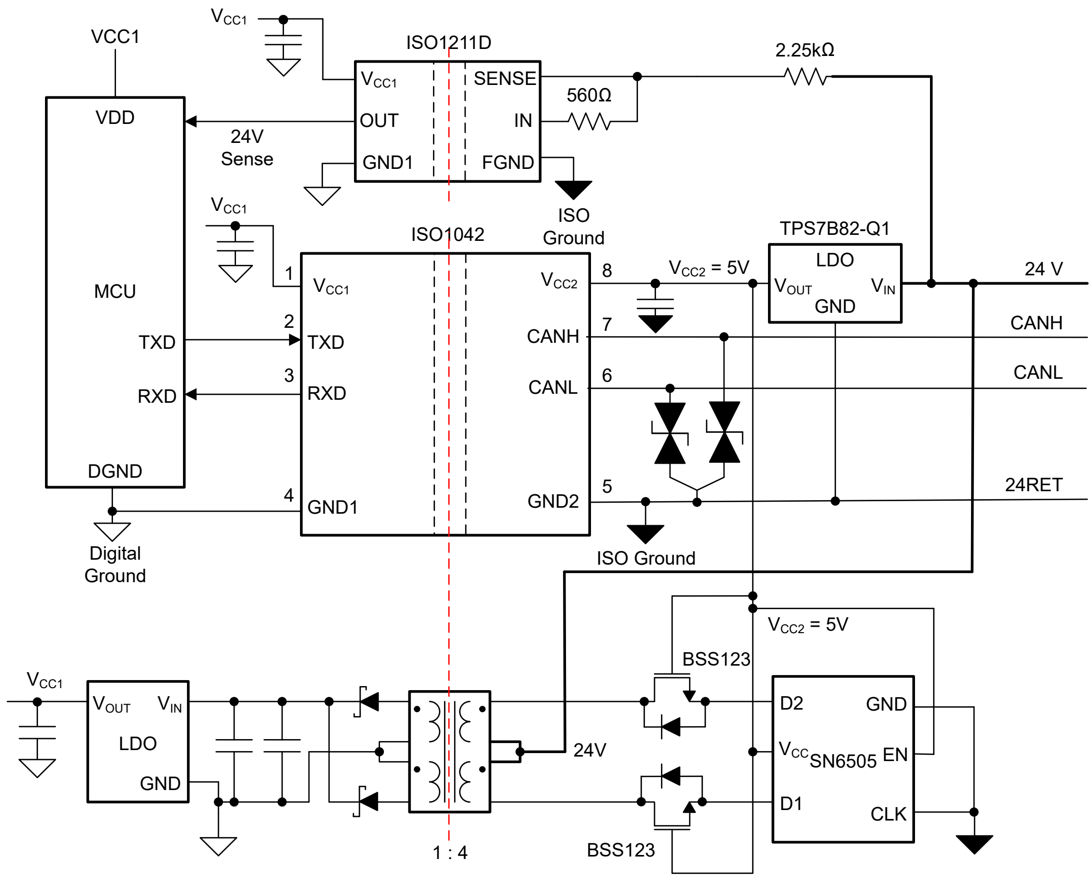


Figure 8-8. ISO1042, ISO1211 and SN6505 Used in a DeviceNet Application

Figure 8-8 shows an application circuit for using ISO1042, ISO1211 and SN6505 in a DeviceNet application. ISO1042 is used to isolate the CAN interface. The ISO1211 24V digital input receiver is used to detect the absence or presence of the 24V field supply. The SN6505 push-pull transformer driver, is used to create an auxiliary isolated power supply for the microcontroller side using the 24V field supply.

8.4 Power Supply Recommendations

To make sure operation is reliable at all data rates and supply voltages, a 0.1µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. In addition, a bulk capacitance, typically 4.7µF, must be placed near the V_{CC2} supply pin. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6505B. For such applications, detailed power supply design, and transformer selection recommendations are available in the *SN6505 Low-Noise 1A Transformer Drivers for Isolated Power Supplies datasheet*.

8.5 Layout

8.5.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Recommended Layer Stack). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

Suggested placement and routing of ISO1042 bypass capacitors and optional TVS diodes is shown in Figure 8-10 and Figure 8-11. In particular, place the V_{CC2} bypass capacitors on the top layer, as close to the device pins as possible, and complete the connection to the V_{CC2} and G_{ND2} pins without using vias. Note that the SOIC-16 variant needs two V_{CC2} bypass capacitor, one on each V_{CC2} pin.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

8.5.1.1 PCB Material

For digital circuit boards operating at less than 150Mbps, (or rise and fall times greater than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.5.2 Layout Example

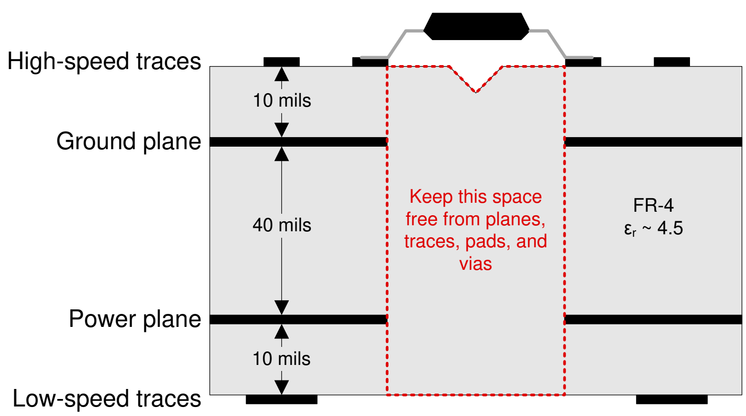


Figure 8-9. Recommended Layer Stack

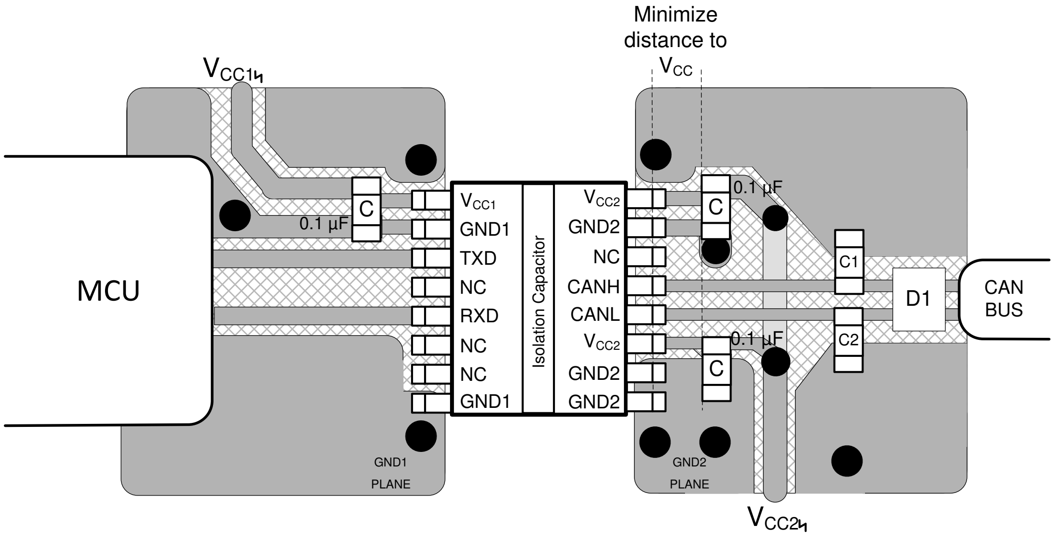


Figure 8-10. 16-DW Layout Example

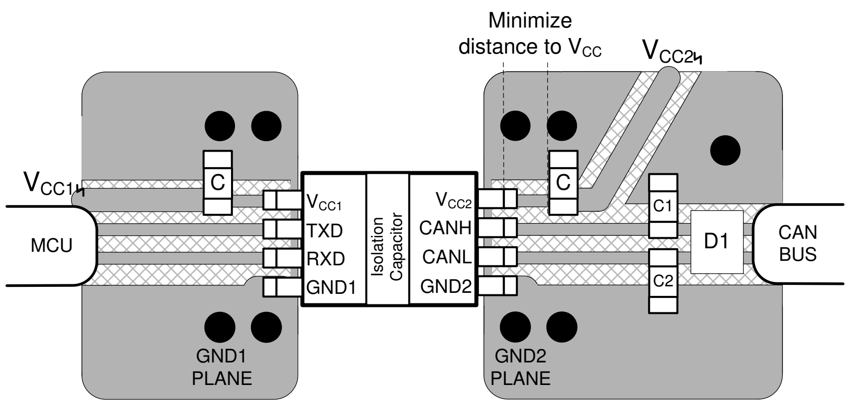


Figure 8-11. 8-DWV Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *ISO1042DW Isolated CAN Transceiver Evaluation Module* User's Guide
- Texas Instruments, *Isolate your CAN systems without compromising on performance or space* application brief
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *High-voltage reinforced isolation: Definitions and test methodologies* marketing white paper
- Texas Instruments, *How to Isolate Signal and Power in Isolated CAN Systems* application brief
- Texas Instruments, *How to Design Isolated CAN Systems With Correct Bus Protection* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2019) to Revision F (August 2026)	Page
• Updated the device certification information throughout the document	1
• Updated the maximum isolation working voltage from 1500 to 2121V_{DC} in the *Insulation Specifications* section	7
• Updated the test conditions of V_{IOSM} in the *Insulation Specifications* section	7
• Updated q_{pd} method b1 test conditions in the *Insulation Specifications* section	7
• Updated the ISO1042 maximum surge isolation voltage from 6250 to 10000V_{PK} the *Insulation Specifications* section	7

- Updated the ISO1042B maximum surge isolation voltage from 4615 to 6000V_{PK} the *Insulation Specifications* section........ 7
- Updated the certificate information throughout the *Safety-Related Certifications* section........ 8
- Added the *Insulation Lifetime* section and *Insulation Lifetime Projection Data* graph........ 26

Changes from Revision D (October 2018) to Revision E (October 2019) **Page**

- Changed new safety certification........ 1

Changes from Revision C (September 2018) to Revision D (October 2018) **Page**

- Added ISO1042-Q1 link........ 1

Changes from Revision B (July 2018) to Revision C (September 2018) **Page**

- Initial Release........ 1

Changes from Revision A (May 2018) to Revision B (July 2018) **Page**

- Increased the size of the GND2 plane and changed the NC pin to GND2 in the *16-DW Layout Example*........ 29

Changes from Revision * (December 2017) to Revision A (May 2018) **Page**

- Changed pin 10 from NC to GND2........ 2

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO1042BDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042BDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042BDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042BDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042BDWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042BDWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042BDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042BDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042B
ISO1042DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWVRG4	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042
ISO1042DWVRG4.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO1042

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

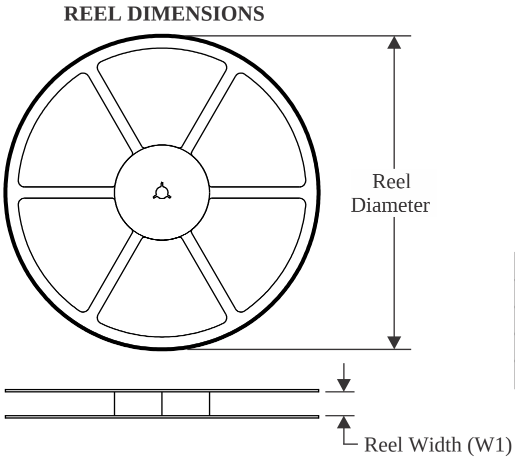
OTHER QUALIFIED VERSIONS OF ISO1042 :

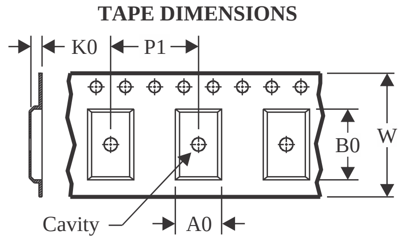
- Automotive : ISO1042-Q1

NOTE: Qualified Version Definitions:

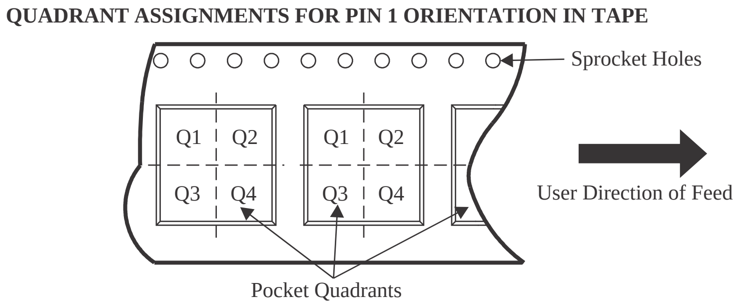
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





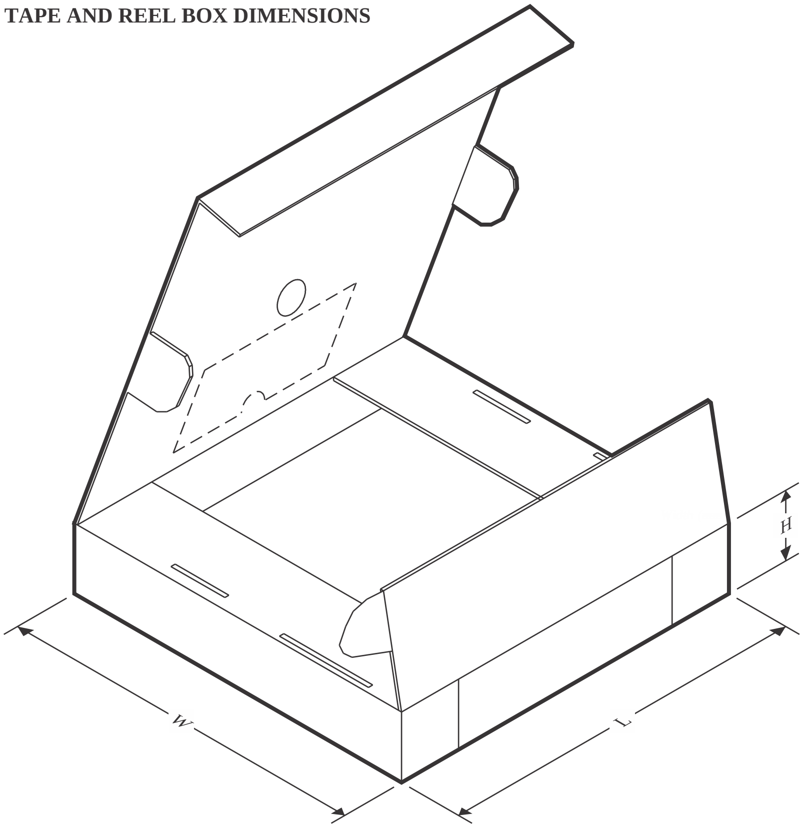
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1042BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1042BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO1042DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1042DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO1042DWVRG4	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

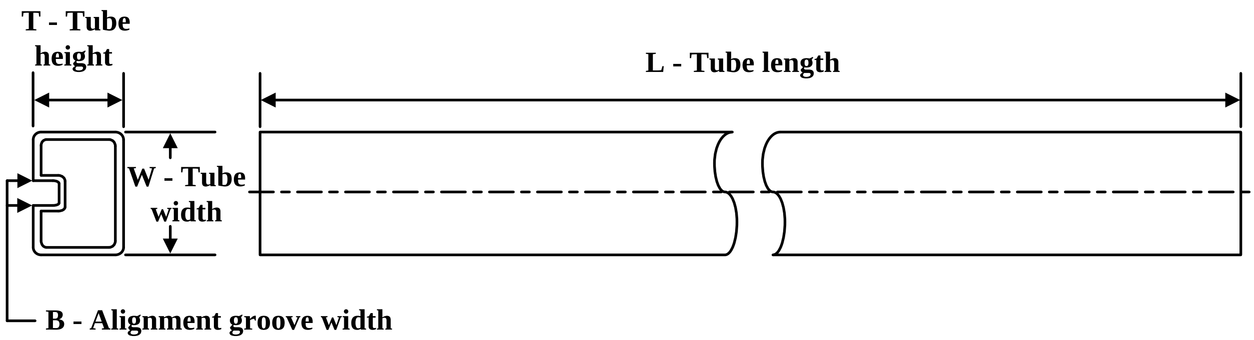
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1042BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1042BDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO1042DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO1042DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO1042DWVRG4	SOIC	DWV	8	1000	350.0	350.0	43.0

TUBE



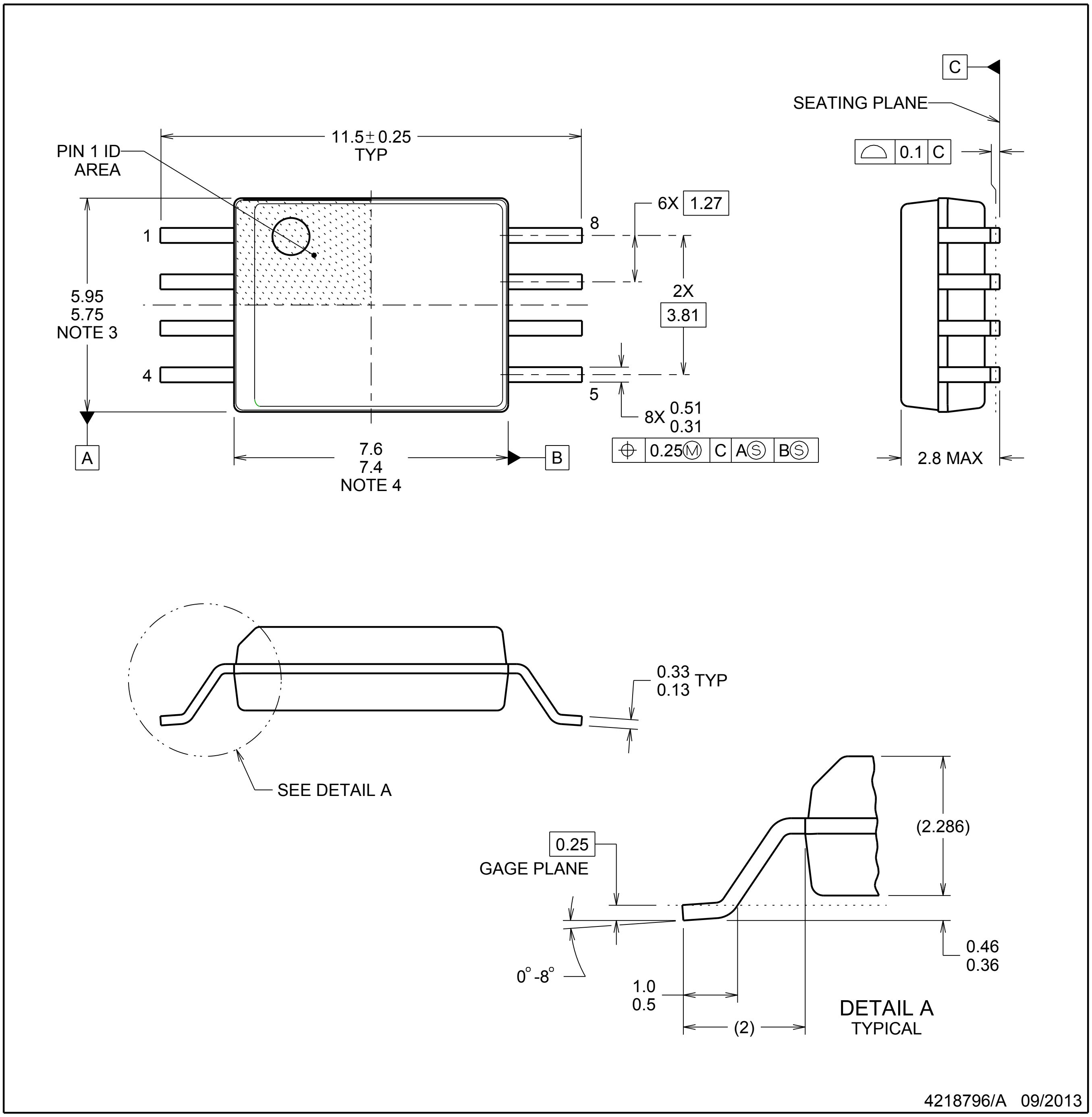
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO1042BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1042BDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1042BDWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
ISO1042BDWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
ISO1042DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1042DW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1042DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
ISO1042DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6

DWV0008A

SOIC - 2.8 mm max height

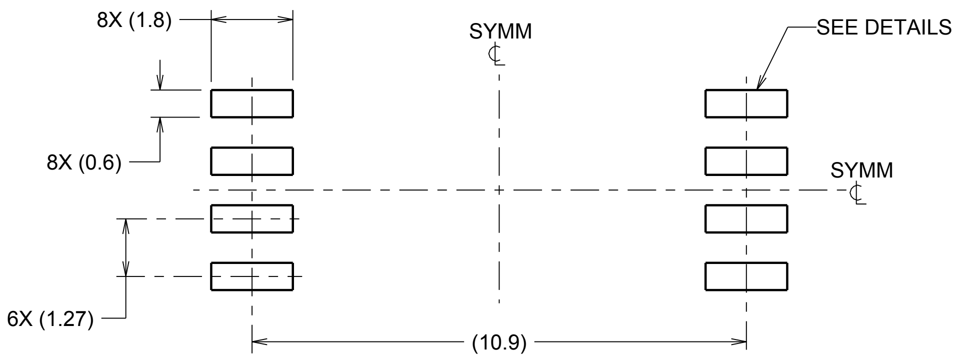
SOIC



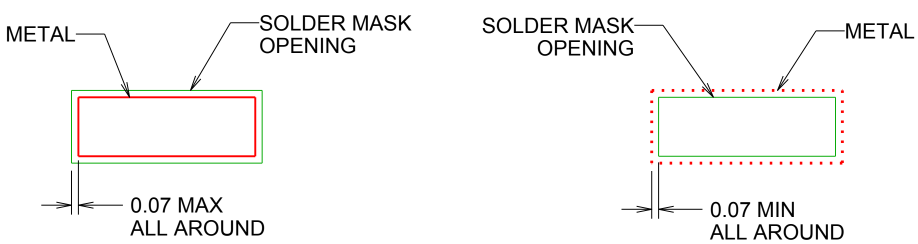
4218796/A 09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



NON SOLDER MASK DEFINED

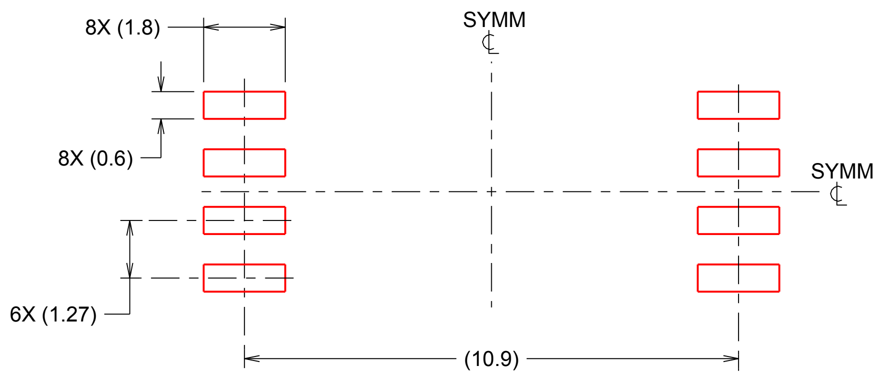
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.