ISO604x Low Power and Low Propagation Delay, Reinforced, 4-Channel Digital Isolator With 0.635mA / ch, 200Mbps, 9ns t_{PD} , 7ps (RMS) jitter and 1.8V Logic Support

1 Features

- Functional Safety-Capable (Planned)
  - Documentation available to aid IEC 61508 system design
- Supports High Bandwidth and Clock Sensitive Applications
  - Up to 200Mbps data rate
  - Low Propagation Delay: 9ns maximum at 5V, 10ns maximum at 3.3V
  - SPI up to: 27.75MHz at 5V, 25MHz at 3.3V
  - Low Pulse Width Distortion: 1.2ns maximum at 5V, 1.2ns maximum at 3.3V
  - Low Jitter: 7ps (RMS) typical supports low impact to ADC and DAC SNR for the sample clock signal
  - Low Channel to Channel Skew: 1.2ns maximum at 5V, 1.2ns maximum at 3.3V
  - Low Part to Part Skew: 3ns maximum at 5V, 3ns maximum at 3.3V
- Supports High Channel Density Applications:
  - Low Power: 0.635mA maximum per channel at 1Mbps and 3.3V
  - Small Footprint Packages: SSOP (DBQ-16) , Wide-SSOP (DFP-16)
- Robust SiO_2 isolation barrier:
  - High lifetime at up to 1061V_{RMS} and 1500V_{DC} working voltage
  - Wide temperature range: –40°C to 125°C
  - Up to 5000V_{RMS} isolation rating
  - Up to 10.4kV surge capability
  - Up to ±175kV/µs typical CMTI
- Supply range: 1.71V to 5.5V
- Overvoltage tolerant inputs
- Default output *high* (ISO604xH) and *low* (ISO604xL) options
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Safety-Related Certifications (Planned):
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 and CSA CAS Notice No. 5A
  - IEC 62368-1, IEC 61010-1 and GB 4943.1 certifications

2 Applications

- Test and Measurement
- Data Acquisition
- Factory Automation
- Medical and Healthcare

3 Description

The ISO604x devices are high performance digital isolators. The devices are certified by VDE, UL, TUV, and CQC. See the Safety-Related Certifications section for details.

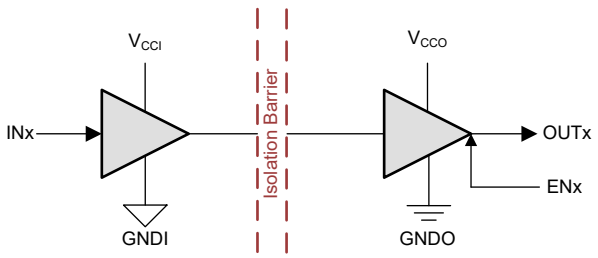
The ISO604x devices provide high data rates at very low supply current with low propagation delay, low jitter and low channel to channel and part to part skew while isolating CMOS or LVCMOS digital I/Os. These devices come with enable pins that can be used to put the respective outputs in high impedance.

Devices in the family have channel configurations for specific numbers of forward and reverse directions across the isolation barrier, default output levels, and packaging. See the Device Comparison section for details on the device configurations. Four channel devices accommodate four channel designs, including SPI, RS-485, and digital I/O applications. Multiple four channel devices or combinations with two and six channel devices can be used to transmit any number of parallel I/O, SPI chip selects, status or fault signals required by the application.

Package Information

PART NUMBER(1) (3)	PACKAGE	PACKAGE SIZE(2)
ISO604xH , ISO604xL	Wide-SOIC (DW-16) (3)	10.3mm × 10.3mm
ISO604xH , ISO604xL	Wide-SSOP (DFP-16) (3)	10.3mm × 4.6mm
ISO604xH , ISO604xL	SSOP (DBQ-16) (3)	6mm x 4.9mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Please refer to Device Comparison and Packaging Information table on the Package Option Addendum page in the Mechanical, Packaging, and Orderable Information section for device details and Production or Preproduction status for specific device and package.



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground

Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Device Comparison

Table 4-1. Device Comparison Table

DEVICE NAME	TOTAL CHANNELS	REVERSE CHANNELS	DEFAULT OUTPUT	PACKAGE	CREEPAGE & CLEARANCE	VDE RATING	UL V_{ISO}
ISO6040HDWR	4	0	HIGH	Wide-SOIC (DW-16)	>8.15mm	Reinforced	5000V_{RMS}
ISO6040LDWR			LOW				
ISO6041HDWR		1	HIGH				
ISO6041LDWR			LOW				
ISO6042HDWR		2	HIGH				
ISO6042LDWR			LOW				
ISO6040HDFPR	4	0	HIGH	Wide-SSOP (DFP-16)	>8mm	Reinforced	5000V_{RMS}
ISO6040LDFPR			LOW				
ISO6041HDFPR		1	HIGH				
ISO6041LDFPR			LOW				
ISO6042HDFPR		2	HIGH				
ISO6042LDFPR			LOW				
ISO6040HDBQR	4	0	HIGH	SSOP (DBQ-16)	>3.7mm	Reinforced	3000V_{RMS}
ISO6040LDBQR			LOW				
ISO6041HDBQR		1	HIGH				
ISO6041LDBQR			LOW				
ISO6042HDBQR		2	HIGH				
ISO6042LDBQR			LOW				

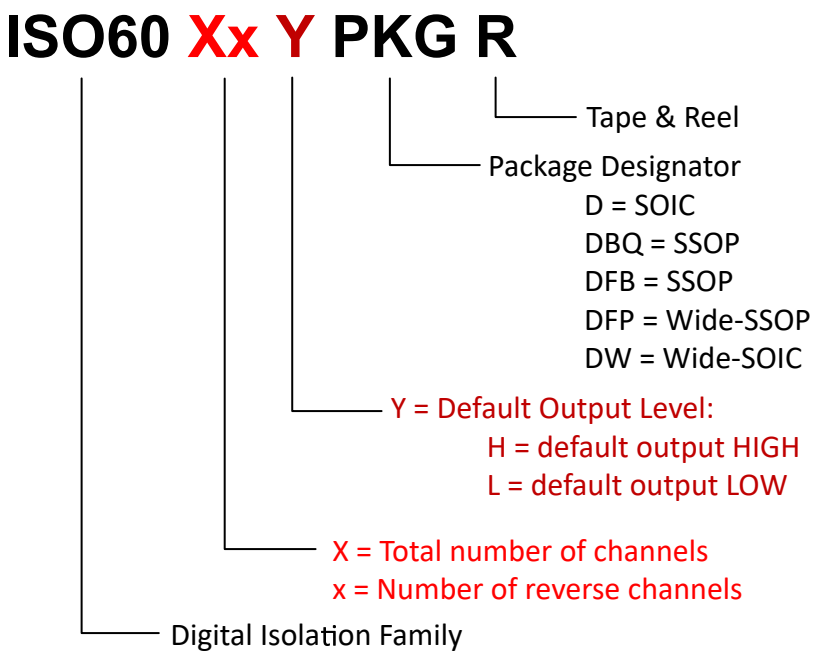

Figure 4-1. Device Nomenclature

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5 Pin Configuration and Functions

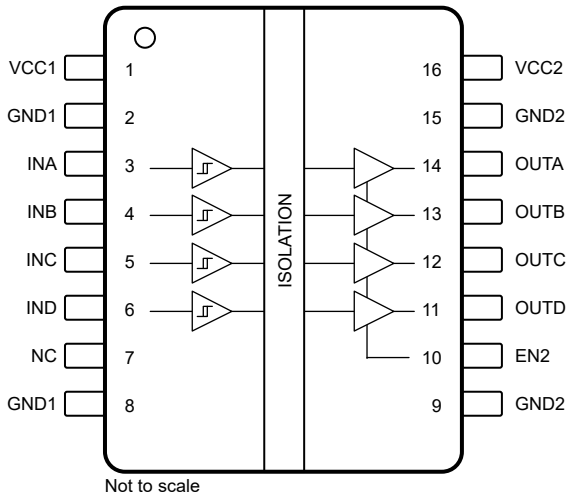

Figure 5-1. ISO6040H and ISO6040L Top View

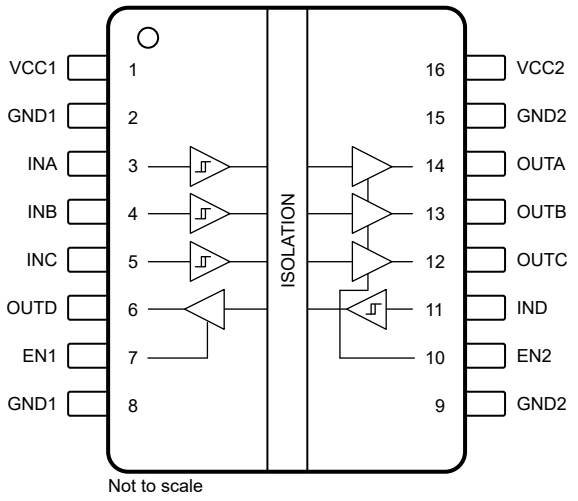

Figure 5-2. ISO6041H and ISO6041L Top View

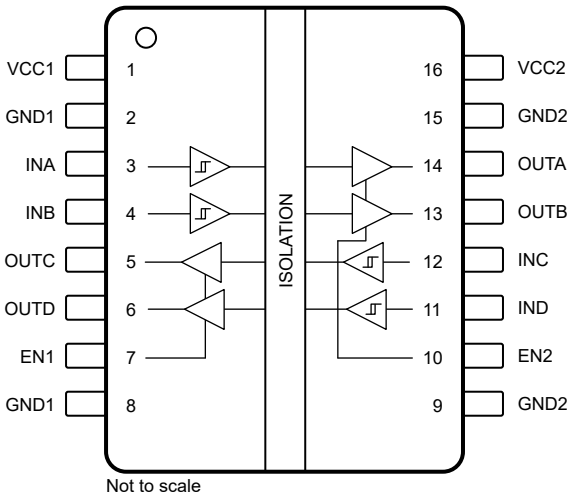

Figure 5-3. ISO6042H and ISO6042L Top View

Table 5-1. Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	ISO6041H , ISO6041L		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2,8	—	Ground connection for V_{CC1}, connect both pins to Ground 1 through a low impedance ground plane or connection.
GND2	9,15	—	Ground connection for V_{CC2}, connect both pins to Ground 2 through a low impedance ground plane or connection.
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D

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Table 5-1. Pin Functions (continued)

PIN		Type[1]	DESCRIPTION
NAME	ISO6041H , ISO6041L		
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Digital Input Voltage	INx to GNDx	-0.5	6	V
Digital Input Voltage	ENx to GNDx	-0.5	6	V
Digital Output Voltage	OUTx to GNDx	-0.5	V_{CCX} + 0.5 (3)	V
Digital Output current	I_O	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC_RO} (1)	Supply Voltage Side 1 and Side 2 (Recommended Operating Range)	V_{CC1} = 1.8V to 5V (3)	1.71		5.5	V
V_{CC_UVLO+}	V_{CC} UVLO threshold when supply voltage is rising			1.52	1.70	V
V_{CC_UVLO-}	V_{CC} UVLO threshold when supply voltage is falling		1.2	1.41		
$V_{CC_UVLO_HYS}$	V_{CC} Supply voltage UVLO hysteresis		0.075	0.09		
$V_{IH(ENx)}$	Enable (ENx): High level input voltage		0.7 × V_{CCI} (2)		V_{CCI}	V
$V_{IL(ENx)}$	Enable (ENx): High level input voltage		0		0.3 × V_{CCI}	
$V_{IMAX(ENx)}$	Enable (ENx): maximum input voltage		0		5.5	
$V_{IH(INx)}$	Input (INx): High level input voltage		0.7 × V_{CCI} (2)		V_{CCI}	V
$V_{IL(INx)}$	Input (INx): Low level input voltage		0		0.3 × V_{CCI}	
$V_{IMAX(INx)}$	Input (INx): maximum input voltage		0		5.5	
I_{OH}	Output (OUTx): High level output current	V_{CCO} = 5V (2)	-4			mA
		V_{CCO} = 3.3V (2)	-2			
		V_{CCO} = 2.5V (2)	-1			
		V_{CCO} = 1.8V (2)	-1			
I_{OL}	Output (OUTx): Low level output current	V_{CCO} = 5V (2)			4	mA
		V_{CCO} = 3.3V (2)			2	
		V_{CCO} = 2.5V (2)			1	
		V_{CCO} = 1.8V (2)			1	
DR	Data Rate	2.25V ≤ V_{CCx} ≤ 5.5V and C_L≤15pF(4)	0		200	Mbps
		1.71V ≤ V_{CCx} < 2.25V and C_L≤10pF(4)	0		200	
		1.71V ≤ V_{CCx} < 2.25V and 10pF < C_L≤ 15pF(4)	0		150	
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(3) The channel outputs are in undetermined state when V_{CC_UVLO-} ≤ V_{CC1}, V_{CC2} < $V_{CC_RO(MIN)}$.
(4) See Section 7 .

6.4 Thermal Information

		THERMAL METRIC(1)						UNIT
PACKAGE	PINS	$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DW (Wide-SOIC)	16	71.8	35.2	37.6	17	37.1	NA	°C/W
DFP (Wide-SSOP)	16	97.2	49.1	60.0	21.3	58.7	NA	°C/W
DBQ (SSOP)	16	91.8	42.3	49.7	16.4	49.1	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6040d (d = H for default high and d = L for default low)						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 100MHz 50% duty cycle square wave			375	mW
P_{D1}	Maximum power dissipation (side-1)				93.3	mW
P_{D2}	Maximum power dissipation (side-2)				281.7	mW
ISO6041d (d = H for default high and d = L for default low)						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L =15pF, Input a 100MHz 50% duty cycle square wave			375	mW
P_{D1}	Maximum power dissipation (side-1)				141	mW
P_{D2}	Maximum power dissipation (side-2)				234	mW
ISO6042d (d = H for default high and d = L for default low)						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 100MHz 50% duty cycle square wave			384	mW
P_{D1}	Maximum power dissipation (side-1)				188	mW
P_{D2}	Maximum power dissipation (side-2)				186	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	PACKAGE			UNIT
			16-DW	16-DFP	16-DBQ	
IEC 60664-1						
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8.15	>8	>3.7	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	>8.15	>8	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17	>17	µm
CTI	Comparative tracking index	IEC 60112	> 600	> 600	> 600	V
	Material Group	According to IEC 60664-1	I	I	I	
	Overvoltage category	Rated mains voltage ≤ 150V_{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 300V_{RMS}	I-IV	I-IV	I-III	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	I-IV	n/a	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	I-III	n/a	
DIN EN IEC 60747-17 (VDE 0884-17)						
	Suitability	DIN EN IEC 60747-17 (VDE 0884-17) suitability(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	1500	707	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test.	1061	1061	500(7)	V_{RMS}
		DC voltage	1500	1500	707	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t= 1s (100% production)	7071	7071	4243	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	8000	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	V_{IOSM} ≥ 1.3 × V_{IMP}; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	10400	10400	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input-output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤5	≤5	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤5	≤5	≤ 5	
		Method b: At routine test (100% production); V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1MHz	≅1.7	≅1.8	≅1.85	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V, T_A = 25°C	>10^{12}	>10^{12}	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	>10^{11}	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	>10^9	>10^9	> 10^9	
	Pollution degree		2	2	2	
	Climatic category		40/125/21	40/125/21	40/125/21	
UL 1577						

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PARAMETER		TEST CONDITIONS	PACKAGE			UNIT
			16-DW	16-DFP	16-DBQ	
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This device is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.
(7) $1000V_{RMS}$ per IEC 60664-1 for pollution degree 1, basic isolation use cases. For reinforced isolation use cases the working voltage is package limited to $500V_{RMS}$ for pollution degree 1. Please refer to IEC 60664-1 or relevant standard for other use cases and pollution degrees.

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6.7 Safety-Related Certifications

VDE	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to UL 1577 and CSA CAS Notice No. 5A	Plan to certify according to GB4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 (Wide-SOIC) Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 71.8°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			316.5	mA
		$R_{\theta JA}$ = 71.8°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			483.6	
		$R_{\theta JA}$ = 71.8°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			633.1	
		$R_{\theta JA}$ = 71.8°C/W, V_I = 1.89V, T_J = 150°C, T_A = 25°C			921.1	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 71.8°C/W, T_J = 150°C, T_A = 25°C			1740.9	mW
T_S	Maximum safety temperature				150	°C
DFP-16 (Wide-SSOP) Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 97.2°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			233.8	mA
I_S		$R_{\theta JA}$ = 97.2°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			357.2	
I_S		$R_{\theta JA}$ = 97.2°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			467.6	
I_S		$R_{\theta JA}$ = 97.2°C/W, V_I = 1.89V, T_J = 150°C, T_A = 25°C			680.4	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 97.2°C/W, T_J = 150°C, T_A = 25°C			1286.0	mW
T_S	Maximum safety temperature				150	°C
DBQ-16 (SSOP) Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 91.8°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			247.6	mA
I_S		$R_{\theta JA}$ = 91.8°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			378.2	
I_S		$R_{\theta JA}$ = 91.8°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			495.1	
I_S		$R_{\theta JA}$ = 91.8°C/W, V_I = 1.89V, T_J = 150°C, T_A = 25°C			720.5	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 91.8°C/W, T_J = 150°C, T_A = 25°C			1361.7	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics-5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -4mA; See Section 7	V_{CCO} - 0.4 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 4mA; See Section 7			0.4	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.02 × V_{CCI}	0.07 × V_{CCI}		V
$I_{I(INx)}$	INx (input) input current (default high device, with H suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage and current through default high pull-up resistance)	-10			
	INx (input) input current (default low device, with L suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage and current through default low pull-down resistance)			10	
		LOW Input Current: V_{IL} = 0V at INx (leakage current)	-1			
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.02 × V_{CCI}	0.04 × V_{CCI}		V
$I_{I(ENx)}$	ENx (enable) input current (integrated pull-up)	HIGH Input Current: V_{IH} = V_{CCI} (1) at ENx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at ENx (leakage and current through default high pull-up resistance)	-10			
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V, V_{ENx} = V_{CC} ; See Section 7	100	175		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 5V		1.5		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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6.10 Supply Current Characteristics-5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6040d ISO60P40d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high device, H); V_I = 0V (default low device, L)		I_{CC1}			1.06	mA
			I_{CC2}			1.53	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}			1.06	
			I_{CC2}			1.53	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			1.06	
			I_{CC2}			1.53	
		10Mbps	I_{CC1}			2.10	
			I_{CC2}			2.96	
		25Mbps	I_{CC1}			3.66	
			I_{CC2}			5.10	
		100Mbps	I_{CC1}			11.46	
			I_{CC2}			15.79	
ISO6041d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}		0.88	1.25	mA
			I_{CC2}		1	1.40	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}		0.89	1.25	
			I_{CC2}		1	1.40	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}		0.93	1.25	
			I_{CC2}		1	1.40	
		10Mbps	I_{CC1}		1.6	2.00	
			I_{CC2}		1.7	2.16	
		25Mbps	I_{CC1}		2.6	3.25	
			I_{CC2}		2.8	3.44	
		100Mbps	I_{CC1}		7.8	9.40	
			I_{CC2}		8.1	9.95	
ISO6042d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}			1.22	mA
			I_{CC2}			1.20	
	V_I = 0V (default high device, H); V_I = V_{CC1} ((default low device, L)		I_{CC1}			1.22	
			I_{CC2}			1.20	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			1.22	
			I_{CC2}			1.20	
		10Mbps	I_{CC1}			2.45	
			I_{CC2}			2.43	
		25Mbps	I_{CC1}			4.30	
			I_{CC2}			4.28	
		100Mbps	I_{CC1}			13.55	
			I_{CC2}			13.53	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

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6.11 Electrical Characteristics-3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -2mA; See Section 7	V_{CCO} - 0.2 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 2mA; See Section 7			0.2	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.02 × V_{CCI}	0.07 × V_{CCI}		V
$I_{I(INx)}$	INx (input) input current (default high device, with H suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage and current through default high pull-up resistance)	-10			
	INx (input) input current (default low device, with L suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage and current through default low pull-down resistance)			10	
		LOW Input Current: V_{IL} = 0V at INx (leakage current)	-1			
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.02 × V_{CCI}	0.04 × V_{CCI}		V
$I_{I(ENx)}$	ENx (enable) input current (integrated pull-up)	HIGH Input Current: V_{IH} = V_{CCI} (1) at ENx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at ENx (leakage and current through default high pull-up resistance)	-10			
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V, V_{ENx} = V_{CC} ; See Section 7	100	175		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 3.3V		1.6		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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6.12 Supply Current Characteristics-3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6040d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high device, H); V_I = 0V (default low device, L)		I_{CC1}			1.00	mA
			I_{CC2}			1.48	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}			1.00	
			I_{CC2}			1.48	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			1.00	
			I_{CC2}			1.48	
		10Mbps	I_{CC1}			1.94	
			I_{CC2}			2.47	
		25Mbps	I_{CC1}			3.34	
			I_{CC2}			3.95	
		100Mbps	I_{CC1}			10.36	
			I_{CC2}			11.37	
ISO6041d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}	0.85		1.20	mA
			I_{CC2}	0.97		1.34	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}	0.85		1.20	
			I_{CC2}	0.97		1.34	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}	0.9		1.20	
			I_{CC2}	1		1.34	
		10Mbps	I_{CC1}	1.4		1.83	
			I_{CC2}	1.5		1.90	
		25Mbps	I_{CC1}	2.4		2.91	
			I_{CC2}	2.3		2.86	
		100Mbps	I_{CC1}	6.8		8.27	
			I_{CC2}	6.4		7.81	
ISO6042d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}			1.16	mA
			I_{CC2}			1.14	
	V_I = 0V (default high device, H); V_I = V_{CC1} ((default low device, L)		I_{CC1}			1.16	
			I_{CC2}			1.14	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			1.16	
			I_{CC2}			1.14	
		10Mbps	I_{CC1}			2.12	
			I_{CC2}			2.11	
		25Mbps	I_{CC1}			3.57	
			I_{CC2}			3.55	
		100Mbps	I_{CC1}			10.79	
			I_{CC2}			10.77	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

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6.13 Electrical Characteristics-2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -1mA; See Section 7	V_{CCO} - 0.1 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 1mA; See Section 7			0.1	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.02 × V_{CCI}	0.07 × V_{CCI}		V
$I_{I(INx)}$	INx (input) input current (default high device, with H suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage and current through default high pull-up resistance)	-10			
	INx (input) input current (default low device, with L suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage and current through default low pull-down resistance)			10	
		LOW Input Current: V_{IL} = 0V at INx (leakage current)	-1			
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.02 × V_{CCI}	0.04 × V_{CCI}		V
$I_{I(ENx)}$	ENx (enable) input current (integrated pull-up)	HIGH Input Current: V_{IH} = V_{CCI} (1) at ENx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at ENx (leakage and current through default high pull-up resistance)	-10			
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V, V_{ENx} = V_{CC} ; See Section 7	100	175		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 2.5V		1.7		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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6.14 Supply Current Characteristics-2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6040d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high device, H); V_I = 0V (default low device, L)		I_{CC1}			0.98	mA
			I_{CC2}			1.45	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}			0.98	
			I_{CC2}			1.45	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			0.98	
			I_{CC2}			1.45	
		10Mbps	I_{CC1}			1.86	
			I_{CC2}			2.24	
		25Mbps	I_{CC1}			3.18	
			I_{CC2}			3.42	
		100Mbps	I_{CC1}			9.77	
			I_{CC2}			9.31	
ISO6041d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}	0.85		1.17	mA
			I_{CC2}	0.95		1.32	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}	0.85		1.17	
			I_{CC2}	0.95		1.32	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}	0.88		1.17	
			I_{CC2}	1		1.32	
		10Mbps	I_{CC1}	1.4		1.75	
			I_{CC2}	1.4		1.74	
		25Mbps	I_{CC1}	2.2		2.74	
			I_{CC2}	2		2.56	
		100Mbps	I_{CC1}	6.4		7.76	
			I_{CC2}	5.3		6.64	
ISO6042d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}			1.14	mA
			I_{CC2}			1.12	
	V_I = 0V (default high device, H); V_I = V_{CC1} ((default low device, L)		I_{CC1}			1.14	
			I_{CC2}			1.12	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			1.14	
			I_{CC2}			1.12	
		10Mbps	I_{CC1}			1.97	
			I_{CC2}			1.95	
		25Mbps	I_{CC1}			3.22	
			I_{CC2}			3.20	
		100Mbps	I_{CC1}			9.46	
			I_{CC2}			9.45	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

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6.15 Electrical Characteristics-1.8V Supply

V_{CC1} = V_{CC2} = 1.8V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -1mA; See Section 7	V_{CCO} - 0.1 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 1mA; See Section 7			0.1	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.02 × V_{CCI}	0.07 × V_{CCI}		V
$I_{I(INx)}$	INx (input) input current (default high device, with H suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage and current through default high pull-up resistance)	-10			
	INx (input) input current (default low device, with L suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage and current through default low pull-down resistance)			10	
		LOW Input Current: V_{IL} = 0V at INx (leakage current)	-1			
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 × V_{CCI}			V
$V_{I_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.02 × V_{CCI}	0.07 × V_{CCI}		V
$I_{I(ENx)}$	ENx (enable) input current (integrated pull-up)	HIGH Input Current: V_{IH} = V_{CCI} (1) at ENx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at ENx (leakage and current through default high pull-up resistance)	-10			
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V, V_{ENx} = V_{CC} ; See Section 7	75	175		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 2.5V		1.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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6.16 Supply Current Characteristics-1.8V Supply

V_{CC1} = V_{CC2} = 1.8V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6040d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high device, H); V_I = 0V (default low device, L)		I_{CC1}			0.97	mA
			I_{CC2}			1.44	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}			0.97	
			I_{CC2}			1.44	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			0.97	
			I_{CC2}			1.44	
		10Mbps	I_{CC1}			1.77	
			I_{CC2}			2.01	
		25Mbps	I_{CC1}			2.97	
			I_{CC2}			2.86	
		100Mbps	I_{CC1}			9.00	
			I_{CC2}			7.13	
ISO6041d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}	0.83		1.16	mA
			I_{CC2}	0.94		1.30	
	V_I = 0V (default high device, H); V_I = V_{CC1} (default low device, L)		I_{CC1}	0.83		1.16	
			I_{CC2}	0.93		1.30	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}	0.86		1.16	
			I_{CC2}	0.97		1.30	
		10Mbps	I_{CC1}	1.3		1.69	
			I_{CC2}	1.3		1.64	
		25Mbps	I_{CC1}	2.1		2.62	
			I_{CC2}	1.9		2.28	
		100Mbps	I_{CC1}	6.2		7.30	
			I_{CC2}	4.6		5.50	
ISO6042d (d = H for default high and d = L for default low)							
Supply current - DC signal (2)	V_I = V_{CC1} (1) (default high device, H); V_I = 0V (default low device, L)		I_{CC1}			1.13	mA
			I_{CC2}			1.11	
	V_I = 0V (default high device, H); V_I = V_{CC1} ((default low device, L)		I_{CC1}			1.13	
			I_{CC2}			1.11	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 0pF	1Mbps	I_{CC1}			1.13	
			I_{CC2}			1.11	
		10Mbps	I_{CC1}			1.81	
			I_{CC2}			1.80	
		25Mbps	I_{CC1}			2.84	
			I_{CC2}			2.82	
		100Mbps	I_{CC1}			7.99	
			I_{CC2}			7.97	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

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6.17 Switching Characteristics-5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 7			9	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1.2	
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.2	
		Opposite-direction channels			1.2	
$t_{sk(pp)}$	Part-to-part skew time(3)				3	
t_r	Output signal rise time	See Section 7			3.5	
t_f	Output signal fall time				3.5	
t_{PHZ}	Disable propagation delay, high-to-high impedance output				13.5	
t_{PLZ}	Disable propagation delay, low-to-high impedance output				13.5	
t_{PZH}	Enable propagation delay, high impedance-to-high output for device versions with Enable (EN)	See Section 7			11	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for device versions with Enable (EN)				12	
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			90	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC_UVLO-(MIN)}$. See Section 7			20	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 200Mbps, C_L as defined in Recommended Operating Conditions, one channel switching		130		ps
$t_{JCLK(RMS)}$	Clock Jitter (RMS)	10MHz clock input, rising/falling edges, C_L as defined in Recommended Operating Conditions, one channel switching		7		ps

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.18 Switching Characteristics-3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 7			10	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1.2	
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.2	
		Opposite-direction channels			1.2	
$t_{sk(pp)}$	Part-to-part skew time(3)				3	
t_r	Output signal rise time	See Section 7			4	
t_f	Output signal fall time				4	
t_{PHZ}	Disable propagation delay, high-to-high impedance output				20	
t_{PLZ}	Disable propagation delay, low-to-high impedance output				20	
t_{PZH}	Enable propagation delay, high impedance-to-high output for device versions with Enable (EN)	See Section 7			17	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for device versions with Enable (EN)				18	
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			70	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC_UVLO-(MIN)}$. See Section 7			20	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 200Mbps, C_L as defined in Recommended Operating Conditions, one channel switching		115		ps
$t_{JCLK(RMS)}$	Clock Jitter (RMS)	10MHz clock input, rising/falling edges, C_L as defined in Recommended Operating Conditions, one channel switching		7		ps

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.19 Switching Characteristics-2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 7			13.1	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1.2	
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.2	
		Opposite-direction channels			1.2	
$t_{sk(pp)}$	Part-to-part skew time(3)				3	
t_r	Output signal rise time	See Section 7			5	
t_f	Output signal fall time				5	
t_{PHZ}	Disable propagation delay, high-to-high impedance output				28	
t_{PLZ}	Disable propagation delay, low-to-high impedance output				28	
t_{PZH}	Enable propagation delay, high impedance-to-high output for device versions with Enable (EN)	See Section 7			25	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for device versions with Enable (EN)				26.5	
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			80	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC_UVLO-(MIN)}$. See Section 7			20	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 200Mbps, C_L as defined in Recommended Operating Conditions, one channel switching		125		ps
$t_{JCLK(RMS)}$	Clock Jitter (RMS)	10MHz clock input, rising/falling edges, C_L as defined in Recommended Operating Conditions, one channel switching		7		ps

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.20 Switching Characteristics-1.8V Supply

V_{CC1} = V_{CC2} = 1.8V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 7			14.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				1.2	
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.2	
		Opposite-direction channels			1.2	
$t_{sk(pp)}$	Part-to-part skew time(3)				5	
t_r	Output signal rise time	See Section 7			5	
t_f	Output signal fall time				5	
t_{PHZ}	Disable propagation delay, high-to-high impedance output				44	
t_{PLZ}	Disable propagation delay, low-to-high impedance output				44	
t_{PZH}	Enable propagation delay, high impedance-to-high output for device versions with Enable (EN)	See Section 7			41	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for device versions with Enable (EN)				44	
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			80	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC_UVLO-(MIN)}$. See Section 7			20	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 200Mbps, C_L as defined in Recommended Operating Conditions, one channel switching		195		ps
$t_{JCLK(RMS)}$	Clock Jitter (RMS)	10MHz clock input, rising/falling edges, C_L as defined in Recommended Operating Conditions, one channel switching		7		ps

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.21 Insulation Characteristics Curves

Insulation Characteristics Curves for Wide-SOIC (DW-16) Package

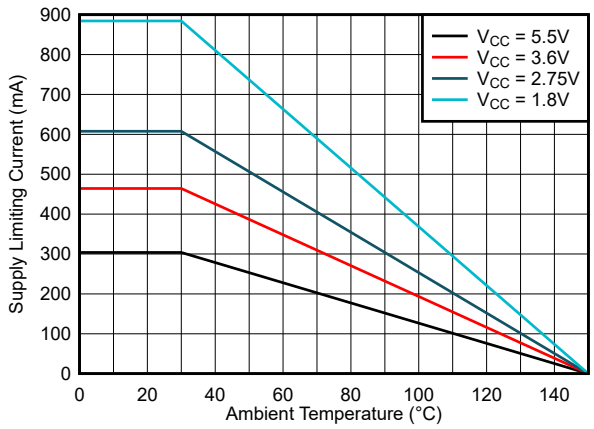

Figure 6-1. Thermal Derating Curve for Safety Limiting Current for Wide-SOIC (DW-16) Package

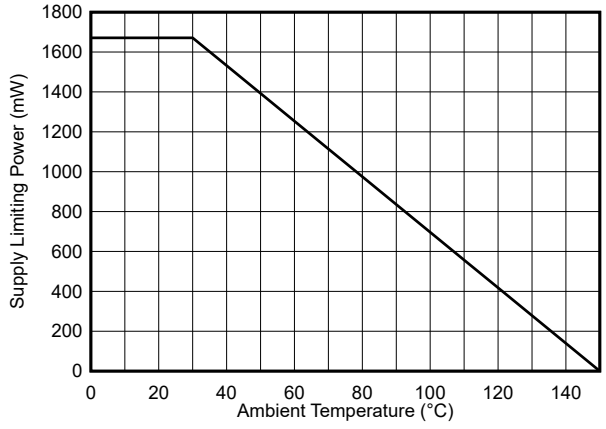

Figure 6-2. Thermal Derating Curve for Safety Limiting Power for Wide-SOIC (DW-16) Package

Insulation Characteristics Curves for Wide-SSOP (DFP-16) Package

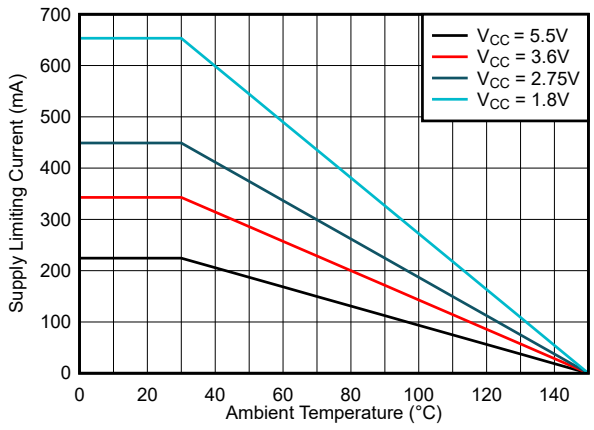

Figure 6-3. Thermal Derating Curve for Safety Limiting Current for Wide-SSOP (DFP-16) Package

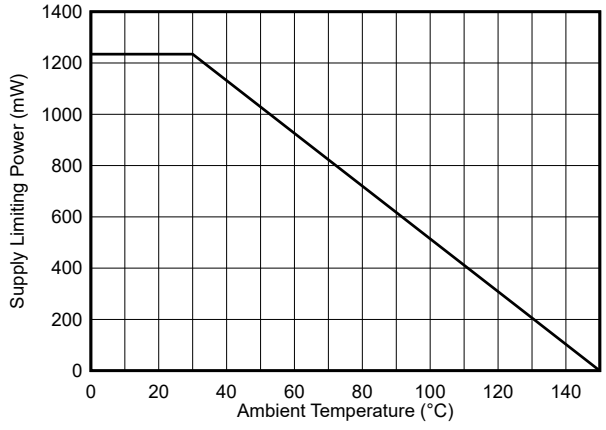

Figure 6-4. Thermal Derating Curve for Safety Limiting Power for Wide-SSOP (DFP-16) Package

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Insulation Characteristics Curves for SSOP (DBQ-16) Package

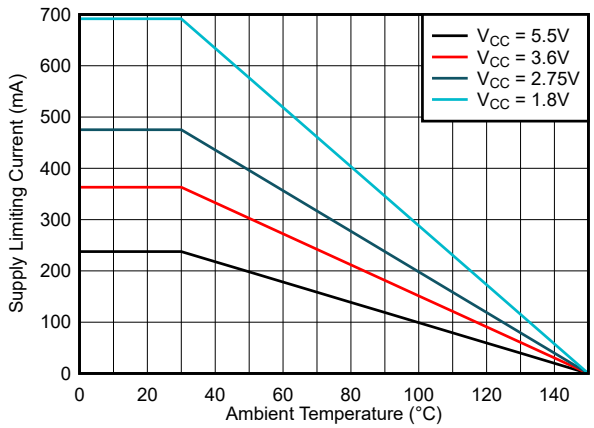

Figure 6-5. Thermal Derating Curve for Safety Limiting Current for SSOP (DBQ-16) Package

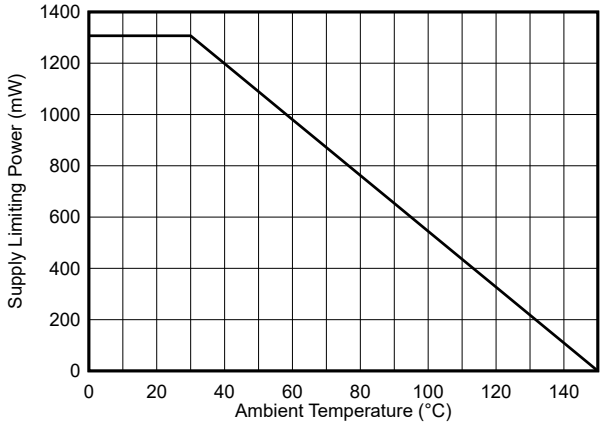

Figure 6-6. Thermal Derating Curve for Safety Limiting Power for SSOP (DBQ-16) Package

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6.22 Typical Characteristics

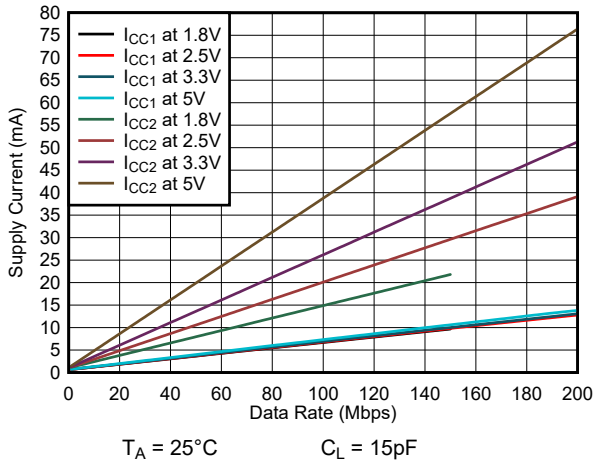

Figure 6-7. ISO6040H or ISO6040L Supply Current vs Data Rate (With 15pF Load)

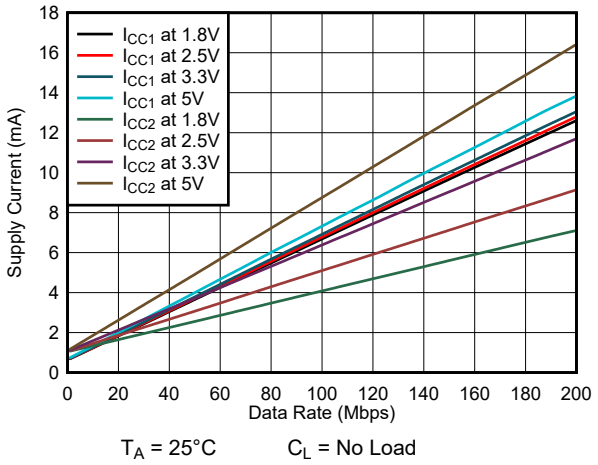

Figure 6-8. ISO6040H or ISO6040L Supply Current vs Data Rate (With No Load)

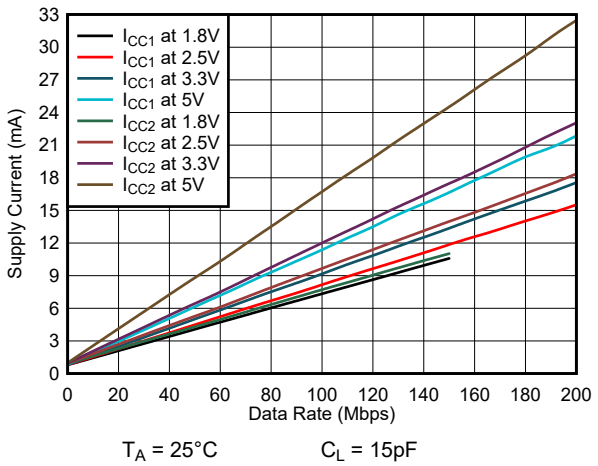

Figure 6-9. ISO6041H or ISO6041L Supply Current vs Data Rate (With 15pF Load)

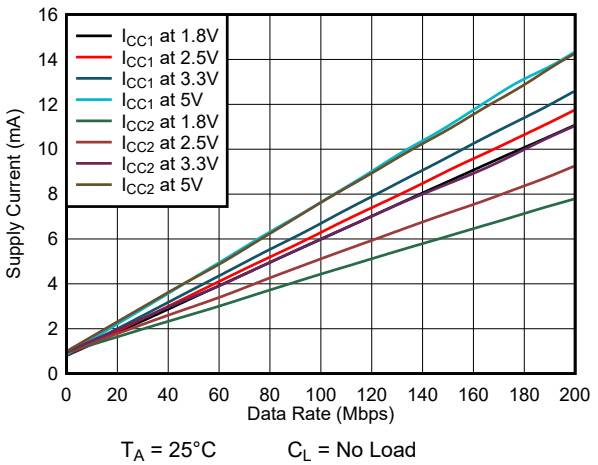

Figure 6-10. ISO6041H or ISO6041L Supply Current vs Data Rate (With No Load)

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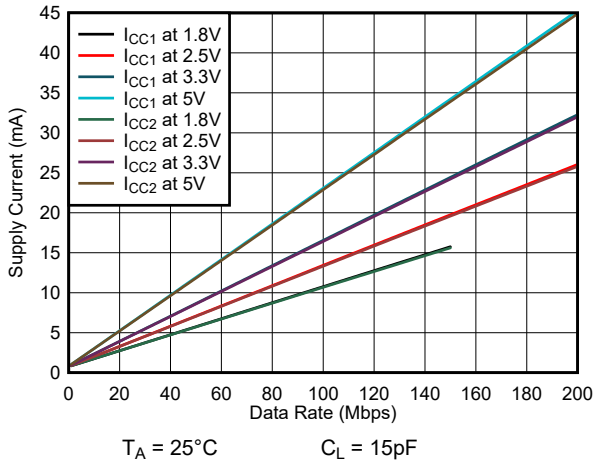


Figure 6-11. ISO6042H or ISO6042L Supply Current vs Data Rate (With 15pF Load)

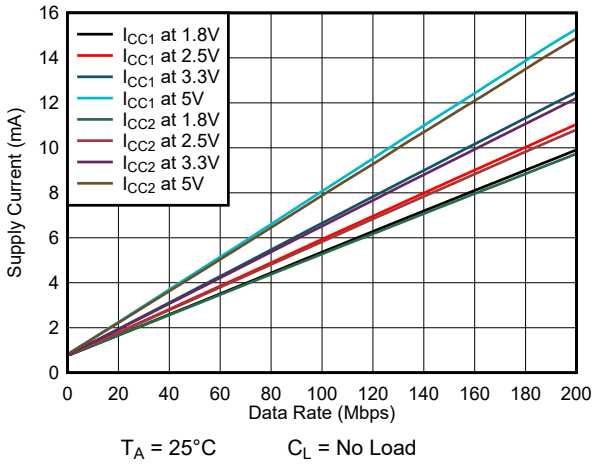


Figure 6-12. ISO6042H or ISO6042L Supply Current vs Data Rate (With No Load)

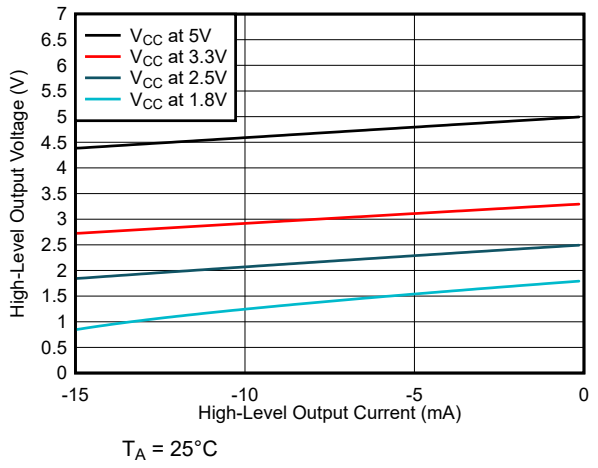


Figure 6-13. High-Level Output Voltage vs High-level Output Current

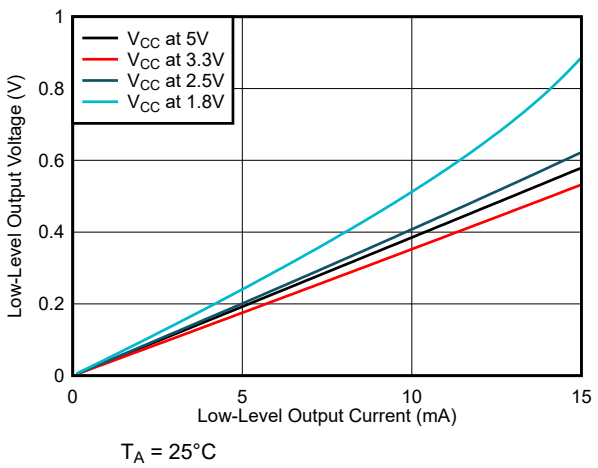


Figure 6-14. Low-Level Output Voltage vs Low-Level Output Current

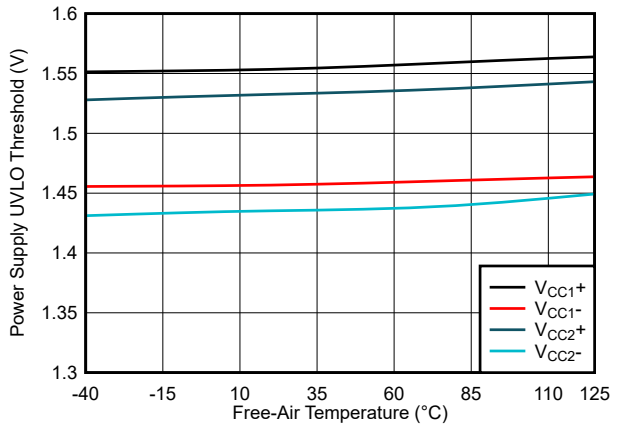


Figure 6-15. Power Supply Undervoltage Threshold vs Free-Air Temperature

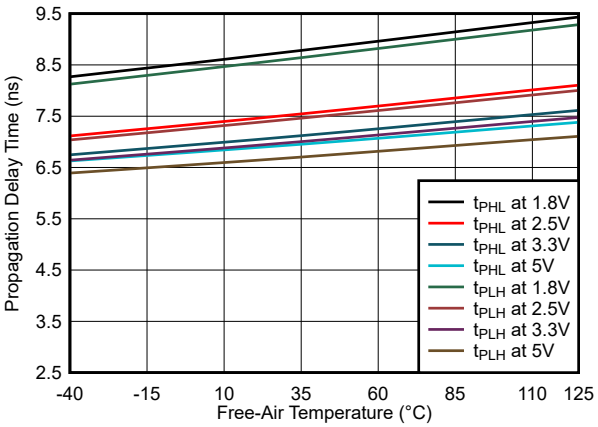
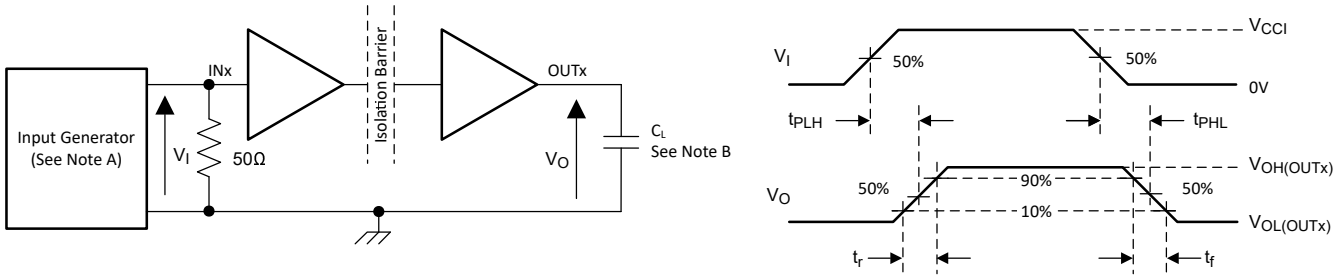


Figure 6-16. Propagation Delay Time vs Free-Air Temperature

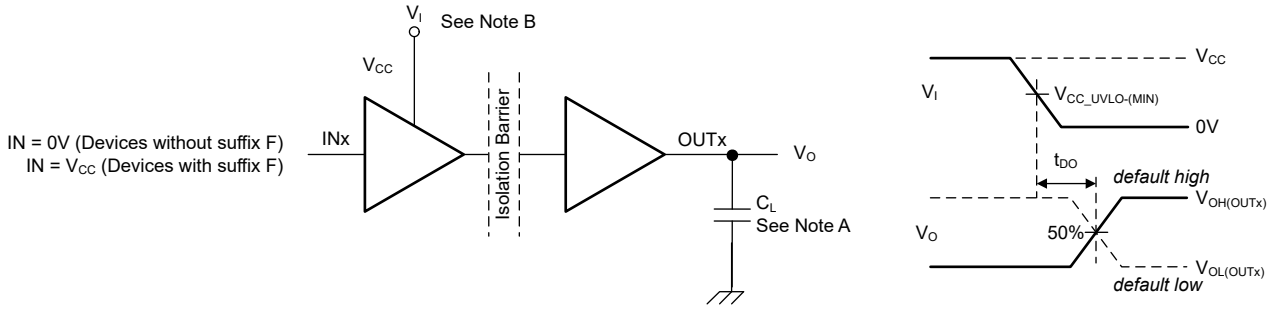
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 1ns, t_f ≤ 1ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate INx (input) generator signal. The 50Ω resistor is not needed in the actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

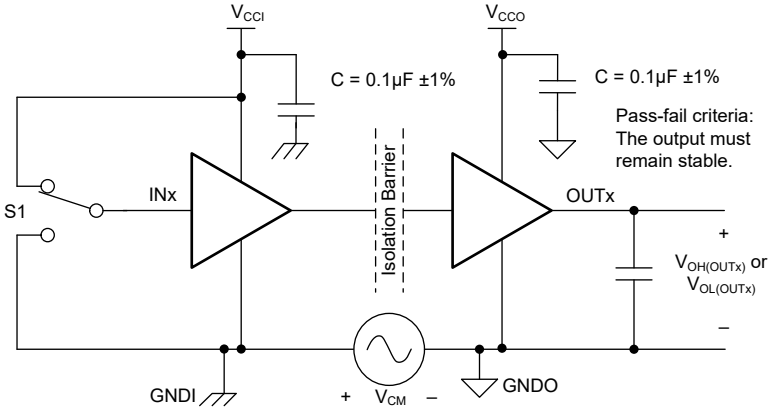
Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10mV/ns

Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. ENx = V_{CC}, channels are enabled during CMTI test.

Figure 7-3. Common-Mode Transient Immunity Test Circuit

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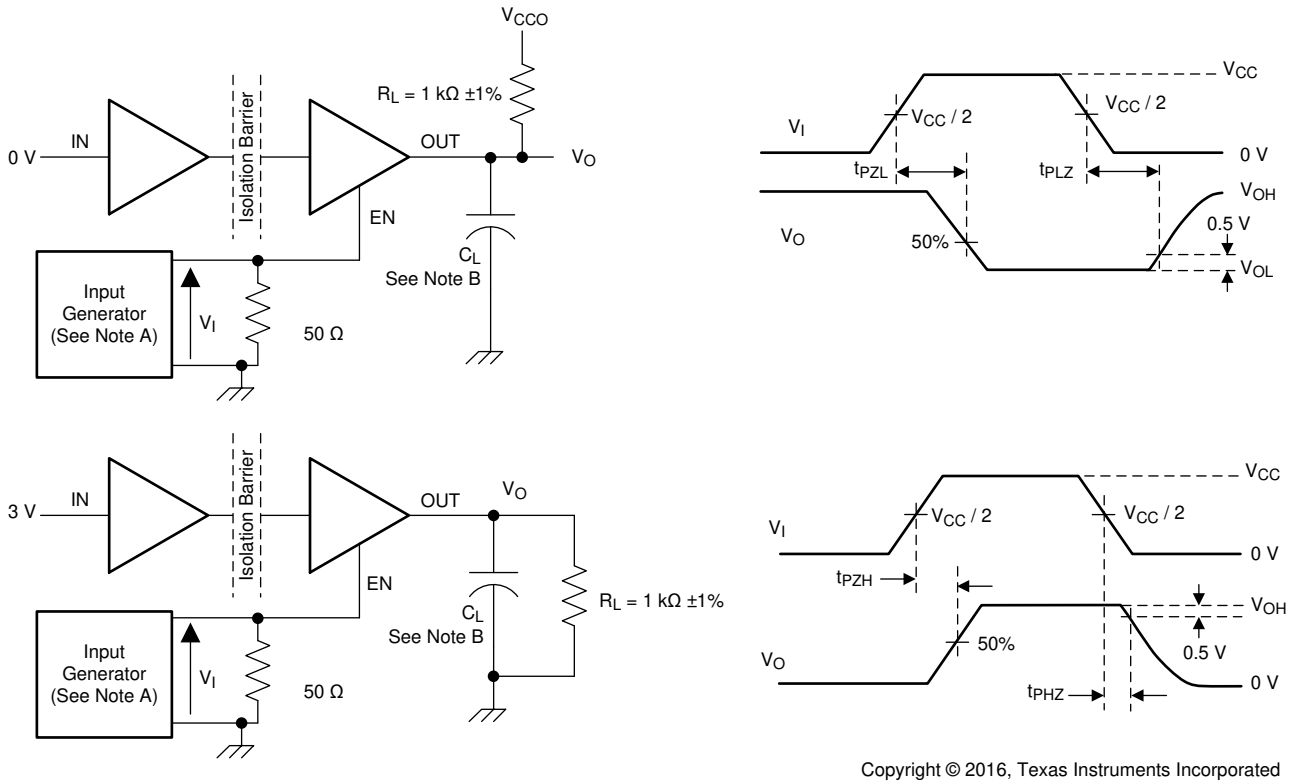

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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 7-4. Enable Propagation Delay Time Test Circuit and Waveform

8 Detailed Description

8.1 Overview

The ISO604x family of devices have an edge based scheme to transmit the digital data across a silicon dioxide based isolation barrier.

The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

8.2 Functional Block Diagram

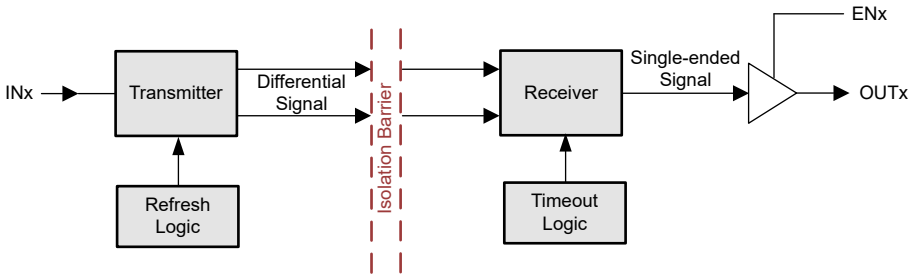

Figure 8-1. Conceptual Block Diagram of an Edge Based Digital Isolator

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8.3 Feature Description

Table 8-1 provides an overview of the device features.

Table 8-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO6040H	4 Forward 0 Reverse	200Mbps	High
ISO6040L	4 Forward 0 Reverse	200Mbps	Low
ISO6041H	3 Forward 1 Reverse	200Mbps	High
ISO6041L	3 Forward 1 Reverse	200Mbps	Low
ISO6042H	2 Forward 2 Reverse	200Mbps	High
ISO6042L	2 Forward 2 Reverse	200Mbps	Low

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are defined and tested by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO604x family of devices incorporates many chip-level design techniques to help overall system robustness.

8.4 Device Functional Modes

The following table lists the functional modes for the ISO604x devices.

Table 8-2. Function Table

V_{CCI}(1)	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is *High* for ISO604xH and *Low* for ISO604xL (with F suffix).
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO604xH and *Low* for ISO604xL (with F suffix). When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq V_{CC_RO(MIN)}$); PD = Powered down ($V_{CC} \leq V_{CC_UVLO-}$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance

(2) The outputs are in undetermined state when $V_{CC_UVLO-} \leq V_{CCI}$ or $V_{CCO} < V_{CC} \geq V_{CC_RO(MIN)}$.

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8.5 Device I/O Schematics

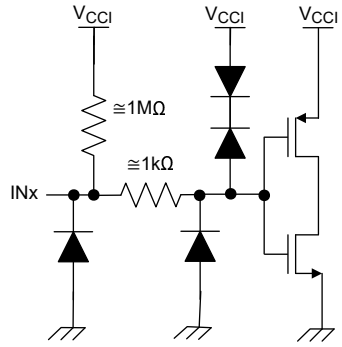

Figure 8-2. Input (INx) Default High (Device With H Suffix) Schematics

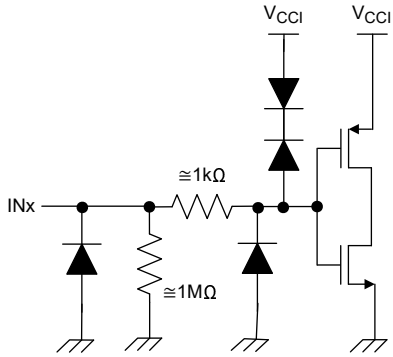

Figure 8-3. Input (INx) Default High (Device With L Suffix) Schematics

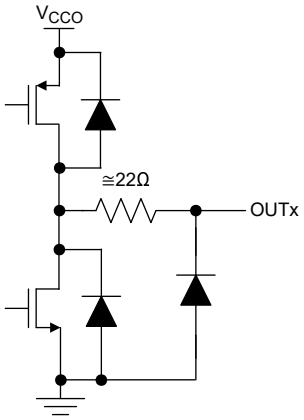

Figure 8-4. Output (OUTx) Schematics

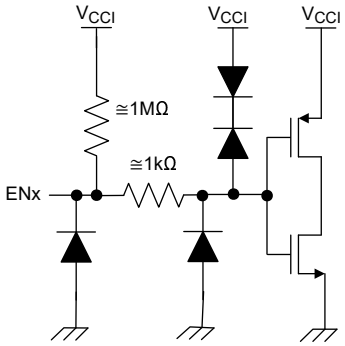

Figure 8-5. Enable (ENx) Schematics

8.6 Overvoltage Tolerant Input

The input pins of this device, INx and ENx, support input signal voltage in excess of the supply voltage (V_{CCI}) on the input side of the device as long as the voltage on the inputs remains below the voltages listed in the Recommended Operating Conditions and Absolute Maximum sections.

This allows the device to support input signal voltages on the inputs when the input supply, V_{CCI}, is unpowered. In this use case, the outputs transition to the default output state when the input side no longer has a valid supply.

These inputs also provide the capability of the inputs to down translate input signal voltages up to the V_{IMAX} in the Recommended Operating Conditions section. For example, an input signal 5V high-level can be used while V_{CCI} is operating a 3.3V.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO604x devices are high-performance, low power, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for parallel (multiple) driver applications. The ISO604x devices use single-ended CMOS-logic switching technology.

The supply voltage range is from 1.71V to 5.5V for both supplies, V_{CC1} and V_{CC2}. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within the Recommended Operating Conditions section. As an example, supplying ISO604x V_{CC1} with 3.3V (which is within 1.71V to 5.5V) and V_{CC2} with 5V (which is also within 1.71V to 5.5V) is possible. You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

Figure 9-1 shows an isolated serial peripheral interface (SPI) for analog input with minimal SPI connections and Figure 9-2 shows the same ADC with all digital IOs and SPI isolated.

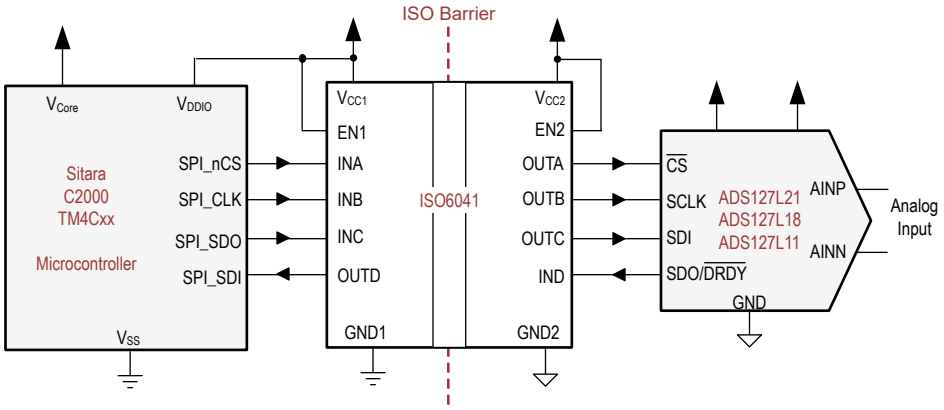

Figure 9-1. Isolated SPI for an Analog Input, Minimal SPI Connections to ADC

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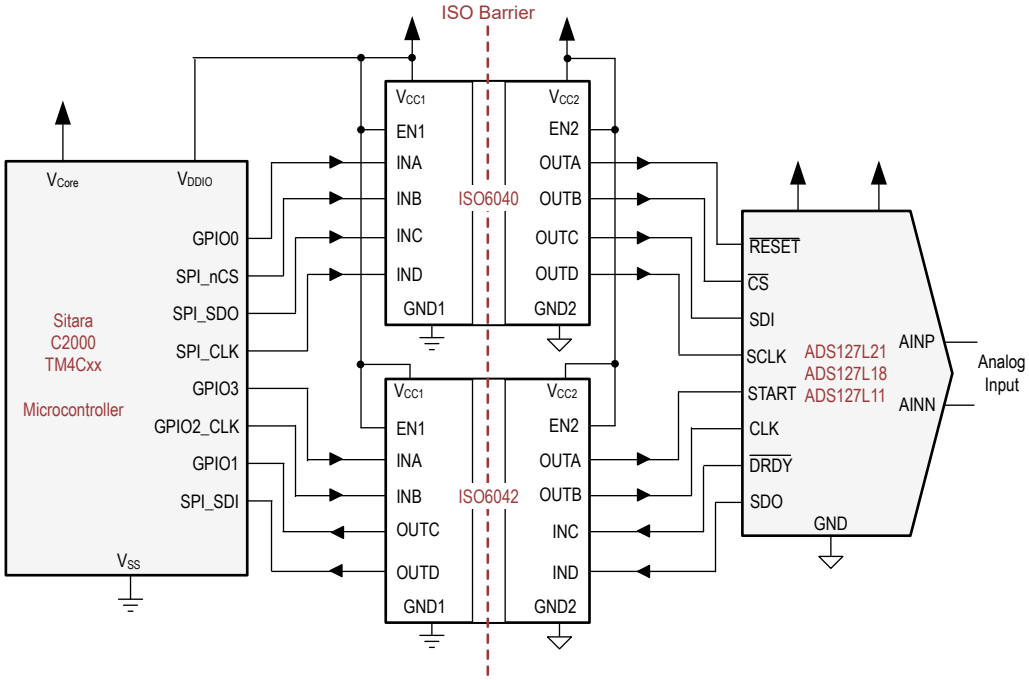

Figure 9-2. Isolated SPI for an Analog Input, Full IO Connection to the ADC

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9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO604x family of devices only require two external bypass capacitors to operate.

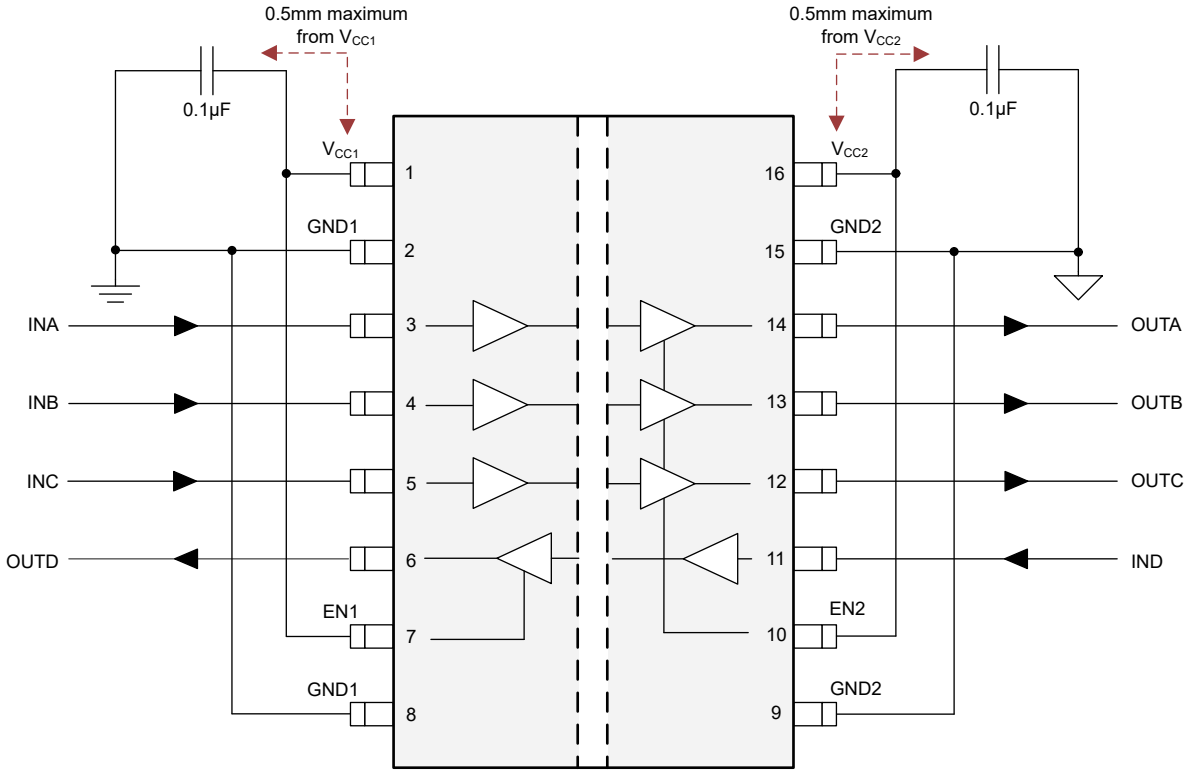
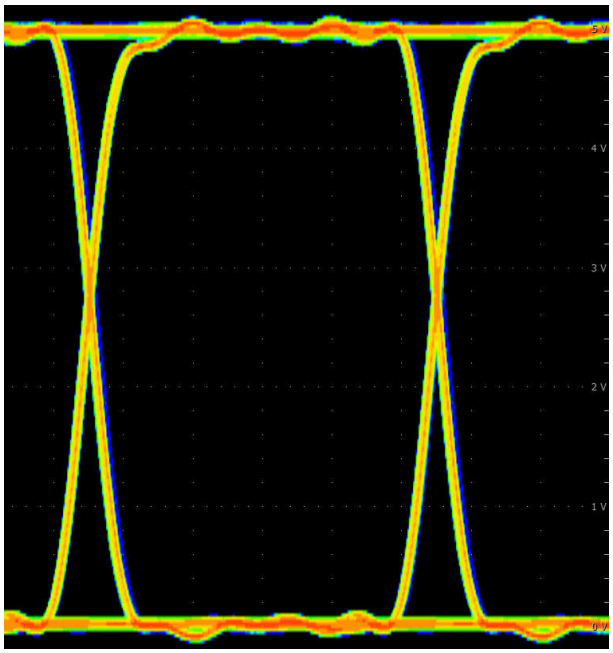


Figure 9-3. Typical ISO604x Circuit

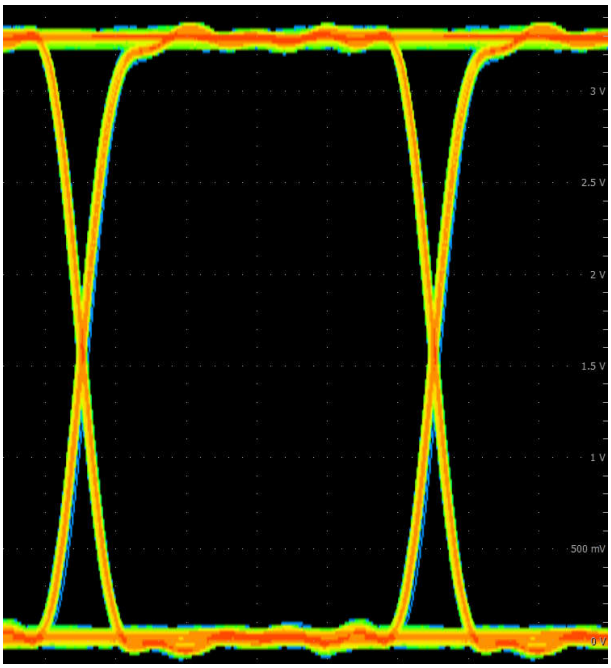
9.2.3 Application Curve

The following typical eye diagrams of the ISO604x family of devices indicates low jitter and wide open eye at the maximum data rate of 200Mbps.



Horizontal 1ns / division, Vertical 1V / division.

Figure 9-4. ISO604x Eye Diagram at 200Mbps PRBS 2^{16} – 1, 5V and 25°C



Horizontal 1ns / division, Vertical 500mV / division.

Figure 9-5. ISO604x Eye Diagram at 200Mbps PRBS 2^{16} – 1, 3.3V and 25°C

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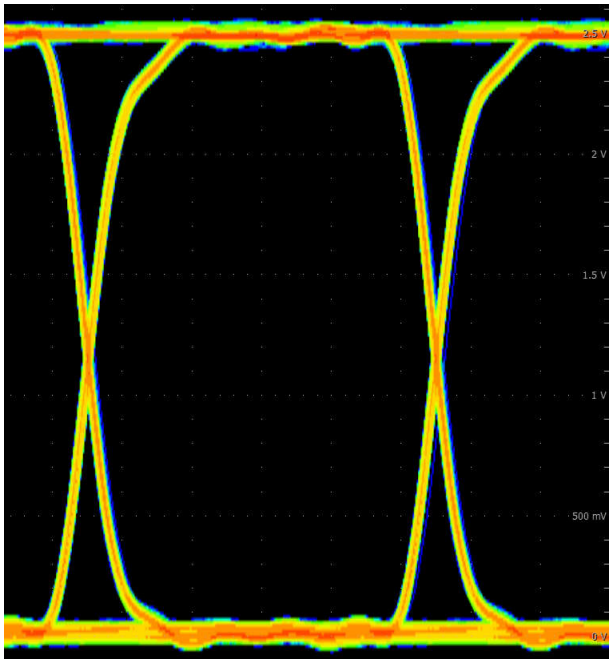
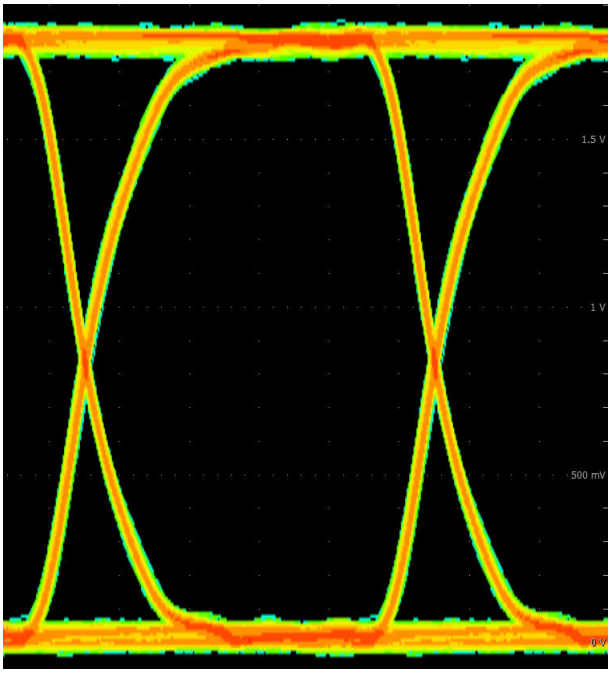


Horizontal 1ns / division, Vertical 500mV / division.

Figure 9-6. ISO604x Eye Diagram at 200Mbps PRBS 2^{16} – 1, 2.5V and 25°C



Horizontal 1ns / division, Vertical 500mV / division.

Figure 9-7. ISO604x Eye Diagram at 200Mbps PRBS 2^{16} – 1, 1.8V and 25°C

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9.3 Power Supply Recommendations

To provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' SN6501 or SN6505B. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* or *SN6505B Low-noise, 1A Transformer Drivers for Isolated Power Supplies* .

9.4 Layout

9.4.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see Figure 9-8). Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide* application note.

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9.4.2 Layout Example

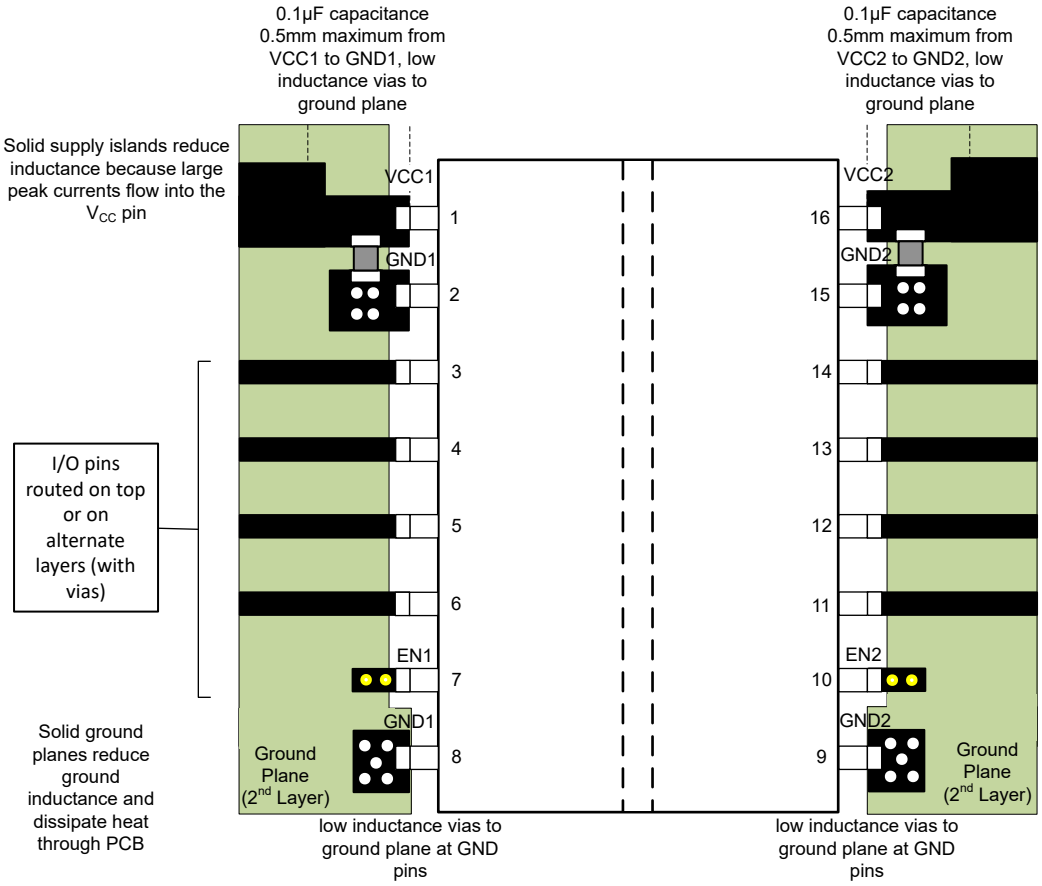

Figure 9-8. Layout Example

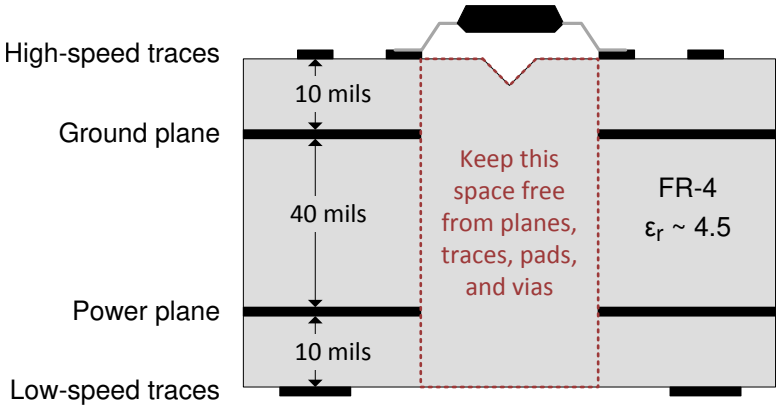

Figure 9-9. Layout Example PCB cross section

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ISO6040 Technical Documents*
- Texas Instruments, *ISO6041 Technical Documents*
- Texas Instruments, *ISO6042 Technical Documents*

- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *Maintain Isolation Ratings in Half the Size with DFB and DFP Digital Isolator Packaging*, application note
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*, application note

- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies*, data sheet
- Texas Instruments, *ADS127L21 512kSPS, Programmable Filter, 24-Bit, Wideband Delta-Sigma ADC*, data sheet
- Texas Instruments, *ADS127L1x 512kSPS, Quad and Octal, Simultaneous-Sampling, 24-Bit ADCs*, data sheet
- Texas Instruments, *ADS127L11 400-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC*, data sheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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10.4 Device Nomenclature

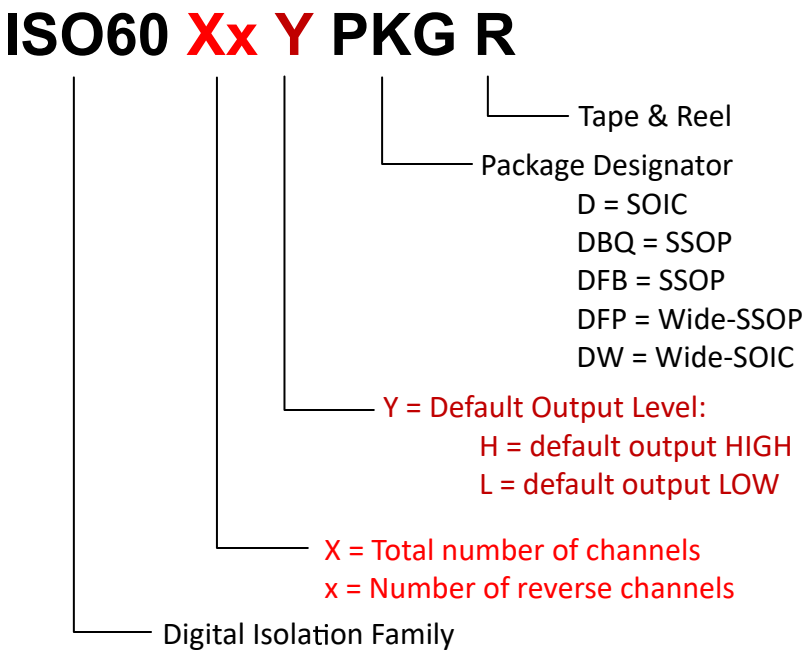

Figure 10-1. Device Nomenclature

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 1, 2026 to August 7, 2026 (from Revision A (March 2026) to Revision B (August 2026)) — **Page**

- Updated document title for clarity of device performance. 0
- Added RMS clock jitter timing throughout the document. 1
- Changed the Part Number in the Package Information table to the general part numbers ISO604xL and ISO604xH with footnote to refer to Device Comparison section for a more detailed list of device features and package options by orderable part number. 1
- Added ISO6040 and ISO6042 devices to the data sheet. 2
- Added 16-DBQ and 16-DFP packages to the data sheet. 2
- Added corrected for C_L from 0pF to 15pF in Parametric Measurement Information section for switching characteristics tests. 27

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- Removed Package from Device Features table, package option per device configuration is summarized in the Device Comparison and Mechanical, Packaging, and Orderable Information sections. 31
- Updated eye diagrams in the Application Curve section..... 36
- Added app note "Maintain Isolation Ratings in Half the Size with DFB and DFP Digital Isolator Packaging" to Related Documentation section..... 40

Changes from Revision * (December 2025) to Revision A (March 2026) **Page**

- Updated status of the data sheet to mixed status for both production and advanced information devices, refer to the Packaging Information table on the Package Option Addendum page in the Mechanical, Packaging, and Orderables section for Production or Preproduction status for specific device and package. Added small form factor packages Wide-SSOP (DFP-16) and SSOP (DBQ-16) to document. 1
- Updated the CMTI minimum and typical values, updated part to part skew maximum values and removed clock jitter throughout the document. 1
- Deleted planned CSA certification and added planned UL 1577 and CSA CAS Notice No. 5A certification throughout the document. Removed IEC 60601-1 from planned certifications. 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Updated the part to part skew for 2.5V, 3.3V and 5V V_{CC} maximum values and updated the time interval error (t_{ie}) typical values for all V_{CCs} in the Switching Characteristics sections. 6
- Updated the minimum and typical CMTI values for all V_{CCs} and updated the typical values for input capacitance (C_I) for all V_{CCs} in Electrical Characteristics sections. 6
- Updated the maximum I_{CC1} and I_{CC2} values for all V_{CCs} in the Supply Current sections for 10Mbps, 25Mbps and 100Mbps. Added typical ICC I_{CC1} and I_{CC2} values for all V_{CCs} in the Supply Current sections..... 6
- Added the Insulation Characteristics Curves section to the document..... 24
- Added the Typical Characteristics section to the document..... 26
- Added the Application Curve section to the document..... 36

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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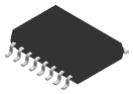
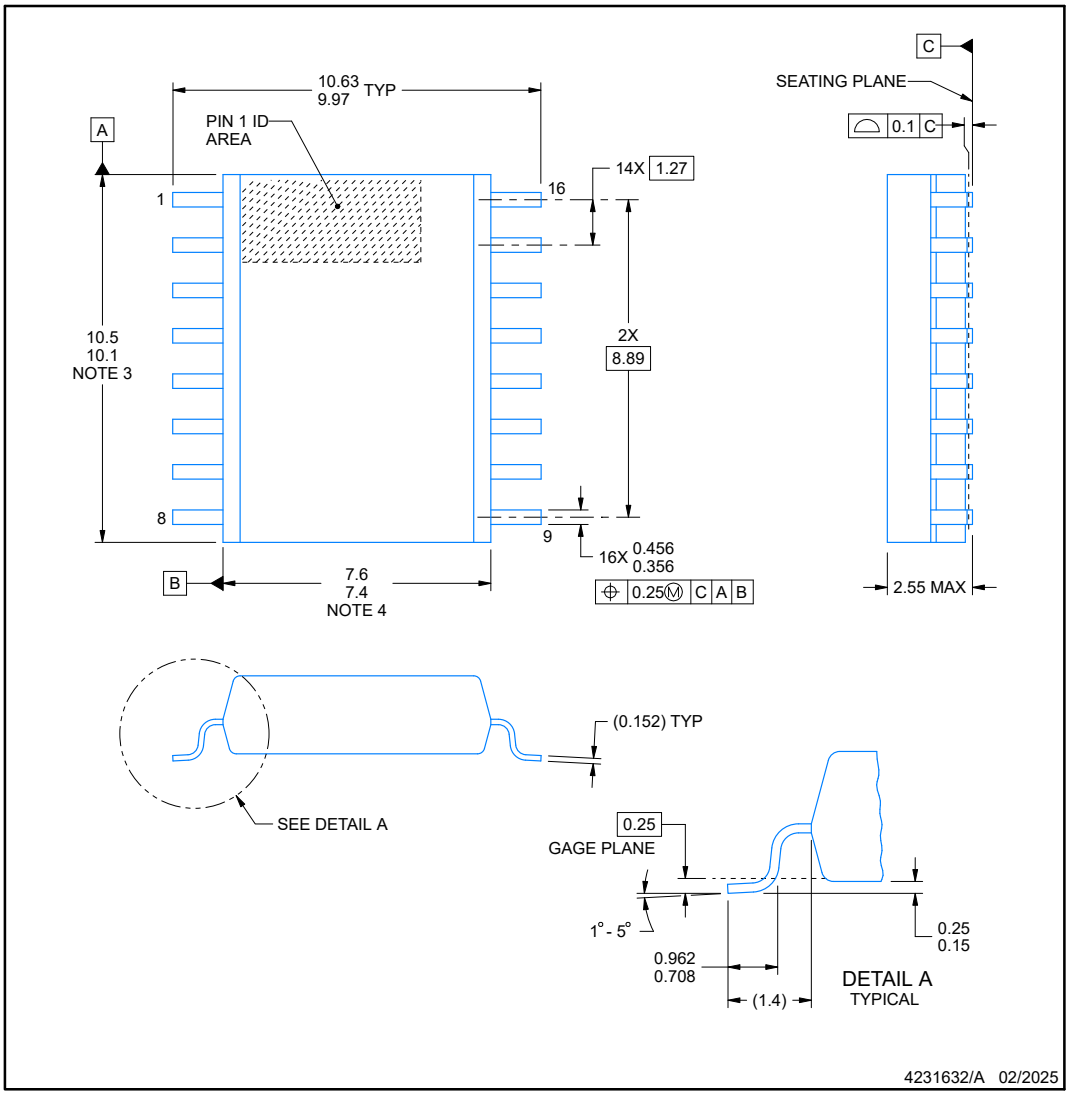


PACKAGE OUTLINE

DW0016C-C01

SOIC - 2.55 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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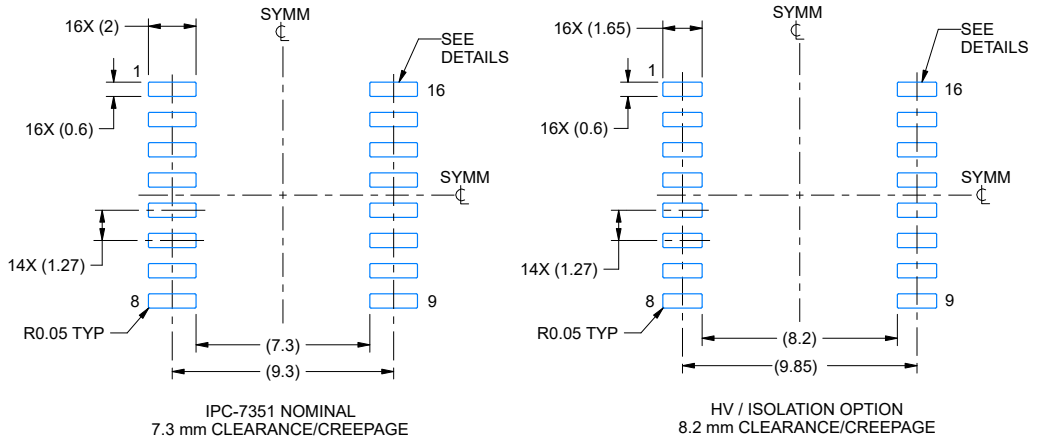
EXAMPLE BOARD LAYOUT

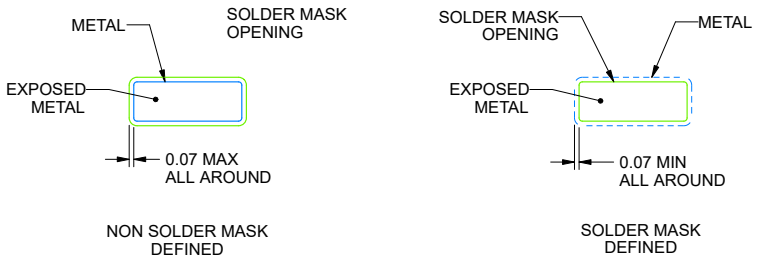
DW0016C-C01

SOIC - 2.55 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



SOLDER MASK DETAILS

4231632/A 02/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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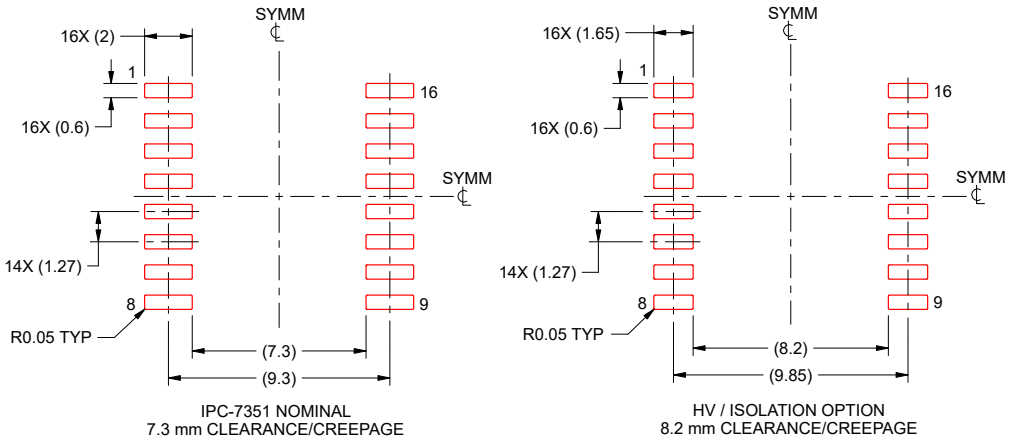
EXAMPLE STENCIL DESIGN

DW0016C-C01 — **SOIC - 2.55 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4231632/A 02/2025

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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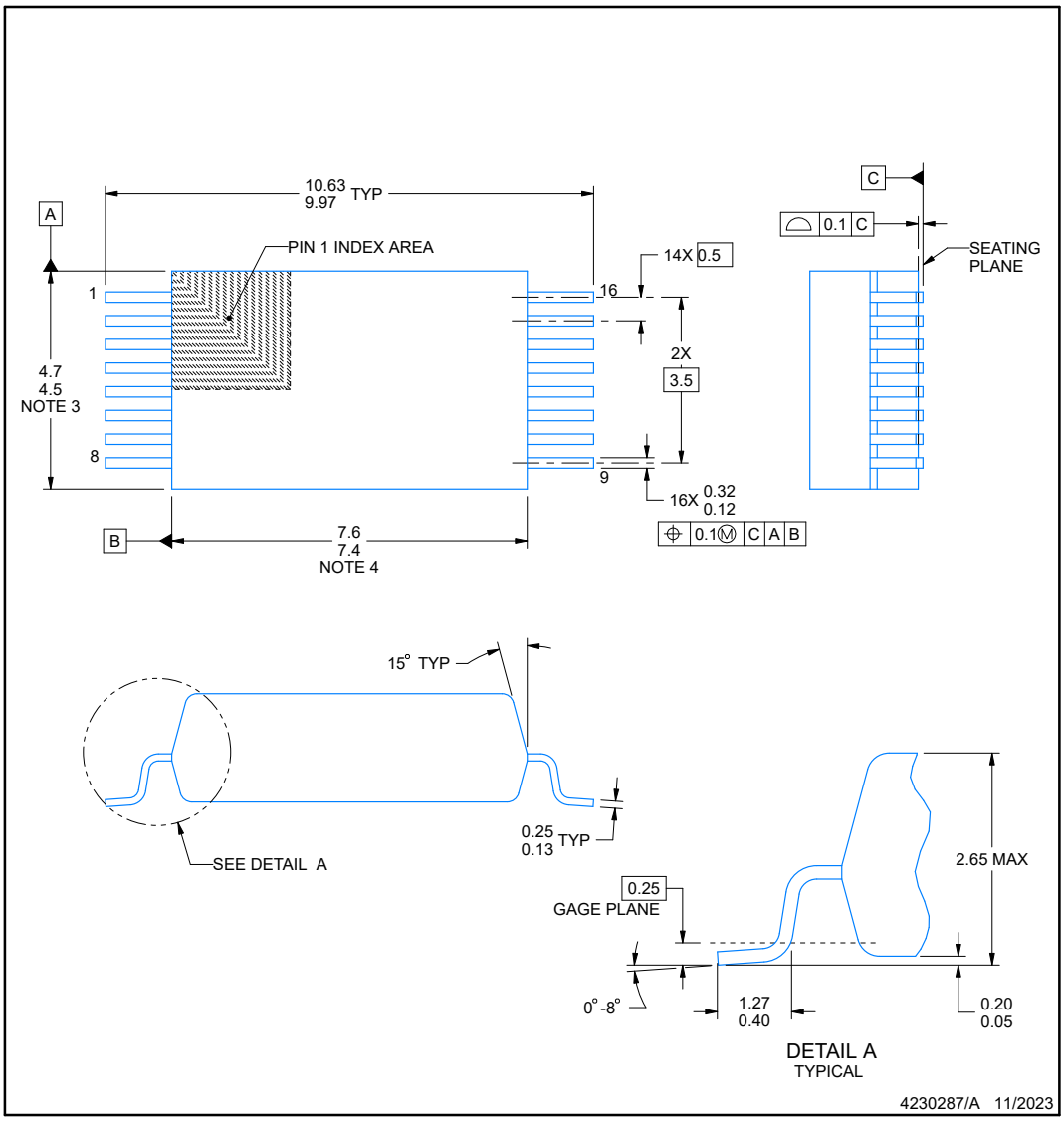
PACKAGE OUTLINE

DFP0016A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

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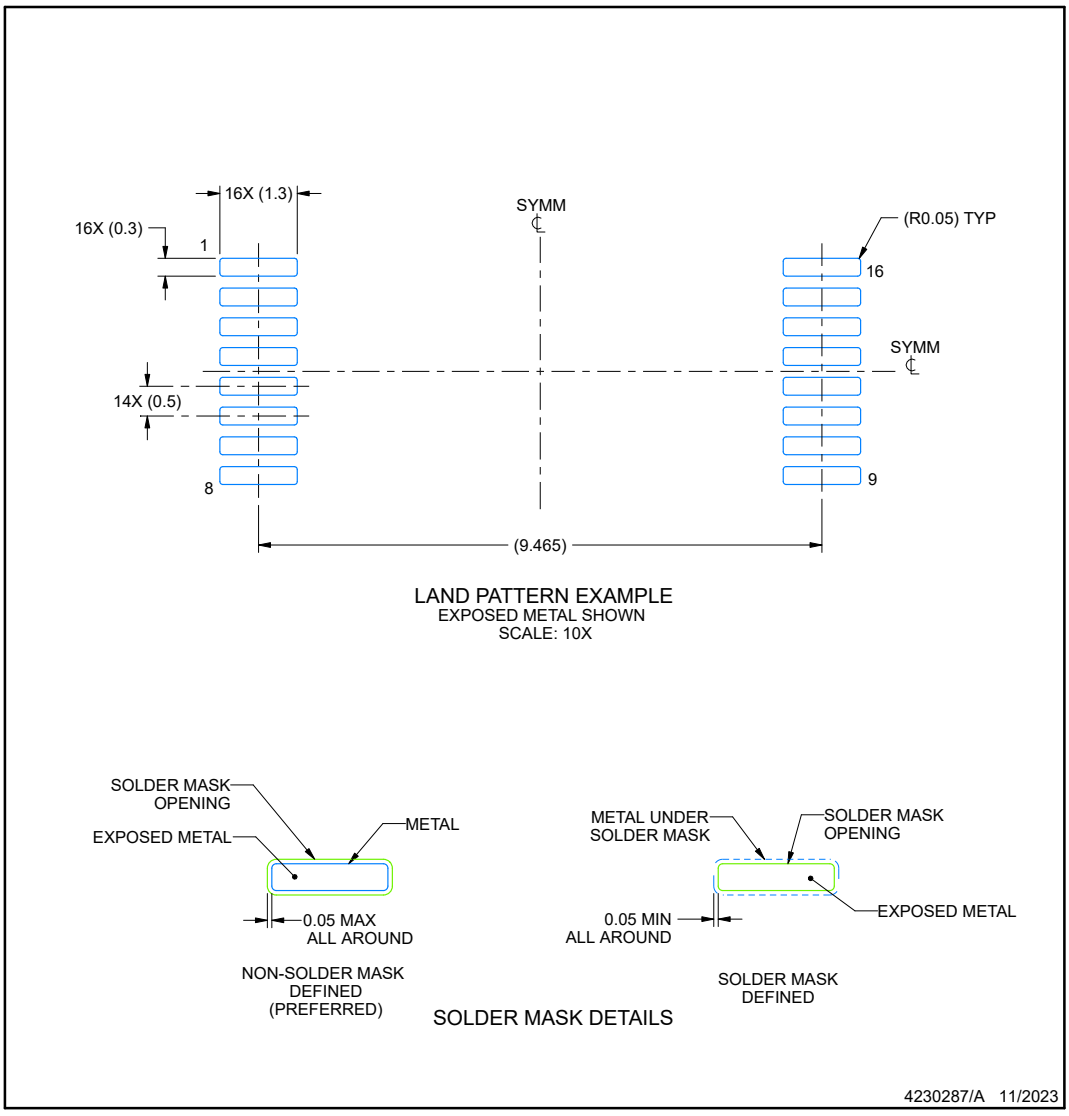
EXAMPLE BOARD LAYOUT

DFP0016A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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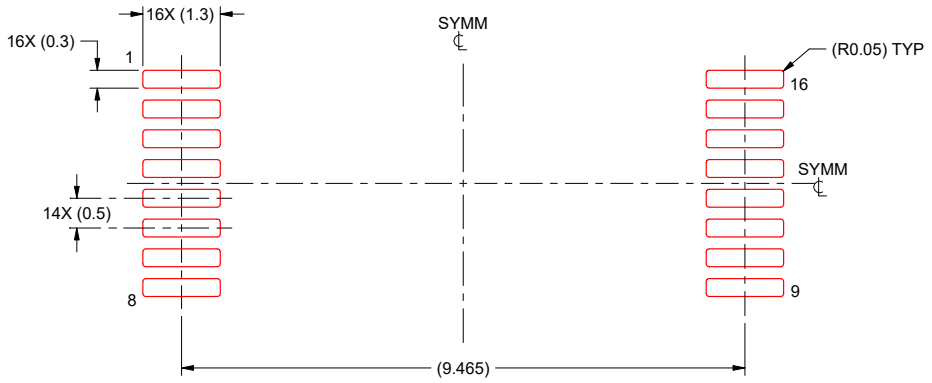
EXAMPLE STENCIL DESIGN

DFP0016A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4230287/A 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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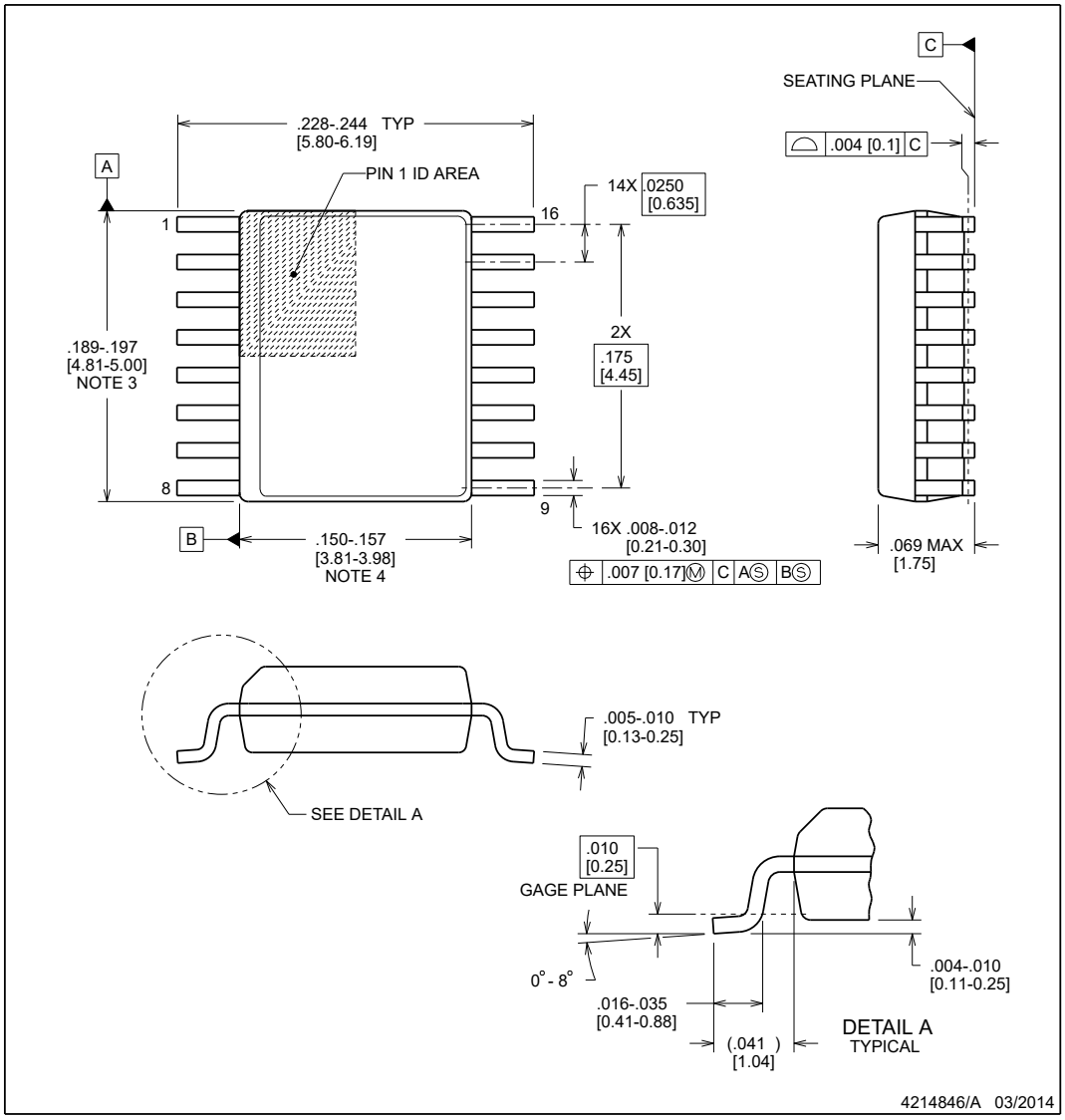
PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

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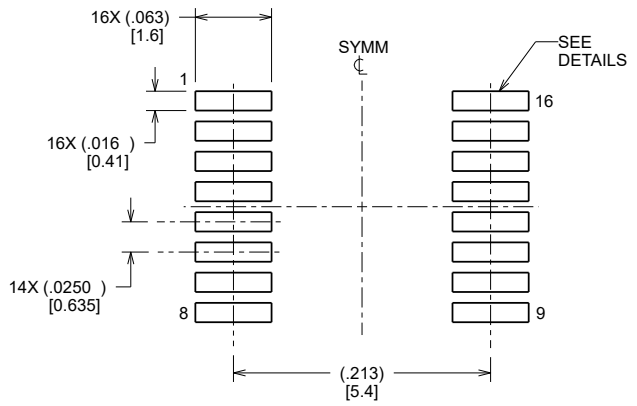
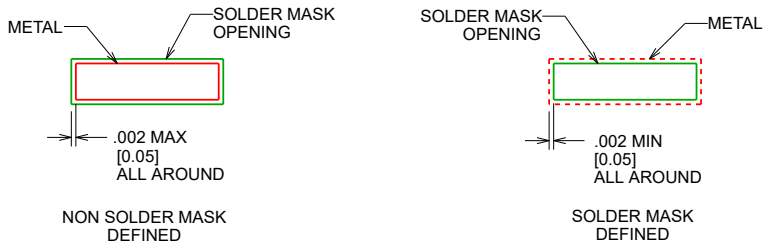
EXAMPLE BOARD LAYOUT

DBQ0016A — **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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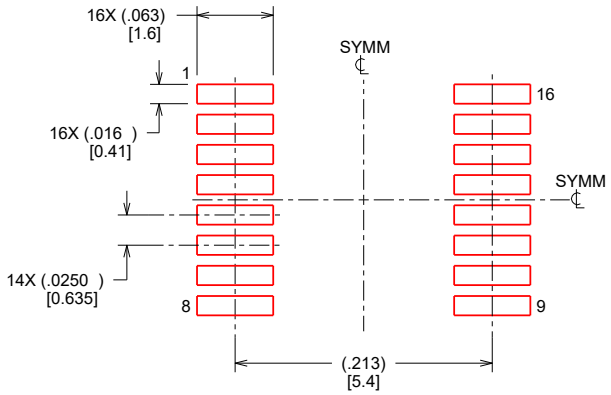
EXAMPLE STENCIL DESIGN

DBQ0016A — **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO6041LDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6041L
XISO6041HDBQR	Active	Preproduction	SSOP (DBQ) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6041HDFPR	Active	Preproduction	SSOP (DFP) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6041HDWR	Active	Preproduction	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6041LDBQR	Active	Preproduction	SSOP (DBQ) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6041LDFPR	Active	Preproduction	SSOP (DFP) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

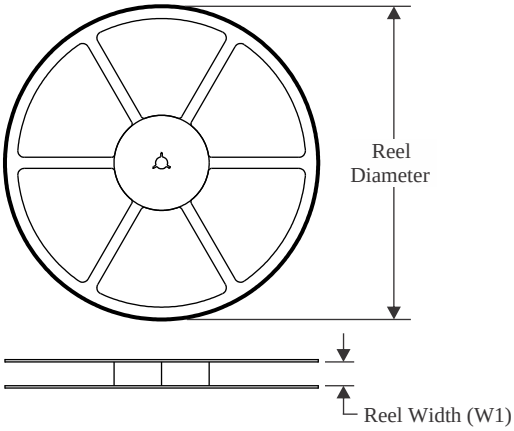
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

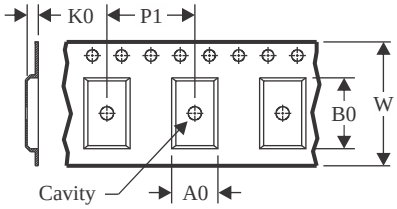
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

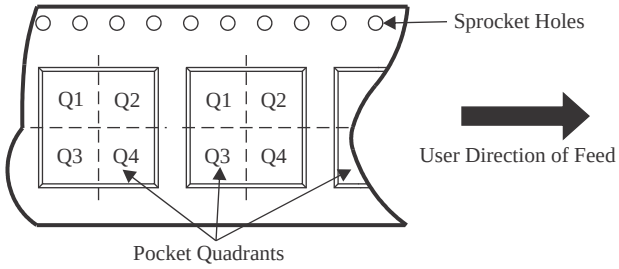


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

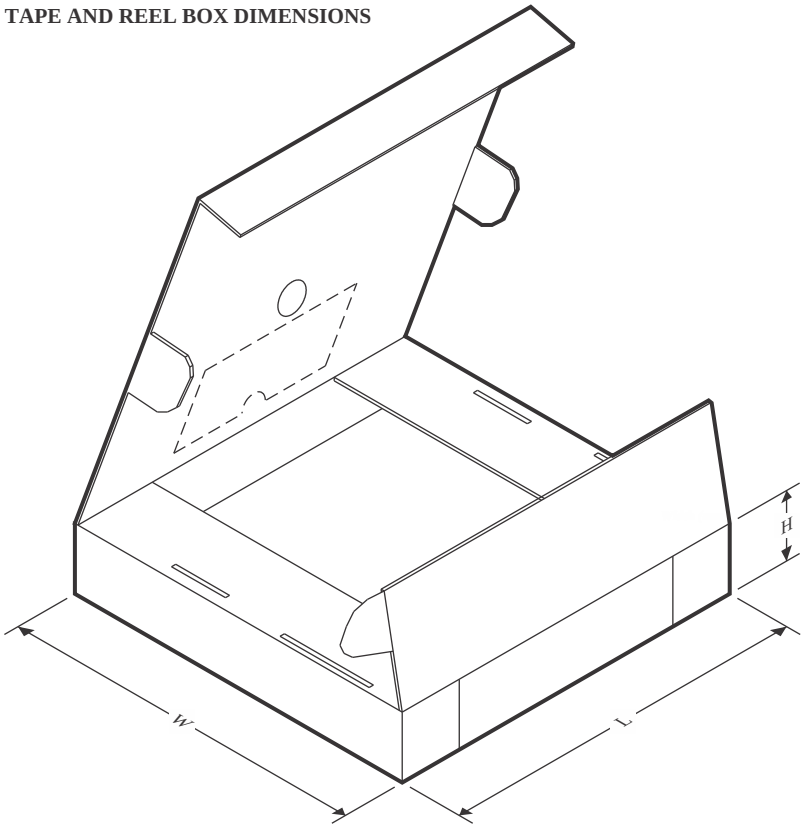
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6041LDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6041LDWR	SOIC	DW	16	2000	353.0	353.0	32.0

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