TPS1HA08-Q1 TPS1HA08-Q1, 40V, 8mΩ Single-Channel Smart High-Side Switch

1 Features

- Single-channel smart high-side switch with 8mΩ R_{ON} (T_J = 25°C)
- Qualified for automotive applications:
  - AEC Q-100 Qualified
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Withstands 40V load dump
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Improve reliability through selectable current limiting
  - Current limit set-point at 20A or 80A
  - Overcurrent response of current clamping or instant shutdown
- Robust integrated output protection:
  - Integrated thermal protection
  - Protection against short to ground and battery
  - Automatic switch-on during reverse battery
  - Automatic shut off if loss of battery and ground occurs
  - Integrated output clamp to demagnetize inductive loads
  - Configurable fault handling
- Analog sense output can be configured to accurately measure:
  - Load current
  - Supply voltage
  - Device temperature
- Provides FLT indication back to MCU
  - Detection of open load and short-to-battery

2 Applications

- Body control modules
- Incandescent and LED lighting
- Heating elements:
  - Seat heaters
  - Glow plug
  - Tank heaters
- Transmission control unit
- Climate control
- Infotainment display
- ADAS modules

3 Description

The TPS1HA08-Q1 device is a single-channel smart high-side switch intended for use with 12V automotive systems. The device integrates robust protection and diagnostic features to provide output port protection even during harmful events like short circuits. The device protects against faults through a reliable current limit, which, depending on device variant, is available at both 80A and 20A and is configurable to react to an overcurrent event by either instantly turning the switch off or by regulating the output current at the set point. The high current limit option allows for usage in loads that require large transient currents, while the low current limit option provides improved protection for loads that do not require high peak current.

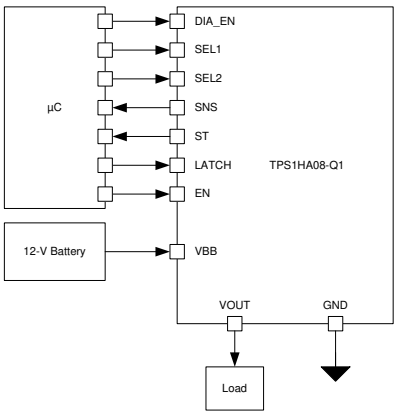
The TPS1HA08-Q1 also provides a high accuracy analog current sense that allows for improved diagnostics when driving varied load profiles. By reporting load current, device temperature, and supply voltage to a system MCU, the device enables predictive maintenance and load diagnostics that lengthen the system lifetime.

The TPS1HA08-Q1 is available in a small 16-pin HTSSOP package which allows for reduced PCB footprint.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS1HA08-Q1	HTSSOP (16)	5.00mm × 4.40mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison Table

Device Version	Full Device Number	Current Limit (I_{CL})	Overcurrent Behavior	Watchdog Feature
A	TPS1HA08**A**-Q1	20A	Disable Switch Immediately	Disabled
B	TPS1HA08**B**-Q1	80A	Disable Switch Immediately	Disabled
C	TPS1HA08**C**-Q1	20A	Clamp Current at I_{CL} until Thermal Shutdown	Disabled
D	TPS1HA08**D**-Q1	80A	Clamp Current at I_{CL} until Thermal Shutdown	Disabled
E	TPS1HA08**E**-Q1	20A	Disable Switch Immediately	Enabled

5 Pin Configuration and Functions

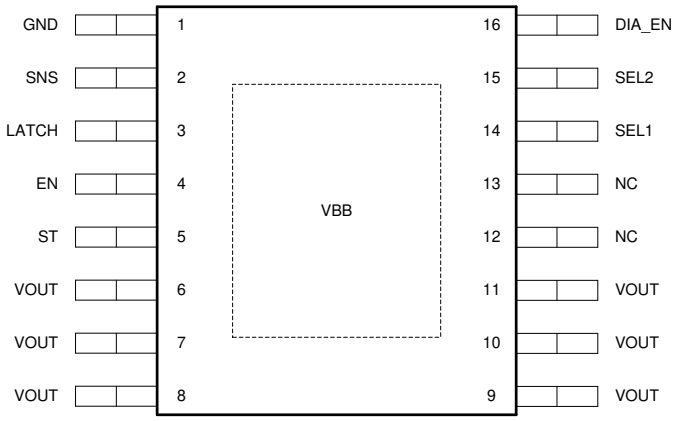


Figure 5-1. PWP Package 16-Pin HTSSOP Top View

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	GND	—	Device ground
2	SNS	O	Sense output
3	LATCH	I	Sets fault handling behavior (latched or auto-retry)
4	EN	I	Switch control input, active high
5	$\overline{ST}$	O	Switch diagnostic feedback, active low
6, 7, 8, 9, 10, 11	VOUT	O	Switch output
12	NC	--	No connect
13	NC	--	No connect
14	SEL1	I	Diagnostics Select 1
15	SEL2	I	Diagnostics Select 2
16	DIA_EN	I	Diagnostic enable, active high
Exposed pad	VBB	I	Power supply input

(1) I = input, O = output

5.1 Recommended Connections for Unused Pins

The TPS1HA08-Q1 device is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins can be optional.

Table 5-2. Connections for Optional Pins

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SNS	Ground through 1kΩ resistor	Analog sense is not available.
LATCH	Float or ground through R_{PROT} resistor	With LATCH unused, the device auto-retries after a fault. If latched behavior is desired, it is possible to use one microcontroller output to control the latch function of several high-side channels.
$\overline{ST}$	Float	All faults are indicated by the analog SNS pin. The $\overline{ST}$ pin provides the additional benefits: • Provide fault indication when DIA_EN = 0 • Provide fault indication regardless of SELx pin conditions • Provide fault indication to a simple digital I/O (rather than ADC or comparator used with the SNS signal)

Table 5-2. Connections for Optional Pins (continued)

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SEL1	Float or ground through R_{PROT} resistor	SEL1 selects between the V_{BB} and T_J sensing features. With SEL1 unused, only load diagnostics are available.
SEL2	Ground through R_{PROT} resistor	With SEL2 = 0V, V_{BB} measurement diagnostics are not available.
DIA_EN	Float or ground through R_{PROT} resistor	With DIA_EN unused, analog sense, open-load and short-to-battery diagnostics are not available.

R_{PROT} is used to protect the pins from excess current flow during reverse battery conditions. For more information, please see the section on *Reverse Battery* protection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{BB}	Maximum continuous supply voltage			36	V
V_{LD}	Load dump voltage	ISO16750-2:2010(E)		40	V
V_{Rev}	Reverse battery voltage, V_{REV} ≤ 3 minutes		–18		V
V_{EN}	Enable pin voltage		–1	7	V
V_{LATCH}	LATCH pin voltage		–1	7	V
V_{ST}	Status pin voltage		–1	7(2)	V
V_{DIA_EN}	Diagnostic Enable pin voltage		–1	7	V
V_{SNS}	Sense pin voltage		–1	7	V
V_{SEL1}, V_{SEL2}	Select pin voltage		–1	7	V
I_{GND}	Reverse ground current	V_{BB} < 0V		–50	mA
E_{TOFF}	Energy dissipation during turn-off	Single pulse, L_{OUT} = 5mH, T_A = 125°C		95	mJ
		Repetitive pulse, 10Hz, L_{OUT} = 5mH, T_A = 125°C		56	mJ
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) These pins are adjacent to pins that handle high-voltages. In the event of a pin-to-pin short, there is no device damage.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except exposed pad and pins 6 to 11	±2000	V
			Exposed pad and pins 6 to 11	±4000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BB}	Nominal supply voltage		8	18	V
V_{BB}	Extended operating range (1)		3	28	V
V_{EN}	Enable voltage		–1	5.5	V
V_{LATCH}	LATCH voltage		–1	5.5	V
V_{DIA_EN}	Diagnostic enable voltage		–1	5.5	V
V_{SEL1}, V_{SEL2}	Select voltage		–1	5.5	V
V_{ST}	Status voltage		0	5.5	V
V_{SNS}	Sense voltage		–1	$V_{SNSclamp}$	V
I_{MAX}	Continuous load current	T_A = 70°C	0	10	A

(1) Device functions within extended operating range, however some parametric values can not apply.

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS1HA08-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 8V to 18V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT						
V_{Clamp}	V_{DS} clamp voltage		40		58	V
V_{UVLOF}	V_{BB} undervoltage lockout falling			2.5	3	V
V_{UVLOR}	V_{BB} undervoltage lockout rising			2.5	3	V
I_{SB}	Standby current (includes MOSFET leakage)	V_{BB} = 13.5V, T_J = 25°C V_{EN} = V_{DIA_EN} = 0V, V_{OUT} = 0V			0.5	µA
		V_{BB} = 13.5V, T_J = 85°C V_{EN} = V_{DIA_EN} = 0V, V_{OUT} = 0V			0.5	µA
		V_{BB} = 13.5V, T_J = 125°C, V_{EN} = V_{DIA_EN} = 0V, V_{OUT} = 0V			3	µA
$I_{OUT(standby)}$	Output leakage current	V_{BB} = 13.5V, T_J = 25°C V_{EN} = V_{DIA_EN} = 0V, V_{OUT} = 0V		0.01	0.5	µA
		V_{BB} = 13.5V, T_J = 125°C V_{EN} = V_{DIA_EN} = 0V, V_{OUT} = 0V			3	µA
I_{DIA}	Current consumption in diagnostic mode	V_{BB} = 13.5V, I_{SNS} = 0mA V_{EN} = 0V, V_{DIA_EN} = 5V, V_{OUT} = 0V		3	6	mA
I_Q	Quiescent current	V_{BB} = 13.5V V_{EN} = V_{DIA_EN} = 5V, I_{OUT} = 0A, V_{SELX} = 0V		3	6	mA
t_{STBY}	Standby mode delay time	V_{EN} = V_{DIA_EN} = 0V to Standby		20		ms
R_{ON} CHARACTERISTICS						
R_{ON}	On-resistance Includes MOSFET and package	T_J = 25°C, 6V ≤ V_{BB} ≤ 28V		9		mΩ
		T_J = 150°C, 6V ≤ V_{BB} ≤ 28V			20	mΩ
		T_J = 25°C, 3V ≤ V_{BB} ≤ 6V			15	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	T_J = 25°C, -18V ≤ V_{BB} ≤ -8V		9		mΩ
		T_J = 105°C, -18V ≤ V_{BB} ≤ -8V			20	mΩ
CURRENT SENSE CHARACTERISTICS						
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}			4600		

6.5 Electrical Characteristics (continued)

V_{BB} = 8V to 18V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SNSI}	Current sense current and current sense accuracy	V_{EN} = V_{DIA_EN} = 5V, V_{SEL1} = V_{SEL2} = 0V	I_{OUT} = 20A		4.35		mA
				–5		5	%
			I_{OUT} = 8A		1.74		mA
				–5		5	%
			I_{OUT} = 3A		0.65		mA
				–5		5	%
			I_{OUT} = 1A		0.217		mA
				–5		5	%
			I_{OUT} = 300mA		0.065		mA
				–12		12	%
			I_{OUT} = 100mA		0.022		mA
				–42		42	%
T_J SENSE CHARACTERISTICS							
I_{SNST}	Temperature sense current	V_{DIA_EN} = 5V, V_{SEL1} = 5V, V_{SEL2} = 0V	T_J = –40°C		0.12		mA
			T_J = 25°C		0.85		mA
			T_J = 85°C		1.52		mA
			T_J = 150°C		2.25		mA
dI_{SNST}/dT	Coefficient				0.0112		mA/°C
V_{BB} SENSE CHARACTERISTICS							
I_{SNSV}	Voltage sense current	V_{DIA_EN} = 5V, V_{SEL1} = 5V, V_{SEL2} = 5V	V_{BB} = 3V		0.26		mA
			V_{BB} = 8V		0.69		mA
			V_{BB} = 13.5V		1.17		mA
			V_{BB} = 18V		1.56		mA
			V_{BB} = 28V		2.43		mA
dI_{SNSV}/dV	Coefficient				0.0867		mA/V
SNS CHARACTERISTICS							
I_{SNSFH}	I_{SNS} fault high level	V_{DIA_EN} = 5V, V_{SEL1} = 0V, V_{SEL2} = 0		6	6.9	7.6	mA
$I_{SNSleak}$	I_{SNS} leakage	V_{DIA_EN} = 0V		0		1	µA
$V_{SNSclamp}$	V_{SNS} clamp				5.9		V
CURRENT LIMIT CHARACTERISTICS							
I_{CL}	Current Limit	Device Version B/D	T_J = –40°C	75.5	88.8	102.1	A
			T_J = 25°C	68	80	92	
			T_J = 150°C	51	60	69	
		Device Version A/C/E	T_J = –40°C	16	22.2	27.8	A
			T_J = 25°C	14.4	20	25	
			T_J = 150°C	10.8	15	18.8	
$\overline{ST}$ PIN CHARACTERISTICS							
V_{OL}	Open-load detection voltage	V_{EN} = 0V, V_{DIA_EN} = 5V		2	2.5	4	V
t_{OL1}	OL and STB indication time - switch disabled	From falling edge of EN V_{EN}= 5V to 0V, V_{DIA_EN} = 5V, V_{SELx} = 00 I_{OUT} = 0mA, V_{OUT} = 4V		300	500	700	µs
t_{OL2}	OL and STB indication time - switch disabled	From rising edge of DIA_EN V_{EN} = 0V, V_{DIA_EN} = 0V to 5V, V_{SELx} = 00 I_{OUT} = 0mA, V_{OUT} = 4V				50	µs

6.5 Electrical Characteristics (continued)

V_{BB} = 8V to 18V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OL3}	OL and STB indication time - switch disabled	From rising edge of VOUT V_{EN} = 0V, V_{DIA_EN} = 5V, V_{SELx} = 00 I_{OUT} = 0mA, V_{OUT} = 0V to 4V			50	µs
T_{ABS}	Thermal shutdown		160			°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
t_{RETRY}	Retry time	Minimum time from fault shutdown to switch re-enable (for thermal shutdown, current limit, and energy limit)	1	2	3	ms
t_{WD}	Watchdog timer	Device version E	350	400	450	ms
EN PIN CHARACTERISTICS(1)						
$V_{IL, EN}$	Input voltage low level				0.8	V
$V_{IH, EN}$	Input voltage high level	No GND network Diode	2			V
$V_{IHYS, EN}$	Input voltage hysteresis	No GND network Diode		250		mV
$I_{IL, EN}$	Input current low level	V_{EN} = 0.8V		0.8		µA
$I_{IH, EN}$	Input current high level	V_{EN} = 2.0V		2		µA
R_{EN}	Internal pulldown resistor			1		MΩ
DIA_EN PIN CHARACTERISTICS (1)						
V_{IL, DIA_EN}	Input voltage low level	No GND network Diode			0.8	V
V_{IH, DIA_EN}	Input voltage high level	No GND network Diode	2			V
V_{IHYS, DIA_EN}	Input voltage hysteresis			250		mV
I_{IL, DIA_EN}	Input current low level	V_{DIA_EN} = 0.8V		0.8		µA
I_{IH, DIA_EN}	Input current high level	V_{DIA_EN} = 2.0V		2		µA
R_{DIA_EN}	Internal pulldown resistor			1		MΩ
SEL1 AND SEL2 PIN CHARACTERISTICS (1)						
$V_{IL, SELx}$	Input voltage low level	No GND network Diode			0.8	V
$V_{IH, SELx}$	Input voltage high level		2			V
$V_{IHYS, SELx}$	Input voltage hysteresis			250		mV
$I_{IL, SELx}$	Input current low level	V_{SELx} = 0.8V		0.8		µA
$I_{IH, SELx}$	Input current high level	V_{SELx} = 2.0V		2		µA
R_{SELx}	Internal pulldown resistor			1		MΩ
LATCH PIN CHARACTERISTICS (1)						
$V_{IL, LATCH}$	Input voltage low level	No GND network Diode			0.8	V
$V_{IH, LATCH}$	Input voltage high level	No GND network Diode	2			V
$V_{IHYS, LATCH}$	Input voltage hysteresis			250		mV
$I_{IL, LATCH}$	Input current low level	V_{LATCH} = 0.8V		0.8		µA
$I_{IH, LATCH}$	Input current high level	V_{LATCH} = 2.0V		2		µA
R_{LATCH}	Internal pulldown resistor			1		MΩ
ST PIN CHARACTERISTICS (1)						
$V_{OL, ST}$	Output voltage low level	I_{ST} = 1mA			0.4	V
I_{STleak}	Leakage current	V_{ST} = 5V			2	µA

(1) V_{BB} = 3 to 28V

6.6 Switching Characteristics

V_{BB} = 13.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Turn-on delay time	V_{BB} = 13.5V, R_L = 2.6Ω	20	70	100	µs
t_{DF}	Turn-off delay time	V_{BB} = 13.5V, R_L = 2.6Ω	20	50	100	µs
SR_R	VOUT rising slew rate	V_{BB} = 13.5V, 20% to 80% of V_{OUT}, R_L = 2.6Ω	0.1	0.35	0.7	V/µs
SR_F	VOUT falling slew rate	V_{BB} = 13.5V, 80% to 20% of V_{OUT}, R_L = 2.6Ω	0.1	0.5	0.7	V/µs
t_{ON}	Turn-on time	V_{BB} = 13.5V, R_L = 2.6Ω	39	80	145	µs
t_{OFF}	Turn-off time	V_{BB} = 13.5V, R_L = 2.6Ω	39	75	145	µs
t_{ON} - t_{OFF}	Turn-on and off matching	200µs enable pulse	–50	0	50	µs
E_{ON}	Switching energy losses during turn-on	V_{BB} = 13.5V, R_L = 2.6Ω		0.4		mJ
E_{OFF}	Switching energy losses during turn-off	V_{BB} = 13.5V, R_L = 2.6Ω		0.4		mJ

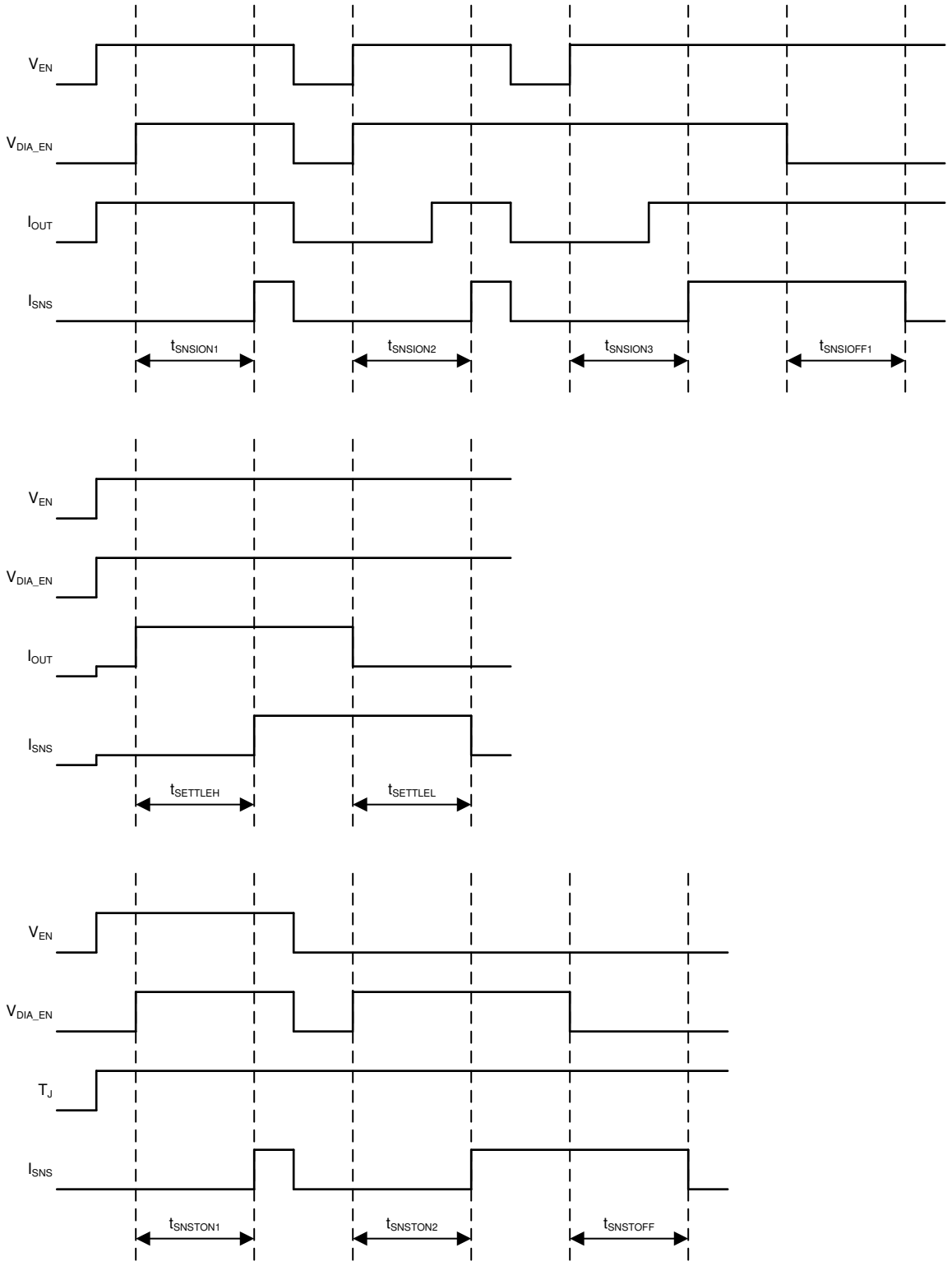
6.7 SNS Timing Characteristics

V_{BB} = 8 to 18V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIA_EN	V_{EN} = 5V, V_{DIA_EN} = 0V to 5V R_{SNS} = 1kΩ, R_L = 2.6Ω			40	µs
$t_{SNSION2}$	Settling time from rising edge of EN	V_{EN} = V_{DIA_EN} = 0V to 5V R_{SNS} = 1kΩ, R_L = 2.6Ω			180	µs
$t_{SNSION3}$	Settling time from rising edge of EN	V_{EN} = 0V to 5V, V_{DIA_EN} = 5V R_{SNS} = 1kΩ, R_L = 2.6Ω			180	µs
$t_{SNSIOFF1}$	Settling time from falling edge of DIA_EN	V_{EN} = 5V, V_{DIA_EN} = 5V to 0V R_{SNS} = 1kΩ, R_L = 2.6Ω			20	µs
$t_{SETTLEH}$	Settling time from rising edge of load step	V_{EN} = 5V, V_{DIA_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 1A to 5A			20	µs
$t_{SETTLEL}$	Settling time from falling edge of load step	V_{EN} = 5V, V_{DIA_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 5A to 1A			20	µs
SNS TIMING - TEMPERATURE SENSE						
$t_{SNSTON1}$	Settling time from rising edge of DIA_EN	V_{EN} = 5V, V_{DIA_EN} = 0V to 5V R_{SNS} = 1kΩ			40	µs
$t_{SNSTON2}$	Settling time from rising edge of DIA_EN	V_{EN} = 0V,$_{VDIA\_EN}$ = 0V to 5V R_{SNS} = 1kΩ			70	µs
$t_{SNSTOFF}$	Settling time from falling edge of DIA_EN	V_{EN} = X, V_{DIA_EN} = 5V to 0V R_{SNS} = 1kΩ			20	µs
SNS TIMING - VOLTAGE SENSE						
$t_{SNSVON1}$	Settling time from rising edge of DIA_EN	V_{EN} = 5V, V_{DIA_EN} = 0V to 5V R_{SNS} = 1kΩ			40	µs
$t_{SNSVON2}$	Settling time from rising edge of DIA_EN	V_{EN} = 0V, V_{DIA_EN} = 0V to 5V R_{SNS} = 1kΩ			70	µs
$t_{SNSVOFF}$	Settling time from falling edge of DIA_EN	V_{EN} = X, V_{DIA_EN} = 5V to 0V R_{SNS} = 1kΩ			20	µs
SNS TIMING - MULTIPLEXER						

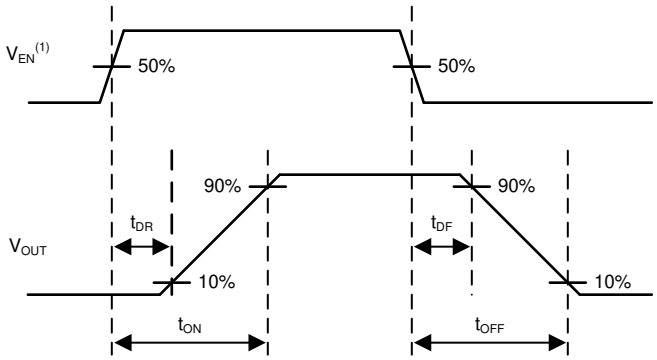
V_{BB} = 8 to 18V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{MUX}	Settling time from temperature sense to current sense	V_{EN}= X, V_{DIA_EN} = 5V V_{SEL1} = 5V to 0V, V_{SEL2} = 0V R_{SNS} = 1kΩ, R_L = 2.6Ω			60	µs
	Settling time from temperature sense to voltage sense	V_{EN} = X, V_{DIA_EN} = 5V V_{SEL1} = 5V, V_{SEL2} = 0V to 5V R_{SNS} = 1kΩ			60	µs
	Settling time from voltage sense to temperature sense	V_{EN} = X, V_{DIA_EN} = 5V V_{SEL1} = 5V, V_{SEL2} = 5V to 0V R_{SNS} = 1kΩ			60	µs
	Settling time from voltage sense to current sense	V_{EN} = X, V_{DIA_EN} = 5V V_{SEL1} = V_{SEL2} = 5V to 0V, R_{SNS} = 1kΩ, R_L = 2.6Ω			60	µs
	Settling time from current sense to temperature sense	V_{EN} = X, V_{DIA_EN} = 5V V_{SEL1} = 0V to 5V, V_{SEL2} = 0V R_{SNS} = 1kΩ, R_L = 2.6Ω			60	µs
	Settling time from current sense to voltage sense	V_{EN} = X, V_{DIA_EN} = 5V V_{SEL1} = V_{SEL2} = 0V to 5V R_{SNS} = 1kΩ, R_L = 2.6Ω			60	µs



Rise and fall times of control signals are 100ns. Control signals include: EN, DIA_EN, SEL1, SEL2.
Set SEL1 and SEL2 to the appropriate values.
Use the temperature sense timing diagram to depict the voltage sense timings.

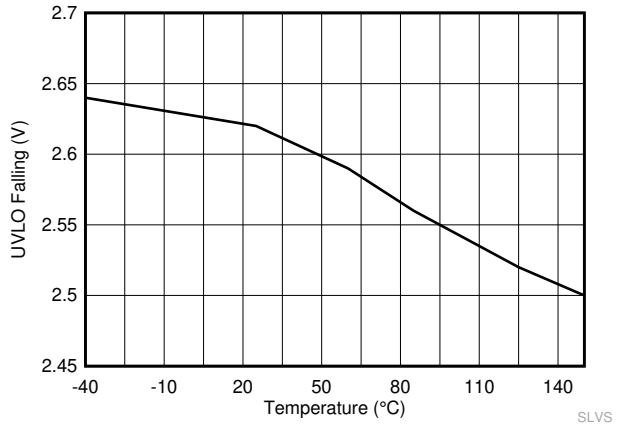
Figure 6-1. SNS Timing Characteristics Definitions



Rise and fall time of V_{EN} is 100ns.

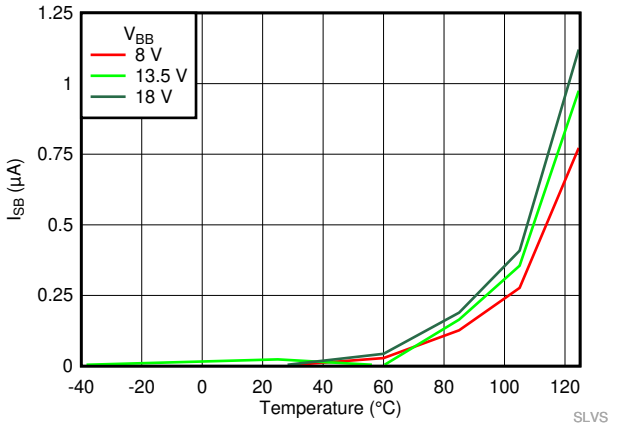
Figure 6-2. Switching Characteristics Definitions

6.8 Typical Characteristics



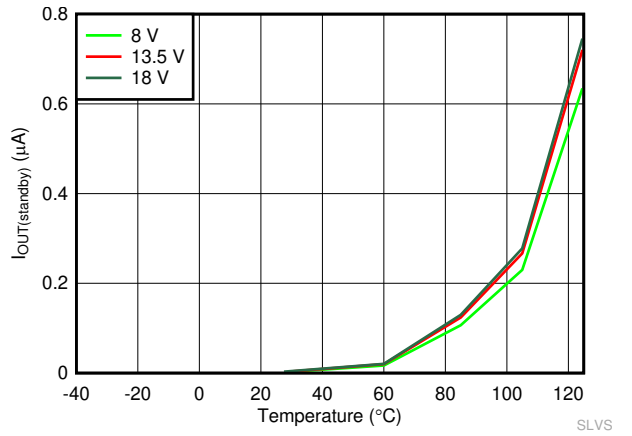
V_{BB} = 13.5V to 0V R_{OUT} = 1kΩ V_{DIAG_EN} = 0V
V_{EN} = 5V

Figure 6-3. Falling Undervoltage Lockout (V_{UVLOF}) vs Temperature



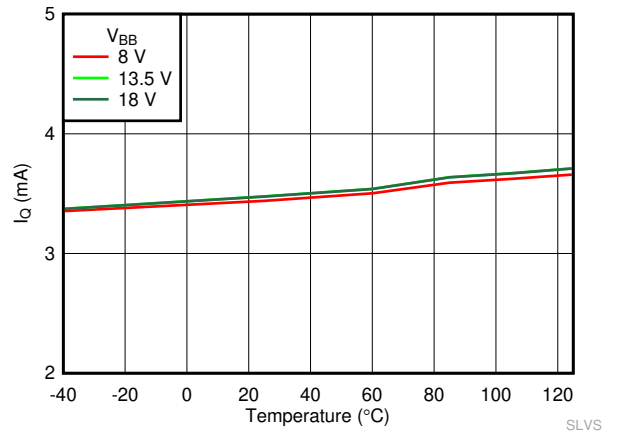
V_{OUT} = 0V V_{EN} = 0V V_{DIAG_EN} = 0V

Figure 6-4. Standby Current (I_{SB}) vs Temperature



V_{OUT} = 0V V_{EN} = 0V V_{DIAG_EN} = 0V

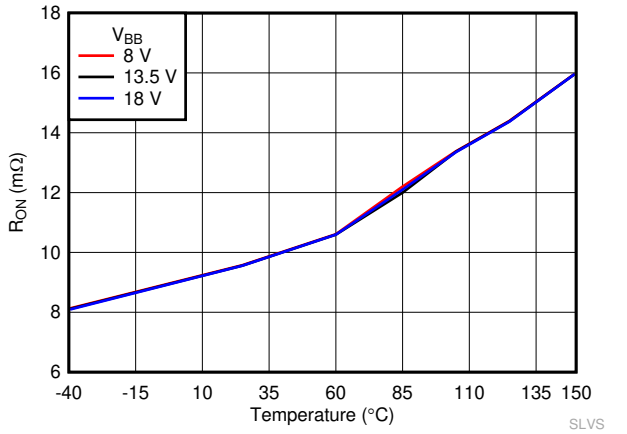
Figure 6-5. Output Leakage Current ($I_{OUT(standby)}$) vs Temperature



I_{OUT} = 0A V_{EN} = 5V V_{DIAG_EN} = 5V
R_{SNS} = 1kΩ V_{SEL1} = V_{SEL2} = 0V

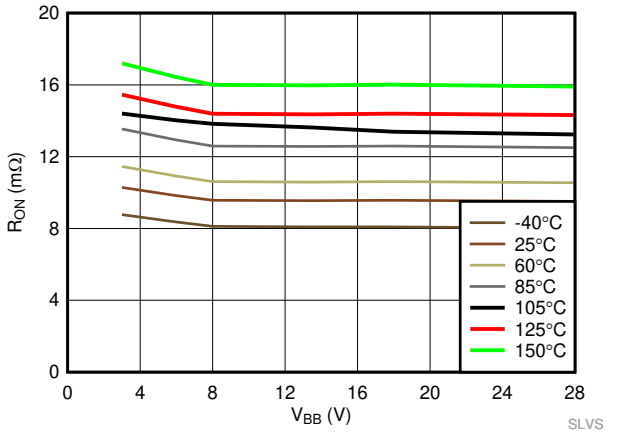
Figure 6-6. Quiescent Current (I_Q) vs Temperature

6.8 Typical Characteristics (continued)



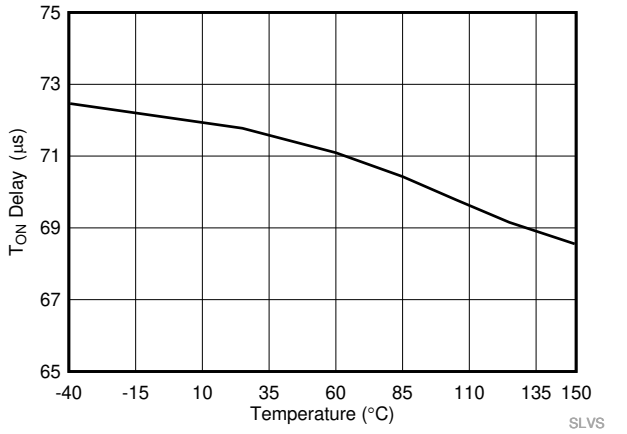
I_{OUT} = 200mA V_{EN} = 5V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ

Figure 6-7. On Resistance (R_{ON}) vs Temperature



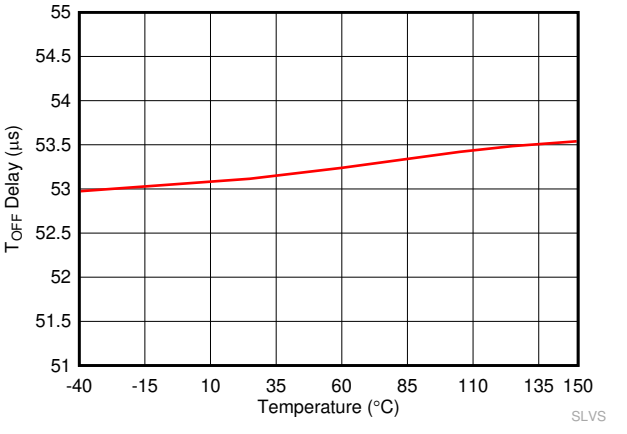
I_{OUT} = 200mA V_{EN} = 5V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

Figure 6-8. On Resistance (R_{ON}) vs V_{BB}



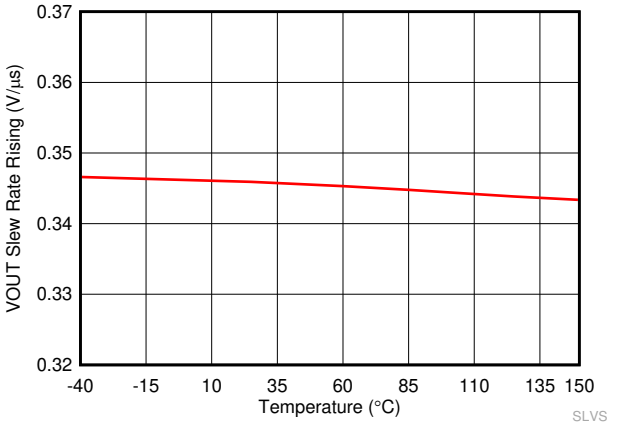
R_{OUT} = 2.6Ω V_{EN} = 0V to 5V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

Figure 6-9. Turn-on Delay Time (t_{DR}) vs Temperature



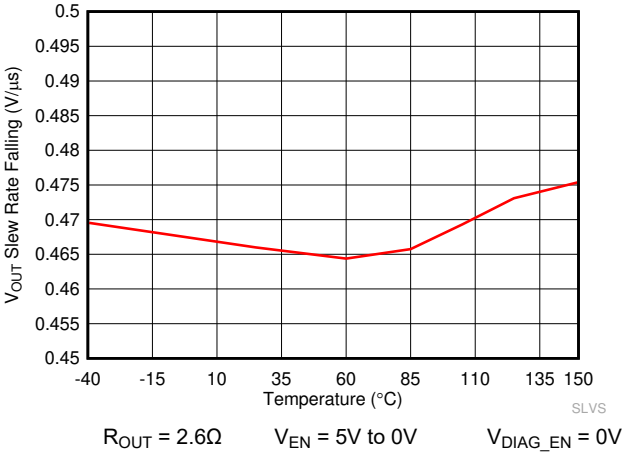
R_{OUT} = 2.6Ω V_{EN} = 5V to 0V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

Figure 6-10. Turn-off Delay Time (t_{DF}) vs Temperature



R_{OUT} = 2.6Ω V_{EN} = 0V to 5V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

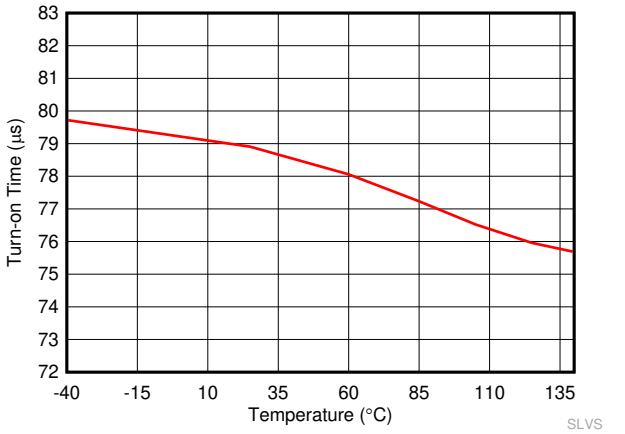
Figure 6-11. V_{OUT} Slew Rate Rising (SR_R) vs Temperature



R_{OUT} = 2.6Ω V_{EN} = 5V to 0V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

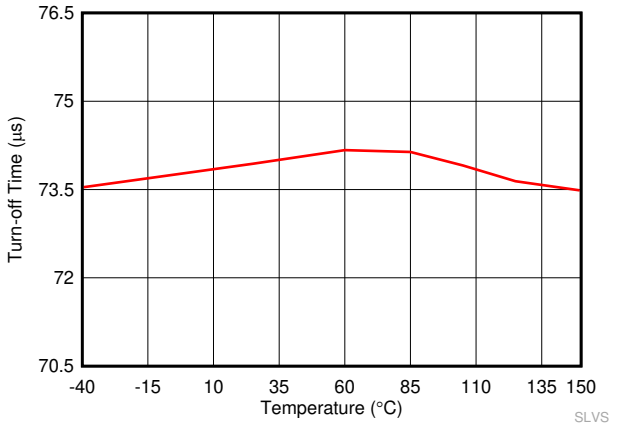
Figure 6-12. V_{OUT} Slew Rate Falling (SR_F) vs Temperature

6.8 Typical Characteristics (continued)



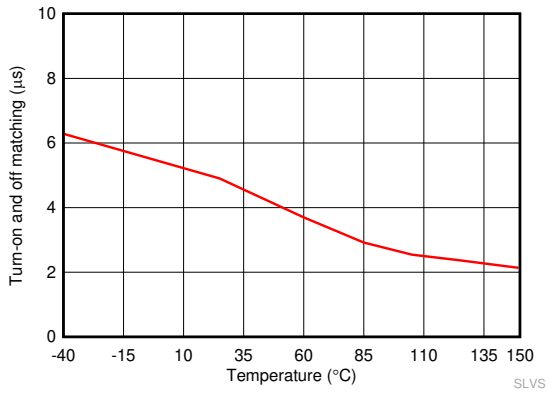
R_{OUT} = 2.6Ω V_{EN} = 0V to 5V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

Figure 6-13. Turn-on Time (t_{ON}) vs Temperature



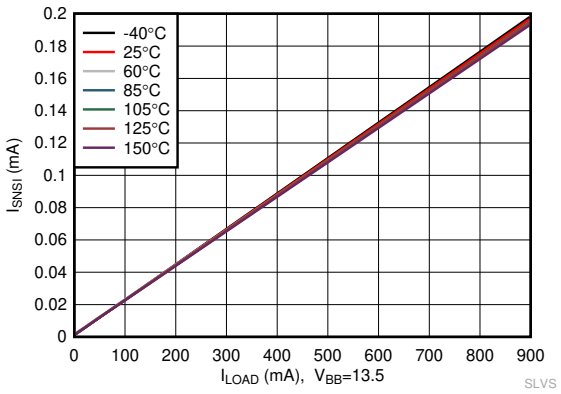
R_{OUT} = 2.6Ω V_{EN} = 5V to 0V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

Figure 6-14. Turn-off Time (t_{OFF}) vs Temperature



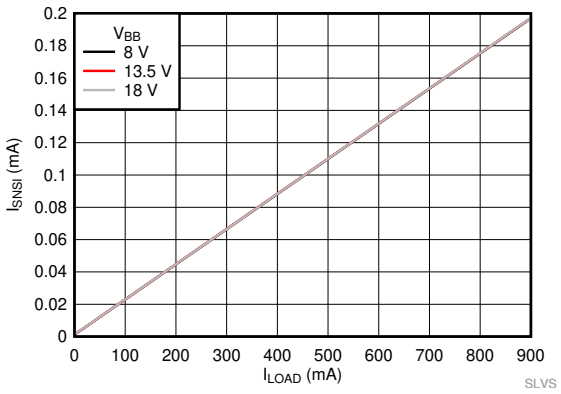
R_{OUT} = 2.6Ω V_{EN} = 0V to 5V and from 5V to 0V V_{DIAG_EN} = 0V
R_{SNS} = 1kΩ V_{BB} = 13.5V

Figure 6-15. Turn-on and Turn-off Matching (t_{ON} - t_{OFF}) vs Temperature



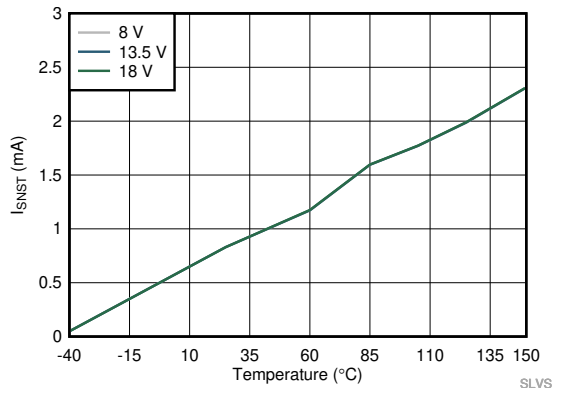
V_{SEL1} = V_{SEL2} = 0V V_{EN} = 5V V_{DIAG_EN} = 5V
R_{SNS} = 1kΩ V_{BB} = 13.5V

Figure 6-16. Current Sense Output Current (I_{SNSI}) vs Load Current (I_{OUT}) across Temperature



V_{SEL1} = V_{SEL2} = 0V V_{EN} = 5V V_{DIAG_EN} = 5V
R_{SNS} = 1kΩ T_A = 25°C

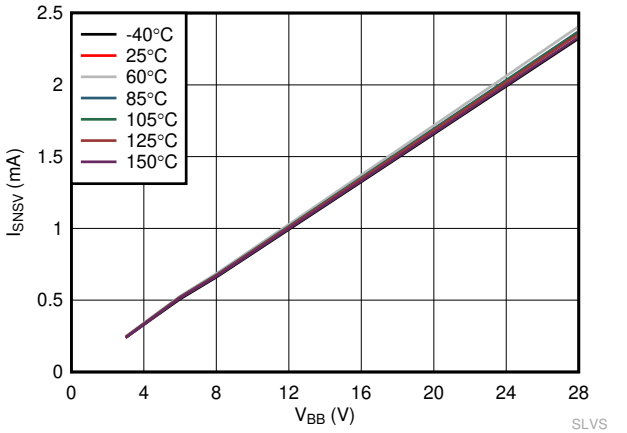
Figure 6-17. Current Sense Output Current (I_{SNSI}) vs Load Current (I_{OUT}) across V_{BB}



V_{SEL1} = 5V V_{SEL2} = 0V V_{DIAG_EN} = 5V
R_{SNS} = 1kΩ V_{EN} = 0V

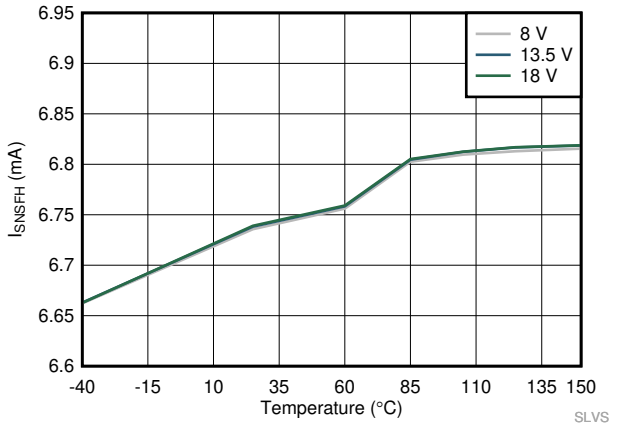
Figure 6-18. Temperature Sense Output Current (I_{SNST}) vs Temperature

6.8 Typical Characteristics (continued)



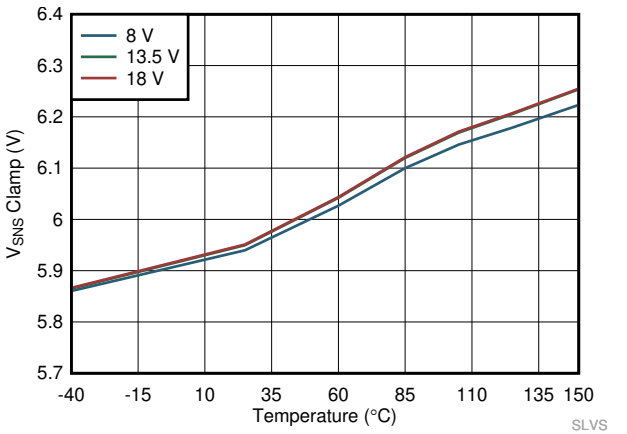
V_{SEL1} = V_{SEL2} = 5V | V_{EN} = 0V | V_{DIAG_EN} = 5V
R_{SNS} = 1kΩ | I_{OUT} = 0A

Figure 6-19. Voltage Sense Output Current (I_{SNSV}) vs V_{BB}



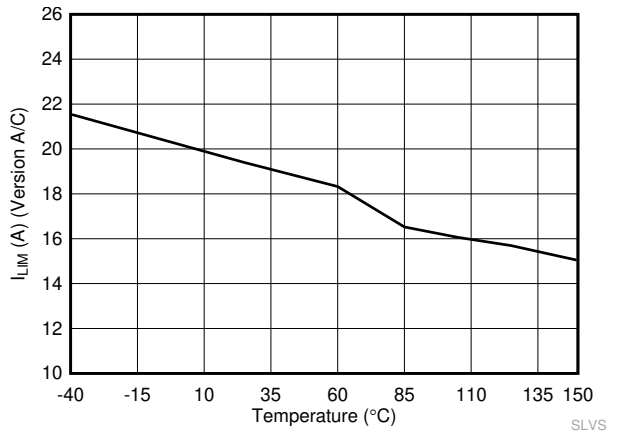
V_{SEL1} = V_{SEL2} = 0V | V_{EN} = 0V | V_{DIAG_EN} = 5V
R_{SNS} = 500Ω | V_{OUT} Floating

Figure 6-20. Fault High Output Current (I_{SNSFH}) vs Temperature



V_{SEL1} = V_{SEL2} = 0V | V_{EN} = 5V | V_{DIAG_EN} = 5V
R_{SNS} = 10kΩ | I_{OUT} = 4A

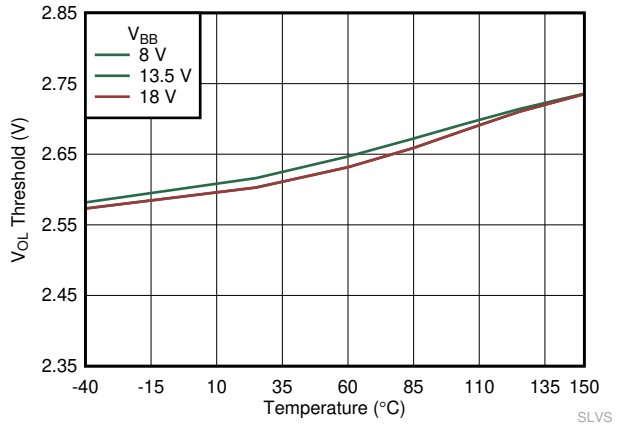
Figure 6-21. Sense Pin Clamp Voltage ($V_{SNSCLAMP}$) vs Temperature



V_{BB} = 13.5V | V_{OUT} = 0V | V_{DIAG_EN} = 0V
Device Version C | V_{EN} = 5V | V_{LATCH} = 5V

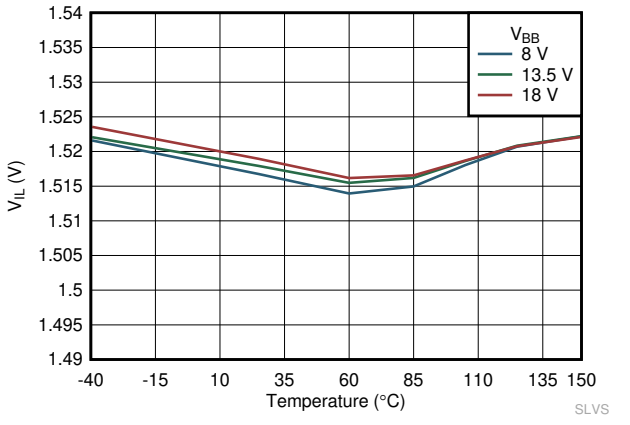
Figure 6-22. Current Limit (I_{CL}) vs Temperature

6.8 Typical Characteristics (continued)



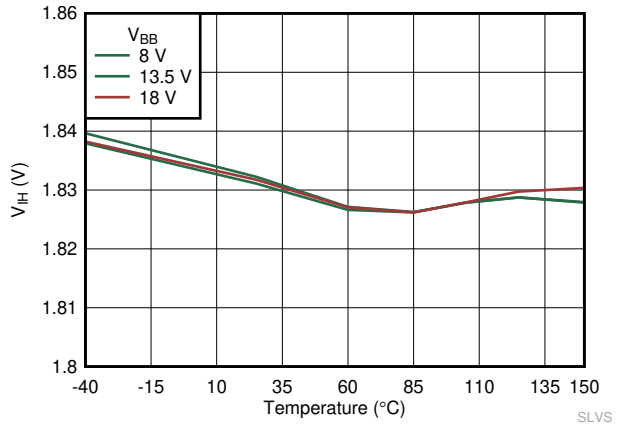
V_{EN} = 0V V_{OUT} = 0V to 5V I_{OUT} = 0A
V_{DIAG_EN}= 5V V_{SEL1} = V_{SEL2} = 0V

Figure 6-23. Open Load Detection Voltage (V_{OL}) vs Temperature



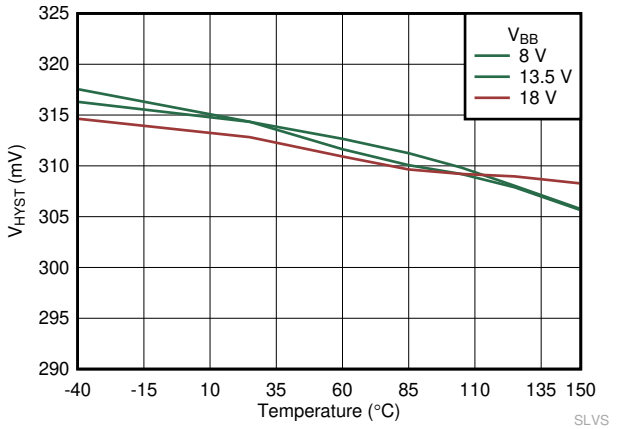
V_{EN} = 3.3V to 0V V_{OUT} = 0V V_{DIAG_EN} = 0V
R_{OUT} = 1kΩ

Figure 6-24. V_{IL} vs Temperature



V_{EN} = 0V to 3.3V V_{OUT} = 0V V_{DIAG_EN} = 0V
R_{OUT} = 1kΩ

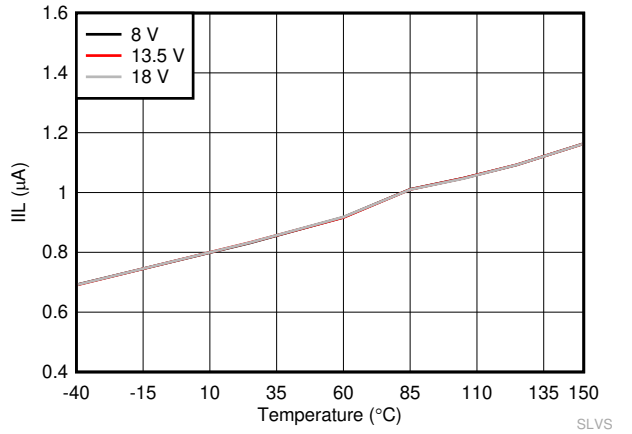
Figure 6-25. V_{IH} vs Temperature



V_{EN} = 0V to 3.3V and from 3.3V to 0V V_{OUT} = 0V V_{DIAG_EN} = 0V
R_{OUT} = 1kΩ

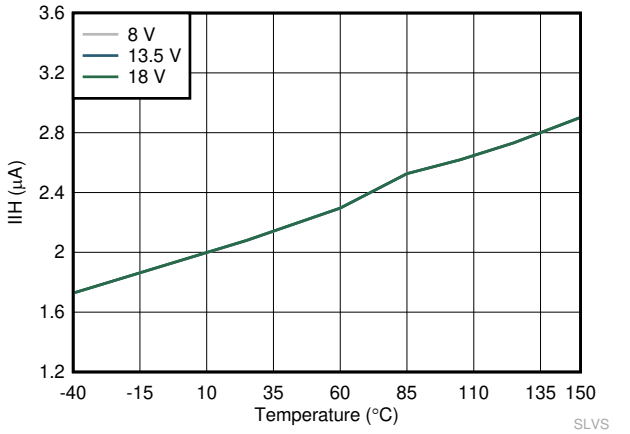
Figure 6-26. V_{IHYS} vs Temperature

6.8 Typical Characteristics (continued)



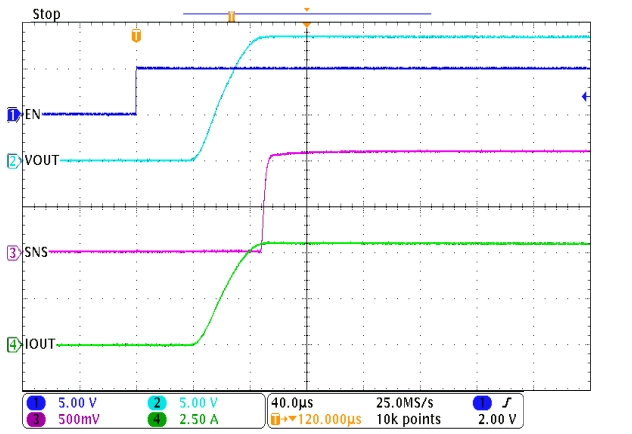
V_{EN} = 0.8V V_{OUT} = 0V V_{DIAG_EN} = 0V
R_{OUT} = 1kΩ

Figure 6-27. I_{IL} vs Temperature



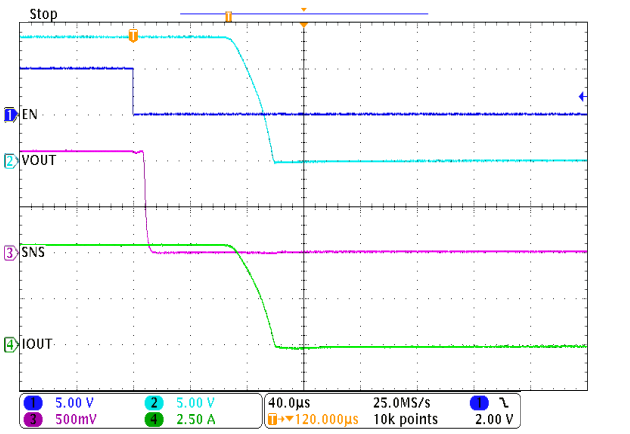
V_{EN} = 2V V_{OUT} = 0V V_{DIAG_EN} = 0V
R_{OUT} = 1kΩ

Figure 6-28. I_{IH} vs Temperature



R_{OUT} = 2.6Ω R_{SNS} = 1kΩ V_{DIA_EN} = 5V
V_{SEL1} = V_{SEL2} = 0V

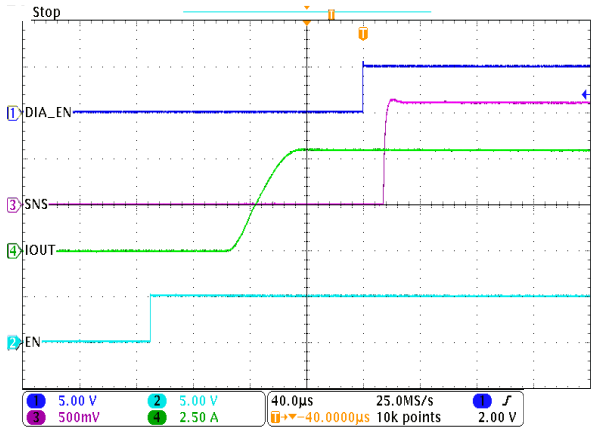
Figure 6-29. Turn-on Time (t_{ON})



R_{OUT} = 2.6Ω R_{SNS} = 1kΩ V_{DIA_EN} = 5V
V_{SEL1} = V_{SEL2} = 0V

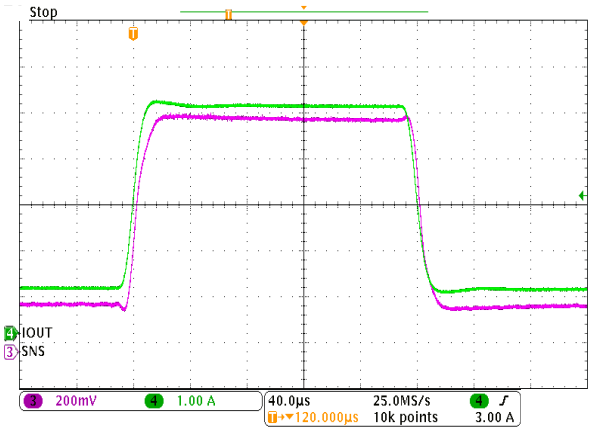
Figure 6-30. Turn-off Time (t_{OFF}) and Sense Settle Time ($t_{SNSION2}$)

6.8 Typical Characteristics (continued)



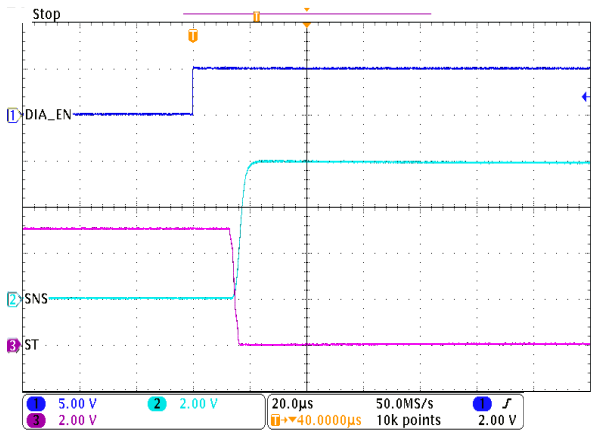
R_{OUT} = 2.6Ω R_{SNS} = 1kΩ V_{DIA_EN}= 0V to 5V
V_{SEL1} = V_{SEL2} = 0V

Figure 6-31. I_{SNS} Settling Time ($t_{SNSION1}$) on DIA_EN Transition



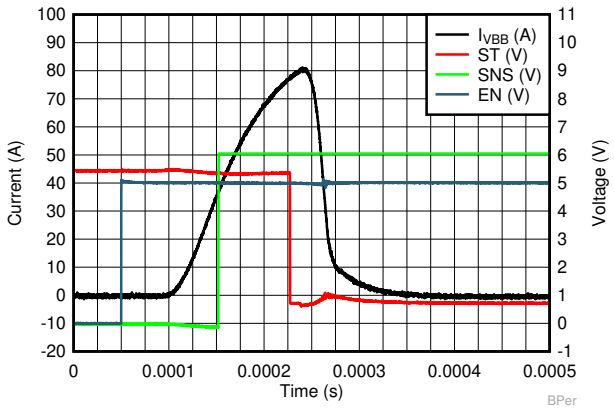
I_{OUT} = 1A to 5A R_{SNS} = 1kΩ V_{DIA_EN} = 5V
V_{SEL1} = V_{SEL2} = 0V

Figure 6-32. I_{SNS} Settling Time ($t_{SETTLEH}$) on Rising Load Step



V_{OUT} = V_{BB} R_{SNS} = 1kΩ V_{SEL1} = V_{SEL2} = 0V
V_{EN} = 0V V_{DIAG_EN} = 5V

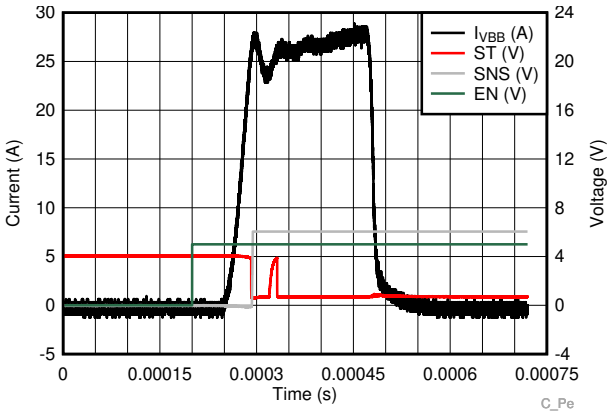
Figure 6-33. Open Load Detection Time (t_{OL2}) on Rising DIAG_EN



V_{BB} = 13.5V B Device Version V_{OUT} = 0V
V_{EN} = 0V to 5V T_A = 25°C

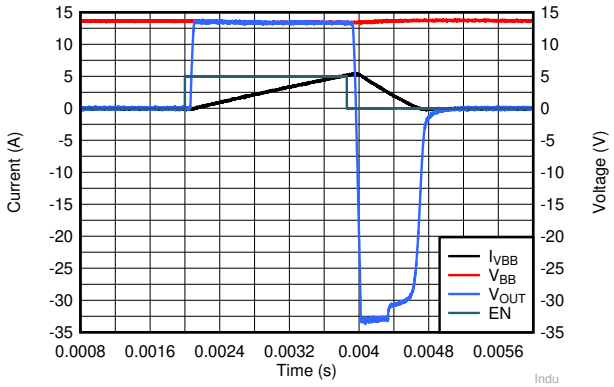
Figure 6-34. Short Circuit Behavior with B Device Version

6.8 Typical Characteristics (continued)



V_{BB} = 13.5V C Device Version V_{OUT} = 0V
V_{EN} = 0V to 5V T_A = 25°C

Figure 6-35. Short Circuit Behavior with C Device Version



V_{BB} = 13.5V T_A = 125°C L_{OUT} = 5mH
V_{EN} = 0V to 5V, 5V to 0V

Figure 6-36. Inductive Load Demagnetization

7 Parameter Measurement Information

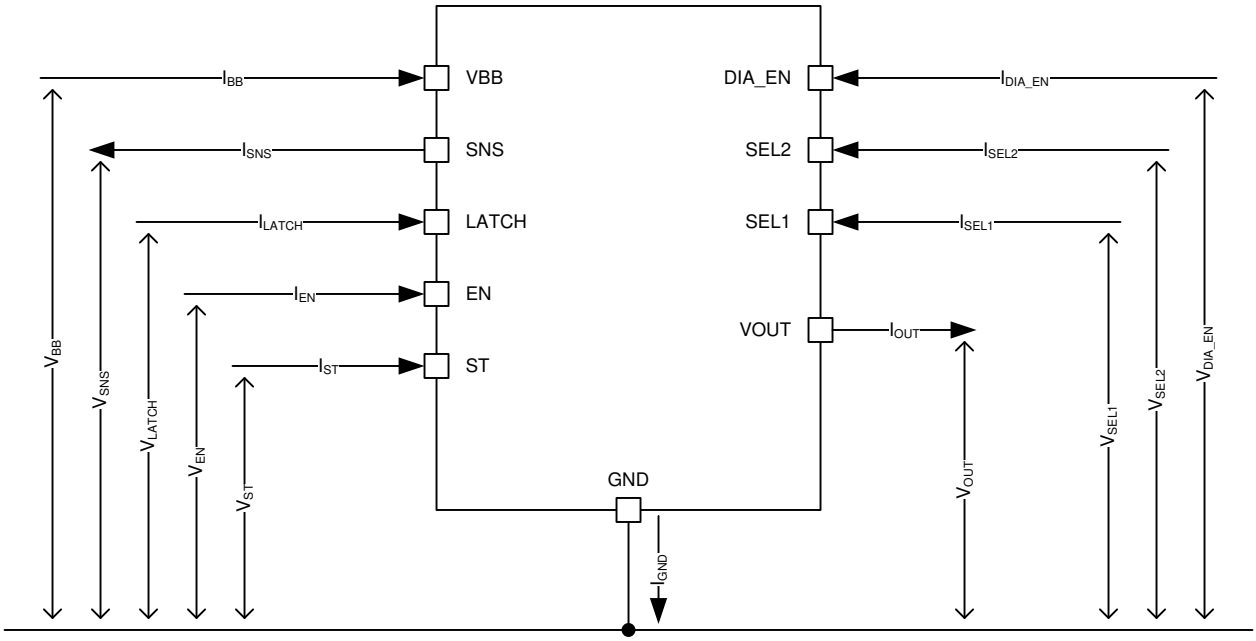


Figure 7-1. Parameter Definitions

8 Detailed Description

8.1 Overview

The TPS1HA08-Q1 device is a single-channel smart high-side power switch intended for use with 12V automotive batteries. Many protection and diagnostic features are integrated in the device.

Diagnostics features include the analog SNS output and the open-drain fault indication ($\overline{ST}$). The analog SNS output is capable of providing a signal that is proportional to device temperature, supply voltage, or load current. The high-accuracy load current sense allows for diagnostics of complex loads.

This device includes protection through thermal shutdown, current limit, transient withstand, and reverse battery operation. For more details on the protection features, refer to the *Feature Description* and *Application Information* sections of the document.

8.1.1 Device Nomenclature

The TPS1HA08-Q1 is one device in the TI family of Smart High Side Switches. Figure 8-1 shows the family part number nomenclature and explains how to determine device characteristics from the part number for TI Smart High Side Switches.

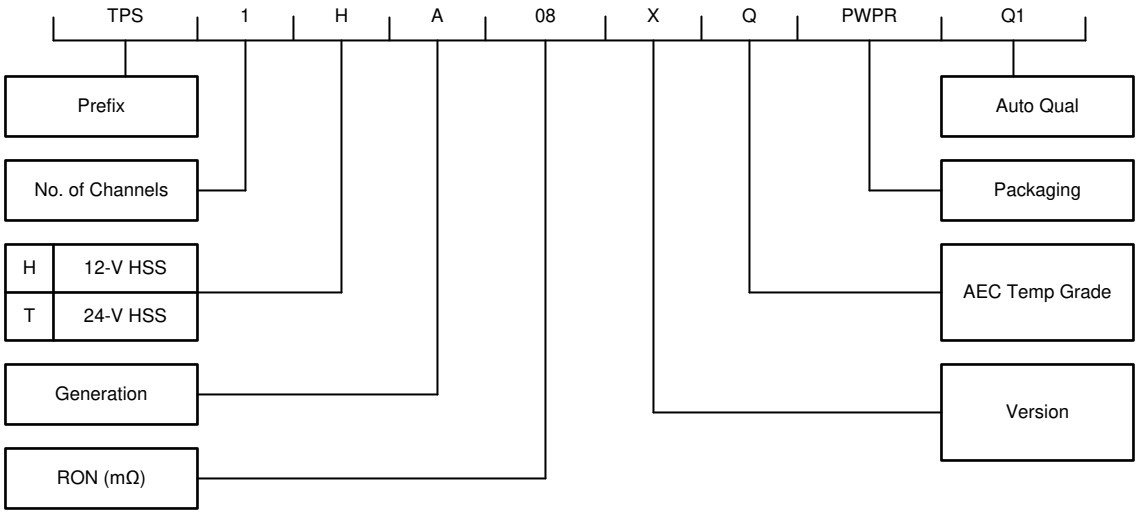
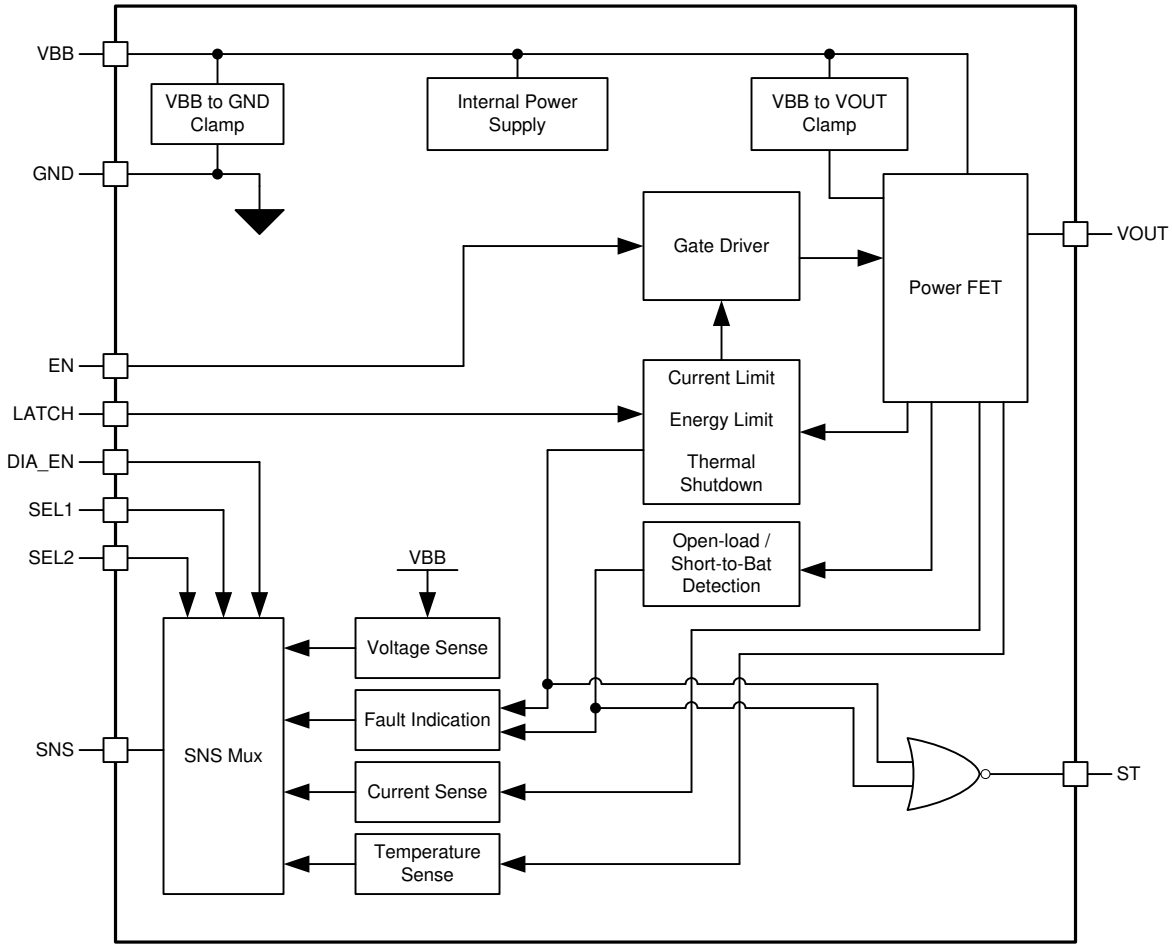


Figure 8-1. Naming Convention

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protection Mechanisms

The TPS1HA08-Q1 is designed to operate in the automotive environment. The protection mechanisms allow the device to be robust against many system-level events such as load dump, reverse battery, short-to-ground and more.

There are three protection features which, if triggered, cause the switch to automatically disable:

- Thermal Shutdown
- Current Limit (Versions A,B,E)
- Energy Limit

When any of these protections are triggered, the device enters the FAULT state. In the FAULT state, the fault indication is available on both the SNS pin and the $\overline{ST}$ pin (see the diagnostic section of the data sheet for more details).

The switch is no longer held off and the fault indication is reset when all of the below conditions are met:

- LATCH pin is low
- t_{RETRY} has expired
- All faults are cleared (thermal shutdown, current limit, energy limit)

8.3.1.1 Thermal Shutdown

The TPS1HA08-Q1 includes temperature sensors on the FET and inside of the device controller. When $T_{J,FET} > T_{ABS}$, the device sees a thermal shutdown fault. After the fault is detected, the switch turns off. The fault is cleared when the switch temperature decreases by the hysteresis value, T_{HYS}.

8.3.1.2 Current Limit

When I_{OUT} reaches the current limit threshold, I_{CL}, the device can switch off immediately (Versions A,B,E), or the device can remain enabled and limit I_{OUT} (Versions C/D) to I_{CL} (see *Device Comparison Table* section for more details). In the case that the device remains enabled and limits I_{OUT}, the thermal shutdown or energy limit protection feature can trigger due to the high amount of power dissipation in the device.

During a short-circuit event, the device hits the I_{CL} threshold that is listed in the *Specifications* (for the given device version) and then turns the output off or regulate the output current to protect the device. The device registers a short-circuit event when the output current exceeds I_{CL}, however the measured maximum current can exceed the I_{CL} threshold due to the TPS1HA08-Q1 deglitch filter and turn-off time. The device is specified to protect itself during a short-circuit event over the nominal supply voltage range (as defined in the *Specifications* section) at 125°C.

8.3.1.2.1 Current Limit Foldback

The TPS1HA08-Q1 implements a current limit foldback feature that is designed to protect the device in the case of a long-term fault condition. If the device undergoes three consecutive fault shutdown events (any of thermal shutdown, current limit, or energy limit), the current limit is reduced to half of the original value. The device reverts back to the original current limit threshold if either of the following occurs:

- The device goes to *Standby Delay*.
- The switch turns on and turns off without any fault occurring.

8.3.1.2.2 Selectable Current Limit Threshold

The TPS1HA08-Q1 offers two current limit thresholds. The high threshold is designed to allow for a large transient load current (for example, inrush current of a 65W bulb). The low threshold is designed to provide improved system-level protection for loads that do not have large transient currents (for example, heating element). The lower threshold can allow for reduced size and cost in the current carrying components such as PCB traces and module connectors. Version A (20A current limit) is an excellent choice for charging capacitors, as it enables the device to prevent inrush current and clamp the overcurrent to linearly charge the capacitor.

8.3.1.2.3 Undervoltage Lockout (UVLO)

The device monitors the supply voltage V_{BB} to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{UVLOF}, the output stage is shut down automatically. When the supply rises up to V_{UVLOR}, the device turns back on.

During an initial ramp of V_{BB} from 0V at a ramp rate slower than 1V/ms, V_{EN} pin has to be held low until V_{BB} is above UVLO threshold (with respect to board ground) and the supply voltage to the device has reliably reached above the UVLO condition. For best operation, ensure that V_{BB} has risen above UVLO before setting the V_{EN} pin to high.

8.3.1.2.4 V_{BB} during Short-to-Ground

When V_{OUT} is shorted to ground, the module power supply (V_{BB}) can have a transient decrease. This decrease is caused by the sudden increase in current flowing through the wiring harness cables. To achieve peak system behavior, TI recommends that the module maintain $V_{BB} > 3V$ during V_{OUT} short-to-ground. This is typically accomplished by placing bulk capacitance on the power supply node.

8.3.1.3 Energy Limit

The energy limiting feature is implemented to protect the switch from excessive stress. The device continuously monitors the amount of energy dissipated in the FET. If the energy limit threshold is reached, the switch automatically disables. In practice, the energy limit is only reached during a fault event such as short-to-ground.

Energy limit events have the same system-level behavior as thermal shutdown events.

8.3.1.4 Voltage Transients

The TPS1HA08-Q1 contains two voltage clamps which protect the device against system-level voltage transients.

The clamp from V_{BB} to GND is primarily used to protect the controller from positive transients on the supply line (for example, ISO7637-2). The clamp from V_{BB} to V_{OUT} is primarily used to limit the voltage across the FET when switching off an inductive load. Both clamp levels are set to protect the device during these fault conditions. If the voltage potential from V_{BB} to GND exceeds the V_{BB} clamp level, the clamp allows current to flow through the device from V_{BB} to GND (Path 2). If the voltage potential from V_{BB} to V_{OUT} exceeds V_{CLAMP}, the power FET allows current to flow from V_{BB} to V_{OUT} (Path 3).

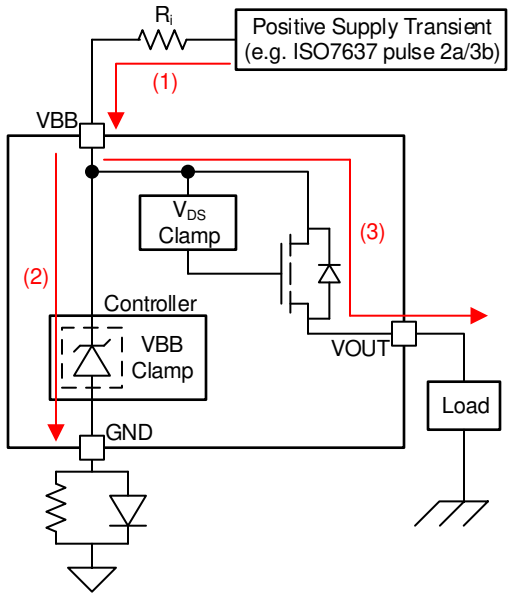


Figure 8-2. Current Path During Supply Voltage Transient

8.3.1.4.1 Load Dump

The TPS1HA08-Q1 is tested according to ISO 16750-2:2010(E) suppressed load dump pulse. The device supports up to 40V load dump transient. The switch maintains normal operation during the load dump pulse. If the switch is enabled, it stays enabled. If the switch is disabled, it stays disabled.

8.3.1.4.2 Driving Inductive and Capacitive Loads

When switching off an inductive load, the inductor can impose a negative voltage on the output of the switch. The TPS1HA08-Q1 includes a voltage clamp to limit voltage across the FET. The maximum acceptable load inductance is a function of the device robustness. With a 5mH load, the TPS1HA08-Q1 can withstand one pulse of 95mJ inductive dissipation at 125°C and can withstand 56mJ of inductive dissipation with a 10Hz repetitive pulse. If the application parameters exceed this device limit, it use a protection device like a freewheeling diode to dissipate the energy stored in the inductor. Figure 8-3 shows the TPS1HA08-Q1 discharging a 5mH load that is driven at 5A.

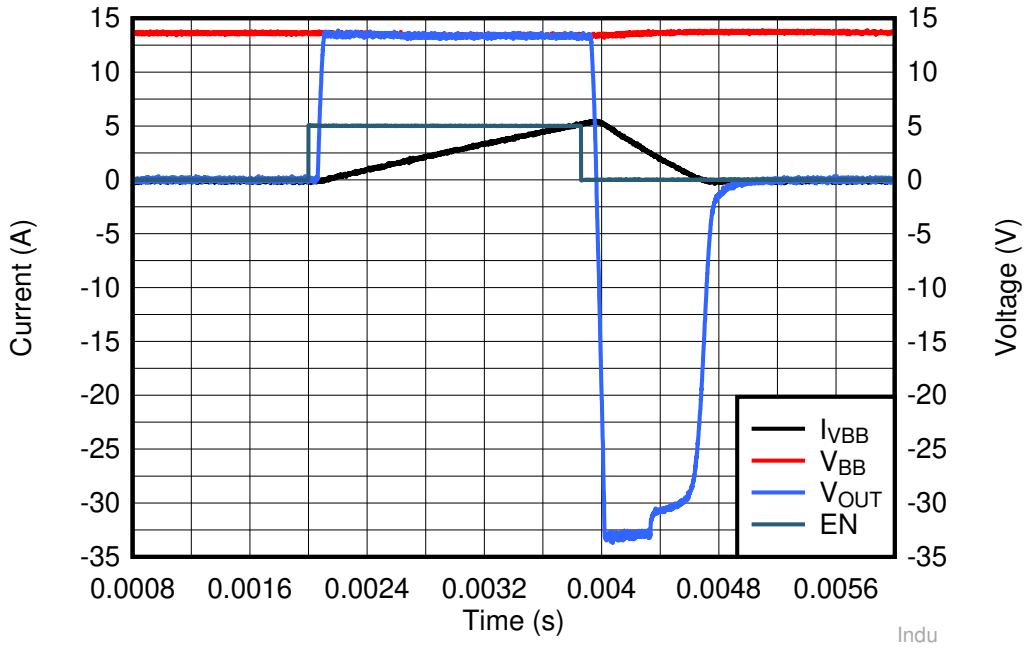


Figure 8-3. Inductive Discharge (5mH, 5A)

This device is not designed for charging large capacitive loads. During capacitive inrush events, energy is dissipated across the internal FET, which may cause the device to enter a fault condition and turn off. If auto-retry is enabled, the device may successfully charge the capacitive load after several retry attempts; however, the time required and the number of retries before the load is fully charged can vary significantly across devices. For applications requiring capacitive load charging, it is recommended to use TI's latest generation of high side switches, which are specifically designed for this purpose.

For more information on driving inductive or capacitive loads, reference *TI's "How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switch* application note.

8.3.1.5 Reverse Battery

In the reverse battery condition, the switch is automatically enabled (regardless of EN status) to prevent power dissipation inside the MOSFET body diode. In many applications (for example, resistive load), the full load current can be present during reverse battery. To activate the automatic switch on feature, the SEL2 pin must have a path to module ground. This can be path 1 as shown below, or, if the SEL2 pin is unused, the path can be through R_{PROT} to module ground.

Protection features (for example, thermal shutdown) are not available during reverse battery. Take care to verify that excessive power is not dissipated in the switch during the reverse battery condition.

There are two options for blocking reverse current in the system. Option 1 is to place a blocking device (FET or diode) in series with the battery supply. This method blocks all current paths. Option 2 is to place a blocking diode in series with the GND node of the high-side switch. This method protects the controller portion of the switch (path 2), but it does not prevent current from flowing through the load (path 3). The diode used for Option 2 can be shared amongst multiple high-side switches.

Path 1 shown in Figure 8-4 is blocked inside of the device.

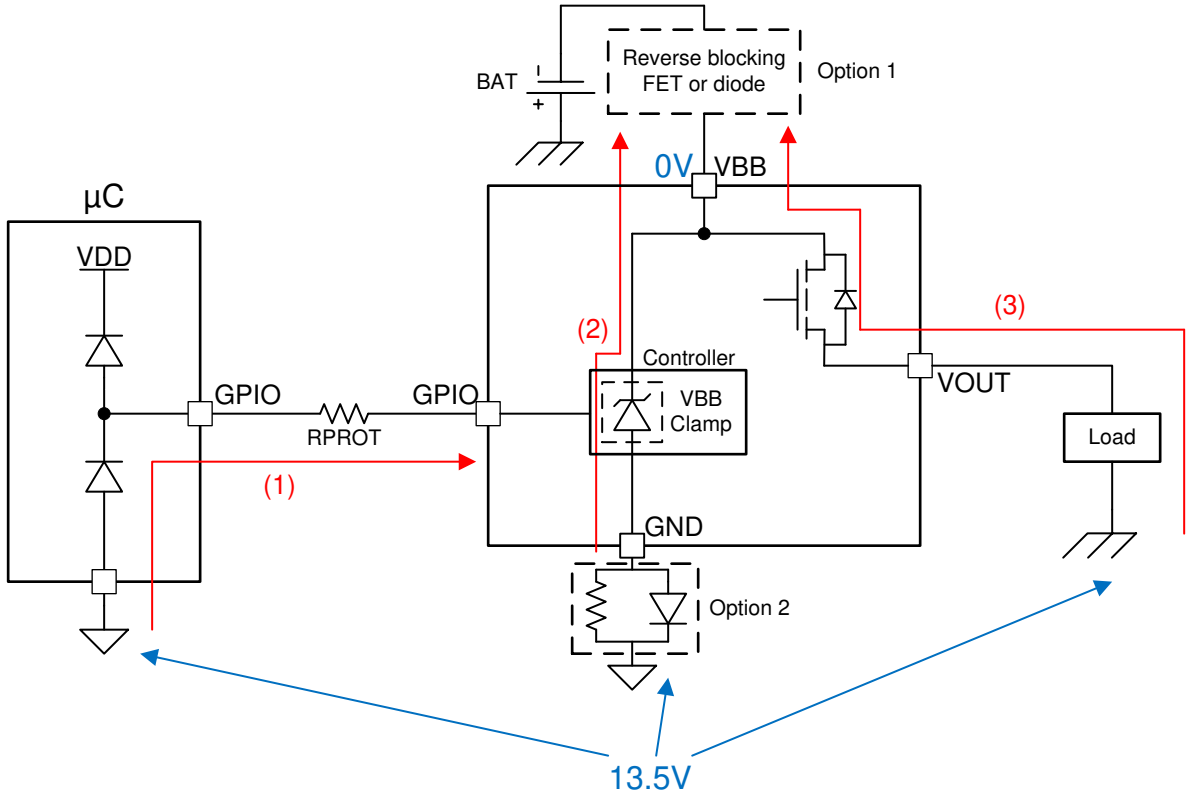


Figure 8-4. Current Path During Reverse Battery

8.3.1.6 Fault Event – Timing Diagrams

Note

All timing diagrams assume that the SELx pins are set to 00.

The user controls the LATCH, DIA_EN, and EN pins. The timing diagrams represent a possible use case.

Figure 8-5 shows the immediate current limit switch off behavior of Versions A,B,E. The diagram also shows the retry behavior. As shown, the switch remains latched off until the LATCH pin is low.

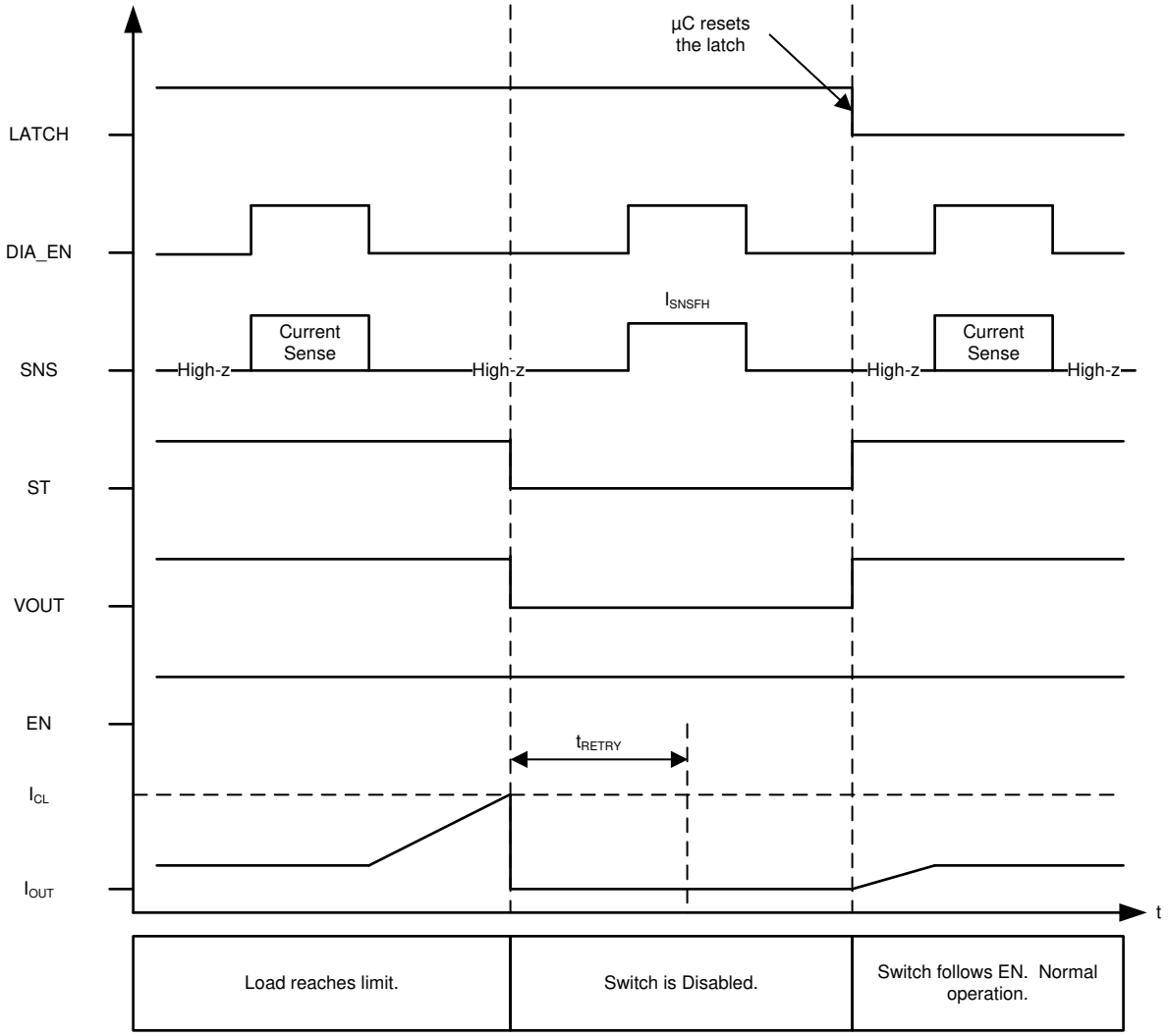


Figure 8-5. Current Limit – Version A, B, E - Latched Behavior

Figure 8-6 shows the immediate current limit switch off behavior of versions A,B,E. In this example, LATCH is tied to GND; hence, the switch retries after the fault is cleared and t_{RETRY} has expired.

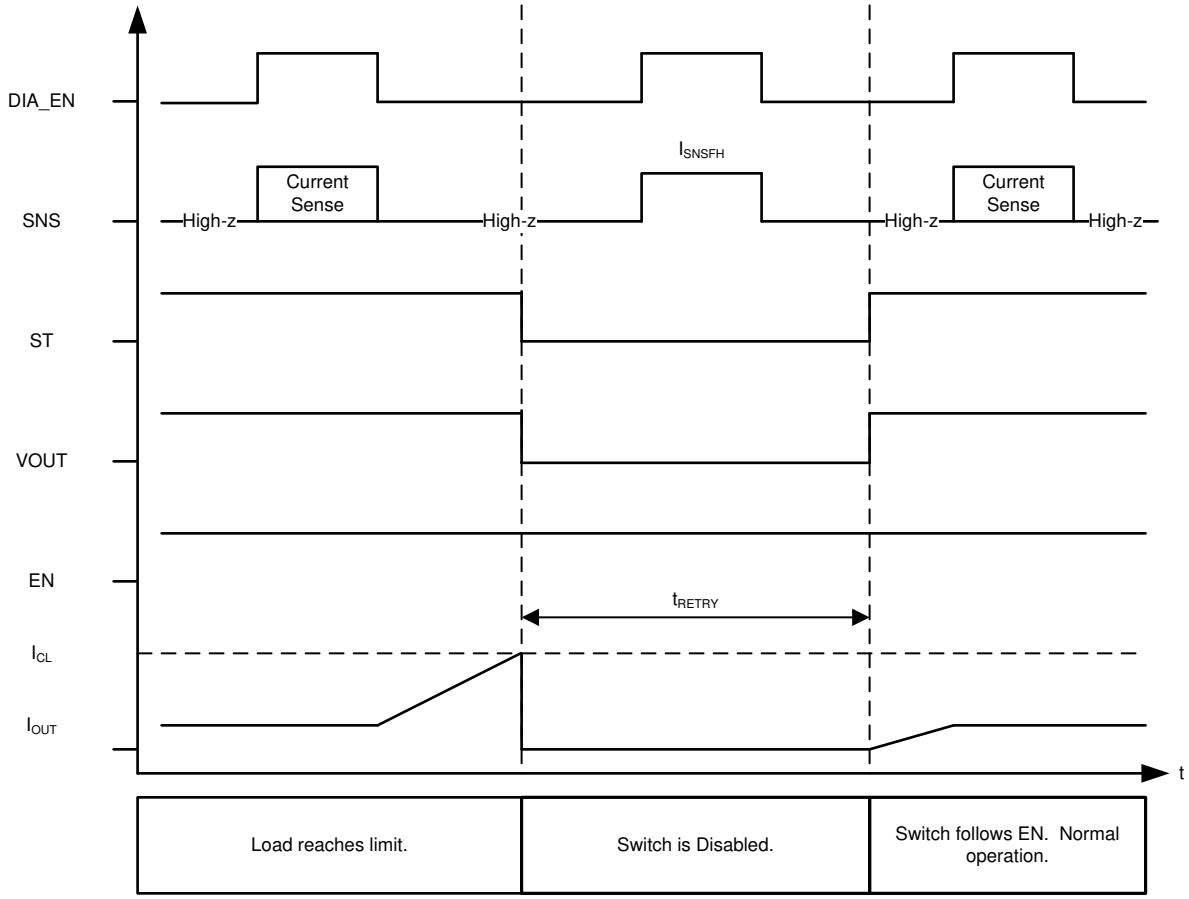


Figure 8-6. Current Limit – Version A, B, E - LATCH = 0

Figure 8-7 shows the active current limiting behavior of versions C, D. In versions C, D, the switch does not shutdown until either the energy limit or the thermal shutdown is reached.

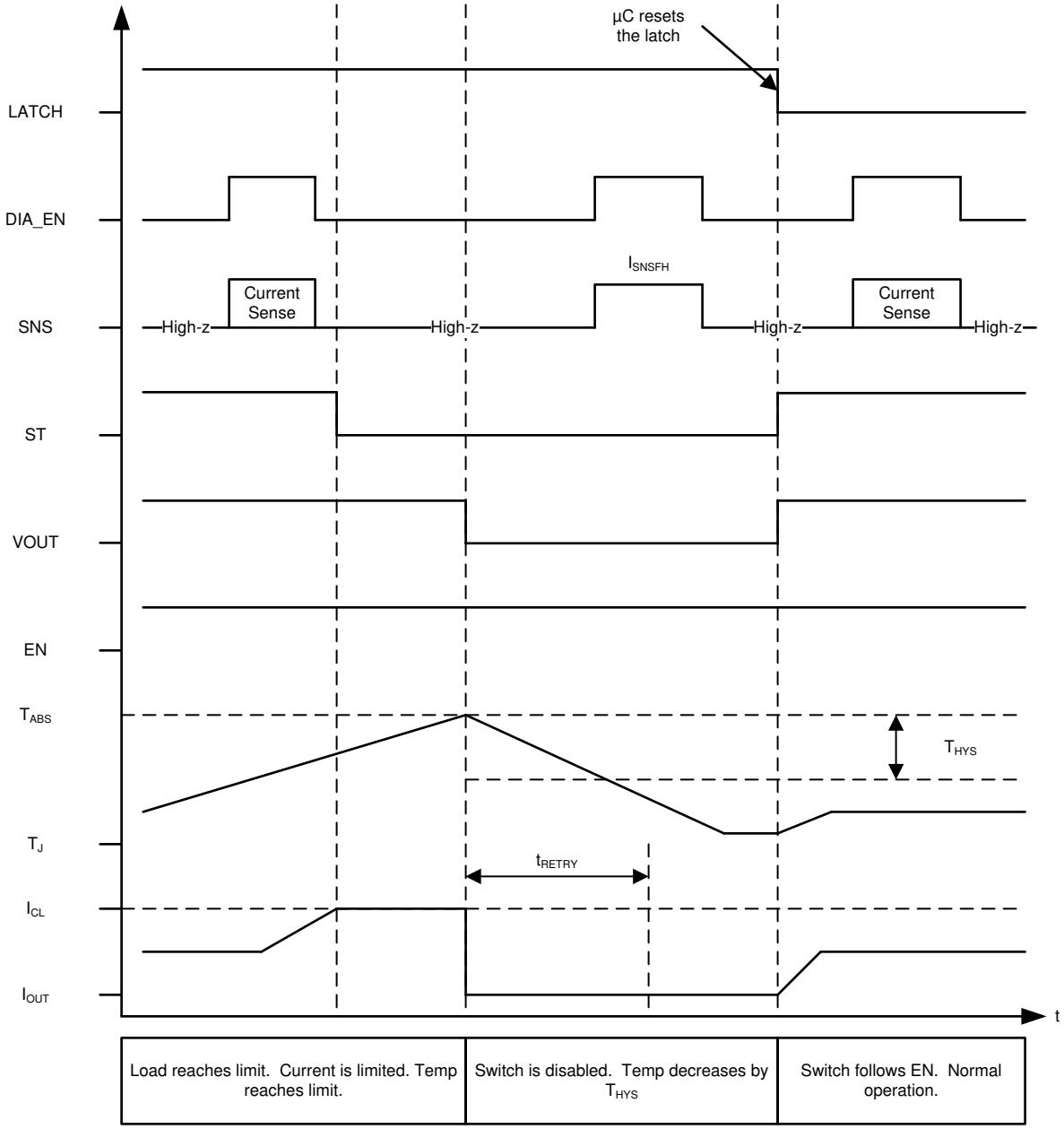


Figure 8-7. Current Limit – Version C, D - Latched Behavior

Figure 8-8 shows the active current limiting behavior of versions C, D. The switch does not shutdown until either thermal shutdown or energy limit is tripped. In this example, LATCH is tied to GND.

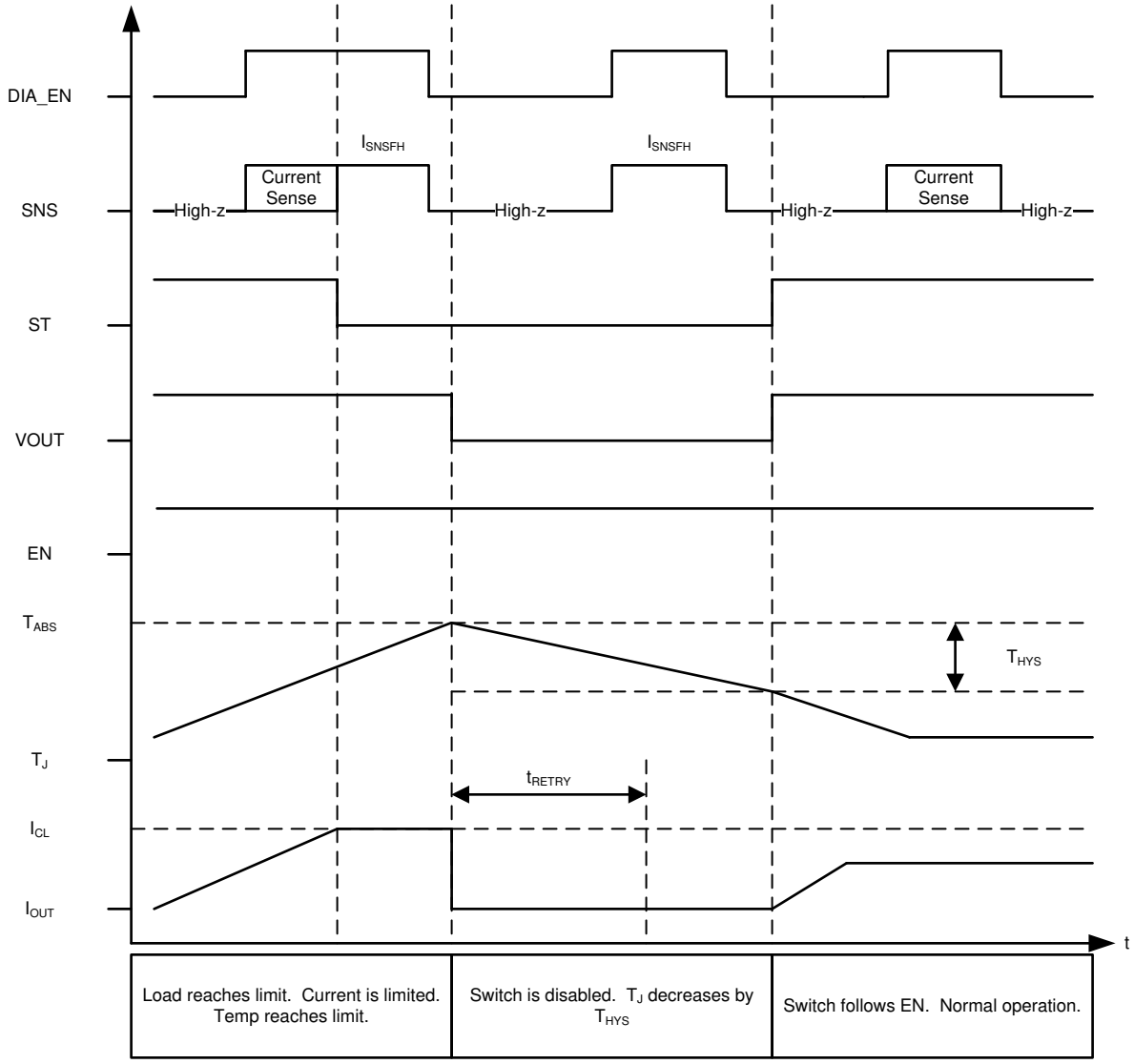


Figure 8-8. Current Limit – Version C, D - LATCH = 0

When the switch retries after a shutdown event, the SNS fault indication remains until V_{OUT} has risen to V_{BB} – 1.8V. After V_{OUT} has risen, the SNS fault indication is reset and current sensing is available. $\overline{ST}$ fault indication is reset as soon as the switch is re-enabled (does not wait for V_{OUT} to rise). If there is a short-to-ground and V_{OUT} is not able to rise, the SNS fault indication remains indefinitely. The following diagram shows auto-retry behavior and provides a zoomed-in view of the fault indication during retry.

Note

Figure 8-9 assumes that t_{RETRY} is expired by the time that T_J reaches the hysteresis threshold.

LATCH = 0V and DIA_EN = 5V

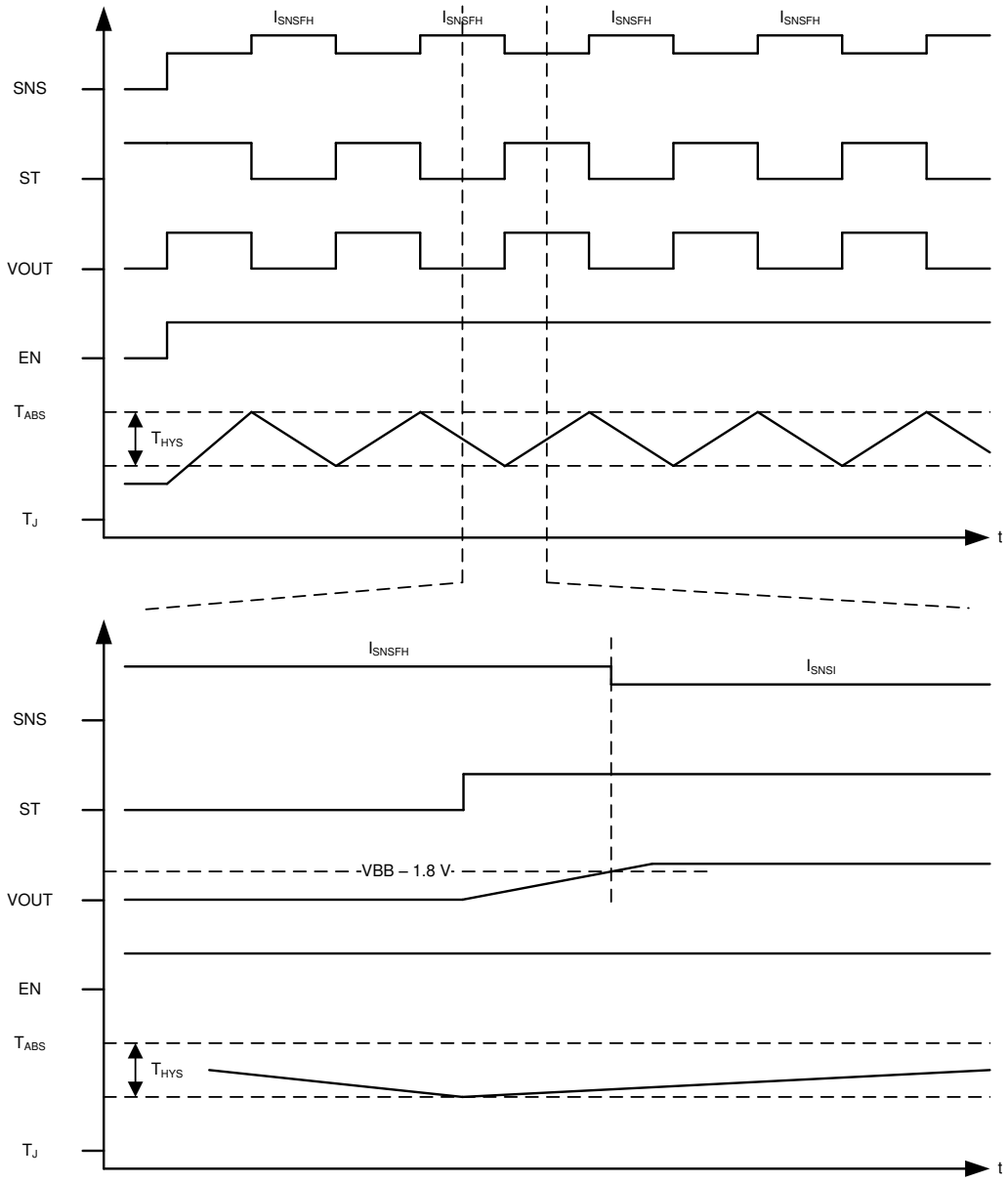


Figure 8-9. Fault Indication During Retry

8.3.2 Diagnostic Mechanisms

8.3.2.1 V_{OUT} Short-to-Battery and Open-Load

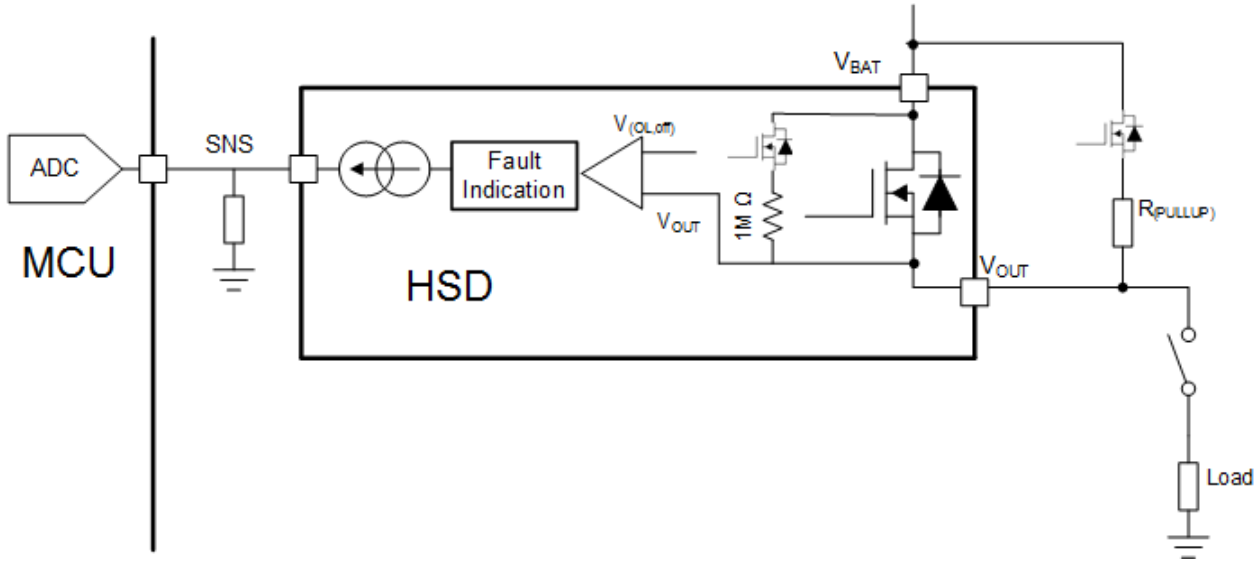
8.3.2.1.1 Detection with Switch Enabled

When the switch is enabled, the V_{OUT} short-to-battery and open-load conditions can be detected with the current sense feature. In both cases, the load current is measured through the SNS pin and is below the expected value.

8.3.2.1.2 Detection with Switch Disabled

While the switch is disabled, if DIA_EN is high, an internal comparator detects the condition of V_{OUT}. If the load is disconnected (open load condition) or there is a short-to-battery, the$_{OUT}$ voltage is higher than the open load threshold ($V_{OL,off}$) and a fault is indicated on the SNS pin. An internal pullup of 1MΩ is in series with an internal MOSFET switch, so no external component is required if only a completely open load is detected. However, if

there is significant leakage or other current draw even when the load is disconnected, externally add a lower value pullup resistor and switch to set the V_{OUT} voltage above the $V_{OL,off}$ during open load conditions.



A. This figure assumes that the device ground and the load ground are at the same potential. In application, there may be a ground shift voltage from 1V to 2V.

Figure 8-10. Short-to-Battery and Open Load Detection

The detection circuitry is only enabled when DIA_EN = HIGH and EN = LOW.

If $V_{OUT} > V_{OL}$, the SNS pin goes to the fault level.

If $V_{OUT} < V_{OL}$, then there is no fault indication.

The fault indication only occurs if the SEL1 pin is set to diagnose the channel.

While the switch is disabled and DIA_EN is high, the fault indication mechanisms continuously represent the present status. For example, if V_{OUT} decreases from $>V_{OL}$ to $<V_{OL}$, the fault indication is reset. Additionally, the fault indication is reset upon the falling edge of DIA_EN or the rising edge of EN.

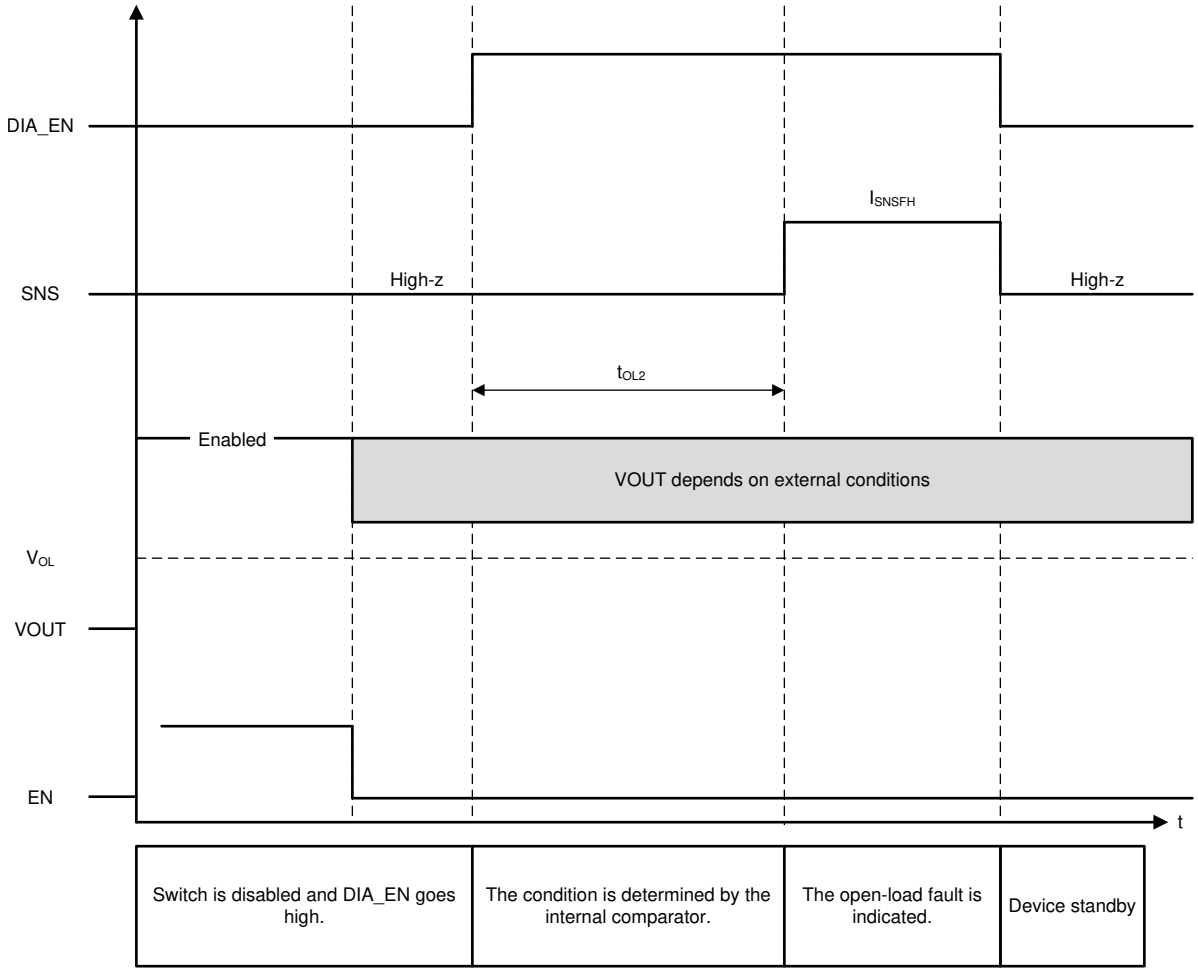


Figure 8-11. Open Load

8.3.2.2 SNS Output

Use the SNS output to sense the load current, supply voltage, or device temperature. The SELx pins select the desired sense signal. The sense circuit provides a current that is proportional to the selected parameter. This current is sourced into an external resistor to create a voltage that is proportional to the selected parameter. Measure this voltage using an ADC or comparator.

To verify accurate sensing measurement, connect the sensing resistor to the same ground potential as the µC ADC.

The SNS Output includes an internal clamp, $V_{SNSclamp}$. This clamp is designed to prevent a high voltage at the SNS output and the ADC input.

Table 8-1. Analog Sense Transfer Function

PARAMETER	TRANSFER FUNCTION	
Load current	$I_{SNSI} = \frac{I_{OUT}}{4600}$	(1)
Supply voltage[1]	$I_{SNSV} = (V_{BB}) \times \frac{dI_{SNSV}}{dV}$	(2)

Table 8-1. Analog Sense Transfer Function (continued)

PARAMETER	TRANSFER FUNCTION
Device temperature	$I_{SNST} = \left(T_J - 25℃\right) \times \frac{dI_{SNS}}{dT} + 0.85$ (3)

(1) Voltage potential between the V_{BB} pin and the GND pin.

The SNS output is also used to indicate system faults. I_{SNS} goes to the predefined level, I_{SNSFH}, when there is a fault. This level is defined in the electrical specifications.

8.3.2.2.1 R_{SNS} Value

Consider the following factors when selecting the R_{SNS} value:

- Current sense ratio
- Largest and smallest diagnosable load current
- Full-scale voltage of the ADC
- Resolution of the ADC

For an example of selecting R_{ISNS} value, reference *Selecting the R_{ISNS} Value* in the applications section of this datasheet.

8.3.2.2.1.1 High Accuracy Load Current Sense

In many automotive modules, the high-side switch must provide diagnostic information about the downstream load. With more complex loads, high accuracy sensing is required. A few examples follow:

- **LED Lighting**: In many architectures, the Body Control Module must be compatible with both incandescent bulbs and also LED modules. The bulb may be relatively simple to diagnose. However, the LED module consumes less current and also can include multiple LED strings in parallel. The same BCM is used in both cases, so the high-side switch must be able to accurately diagnose both load types.
- **Solenoid Protection**: Often solenoids are precisely controlled by low-side switches. However, in a fault event, the low-side switch cannot disconnect the solenoid from the power supply. A high-side switch can be used to continuously monitor several solenoids. If the system current becomes higher than expected, the high-side switch can disable the module.

8.3.2.2.1.2 SNS Output Filter

To achieve the most accurate current sense value, TI recommends to apply filtering to the SNS output. There are two methods of filtering:

- Low-Pass RC filter between the SNS pin and the ADC input. This filter is illustrated in Figure 9-1 and typical values for the resistor and capacitor are given. The designer must select a C_{SNS} capacitor value based on system requirements. A larger value provides improved filtering. A smaller value allows for faster transient response.
- The ADC and microcontroller can also be used for filtering. TI recommends that the ADC collects several measurements of the SNS output. The median value of this data set must be considered as the most accurate result. By performing this median calculation, the microcontroller is able to filter out any noise or outlier data.

8.3.2.3 $\overline{ST}$ Pin

The $\overline{ST}$ pin is an open-drain output. The pin indicates the status of the switch channel. The output is high-z when there is no fault condition. The output is pulled low when there is a fault condition.

8.3.2.4 Fault Indication and SNS Mux

The following faults are communicated through the SNS and $\overline{ST}$ outputs:

- Switch shutdown, due to:
  - Thermal shutdown
  - Current limit

  - Energy limit
- Active current limiting
- Open-load / V_{OUT} shorted-to-battery

Open-load and Short-to-battery are not indicated while the switch is enabled (though these conditions can be detected through the sense current). Hence, if there is a fault indication corresponding to an enabled channel, then it must be either switch shutdown or active current limiting.

The SNS pin only indicates the fault if the SELx = 00. Switch shutdown fault indication occurs on the $\overline{ST}$ pin regardless of the SELx pins; however, OL/STB fault indication is only available when the SELx = 00.

Table 8-2. SNS Mux

INPUTS				OUTPUTS	
DIA_EN	SEL1	SEL2	FAULT DETECT(1)	SNS	ST
0	X	X	0	High-z	High-z
0	X	X	1	High-z	Pull low
1	0	0	0	Load current	High-z
1	0	1	0	Not Used	Not Used
1	1	0	0	Device temperature	High-z
1	1	1	0	Supply voltage	High-z
1	0	0	1	I_{SNSFH}	Pull low
1	0	1	1	Not Used	Not Used
1	1	0	1	Device temperature	Pull low
1	1	1	1	Supply voltage	Pull low

(1) Fault Detect encompasses the below conditions:
- Switch shutdown and waiting for retry
- Active current limiting
- OL / STB

8.3.2.5 Resistor Sharing

Multiple high-side switch channels may use the same SNS resistor as shown in Figure 8-12 below. This action reduces the total number of passive components in the system and the number of ADC terminals that are required of the microcontroller.

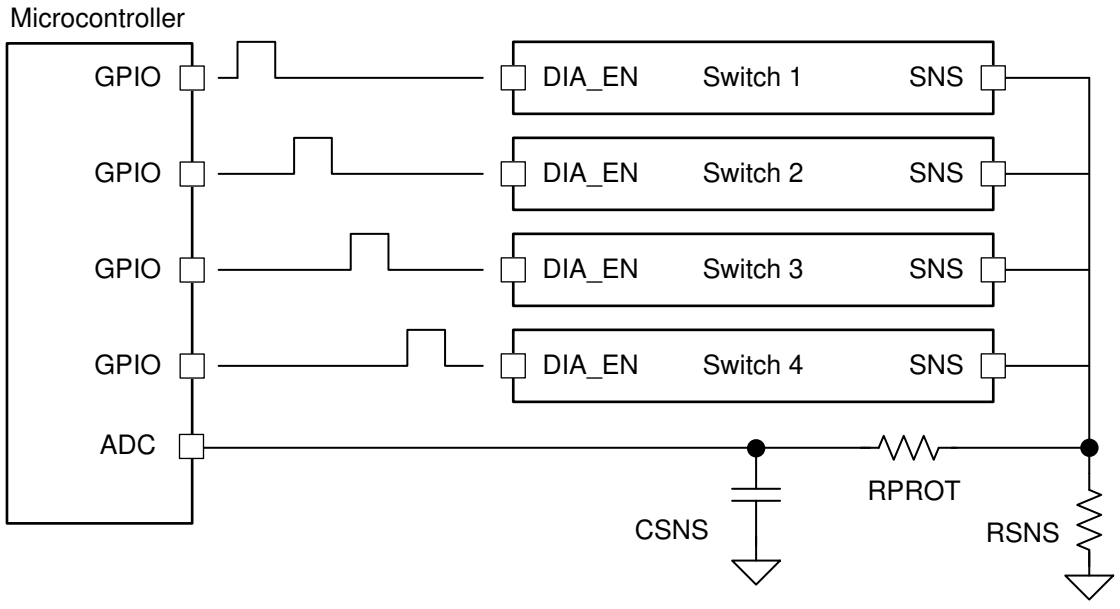


Figure 8-12. Sharing R_{SNS} Among Multiple Devices

8.3.2.6 High-Frequency, Low Duty-Cycle Current Sensing

Some applications operate with a high-frequency, low duty-cycle PWM. Such applications require fast settling of the SNS output. For example, a 250Hz, 5% duty cycle PWM has an on-time of only 200µs. The microcontroller ADC may sample the SNS signal after the defined settling time, $t_{SNSION3}$.

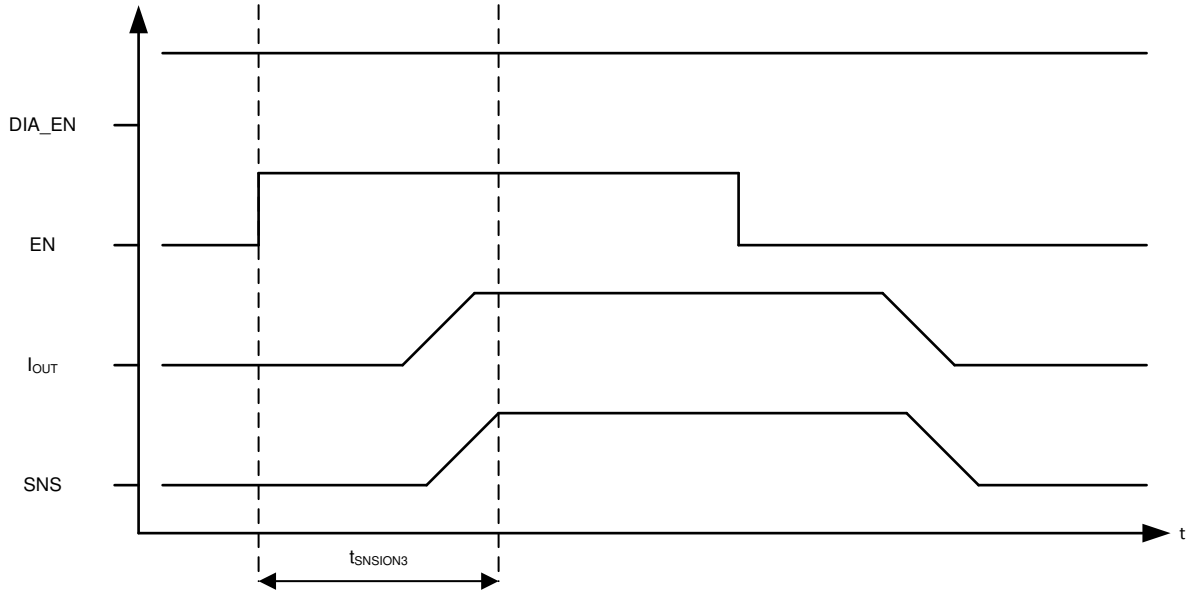
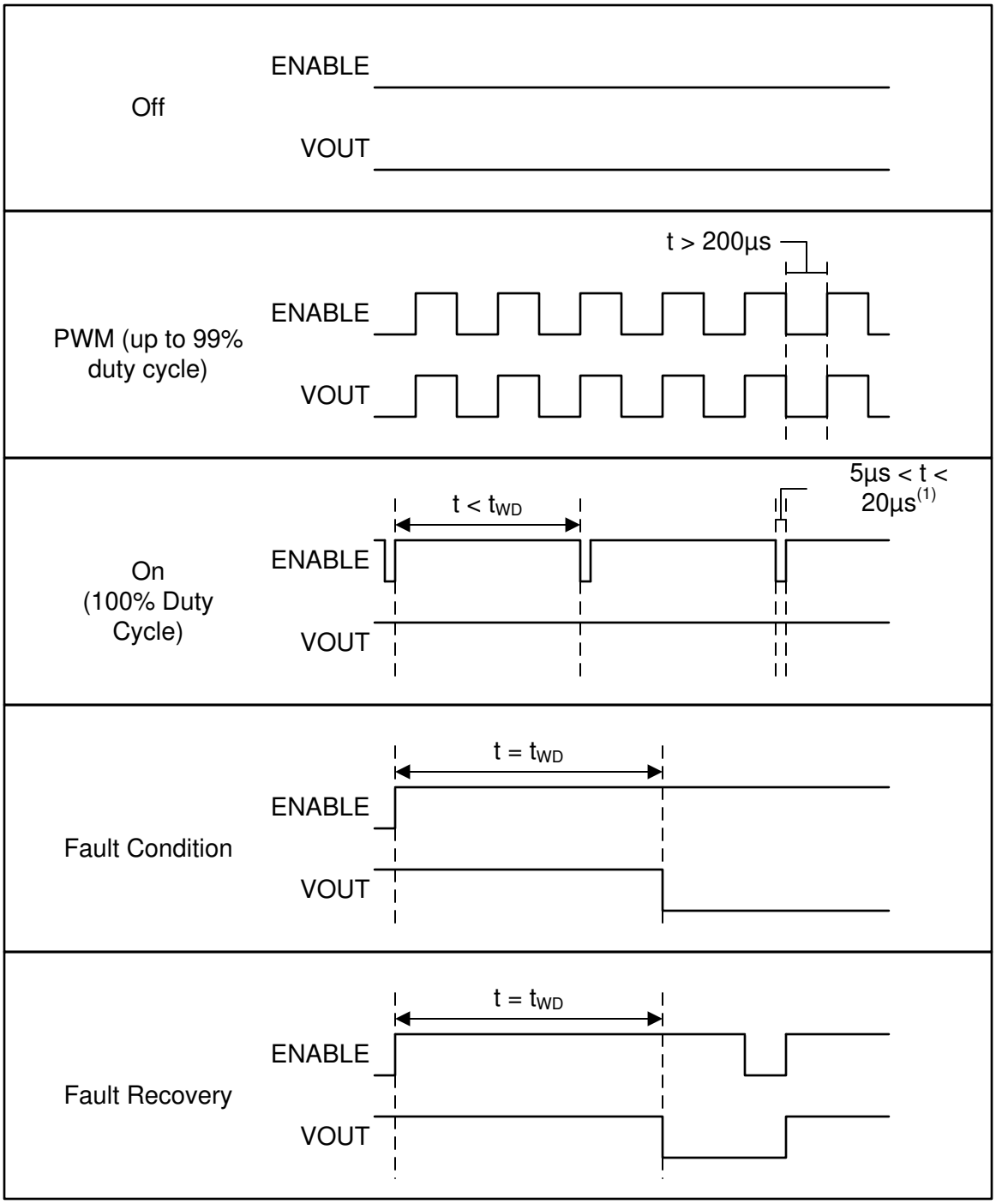


Figure 8-13. Current Sensing in Low-Duty Cycle Applications

8.3.3 Enable Watchdog

For some automotive applications, continuously verify that there is valid communication between the microcontroller and the switch enable pin. The purpose of this is to protect against possible communication faults (for example, microcontroller failure). The TPS1HA08-Q1 includes an optional watchdog feature which continuously polls the enable pin. Note that this feature is only activated for device version E, so the below information is only applicable to version E.

To use the watchdog feature, the microcontroller must apply a PWM to the switch enable pin. If this PWM is not present (EN is high continuously for ≥ t_{WD}) the switch automatically is disabled. The watchdog timer is reset on the rising edge of EN. The fault indications are cleared upon the falling edge of EN. The following figure illustrates how the switch responds to the EN PWM.



The watchdog feature requires that a PWM is applied to the switch enable pin. To maintain V_{OUT} at 100% duty cycle, the microcontroller must periodically apply a short pulse to the enable pin. This short pulse resets the watchdog timer, but does not cause the switch to turn off. The pulse must be > 5 µs to ensure that it is recognized by the device. There is no upper limit on the pulse width; however, if the pulse is longer than 20 µs, the switch may start to transition from enabled to disabled.

Figure 8-14. Enable Watchdog - Overview

Figure 8-15 illustrates the behavior of the watchdog feature.

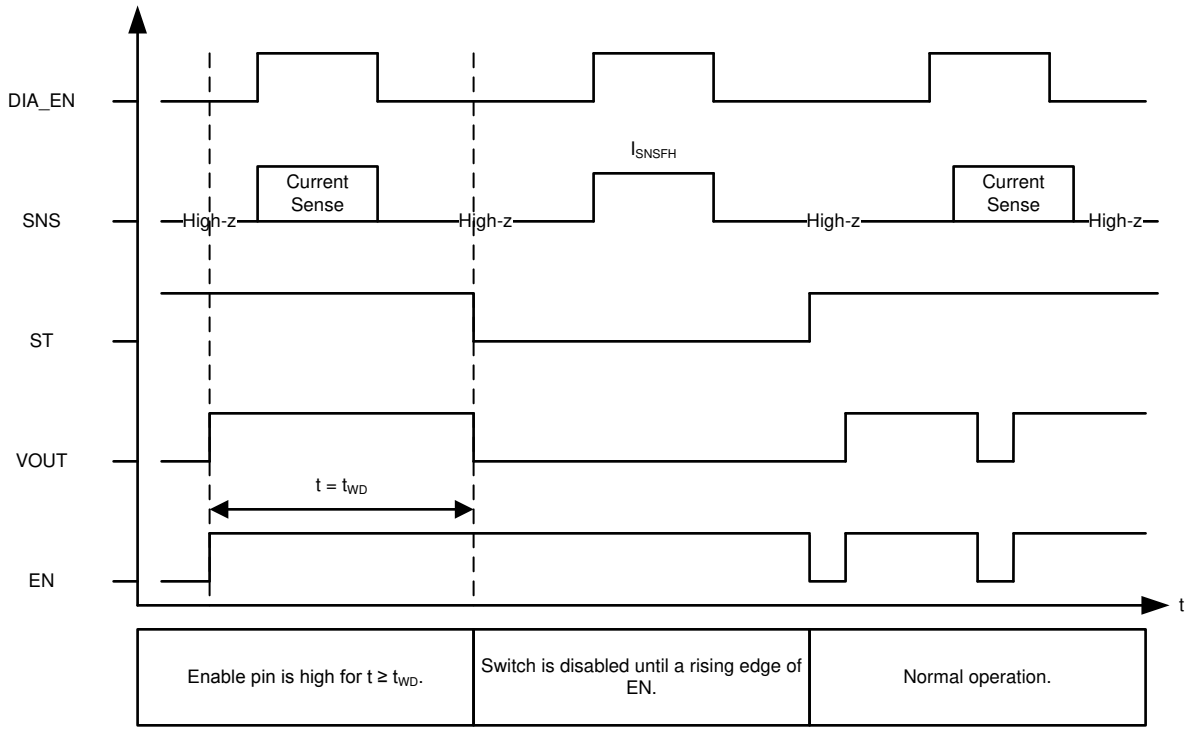


Figure 8-15. Enable Watchdog Timing Diagram

8.4 Device Functional Modes

8.4.1 Off

Off state occurs when the device is not powered.

8.4.2 Standby

Standby state is a low-power mode used to reduce power consumption to the lowest level. Diagnostic capabilities are not available in standby mode.

8.4.3 Diagnostic

Diagnostic state may be used to perform diagnostics while the switch is disabled.

8.4.4 Standby Delay

The standby delay state is entered when EN and DIA_EN are low. After t_{STBY}, if the EN and DIA_EN pins are still low, the device goes to standby State.

8.4.5 Active

In Active state, the switch is enabled. The diagnostic functions may be turned on or off during active state.

8.4.6 Fault

The fault state is entered if a fault shutdown occurs (thermal shutdown, current limit, energy limit). After all faults are cleared, the LATCH pin is low, and the retry timer has expired, the device transitions out of fault state. If the Enable pin is high, the switch re-enables. If the Enable pin is low, the switch remains off.

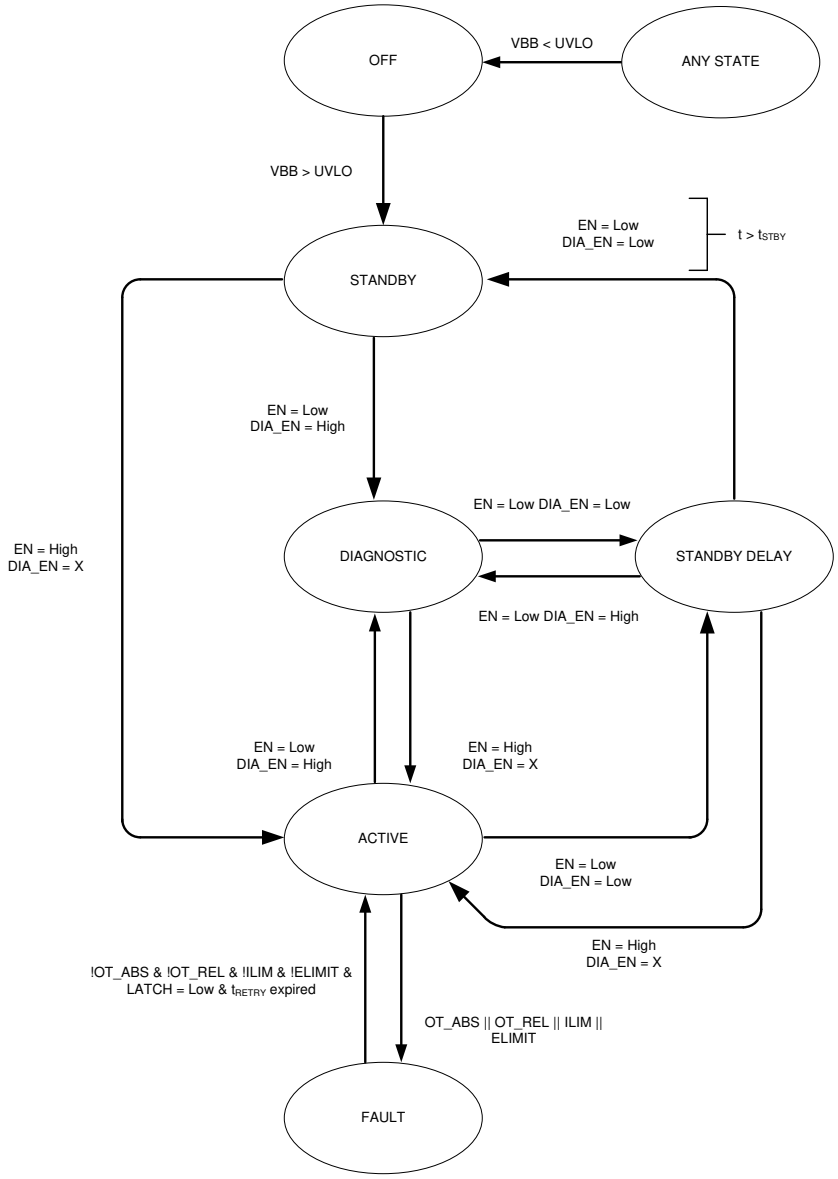


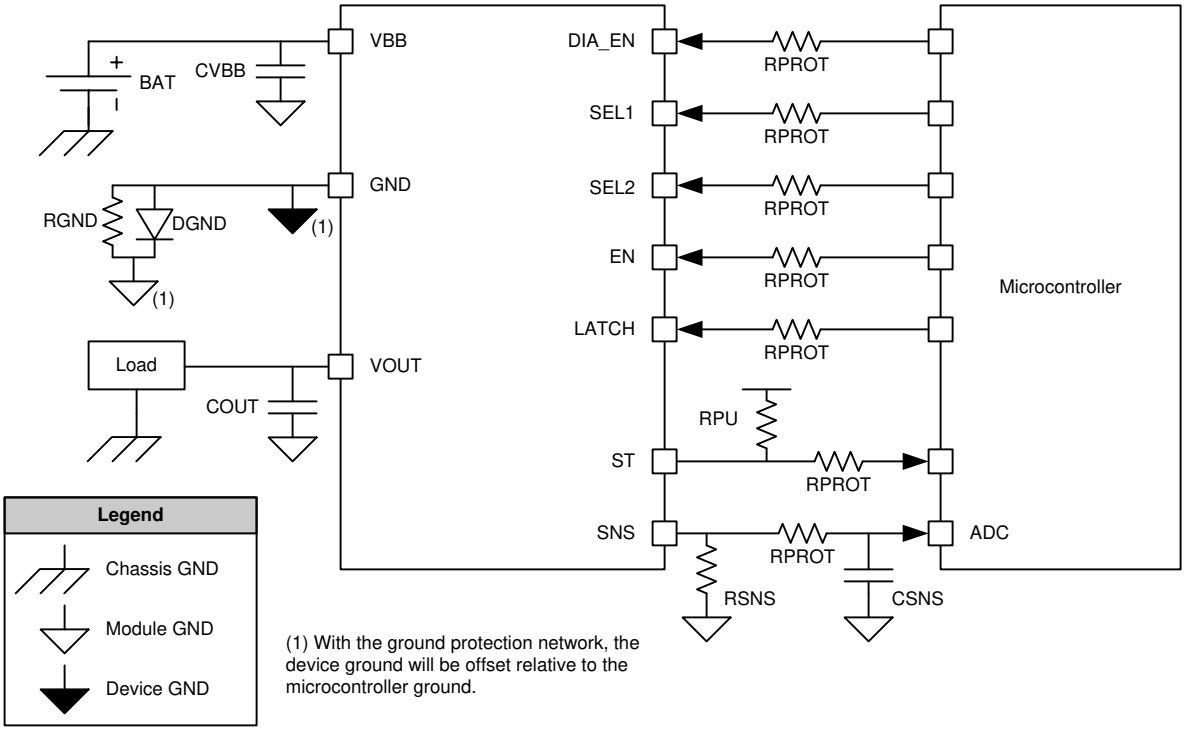
Figure 8-16. State Diagram

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information



With the ground protection network, the device ground is offset relative to the microcontroller ground.

Figure 9-1. System Diagram

Table 9-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{PROT}	15kΩ	Protect microcontroller and device I/O pins
R_{SNS}	1kΩ	Translate the sense current into sense voltage
R_{PU}	10kΩ	Provide pullup source for open-drain output
C_{SNS}	100pF – 10nF	Low-pass filter for the ADC input
R_{GND}	4.7kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	BAS21 Diode	Protects device during reverse battery
C_{VBB}	220nF to Device GND	Filtering of voltage transients (for example, ESD, ISO7637-2) and improved emissions
	100nF to Module GND	Stabilize the input supply and filter out low frequency noise.
C_{OUT}	22nF	Filtering of voltage transients (for example, ESD, ISO7637-2)

9.1.1 Ground Protection Network

As discussed in the section regarding Reverse Battery, use D_{GND} to prevent excessive reverse current from flowing into the device during a reverse battery event. Additionally, R_{GND} is placed in parallel with D_{GND} if the switch is used to drive an inductive load. Multiple high-side switches can share the ground protection network (D_{GND} and R_{GND}).

Using the absolute maximum rating for I_{GND}, calculate a minimum value for R_{GND}. During the reverse battery condition:

$$I_{GND} = \frac{V_{BB}}{R_{GND}} \quad (4)$$

$$R_{GND} = \frac{V_{BB}}{I_{GND}} \quad (5)$$

- Set V_{BB} = –13.5V
- Set I_{GND} = –50mA (absolute maximum rating)

$$R_{GND} \geq \frac{-13.5V}{-50mA} = 270\Omega \quad (6)$$

In this example, it is found that R_{GND} must be at least 270Ω. Consider the power dissipation in R_{GND} during the reverse battery event:

$$P_{RGND} = \frac{V_{BB}^2}{R_{GND}} \quad (7)$$

$$P_{RGND} = \frac{(13.5V)^2}{270\Omega} = 0.675W \quad (8)$$

In practice, R_{GND} is possibly not rated for such a high power. In this case, select a larger resistor value.

9.1.2 Interface with Microcontroller

The ground protection network causes the device ground to be at a higher potential than the module ground (and microcontroller ground). This offset impacts the interface between the device and the microcontroller.

Logic pin voltage is offset by the forward voltage of the diode. For input pins (for example, EN), the designer must consider the V_{IH} specification of the switch and the V_{OH} specification of the microcontroller. For a system that *does not* include D_{GND}, it is required that $V_{OH} > V_{IH}$. For a system that *does* include D_{GND}, it is required that $V_{OH} > (V_{IH} + V_F)$. V_F is the forward voltage of D_{GND}.

For use of the status pin, ST, a similar consideration is necessary. The designer must consider the $V_{OL,\ ST}$ specification and the V_{IL} specification of the microcontroller. For a system that includes DGND, it is required that $V_{OL,\ ST} + V_F < V_{IL,\ \mu C}$.

The sense resistor, R_{SNS}, must be terminated to the microcontroller ground. In this case, the ADC can accurately measure the SNS signal even if there is an offset between the microcontroller ground and the device ground.

9.1.3 I/O Protection

R_{PROT} is used to protect the microcontroller I/O pins during system-level voltage transients such as ISO pulses or reverse battery. A large resistance value establishes that current through the pin is limited to a safe level.

9.1.4 Inverse Current

Inverse current occurs when $0V < V_{BB} < V_{OUT}$. In this case, current may flow from V_{OUT} to V_{BB}. Inverse current cannot be caused by a purely resistive load. However, a capacitive or inductive load can cause inverse current. For example, if there is a significant amount of load capacitance and the V_{BB} node has a transient droop, V_{OUT} may be greater than V_{BB}.

TPS1HA08-Q1 does not detect inverse current. When the switch is enabled, inverse current passes through the switch. When the switch is disabled, inverse current may pass through the MOSFET body diode. The device continues operating in the normal manner during an inverse current event.

9.1.5 Loss of GND

The ground connection may be lost either on the device level or on the module level. If the ground connection is lost, both switches are disabled. If the switch was already disabled when the ground connection was lost, the switch remains disabled. When the ground is reconnected, normal operation resumes.

9.1.6 Automotive Standards

9.1.6.1 ISO7637-2

TPS1HA08-Q1 is tested according to the ISO7637-2:2011 (E) standard. The test pulses are applied both with the switches enabled and disabled. The test setup includes only the DUT and minimal external components: C_{VBB}, C_{OUT}, D_{GND}, and R_{GND}.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as: “The function does not perform as designed during the test but returns automatically to normal operation after the test.”

Table 9-2. ISO7637-2:2011 (E) Results

TEST PULSE	TEST PULSE SEVERITY LEVEL WITH STATUS II FUNCTIONAL PERFORMANCE		MINIMUM NUMBER OF PULSES OR TEST TIME	BURST CYCLE / PULSE REPETITION TIME	
	LEVEL	US		MIN	MAX
1	IV	–150V	500 pulses	0.5s	--
2a	III	+55V	500 pulses	0.20	5s
2b	IV	+10V	10 pulses	0.5s	5s
3a	III	–165V	1 hour	90ms	100ms
3b	III	+112V	1 hour	90ms	100ms

9.1.6.2 AEC – Q100-012 Short Circuit Reliability

The TPS1HA08-Q1 is tested according to the AEC - Q100-012 Short Circuit Reliability standard. This test is performed to demonstrate the robustness of the device against V_{OUT} short-to-ground events. Test results are summarized in Table 9-3. For further details, see also the AEC - Q100-012 standard document or TI's *Short Circuit Reliability Test for Smart Power Switches* application note.

Test conditions:

- LATCH = 0V
- T_A = –40°C
- 10 units from 3 separate lots for a total of 30 units
- L_{supply} = 5µH, R_{supply} = 10mΩ
- V_{BB} = 14V

Test procedure:

- Parametric data is collected on each unit pre-stress.
- Each unit is enabled into a short circuit with the required short circuit cycles or duration as specified.
- Parametric data is re-collected on each unit post-stress to verify that no parametric shift is observed.

The cold repetitive test is run at –40°C which is the worst-case condition for the TPS1HA08-Q1. The current limit threshold is highest at cold temperature; hence, the short-circuit pulse contains more energy at cold temperature. The cold repetitive test refers to the device being given time to cool down between pulses, within than being run at a cold temperature. The load short circuit is the worst-case situation, since the energy stored in the cable inductance can cause additional harm. The fast response of the device establishes that current limiting occurs quickly and at a current close to the load short condition. In addition, the hot repetitive test is performed as well.

Table 9-3. AEC - Q100-012 Test Results

TEST	LOCATION OF SHORT	DEVICE VERSION	NO. OF CYCLES	NO. OF UNITS	NO. OF FAILS
Cold Repetitive - Long Pulse	Load Short Circuit, L_{short} = 5µH, R_{short} = 100mΩ, T_A = –40°C	D	200k	30	0
Hot Repetitive - Long Pulse	Terminal Short Circuit, L_{short} = 5µH, R_{short} = 100mΩ, T_A = 25°C	D	100 hours	30	0

9.1.7 Thermal Information

When outputting current, the TPS1HA08-Q1 heats up due to the power dissipation. Figure 9-2 shows the transient thermal impedance curve that can be used to determine the device temperature during 1W pulse of a given length.

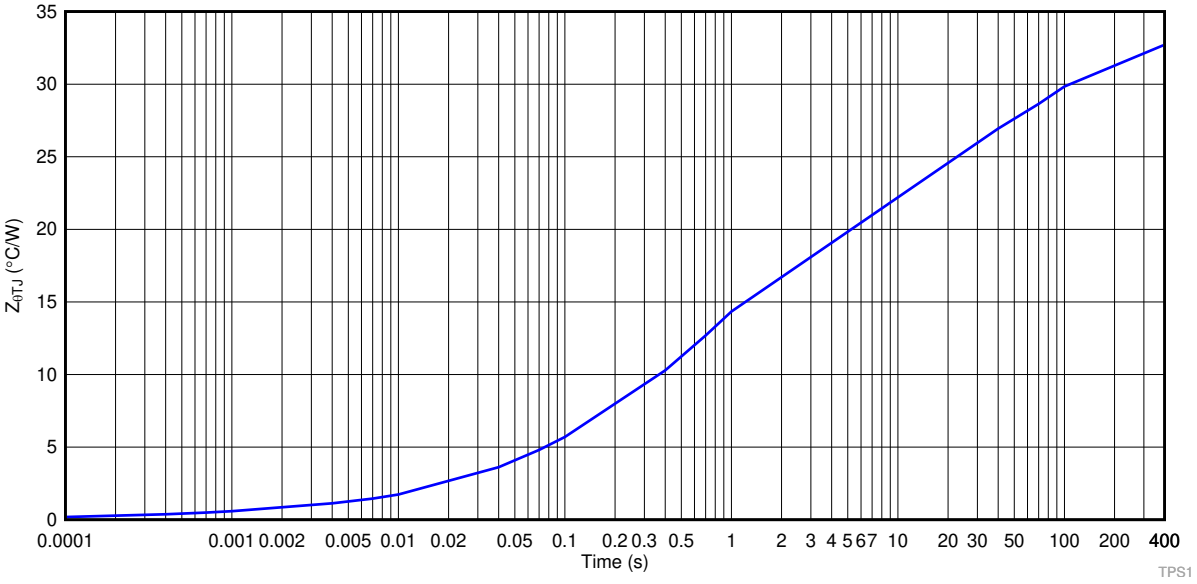


Figure 9-2. Transient Thermal Impedance

9.2 Typical Application

This application example demonstrates how the TPS1HA08-Q1 device can be used to power resistive heater loads as in seat heaters. Figure 9-3 shows a typical application where the load is a resistive seat heater. This document highlights the basics of this type of application, however for a more detailed discussion reference *TI's Smart Power Switch Seat Heater Reference Design*.

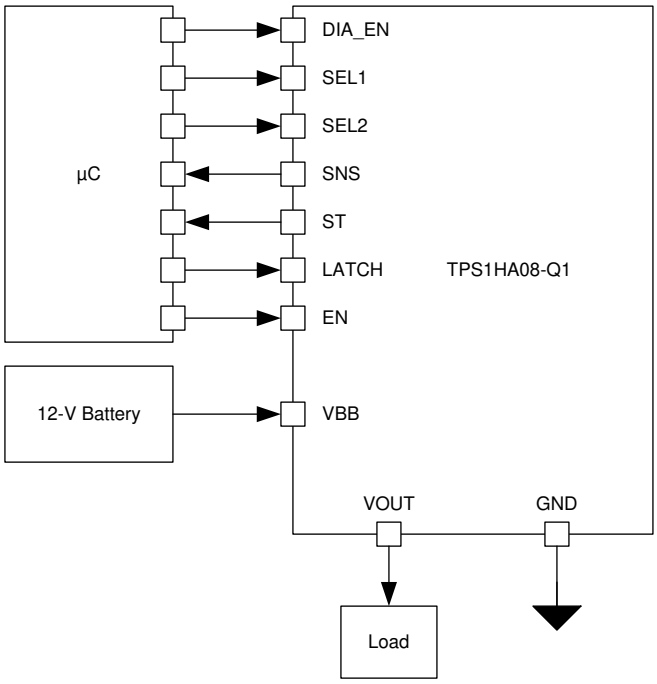


Figure 9-3. Block Diagram for Powering Heater Loads

9.2.1 Design Requirements

For this design example, use the input parameters shown in Table 9-4.

Table 9-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BB}	12.8V
Heater load	90W maximum
Load current sense	100mA to 20A
Ambient temperature	85°C
$R_{\theta JA}$	32.8°C/W (depending on PCB)

9.2.2 Detailed Design Procedure

9.2.2.1 Thermal Considerations

The DC current under maximum load power condition is around 7.03A. Power dissipation in the switch is calculated in Equation 9. R_{ON} is assumed to be 20mΩ because this is the maximum specification. In practice, R_{ON} is lower.

$$P_{FET} = I^2 \times R_{ON} \tag{9}$$

$$P_{FET} = (7.03A)^2 \times 20m\Omega = 0.988W \tag{10}$$

Calculate the junction temperature of the device using Equation 11 and the $R_{\theta JA}$ value from the *Specifications* section.

$$T_J = T_A + R_{\theta JA} \times P_{FET} \tag{11}$$

$$T_J = 85°C + 32.8°C/W \times 0.988W = 117.4°C$$

The maximum junction temperature rating for TPS1HA08-Q1 device is T_J = 150°C. Based on the above example calculation, the device temperature stays below the maximum rating.

9.2.2.2 Diagnostics

If the resistive heating load is disconnected (heater malfunction), an alert is desired. Open-load detection can be performed in the switch-enabled state through the current sense feature of the TPS1HA08-Q1 device. Alternatively, under open load condition in off-state with diagnostics enabled, the current in the SNS pin is the fault current and the can be detected from the sense voltage measurement.

9.2.2.2.1 Selecting the R_{ISNS} Value

Table 9-5 shows the requirements for the load current sense in this application. The K_{SNS} value is specified for the device and can be found in the *Specifications* section.

Table 9-5. R_{SNS} Calculation Parameters

PARAMETER	EXAMPLE VALUE
Current Sense Ratio (K_{SNS})	4600
Largest diagnosable load current	20A
Smallest diagnosable load current	50mA
Full-scale ADC voltage	5V
ADC resolution	10 bit

The load current measurement requirements of 20A establishes that current can be sensed up to the 20A current limit, while the low level of 100mA allows for accurate measurement of low load currents.

The R_{SNS} resistor value must be selected such that the largest diagnosable load current puts V_{SNS} at about 90% of the ADC full-scale. With this design, any ADC value above 90% can be considered a fault. Additionally, the R_{SNS} resistor value verifies that the smallest diagnosable load current does not cause V_{SNS} to fall below 1LSB of the ADC. With the given example values, a 1kΩ sense resistor satisfies both requirements shown in Table 9-6.

Table 9-6. V_{SNS} Calculation

LOAD (A)	SENSE RATIO	I_{SNS} (mA)	R_{SNS} (Ω)	V_{SNS} (V)	% OF 5V ADC
0.050	4600	0.011	1000	0.011	0.22%
20.000	4600	4.348	1000	4.348	87%

9.2.3 Application Curves

Figure 9-4 shows the behavior of the TPS1HA08-Q1 in this application when the MCU provides an enable pulse to beginning heating the resistive element. Shortly after the EN pin goes high, the load current begins to flow and the SNS pin measures the output current.

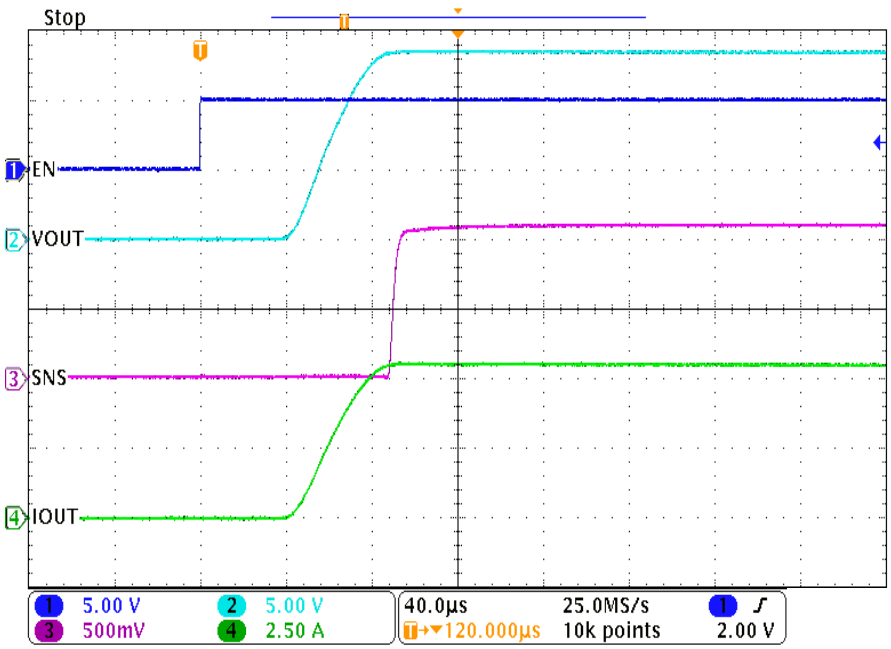


Figure 9-4. Heater Turn-on Time

By measuring the voltage on the SNS pin, the TPS1HA08-Q1 can communicate back to the system MCU what the load current is. Figure 9-5 shows that when the seat heater approaches full load and I_{OUT} jumps from a low load current of 1A up to a 5A load current, the load step is mirrored on the SNS pin.

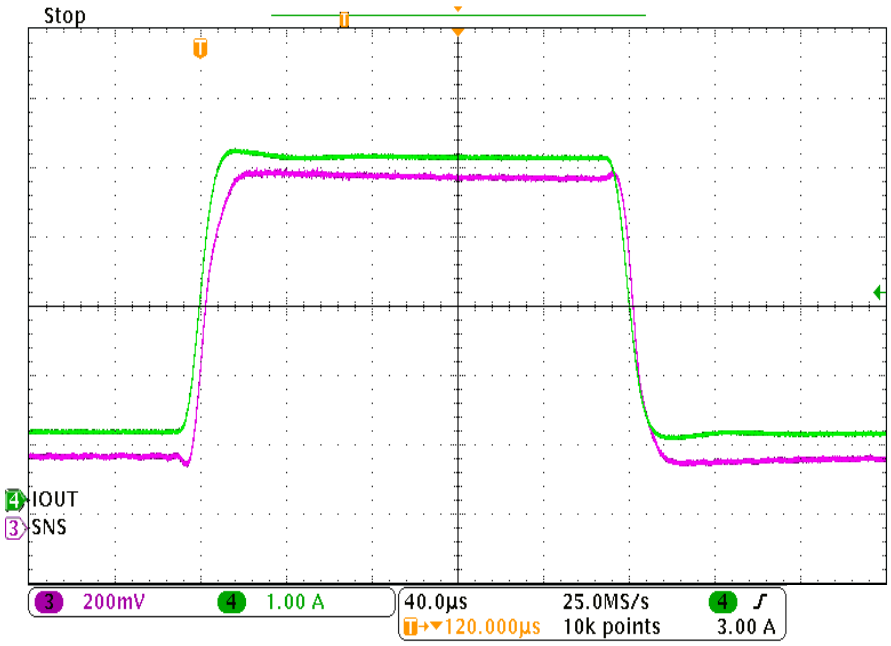


Figure 9-5. SNS Response During Heater Load Step

One common concern in these type of applications is that the heating element can accidentally lose connection, creating an open load situation. In this case, it is designed for the TPS1HA08-Q1 to recognize that the load has been removed and report a FLT to the MCU. Figure 9-6 shows the behavior of the TPS1HA08-Q1 when there is no load attached. As soon as the DIAG_EN pin is engaged, the SNS output goes high and the $\overline{ST}$ output engages low. By monitoring these pins, the MCU can recognize there is a fault and notify the user that maintenance is required.

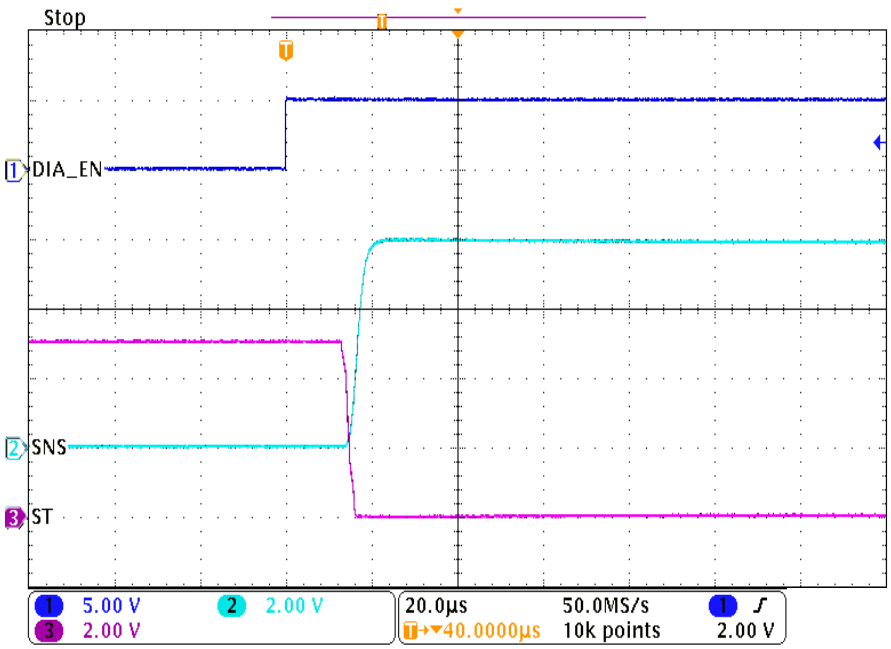


Figure 9-6. Open Load Detection If Heating Element is Missing

Importantly, the TPS1HA08-Q1 also protects the system in the event of a short-circuit. Figure 9-7 shows the behavior of the device if it is enabled into a short circuit condition. If this is using the device option C, the current is clamped to the current limit I_{CL} until it hits an over temperature event, at which point it shuts down. In this way, the system is protected from unchecked overcurrent in the event of a short circuit.

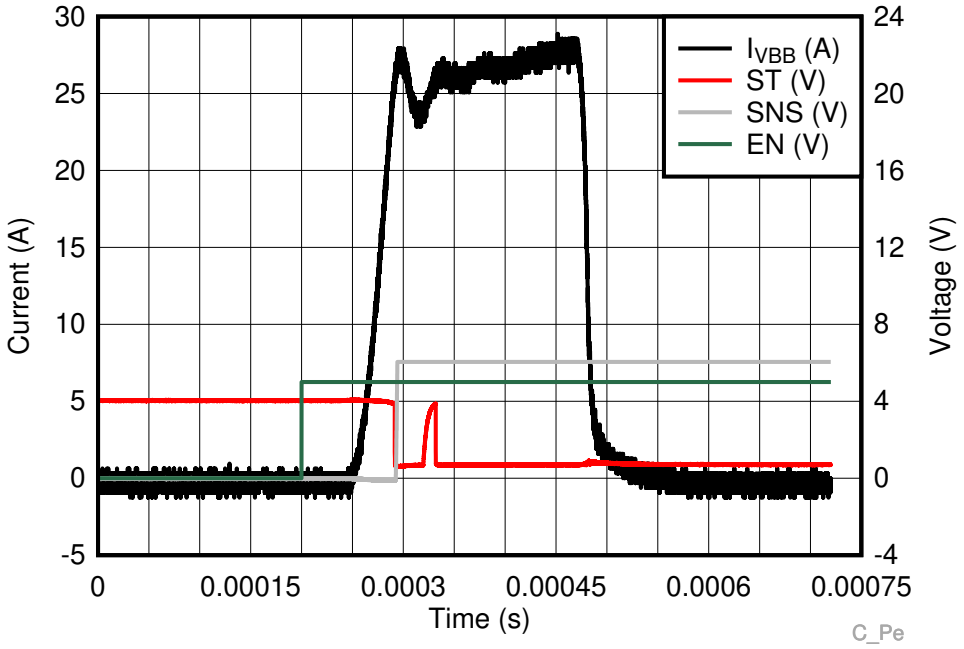


Figure 9-7. Overcurrent Behavior During Short Circuit Event

9.3 Power Supply Recommendations

The TPS1HA08-Q1 is designed to operate in a 12V automotive system. The nominal supply voltage range is from 8V to 18V. The device is also designed to withstand voltage transients beyond this range. When operating

outside of the nominal voltage range, the device exhibits normal functional behavior. However, parametric specifications are not verified.

Table 9-7. Operating Voltage Range

V_{BB} Voltage Range	Note
3V to 8V	Transients such as cold crank and start-stop, functional operation specified but some parametric specifications may not apply. The device is completely short-circuit protected up to 125°C
8V to 18V	Nominal supply voltage, all parametric specifications apply. The device is completely short-circuit protected up to 125°C
18V to 40V	Transients such as jump-start and load-dump, functional operation specified but some parametric specifications may not apply

9.4 Layout

9.4.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed pad to a large copper pour. On the top PCB layer, the pour can extend beyond the pad dimensions as shown in the example below. In addition to this, TI recommends to also have a V_{BB} plane either on one of the internal PCB layers or on the bottom layer. Vias must connect this plane to the top V_{BB} pour.

TPS1HA08-Q1 has six V_{OUT} pins. All V_{OUT} pins must be shorted together on the PCB. Additionally, the layout validates that the current path is symmetrical for both sides of the device. If the path is not symmetrical, there is some imbalance in current spreading across the power FET. This can impact accuracy of the current sense measurement.

9.4.2 Layout Example

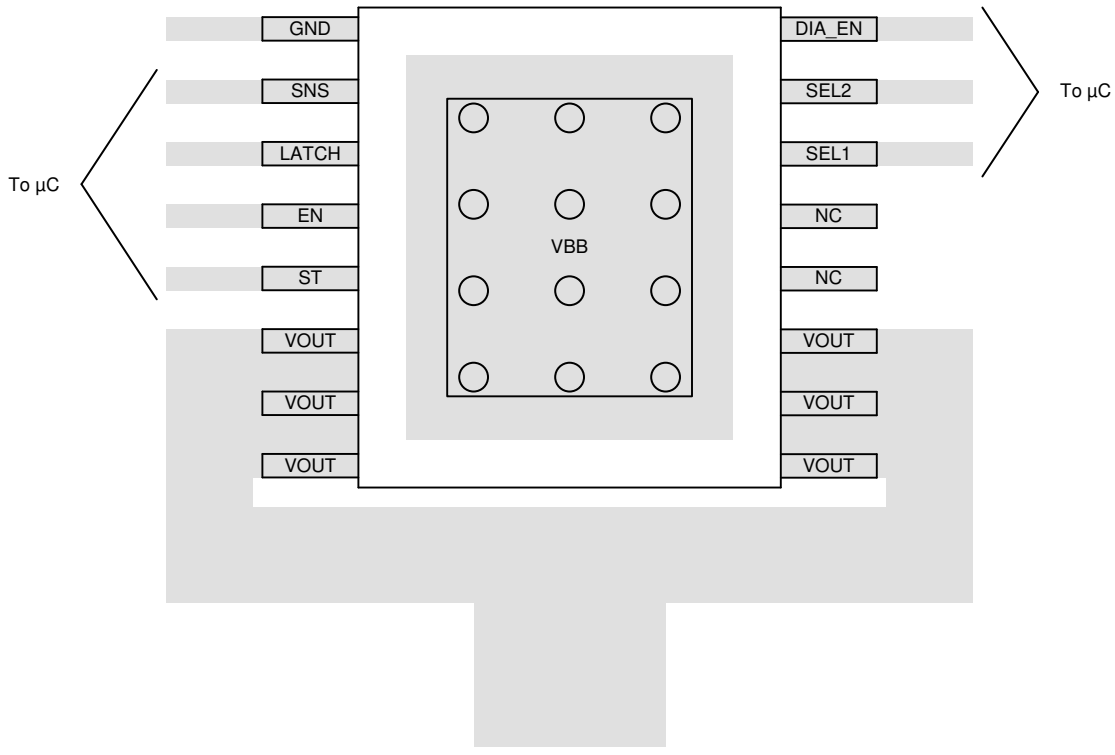


Figure 9-8. PWP Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TI's "How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switch* application note
- Texas Instruments, *Short Circuit Reliability Test for Smart Power Switches* application note
- Texas Instruments, *TI's Smart Power Switch Seat Heater Reference Design*
- Texas Instruments, *Reverse Battery Protection for High Side Switches* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2019) to Revision E (June 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added link to the functional safety sub-bullet in the *Features* section	1
• Updated driving inductive and capacitive loads	26

Changes from Revision C (May 2019) to Revision D (December 2019)	Page
• Added functional safety capable link to the *Features* section	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS1HA08AQPWPRQ1	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08A
TPS1HA08AQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08A
TPS1HA08BQPWPRQ1	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08B
TPS1HA08BQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08B
TPS1HA08CQPWPRQ1	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08C
TPS1HA08CQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08C
TPS1HA08DQPWPRQ1	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08D
TPS1HA08DQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08D
TPS1HA08EQPWPRQ1	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08E
TPS1HA08EQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HA08E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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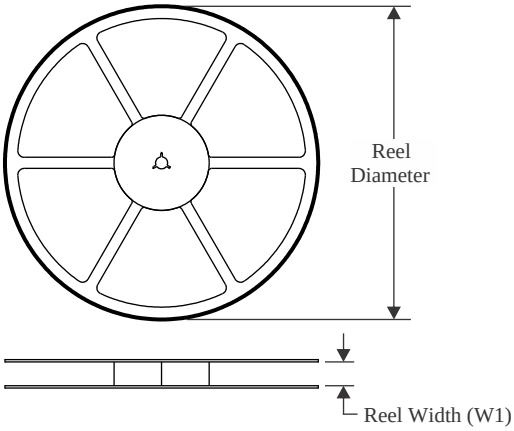
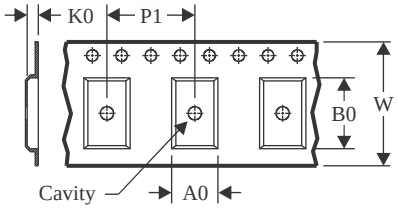
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

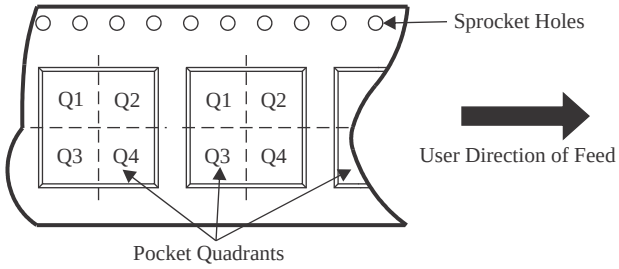


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

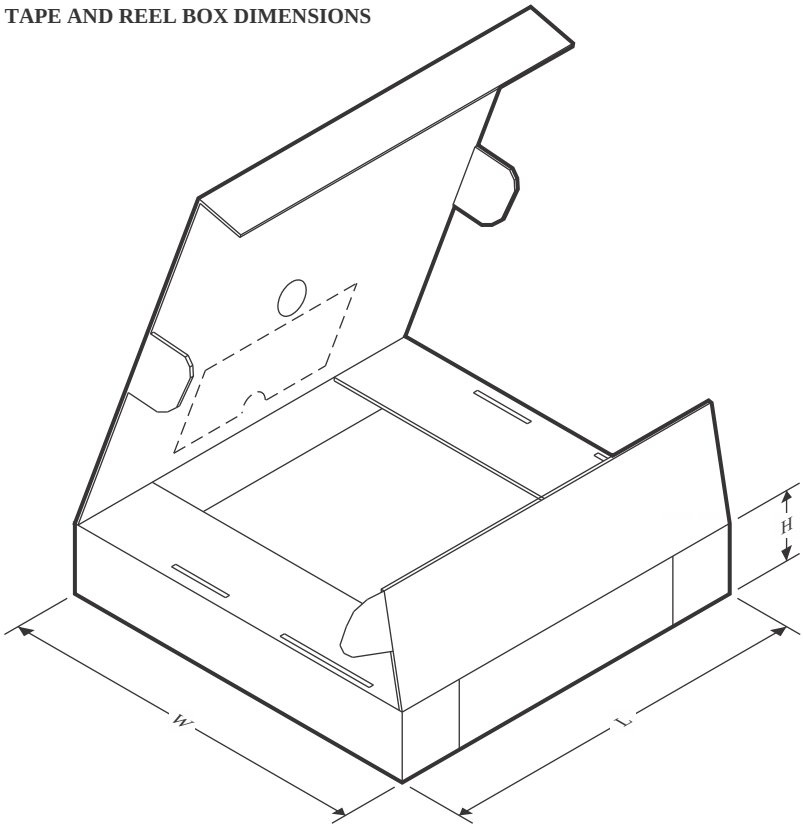
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1HA08AQPWPRQ1	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS1HA08BQPWPRQ1	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS1HA08CQPWPRQ1	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS1HA08DQPWPRQ1	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS1HA08EQPWPRQ1	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

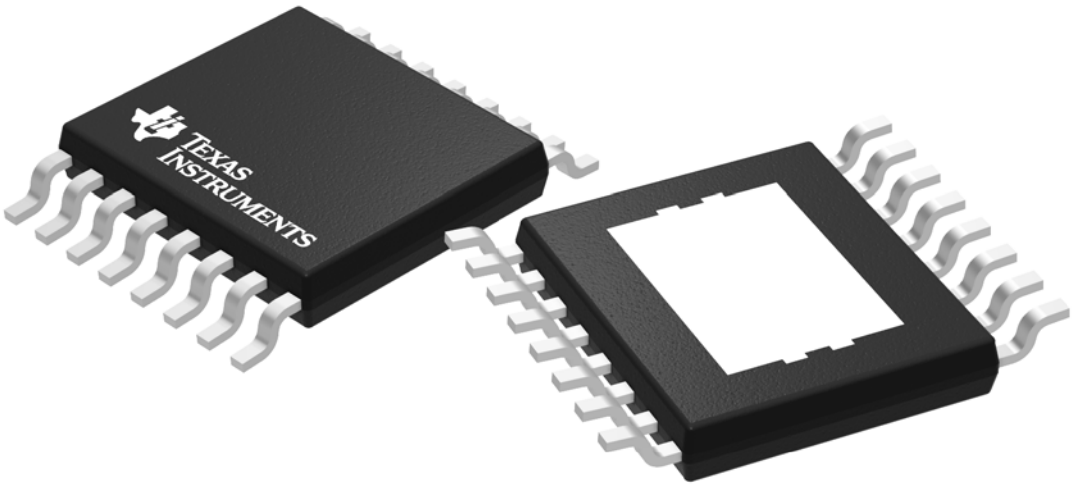


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1HA08AQPWPRQ1	HTSSOP	PWP	16	3000	350.0	350.0	43.0
TPS1HA08BQPWPRQ1	HTSSOP	PWP	16	3000	350.0	350.0	43.0
TPS1HA08CQPWPRQ1	HTSSOP	PWP	16	3000	350.0	350.0	43.0
TPS1HA08DQPWPRQ1	HTSSOP	PWP	16	3000	350.0	350.0	43.0
TPS1HA08EQPWPRQ1	HTSSOP	PWP	16	3000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



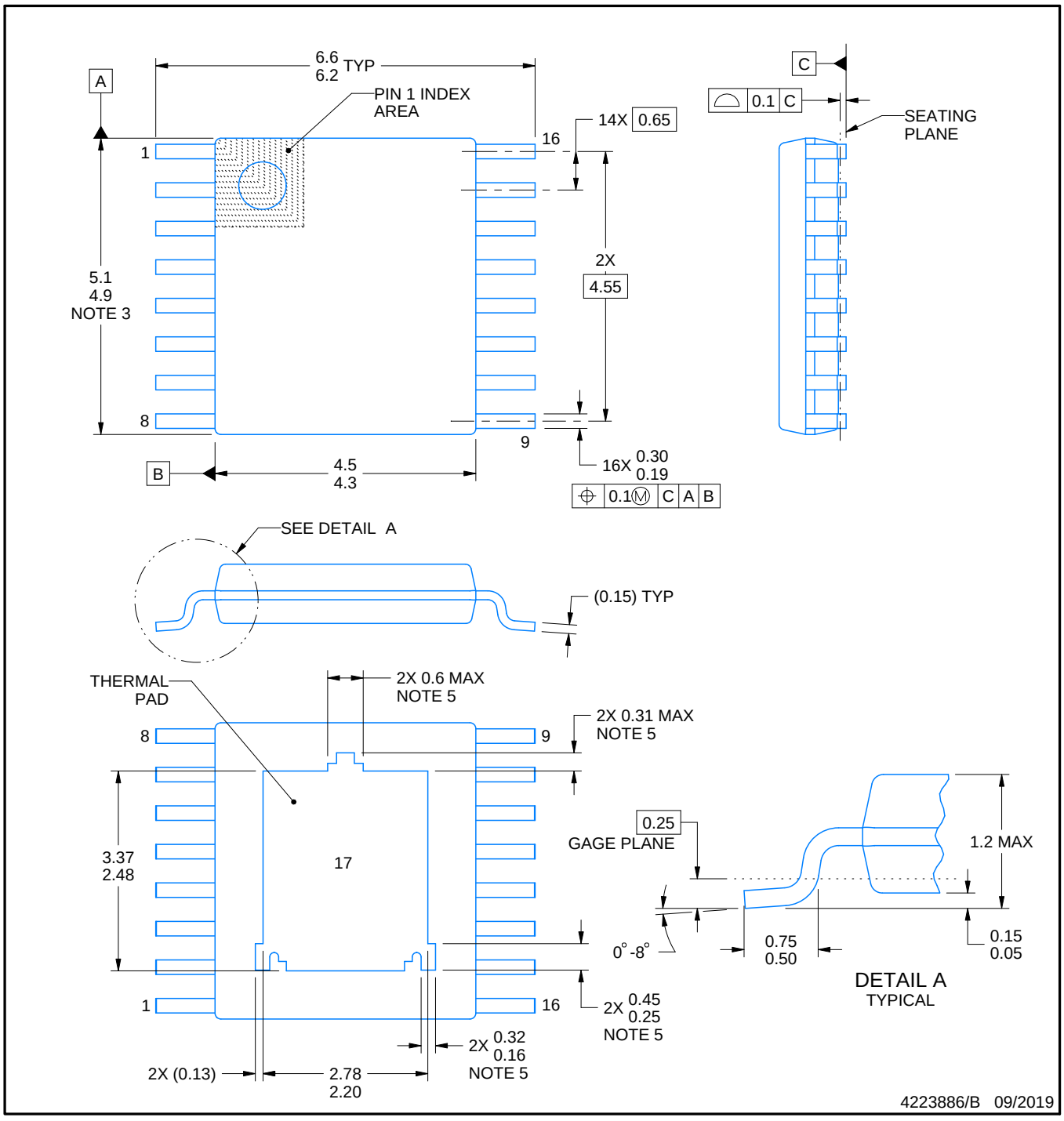
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PWP0016M

PowerPAD™ TSSOP - 1.2 mm max height

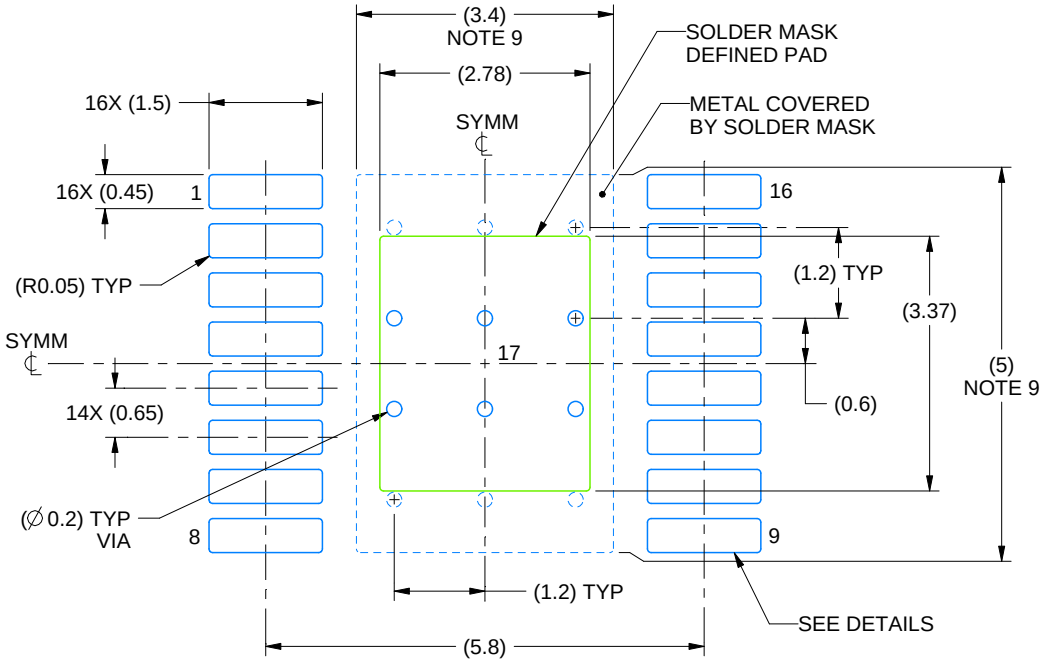
SMALL OUTLINE PACKAGE



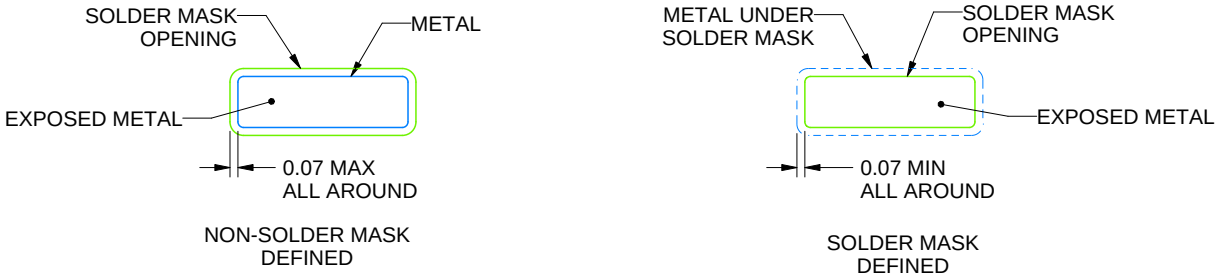
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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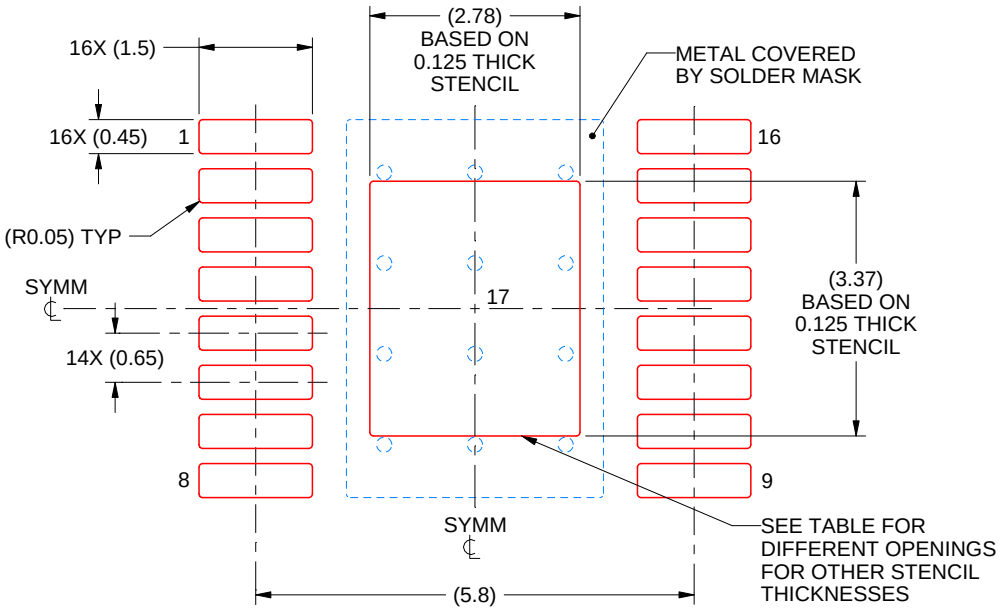
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.11 X 3.77
0.125	2.78 X 3.37 (SHOWN)
0.15	2.54 X 3.08
0.175	2.35 X 2.85

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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