TPS7H2201SP and TPS7H2201-SEP Radiation Hardened 1.5V to 7V, 6A eFuse

1 Features

- Standard micro circuit available, SMD 5962R17220
- Vendor item drawing available, VID V62/23608
- Radiation performance:
  - Radiation hardness assurance (RHA) up to TID 100krad(Si)
  - Single event latchup (SEL), single event burnout (SEB), and single event gate rupture (SEGR) immune to LET = 75MeV-cm^2/mg
  - SEFI/SET characterized to LET = 75MeV-cm^2/mg
- Integrated single channel eFuse
- Input voltage range: 1.5V to 7V
- Low on-resistance (R_{ON}) of:
  - 35mΩ maximum at 25°C and VIN = 5V for CFP and KGD
  - 23mΩ maximum at 25°C and VIN = 5V for HTSSOP
- 6A maximum continuous switch current
- Low control input threshold enables use of 1.2, 1.8, 2.5, and 3.3V logic
- Configurable rise time (soft start)
- Reverse current protection
- Programmable and internal current limiting (fast-trip)
- Programmable fault timer (current limit and retry modes)
- Thermal shutdown
- Ceramic and plastic package with thermal pad

2 Applications

- Space satellite power management and distribution
- Radiation hardened and tolerant power tree applications
- Available in military (–55°C to 125°C) temperature range

3 Description

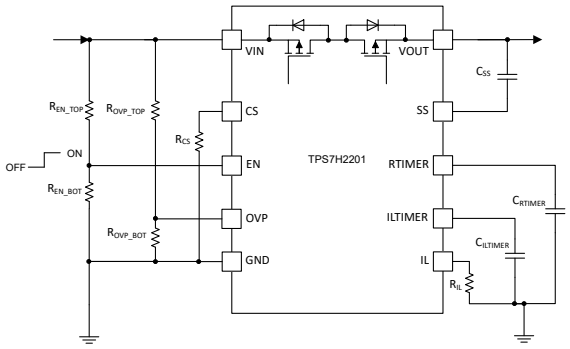
The TPS7H2201 is a single channel eFuse that provides configurable rise time to minimize inrush current and reverse current protection. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.5V to 7V and can support a maximum continuous current of 6A. The switch is controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals.

The TPS7H2201 is available in a ceramic and plastic package with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –55°C to 125°C.

Device Information

PART NUMBER(1)	GRADE	PACKAGE SIZE(4)
5962R1722001VXC	Flight grade RHA 100krad(Si)	16-pin CDFP 11.00 × 9.60mm Weight: 1.56g(3)
5962-1722001VXC	Flight grade QMLV	
TPS7H2201HKR/EM	Engineering samples(2)	
5962R1722002PYE	QMLP-RHA	32-pin HTSSOP 6.10 × 11.00mm Weight: 0.191g(3)
TPS7H2201MDAPTSEP	SEP	
TPS7H2201EVM-CVAL	Ceramic evaluation board	EVM

(1) For more information, see Section 12. Refer also to Device Options.
(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.
(3) Dimension and mass values are nominal.
(4) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Options

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H2201SP	TID of 100 krad(Si) RLAT, DSEE free to 75 MeV-cm^2/mg	QMLV-RHA	16-pin HKR CFP	5962R1722001VXC
		QMLP-RHA	32-pin DAP HTSSOP	5962R1722002PYE
		KGD (QMLV-RHA)	Die	5962R1722001V9A
	None	Engineering Model (3)	16-pin HKR CFP	PTS7H2201HKR/EM
			Die	TPS7H2201Y/EM
TPS7H2201-SEP	TID of 50 krad(Si) RLAT, DSEE free to 43 MeV-cm^2/mg	Space Enhanced Plastic	32-pin DAP HTSSOP	TPS7H2201MDAPTSEP

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.

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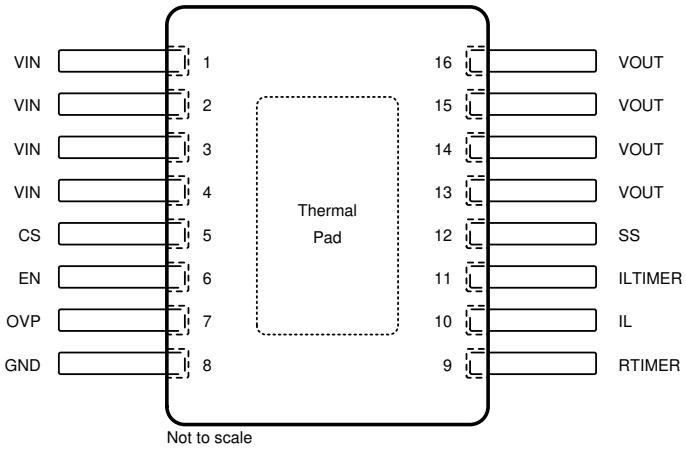
5 Pin Configuration and Functions

HKR Package
16-Pin CFP With Thermal Pad
Top View



DAP Package
32-Pin HTSSOP With Thermal Pad
Top View

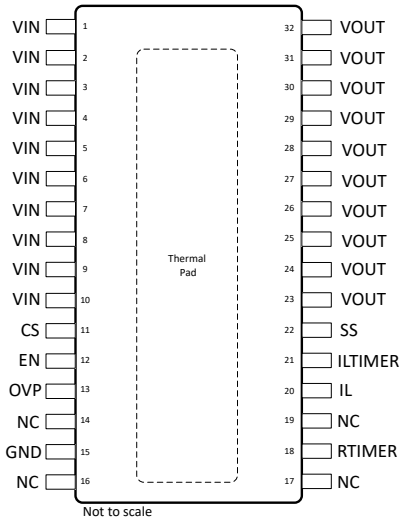


Table 5-1. Pin Functions

PIN			Type[1]	DESCRIPTION
HKR (16) NO.	PW (32) NO.	NAME		
1-4	1-10	VIN	I	Switch input. Requires a minimum 10µF input bypass capacitor for minimizing V_{IN} dip.
5	11	CS	O	Current sense pin proportional to output current. Connect a resistor to GND. Can leave floating if unused. Do not connect directly to GND.
6	12	EN	I	Active high switch control input. Do not leave floating.
7	13	OVP	I	Overvoltage protection. Programmable using an external resistor divider. If no OVP is desired, this pin must be connected to GND.
8	15	GND	—	Device ground. [2]
9	18	RTIMER	I/O	Capacitor programmed fault timer control during disabled and retry mode. Connecting this pin to GND holds the switch disabled until the EN pin is cycled. Do not float this pin or connect the pin to VIN.
10	20	IL	I/O	Current limiter control. Programmable using an external resistor to GND. Do not float this pin.
11	21	ILTIMER	I	Capacitor programmed fault timer control during current limiting mode. Connecting this pin to VIN uses the internal current limit timer and connecting this pin to GND disables the internal timer functionality for the ILTIMER as well as retry mode. In this case, the device remains at programmed current limit indefinitely in the event of a short without going intro retry mode. Do not float this pin.
12	22	SS	I/O	Switch slew rate control. See the *Section 8.3.2* section for more information.
13-16	23-32	VOUT	O	Switch output. Requires a minimum 10µF output capacitor.
	14,16,17,19	NC	—	No connect. This pin is not internally connected. Connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
	—	Thermal Pad	—	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND.

(1) I = Input, O = Output, I/O = Input or Output, — = Other
(2) Thermal pad is internally connected to the seal ring and GND for HKR option.

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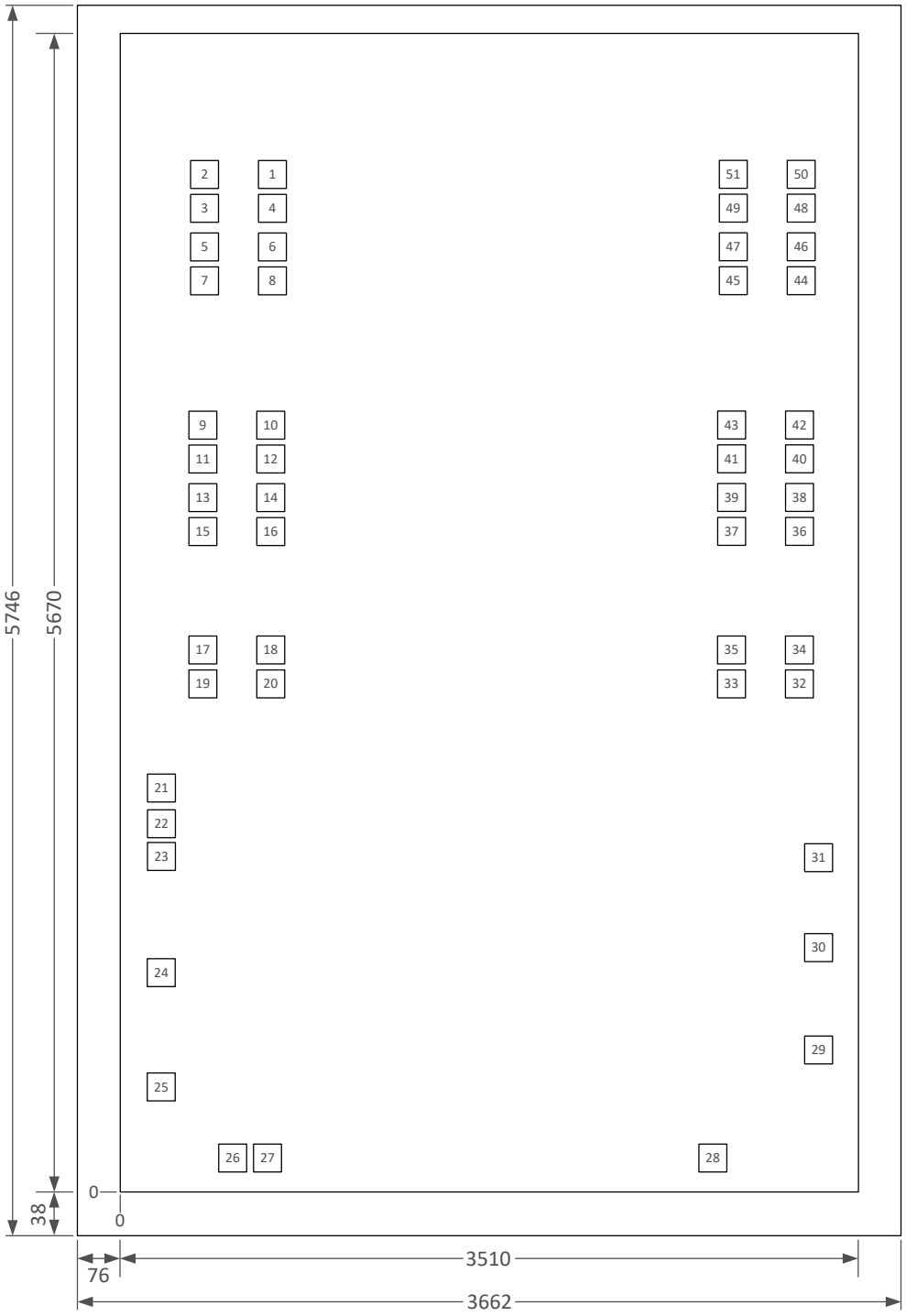
Table 5-2. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	ALCU	1050nm



1. All dimensions in microns (µm).
2. The inner rectangle is the die and the outer rectangle is the die plus scribe lines.

Table 5-3. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VIN	1	611.78	4976.1	751.73	5116.05
VIN	2	258.17	4976.1	398.12	5116.05
VIN	3	258.17	4809.15	398.12	4949.1
VIN	4	611.78	4809.15	751.73	4949.1
VIN	5	258.17	4641.39	398.12	4781.34
VIN	6	611.78	4641.39	751.73	4781.34
VIN	7	258.17	4473.59	398.12	4613.54
VIN	8	611.78	4473.59	751.73	4613.54
VIN	9	258.17	3647.7	398.12	3787.65
VIN	10	611.78	3647.7	751.73	3787.65
VIN	11	258.17	3480.75	398.12	3620.7
VIN	12	611.78	3480.75	751.73	3620.7
VIN	13	258.17	3312.99	398.12	3452.94
VIN	14	611.78	3312.99	751.73	3452.94
VIN	15	258.17	3145.19	398.12	3285.14
VIN	16	611.78	3145.19	751.73	3285.14
VIN	17	258.17	2315.57	398.12	2455.52
VIN	18	611.78	2315.57	751.73	2455.52
VIN	19	258.17	2146.37	398.12	2286.32
VIN	20	611.78	2146.37	751.73	2286.36
AVDD	21	54.99	1842.03	194.94	1981.98
AVDD	22	54.99	1671.48	194.94	1811.43
CS	23	54.99	1480.77	194.94	1620.72
EN	24	54.99	972.68	194.94	1112.63
OVP	25	54.99	406.26	194.94	546.21
GND	26	407.21	54.99	547.16	194.94
GND	27	577.76	54.99	717.71	194.94
RTIMER	28	2792.88	54.99	2932.83	194.94
IL	29	3315.06	587.43	3455.01	727.38
ILTIMER	30	3315.06	1099.26	3455.01	1239.21
SS	31	3315.06	1544.09	3455.01	1684.04
VOUT	32	3111.66	2146.37	3251.61	2286.32
VOUT	33	2758.05	2146.37	2898	2286.32
VOUT	34	3111.66	2315.57	3251.61	2455.52
VOUT	35	2758.05	2315.57	2898	2455.52
VOUT	36	3111.66	3145.19	3251.61	3285.14
VOUT	37	2758.05	3145.19	2898	3285.14
VOUT	38	3111.66	3312.99	3251.61	3452.94
VOUT	39	2758.05	3312.99	2898	3452.94
VOUT	40	3111.66	3480.75	3251.61	3620.7
VOUT	41	2758.05	3480.75	2898	3620.7
VOUT	42	3111.66	3647.7	3251.61	3787.65
VOUT	43	2758.05	3647.7	2898	3787.65
VOUT	44	3111.66	4473.59	3251.61	4613.54
VOUT	45	2758.05	4473.59	2898	4613.54

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Table 5-3. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VOUT	46	3111.66	4641.39	3251.61	4781.34
VOUT	47	2758.05	4641.39	2898	4781.34
VOUT	48	3111.66	4809.15	3251.61	4949.1
VOUT	49	2758.05	4809.15	2898	4949.1
VOUT	50	3111.66	4976.1	3251.61	5116.05
VOUT	51	2758.05	4976.1	2898	5116.05

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VIN	Input voltage	–0.3	7.5	V
VOUT	Output voltage	–0.3	7.5	V
EN, OVP	Enable and over voltage protection pins	–0.3	7.5	V
CS, ILTIMER, RTIMER, IL, SS	Current sense, current limit timer, retry timer, current limit and soft start pins	–0.3	VIN + 0.3	V
I_{MAX}	Maximum continuous switch current		9	A
I_{PLS}	Maximum pulsed switch current (t≤5µs)		45	A
T_J	Maximum junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Input voltage	1.5	7	V
SR_{VIN}	Input voltage slew rate		0.01	V/µs
VOUT	Output voltage	0	7 (1)	V
I_{MAX}	Maximum continuous switch current		6	A
T_J	Operating junction temperature(2)	–55	125	°C

(1) This maximum VOUT voltage is only applicable when the device is disabled (EN = Low). When the device is enabled (EN = High), the maximum VOUT voltage is the input voltage, VIN.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature can require derating. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation: $T_{A\ (max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.

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6.4 Thermal Information

THERMAL METRIC (1)		TPS7H2201-SP HKR (CFP) 16 PINS	TPS7H2201-SEP DAP (HTSSOP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	23.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	11.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	5.4	
ψ_{JT}	Junction-to-top characterization parameter	3.3	0.1	
ψ_{JB}	Junction-to-board characterization parameter	42.5	5.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	0.5	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics: All Devices

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP (1)	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
VIN_{HUVLO}	Internal VIN UVLO voltage, rising					1.32		V
VIN_{LUVLO}	Internal VIN UVLO voltage, falling					1.23		V
$HYST_{VIN-UVLO}$	Internal VIN UVLO hysteresis					92		mV
I_Q	Quiescent current	I_{OUT} = 0mA, V_{IN} = EN = 5V, CS resistor of 20 kΩ to GND		1, 2, 3		2.4	6.5	mA
I_F	VIN to VOUT forward leakage current	EN = VOUT = GND, measured VOUT current	1.5V ≤ VIN ≤ 7V	1, 2, 3			250	µA
			VIN =1.5V	1, 2, 3		3.27		
			VIN = 1.8V	1, 2, 3		3.35		
			VIN= 3.3V	1, 2, 3		3.62		
			VIN = 5V	1, 2, 3		4.11		
			VIN = 7V	1, 2, 3		6.82		
I_{SD} VIN	VIN off-state supply current	EN = GND, I_{OUT} = 0mA, measured VIN current	VIN = 5V	1, 2, 3		0.4	3	mA
			VIN = 3.3 V	1, 2, 3		0.3	3	
			VIN = 1.8 V	1, 2, 3		0.2	3	
			After TID = 100 krad, VIN = 1.8, 3.3, and 5V	1			3.1	
I_{RCP}	Reverse current protection leakage current	EN = 0V, VIN = 0V to 7V, VOUT = 0V to 7V for VOUT > VIN	SEP	1, 2, 3		0.45	2.5	mA
			QMLV, QMLP and KGD pre TID	1, 2, 3				
			QMLV, QMLP and KGD, after TID=100krad(Si)	1, 2, 3		0.45	20	
		EN = 7V, VIN = 0V, VOUT = 0V to 7V	SEP	1, 2, 3		0.45	2.5	
			QMLV, QMLP and KGD pre TID	1, 2, 3				
			QMLV, QMLP and KGD, after TID=100krad(Si)	1, 2, 3		0.45	20	

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6.5 Electrical Characteristics: All Devices (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP (1)	MIN	TYP	MAX	UNIT
SOFT START								
I_{SS}	Soft start charge current	1V on SS pin		1, 2, 3		65	83	µA
SR_{SS}	Soft start slew rate	SS pin floating, COUT = 10 µF				295		mV/µs
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT								
V_{IHEN}	EN/UVLO threshold voltage, rising			1, 2, 3	0.56	0.61	0.65	V
V_{ILEN}	EN/UVLO threshold voltage, falling			1, 2, 3	0.47	0.51	0.55	V
$HYST_{EN}$	EN/UVLO hysteresis voltage			1, 2, 3		93	124	mV
t_{LOW}	EN signal low time during cycling	RTIMER = GND, IL = 1 A, I_{VOUT} = 2 A	See Figure 8-3	9, 10, 11	20			µs
VIN_{EN}	VIN percentage for enable(2)			4, 5, 6	75%			
I_{EN}	EN pin input leakage current	EN = VIN = 5V		1, 2, 3			12	nA
OVERVOLTAGE PROTECTION (OVP)								
V_{OVPR}	OVPR threshold voltage, rising			1, 2, 3	0.52	0.57	0.63	V
V_{OVPF}	OVPF threshold voltage, falling			1, 2, 3	0.5	0.55	0.59	V
$HYST_{OVP}$	OVP hysteresis voltage	1.6V < VIN < 7V		1, 2, 3		20	55	mV
I_{OVP}	OVP pin input leakage current			1, 2, 3			15	nA
CURRENT LIMIT AND CURRENT SENSE								
t_{CSEN}	Time for valid CS output after enable	C_{SS} = 120nF		9, 10, 11			5	ms
Minimum VOUT current for valid CS output				1, 2, 3	750			mA
VOUT current change to CS change delay time		0.5A rising step, 100mA/µs, 1.5V ≤ VIN ≤ 7V		9, 10, 11		16	74	µs
VOUT current change to CS change delay time		0.5A falling step, 100mA/µs, 1.5V ≤ VIN ≤ 7V		9, 10, 11		16	73	µs
CS pin accuracy		0.75 A ≤ I_{VOUT} ≤ 7.5 A		4, 5, 6	–10%		10%	
CS pin voltage		0.75 A ≤ I_{VOUT} ≤ 7.5 A, no OCP		1, 2, 3			VIN – 0.4	V
Current limit setting, I_{IL}		I_{VOUT} ≤ 1 A		1, 2, 3	I_{VOUT} + 0.5			A
		1A < I_{VOUT} ≤ 3 A		1, 2, 3	I_{VOUT} + 1			
		I_{VOUT} > 3 A		1, 2, 3	I_{VOUT} + 1.5			
Programmable current limit accuracy		1.5V ≤ VIN ≤ 7V		4, 5, 6	–20%		20%	
Fast trip off current limit		VIN = 5V, 10mΩ short in 10 µs				22		A
TIMERS								
$I_{ILTIMER}$	ILTIMER charge current			1, 2, 3	0.7	1	1.38	µA
$PD_{ILTIMER}$	ILTIMER internal pull-down resistance	40mV on ILTIMER pin		1, 2, 3		38	153	Ω
I_{RTIMER}	RTIMER charge current			1, 2, 3	0.7	1	1.38	µA
PD_{RTIMER}	RTIMER internal pull-down resistance	40mV on RTIMER pin		1, 2, 3		38	153	Ω
THERMAL SHUTDOWN								
Thermal shutdown		VIN = 5V				175		°C
Thermal shutdown hysteresis		VIN = 5V				20		°C

(1) For subgroup definitions, see Quality Conformance Inspection table.
(2) VIN must be ≥ 75% of its final value before EN is asserted only if VIN_{SR} > $VOUT_{SR}$.

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6.6 Electrical Characteristics: CFP and KGD Options

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP(1)	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
CURRENT LIMIT AND CURRENT SENSE								
Fast trip off off-time (2)		VIN = 5V, C_{SS} = 2.7nF		9, 10, 11		61	158	µs
Internal current limit timer (fast trip off current limit) (2)		VIN = 5V, I_{VOUT} = 3 A, IL = 6 A, ILTIMER = VIN, 10mΩ short in 10 µs		9, 10, 11		15	35	µs
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance, lead length = 2.5mm	VIN = 7V, I_{IL} = 7.5 A	–55°C	1, 2, 3			24	mΩ
			–40°C				26	
			25°C			31	34	
			85°C			37	40	
			125°C			41	45	
		VIN = 5V, I_{IL} = 7.5 A	–55°C	1, 2, 3			26	
			–40°C				27	
			25°C			32	35	
			85°C			39	42	
			125°C			43	47	
		VIN = 3.3V, I_{IL} = 7.5 A	–55°C	1, 2, 3			28	
			–40°C				30	
			25°C			35	38	
			85°C			42	46	
			125°C			47	52	
		VIN = 1.8V, I_{IL} = 7.5 A	–55°C	1, 2, 3			36	
			–40°C				39	
			25°C			45	51	
			85°C			55	62	
			125°C			61	70	
		VIN = 1.5V, I_{IL} = 7.5 A	–55°C	1, 2, 3			44	
			–40°C				48	
			25°C			52	63	
			85°C			63	77	
			125°C			70	87	

(1) For subgroup definitions, see Quality Conformance Inspection table.
(2) Bench verified; not tested in production

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6.7 Electrical Characteristics: HTSSOP Option

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
CURRENT LIMIT AND CURRENT SENSE								
Fast trip off off-time		VIN = 5V, C_{SS} = 2.7nF		9, 10, 11		61		µs
Internal current limit timer (fast trip off current limit)		VIN = 5V, I_{VOUT} = 3 A, IL = 6 A, ILTIMER = VIN, 10mΩ short in 10 µs		9, 10, 11		15		µs
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	VIN = 7V, I_{IL} = 7.5 A	–55°C	1, 2, 3		15.9	17	mΩ
			–40°C			16.9		
			25°C			19.9	21	
			85°C			22.9		
			125°C			25	27	
		VIN = 5V, I_{IL} = 7.5 A	–55°C	1, 2, 3		17	18	
			–40°C			18		
			25°C			21.4	23	
			85°C			24.8		
			125°C			27	29	
		VIN = 3.3V, I_{IL} = 7.5 A	–55°C	1, 2, 3		19.2	21	
			–40°C			20.4		
			25°C			24.5	26	
			85°C			28.5		
			125°C			31.2	33	
		VIN = 1.8V, I_{IL} = 7.5 A	–55°C	1, 2, 3		27.1	29	
			–40°C			28.7		
			25°C			34.9	37	
			85°C			41		
			125°C			44.9	48	
		VIN = 1.5V, I_{IL} = 7.5 A	–55°C	1, 2, 3		33	36	
			–40°C			35		
			25°C			42.7	46	
			85°C			46.2		
			125°C			55	59	

(1) For subgroup definitions, see Quality Conformance Inspection table.

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6.8 Switching Characteristics (All Devices)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = EN = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		208		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		60		µs
t_F	VOUT fall time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		90		µs
t_{ASSERT}	OVP assert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		4.5		µs
$t_{DEASSERT}$	OVP deassert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9.6		µs
VIN = EN = 1.5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		173		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		64		µs
t_F	VOUT fall time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		70		µs
t_{ASSERT}	OVP assert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		2.65		µs
$t_{DEASSERT}$	OVP deassert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		6.56		µs

6.9 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

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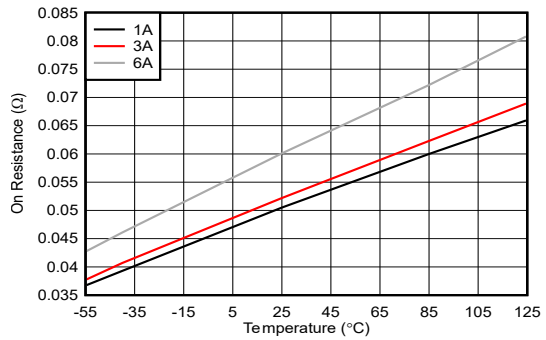
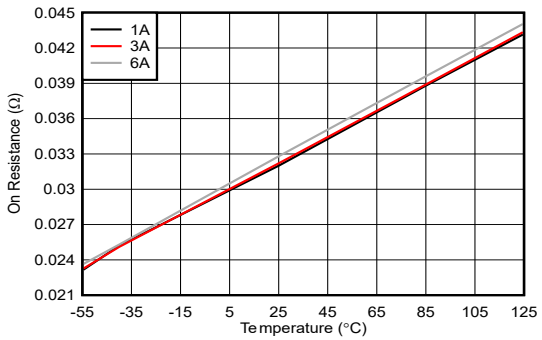
6.10 Typical Characteristics



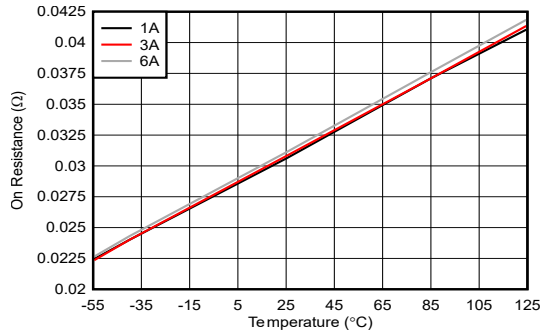
I_{IL} = 7.5A

Figure 6-1. On-Resistance vs Temperature Across Loads for CFP and KGD at VIN = 1.5V



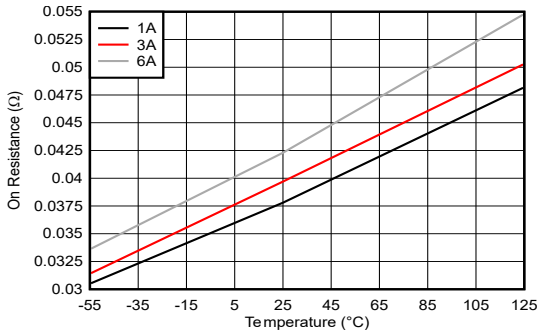
I_{IL} = 7.5A

Figure 6-2. On-Resistance vs Temperature Across Loads for CFP and KGD at VIN = 5V



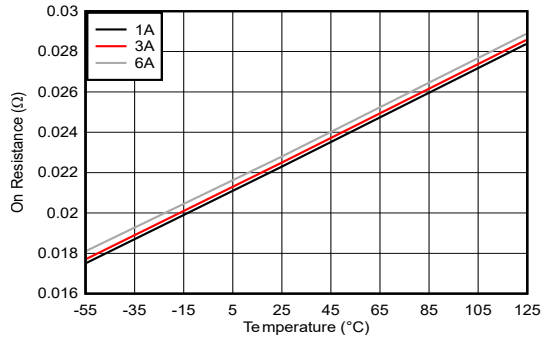
I_{IL} = 7.5A

Figure 6-3. On-Resistance vs Temperature Across Loads for CFP and KGD at VIN = 7V



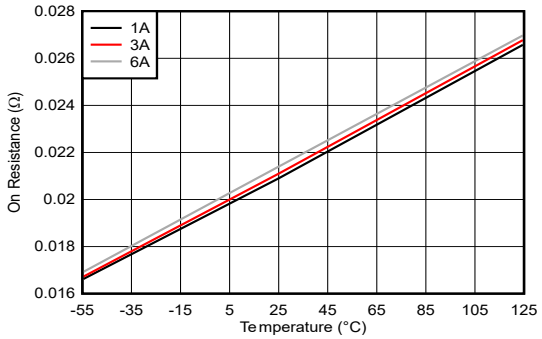
I_{IL} = 7.5A

Figure 6-4. On-Resistance vs Temperature Across Loads for HTSSOP at VIN = 1.5V



I_{IL} = 7.5A

Figure 6-5. On-Resistance vs Temperature Across Loads for HTSSOP at VIN = 5V



I_{IL} = 7.5A

Figure 6-6. On-Resistance vs Temperature Across Loads for HTSSOP at VIN = 7V

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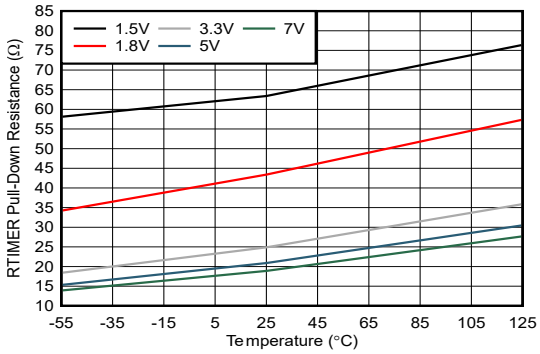

Figure 6-7. RTIMER Pull-Down Resistance vs Temperature Across VIN

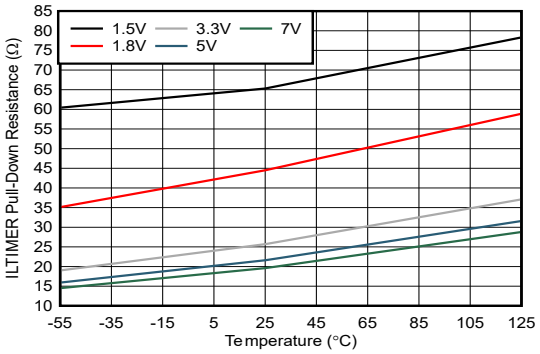

Figure 6-8. ILTIMER Pull-Down Resistance vs Temperature Across VIN

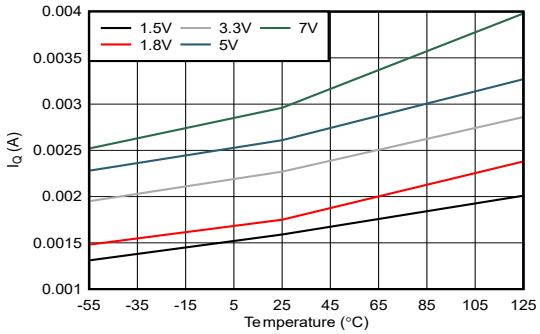

Figure 6-9. I_Q vs Temperature Across VIN

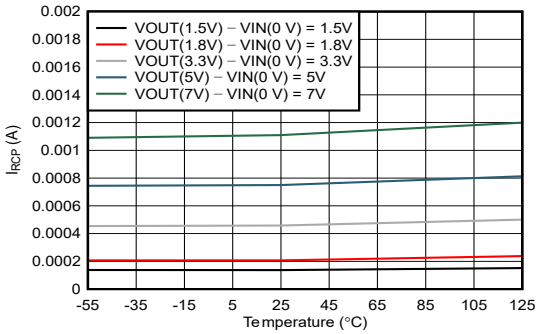

Figure 6-10. I_{RCP} vs Temperature With EN = 7V

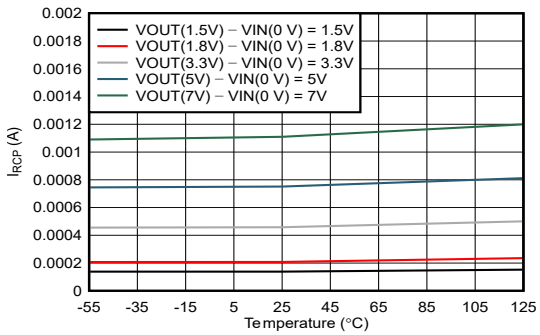

Figure 6-11. I_{RCP} vs Temperature With EN = GND

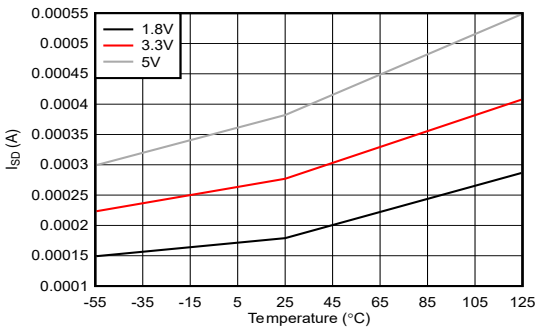

Figure 6-12. I_{SD} VIN vs Temperature Across VIN

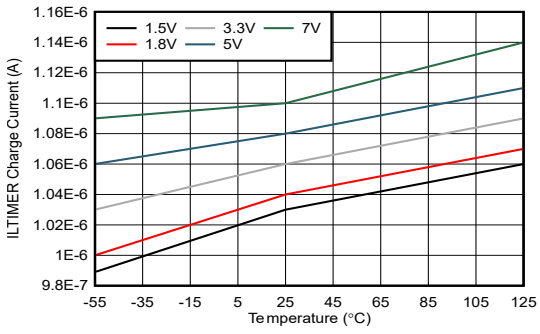

Figure 6-13. ILTIMER Charge Current vs Temperature Across VIN

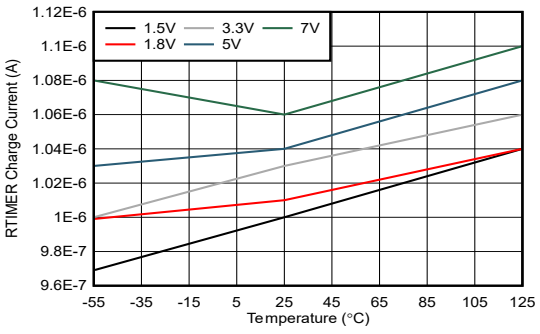

Figure 6-14. RTIMER Charge Current vs Temperature Across VIN

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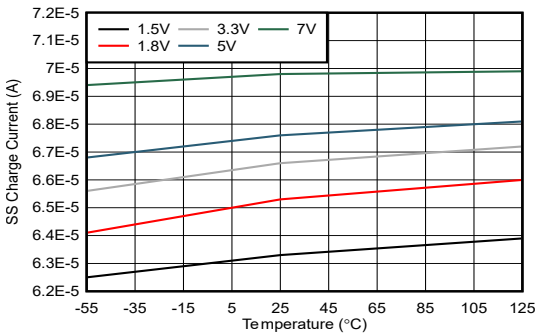
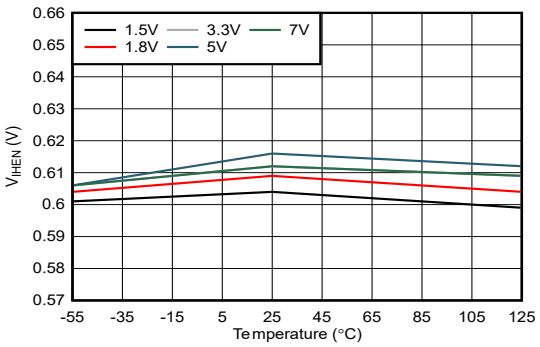
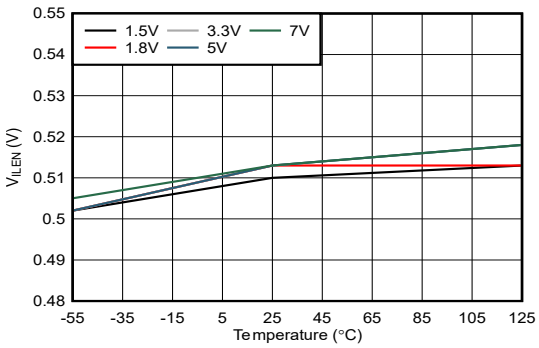


Figure 6-15. SS Charge Current vs Temperature Across VIN



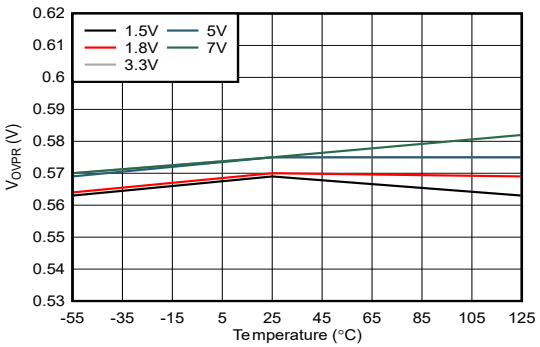
EN pin driven directly

Figure 6-16. V_{IHEN} vs Temperature Across VIN



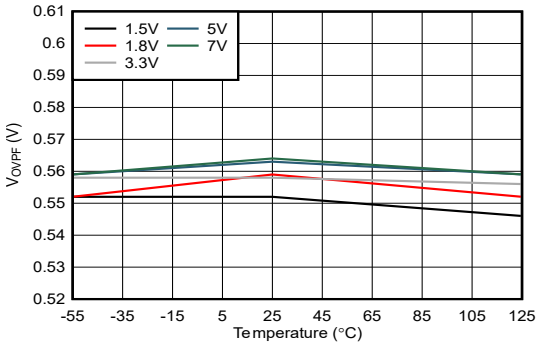
EN pin driven directly

Figure 6-17. V_{ILEN} vs Temperature Across VIN



OVP pin driven directly
Waveform at 3.3V is obscured by the 5V

Figure 6-18. V_{OVPR} vs Temperature Across VIN



OVP pin driven directly

Figure 6-19. V_{OVPF} vs Temperature Across VIN

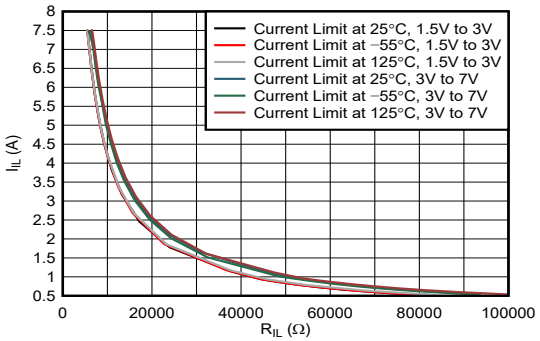


Figure 6-20. I_{IL} vs R_{IL} Across Temperature

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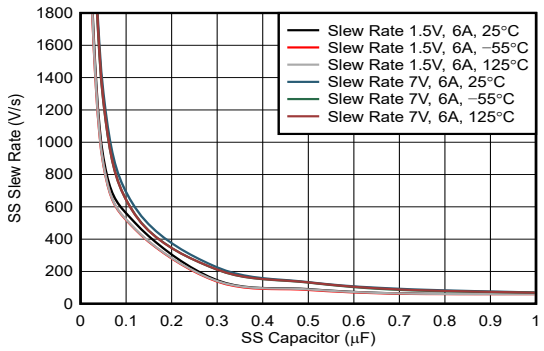

Figure 6-21. SS Slew Rate vs SS Capacitor Across Temperature

7 Parameter Measurement Information

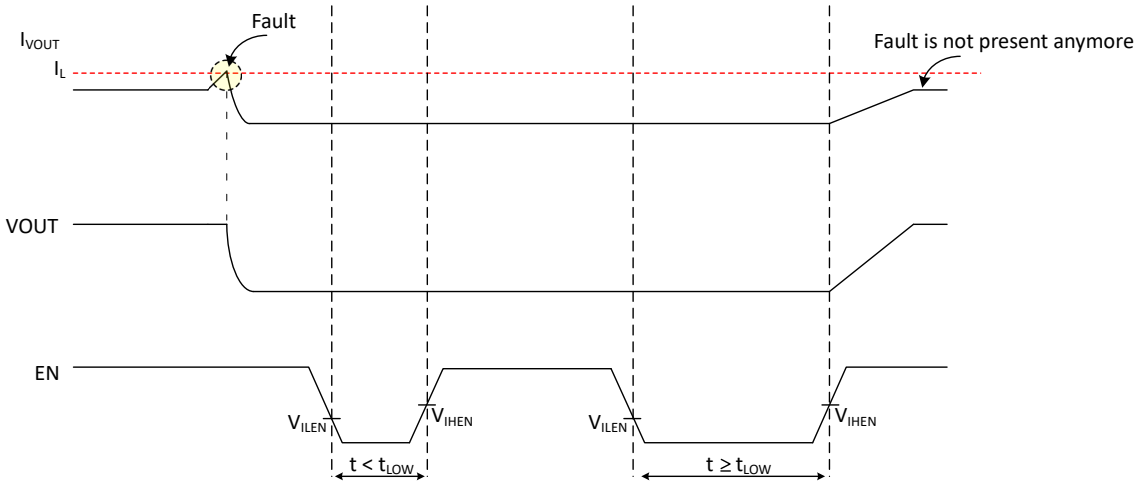

Figure 7-1. EN Signal Low Time to Restart Device (t_{LOW})

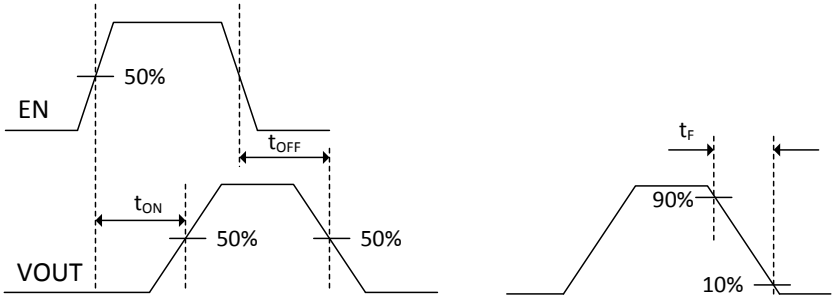

Figure 7-2. Turn-On (t_{ON}), Turn-Off (t_{OFF}) and VOUT Fall Time (t_F) Waveforms

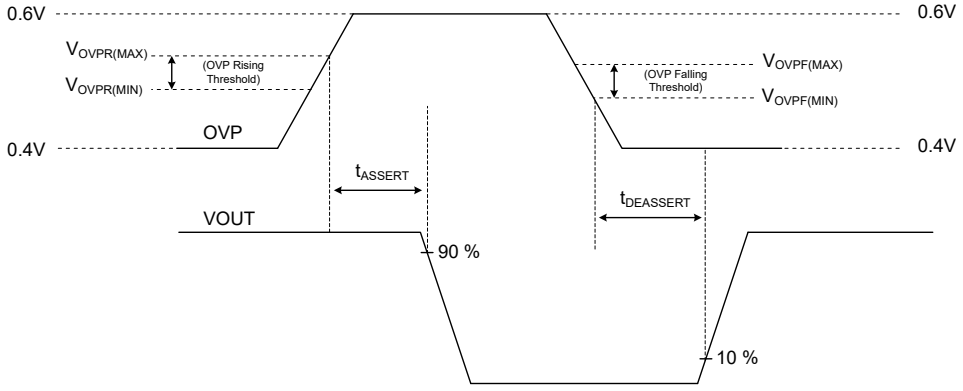

Figure 7-3. OVP Assert (t_{ASSERT}) and OVP Deassert ($t_{DEASSERT}$) Waveforms

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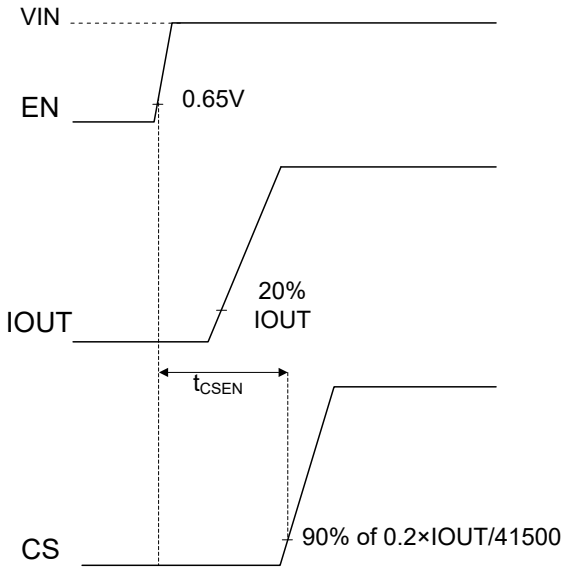

Figure 7-4. t_{CSEN} Waveforms

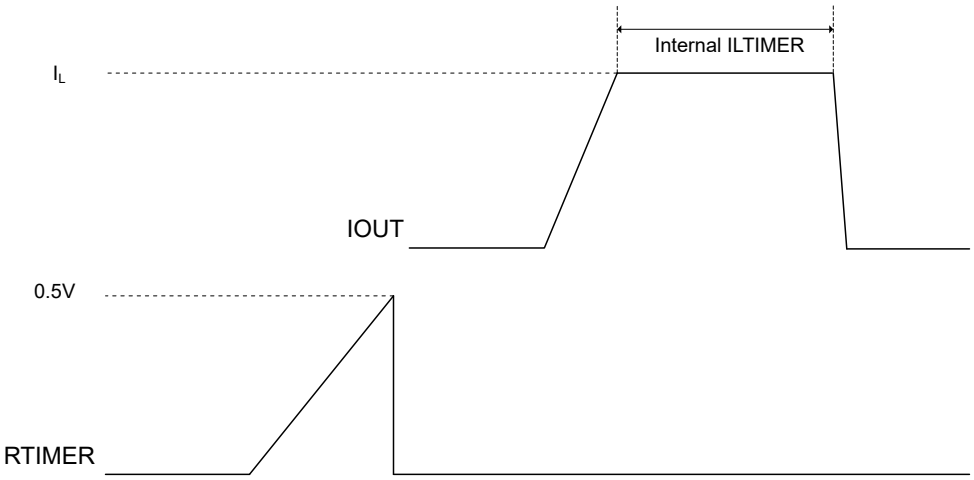

Figure 7-5. Internal ILTIMER Waveforms

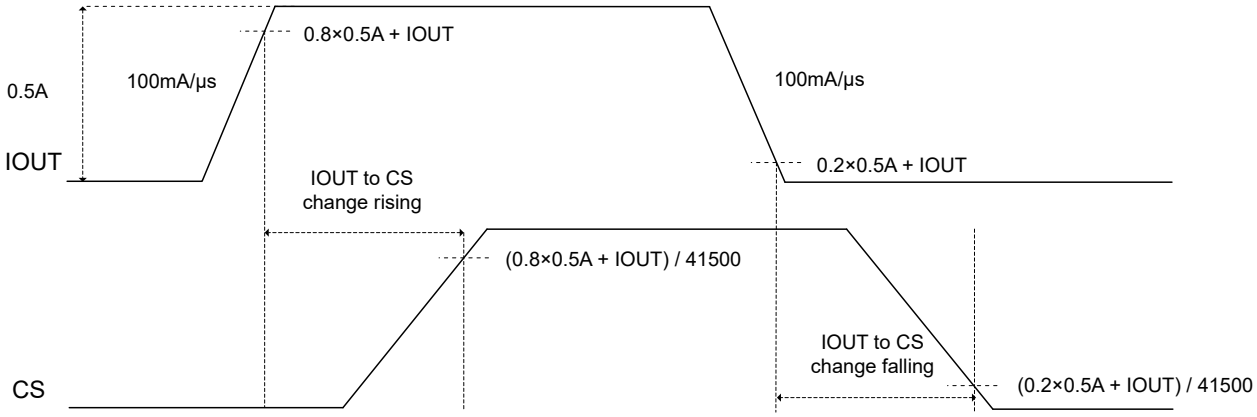

Figure 7-6. VOUT Current to CS Change Delay Time

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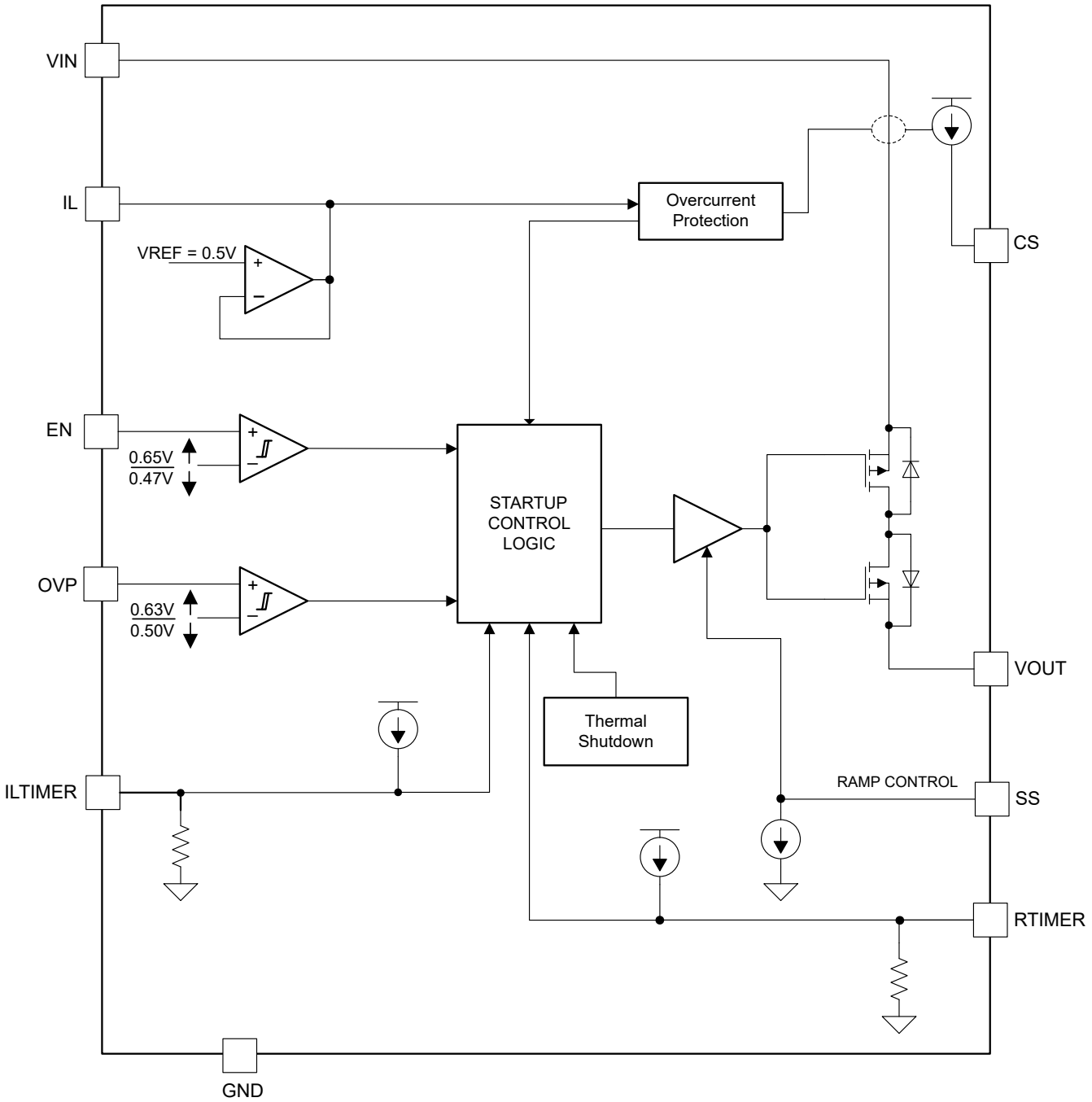
8 Detailed Description

8.1 Overview

The TPS7H2201 device is a single channel, 6A eFuse with a programmable slew rate for applications that require specific rise-time as well as programmable current limit for protection purposes. In addition, the TPS7H2201 features a reverse current protection capability for power distribution applications.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Enable, Undervoltage, and Overvoltage Protection

Figure 8-1 shows how resistor dividers from VIN connected to the EN and OVP pins can be used to set the UVLO and OVP trip voltages. The EN pin controls the ON and OFF state of the internal FET. A voltage at this pin greater than V_{IHEN} turns on the FET and a voltage less than V_{ILEN} turns the FET off. The addition of an external resistor divider from VIN allows the EN pin to configure a different enable rising voltage or an undervoltage monitor (UVLO) based on the V_{IHEN} and V_{ILEN} specifications respectively. Typically, applications are optimized to either configure the enable rising voltage or the UVLO threshold. As an example, Equation 1 can be used to calculate the UVLO trip point fixing R_{TOP_EN} = 100kΩ.

In a similar way to the EN pin, the overvoltage protection (OVP) feature of the device can be configured using a resistor divider from VIN connected to the OVP pin. The trip voltage for the OVP has to be less than the absolute maximum VIN voltage. A voltage at the OVP pin greater than V_{OVPR} trips the OVP feature and turns off the FET and a voltage less than V_{OVPF} keeps the FET on. If this feature is not desired, the OVP pin must be grounded. Equation 2 can be used to calculated the rising OVP trip point fixing R_{TOP_OVP} = 100kΩ.

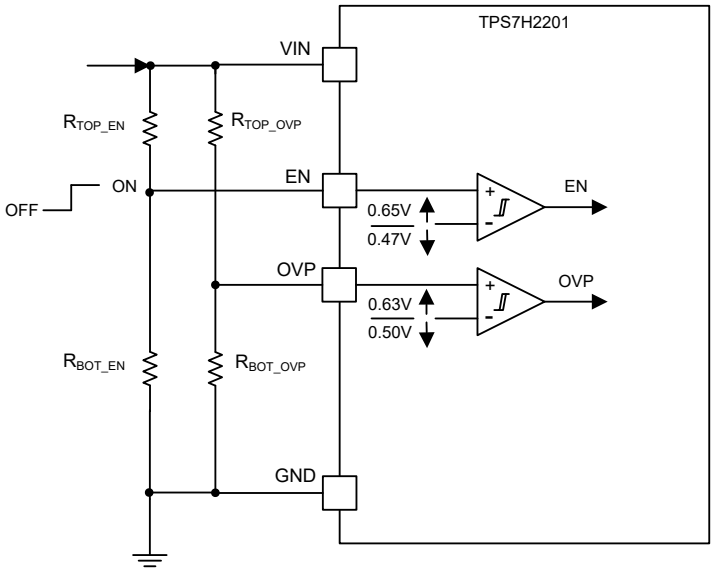

Figure 8-1. UVLO and OVP Thresholds Set by Resistor Dividers

$$R_{BOT_EN}(k\Omega) \leq \frac{47}{V_{UV_{TRIP}}(V) - 0.47} \quad (1)$$

$$R_{BOT_OVP}(k\Omega) \leq \frac{63}{V_{OVP_{TRIP}}(V) - 0.63} \quad (2)$$

8.3.2 Adjustable Rise Time

An external capacitor, C_{SS}, connected between the VOUT and SS pins sets the slew rate. The desired slew rate $VOUT_{SR}$ is determined by t_r, the rise time in seconds, and ΔV, the change in VOUT voltage in Volts as shown in Equation 3.

$$VOUT_{SR}(V/s) = \frac{\Delta V_{OUT}(V)}{t_r(s)} \quad (3)$$

To avoid false trips due to the programmable current limit, the desired slew rate must be less than $VOUT_{SR,MAX}$ as shown in Equation 4, where I_L is the programmed current limit, I_{VOUT} is the normal operation current flowing through the switch, and C_{OUT} is the output capacitor.

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$$VOUT_{SR,\,MAX}(V/s) < \frac{0.8 \times I_L - 0.95 \times I_{VOUT}(A)}{C_{OUT}(F)} \quad (4)$$

Once the slew rate has been calculated and meeting the constraint in Equation 4, the C_{SS} capacitor is then calculated using Equation 5 for VIN < 3V and IOUT ≥ 3A applications. For all other applications, use Equation 6.

For VIN < 3V and IOUT ≥ 3A:

$$C_{SS}(\mu F) = \frac{45}{VOUT_{SR}(V/s)} \quad (5)$$

For all other conditions:

$$C_{SS}(\mu F) = \frac{I_{SS}}{VOUT_{SR}(V/s)} \quad (6)$$

where:

- I_{SS} = 65

8.3.3 Programmable Current Limiting

A current limit can be programmed using an external resistor connected from the IL pin to GND. This programmed current limit (±20% accurate) refers to the continuous current through the device and therefore, when operated at the maximum current rating (6A), the programmed current limit needs to be set 20% higher. The programmable current limit protects against soft shorts as shown in Figure 8-3. Calculate the current limit resistor value, R_{IL}, in ohms using Equation 7 for VIN ≤ 3V, and Equation 8 for VIN > 3V, where I_L is the programmed current limit value in amperes.

For VIN ≤ 3V:

$$R_{IL}(\Omega) = \frac{45500}{I_L(A)} \quad (7)$$

For VIN > 3V:

$$R_{IL}(\Omega) = \frac{49000}{I_L(A)} \quad (8)$$

This programmable current limiting feature is different from the internal current limiting activated during fast trip mode as shown in Figure 8-4. A current limit event in this case is defined as a hard short and this current limit (typical of 22A) cannot be programmed.

8.3.4 Programmable Fault Timer

The TPS7H2201SP contains two programmable fault timers, the *current limit timer* and the *retry timer* controlled by ILTIMER and RTIMER pins respectively.

The *current limit timer* controls the time the device remains in current limit mode in the event of an overcurrent event. The device remains in current limit mode until the fault is removed or until the programmable current limit fault time, $t_{ILTIMER}$, expires. $t_{ILTIMER}$ is programmed using capacitor $C_{ILTIMER}$ connected from ILTIMER to GND and can be calculated using Equation 9. The ILTIMER pin charges the capacitor to 0.5V during an overload condition and discharges the capacitor otherwise through an internal pull down resistance. Connecting this pin to GND disables the internal timer functionality completely and therefore, in the case of a short, the device remains at the programmed current limit indefinitely. Connecting this pin to VIN causes the device to be disabled once the internal current limit timer expires as shown in Figure 7-5. When using the internal timer, the programmable current limit does not always have time to settle to the programmed value. Because of this, the programmable current limit can briefly fall outside of the defined accuracy threshold. The fast trip off current limit, remains valid. Table 8-1 summarizes the current limit fault duration time based on the pin conditions.

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The *retry timer* controls the time that the device remains disabled (switch turned off) after the current limit timer expires. The device remains disabled until the programmable retry time, t_{RTIMER}, expires. After t_{RTIMER} expires, the device attempts to restart. t_{RTIMER} is programmed using capacitor C_{RTIMER} connected from RTIMER to GND and can be calculated using Equation 9. The RTIMER pin charges the capacitor to 0.5V after the switch is turned off and discharges the capacitor otherwise. Connecting this pin to GND keeps the device disabled and requires the device to be enabled by cycling the EN pin (Refer to EN Signal Low Time to Restart Device (t_{LOW})). Table 8-2 summarizes the retry time based on the pin conditions.

$$t(\mu s) = \frac{C(pF)}{2} \tag{9}$$

The programmable fault timers, ILTIMER and RTIMER, must be set in such a way that the capacitor for one timer is discharged before the other timer expires to provide proper operation. Figure 8-2 shows a situation where this constraint is not met as the RTIMER is much larger than the ILTIMER and therefore, the C_{RTIMER} is not discharged before the $C_{ILTIMER}$ reaches 0.5V, which is when the ILTIMER expires. To avoid this situation, the constraint shown in Equation 10 must be met. Using this equation, once a capacitor for a timer has been selected (C_1 in Equation 10), the maximum value for the capacitor of the second timer can be determined. In the specific case of using the internal ILTIMER, the RTIMER capacitor must be sized such that the capacitor is discharged before the internal ILTIMER expires, assuming the fault is still present. The internal pull-down resistance for each of the timers can be found in the *Electrical Characteristics: All Devices* table. For the situation shown in Figure 8-2, C_1 and R_{PD1} in Equation 10 correspond to the RTIMER.

$$C_1(\mu F) < \frac{C_2(pF)}{8 \times R_{PD1}(\Omega)} \tag{10}$$

Table 8-1. Fault Time Duration for ILTIMER Pin Conditions

ILTIMER Pin Condition	Fault Time Duration During Overload
VIN (Internal Timer)	15µs (typ), 35µs (max)
GND (Disabled)	Indefinitely
Capacitor to GND ($C_{ILTIMER}$) (Programmed)	Equation 9
Float	Not valid (do not float pin)

Table 8-2. Time to Retry During an Overload Condition for RTIMER Pin Conditions

RTIMER Pin Condition	Time to Retry During an Overload
GND (Disabled)	Disabled (switch off) until EN is low for t > t_{LOW} (20µs)
Capacitor to GND (C_{RTIMER}) (Programmed)	Equation 9
Float	Not valid (do not float pin)

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Examples of different faults types and fault timer configurations are shown in the following diagrams:

- Figure 8-2: Programmable fault timer capacitors constraint
- Figure 8-3: Single soft short event using the current limit timer and the retry timer.
- Figure 8-4: Single hard short event using the current limit timer and the retry timer.
- Figure 8-5: Hard short event using the internal current limit timer and disabling retry timer.

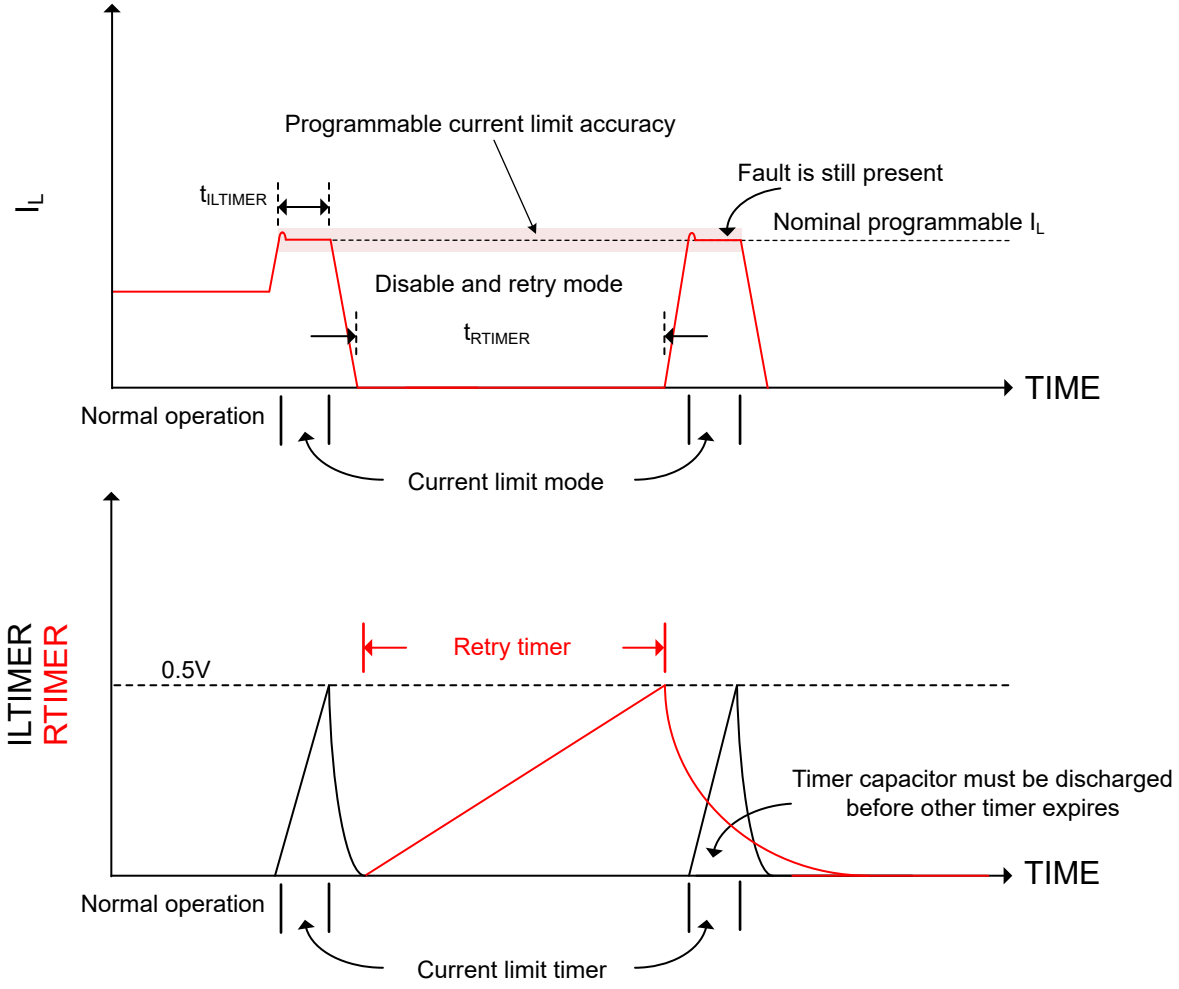

Figure 8-2. Programmable Fault Timer Capacitors Constraint

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The behavior of the ILTIMER and RTIMER pins for a soft short (one in which the programmable current limit is reached and responds) is shown in Figure 8-3. In this figure, the fault is assumed to not be present after the switch has been disabled and enabled again (retry mode). If the fault is present after the retry mode, the device goes into current limit mode and this cycle repeats until the fault is no longer present.

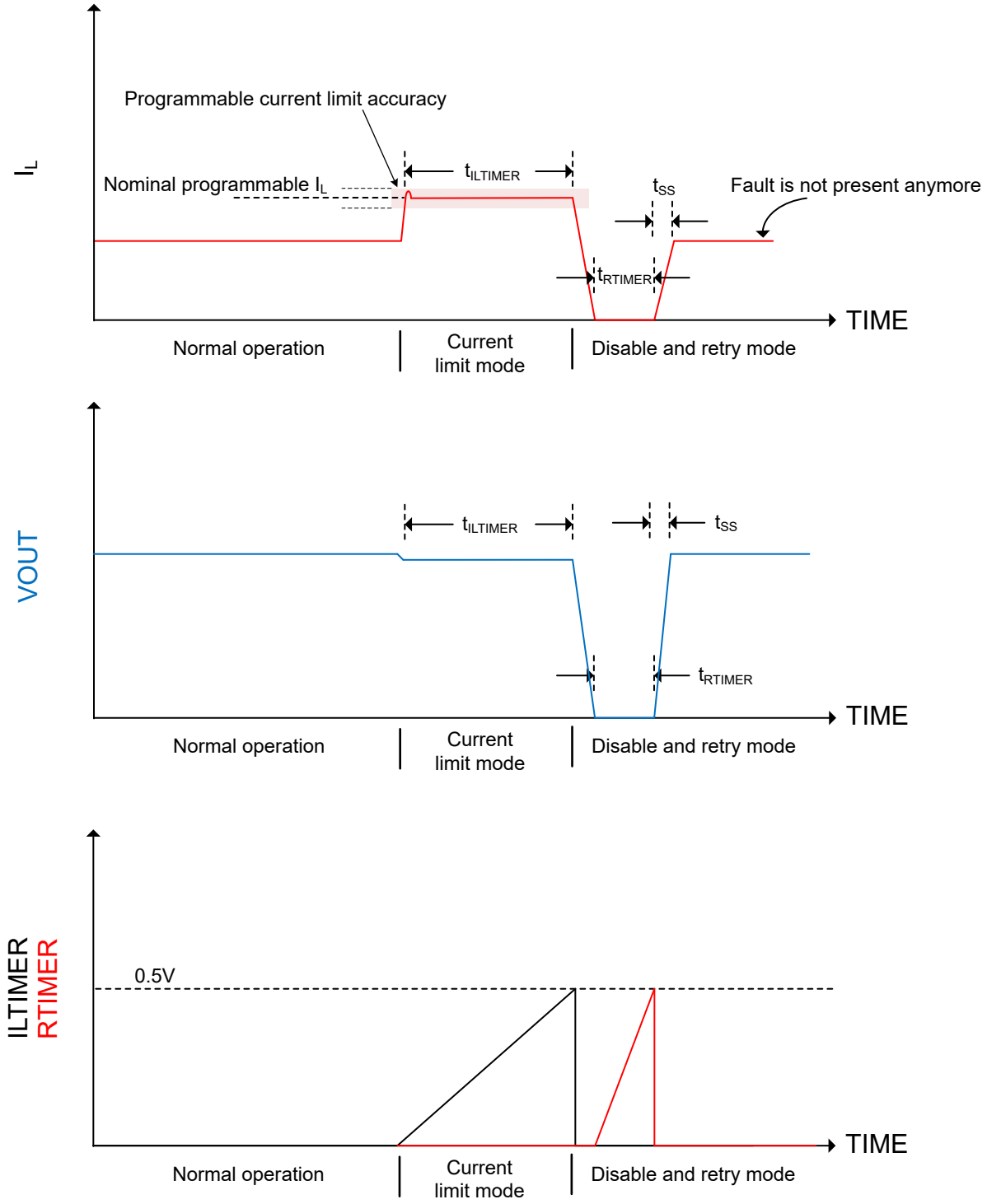

Figure 8-3. Soft Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

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The behavior of the ILTIMER and RTIMER pins for a hard short (one in which the fast current limit responds before the programmable current limit has time to respond) is shown in Figure 8-4. In this figure, the fault is assumed to not be present after the switch has been disabled and enabled again (retry mode). If the fault is present after the retry mode, the device goes into current limit mode and this cycle repeats until the fault is no longer present.

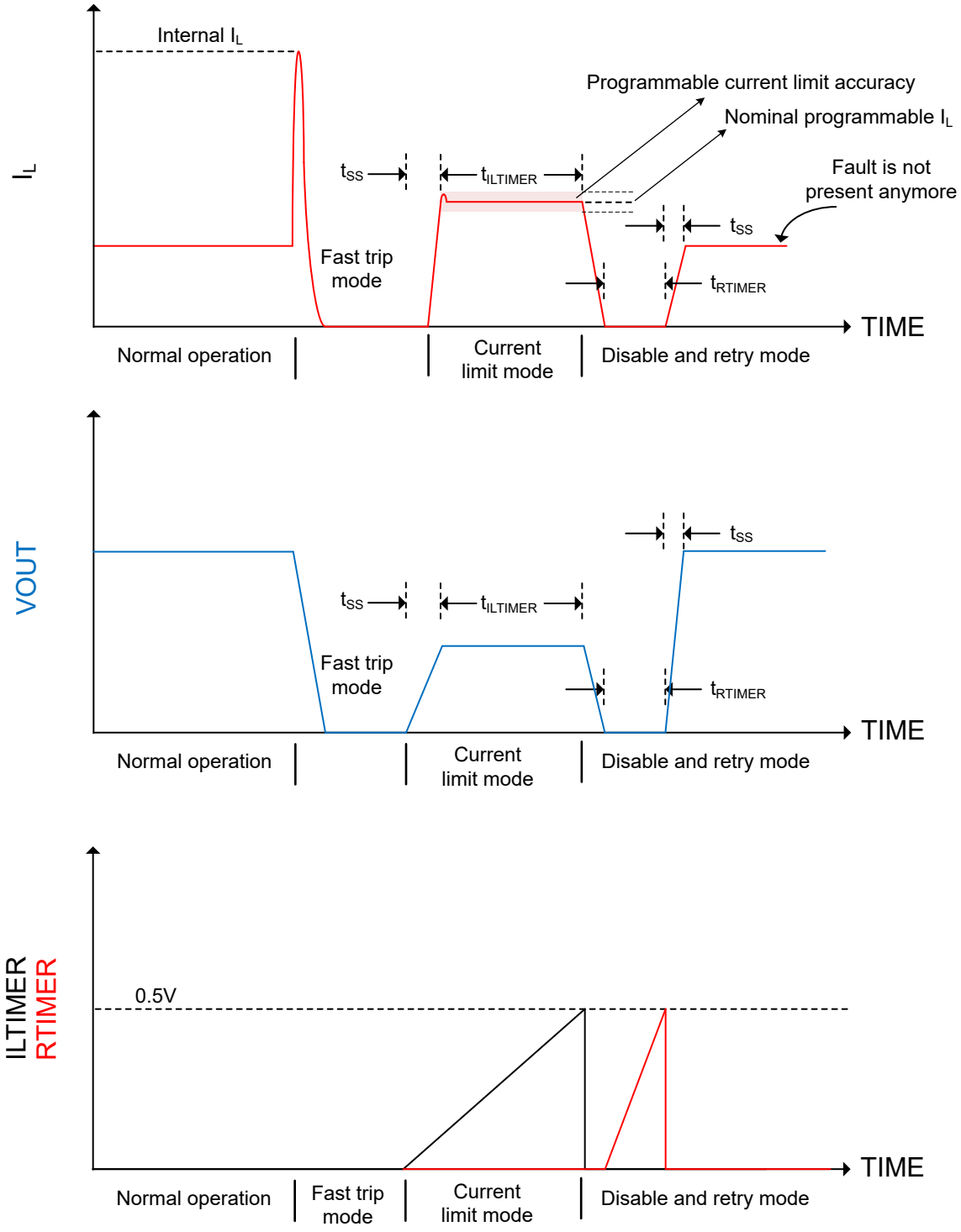

Figure 8-4. Hard Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

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The behavior of the ILTIMER and RTIMER pins for the internal timer conditions with the retry mode disabled is shown in Figure 8-5.

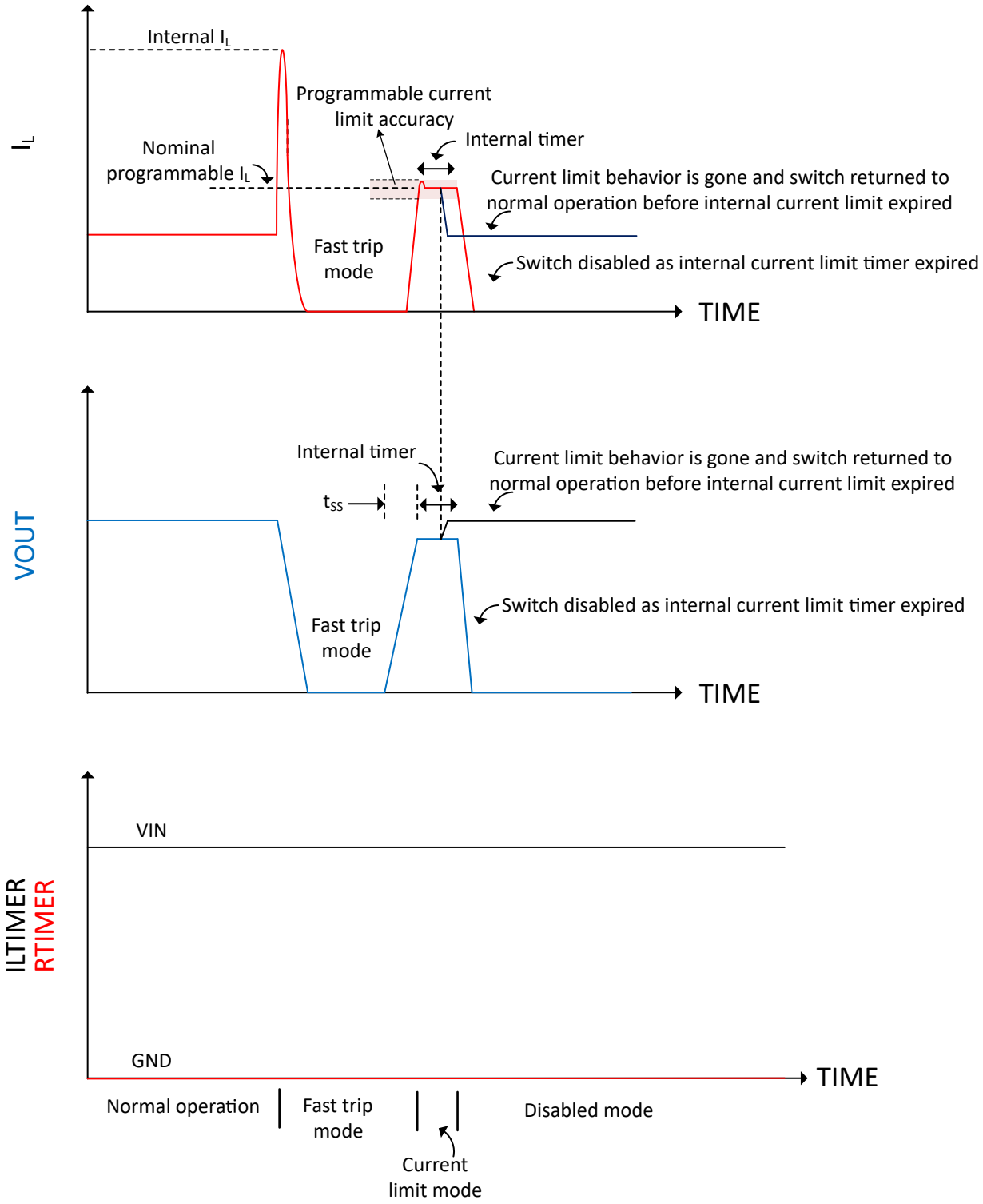

Figure 8-5. Programmable Fault Timer Operation Using the Internal Current Limit Timer and Disabling the Retry Mode

8.3.5 Current Sense

This pin outputs a current proportional to the output current of the switch for current sensing applications. A resistor to GND converts this current to voltage for current sensing purposes. The output current is the switch current divided by 41,500. The CS pin has a valid output 5ms after the device has been enabled. To operate the current sense in the linear region, the voltage at the CS pin at the application maximum load, must not exceed the CS pin voltage specification (VIN - 400mV).

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8.3.6 Parallel Operation

The TPS7H2201 can be configured in parallel operation either to increase the current capability, up to 12A, or to reduce the on-state resistance. In this case, all pins are shared as shown in Figure 8-6, except the current limit resistor (R_{IL}) for proper operation of the internal current limit loop. The current limiting resistors must be sized as described in the *Programmable Current Limiting* section.

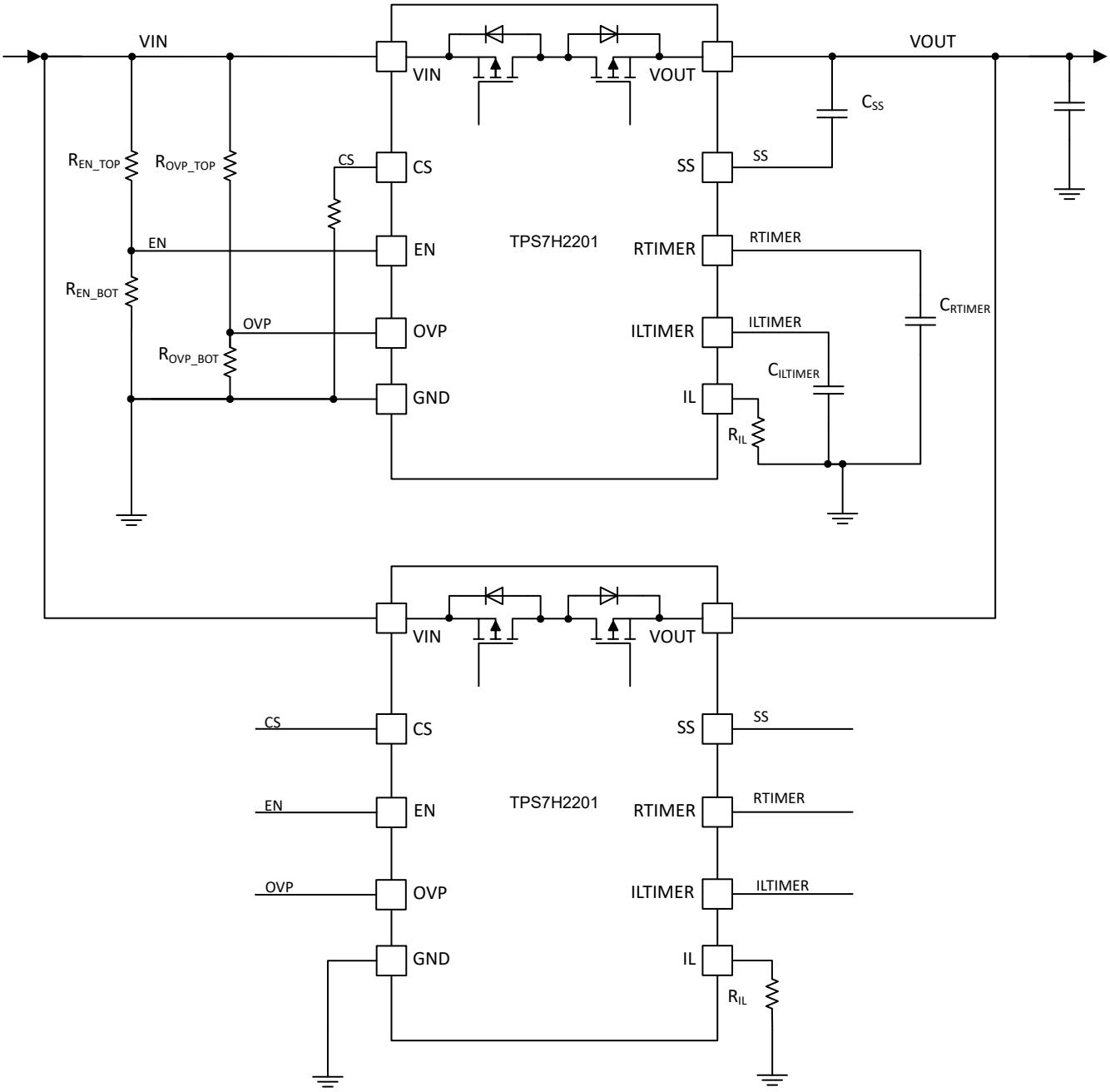

Figure 8-6. Parallel Configuration to Reduce Resistance or Increase Current Capability

8.3.7 Reverse Current Protection

The TPS7H2201 eFuse features back to back FETs to prevent current flow from VIN to VOUT and from VOUT to VIN when the switch is disabled (excluding leakage currents). This supports cold sparing (redundancy) applications. For example, VOUT can be up to 7V while VIN is between 0V and 7V. In all cases, only small leakage current is the result.

8.3.8 Forward Leakage Current

When VIN is powered but the TPS7H2201 is disabled (EN is low), the internal FETs are disabled, creating a high impedance path from VIN to VOUT. However, there are parasitic leakage paths that can cause VOUT to slowly charge. The forward leakage current, I_F, indicates how much current flows from VIN to VOUT during this situation. The maximum forward of the TPS7H2201SP current is specified at 250µA across voltage, temperature and radiation.

Some applications need to pay particular attention to this behavior. Is particularly relevant when VOUT is a high impedance node (and therefore the leakage current goes entirely to charging VOUT instead of being dissipated). By using the basic capacitor equation shown in Equation 11, the time for the voltage to rise to a given value can be theoretically calculated.

$$\Delta t = \Delta V_{OUT} \times C_{OUT} / I_F \quad (11)$$

where

- Δt = time to charge to final value
- ΔV_{OUT} = change in output voltage; for a 0V starting voltage, use V_{IN}

For example, with a 7V input voltage and a 220µF output capacitance, VOUT typically charge to 7V in approximately 6.2 seconds (using I_F = 150µA, ΔV_{OUT} = 7V, C_{OUT} = 220µF).

If the output voltage must remain below a certain value, a pull-down resistor can be utilized with a value as calculated by using Equation 12.

$$VOUT_{LKG_MAX} = I_F \times R_{PULL_DOWN} \quad (12)$$

where

- $VOUT_{LKG_MAX}$ = maximum output voltage due to leakage current, I_F
- R_{PULL_DOWN} = external pull-down resistor from VOUT to GND

For example, placing a 2.6kΩ resistor between VOUT and ground makes sure VOUT does not rise above 0.65V worse case due to the I_F current. The resistor need to be able to handle the worst case power dissipation when the switch is enabled and VOUT ≅ VIN.

8.4 Device Functional Modes

VOUT Connection due to V_{EN} and V_{OVP} lists the VOUT pin state as determined by the EN and OVP pin voltages.

Table 8-3. VOUT Connection due to V_{EN} and V_{OVP}

EN PIN	OVP PIN	TPS7H2201SP and TPS7H2201-SEP (5) (6)
0 (1)	0 (3)	Open
0	1 (4)	Open
1 (2)	0	VIN
1	1	Open

(1) $V_{EN} < V_{ILEN(MIN)} = 0$
(2) $V_{EN} > V_{IHEN(MAX)} = 1$
(3) $V_{OVP} < V_{OVPF(MIN)} = 0$
(4) $V_{OVP} > V_{OVPR(MAX)} = 1$
(5) Refer to Turn-On (t_{ON}), Turn-Off (t_{OFF}) and VOUT Fall Time (t_F) Waveforms for more details.
(6) Refer to OVP Assert (t_{ASSERT}) and OVP Deassert ($t_{DEASSERT}$) Waveforms for more details.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H2201 device is a single channel, 6A eFuse with multiple programmable features such as current limit, undervoltage and overvoltage, current limit and retry timers, and soft start. In addition, the TPS7H2201 features a reverse current protection capability for power distribution applications and current sensing for load monitoring purpose. The TPS7H2201SP user's guide is available on the TI website, *TPS7H2201EVM-CVAL Evaluation Module (EVM) User's Guide*. The guide highlights standard EVM configurations, test results, schematic, and BOM for reference.

9.2 Typical Applications

In addition to the standard power management applications where a power switch can be used, there are 2 main applications in which the TPS7H2201 can be used in space power applications:

- Redundancy for primary and secondary voltage rails common in satellite applications
- Protection for critical or SEL sensitive loads

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9.2.1 Redundancy

In applications where primary and secondary (redundant) power rails are present, the TPS7H2201 is designed to implement redundancy because of the reverse current blocking capability. In this case, since the eFuse is placed at the input of the point of load regulator, the on-resistance of the switch is not as critical.

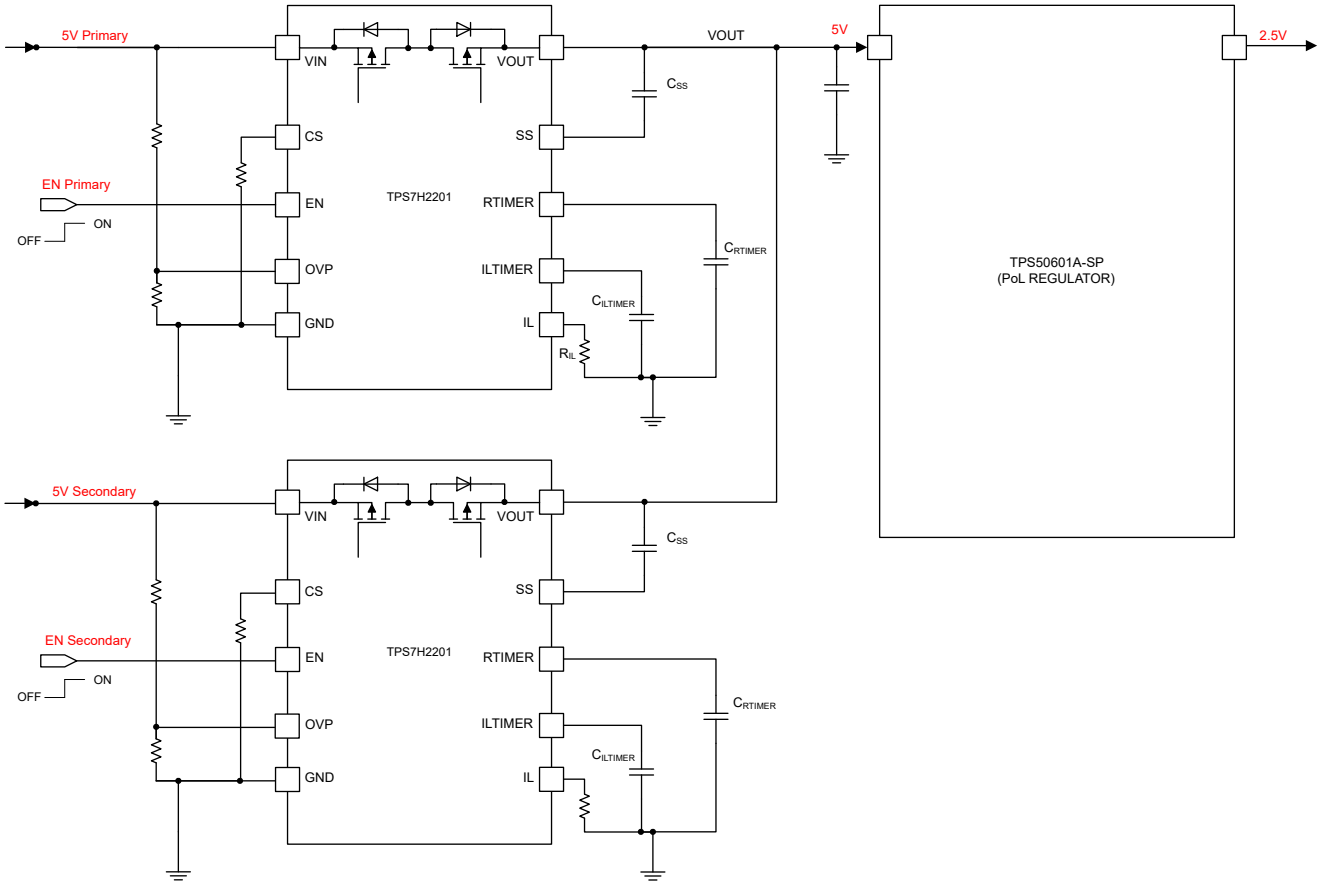

Figure 9-1. Redundancy Example Using the TPS7H2201

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9.2.2 Protection

The protection features of the TPS7H2201 can also be used for SEL sensitive loads. In such case, the on-resistance of the switch can be more relevant as the switch is placed after the point of load regulator but in such case, two eFuse can be placed in parallel to reduce the on-resistance if needed. The main advantages of using the eFuse at this location is faster response to SEL events and automatic recovery due to the retry mode of the programmable fault timer.

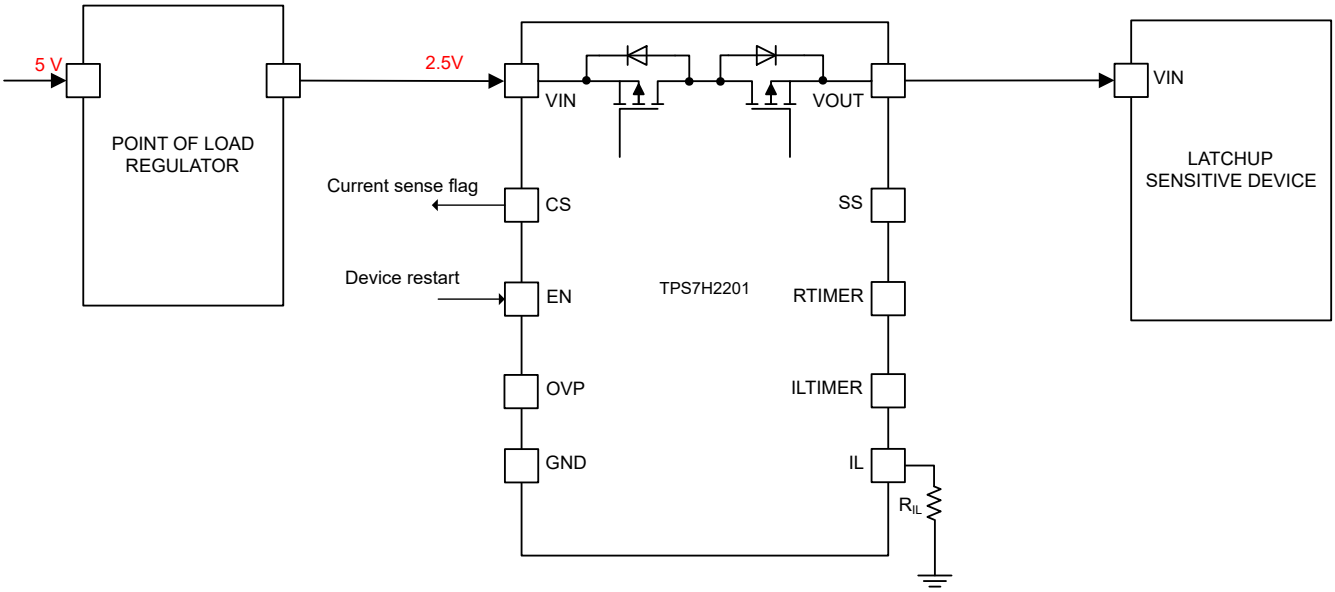

Figure 9-2. Protection Example Using the TPS7H2201

9.2.3 Design Requirements

Figure 9-3 shows a typical application schematic that is applicable to both the redundancy and the protection applications previously discussed.

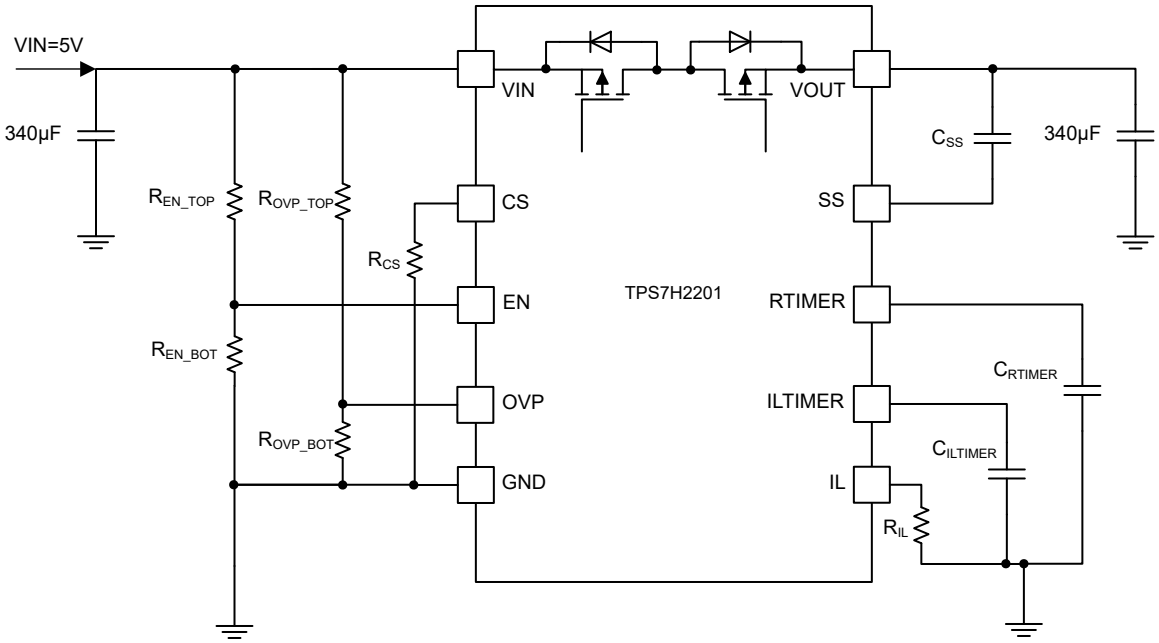

Figure 9-3. Typical Application Schematic

Table 9-1 shows the design parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VIN	5V
Undervoltage lockout set point	3.5V
Overvoltage protection set point	6.5V
Output current	6A
Current limit	7.5A
Current limit timer	1ms
Retry timer	1ms
Soft start time	9ms
Input and output capacitors	340µF

9.2.4 Detailed Design Procedure

9.2.4.1 Undervoltage Lockout

The undervoltage lockout set point is configured using the resistor divider, R_{EN_TOP} and R_{EN_BOT} connected to the EN pin. Set the R_{EN_TOP} = 100kΩ and, using Equation 1, calculate the value for R_{EN_BOT}. For an UVLO = 3.5V, R_{EN_BOT} = 15.5kΩ. When choosing the UVLO set point, the resistor divider must verify that the device is still enabled for the VIN used in the application. This is achieved by making sure that the V_{IHEN} requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is smaller than the VIN used in the application. Equation 13 shows this VIN and V_{IHEN} requirement to set the UVLO point. For this particular application, the requirement is met as the result is 4.84V.

$$V_{IHEN} \times \frac{R_{EN_TOP} + R_{EN_BOT}}{R_{EN_BOT}} \leq VIN \tag{13}$$

9.2.4.2 Overvoltage Protection

In a similar way to the UVLO set point, the overvoltage protection set point is configured using the resistor divider, R_{OVP_TOP} and R_{OVP_BOT} connected to the OVP pin. Set the R_{OVP_TOP} = 100kΩ and, using Equation 2, calculate the value for R_{OVP_BOT}. For an OVP = 6.5V, R_{OVP_BOT} = 10.7kΩ. When choosing the OVP set point, the resistor divider must verify that the device is still enabled for the VIN used in the application. This is achieved by making sure that the V_{OVPF} requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is larger than the VIN used in the application. Equation 14 shows this VIN and V_{OVPF} requirement to set the OVP point. For this particular application, the requirement is met as the result is 5.16V.

$$V_{OVPF} \times \frac{R_{OVP_TOP} + R_{OVP_BOT}}{R_{OVP_BOT}} \geq VIN \tag{14}$$

9.2.4.3 Current Limit

The current limit is configured using R_{IL}. Additionally, the minimum current limit setting specification in the *Electrical Characteristics* must be followed to verify there are no false current trips during device startup. Based on the output current for this design, the minimum current limit that can be programmed is IOUT + 1.5A for a total of 7.5A. As a result, using Equation 8, the resistor value is 6.53kΩ.

9.2.4.4 Programmable Fault Timers

The programmable fault timers are configured using the $C_{ILTIMER}$ and the C_{RTIMER} capacitors. For this particular design, both timers are set to 1ms. Therefore, using Equation 9, the value for each capacitor is 2000pF. These capacitor values meet the requirement in Equation 10.

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9.2.4.5 Soft Start Time

The soft start time is configured using the C_{SS} capacitor. To calculate the value of the capacitor, the VOUT slew rate needs to be calculated using Equation 3 to make sure the maximum VOUT slew rate requirement shown in Equation 4 is satisfied. This requirement is particularly important for space applications where large output capacitance is typically used, which translates to a lower maximum allowable VOUT slew rate. For this particular design, the VOUT slew rate is 555V/s which is less than the maximum VOUT slew rate of 882V/s, meeting the requirement from Equation 4. Now, the soft start capacitor value can be calculated as 117nF using Equation 6, since VIN = 5V for this application.

9.2.5 Application Curves

The power-up behavior of this design example is shown in Figure 9-4 and the current limit behavior is shown in Figure 9-5.

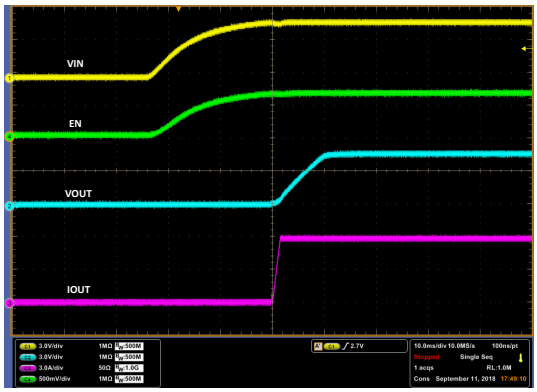

Figure 9-4. Power-up Behavior of the TPS7H2201SP

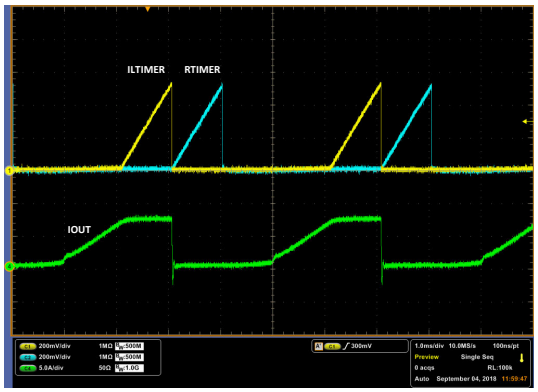

Figure 9-5. ILTIMER and RTIMER Waveforms When IL is Set to 7.5A

9.3 Power Supply Recommendations

The TPS7H2201 is designed to operate from an input voltage supply range between 1.5V to 7V. This supply voltage must be well regulated and proper local bypass capacitors must be used for proper electrical performance from VIN to GND. Due to stringent requirements for space applications, typically numerous input bypass capacitors are used and the total capacitance is much larger than for commercial applications. The TPS7H2201SP Evaluation Module uses one 330µF tantalum capacitor in parallel with one 10µF and one 0.1µF ceramic capacitor.

9.4 Layout

9.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects. In general, the components must be placed close to the device such that traces remain as short as possible to avoid parasitic capacitance. In addition, due to the possibility of large power dissipation in fault conditions (short at VOUT), thermal vias must be placed in the PCB for the thermal pad.

9.4.2 Layout Example

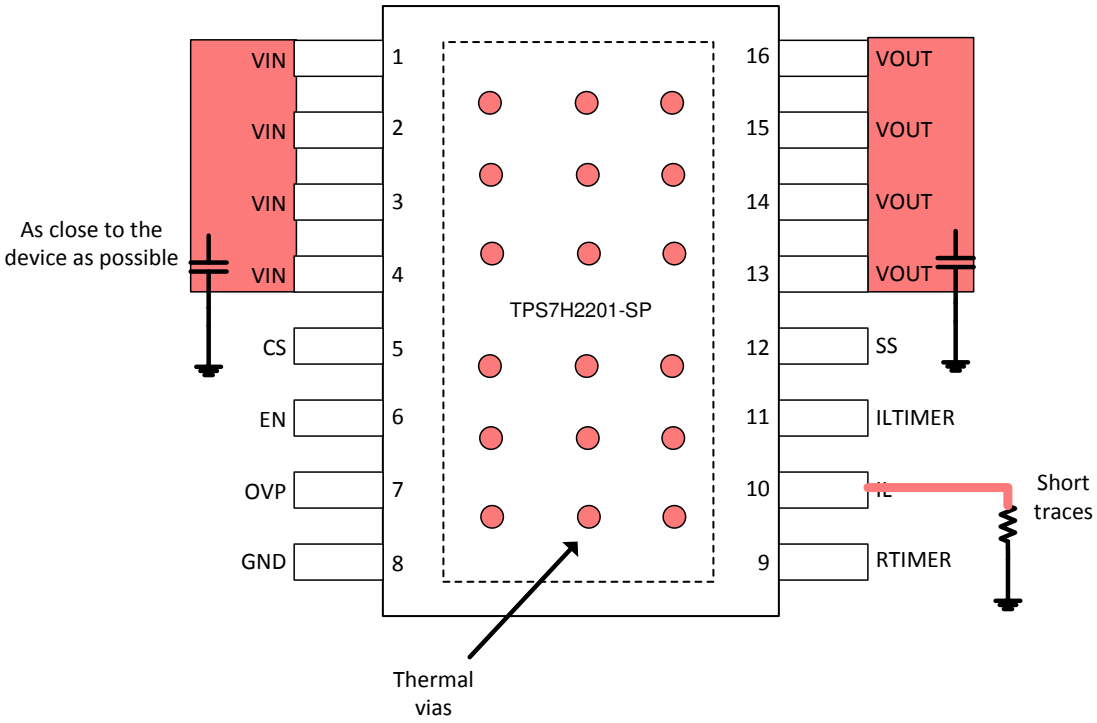

Figure 9-6. Layout Recommendation

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H2201-SP Total Ionizing Dose (TID) Report*
- Texas Instruments, *TPS7H2201-SEP TID Radiation Report*
- Texas Instruments, *Single-Events Effects Test Report of the TPS7H2201-SP eFuse*
- Texas Instruments, *Single-Event-Effects Test Report of the TPS7H2201-SEP eFuse*
- Texas Instruments, *TPS7H2201-SP Neutron Displacement Damage Characterization*
- Texas Instruments, *TPS7H2201EVM-CVAL Evaluation Module (EVM) User's Guide*
- Texas Instruments, *TPS7H2201EVM Evaluation Module (EVM)*
- Texas Instruments, *Unencrypted PSpice Transient Model*
- Texas Instruments, *Load Switch Thermal Considerations*
- Texas Instruments, *Basics of eFuses*
- Texas Instruments, *Basics of Load Switches*
- *Standard Microcircuit Drawing, 5962R17220*
- *Vendor Item Drawing, V6223608*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2024) to Revision G (December 2025)	Page
• Added 5962R1722002PYE information to Device Information table in *Description* section	1
• Change the IRCP limits to 20mA after TID=100krad(Si)	9
• Reorganized and reworded for clarification in *Programmable Fault Timer* section	22

Changes from Revision E (December 2023) to Revision F (March 2024)	Page
• Removed TPS7H2201MDAPTSEP advance-information notes in *Description* and *Device Options* sections	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-1722001VXC	Active	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962-1722001VXC TPS7H2201MHKRV
5962R1722001V9A	Active	Production	XCEPT (KGD) | 0	25 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R1722001VXC	Active	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962R1722001VXC TPS7H2201MHKRV
5962R1722001VXC.A	Active	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962R1722001VXC TPS7H2201MHKRV
5962R1722002PYE	Active	Production	HTSSOP (DAP) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1722002PYE
5962R1722002PYE.A	Active	Production	HTSSOP (DAP) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1722002PYE
TPS7H2201HKR/EM	Active	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	25 to 25	TPS7H2201HKREM
TPS7H2201MDAPTSEP	Active	Production	HTSSOP (DAP) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPS7H2201
TPS7H2201Y/EM	Active	Production	XCEPT (KGD) | 0	5 | OTHER	Yes	Call TI	N/A for Pkg Type	25 to 25	
V62/23608-01XE	Active	Production	HTSSOP (DAP) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPS7H2201

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS7H2201-SEP, TPS7H2201-SP :

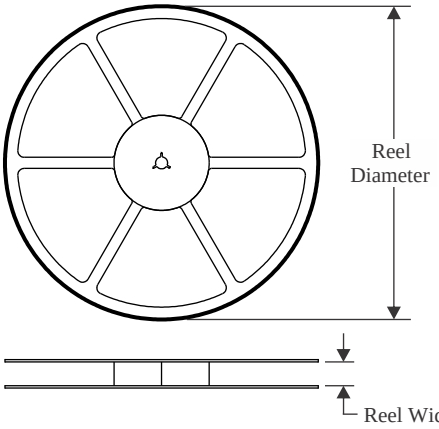
- Catalog : TPS7H2201-SEP
- Space : TPS7H2201-SP

NOTE: Qualified Version Definitions:

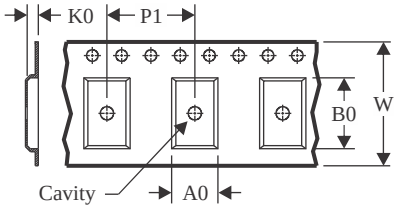
- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

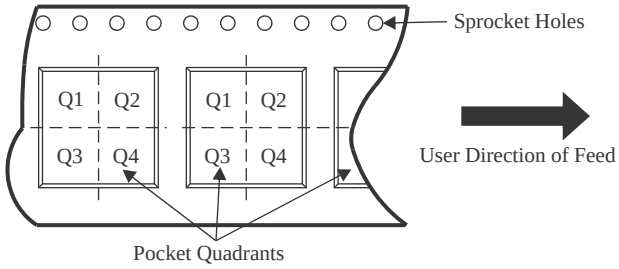


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

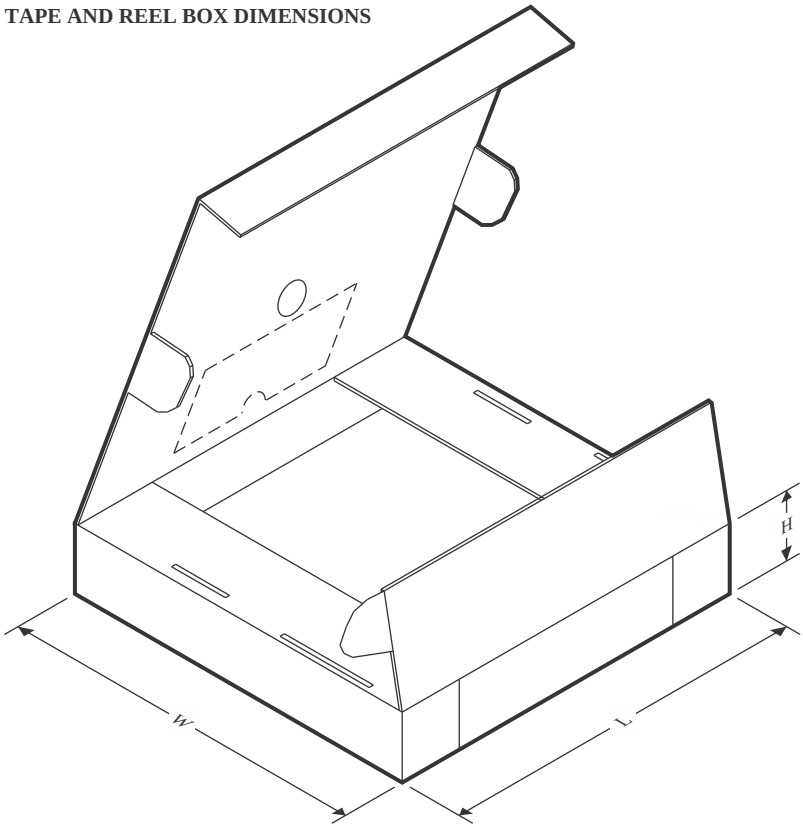
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962R1722002PYE	HTSSOP	DAP	32	250	178.0	24.4	8.8	11.8	1.8	12.0	24.0	Q1
TPS7H2201MDAPTSEP	HTSSOP	DAP	32	250	178.0	24.4	8.8	11.8	1.8	12.0	24.0	Q1

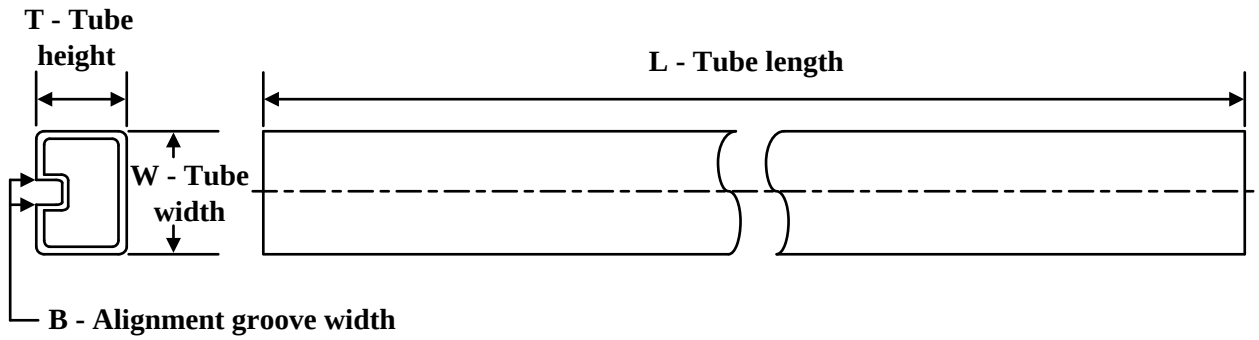
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962R1722002PYE	HTSSOP	DAP	32	250	223.0	191.0	55.0
TPS7H2201MDAPTSEP	HTSSOP	DAP	32	250	223.0	191.0	55.0

TUBE



*All dimensions are nominal

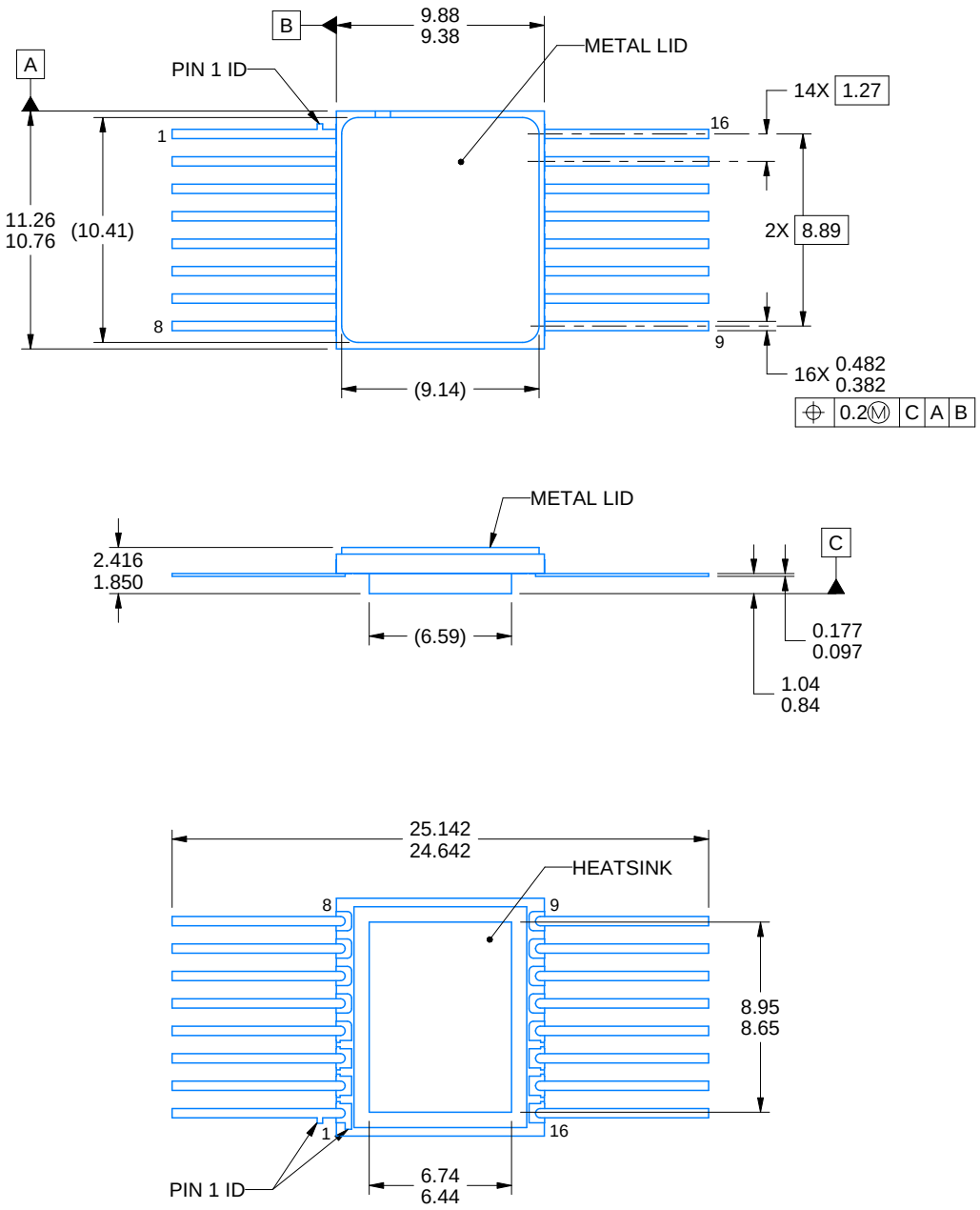
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1722001VXC	HKR	CFP	16	25	506.98	26.16	6220	NA
5962R1722001VXC	HKR	CFP	16	25	506.98	26.16	6220	NA
5962R1722001VXC.A	HKR	CFP	16	25	506.98	26.16	6220	NA
TPS7H2201HKR/EM	HKR	CFP	16	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKR0016A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



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NOTES:

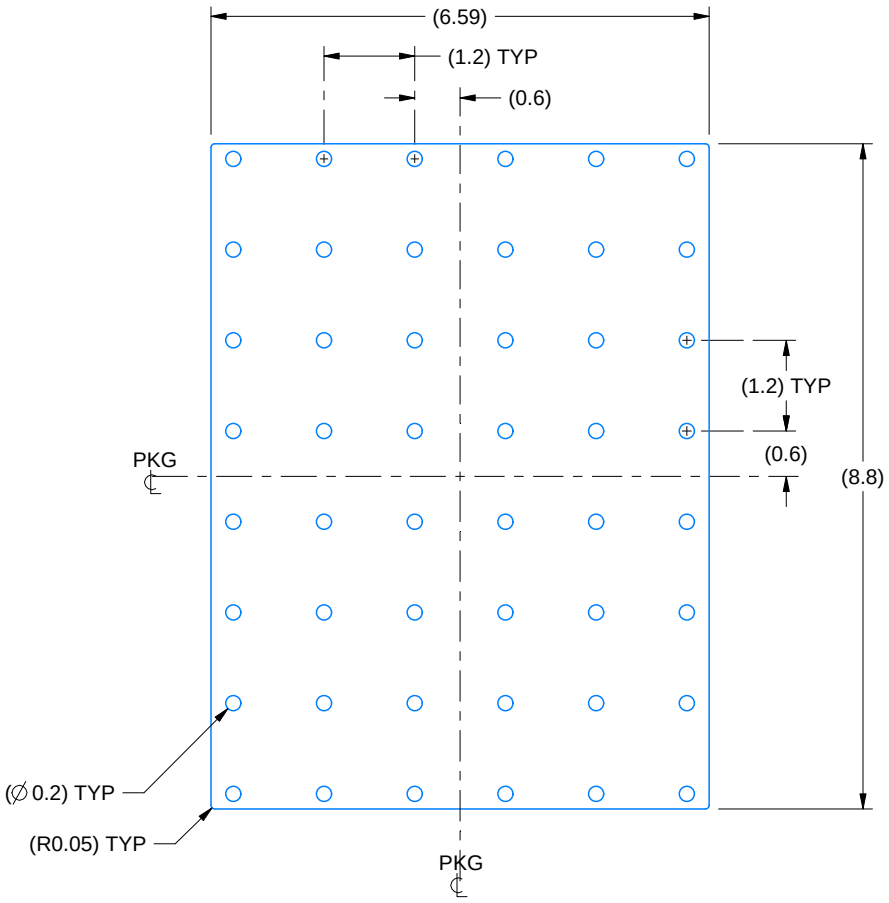
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

EXAMPLE BOARD LAYOUT

HKR0016A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

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GENERIC PACKAGE VIEW

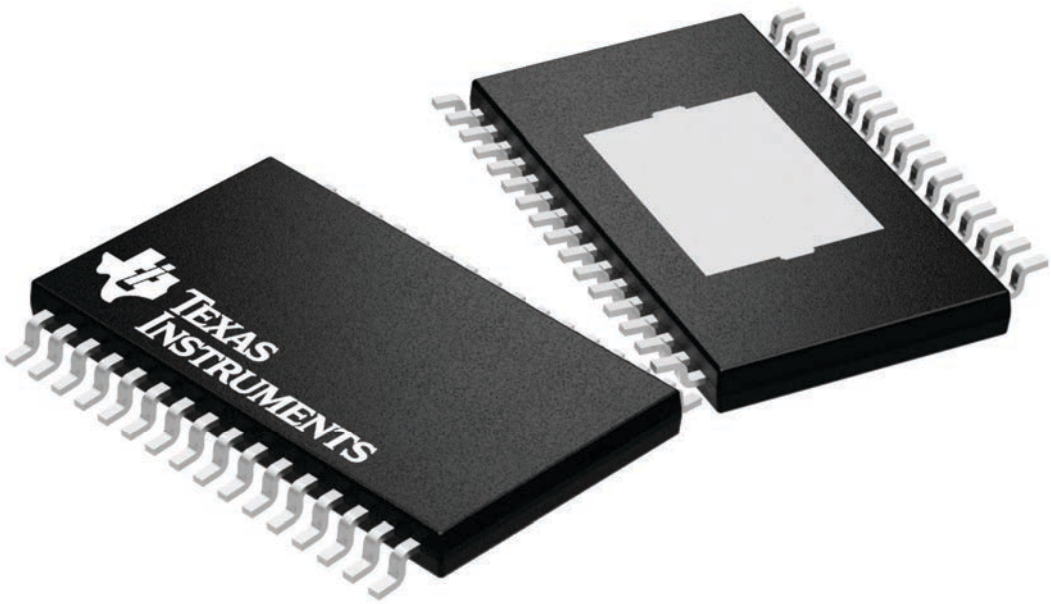
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

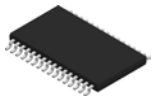
8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

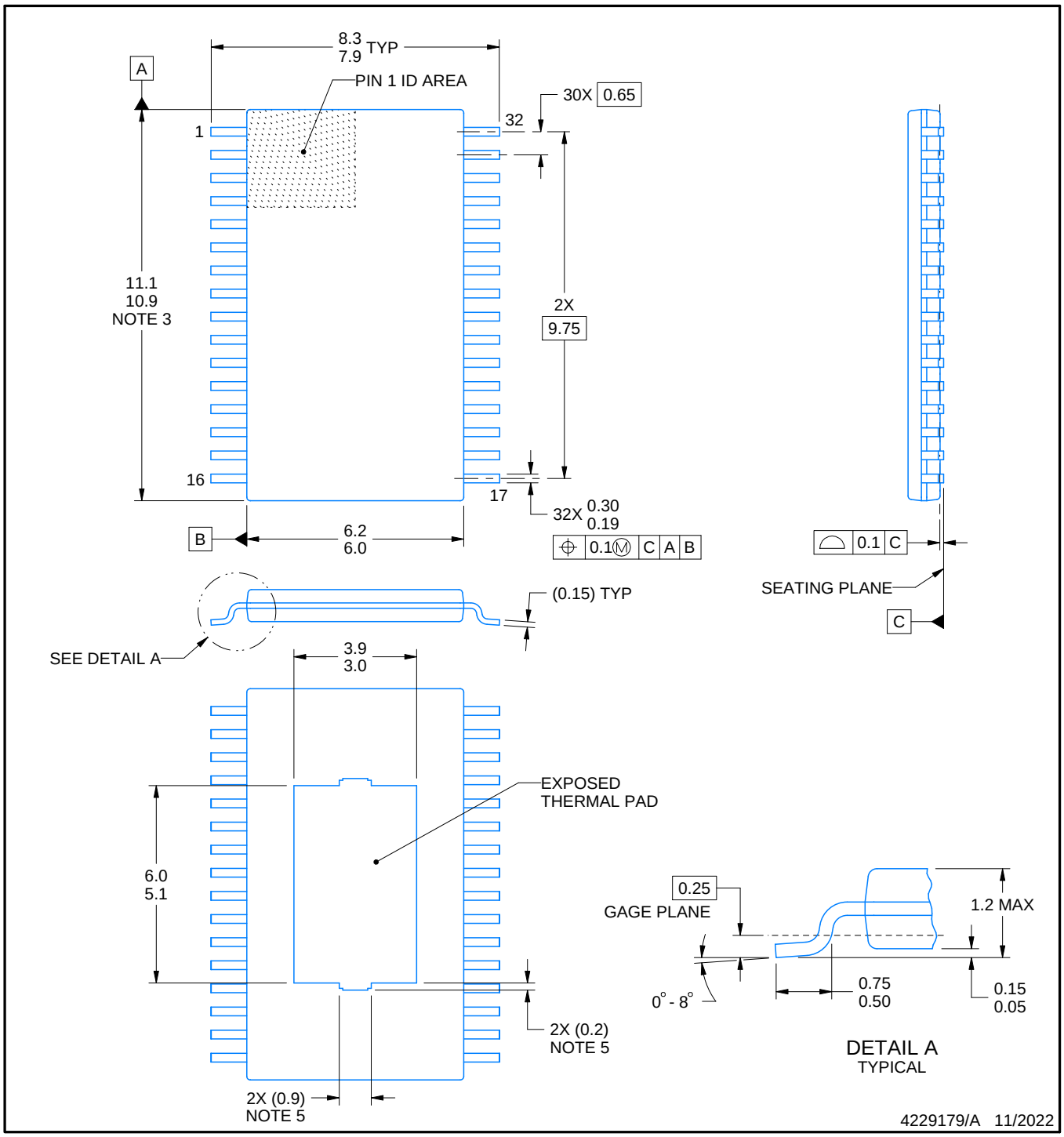


PACKAGE OUTLINE

DAP0032G

PowerPAD™ TSSOP - 1.2 mm max height

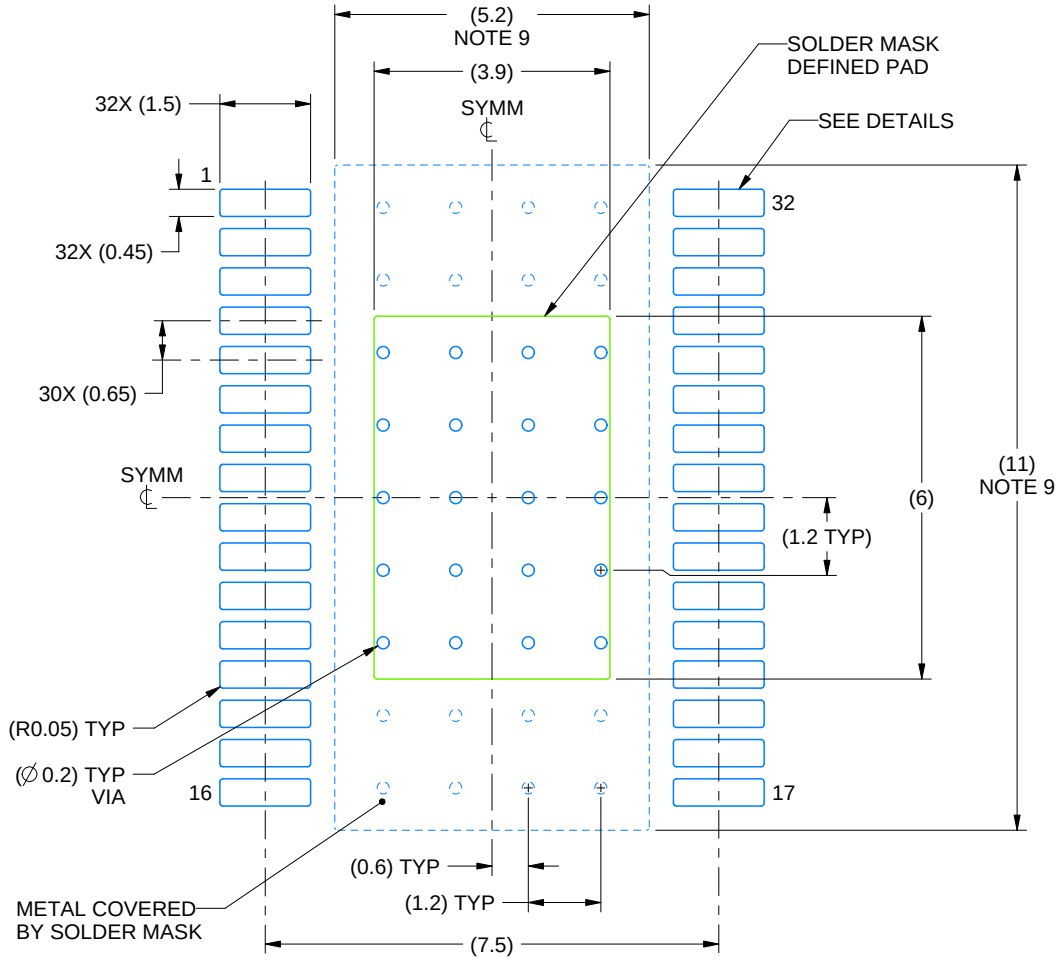
PLASTIC SMALL OUTLINE



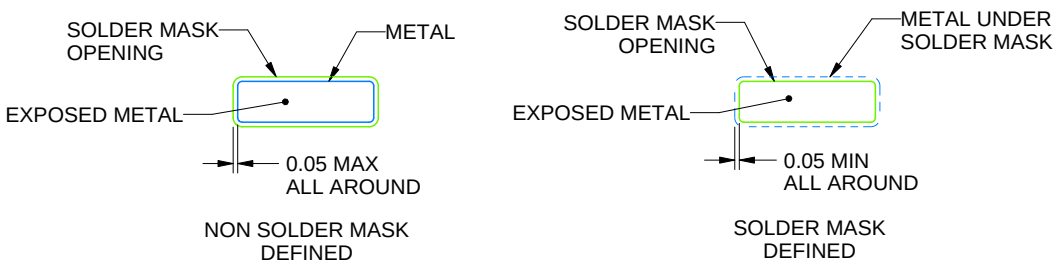
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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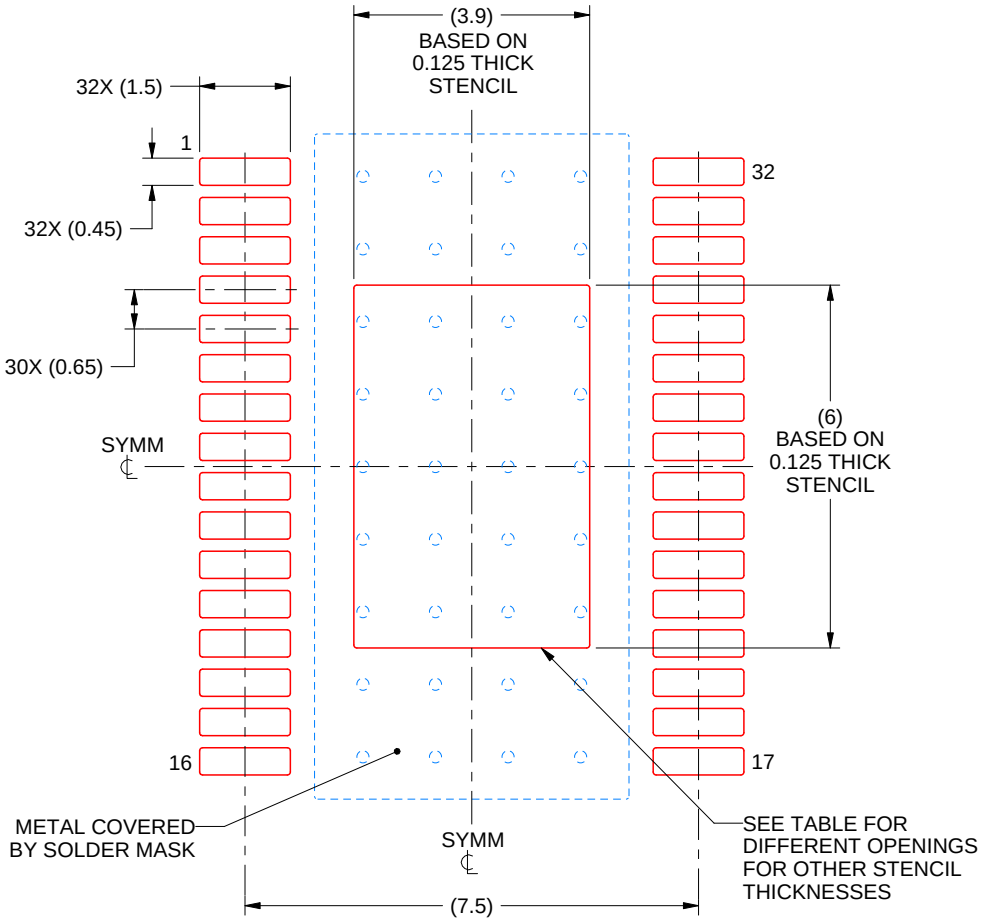
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.36 X 6.71
0.125	3.90 X 6.00 (SHOWN)
0.15	3.56 X 5.48
0.175	3.30 X 5.07

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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