# TPS61378-Q1 Automotive, 25µA Quiescent Current Synchronous Boost Converter With Load Disconnect

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- TPS61378-Q1 wettable flank
- TPS61378L-Q1 immersion Sn
  - Provides shorter production cycle time and longer shelf life
- Function Safety-Capable
  - Documentation available to aid functional safety system design
- Flexible input and output operation range
  - Input voltage range: 2.3V to 14V
  - Programmable output voltage : 4.0V to 18.5V
  - Fixed output options: 5V, 5.25V, and 5.5V
  - Programmable peak current limit: 1A to 4.8A
- Avoid AM band interference and crosstalk
  - Dynamically programmable switching frequency: 200kHz to 2.2MHz
  - Spread spectrum frequency modulation at FPWM mode
  - Optional clock synchronization
- Minimize design size for space constraint applications
  - Integrated LS/HS/ISO FET: $R_{DS(ON)}$ 50mΩ/50mΩ/100mΩ
  - Support up to 2.2MHz with small L-C
- Minimized light load and idle state current consumption
  - 25µA quiescent current into VIN pin
  - 0.5µA shutdown current into VIN pin
  - Selectable auto PFM and forced PWM mode
  - True load disconnect during shutdown or fault conditions
- Integrated protection features
  - Supports VIN close to VOUT operation
  - Input undervoltage lockout and output overvoltage protection
  - Hiccup output short-circuit protection
  - Power-good indicator
  - Thermal shutdown protection at 165°C
- Higher than 90% efficiency under 0.8A load from 3.3V to 9V conversion

## 2 Applications

- Advanced driver assistance system (ADAS)
- Automotive infotainment and cluster
- Body electronics and lighting
- Emergency call (eCall)

## 3 Description

The TPS61378-Q1 is a fully-integrated synchronous boost converter with an integrated load disconnect function. The input voltage covers 2.3V to 14V while the maximal output voltage covers up to 18.5V. The switching current limit is programmable from 1A to 4.8A. The device consumes 25µA quiescent current from $V_{IN}$.

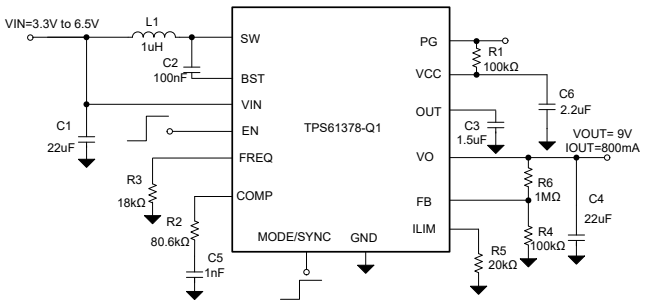
The TPS61378-Q1 employs peak current mode control with the switching frequency programmable from 200kHz to 2.2MHz. The device works in fixed frequency PWM operation in medium to heavy loads. There are two optional modes in light load by configuring the MODE pin: auto PFM mode and forced PWM to balance the efficiency and noise immunity in light load. The switching frequency can be synchronized to an external clock. The TPS61378-Q1 uses the spread spectrum of the internal clock to be more EMI friendly at FPWM mode. In addition, there is an internal soft-start time to limit the inrush current.

The TPS61378-Q1 has various fixed output voltage versions to save the external feedback resistor. The device supports the external loop compensation so that the stability and transient response can be optimized at wider $V_{OUT}/V_{IN}$ ranges. The device also integrates robust protection features including output short protection, output overvoltage protection, and thermal shutdown protection. The TPS61378-Q1 is available in a 3mm × 3mm 16-pin QFN package with wettable flank.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS61378-Q1 | RTE (WQFN, 16) | 3mm × 3mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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## 4 Device Comparison Table

| PART NUMBER | OUTPUT VOLTAGE (V) | OUTPUT VOLTAGE SELECTION RESISTOR ($R_{FB}$)(2) | SPREAD SPECTRUM |
|---|---|---|---|
| TPS61378-Q1 | 5 | 0Ω≤ $R_{FB}$ ≤ 2.4kΩ | Enable |
| | 5.25 | 3.6kΩ ≤ $R_{FB}$≤ 4.8kΩ | |
| | 5.5 | 7.2kΩ ≤ $R_{FB}$ ≤ 9.6kΩ | |
| | Adjustable | $R_{FB}$ ≥ 14.4kΩ | |
| TPS613781-Q1(1) | 5.7 | 0Ω≤ $R_{FB}$ ≤ 2.4kΩ | Enable |
| | 6.2 | 3.6kΩ ≤ $R_{FB}$ ≤ 4.8kΩ | |
| | 7 | 7.2kΩ ≤ $R_{FB}$ ≤ 9.6kΩ | |
| | 8 | $R_{FB}$ ≥ 14.4kΩ | |
| TPS613782-Q1(1) | 9 | 0Ω≤ $R_{FB}$ ≤ 2.4kΩ | Enable |
| | 10 | 3.6kΩ ≤ $R_{FB}$ ≤ 4.8kΩ | |
| | 11 | 7.2kΩ ≤ $R_{FB}$ ≤ 9.6kΩ | |
| | 12 | $R_{FB}$ ≥ 14.4kΩ | |
| TPS613783-Q1 | 5 | 0Ω≤ $R_{FB}$ ≤ 2.4kΩ | Disable |
| | 5.25 | 3.6kΩ ≤ $R_{FB}$ ≤ 4.8kΩ | |
| | 5.5 | 7.2kΩ ≤ $R_{FB}$ ≤ 9.6kΩ | |
| | Adjustable | $R_{FB}$ ≥ 14.4kΩ | |
| TPS613784-Q1(1) | 5.7 | 0Ω≤ $R_{FB}$ ≤ 2.4kΩ | Disable |
| | 6.2 | 3.6kΩ ≤ $R_{FB}$ ≤ 4.8kΩ | |
| | 7 | 7.2kΩ ≤ $R_{FB}$ ≤ 9.6kΩ | |
| | 8 | $R_{FB}$ ≥ 14.4kΩ | |
| TPS613785-Q1 | 9 | 0Ω≤ $R_{FB}$ ≤ 2.4kΩ | Disable |
| | 10 | 3.6kΩ ≤ $R_{FB}$ ≤ 4.8kΩ | |
| | 11 | 7.2kΩ ≤ $R_{FB}$ ≤ 9.6kΩ | |
| | 12 | $R_{FB}$ ≥ 14.4kΩ | |

(1) Product Preview (not Production Data). Contact TI factory for more information.
(2) $R_{FB}$ is the sensed resistor from FB pin. See also Section 8.2.2.1 for details. Avoid using resistors other than the recommended values, otherwise the output voltage value cannot be specified.

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# 5 Pin Configuration and Functions

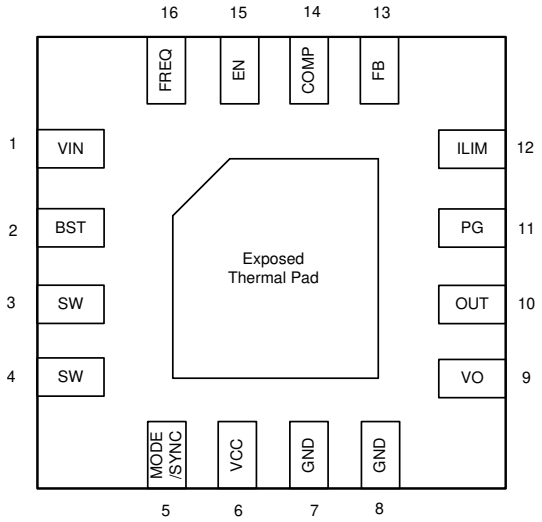



**Figure 5-1. 16-Pin WQFN RTE Package (Transparent Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VIN | 1 | I | IC power supply input |
| BST | 2 | I | Power supply for high-side N-MOSFET gate drivers. A capacitor must be connected between this pin and the SW pin. |
| SW | 3, 4 | PWR | The switching node pin of the converter. This pin is connected to the drain of the internal low-side FET and the source of the high-side FET. |
| MODE/SYNC | 5 | I | Mode selection pin.<br>MODE = high, forced PWM mode<br>MODE = low or floating, auto PFM mode<br>This pin can also be used to synchronize the external clock. Refer to Table 7-2 for details. |
| VCC | 6 | O | Output of internal regulator. A ceramic capacitor with more than 1µF must be connected between this pin and GND. |
| GND | 7, 8 | PWR | Power ground of the IC. this pin is connected to the source of the low-side FET. |
| VO | 9 | PWR | Output of the isolation FET. Connect load to this pin to achieve input/output isolation. |
| OUT | 10 | PWR | Output of the drain of the HS FET. Connect this pin because the output can disable the load disconnect/short protection feature (or short this pin with the VO pin). |
| PG | 11 | O | Power good indicator and open drain output |
| ILIM | 12 | I | Current limit setting pin. Use a resistor to set the desired peak current limit. See also Section 7.3.7. |
| FB | 13 | I | Feedback pin. Use a resistor divider to set the desired output voltage. See also Section 8.2.2.1. |
| COMP | 14 | I | Output of the internal transconductance error amplifier. An external RC network is connected to this pin to optimize the loop stability and response time. |
| EN | 15 | I | Enable logic input |
| FREQ | 16 | I | Frequency setting pin. Connect a resistor between this pin and GND pin to set the desired frequency. |
| Thermal Pad | — | — | The thermal pad must be connected to the power ground plane for good power dissipation. |

(1) I = input, O = output, PWR = power


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range at terminals (2) | VIN | –0.3 | 16 | V |
| Voltage range at terminals (2) | VO, SW, OUT | –0.3 | 23 | V |
| Voltage range at terminals (2) | SW spike at 150ns | –0.7 | | V |
| | SW spike at 10ns | –2 | 25 | V |
| | SW spike at 1ns | –4 | 26 | V |
| | BST | –0.3 | SW + 6 | V |
| | MODE/SYNC, FB, FREQ, ILIM, VCC, COMP, EN | –0.3 | 6 | V |
| | PG | –0.3 | 20 | V |
| $T_J$(3) | Operating junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetime. Operating lifetime is derated for junction temperatures greater than 125°C

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$(1) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(2) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011, all pins | ±500 | |
| $V_{(ESD)}$(1) | Electrostatic discharge | Charged-device model (CDM), per AEC Q100-011, corner pins (1,4,5,8,9,12,13,16) | ±750 | V |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.3 | | 14 | V |
| $V_{OUT}$ | Outputvoltage | 4 | | 18.5 | V |
| $T_J$ | Operating junction temperature(1) | –40 | | 150 | °C |

(1) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS61378-Q1 RTE 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 46.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 43.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 18.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 18.5 | °C/W |

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## 6.4 Thermal Information (continued)

| THERMAL METRIC(1) | | TPS61378-Q1 RTE 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 8.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 6.5 Electrical Characteristics

$T_J$ = –40 to 125°C, L = 1 µH, $V_{IN}$ = 3.3 V and $V_{OUT}$ = 9 V (VO pin). Typical values are at $T_J$ = 25°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | | 2.3 | | 14 | V |
| $V_{IN_UVLO}$ | VIN under voltage lockout threshold | $V_{IN}$ rising | | 2.2 | 2.3 | V |
| | | $V_{IN}$ falling | | 2.04 | 2.2 | V |
| $V_{IN_HYS}$ | VIN UVLO hysteresis | | | 160 | | mV |
| $V_{CC_UVLO}$ | VCC UVLO threshold | $V_{CC}$ rising | | 2.2 | | V |
| $V_{CC_HYS}$ | VCC UVLO hysteresis | $V_{CC}$ hysteresis | | 150 | | mV |
| $V_{CC}$ | VCC regulation | $I_{VCC}$ = 6mA, $V_{OUT}$ = 9V | | 4.8 | | V |
| $I_Q$ | Quiescent current into $V_{IN}$ pin | IC enabled, no load, $V_{IN}$ = 3.3V, $V_{OUT}$ = 18.5V, $V_{FB}$ = $V_{REF}$ + 0.1V, | | 25 | 35 | µA |
| $I_Q$ | Quiescent current into OUT pin | IC enabled, no load, $V_{IN}$ = 3.3V, $V_{OUT}$ = 18.5V, $V_{FB}$ = $V_{REF}$ + 0.1V, | | 10 | 20 | µA |
| $I_{SD}$ | Shutdown current into VIN pin | IC disabled, $V_{IN}$ =14V, EN = GND | | 0.6 | 5 | µA |
| $I_{SW_LKG}$ | Leakage current into SW | IC disabled, $V_{IN}$ = OUT = SW =14V | | | 5 | µA |
| $I_{VO_LKG}$ | Reverse leakage current into VO | IC disabled, OUT= VO = 5V, SW = 0V | | | 5 | µA |
| **OUTPUT VOLTAGE** | | | | | | |
| $V_{OVP}$ | Output over-voltage protection threshold | $V_{IN}$ = 3.3V, $V_{OUT}$ rising | 19.3 | 20 | 20.5 | V |
| $V_{OVP_HYS}$ | Output over-voltage protection hysteresis | $V_{IN}$ = 3.3V, OVP threshold | | 0.5 | | V |
| **VOLTAGE REFERENCE** | | | | | | |
| $V_{REF}$ | Reference Voltage at FB pin | $T_J$ = –40 to 125°C, $R_{FB}$ = 16.0kΩ | 0.788 | 0.800 | 0.812 | V |
| $V_{OUT_5V}$ | | $T_J$ = –40 to 125°C, $R_{FB}$ = 2.0kΩ | 4.85 | 5.00 | 5.15 | V |
| $V_{OUT_5.25V}$ | | $T_J$ = –40 to 125°C, $R_{FB}$ = 4.0kΩ | 5.10 | 5.25 | 5.35 | V |
| $V_{OUT_5.5V}$ | | $T_J$ = –40 to 125°C, $R_{FB}$ = 8.0kΩ | 5.35 | 5.50 | 5.65 | V |
| $V_{OUT_5V}$ | | TPS613783Q1, $T_J$ = –40 to 125°C, $R_{FB}$ = 2.0kΩ | 4.85 | 5.00 | 5.15 | V |
| $V_{OUT_5.25V}$ | | TPS613783Q1, $T_J$ = –40 to 125°C, $R_{FB}$ = 4.0kΩ | 5.10 | 5.25 | 5.35 | V |
| $V_{OUT_5.5V}$ | | TPS613783Q1, $T_J$ = –40 to 125°C, $R_{FB}$ = 8.0kΩ | 5.35 | 5.50 | 5.65 | V |
| $V_{OUT_9V}$ | | TPS613785Q1, $T_J$ = –40 to 125°C, $R_{FB}$ = 2.0kΩ | 8.75 | 9.00 | 9.15 | V |
| $V_{OUT_10V}$ | | TPS613785Q1, $T_J$ = –40 to 125°C, $R_{FB}$ = 4.0kΩ | 9.75 | 10.00 | 10.20 | V |
| $V_{OUT_11V}$ | | TPS613785Q1, $T_J$ = –40 to 125°C, $R_{FB}$ = 8.0kΩ | 10.70 | 11.00 | 11.20 | V |
| $V_{OUT_12V}$ | | TPS613785Q1, $T_J$ = –40 to 125°C, $R_{FB}$ = 16.0kΩ | 11.70 | 12.00 | 12.22 | V |
| $I_{FB_LKG}$ | Leakage current into FB pin | | | | 50 | nA |
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | Low-side MOSFET on resistance | $V_{CC}$ = 4.85V | | 50 | | mΩ |
| $R_{DS(on)}$ | High-side MOSFET on resistance | $V_{CC}$ = 4.85V | | 50 | | mΩ |


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## 6.5 Electrical Characteristics (continued)

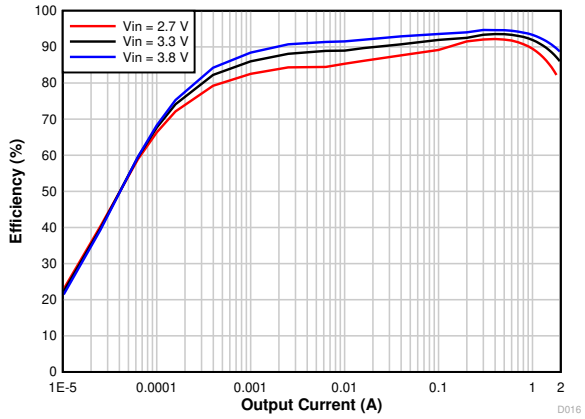
$T_J$ = –40 to 125°C, L = 1 µH, $V_{IN}$ = 3.3 V and $V_{OUT}$ = 9 V (VO pin). Typical values are at $T_J$ = 25°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DS(on)}$ | Isolation MOSFET on resistance | $V_{CC}$ = 4.85V | | 100 | | mΩ |
| **CURRENT LIMIT** | | | | | | |
| $I_{LIM_SW}$ | Peak switching current limit FPWM | $R_{LIM}$ = 20kΩ , Duty cycle = 65% | 4 | 4.8 | 5.55 | A |
| $I_{LIM_SW}$ | Peak switching current limit Auto PFM | $R_{LIM}$ = 20kΩ , Duty cycle = 65% | 4 | 4.8 | 5.55 | A |
| $I_{LIM_SW}$ | Peak switching current limit FPWM | $R_{LIM}$ = 102kΩ, Duty cycle = 65%, 4.7uH | | 0.75 | | A |
| $I_{LIM_SW}$ | Peak switching current limit Auto PFM | $R_{LIM}$ = 102kΩ, Duty cycle = 65%, 4.7uH | | 0.75 | | A |
| $I_{LIM_SS_1}$ | Peak switching current limit at softstart | $V_{IN}$ = 3.3V, $V_{OUT}$ = 0V, $R_{LIM}$ = 20kΩ | 0.9 | 1.15 | 1.4 | A |
| **SWITCHING FREQUENCY** | | | | | | |
| Fsw | Switching frequency | $R_{FREQ}$ = 18kΩ | 2050 | 2200 | 2400 | kHz |
| Fsw | Switching frequency | $R_{FREQ}$ = 218kΩ | 180 | 200 | 230 | kHz |
| $D_{max}$ | Maximum Duty Cycle | $R_{FREQ}$ = 18kΩ | 78 | | | % |
| $t_{ON_min}$ | Minimal on time | | | 70 | | ns |
| $F_{DITHER}$ | | | | 10% | | Fsw |
| $F_{pattern}$ | | | | 0.4% | | Fsw |
| **ERROR AMPLIFIER** | | | | | | |
| $I_{SINK}$ | COMP pin sink current | $V_{FB}$ = $V_{REF}$ + 0.2V | | 6 | | µA |
| $I_{SOURCE}$ | COMP pin source current | $V_{FB}$ = $V_{REF}$ - 0.2V | | 6 | | µA |
| $V_{CCLPH}$ | COMP pin high clamp voltage | $V_{FB}$ = $V_{REF}$ - 0.2V, ILIM = 4.8A | | 1.3 | | V |
| $V_{CCLPL}$ | COMP pin high low voltage | $V_{FB}$ = $V_{REF}$ + 0.2V, | | 0.6 | | V |
| $G_{mEA}$ | Error amplifier trans conductance | $V_{COMP}$ = 1.0V | | 70 | | µS |
| **POWER GOOD** | | | | | | |
| $V_{PG_TH}$ | PG threhold for rising FB voltage | Reference to $V_{REF}$ | | 90% | | |
| $V_{PG_HYS}$ | PG hysteresis | Reference to $V_{REF}$ | | 5% | | |
| $I_{PG_SINK}$ | PG pin sink current capability | $V_{PG}$ = 0.4V | | 20 | | mA |
| $t_{PG_DELAY}$ | PG delay time | | 2.5 | 3.4 | 4.3 | ms |
| **DOWN MODE** | | | | | | |
| $t_{EN_DELAY}$ | Delay time between EN high and device working | | | 0.4 | | ms |
| $t_{SS}$ | Softstart time | | | 2.5 | | ms |
| $t_{HCP_ON}$ | Hiccup on time | | | 1.8 | | ms |
| $t_{HCP_OFF}$ | Hiccup off time | | | 67 | | ms |
| **SYNC TIMING** | | | | | | |
| $f_{SYNC_MIN}$ | | | | 200 | | kHz |
| $f_{SYNC_MAX}$ | | | | 2200 | | kHz |
| **EN/SYNC LOGIC** | | | | | | |
| $VI_H$ | EN, MODE/SYNC pins Logic high threshold | | | | 1.2 | V |
| $VI_L$ | EN, MODE/SYNC pins Logic Low threshold | | 0.4 | | | V |
| $R_{DOWN}$ | EN, MODE/SYNC pins internal pull down resistor | | | 800 | | kΩ |
| **THERMAL SHUTDOWN** | | | | | | |
| $t_{SD_R}$ | Thermal shutdown rising threshold | TJ rising | | 165 | | °C |
| $t_{SD_F}$ | Thermal shutdown falling threshold | TJ falling | | 145 | | °C |

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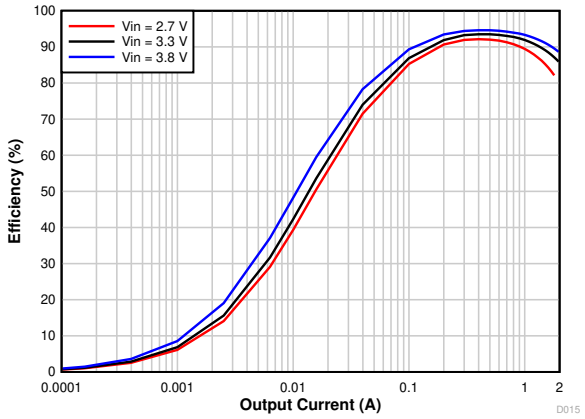
## 6.6 Typical Characteristics

$V_{IN}$ = 3.3V, $V_{OUT}$ = 9V (VO pin), $T_A$ = 25°C, Fsw = 2.2MHz, unless otherwise noted.



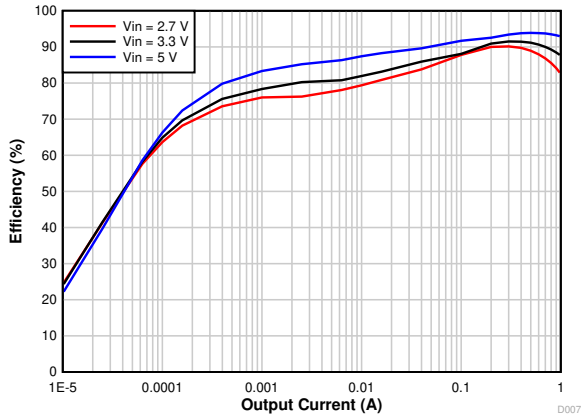

VOUT = 5V Auto PFM Fsw = 2.2MHz

**Figure 6-1. 5 $V_{OUT}$ Efficiency vs Output Current**



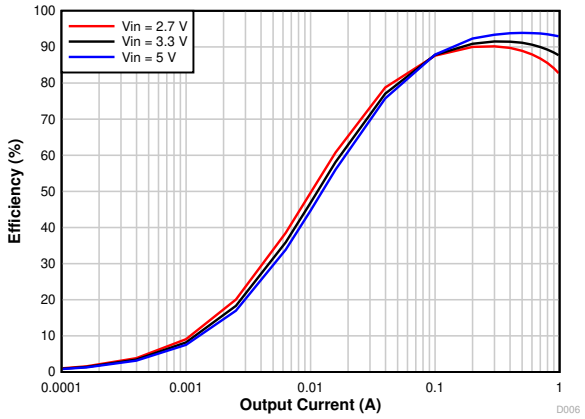

VOUT = 5V FPWM Fsw = 2.2MHz

**Figure 6-2. 5 $V_{OUT}$ Efficiency vs Output Current**



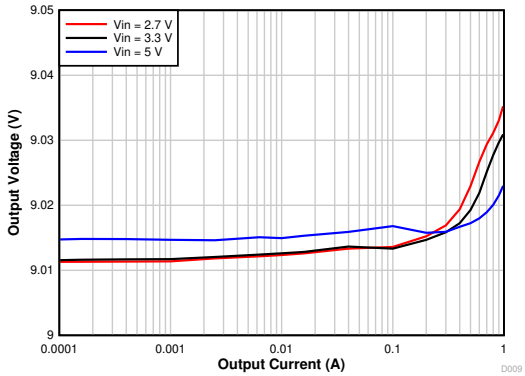

VOUT = 9V Auto PFM Fsw = 2.2MHz

**Figure 6-3. 9 $V_{OUT}$ Efficiency vs Output Current**




VOUT = 9V FPWM Fsw = 2.2MHz

**Figure 6-4. 9 $V_{OUT}$ Efficiency vs Output Current**




VOUT = 9V PFM Fsw = 2.2MHz

**Figure 6-5. 9 $V_{OUT}$ Regulation vs Output Current**

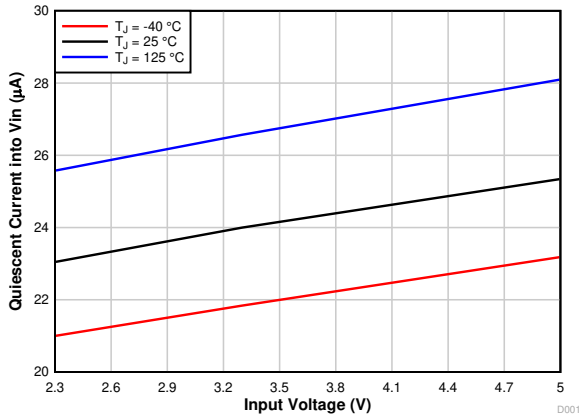



**Figure 6-6. Quiescent Current Into $V_{IN}$ vs Input Voltage**


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## 6.6 Typical Characteristics (continued)

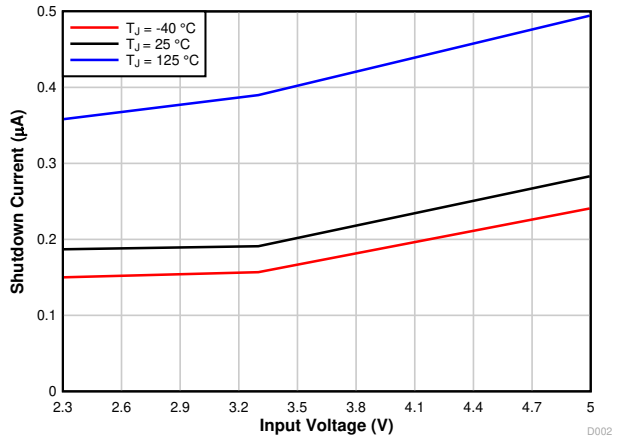



Figure 6-7. Shutdown Current vs Input Voltage

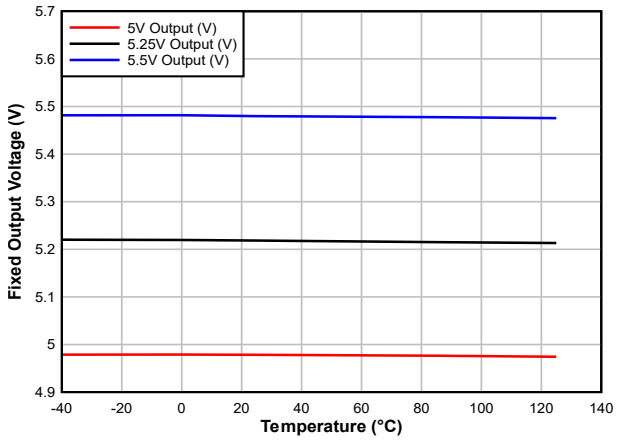



Figure 6-8. Fixed Output Voltage vs Temperature

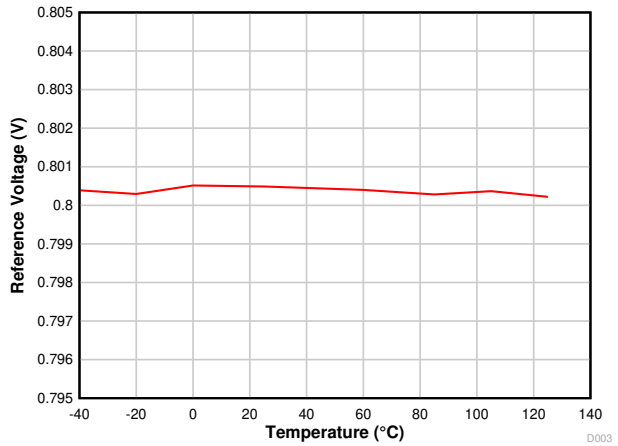



Figure 6-9. Reference Voltage vs Temperature

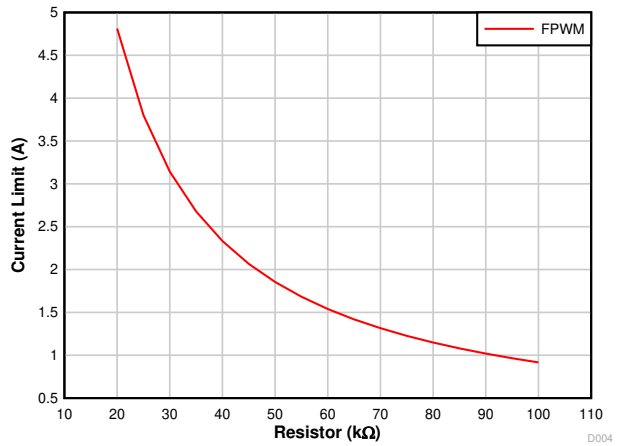



Figure 6-10. Current Limit vs Setting Resistance

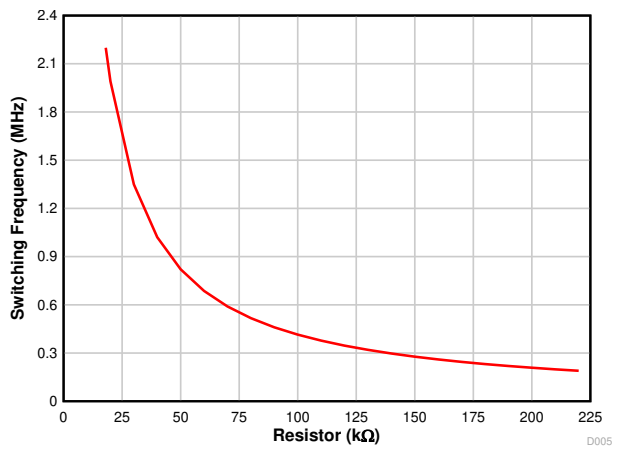



Figure 6-11. Switching Frequency vs Setting Resistance

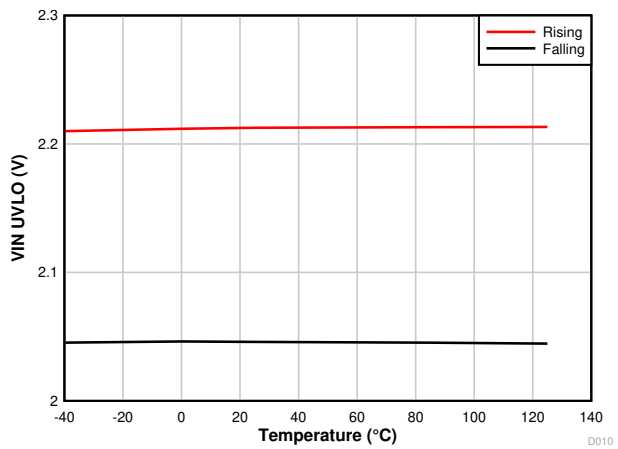



Figure 6-12. $V_{IN}$ UVLO Threshold Voltage vs Temperature

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## 6.6 Typical Characteristics (continued)

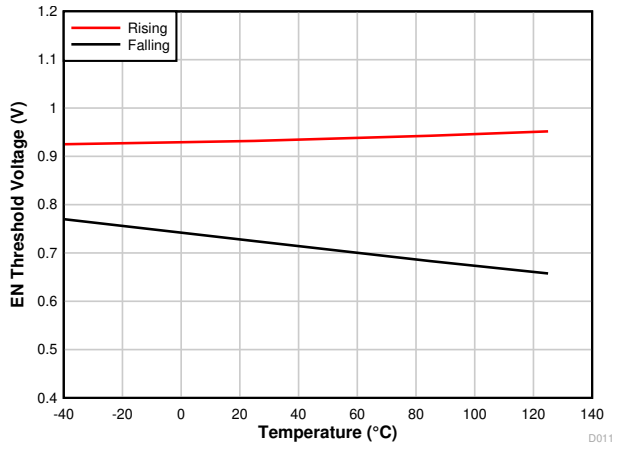



Figure 6-13. EN Threshold Voltage vs Temperature

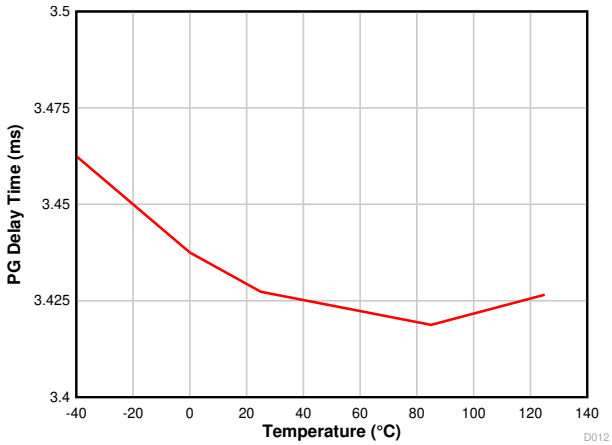



Figure 6-14. PG Delay Time vs Temperature

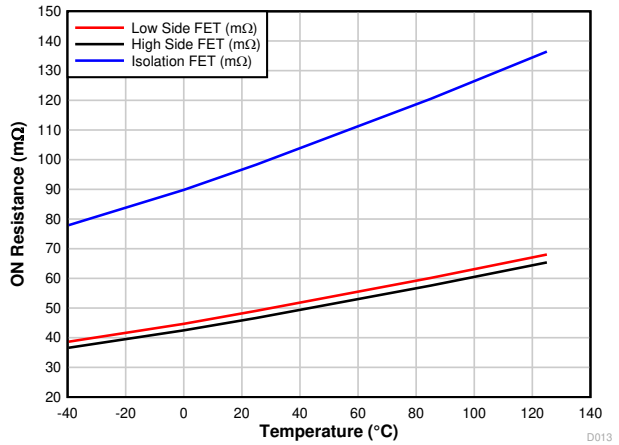



Figure 6-15. $R_{DSON}$ vs Temperature

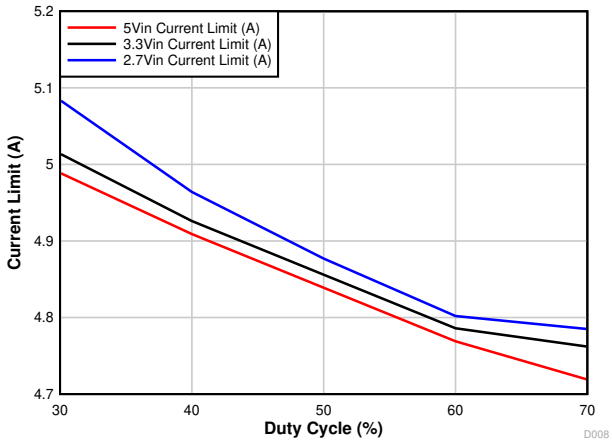



Figure 6-16. Duty Cycle vs Current Limit


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# 7 Detailed Description

## 7.1 Overview

The TPS61378-Q1 is a fully-integrated synchronous boost converter with load disconnect function. The device supports output voltage up to 18.5V with a maximum of a 4.8A programmable switching peak current limit. The input voltage ranges from 2.3V to 14V while consuming 25µA quiescent current.

The TPS61378-Q1 uses the fixed-frequency peak current control scheme, which has an internal oscillator and supports adjustable switching frequency from 200kHz to 2.2MHz.

The TPS61378-Q1 operates with fixed-frequency pulse width modulation (PWM) from medium to heavy load. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on. The inductor current ramps up to a peak current that is determined by the output of the internal error amplifier (EA). Once the switching peak current triggers the output of the EA, the low-side N-MOSFET is turned off and the high-side N-MOSFET is turned on after a short dead time. The high-side N-MOSFET switch is not turned off until the next cycle as determined by the internal oscillator. The low-side switch turns on again after a short dead time and the switching cycle is repeated.

The TPS61378-Q1 provides either auto PFM or forced PWM for the light load operation by configuring the MODE/SYNC pin. In forced PWM mode, the switching frequency remains constant across the entire load range, which helps avoid frequency variation with load. The internal oscillator can be synchronized to an external clock applied on the MODE/SYNC pin. Spread spectrum modulation of the frequency in forced PWM mode helps optimize the EMI performance for automotive applications. In auto PFM mode, the switching frequency can decrease, resulting in higher efficiency.

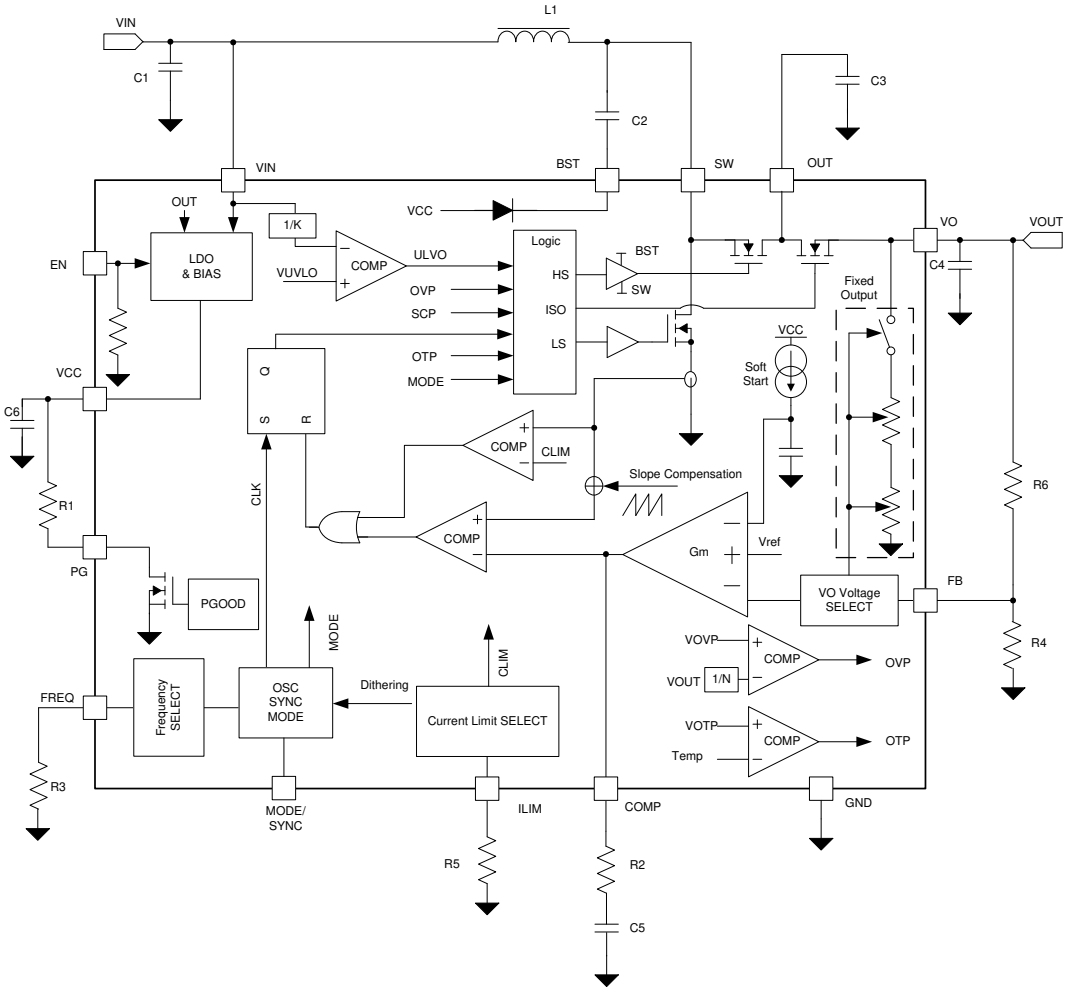
The TPS61378-Q1 implements a cycle-by-cycle current limit to protect the device from overload during the boost operation phase. If the output current further increases and triggers the output voltage to fall below the input voltage, the TPS61378-Q1 enters into hiccup mode short protection.

There is a built-in soft-start time, which prevents the inrush current during the start-up. The TPS61378-Q1 also provides a power good (PG) indicator to enable the power sequence control for start-up.

The TPS61378-Q1 also has several protection features including output short protection, output overvoltage protection (OVP), and thermal shutdown protection (OTP).

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## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 VCC Power Supply

The internal LDO in the TPS61378-Q1 outputs a regulated voltage of 4.8V with 10mA output current capability. A ceramic capacitor is connected between the VCC pin and GND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The value of this ceramic capacitor must be above 1µF. Ti recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10V.

### 7.3.2 Input Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.04V (typical). A hysteresis of 160mV (typical) is added so that the device cannot be enabled again until the input voltage exceeds 2.2V (typical). This function is implemented to prevent the device from malfunctioning when the input voltage is between 2.04V and 2.2V.

### 7.3.3 Enable and Soft Start

When the input voltage is above the UVLO threshold and the EN pin is pulled above 1.2V, the TPS61378-Q1 is enabled. The device starts to monitor the FB pin. With a typical 400-µs delay time after EN is pulled high, the TPS61378-Q1 starts switching. There is an internal built-in start-up time, typically 2.5ms, to limit the inrush current during start-up.


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### 7.3.4 Shut Down

When the input voltage is below the UVLO threshold or the EN pin is pulled low, The TPS61378-Q1 is in shutdown mode and all the functions are disabled. The input voltage is isolated from the output to minimize the leakage currents.

### 7.3.5 Switching Frequency Setting

The TPS61378-Q1 uses a fixed-frequency control scheme. The switching frequency can be programmed between 200kHz and 2.2Mhz using a resistor from the FREQ pin to GND. The resistor must be connected when the oscillator is synchronized by external clock. The resistance is defined by Equation 1.

$$F_{SW}(MHz) = \frac{41.9}{R_{FREQ}(k\Omega) + 1.05} \quad (1)$$

where

- $R_{FRQE}$ is the resistance between the FREQ pin and the GND pin

For example, the switching frequency is 2.2MHz if the resistance between FREQ pin and GND is 18kΩ. This pin cannot be left floating or tied to VCC.

### 7.3.6 Spread Spectrum Frequency Modulation

The TPS61378-Q1 uses a triangle waveform to spread the switching frequency with ±10% of normal frequency. The frequency of the triangle waveform is typically 0.4% of the switching frequency. For example, if the normal switching frequency of the TPS61378-Q1 is programmed to 2.2MHz, the spread spectrum function modulates the switching frequency in the range of 1.98MHz to 2.42MHz in a triangle behavior with an 8.8kHz rate.

The spread spectrum is only available while the clock of the TPS61378-Q1 is free running at the natural frequency in FPWM mode. Any of the following conditions overrides spread spectrum, turning spread spectrum off:

- An external clock is applied to the MODE/SYNC pin.
- The MODE/SYNC pin is configured to be logic low or floating.

### 7.3.7 Adjustable Peak Current Limit

The TPS61378-Q1 adopts a cycle-by-cycle peak current limit internally and changes the current limit with different working conditions. The low-side switch is turned off immediately as soon as the switch peak current triggers the peak current limit. The peak switch current limit can be set by a resistor from the ILIM pin to ground. Equation 2 shows the relationship between the peak current limit and the resistor.

$$R_{LIM}(k\Omega) = 1.184 + \frac{90.56}{I_{LIM}(A)} \quad (2)$$

where

- $R_{ILIM}$ is the resistance between the ILIM pin and the GND. This pin cannot be left floating or connected to VCC.
- $I_{LIM}$ is switch peak current limit

For instance, the current limit is set to 4.8A if the $R_{LIM}$ is 20kΩ.

Table 7-1 lists the peak current limit under various conditions. The current limit applies to the start-up phase.

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**Table 7-1. Switch Peak Current Limit**

| BEHAVIOR | SWITCH PEAK CURRENT LIMIT |
|---|---|
| Vin < VO (Not in Down Mode) | $I_{LIM}$(1) |
| Vin < VO (In Down Mode) | $2/3I_{LIM}$ |
| 3V > Vin – VO > 0V | $4/9I_{LIM}$ |
| 6V > Vin - VO > 3V | $1/4I_{LIM}$ |
| Vin – VO > 6V | $1/4I_{LIM}$ and Fsw Clamp to 1.1MHz if FREQ pin setting is > 1.1MHz |
| FB ≤ 0.1V | $1/5I_{LIM}$ and Fsw Clamp to 1.1MHz if FREQ pin setting is > 1.1MHz |

(1) $I_{LIM}$ is switch peak current limit programmed in Equation 2.

### 7.3.8 Bootstrap

The TPS61378-Q1 has an integrated bootstrap regulator circuit. A small ceramic capacitor is needed between the BST pin and SW pin to provide the gate drive supply voltage for high-side switches. The bootstrap capacitor is charged during the time when the low-side switch is in the ON state. The value of this ceramic capacitor must be above 0.1µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 6.3V.

### 7.3.9 Load Disconnect

The TPS61378-Q1 integrates a load disconnect function when the input source is DC, completely cutting off the path between the input side and output side during shutdown.

The output disconnect function also allows the output short protection and minimizes the inrush current at start-up.

### 7.3.10 MODE/SYNC Configuration

Table 7-2 summarizes the MODE/SYNC function and the entry condition.

**Table 7-2. MODE/SYNC Configuration**

| MODE/SYNC PIN CONFIGURATION | MODE |
|---|---|
| Logic Low or Floating | Auto PFM Mode |
| Logic High | Forced PWM Mode |
| External Synchronization | Forced PWM Mode |

The TPS61378-Q1 can be synchronized to an external clock applied to the MODE/SYNC pin.

### 7.3.11 Overvoltage Protection (OVP)

If the output voltage exceeds the OVP threshold (typically 20V), the TPS61378-Q1 immediately stops switching until the output voltage drops below the recovery threshold (typically 19.5V). This function protects the device against excessive voltage.

### 7.3.12 Output Short Protection/Hiccup

In addition to the cycle-by-cycle current limit function, the TPS61378-Q1 also has output short protection.

During normal working condition, when output draws an excessive amount of current, causing the low-side FET to reach peak current limit and the output voltage is pulled below the input voltage, the device enters short-circuit protection mode, triggering the hiccup timer. When the hiccup timer is active, the device limits the current for 1.8ms and then shuts down. After 67ms, the device restarts.

During start-up, whether normal start-up or hiccup restart, the device can trigger short protection. The device has limited loading capacity at start up phase because of smaller peak current limit, which is listed in Table 7-1.

Starting up with heavy load or very large capacitors at output side can cause short hiccup protection.


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#### 7.3.13 Power-Good Indicator

The TPS61378-Q1 integrates a power-good function. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connect to an appropriate voltage supply like VCC. The PG pin goes high with a typical 3.4ms delay time after VOUT reaches 90% of the target output voltage. When the output voltage drops below 85% of the target output voltage, the PG pin immediately goes low without delay.

#### 7.3.14 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown occurs at junction temperatures exceeding 165°C. When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 145°C (typical).

### 7.4 Device Functional Modes

#### 7.4.1 Forced PWM Mode

The TPS61378-Q1 enters forced PWM mode by pulling the MODE/SYNC pin to logic high for more than five switching cycles. In forced PWM mode, the TPS61378-Q1 keeps the switching frequency constant at light load condition. When the load current decreases, the output of the internal error amplifier also decreases to keep the inductor peak current down. When the output current decreases further, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant.

#### 7.4.2 Auto PFM Mode

The TPS61378-Q1 enters auto PFM Mode by pulling the MODE/SYNC pin to logic low for more than five switching cycles or leaving the pin floating. The TPS61378-Q1 improves the efficiency at light load when operating in PFM mode. When the output current decreases to a certain level, the output voltage of the error amplifier is clamped by the internal circuit. If the output current reduces further, the inductor current through the high-side switch is clamped but not lowered further. Pulses are skipped to improve the efficiency at light load.

#### 7.4.3 External Clock Synchronization

The TPS61378-Q1 supports external clock synchronization with a range of 200kHz to 2.2MHz. The external clock must be within -+20% of the setting frequency to confirm a reliable synchronization. The TPS61378-Q1 remains in forced PWM mode and operates in CCM across the entire load range if the oscillator is synchronized by an external clock. The spread-spectrum feature is disabled when external synchronization is used.

#### 7.4.4 Down Mode

The TPS61378-Q1 features down mode operation when input voltage is close to or higher than output voltage. In down mode, output voltage is regulated at target value, even when $V_{IN} > V_O$. The TPS61378-Q1 high-side and low-side FETs are switching devices that always work in boost operation, where the isolation FET always works as a linear device.

For boost circuits, on-time or duty cycle is reduced as input voltage approaches output voltage. The TPS61378-Q1 enters down mode when $V_{IN}$ reaches 85% (typical) of $V_O$ voltage at 2.2MHz. Exiting down mode requires $V_{IN}$ to be reduced below 85% (typical) of $V_O$ voltage at 2.2MHz.

In normal operation, the isolation FET is fully on.

When down mode is triggered and $V_{IN}$ is less than VO pin voltage, the OUT pin has a fixed 2V (typical) above VO pin voltage. An isolation FET works in LDO mode to regulate VO pin voltage with a 2V constant voltage drop.

When down mode is triggered and $V_{IN}$ is 100mV (typical) higher than VO pin voltage, the OUT pin has an approximated 3V (typical) above the $V_{IN}$ pin voltage. As $V_{IN}$ keeps rising, the OUT pin continues rising with 3V on top of $V_{IN}$. In addition, an isolation FET works in LDO mode to regulate VO pin voltage with a voltage differential of the OUT pin and VO pin.

See also Figure 7-1.

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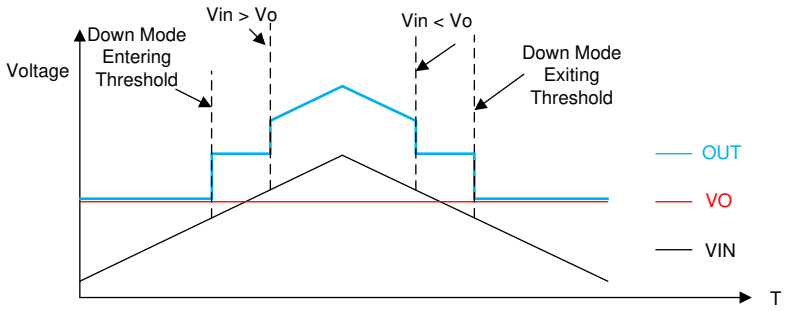



**Figure 7-1. Down Mode**

Take care during short-to-ground condition when operation $V_{IN}$ is above 6V. During hiccup on, the device operates in down mode and the isolation FET voltage drop is $V_{IN}$ + 3V (OUT pin to VO pin).


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS61378-Q1 is a 25-µA quiescent current boost converter that supports a 2.3V to 14V input voltage range. The device also supports load disconnect to minimize the leakage current. The following design procedure can be used to select component values for the TPS61378-Q1.

## 8.2 Typical Application

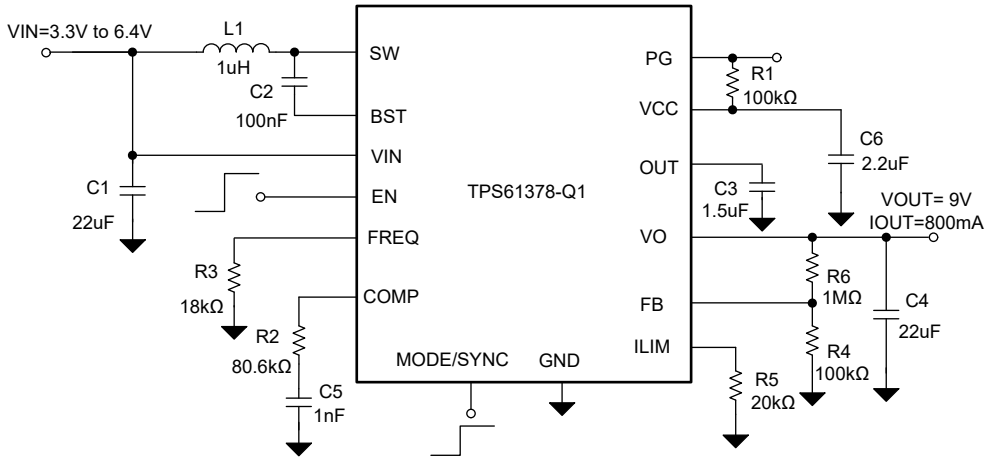



**Figure 8-1. Typical Application**

### *8.2.1 Design Requirements*

A typical application example is dual cameras powered through a coax cable, which normally requires 9.0V output as the bias voltage and consumes less than 600mA current. 800mA load current is designed to provide margin. The following design procedure can be used to select external component values for the TPS61378-Q1.

**Table 8-1. Design Requirements**

| PARAMETERS | VALUES |
|---|---|
| Input voltage | 3.3V to 6.4V |
| Output voltage | 9.0V |
| Switching frequency | 2.2MHz |
| Output current | 800mA |
| Output voltage ripple | ± 25mV |

### *8.2.2 Detailed Design Procedure*

#### 8.2.2.1 Programming the Output Voltage

The output voltage is determined by the resistor sensed from FB pin before device is enabled.

There are two ways to set the output voltage of the TPS61378-Q1, adjustable output voltage (for TPS61378-Q1 and TPS613783-Q1 only) and fixed output voltage.

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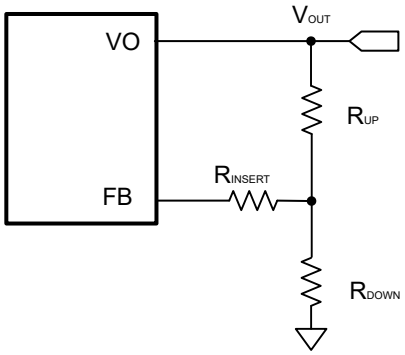



**Figure 8-2. Typical Connection of FB Pin For Adjustable Output Voltage**

Figure 8-2 shows the typical circuit of the FB pin connection for adjustable output voltage. Equation 3 calculates the FB resistor $R_{FB}$:

$$R_{FB} = R_{INSERT} + \frac{R_{UP} \times R_{DOWN}}{R_{UP} + R_{DOWN}} \quad (3)$$

When selected for adjustable output voltage, $R_{FB}$ must be above 14.4kΩ. The FB pin is connected to the negative input of the internal error amplifier directly. The output voltage can be programmed by adjusting the external resistor divider $R_{UP}$ and $R_{DOWN}$ according to Equation 4.

$$V_{OUT} = V_{REF} \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} \quad (4)$$

Equation 4 shows that the output voltage setting is only influenced by $R_{UP}$ and $R_{DOWN}$. In normal application, $R_{INSERT}$ can be 0Ω, that is, directly connect FB pin to middle point of feedback voltage divider.

For automotive application that do not prefer to use resistors more than 100kΩ, $R_{INSERT}$ (> 15kΩ) can be used so that calculated $R_{UP}$ and $R_{DOWN}$ feedback resistor value can be less than 100kΩ.

When working with adjustable voltage, for the best accuracy, TI recommends $R_{DOWN}$ to be smaller than 160kΩ to confirm that the current flowing through $R_{DOWN}$ is at least 100 times larger than FB pin leakage current. Changing $R_{DOWN}$ toward the lower value increases the robustness against noise injection. Changing $R_{DOWN}$ to higher values reduces the quiescent current to achieve higher efficiency at light load.

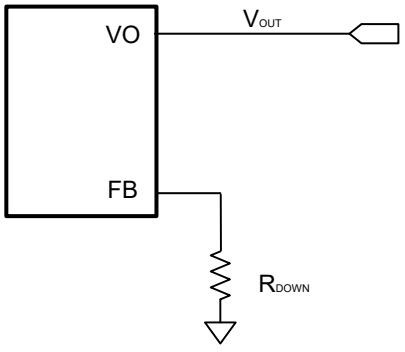



**Figure 8-3. Typical Connection of FB Pin For Fixed Output Voltage**

Figure 8-3 shows the typical circuit of the FB pin connection for fixed output voltage. Equation 5 calculates the FB resistor $R_{FB}$:

$$R_{FB} = R_{DOWN} \quad (5)$$


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When designed for fixed output voltage, the TPS61378-Q1 uses the internal resistor divider and works with fixed output voltage. The TPS61378-Q1 subdivides the voltage due to $R_{FB}$ and device part number. See also *Device Comparison Table* for detailed information.

#### 8.2.2.2 Setting the Switching Frequency

The switching frequency of the TPS61378-Q1 is set at 2.2MHz. Use Equation 1 to calculate the required resistor value. The calculated value is 18kΩ to get the frequency of 2.2MHz.

#### 8.2.2.3 Setting the Current Limit

The current limit of the TPS61378-Q1 can be programmed by an external resistor. For a target current limit of 4.8A, use Equation 2. The calculated resistor value is 20kΩ.

#### 8.2.2.4 Selecting the Inductor

A boost converter normally requires two main passive components for storing energy during power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency), transient behavior, and loop stability, which makes the inductor the most critical component in application.

When selecting the inductor and the inductance, the other important parameters are:

- The maximum current rating (consider RMS and peak current)
- The series resistance
- Operating temperature

The TPS61378-Q1 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 2A, the slope compensation can not be adequate, and the loop can be unstable. Therefore, TI recommends to make the peak-to-peak current ripple between 800mA to 2A when selecting the inductor.

Equation 6, Equation 7, and Equation 8 calculate the inductance:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{6}$$

$$\Delta I_{L_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \tag{7}$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}} \tag{8}$$

where

- $\Delta_{IL}$ is the peak-peak inductor current ripple
- $V_{IN}$ is the input voltage
- D is the duty cycle
- L is the inductor
- $f_{SW}$ is the switching frequency
- Ripple % is the ripple ration versus the DC current
- $V_{OUT}$ is the output voltage
- $I_{OUT}$ is the output current
- η is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have ±20%, or even ±30%, tolerance with no current bias. When the inductor current approaches the saturation level, the inductance can decrease 20% to 35% from the value at 0A bias current,

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depending on how the inductor vendor defines saturation. When selecting an inductor, make sure the rated current, especially the saturation current, is larger than the peak current during the operation.

The inductor peak current varies as a function of the load, switching frequency, and input and output voltages. Equation 9 and Equation 10 calculate the peak current.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L \tag{9}$$

where

- $I_{PEAK}$ is the peak current of the inductor
- $I_{IN}$ is the input average current
- $\Delta_{IL}$ is the ripple current of the inductor

The input DC current is determined by the output voltage. Use the following equation to calculate the output current:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{10}$$

where

- $I_{IN}$ is the input current of the inductor
- $V_{OUT}$ is the output voltage
- $V_{IN}$ is the input voltage
- $\eta$ is the efficiency

While the inductor ripple current depends on the inductance, Equation 6 calculates the frequency, the input voltage, and duty cycle. Replace Equation 6 and Equation 10 into Equation 9 and get the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \tag{11}$$

where

- $I_{PEAK}$ is the peak current of the inductor
- $I_{OUT}$ is the output current
- D is the duty cycle
- $\eta$ is the efficiency
- $V_{IN}$ is the input voltage
- L is the inductor
- $f_{SW}$ is the switching frequency

Equation 12 calculates the heat rating current (RMS):

$$I_{L_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2} \tag{12}$$

where

- $I_{L_RMS}$ is the RMS current of the inductor
- $I_{IN}$ is the input current of the inductor
- $\Delta_{IL}$ is the ripple current of the inductor

Make sure that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature-related rating current of the inductors.


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For a given physical inductor size, increasing inductance typically results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency-dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, there is usually a tradeoff between the loss and foot print. Table 8-2 lists some recommended inductors.

**Table 8-2. Recommended Inductors**

| PART NUMBER | L (µH) | DCR TYP (mΩ) MAX | SATURATION CURRENT (A) | SIZE (L × W × H mm) | VENDOR(1) |
|---|---|---|---|---|---|
| XEL4030-471MEB | 0.47 | 4.1 | 15.5 | 4x 4x 3 | Coilcraft |
| XEL4030-102MEB | 1 | 8.9 | 9 | 4x 4x 3 | Coilcraft |
| DFE2HCAHR47MJ0L | 0.47 | 25 | 5.1 | 2.5x 2x 1.2 | Murata |
| DFE322520FD-1R0M | 1 | 22 | 7.5 | 3.2x 2.5x 2 | Murata |
| TFM322512ALMAR47MTAA | 0.47 | 16 | 7.6 | 3.2x 2.5x 1.2 | TDK |
| TFM322512ALMA1R0MTAA | 1 | 30 | 5.1 | 3.2x 2.5x 1.2 | TDK |

(1) See the *Third-party Products Disclaimer*.

#### 8.2.2.5 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. The loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and the capacitance. Assuming a capacitor with zero ESR, Equation 13 calculates the minimum capacitance needed for a given ripple :

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (13)$$

where

- $C_{OUT}$ is the output capacitor
- $I_{OUT}$ is the output current
- $V_{OUT}$ is the output voltage
- $V_{IN}$ is the input voltage
- $\Delta_V$ is the output voltage ripple required
- $f_{SW}$ is the switching frequency

Equation 14 calculates the additional output ripple component caused by ESR:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (14)$$

where

- $\Delta V_{ESR}$ is the output voltage ripple caused by ESR
- $R_{ESR}$ is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, the ESR ripple must be considered if used.

Equation 15 calculates the minimum ceramic output capacitance needed to meet a load transient requirement:

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$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (15)$$

where

- $\Delta I_{STEP}$ is the transient load current step
- $\Delta V_{TRAN}$ is the allowed voltage dip for the load current step
- $f_{BW}$ is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero)

For the output capacitor on the OUT pin, the effective capacitance is recommended between 0.22µF to 1µF.

Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of the capacitance at the respective rated voltage. Therefore, enough margins on the voltage rating must be considered to confirm adequate capacitance at the required output voltage.

#### 8.2.2.6 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter because multilayer ceramic capacitors have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 22µF input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the device. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, must be placed between $C_{IN}$ and the power source lead to reduce ringing that can occur between the inductance of the power source leads and $C_{IN}$.

#### 8.2.2.7 Loop Stability and Compensation

##### *8.2.2.7.1 Small Signal Model*

The TPS61378-Q1 uses the fixed frequency peak current mode control. There is an internal adaptive slope compensation to avoid subharmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and $C_{OUT}$, to a single-pole system, created by $R_{OUT}$ and $C_{OUT}$. The single-pole system is easily used with the loop compensation. Figure 8-4 shows the equivalent small signal elements of a boost converter.

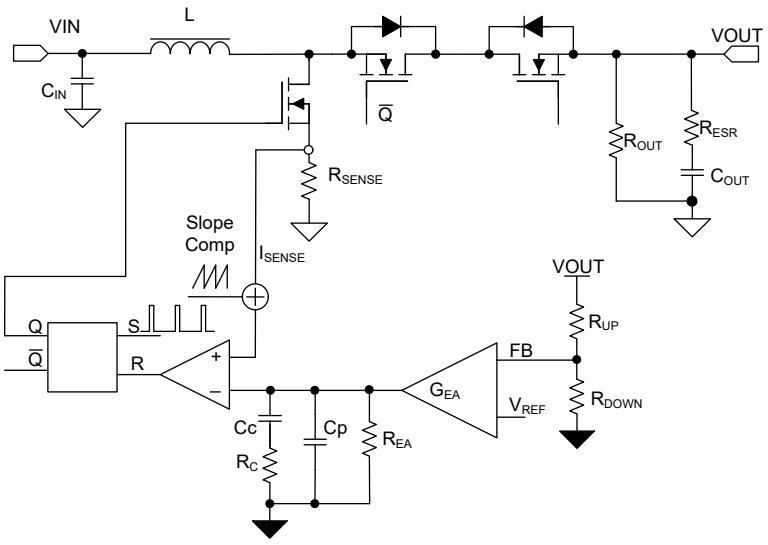



**Figure 8-4. TPS61378-Q1 Control Equivalent Circuitry Model**

The small signal of power stage is:


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$$K_{PS}(S) = \frac{R_{OUT} \times (1-D)}{2 \times R_{SENSE}} \times \frac{(1+\frac{S}{2\pi \times f_{ESR}})(1-\frac{S}{2\pi \times f_{RHP}})}{(1+\frac{S}{2\pi \times f_P})} \quad (16)$$

where

- D is the duty cycle
- $R_{OUT}$ is the output load resistor
- $R_{SENSE}$ is the equivalent internal current sense resistor, which is typically 118mΩ

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \quad (17)$$

where

- $C_{OUT}$ is the output capacitance. For a boost converter having multiple identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (18)$$

where

- $R_{ESR}$ is the equivalent resistance in series of the output capacitor

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1-D)^2}{2\pi \times L} \quad (19)$$

where

- D is the duty cycle
- $R_{OUT}$ is the output load resistor
- L is the inductance

Equation 20 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP}+R_{DOWN}} \times \frac{1+\frac{S}{2\times\pi\times f_Z}}{(1+\frac{S}{2\times\pi\times f_{P1}})\times(1+\frac{S}{2\times\pi\times f_{P2}})} \quad (20)$$

where

- $R_{EA}$ is the output impedance of the error amplifier, typically $R_{EA}$ = 500MΩ
- $f_{P1}$, $f_{P2}$ is the pole frequency of the compensation
- $f_Z$ is the zero's frequency of the compensation network

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_c} \quad (21)$$

where

- $C_C$ is the zero capacitor compensation

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (22)$$

where

- $C_P$ is the pole capacitor compensation
- $R_C$ is the resistor of the compensation network

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (23)$$

#### *8.2.2.7.2 Loop Compensation Design Steps*

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Crossover Frequency, $f_C$.**

   The first step is to set the loop crossover frequency, $f_C$. The higher the crossover frequency, the faster the loop response is. The loop gain crossing over no higher than the lower of either 1/10 of the switching frequency, $f_{SW}$, or 1/5 of the RHPZ frequency, $f_{RHPZ}$, is generally accepted. Then, calculate the loop compensation network values of $R_C$, $C_C$, and $C_P$ by the following equations.
2. **Set the Compensation Resistor, $R_C$.**

   By placing $f_Z$ below $f_C$, for frequencies above $f_C$, $R_C$ | | $R_{EA} \cong R_C$, so $R_C \times G_{EA}$ sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at $f_Z$ results in the total loop gain, $T_{(s)} = K_{PS(s)} \times H_{EA(s)}$, being zero at $f_C$.

   Therefore, to approximate a single-pole rolloff up to $f_{P2}$, rearrange Equation 20 to solve for RC so that the compensation gain, $K_{EA}$, at $f_C$ is the negative of the gain, $K_{PS}$. Read at frequency $f_C$ for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \quad (24)$$

   where

   - $K_{EA}$ is gain of the error amplifier network
   - $K_{PS}$ is the gain of the power stage
   - $G_{EA}$ is the transconductance of the amplifier, the typical value of $G_{EA}$ = 70µA /V
3. **Set the Compensation Zero capacitor, $C_C$.**

   Place the compensation zero at the power stage $R_{OUT}$ ,$C_{OUT}$ pole position to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (25)$$

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \quad (26)$$

4. **Set the Compensation Pole Capacitor, $C_P$.**

   Place the compensation pole at the zero produced by $R_{ESR}$ and $C_{OUT}$. This placement is useful for canceling unhelpful effects of the ESR zero.


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$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (27)$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (28)$$

Set $f_{P2} = f_{ESR}$, and get:

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad (29)$$

#### 8.2.2.7.3 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during the turnon of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1 µF to 1 µF. $C_{BST}$ must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1 µF was selected for this design example.

#### 8.2.2.7.4 $V_{CC}$ Capacitor

The primary purpose of the $V_{CC}$ capacitor is to supply the peak transient currents of the driver and bootstrap capacitor and provide stability for the $V_{CC}$ regulator. The value of $C_{VCC}$ must be at least 10 times greater than the value of $C_{BST}$, and must be a good quality, low-ESR ceramic capacitor. $C_{VCC}$ must be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 2.2 µF was selected for this design example.

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### 8.2.3 Application Curves

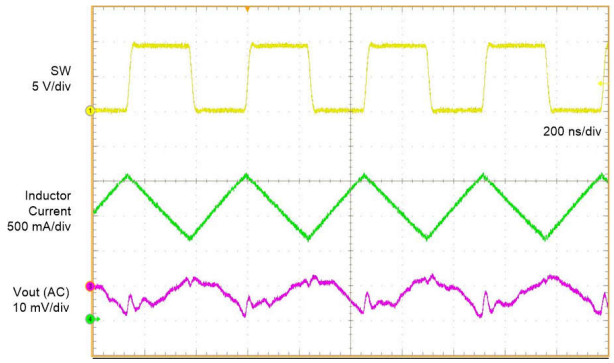



**Figure 8-5. Switching Waveform $V_{IN}$ = 5V, $V_{OUT}$ = 9V, $I_{OUT}$ = 800mA, FPWM**

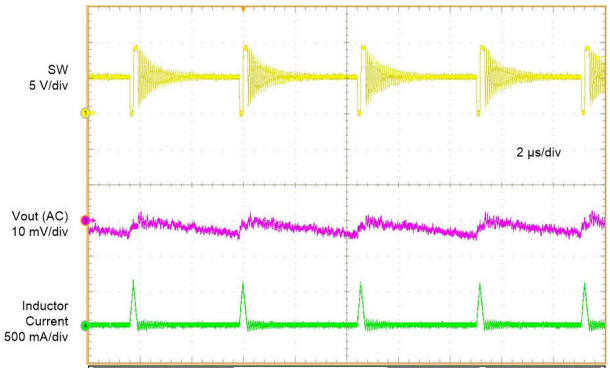



**Figure 8-6. Switching Waveform $V_{IN}$ = 5V, $V_{OUT}$ = 9V, $I_{OUT}$ = 0mA, Auto PFM**

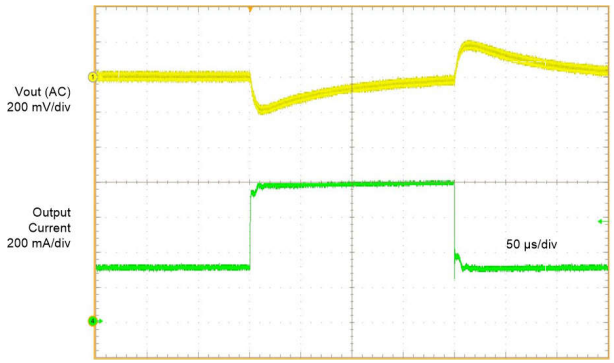



**Figure 8-7. Load Transient $V_{IN}$ = 5V, $V_{OUT}$ = 9V, $I_{OUT}$ = 300mA to 800mA, FPWM**

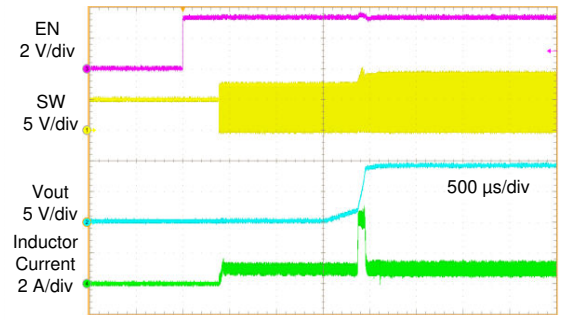



**Figure 8-8. Start-Up From EN Waveform $V_{IN}$ = 5V, $V_{OUT}$ = 9V, $I_{OUT}$ = 500mA, FPWM**

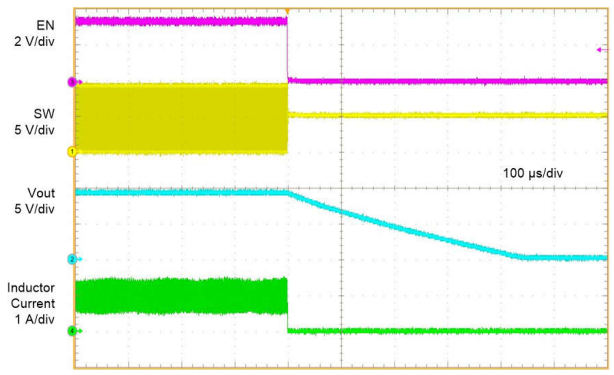



**Figure 8-9. Shutdown From EN Waveforms $V_{IN}$ = 5V, $V_{OUT}$ = 9V, $I_{OUT}$ = 500mA, FPWM**

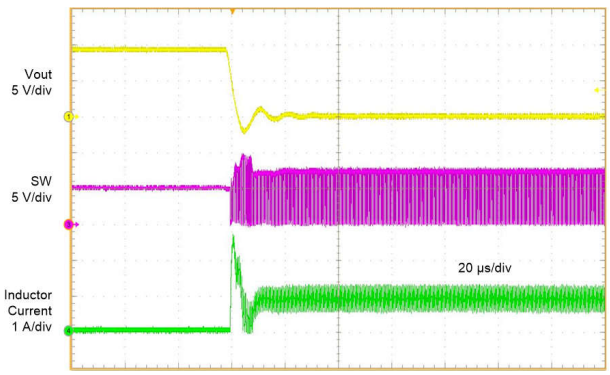



**Figure 8-10. Short-Circuit Protection $V_{IN}$ = 5V, $V_{OUT}$ = 9V, FPWM**


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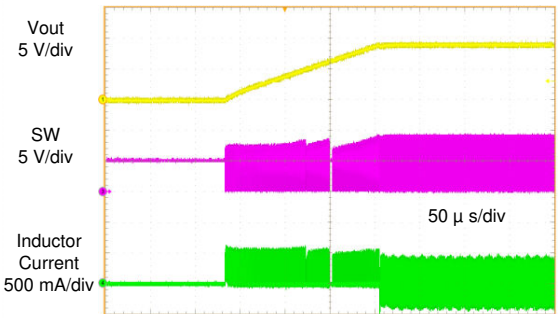



**Figure 8-11. Short-Circuit Recovery $V_{IN}$ = 5V, $V_{OUT}$ = 9V, $I_{OUT}$ = 0mA, FPWM**

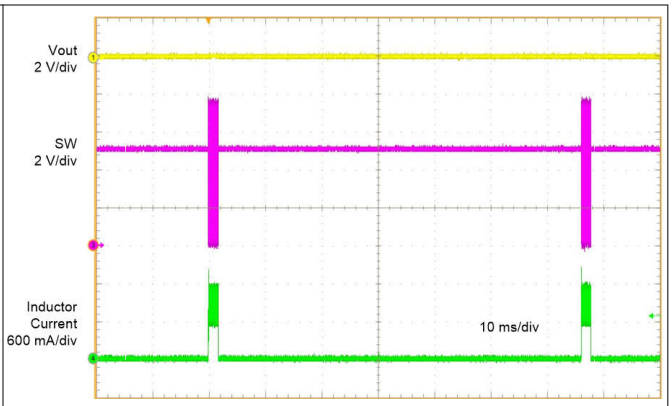



**Figure 8-12. Hiccup Short-Circuit Protection $V_{IN}$ = 5V, $V_{OUT}$ = 9V, FPWM**

## 8.3 Power Supply Recommendations

The TPS61378-Q1 is designed to operate from an input voltage supply range between 2.3V to 14V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

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## 8.4 Layout

### 8.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor must be placed as close as possible to the IC.

### 8.4.2 Layout Example

The bottom layer is a large GND plane connected by vias.

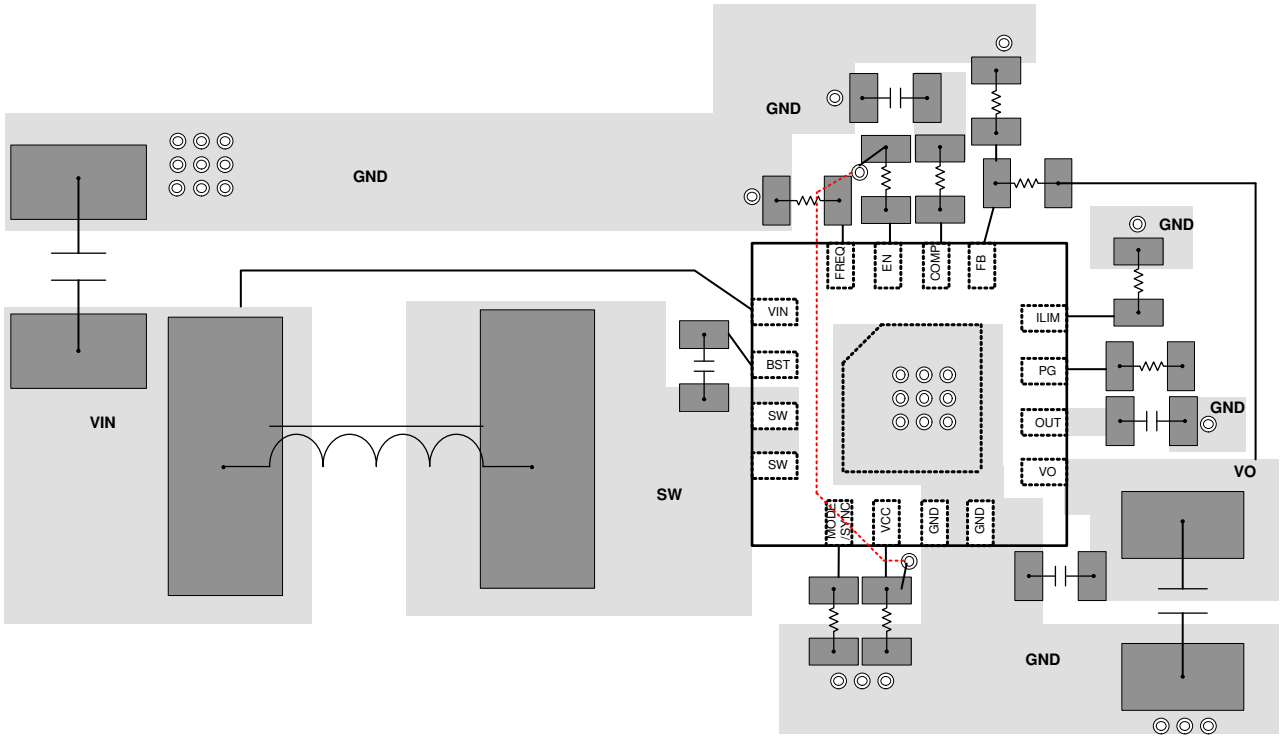



**Figure 8-13. Recommended Layout**


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# 9 Device and Documentation Support

## 9.1 Device Support

### *9.1.1 Third-Party Products Disclaimer*

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## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.4 Trademarks

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## 9.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 10 Revision History

| Changes from Revision E (October 2024) to Revision F (November 2026) | Page |
|---|---|
| • Added *Automotive* to the document title | 1 |
| • Updated table notes in the *ESD Ratings* table | 5 |
| • Add Spike Spec | 5 |

| Changes from Revision D (October 2021) to Revision E (October 2024) | Page |
|---|---|
| • Added TPS61378L | 1 |
| • Added additional features | 1 |
| • Updated Package to WQFN-16 | 1 |
| • Updated Output Voltage Selection Resistor in the Device Comparison Table | 3 |
| • Updated Figure 6-8 | 8 |
| • Added additional information to Spread Spectrum Frequency Modulation | 13 |
| • Added Table 7-1 | 13 |
| • Added additional information to Output Short Protection/Hiccup | 14 |

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- Added "The external clock needs to be within -+20% of the setting frequency to ensure a reliable synchronization."....15
- Updated Figure 8-1....17
- Added additional information and Figure 8-2 and Figure 8-3....17

**Changes from Revision C (June 2021) to Revision D (October 2021)** **Page**

- Updated Section 7.3.13....15
- Updated Figure 8-4....22

**Changes from Revision B (February 2021) to Revision C (June 2021)** **Page**

- Updated resistor from FB to GND values....3
- Updated Section 8.2.2.1....17

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, see also the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS613783QWRTERQ1 | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2G8H |
| TPS613783QWRTERQ1.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2G8H |
| TPS613785QWRTERQ1 | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2G9H |
| TPS613785QWRTERQ1.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2G9H |
| TPS61378LQWRTERQ1 | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 61378L |
| TPS61378LQWRTERQ1.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 61378L |
| TPS61378QWRTERQ1 | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2ELH |
| TPS61378QWRTERQ1.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2ELH |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

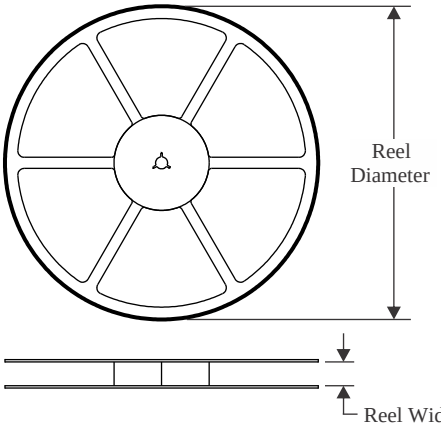
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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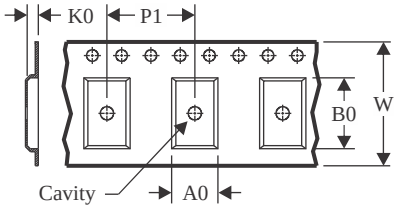
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

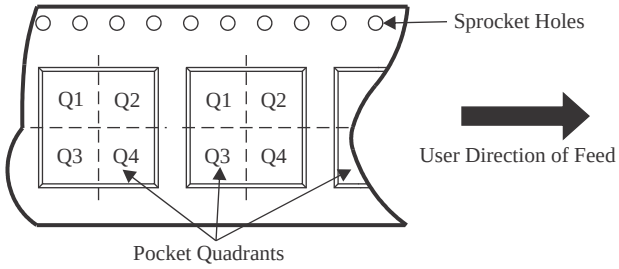



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

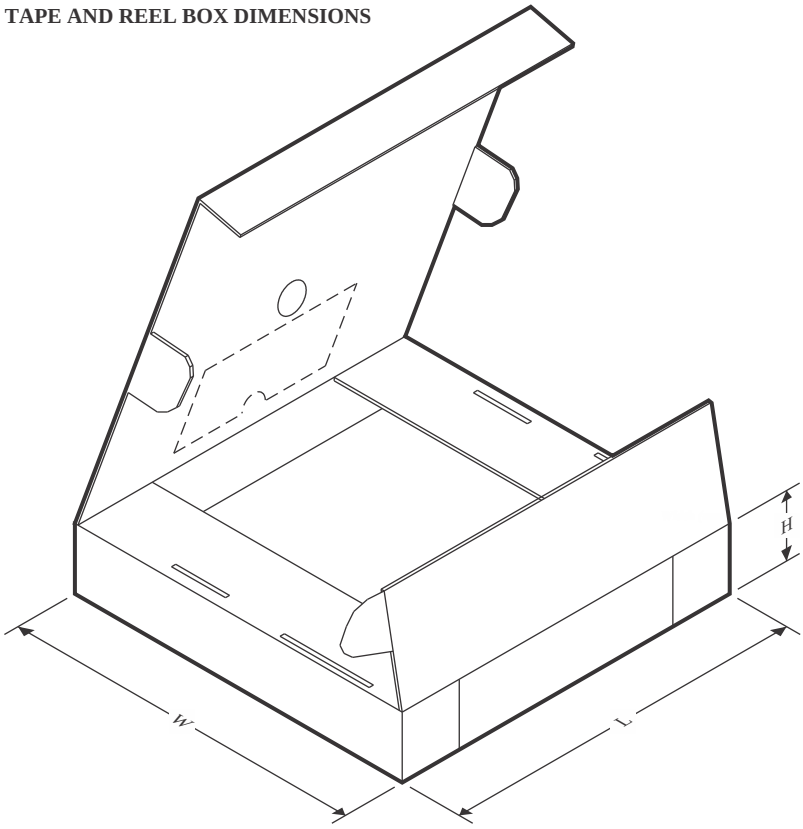
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS613783QWRTERQ1 | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS613783QWRTERQ1 | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS613785QWRTERQ1 | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61378LQWRTERQ1 | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61378QWRTERQ1 | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS613783QWRTERQ1 | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS613783QWRTERQ1 | WQFN | RTE | 16 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS613785QWRTERQ1 | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS61378LQWRTERQ1 | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS61378QWRTERQ1 | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |

# GENERIC PACKAGE VIEW

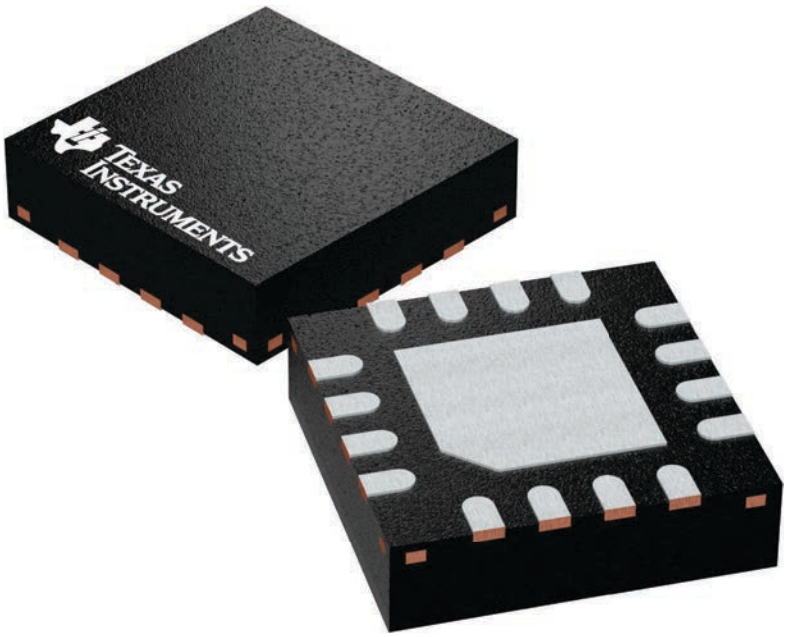
## RTE 16

## WQFN - 0.8 mm max height

**3 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

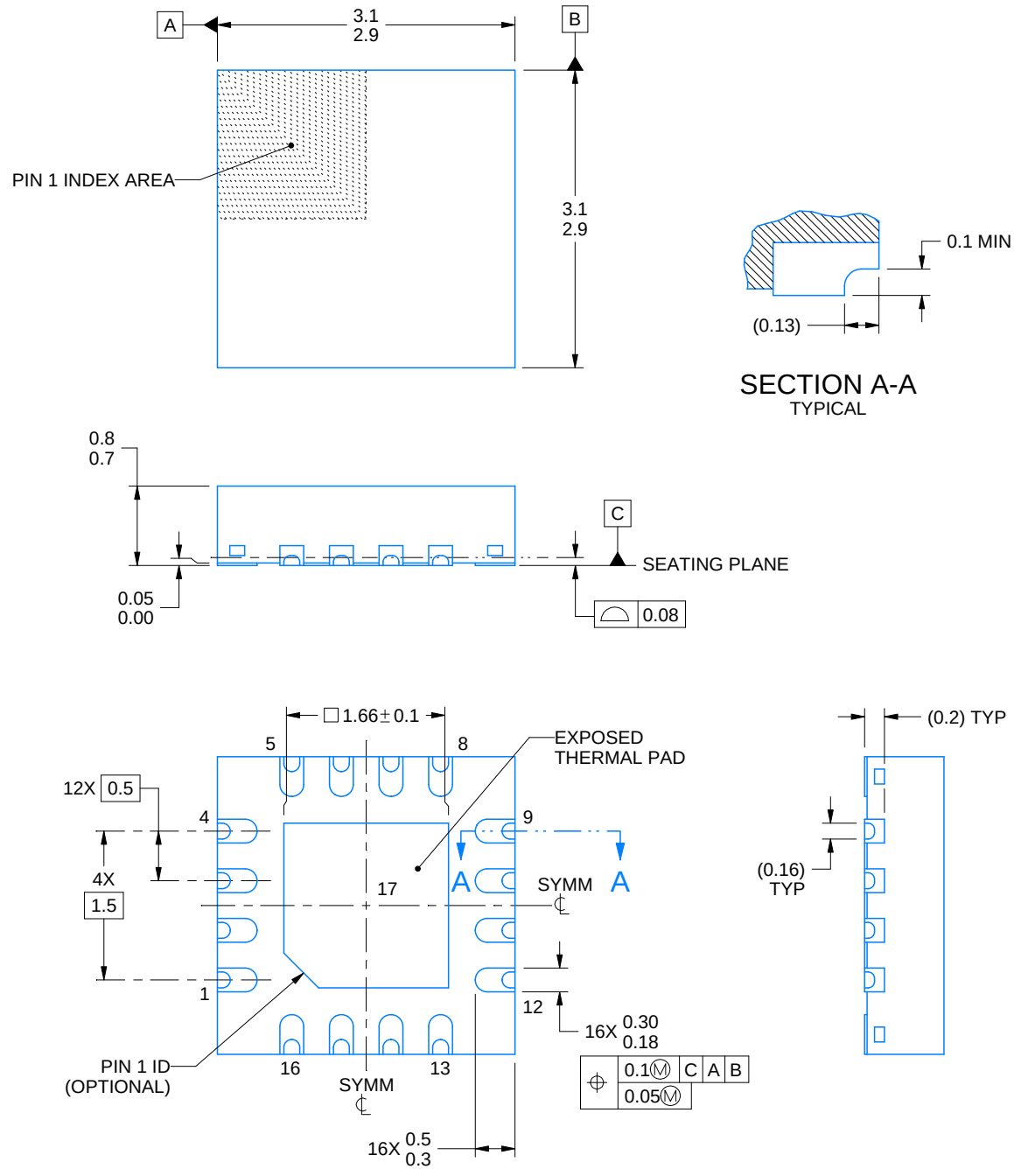


# RTE0016K

# PACKAGE OUTLINE

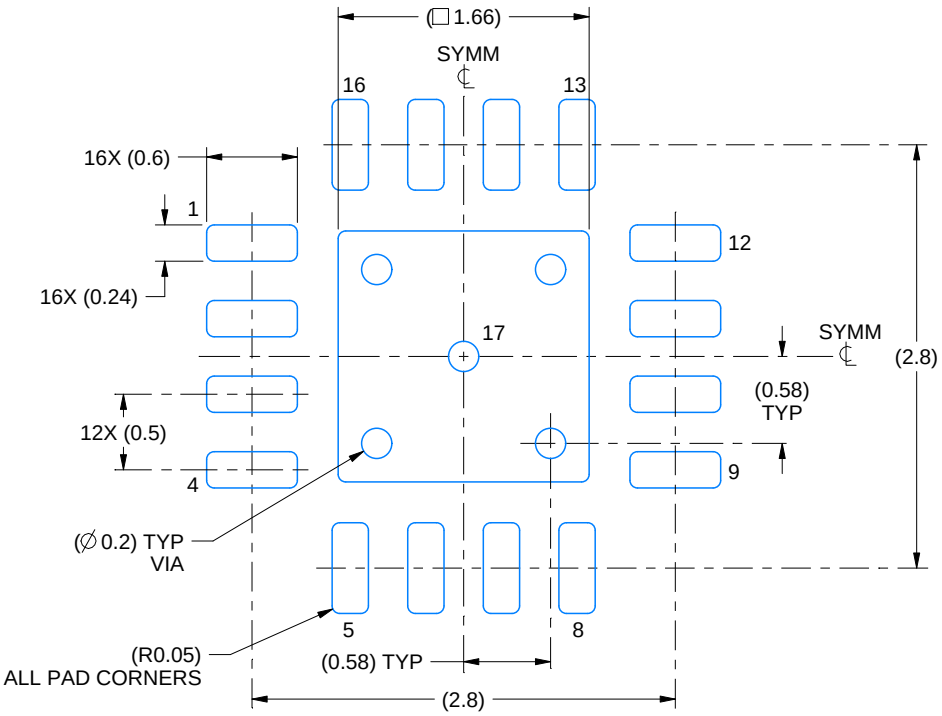
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

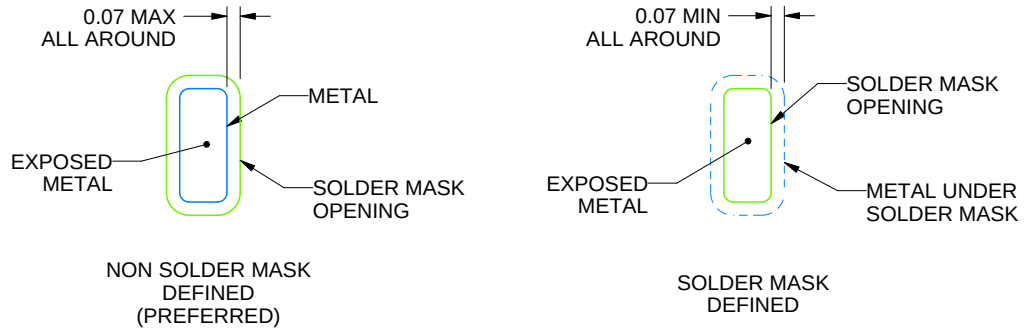



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

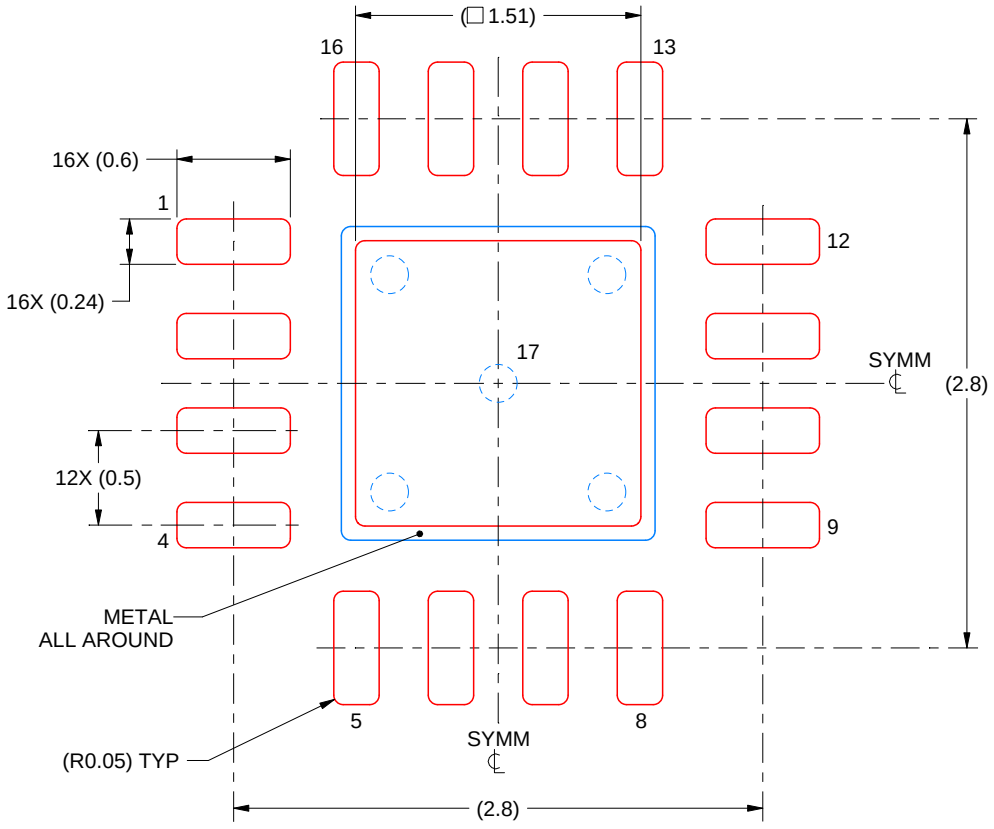



SOLDER MASK DETAILS

4224938/C 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/C 03/2022

NOTES: (continued)

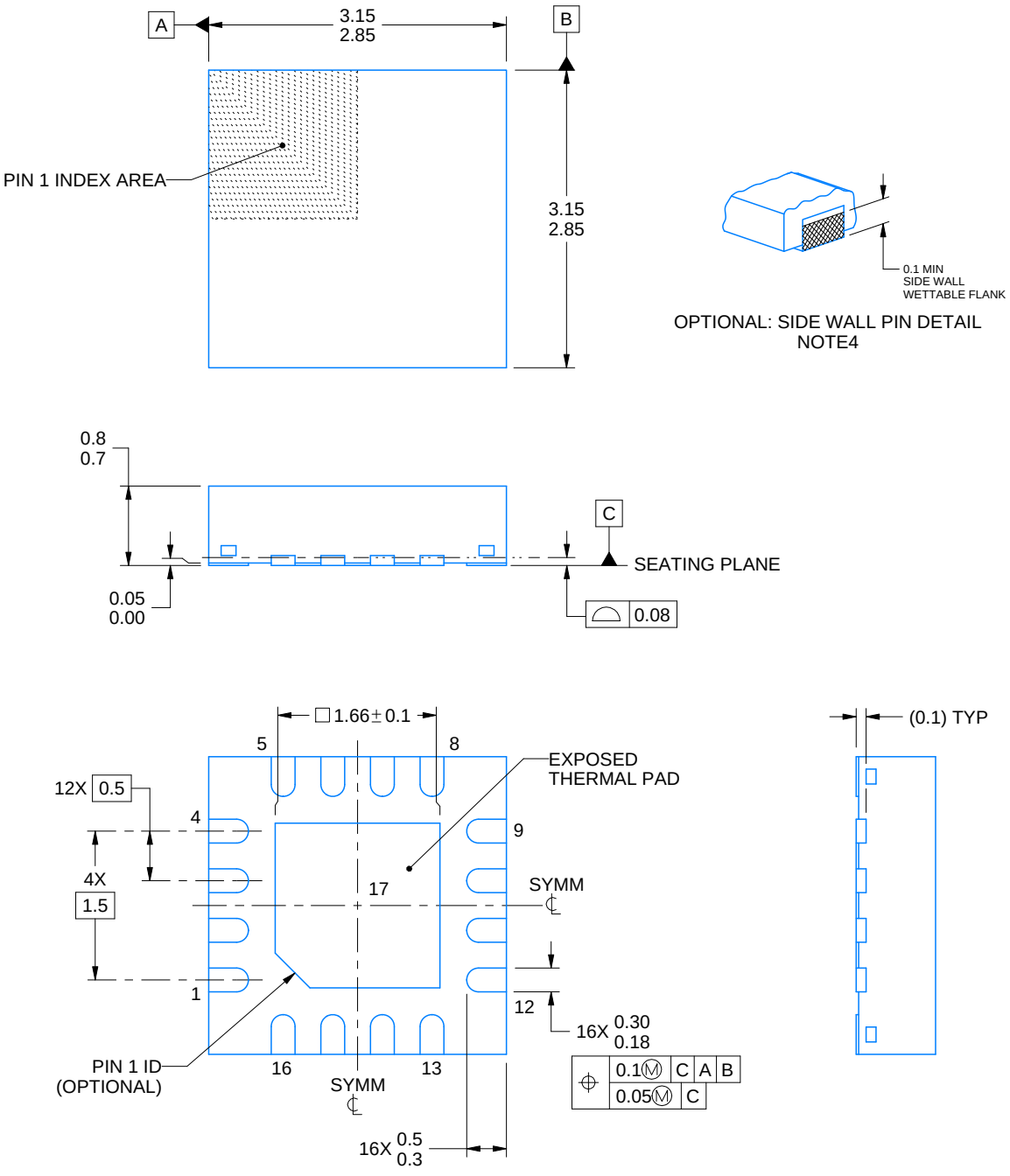
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## RTE0016J

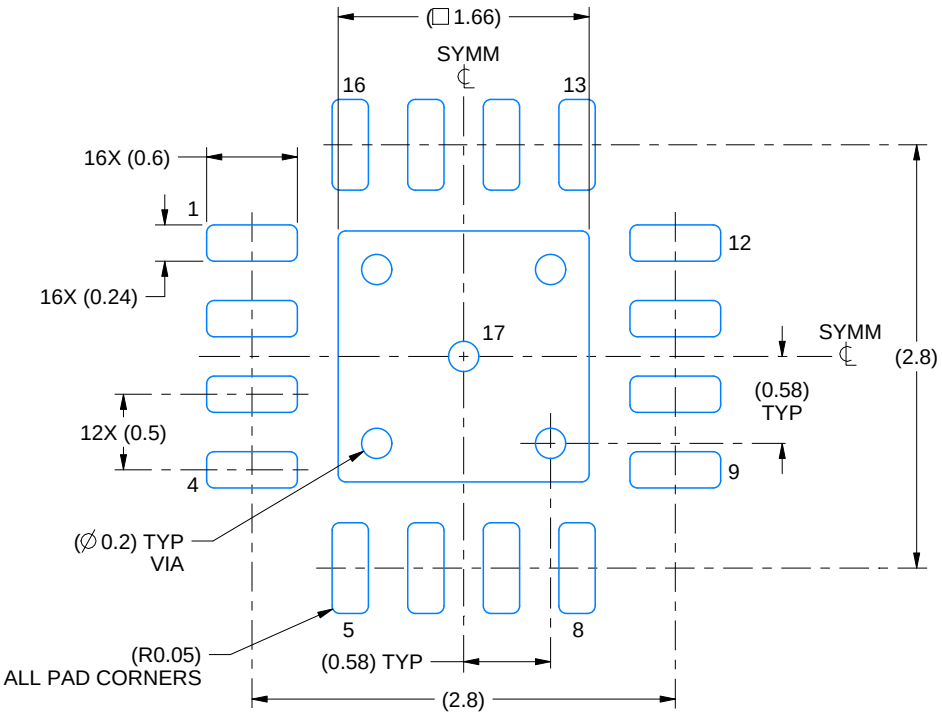
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

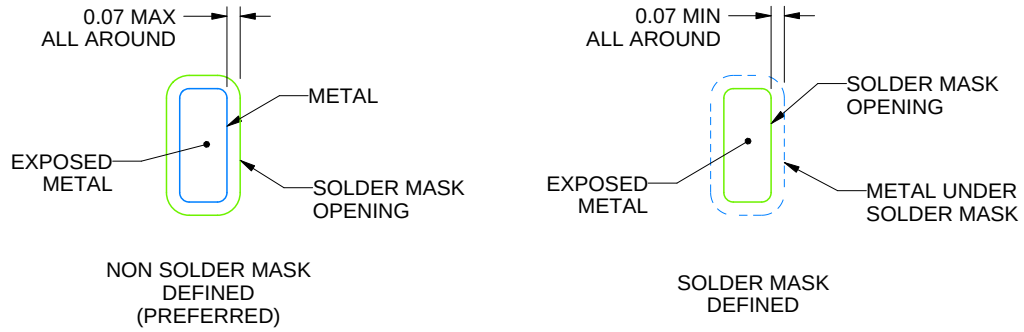



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

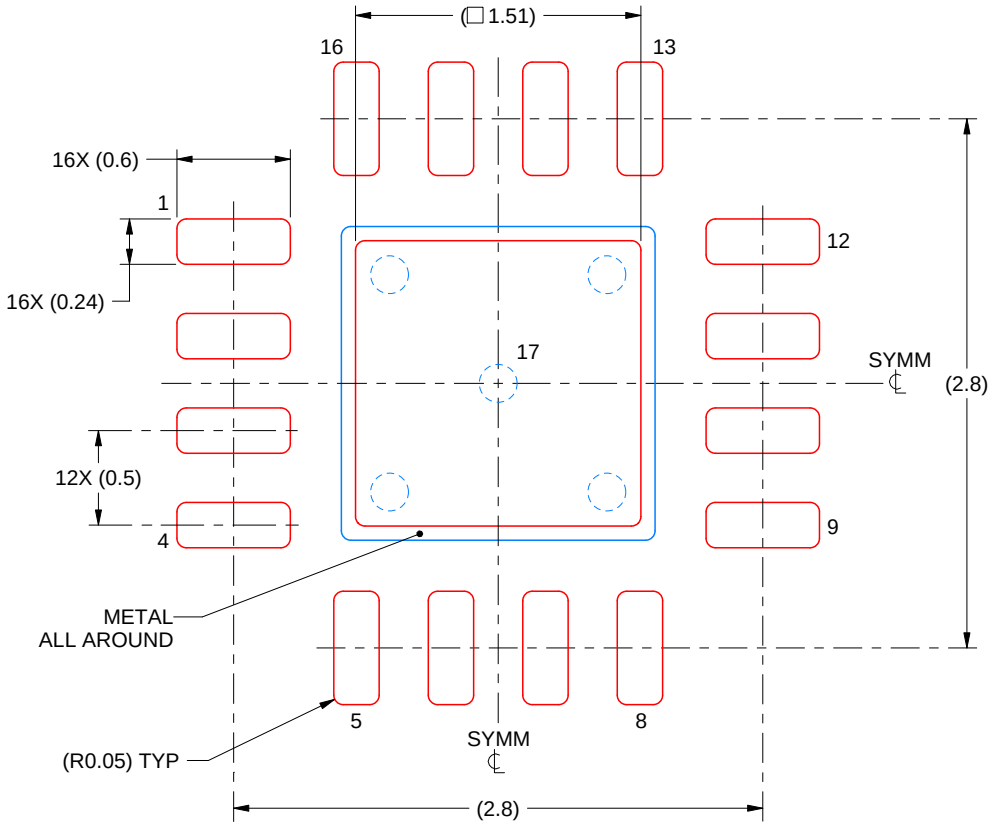



SOLDER MASK DETAILS

4224278/B 06/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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