UCG2883x/4x Self-Biased High Frequency QR Flyback Converter With Integrated GaN

1 Features

- Integrated 750V GaN HEMT
- Dynamic QR/DCM/CCM modes of operation
- High Power density: Up to 500kHz switching frequency
- Enable low BoM cost by integration
  - Remove auxiliary winding with self bias
  - Integrated input and output voltage sensing
  - Integrated current sense
  - Integrated HV start-up
  - Integrated X-cap discharge
- High efficiency and low EMI performance
  - Ultra-low standby power: <30mW
  - Frequency foldback and burst mode
  - Valley locking
  - Frequency dithering
  - Switching slew rate control
- Comprehensive protection features
  - Overtemperature protection
  - Input and output overvoltage protection
  - Short-circuit protection
  - Cycle-by-cycle current limit
  - Two-level over power protection with LPS
  - Brownin and brownout protection
  - Open feedback protection
- Flexible configurability through external resistors
  - X-cap discharge and CCM mode disable
  - Selectable switching slew rate
  - Multiple clamping frequency settings
  - Fault latch or auto-restart
  - Maximum and minimum peak current ratio

2 Applications

- USB-PD adapter for portable electronics
- USB wall outlets and docking stations
- Industrial DIN rail power supplies
- Server aux power supplies

3 Description

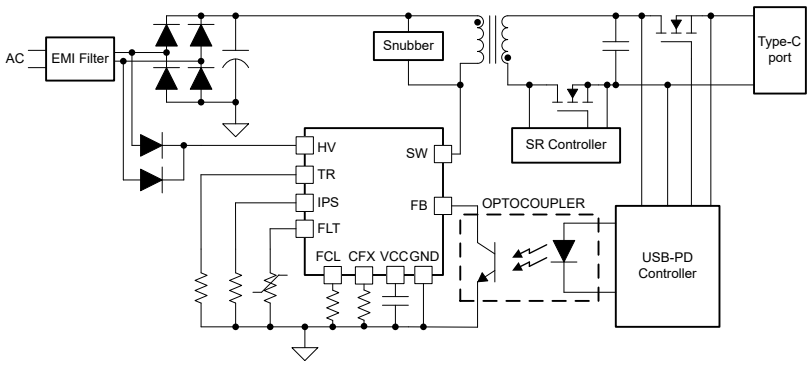
UCG2883x/4x is a high frequency, quasi-resonant flyback converter with a built-in 750V GaN high electron mobility transistor (HEMT) with low $R_{ds(on)}$ for AC to DC power conversion. The UCG2883x/4x is designed for high power density applications, such as cell phone fast chargers and notebook adapters. The key feature of this device is the self-bias and auxless sensing scheme which eliminates the need of the auxiliary winding and simplifies the system design with higher efficiency.

The UCG2883x/4x also features intelligent mode transition (CCM/QR/DCM) to enable high efficiency across a wide power range and <30mW standby power consumption. In addition, UCG2883x/4x includes a full list of protections such as brownin and brownout protection, SCP, OVP, OPP, LPS, OFB, and OTP. The cycle-by-cycle current limit allows for fast response to the fault conditions to safeguard the system and improve the reliability. In a small 5mm × 5mm package, the UCG2883x/4x has dedicated configuration pins to offer more flexibility. Only resistors are needed to tune certain parameters for each system, enabling a platform design with a single device.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCG28836	REZ (QFN, 12)	5mm × 5mm
UCG28846	D (SOIC, 16)	3.9mm × 9.9mm
UCG28838	REZ (QFN, 12)	5mm × 5mm
UCG28844(3)	D (SOIC, 16)	3.9mm × 9.9mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Preview information (not Production Data).



Simplified Schematic of AC/DC Flyback Converter Using UCG2883x/4x

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4 Device Comparison

Table 4-1. Device Comparison

DEVICE NAME	PACKAGE	OUTPUT POWER	TYP. Rdson	MAXIMUM CCM DURATION
UCG28836-1REZR	QFN	65W	170mΩ	Infinite
UCG28838-2REZR	QFN	120W	170mΩ	Infinite
UCG28844-1DR (Preview)	QFN	45W	380mΩ	Infinite
UCG28846-1DR	SOIC	65W	270mΩ	Infinite
UCG28824	QFN	45W	270mΩ	10ms
UCG28826	QFN	65W	170mΩ	10ms
UCG28828	QFN	120W	170mΩ	10ms

Table 4-2. Device Options

	UCG28836-1	UCG28846-1	UCG28838-2	UCG28844-1 (Preview)
Power Level	65W	65W	120W	45W
Rdson	170mΩ	270mΩ	170mΩ	380mΩ
OPPL	100W	Disabled	Disabled	69W
OPPH	140W	140W	190W	97W
LPS	7.5A	7.5A	Disabled	5.2A
OPPL Timer	4.6s	N/A	N/A	4.6s
Brownout/in	80VAC/70VAC	80VAC/70VAC	80VAC/70VAC	80VAC/70VAC
SCP threshold	4.5A	3.8A	4.5A	2.68A
Output OVP	25V	25V	25V	25V
Input OVP	No	No	No	No
High Line CCM	No	No	Yes	No
CCM Depth	70%	70%	50%	70%
EMI Dithering Frequency	390Hz	390Hz	390Hz	390Hz
EMI Dithering Amplitude	±6.25%	±6.25%	±6.25%	±6.25%
Burst mode	three 1st valley pulse	25kHz burst	three 1st valley pulse	three 1st valley pulse
Counting OPP/LPS in CCM	Yes	Yes	No	Yes

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5 Pin Configuration and Functions

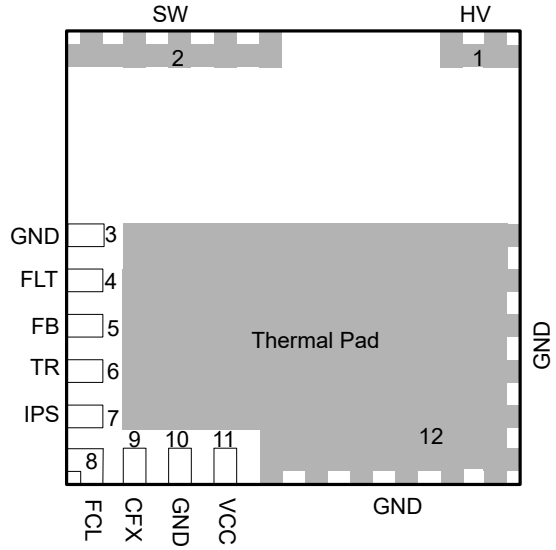


Figure 5-1. UCG2883x/4x 12-Pin QFN (Top View)

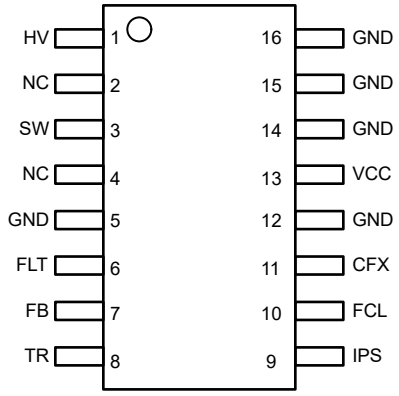


Figure 5-2. UCG2883x/4x16-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	QFN NO.	SOIC NO.		
HV	1	1	P	HV startup, AC line input presence detection and X-cap discharge.
SW	2	3	P	Drain pin of integrated high-voltage GaN HEMT. This is also the sensing pin for valley switching and protections.
GND	3, 10	5, 12	G	Signal ground. Internally connected to power ground.
FLT	4	6	O	Fault pin for external overtemperature protection. Connect an NTC from this pin to GND.
FB	5	7	I	Feedback signal. Connect this pin to the collector of an optocoupler.
TR	6	8	I	Turns ratio setting. A resistor from this pin to GND sets the transformer turns ratio Np/Ns.
IPS	7	9	I	Peak current, and switch node slew rate setting pin. A resistor from this pin to GND sets the maximum and minimum primary-side peak current, and switch node voltage slew rate.
FCL	8	10	I	Switching frequency clamp and fault behavior setting.
CFX	9	11	I	Multifunction pin to enable/disable CCM mode, frequency foldback threshold setting and X-cap discharge enable and disable.

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Table 5-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	QFN NO.	SOIC NO.		
VCC	11	13	P	IC bias supply. Connect an external capacitor (at least 10V rated) from this pin to GND. The capacitor value can be between 15µF to 47µF. The capacitor value is determined by the hold up time for missing input line cycles.
GND	12	14, 15, 16	G	Power ground. Connect to negative terminal of input bulk capacitor. Add a ground plane with sufficient copper area below the thermal pad for efficient heat conduction to the PCB.
NC		2, 4		No connection for high voltage spacing. Do not connect any trace to these pins.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{HV(surge)}$	GaN HEMT drain-source voltage, surge condition			800	V
$V_{SW(tr)(surge)}$	GaN power HEMT transient drain-source voltage, surge condition(2)(4)			800	V
$V_{SW(surge)}$	GaN power HEMT drain-source transient voltage, each switching cycle(3)(4)			750	V
V_{SW}	GaN power HEMT continuous drain-source voltage, FET off			700	V
I_{DS}	GaN power HEMT continuous current, FET on		Internally limited		A
$I_{D(pulse)(oc)}$	Drain (D to S) pulsed current during overcurrent response time			16	A
$I_{S(cnts)}$	Source (S to D) continuous current, FET off			2	A
	Pin voltage	FLT, TR, IPS, FCL, CFX, FB	–0.3	5.5	V
		VCC	–0.3	6.5	
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) One time event with duration limited to <100µs
(3) Damped to VSW(Plateau)=600V in <900ns
(4) See GaN HEMT Switching Capability for more information on the GaN power FET switching capability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_{SW}	SW pin current, continuous	Internally limited			A
V_{VCC}	VCC supply, self-regulating	5.2		6	V
C_{VCC}	Capacitance on VCC pin	15		47	µF
C_{X2}	X2 capacitance	0.1		1	µF
L_{MAG}	Primary magnetizing inductance, UCG28836/46	130		400	µH
L_{LK}	Primary winding leakage inductance			3	%
C_{SW}	SW pin capacitance (GaN HEMT excluded)			300	pF
C_{HV}	HV pin parasitic capacitance		50	100	pF
T_A	Ambient temperature	–40		105	°C
T_J	Junction temperature	–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		UCG28846 D (SOIC) 16 PINS	UCG28836/8 REZ (QFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.9	30.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		7.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.7	1.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	19.3	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY						
$V_{VCCSHORT}$	Threshold for reduced VCC startup current		0.65	0.9	1.2	V
I_{HVLO}	Reduced HV startup current	Before VCC reaches $V_{VCCSHORT}$	0.55	1	1.7	mA
I_{HVHI}	Full HV startup current	After VCC exceeds $V_{VCCSHORT}$	2.2	4	5.66	mA
V_{VCCOFF}	VCC under voltage lock out threshold	Tracking with variation in other thresholds	4.9	5.1	5.3	V
V_{VCC_REG}	VCC regulation voltage and start-up threshold	Tracking with variation in other thresholds	5.6	5.8	6	V
V_{VCC_CHG}	VCC charging trigger threshold	Trigger VCC charging to V_{VCC_REG}	5.4	5.6		V
I_{VCC}	Operating supply current	No switching	500	700	900	µA
$I_{VCCSLEEP}$	Supply current in burst mode	No switching	250	280	325	µA
$I_{VCCFAULT}$	Supply current when a protection is triggered		200	250	300	µA
GAN POWER TRANSISTOR						
R_{DSON}	Drain-source on-resistance	T_J = 25°C, UCG28836/38, I_{DS} =1.5A		170	220	mΩ
R_{DSON}	Drain-source on-resistance	T_J = 25 °C, UCG28846, I_{DS} = 1.5 A		270	351	mΩ
R_{DSON}	Drain-source on-resistance	T_J = 25 °C, UCG28844, I_{DS} = 1.5 A		380	492	mΩ
C_{OSS}	Output capacitance	V_{SW} = 400V, UCG28836/38		40		pF
C_{OSS}	Output capacitance	V_{SW} = 400V, UCG28846		25		pF
C_{OSS}	Output capacitance	V_{SW} = 400V, UCG28844		18		pF
GAN GATE DRIVER						
	Turn-on dV/dt	For SW node, V_{DS} = 325V, Option 2		7		V/ns
	Turn-on dV/dt	For SW node, V_{DS} = 325V, Option 3		5		V/ns
PEAK CURRENT CONTROL						
I_{PKMAX}	Maximum peak current, UCG28844	Option 1	1.84	1.94	2.04	A
I_{PKMAX}	Maximum peak current, UCG28844	Option 2	2.04	2.15	2.25	A
I_{PKMAX}	Maximum peak current, UCG28844	Option 3	2.30	2.42	2.54	A
I_{PKMAX}	Maximum peak current, UCG28836/38/46	Option 1	2.66	2.8	2.94	A
		Option 2	2.95	3.1	3.26	
		Option 3	3.33	3.5	3.68	

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6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PKMAX}/ I_{PKMIN}	Max. to min. peak current ratio	Option 1	3.92	4	4.08	
		Option 2	2.94	3	3.06	
T_{SS}	Soft start time			4		ms
FEEDBACK CONTROL						
R_{FB}	FB pull-up resistor			60		kΩ
V_{FBOPEN}	Open FB Pin voltage		4.5	4.75	5	V
V_{BST_OFF}	Burst-off threshold	Turn-off switching		250		mV
V_{BST_ON}	Burst-on threshold	Resume burst switching		300		mV
V_{BST_EX}	Burst mode exit threshold	Exit to frequency foldback, option 1, VIN=255VDC		583		mV
$f_{MIN,CLAMP}$	Minimum frequency clamp	During normal operation	23	25		kHz
		During soft start		10		
T_{SWMAX}	Maximum time period			40	43	µs
T_{ONMAX}	Maximum on time			30		µs
$f_{MAX,CLAMP}$	Frequency clamp	Option 1		140		kHz
$f_{MAX,CLAMP}$	Frequency clamp	Option 2		100		kHz
$f_{MAX,CLAMP}$	Frequency clamp	Option 3		250		kHz
$f_{MAX,CLAMP}$	Frequency clamp	Option 4		500		kHz
T_{DDCM}	DCM ring fixed timer	From last seen DCM ring valley		3.75		µs
EMI DITHERING						
$f_{carrier}$	Carrier frequency			390		Hz
$I_{Dither,max}$	Carrier amplitude	% of instantaneous peak currents		±6.25		%
PROTECTIONS						
V_{TH_BI}	Brown-in threshold		106	112	118	V
V_{TH_BO}	Brown-out threshold		93	98	103	V
T_{DBO}	Brown-out delay time			60		ms
I_{FLT}	FLT pin source current			75		µA
V_{TH_OTP}	FLT threshold voltage	Triggers external overtemperature fault	0.59	0.6	0.61	V
	I_{FLT} on time			260		µs
	I_{FLT} time period			10		ms
	Number of external TSD cycles	Before fault is triggered		3		
R_{SW}	SW pin impedance		8.2	9.5		MΩ
V_{OVP}	OVP detection threshold	V_{OUT} threshold (1)	23	25	27	V
	Internal overtemperature protection shut down threshold	Temperature increasing		150		°C
	Internal overtemperature protection hysteresis	Temperature reducing		12		°C
T_{RETRY}	Auto-retry time			1		s
V_{OFB}	Open FB protection threshold			3.6		V
P_{OPPH}	Over power protection threshold, UCG28836/46	Triggers after 120ms	125	140	160	W
P_{OPPH}	Over power protection threshold, UCG28838	Triggers after 120ms	169	190	216	W
P_{OPPH}	Over power protection threshold, UCG28844	Triggers after 120ms	87	97.5	111	W

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6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{OPPL}	Over power protection threshold, UCG28836/46	Triggers after 4.6s	89	100	114	W
	Over power protection threshold, UCG28844	Triggers after 4.6s, input referred, recover at 67W	61	69	75	W
I_{LPS}	LPS fault output current threshold, UCG28836/46	Input referred, triggers after 4.6s	6.3	7.5	8.65	A
I_{LPS}	LPS fault output current threshold, UCG28844	Input referred, triggers after 4.6s	4.4	5.2	6	A
I_{SCP}	Short Circuit Protection	Primary current threshold, UCG28844		2.68		A
I_{SCP}	Short Circuit Protection	Primary current threshold, UCG28836/38		4.5		A
I_{SCP}	Short Circuit Protection	Primary current threshold, UCG28846		3.8		A
N_{SCP}	Short Circuit Protection	No. of cycles		3		
t_{SCP}	Short-circuit response time			140		ns
X CAP DISCHARGE						
I_{ACDET}	Line removal detection current	Current sink from HV pin	1.5	2	2.5	mA
I_{XDIS}	X-cap discharge Current		3.8	5	6.2	mA
T_{XDIS}	X-cap discharge Time	C_{XCAP} = 1µF			1	s

(1) Assuming 20V output, and the transformer turns ratio is the same as TR pin programmed

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6.6 Typical Characteristics

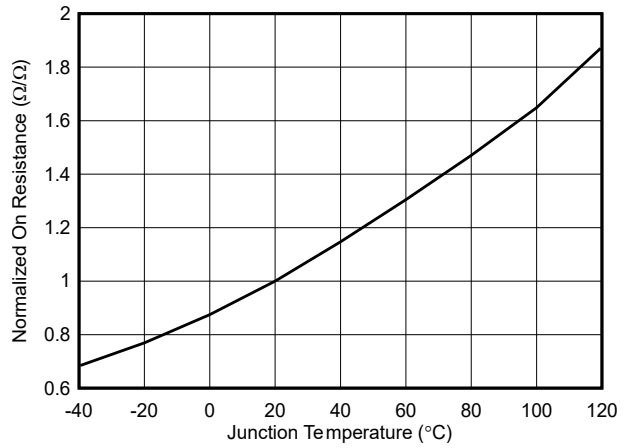


Figure 6-1. Normalized On-Resistance vs Junction Temperature

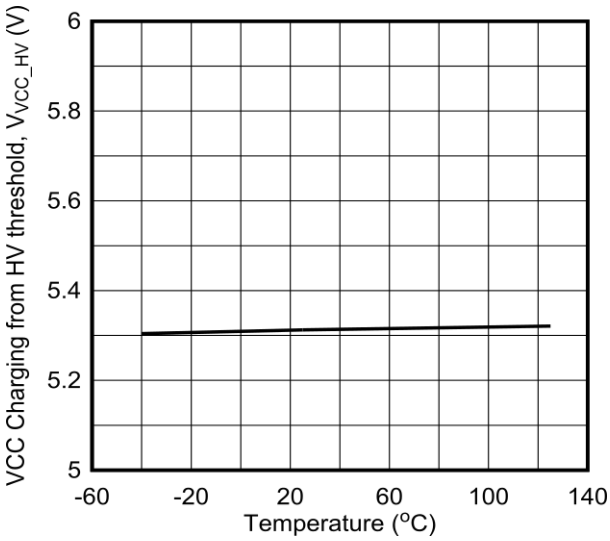


Figure 6-2. VCC Threshold for Charging From HV Pin vs Junction Temperature

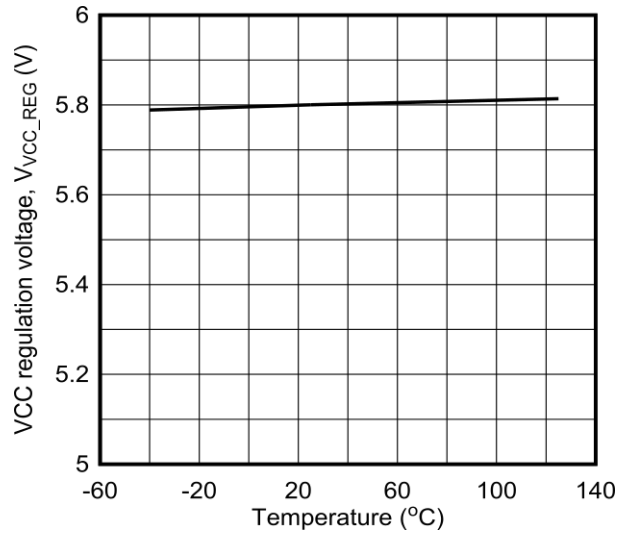


Figure 6-3. VCC Regulation Voltage vs Junction Temperature

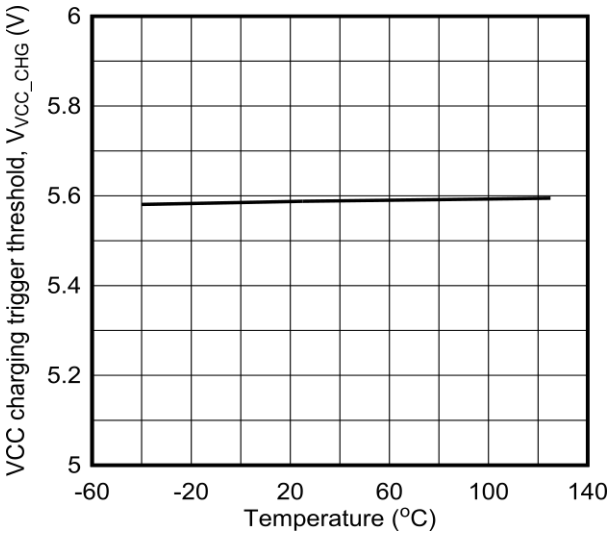
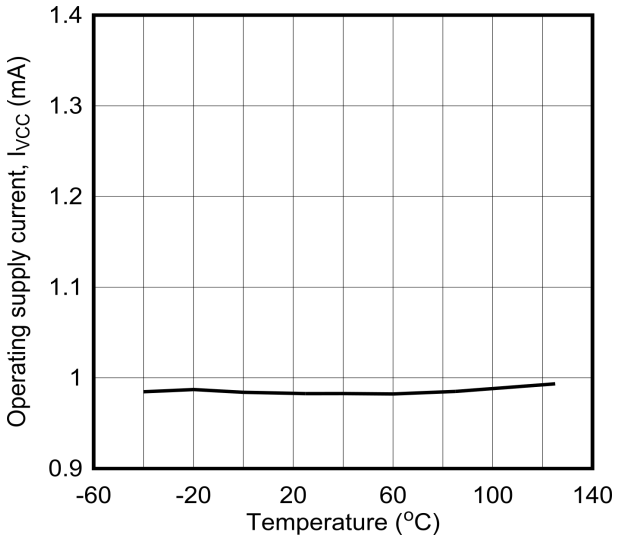


Figure 6-4. VCC Charging Trigger Voltage vs Junction Temperature

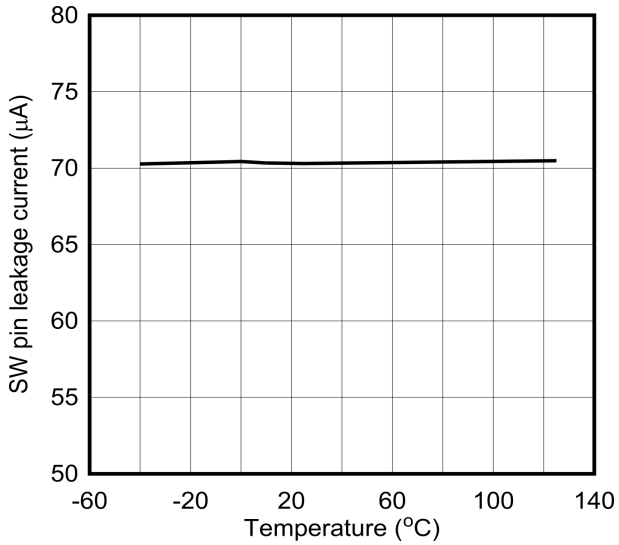
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6.6 Typical Characteristics (continued)



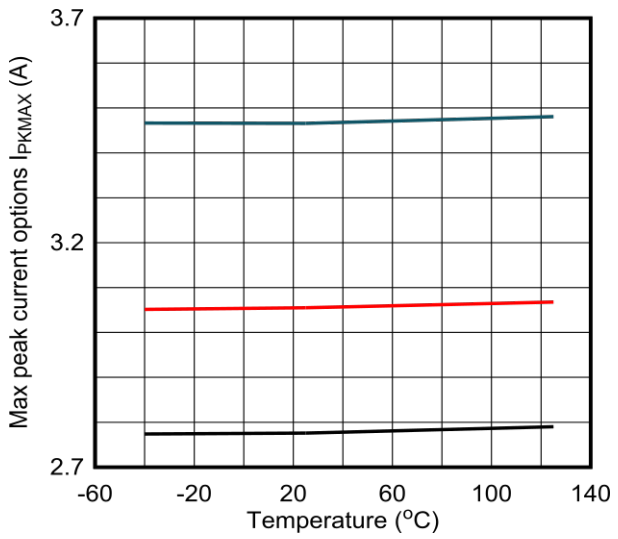
100KHz switching frequency

Figure 6-5. Operating Supply Current vs Junction Temperature



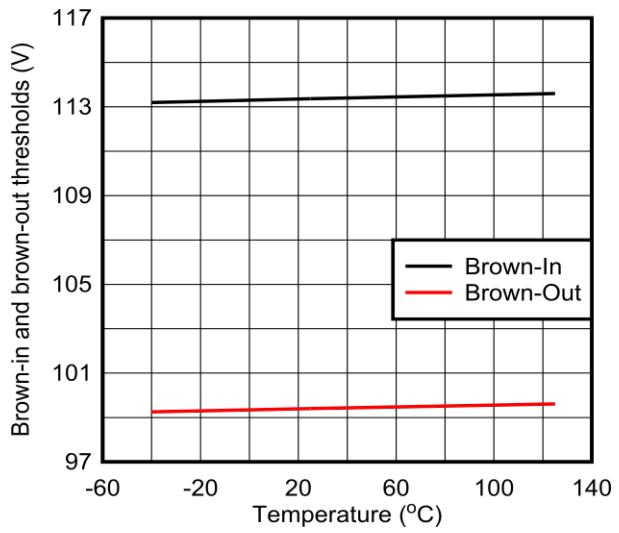
V_{SW} = 650V

Figure 6-6. SW Pin Leakage Current vs Junction Temperature



Peak current options centered around 2.8A, 3.1A and 3.5A

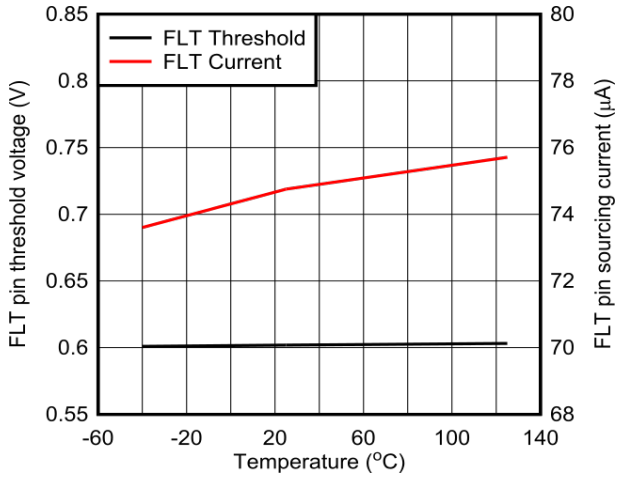
Figure 6-7. Maximum Primary Peak Current vs Junction Temperature



Brown-in and brown-out thresholds centered around 112VDC and 98VDC respectively

Figure 6-8. Brown-in/out Thresholds vs Junction Temperature

6.6 Typical Characteristics (continued)



Voltage and current values centered around 0.6V and 75µA respectively

Figure 6-9. FLT Pin Voltage and Current vs Junction Temperature

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7 Detailed Description

7.1 Overview

The UCG2883x/4x is a high frequency, quasi-resonant (QR) AC/DC flyback converter with integrated 750V primary-side GaN high electron mobility transistor (HEMT), referred to as GaN HEMT, designed for use in AC-to-DC power supplies up to 120W. This device gives benefit of GaN integration to achieve high power density designs with high switching frequency up to 500kHz.

The UCG2883x/4x features the industry's first auxless flyback architecture with self-bias to give a compact and low cost power supply design without the need for an auxiliary winding in the transformer. The self bias feature reduces losses to improve efficiency in wide output voltage applications like USB-PD chargers by eliminating the need for a low dropout regulator (LDO) and the associated losses to generate the device bias.

The UCG2883x/4x supports continuous conduction mode (CCM) operation for transient output power conditions of minimum of two times the nominal output power in low-line input conditions without increase in transformer size, saving space and lowing cost. This device also includes frequency foldback and burst modes for higher efficiency operation during light load and no-load conditions, respectively. The X-cap discharge circuit discharges the X-capacitor in the input EMI filter within less than 1s to prevent the user from an electric shock at the time of unplugging the power supply from the wall socket, meeting different safety standard requirements.

The UCG2883x/4x overcomes the system design limitations of integrated converters by offering resistor programmable options to the user for maximum flexibility to optimize performance at the desired operating point. The device also includes many built-in protections such as output over-voltage protection (OVP), short-circuit protection (SCP), two-level over power protection (OPPH and OPPL) and over-temperature protections (OTP) with auto-restart and latch response for a robust power supply design preventing any damage during such fault conditions.

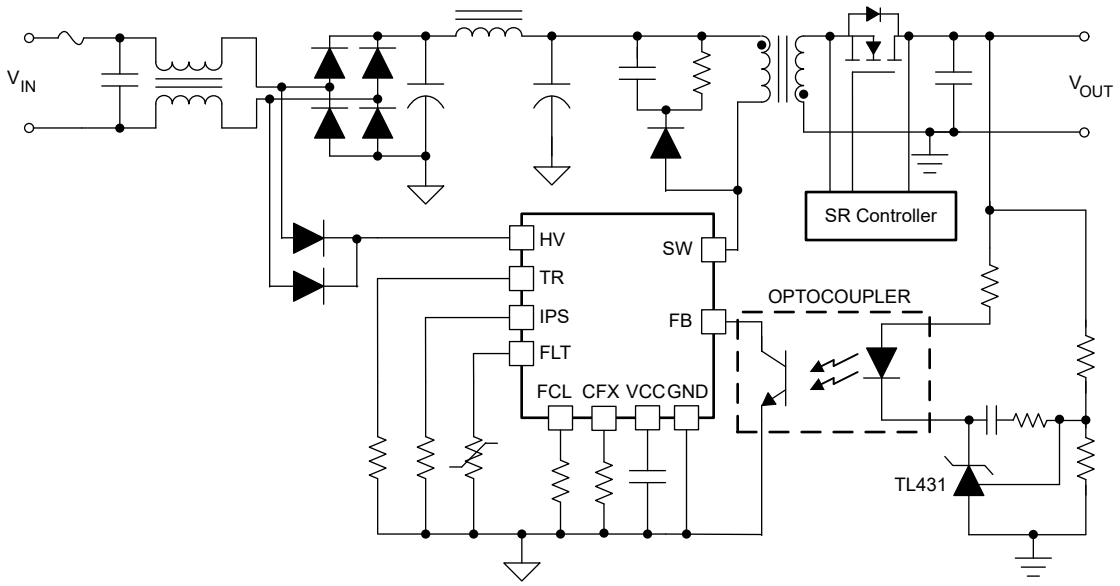
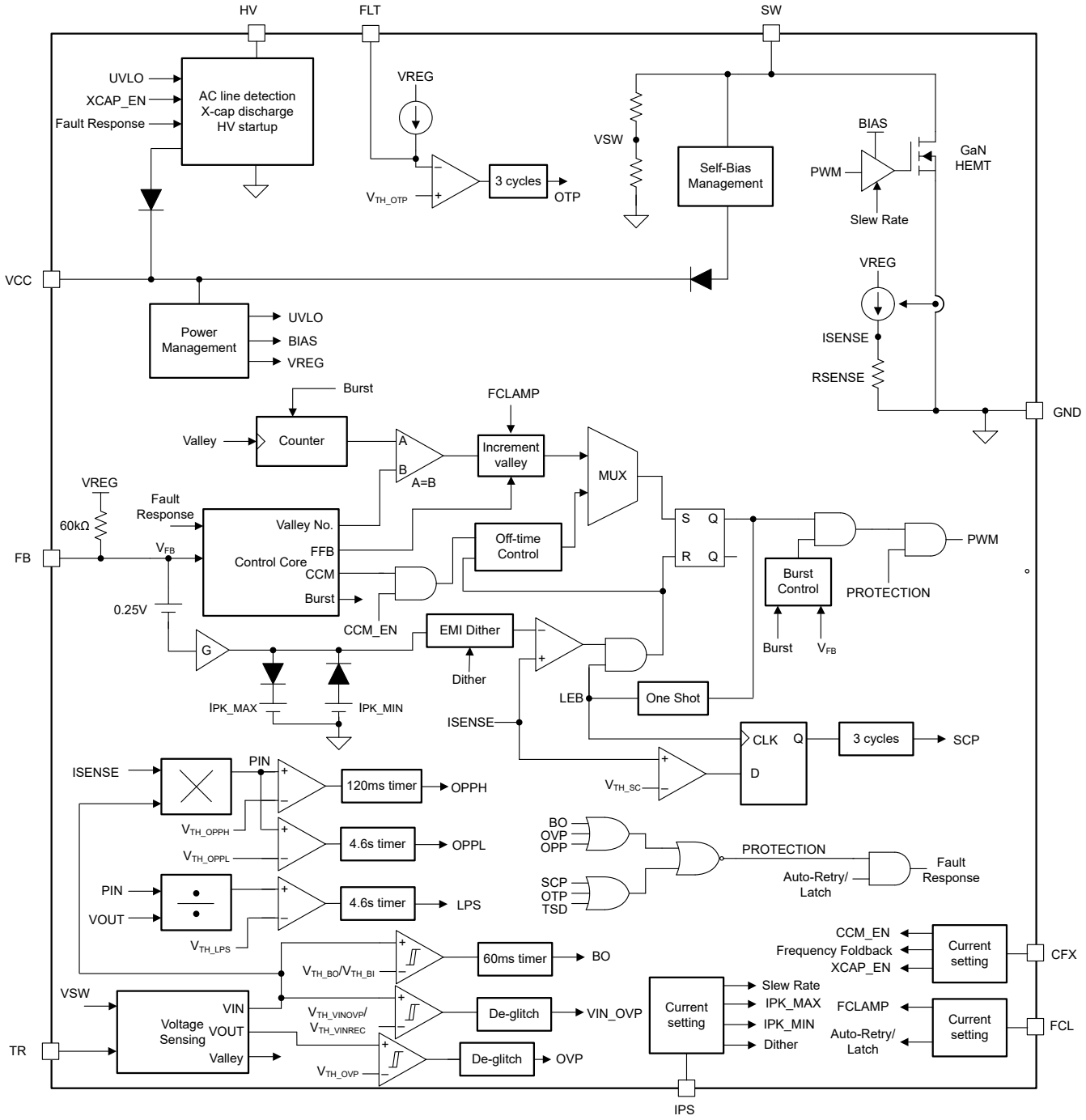


Figure 7-1. AC/DC Flyback Converter Schematic Using UCG2883x/4x

7.2 Functional Block Diagram



7.3 Detailed Pin Descriptions

The UCG2883x/4x is a QR flyback converter with integrated 750V GaN HEMT with self bias and auxless sensing. UCG2883x/4x includes HV, SW and GND pins for interface with the flyback power stage components. Additionally, the device has a bias supply and a feedback pin for secondary side regulation. There are several programmable setting pins for the user to configure the device for an optimized power supply design. These programming pins require a resistor to ground and offer the flexibility to optimize various parameters during power stage design enabling a platform design with a single device. The resistor values on the programming

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pins are detected at the UVLO turn-on event and recorded inside the IC to improves the IC noise immunity. The resistor setting cannot undergo dynamic change during operation.

7.3.1 HV - High Voltage Input

Connect the high voltage (HV) pin to the two ends of the X-capacitor at the line input, through two diodes as shown in Figure 7-1. HV pin charges the bias supply (VCC) capacitor at start-up. The HV pin also discharges the X-capacitor when the input line voltage is removed. When X-cap discharge is not needed, this connection is still required to minimize the standby power consumption. The UCG2883x/4x device charges VCC capacitor through HV pin during standby mode, when the Flyback converter operates in the deep burst mode with long idle period. The charge current can be smoothed out using a resistor (less than 510Ω) in series with the HV pin. When designing for DC input applications, the HV pin can be directly connected to the input bulk capacitor with corresponding resistor setting on the CFX pin to disable the X-cap discharge feature. Due to the lack of line voltage zero crossing, the standby power consumption is slightly increased in DC input applications.

7.3.2 SW - Switch Node

The SW pin is connected to the switch node on the primary side of the flyback converter. SW pin is the drain of the integrated 750V GaN HEMT. SW pin is also the sensing pin for valley switching and OVP, OPP and LPS protections. To keep the switching losses low, minimize the total switch node capacitance at this pin. The capacitance seen at the SW pin includes the transformer parasitic capacitance, GaN HEMT drain-source capacitance, reflected capacitance from secondary side and any additional capacitance which are added to slow down the switch node turn-on and turn-off slew rates.

7.3.3 GND – Ground Return

The GND pin is the external return pin, and provides a reference point for the internal circuitry and the gate drive of the device. This is the return pin for the power stage and must be connected to the negative terminal of the input bulk capacitors. Connect the thermal pad is connected to the GND and verify sufficient copper area around the device to dissipate the heat. Connect pin 10 GND to pin 3 and 12 in the shortest trace possible. VCC bypassing capacitor must return to pin 10.

7.3.4 FLT - External Overtemperature Fault

Connect a negative temperature coefficient (NTC) resistor from this pin to GND for monitoring the temperature of a critical point on the power supply external to the device, and trigger overtemperature protection to avoid damage to components. The device sources 75µA current into the NTC. As the NTC resistance reduces with increase in sensed temperature, the external over-temperature fault is triggered when the voltage on the FLT pin reduces to less than 0.6V. See Section 7.4.10.5 for details of overtemperature protection. Pull the FLT pin low to trigger a fault implemented with external discrete circuits. Other than the FLT pin, the device also includes internal over temperature protection to prevent the device from exceeding the maximum allowable junction temperature.

7.3.5 FB – Feedback

Connect the feedback (FB) pin to the collector of the optocoupler for output regulation. This pin has an internal 60kΩ pull up resistor for optocoupler bias. The instantaneous voltage on this pin determines the switching frequency, peak current and mode of operation (burst, foldback, valley switching or CCM) as per the control law in Figure 7-4 to deliver the required output power. Connect a 100pF or 220pF capacitor from this pin to ground for high frequency noise filtering.

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7.3.6 TR - Turns Ratio

Set the transformer turns ratio information with a resistor from this pin to GND as per values in Table 7-1. The turns ratio information is used for output voltage sensing. The resistor must be 1% accurate.

Table 7-1. Turns Ratio Setting Resistor Values

TR Pin Resistor (kΩ)	Turns Ratio	V_{OUT} OVP Threshold (V, Reflected to Primary)
0	7.875	196.9
5.23	6	150
6.34	6.125	153.1
7.68	6.25	156.2
9.31	6.375	159.4
11.3	6.5	162.5
13.7	6.625	165.6
16.9	6.75	168.7
20.5	6.875	171.9
25.5	7	175
31.6	7.125	178.1
39.2	7.25	181.2
51.1	7.375	184.4
66.5	7.5	187.5
84.5	7.625	190.6
113	7.75	193.7
174	7.875	196.9

The TR pin sets up the transformer turns ratio assuming the design is used for USB-PD application. When used for other applications, the TR pin setting follows different principle. In reality, the TR pin is used to set the output OVP level. The UCG2883x/4x uses the auxless sensing technology and cannot directly tell the output voltage level. The TR pin sets the output OVP level based on the output voltage reflected to the primary side. Basically, in those applications, select the TR pin resistor value based on the V_{OUT} OVP Threshold (V, Reflected to Primary) column in Turns Ratio Setting Resistor Values. Refer to the application note for more details.

7.3.7 IPS - Peak Current, and Slew Rate

This pin offers settings for peak current thresholds, and switch node slew rate. Connect a resistor from this pin to GND as per values in Table 7-2 to select the preferred option for the following specifications:

- Maximum peak current
- Ratio of maximum to minimum peak current
- Switch node slew rate

Table 7-2. IPS Pin Programming Resistor Values

IPS Pin Resistor (kΩ)	Maximum Peak Current (A)	$I_{PK,MAX}/I_{PK,MIN}$	SW Slew Rate (V/ns)
0	3.1	4	5
5.23	2.8	4	7
6.34	3.1	4	7
7.68	3.5	4	7
9.31	2.8	3	7
11.5	3.1	3	7
14.3	3.5	3	7
17.8	2.8	4	5
22.6	3.1	4	5

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Table 7-2. IPS Pin Programming Resistor Values (continued)

IPS Pin Resistor (kΩ)	Maximum Peak Current (A)	$I_{PK,MAX}/I_{PK,MIN}$	SW Slew Rate (V/ns)
28.7	3.5	4	5
36.5	2.8	3	5
51.1	3.1	3	5
75	3.5	3	5

7.3.8 FCL - Frequency Clamp and Fault Response

Use the FCL pin to select the maximum switching frequency clamp value and fault response behavior. Table 7-3 lists the resistor values to be used for the given operating conditions. The resistor must be 1% accurate.

Table 7-3. FCL Pin Programming Resistor Values

FCL Pin Resistor (kΩ)	Frequency Clamp (kHz)	Fault Response
0	140	EXTFLT and Output OVP Latched, rest auto retry
5.23	140	All latched
6.34	100	All latched
7.68	250	All latched
9.31	500	All latched
11.5	140	All auto retry
14.3	100	All auto retry
17.8	250	All auto retry
22.6	500	All auto retry
28.7	140	EXTFLT fault and Output OVP latched, rest auto retry
36.5	100	EXTFLT fault and Output OVP latched, rest auto retry
51.1	250	EXTFLT fault and Output OVP latched, rest auto retry
75	500	EXTFLT fault and Output OVP latched, rest auto retry

7.3.9 CFX - CCM, Frequency Clamp Foldback and X-cap Discharge

Use the CFX pin to enable and disable CCM mode and X-cap discharge. Select the three different frequency clamp foldback modes. Refer to Table 7-4 for values of resistors to connect from this pin to GND for the given operating settings. The resistor must be 1% accurate. The CFX pin is also used for fault reporting for easy debugging during design. Refer to Error Codes for Protections for details. This pin cannot be connected to GND.

Table 7-4. CFX Pin Programming Resistor Values

CFX Pin Resistor (kΩ)	CCM	Frequency foldback setting	X-cap discharge
5.23	Disabled	Option 1	Enabled
6.34	Disabled	Option 2	Enabled
7.68	Disabled	Option 3	Enabled
9.31	Disabled	Option 1	Disabled
11.5	Disabled	Option 2	Disabled
14.3	Disabled	Option 3	Disabled
17.8	Enabled	Option 1	Enabled
22.6	Enabled	Option 2	Enabled
28.7	Enabled	Option 3	Enabled
36.5	Enabled	Option 1	Disabled
51.1	Enabled	Option 2	Disabled
75	Enabled	Option 3	Disabled

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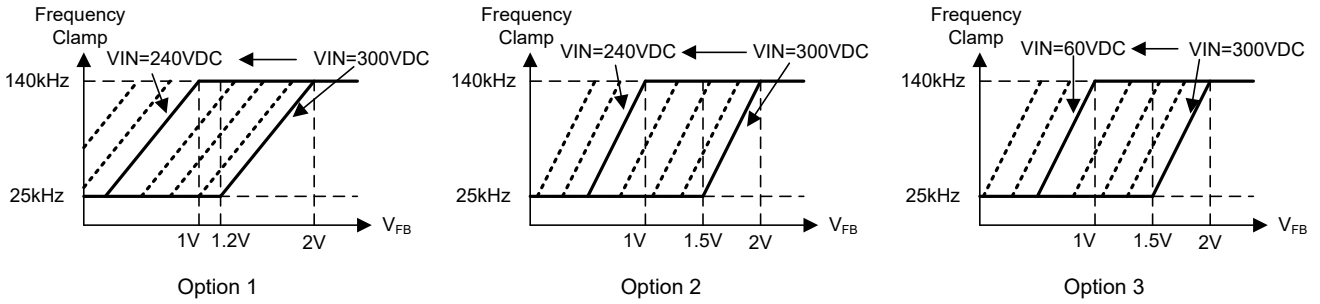


Figure 7-2. Frequency Clamp Foldback Options

These three programming options give power supply designers the control of the frequency clamp foldback at different input voltage conditions. This frequency clamp foldback gives additional switching frequency reduction on top of the control law demanded switching frequency. This further reduces the switching frequency and improves the light load efficiency, especially at high input voltages. The maximum clamp frequency is programmed by FCL pin resistor. The CFX pin resistor then programs how fast the clamp frequency folds back from the maximum value to the minimum value. Frequency Clamp Foldback Options shows that the foldback trajectory is proportional to the input voltage.

7.3.10 VCC - Input Bias

The VCC pin provides the bias to the device, powering the internal references, gate driver, regulators, control circuits and protection features. Use a minimum of 10µF capacitance from this pin to GND for maintaining VCC voltage regulation with self-bias feature. Use of an additional 10nF ceramic capacitor in parallel is recommended for low ESR and minimum overshoot and undershoot on this pin. Use 30µF capacitance at this pin for holdup without reset in the event of two missing line cycles at the input.

7.4 Feature Description

7.4.1 Self Bias and Auxless Sensing

The UCG2883x/4x includes self bias and auxless sensing to eliminate the transformer auxiliary winding. Removing the auxiliary winding and associated components makes the system design simpler, smaller and cheaper .

The self bias feature is especially useful in applications like USB-PD chargers with wide output voltage range. Typically in wide output voltage range designs, the aux winding generates device supply voltage (VCC) greater than the UVLO threshold at the minimum V_{OUT} which is 3.3V. In such case, the voltage on aux winding increases six times when V_{OUT} = 20V which needs an internal or external power conversion stage to reduce the voltage to VCC range, increasing external components and reducing efficiency. The UCG2883x/4x's self bias eliminates the need for the additional power conversion stage at the VCC pin thus reducing the number of components and recovering power losses. The self bias circuit is designed to keep VCC higher than the UVLO threshold throughout the range of operation of the device, given the components around the device are used within the range recommended in the datasheet. Auxless sensing circuits are connected to the SW pin. The device senses the voltage on SW for valley sensing and various protections. The input bulk capacitor voltage and output voltage are derived from the SW pin voltage.

7.4.2 Control Law

The UCG2883x/4x is a peak current mode control QR flyback converter. The converter starts by turning on the primary-side integrated GaN HEMT. The current in the transformer primary side winding I_{PRI} increases with a slope dependent on V_{IN} and primary magnetizing inductance L_M and equals V_{IN}/L_M. Once I_{PRI} reaches the peak value $I_{PK,PRI}$, the GaN HEMT turns off. By flyback action, the secondary winding voltage increases and turns on the synchronous rectifier (SR) FET body diode to clamp to output voltage V_{OUT}. During this time, the secondary winding current reduces from secondary peak current $I_{PK,SEC}$ with a slope V_{OUT}/L_S, where L_S is the secondary winding inductance. The switch node voltage is equal to the sum of V_{IN} and primary to secondary turns ratio N

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times V_{OUT}, called the plateau voltage. Once the secondary current reduces to zero, L_M and total switch node capacitance C_{SW} begin to resonate to cause magnetizing ring. The UCG28826 turns on the primary GaN HEMT at a valley in this magnetizing ring to reduce the turn-on switching losses.

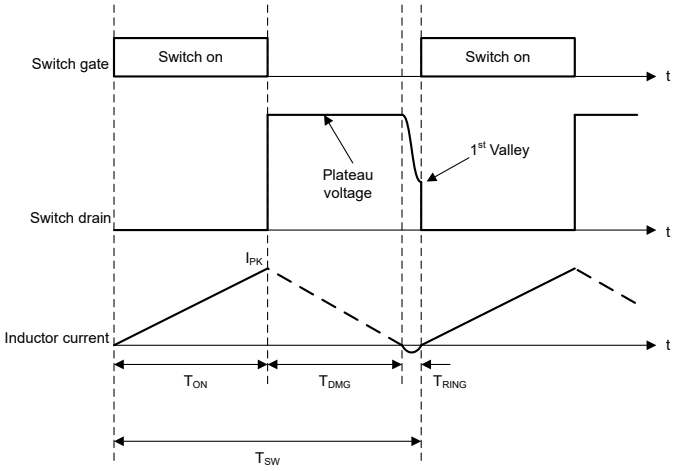


Figure 7-3. Flyback Converter Waveforms

Hence, in UCG2883x/4x, in every switching cycle, the primary GaN HEMT turns off after reaching the peak current threshold and turns on next at a target valley in magnetizing ring during discontinuous mode (DCM) operation. The instantaneous primary peak current and target valley is determined by the feedback (FB) pin voltage as per the control law of Figure 7-4. Connect the FB pin to the optocoupler collector. The negative feedback loop sets FB pin voltage to the required value to support a certain V_{OUT} and P_{OUT} on the output. The device can operate in one of the four modes of operation: burst, frequency foldback, valley switching or continuous conduction mode, as described later.

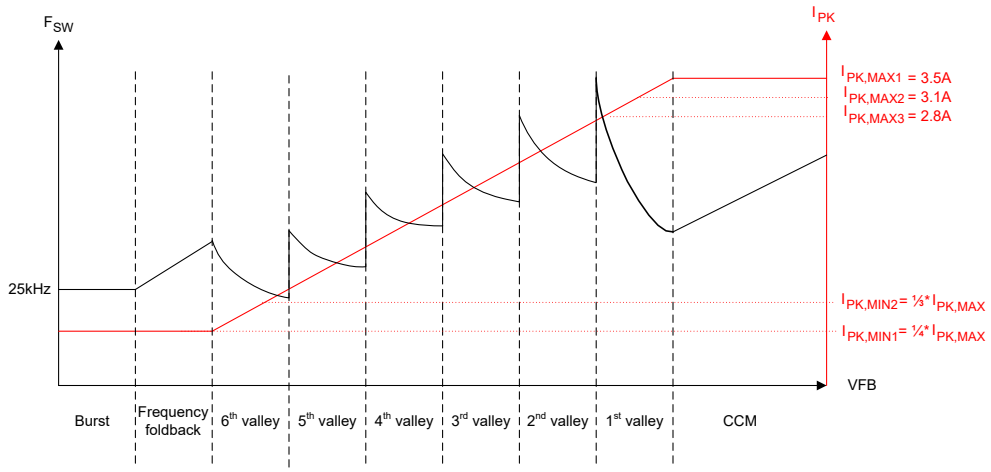


Figure 7-4. UCG2883x/4x Control Law

In the control law shown in Figure 7-4, the UCG2883x/4x offers flexibility to select a max peak current $I_{PK,MAX}$ to optimize for the switching frequency at rated load and transformer size. For each $I_{PK,MAX}$ setting, a scaling ratio of 1/3rd or 1/4th is available for the minimum peak current $I_{PK,MIN}$. This $I_{PK,MIN}$ value determines the switching frequency and losses in light load conditions when the flyback converter is operating in frequency foldback or burst modes. For all values of $I_{PK,MAX}$ and $I_{PK,MIN}$, the slope of control law peak current vs feedback voltage remains the same, as per Equation 1. Table 7-5 shows the threshold voltages for transition between different modes and between valleys for different peak current settings of Table 7-2.

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Table 7-5. FB Pin Voltage Thresholds for Various Peak Current Settings

	PARAMETER	TEST CONDITIONS	$I_{PK,MAX}$=2.8A	$I_{PK,MAX}$=3.1A	$I_{PK,MAX}$=3.5A	UNIT
V_{FBOPEN}	Open FB pin voltage		3.3	3.45	3.65	V
$V_{THCCMto1}$	CCM to 1st valley threshold	VFB decreasing	2.18	2.4	2.65	
V_{TH12}	1st to 2nd valley threshold		1.09	1.19	1.31	
V_{TH23}	2nd to 3rd valley threshold		0.97	1.05	1.16	
V_{TH34}	3rd to 4th valley threshold		0.91	0.98	1.08	
V_{TH45}	4th to 5th valley threshold		0.85	0.92	1.0	
V_{TH56}	5th to 6th valley threshold		0.79	0.85	0.93	
V_{TH65}	6th to 5th valley threshold	VFB increasing	1.16	1.25	1.38	
V_{TH54}	5th to 4th valley threshold		1.22	1.32	1.46	
V_{TH43}	4th to 3rd valley threshold		1.28	1.39	1.53	
V_{TH32}	3rd to 2nd valley threshold		1.34	1.45	1.61	
V_{TH21}	2nd to 1st valley threshold		1.46	1.59	1.76	
$V_{TH1toCCM}$	1st valley to CCM threshold		2.18	2.4	2.65	
V_{THFF}	6th valley to frequency foldback threshold	$I_{PK,MIN}$=1/4x $I_{PK,MAX}$	0.73	0.78	0.85	
		$I_{PK,MIN}$=1/3x $I_{PK,MAX}$	0.89	0.96	1.05	

7.4.2.1 Valley Switching

The UCG2883x/4x is designed to operate with soft switching and primary FET turn-on at a valley to reduce switching losses. The converter operates in valley switching except during peak load transients during which control can transition to CCM mode (if enabled using CFX pin). During valley switching mode, the target valley and peak current threshold are governed by the control law of Figure 7-4 and Equation 1:

$$I_{PK} = 1.45 \times (V_{FB} - 0.25) \quad (1)$$

During valley switching, with increasing output power, the peak current threshold continues to increase linearly as per above equation. The switching frequency also varies based on I_{PK} and valley targets corresponding to the instantaneous FB pin voltage. When output power is increasing from light loads to rated power, the control transitions from the 6th valley till the 1st valley with corresponding linear increase in I_{PK} threshold. As output power continues to increase further to take FB voltage to the edge of the 1st valley operation, the converter transitions into CCM mode operation with I_{PK} clamped to the maximum value $I_{PK,MAX}$ and increase in switching frequency F_{SW} with further increase in output load. This clamp on $I_{PK,MAX}$ limits the transformer size in a high density power supply design. See Section 7.4.2.4 for details of CCM mode of operation. If output power reduces while operating in the 6th valley, the control transitions to frequency foldback mode to operate at higher valleys and lower frequency to reduce switching losses further.

The FB pin voltage thresholds for valley transitions include a hysteresis and vary depending on increasing or decreasing P_{OUT} to enable valley locking and prevent any audible noise due to hopping between valleys. Refer to the Electrical Characteristics table for FB pin voltage thresholds which determine the mode of operation for UCG2883x/4x. For zero optocoupler collector current with large P_{OUT}, the FB pin is pulled up to V_{FBOPEN} through a 60kΩ resistor.

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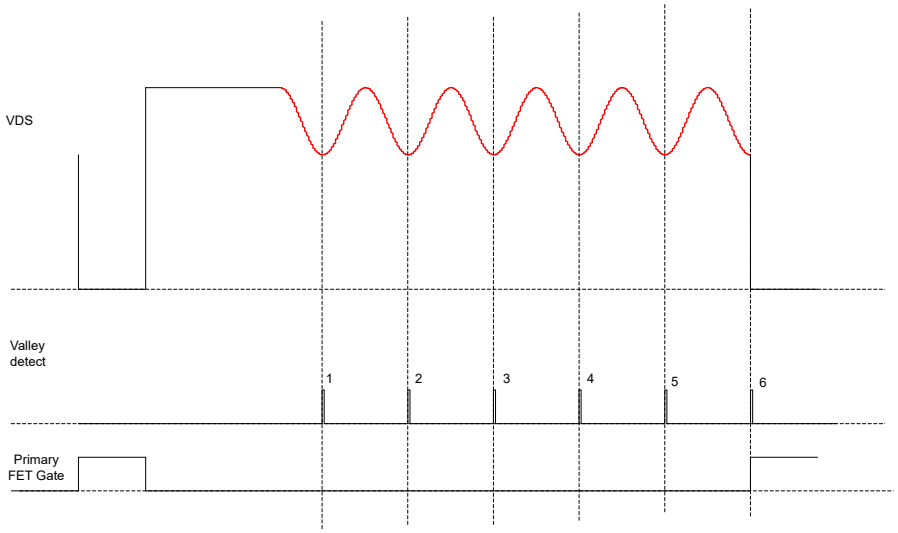


Figure 7-5. Valley Counter With Continuous Valley Occurrence

Typically, the control counts the valleys and turns on the primary GaN HEMT once the target valley is reached, shown in Figure 7-5. For the case when SW node waveform is damped so the valleys disappear before reaching the target valley, a DCM ring fixed timer of 3.75µs starts to continue counting valleys and turn on the primary GaN HEMT once the valley target is reached, shown in Figure 7-6. During start-up (soft start) when V_{OUT} is small, if the valleys do not appear, the controller turns on the primary GaN HEMT after 100µs from last turn on, to switch at 10kHz (the minimum frequency clamp during soft start) for initial few cycles to avoid latch up condition.

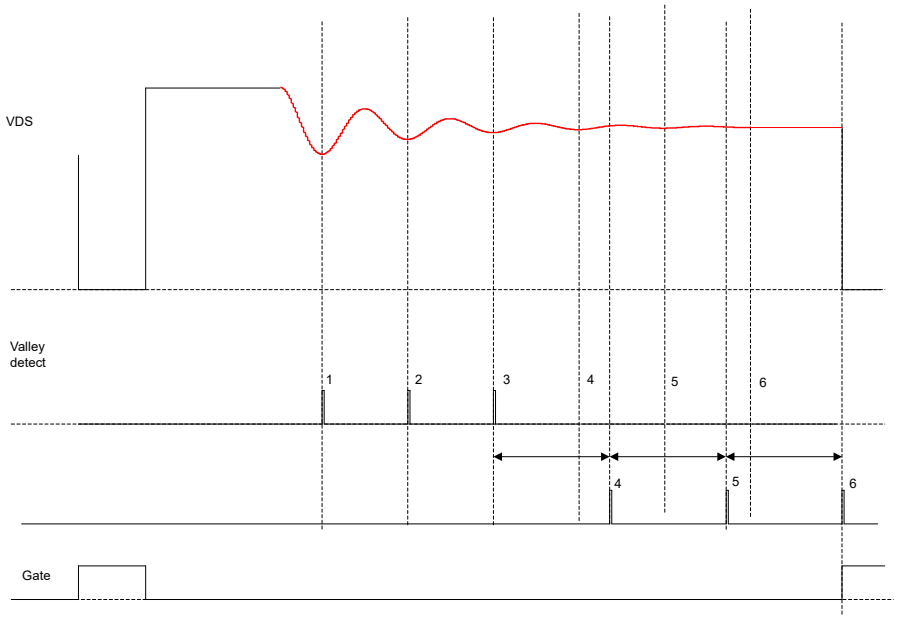


Figure 7-6. Valley Counter With Missing Valleys

The UCG2883x/4x supports infinite CCM operation duration. Because of higher loss in the CCM operation, thermal design of the converter needs to be considered to avoid overheating of the system. At all times during operation of UCG2883x/4x, the maximum switching frequency can be limited with a frequency clamp setting programmable with a resistor from FCL pin to GND, as detailed in Section 7.3.8.

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7.4.2.2 Frequency Foldback

If output power reduces while operating in 6th valley to reduce FB pin voltage below V_{THFF}, the converter transitions to frequency foldback mode and abandons valley switching. The peak current threshold is clamped to $I_{PK,MIN}$ and converter operates at higher valleys after 6th valley, depending on FB pin voltage which causes the switching frequency to reduce further with increase in target valley number, until switching frequency reduces to and is clamped at 25kHz. The minimum switching frequency is clamped to 25kHz to prevent any audible noise, with a total switching cycle time of 40µs. Further reduction in output power takes the converter to burst mode to reduce unnecessary switching losses from periodic switching and achieve very low standby power consumption.

7.4.2.3 Burst Mode

If output power continues to reduce while in frequency foldback mode, the device enters burst mode when FB pin voltages reaches 0.25V for the first time and the device stops switching. Depending on the output power, once FB pin voltage recovers to 0.3V is when device resumes switching in burst mode.

The burst mode of the UCG2883x/4x offers three 1st valley QR switching cycles followed by a minimum 70µs delay before the start of next burst packet. Valley switching reduces switching losses while the delay limits power delivery in burst mode and device transitions to other modes of operation at higher power to maintain high efficiency in the range of output power. In burst mode, frequency clamp is fixed at 250kHz and the primary GaN HEMT turns on at next valley after the expiration of the clamp timer. With burst mode operation, switching losses are kept low with valley switching with limit on electromagnetic emissions with minimum peak current to pass emission standards. Burst mode switching waveforms are shown in Figure 7-7.

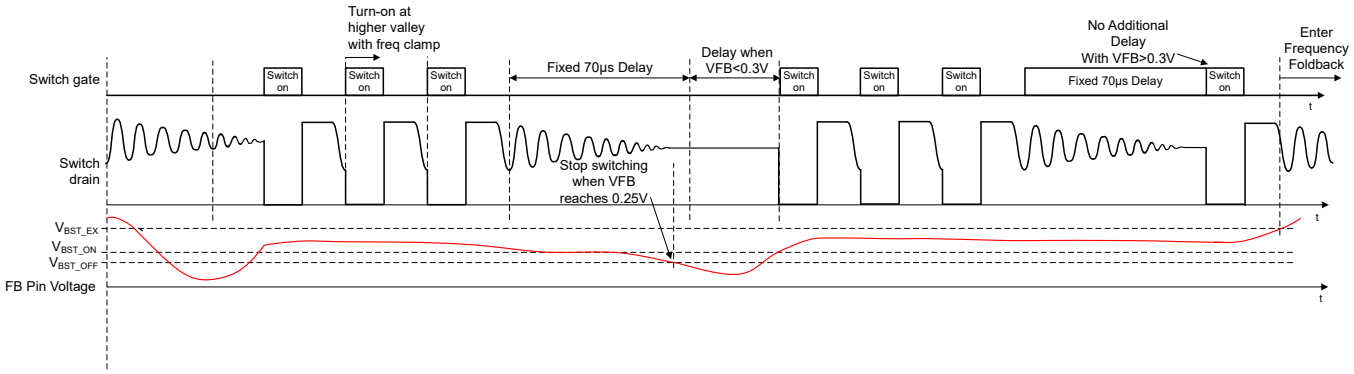


Figure 7-7. Burst Mode Entry and Exit Waveforms

In certain applications, there is a concern that three first valley switching can slightly increase the output voltage ripple during burst mode. in UCG28846, the traditional burst mode is implemented. During burst on time, the converter switching frequency is kept at 25kHz. The burst turn-on and turn-off thresholds are the same.

7.4.2.4 Continuous Conduction Mode (CCM)

As shown in Figure 7-4, once the boundary of 1st valley QR operation is reached with increasing output power, the control clamps I_{PK} to the maximum selected value $I_{PK,MAX}$, and begins to reduce the secondary conduction time T_{OFF} in CCM mode. This reduction in T_{OFF} is proportional to increase in FB pin voltage, until 30% of the QR mode off-time to reach maximum 1.7× the QR mode output power delivery capability. Use a primary side magnetizing inductance L_M large enough to not hit the frequency clamp during CCM mode and avoid any subharmonic oscillations which can increase output voltage ripple, depending on application requirements. In CCM mode, the clamping frequency for the switching frequency clamp is doubled to maximize the peak power capability. For long duration output power transients, the converter returns to 1st valley QR mode after expiry of the 10ms CCM timer for 4 switching cycles of QR mode operation and resumes CCM operation. This operation repeats every 10ms, until the power becomes lower so that the CCM operation is no longer needed. The device offers flexibility to enable or disable CCM mode operation with a resistor from the CFX pin to GND as per values in Table 7-4.

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7.4.3 GaN HEMT Switching Capability

The UCG2883x/4x primary-side integrated GaN HEMT switching capability is explained with the help of Figure 7-8. The figure shows the drain-source voltage (same as SW pin voltage) for the UCG2883x/4x for two distinct switching cycles in a flyback application. The first switching cycle is a normal switching cycle followed by a surge switching cycle in DCM/valley switching condition.

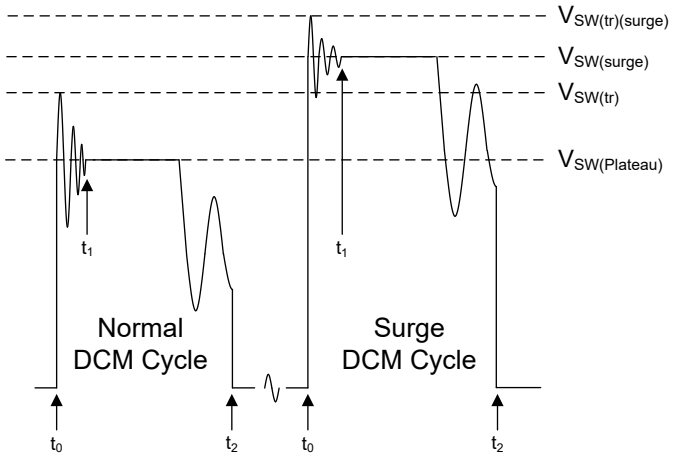


Figure 7-8. GaN HEMT Switching Capability

Each cycle starts before t_0 with the GaN HEMT in on state. At t_0, the GaN HEMT turns off and the parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing has damped out by t_1. Between t_1 and t_2, the HEMT drain-source is at a flat plateau voltage with reducing secondary winding current in a flyback design. At t_2, the GaN HEMT turns on at a valley. During normal operation, the device can safely operates up to 750V leakage transient voltage ($V_{SW(tr)}$) in every switching cycle. For rare surge events, the transient ring voltage is limited to 800V and the plateau is limited to 750V.

7.4.4 Soft Start

When turned on, a flyback converter starts with 0V output voltage. The low voltage can cause the feedback voltage FB to clamp to the maximum value and trigger overload protections. To prevent the clamping from happening, the UCG2883x/4x starts in soft start mode. As Figure 7-9 shows, during this time, an internal FB voltage ramp increases in eight steps from 0V to the maximum value in 4ms. The maximum value of internal FB ramp is equivalent of 80% of the $I_{PK,MAX}$ setting and changes for different resistor settings on the IPS pin. During soft start, the smaller of this internal ramp voltage and actual FB pin voltage is used to determine the device operating point in the control law of Figure 7-4. Once the internal FB ramp voltage reaches the maximum value at the end of 4ms is when control is transferred to FB pin voltage for output regulation. Soft start sequence is executed every time at start up or when recovering from fault (auto-retry or latch) and brown-out conditions. The minimum frequency clamp is changed to 10kHz only during soft start (which is otherwise at 25kHz during normal operation). The 10kHz minimum frequency clamp helps at start-up when valleys are missing and the control law forces turn-on of primary GaN HEMT every 100µs from the last turn-on edge (if valleys are missing), to charge the output capacitor.

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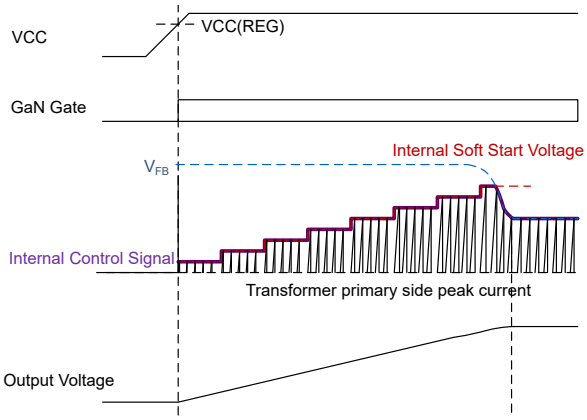


Figure 7-9. Soft Start Sequence

7.4.5 Frequency Clamp

The UCG2883x/4x includes frequency clamp to limit the maximum switching frequency. Frequency clamps are useful during design optimizations to pass emissions standards and reduce switching losses by limiting the switching frequency to a certain value. The device offers four maximum frequency clamp settings at 100kHz, 140kHz, 250kHz and 500kHz which are selected with a resistor from FCL pin to ground as per values in Table 7-3. There are no condition where the switching frequency exceeds the chosen value of clamp frequency, except in burst mode when then clamp frequency is set to 250kHz. The minimum switching frequency is also clamped to a fixed 25kHz to prevent switching in the audible frequency range and noise from the flyback converter. Low switching frequency can occur during operation in higher valleys or frequency foldback mode.

Figure 7-10 illustrates example waveforms that demonstrates the operation of the frequency clamp. In this case, the valley target based on the FB pin voltage is at the 2nd valley. After the secondary winding current reduces to zero, the VDS voltage on SW pin begins to resonate and valleys are counted by the valley detection block. The primary-side GaN HEMT does not turn-on at the 2nd valley because the frequency clamp timer is still counting. Only after the expiration of the frequency clamp timer that the primary GaN HEMT turns-on at the next valley, which is the 3rd valley in this case. Based on this logic, the turn-on of the primary GaN HEMT happens only at the next valley post expiration of the frequency clamp timer.

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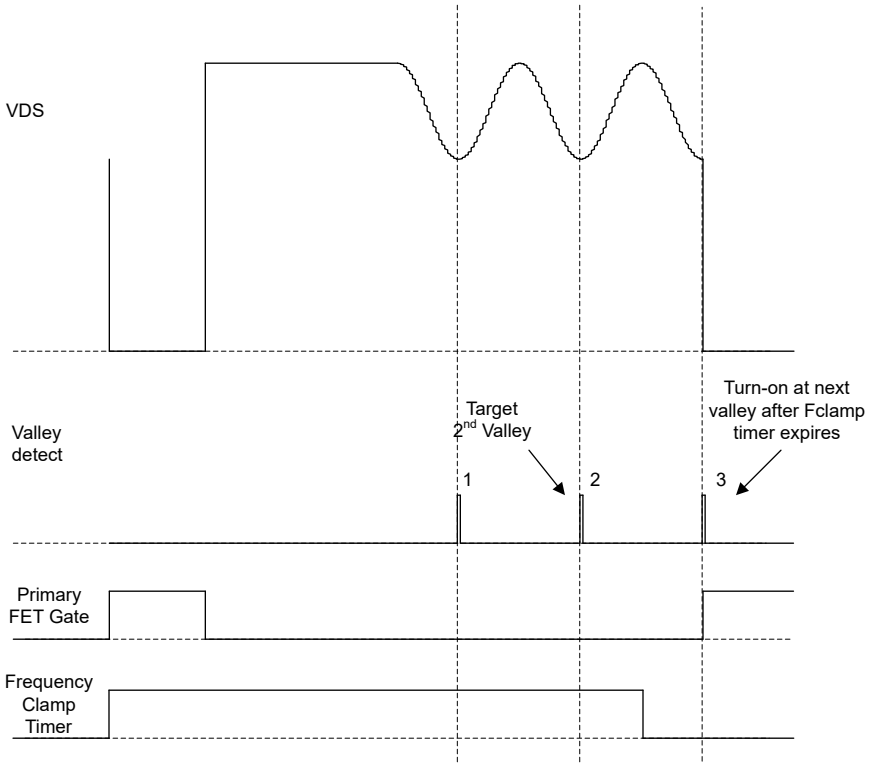


Figure 7-10. Primary GaN HEMT Turn-on Delay Due to Frequency Clamp

7.4.6 Frequency Dithering

The UCG2883x/4x includes frequency dithering to spread the energy in the spectrum around the switching frequency to reduce electromagnetic emissions, making qualifying for various emissions standards easier. Since this device uses peak current mode control to turn-off the primary GAN HEMT and there is no fixed clock signal to set the switching frequency, the dithering in frequency is achieved with small change to the value of peak current threshold in every switching cycle, changing the peak current, and thus the on-time, off-time and switching frequency, in every cycle. The per cent change to peak current threshold varies based on a fixed 6.25kHz or 390Hz (depending on the part number) triangular carrier signal with 32 steps alternating in sign at every transition from minimum (0%) to maximum value (called dithering depth, ±6.25%) in every carrier cycle. The alternating sign of dither perturbation at each step and the low frequency output pole of flyback converter topology averages the cycle-to-cycle power delivery, causing small impact in output ripple due to dithering. The dither perturbation to peak current is asynchronous with the switching frequency and the instantaneous change in peak current is calculated based on the dithering signal during the primary GAN HEMT turn-on time.

Figure 7-11 shows the dithering carrier and peak current perturbation waveforms to dither the switching frequency.

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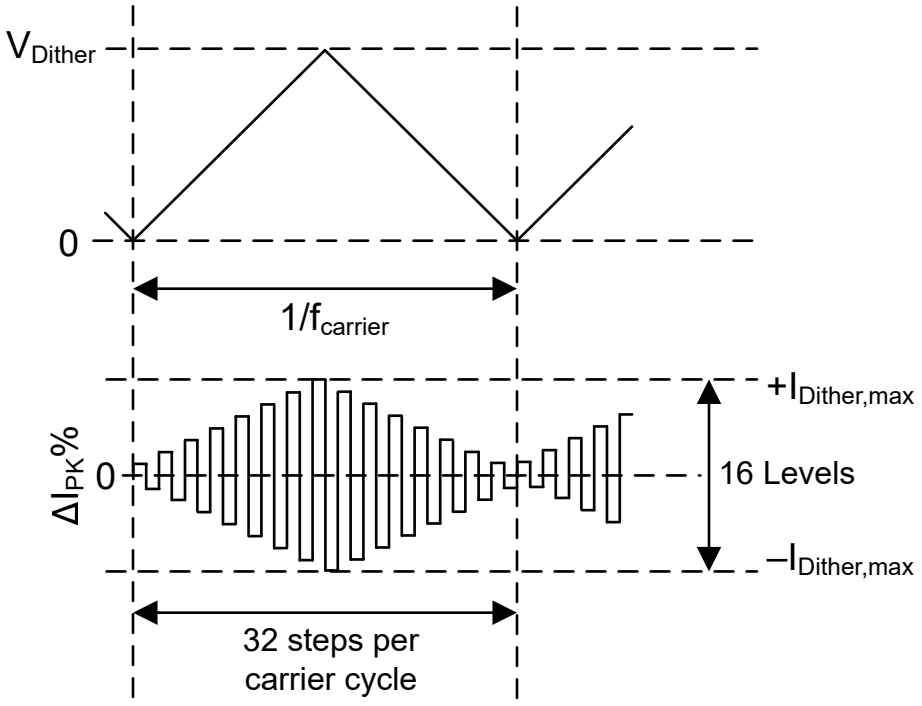


Figure 7-11. Frequency Dithering to Reduce Emissions

7.4.7 Slew Rate Control

The UCG2883x/4x includes slew rate options for drain voltage reduction from switch node valley voltage to ground at the time of primary GaN HEMT turn-on. This GaN HEMT turn-on during valley switching happens at nearly zero current and incurs negligible additional losses with the slower turn-on due to slew rate control helping to meet various electromagnetic emission standards. Three slew rate options are available at 5V/ns, and 7V/ns, which vary marginally based on the valley voltage, as shown in Figure 7-12.

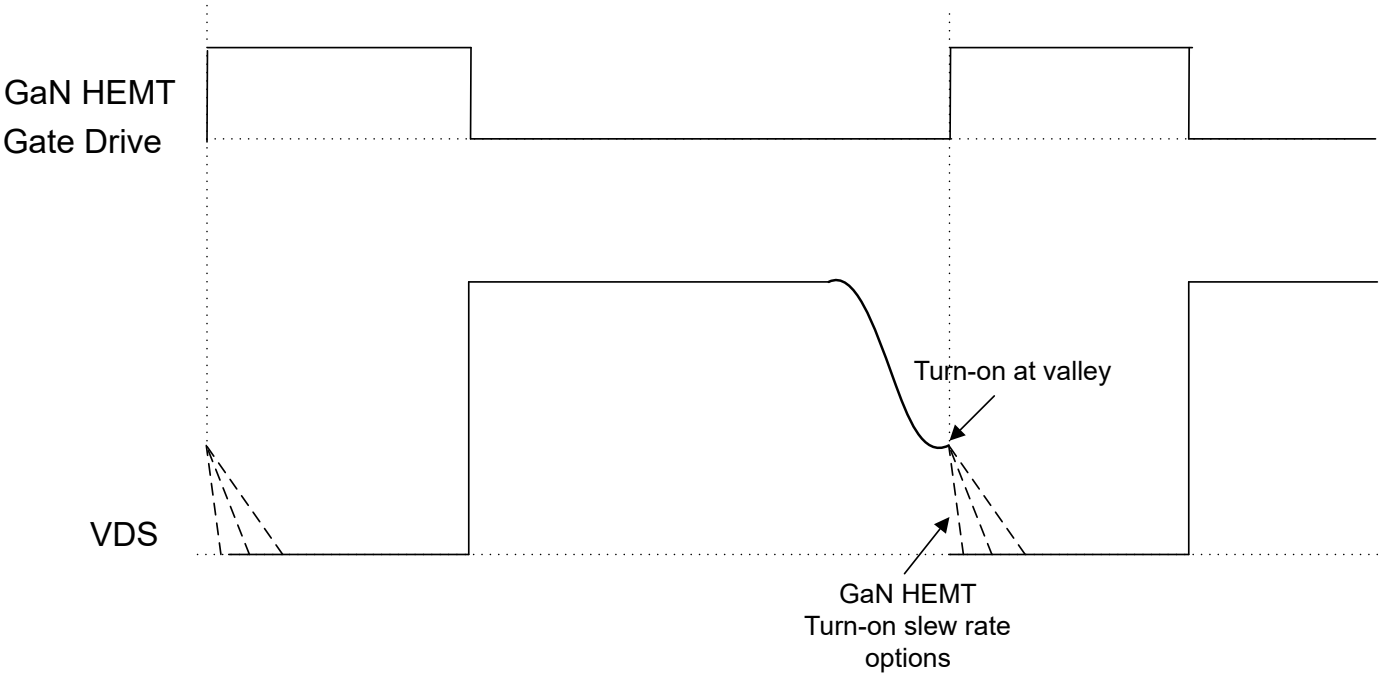


Figure 7-12. GaN HEMT Turn-on Slew Rate Control

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Select the required slew rate value using a resistor from IPS pin to GND as per values in Table 7-2. At the primary GaN HEMT turn-off instant, the increase in SW node voltage depends on I_{PK} and total switch node capacitance C_{SW}. A gate drive current controlled reduction in this turn-off slew rate can increase losses significantly. If a reduction in GaN HEMT turn-off slew rate is needed, add an additional capacitor from GaN HEMT drain (switch node) to GND to reduce the rate of increase in switch node voltage at this turn-off instant.

7.4.8 Transient Peak Power Capability

The UCG2883x/4x supports minimum of two times of transient peak output power capability for applications which require bursts of high power for short durations of time. The peak power is achieved without the need for over sizing the various components such as the transformer, power FETs, and so forth, and the same flyback design is usable for minimum of two times of the continuous output power rating for short durations. With this, a 65W flyback converter designed with UCG2883x/4x can deliver a minimum of 130W transient peak output power for a maximum of 120ms duration limited by the OPPH timer.

At high line input, the transient peak power delivery happens in DCM/QR modes of operation and is limited to maximum 120ms duration as per OPPH protection, as described in Section 7.4.10.4. At low line input, due to limitations in power delivery from DCM/QR modes, the continuous conduction mode (CCM) extends the operation to minimum two times of the nominal power rating. To limit the converter from excessive output power delivery at high line input, the CCM mode is disabled for input bulk capacitor voltage higher than 200V DC. The CCM at high line in some part numbers is enabled to provide more peak power capability at high input voltage. The CCM mode of operation is described in Section 7.4.2.4. Peak power delivery in DCM/QR modes at higher than 140W for longer than 120ms triggers OPPH fault, as detailed in Section 7.4.10.4. A minimum of 2 times transient output power is supported, while maximum instantaneous transient output power in DCM/QR/CCM modes depends on the input bulk capacitor voltage and the power stage component values and is limited in time by the respective OPPH, and OPPL timers.

7.4.9 X-Cap Discharge

Offline AC/DC power supplies use EMI filters with X-capacitors (X-cap) at the input. The UCG2883x/4x includes an internal X-cap discharge circuit to completely discharge the X-cap and protect the user from an electric shock at the time of unplugging the power supply from mains input, as required by regulatory standards.

As shown in Figure 7-1, the X-cap is connected to the device HV pin through two diodes. No resistor is needed in the x-cap discharge path. When the input line voltage is removed from the flyback converter, the X-cap is discharged with a current sink at the HV pin. The device establishes discharge of X-cap within <1s for line frequencies in the range from 45Hz to 66Hz for X-cap values up to 1µF.

7.4.10 Fault Protections

The UCG2883x/4x offers different fault protections which can be programmed for auto-retry or latched response using an appropriate resistor on the FCL pin, as per values in FCL Pin Programming Resistor Values. In auto-retry response, once a protection is triggered, switching stops for 1s duration and normal operation resumes thereafter, as shown in Figure 7-13. When latched response is used, on triggering a protection, the device waits for the supply voltage, V_{CC} to reduce below $V_{VCC(OFF)}$ followed by recovery to greater than $V_{VCC(REG)}$ to resume switching and normal operation, as shown in Figure 7-14.

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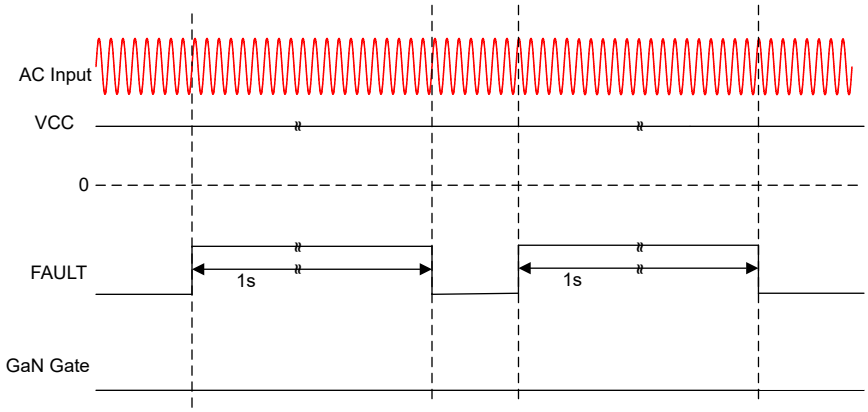


Figure 7-13. Auto-Retry Fault Response

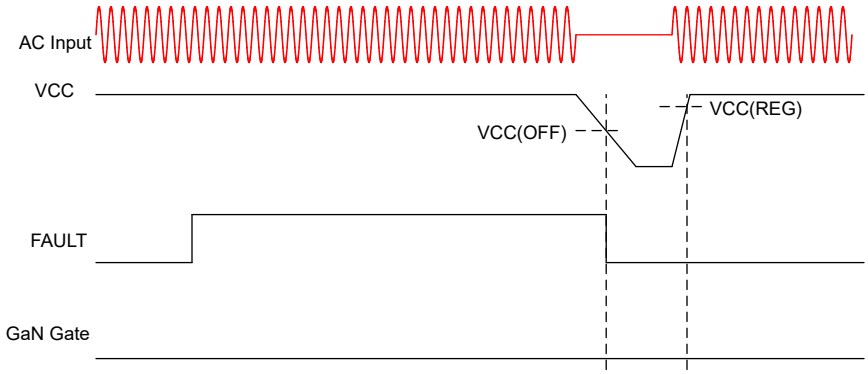


Figure 7-14. Latched Fault Response

7.4.10.1 Brownout Protection

The device stops switching and enters brownout protection if input bulk capacitor voltage V_{BULK} reduces and stays below 98V (DC, or 70V (AC) input) for longer than 60ms duration. This 60ms counter is reset if V_{BULK} exceeds 100V (DC) anytime before the counter expiration. Brownout protection avoids large primary side currents and resultant conduction losses during irregular line input conditions. During low line input conditions, V_{BULK} can reduce below 98V (DC) in every line cycle with large P_{OUT}. However, since V_{BULK} recovers to greater than 100V (DC) in every line half cycle, the counter is reset, thereby avoiding brown-out fault from triggering and normal switching and power transfer continue. Once brownout protection is triggered, the device auto-restarts after a 1s delay if V_{BULK} recovers to greater than 112V (DC, or 80V AC input) followed by soft start sequence to normal operation.

7.4.10.2 Short-Circuit Protection

The UCG2883x/4x includes an overcurrent protection circuit to detect and prevent damage during overload conditions. The overcurrent condition can occur during short-circuit of transformer windings, SR FET drain-source terminals or the flyback converter output. The device detects primary currents exceeding I_{SCP} (4.5A is typical) immediately after primary GaN HEMT turn-on and expiration of the leading edge blanking (LEB) time for SW node capacitance discharge to GND. If short-circuit current threshold is triggered for three consecutive cycles, a short-circuit fault is declared and switching stops. The short-circuit protection response, auto-retry or latch, is selected according to the resistor on the FCL pin.

7.4.10.3 Output Overvoltage Protection

The device monitors output voltage from the SW pin. If V_{OUT} exceeds 25V, an overvoltage protection (OVP) is triggered and switching stops. This protection prevents from damage to the output capacitors in an output overvoltage event, and hence this is a latched fault. Use the right TR pin resistor value to avoid mistriggering this protection. For a fixed output voltage design, use a transformer with primary-to-secondary turns ratio to match

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the output reflected voltage with the case of 20V output and the TR pin setting, to allow the output overvoltage protection still triggers at 25% higher value from the nominal V_{OUT}.

7.4.10.4 Overpower Protection (OPP, LPS)

The limited power source (LPS) regulatory standards require the flyback converter output current to not exceed 8A and the output power to not 100W after 5s. The UCG28836/46 triggers over power protection (low, OPPL) for input power greater than P_{OPPL} or output current (input referred) larger than I_{LPS} for longer than 4.6s duration, to prevent from excessive power delivery to the output in fault conditions. The device also supports transient load requirements of minimum 2 times of the nominal output power rating (130W for 65W design) for up to 120ms beyond which over power protection (high, OPPH) is triggered.

In the UCG28838, the OPPL and LPS protections are disabled and OPPH protection threshold is extended to 190W.

When designing for the output voltage other than 20V, same as the OVP protection, the LPS current level needs to be calculated based on the reflected output voltage on the transformer primary side. The controller assumes the output voltage is 20V, based on the TR pin setting. The LPS current level I_{LPS} is calculated as Equation 2.

$$I_{LPS} = \frac{P_{REF}}{V_{REFLECT}} \times N_{PS_{SETTING}} \quad (2)$$

When the transformer real turns ratio is different than the TR pin setting, due to the output voltage is not 20V, the real LPS current level is calculated using Equation 3.

$$I_{LPS_{REAL}} = \frac{P_{REF}}{V_{REFLECT}} \times N_{PS_{REAL}} \quad (3)$$

Combing Equation 2 and Equation 3, the real LPS current can be calculated as Equation 4.

$$I_{LPS_{REAL}} = \frac{N_{PS_{REAL}}}{N_{PS_{SETTING}}} \times I_{LPS} \quad (4)$$

7.4.10.5 Overtemperature Protection

The UCG2883x/4x offers overtemperature protection to prevent system operation at excessively high temperatures and limit the components from exceeding maximum ambient temperature ratings. The device has separate internal overtemperature protection to limit the die temperature and an external overtemperature protection to monitor and limit the system temperature using a resistor with negative temperature coefficient (NTC). The internal overtemperature fault triggers when die temperature exceeds 150℃ and switching stops. The device recovers to normal operation and switching resumes when the die temperature reduces below 140℃. The internal overtemperature protection is an auto-retry fault.

For the external overtemperature fault, connect the NTC between the FLT and AGND pins. To check for the external overtemperature fault, a 75μA current is sourced from the FLT pin through the external resistor to ground. This current is sourced for a 250μs on-time during every 10ms time period. An up-down counter increments every time when V_{FLT} is lower than 0.6V (typically) with the sourced current. This counter decrements when V_{FLT} is higher than 0.6V (typically) during the 250μs duration. An external overtemperature fault is declared at a count of three. If the FLT is pulled below 0.66V (typically) during initial startup, the device is in overtemperature protection mode and does not start up.

7.4.10.6 Open FB Protection

The UCG2883x/4x monitors for an open FB pin condition to prevent from excessive power from being delivered to the output when then FB pin voltage clamped to the maximum value. The open FB condition can occur with a faulty or open-circuited optocoupler or even large power (greater than the flyback converter's rated power) drawn for long time durations. Open FB protection is asserted when FB pin voltage exceeds the open FB threshold V_{OFB} for >120ms.

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7.4.10.7 Error Codes for Protections

When the device enters fault mode after triggering one or more protections, an error code is sent on the CFX pin. The error code tells about the protection which is triggered, enables quick debugs during the power supply design process and faster time to market for the users. Figure 7-15 shows the error codes sent on the CFX pin for each of the protections. When a protection is triggered, the corresponding error code is sent three times on the CFX pin. Additionally, a pin configure error code is generated when UCG2883x/4x detects a configure pin is open, or a non-valid resistor is connected to the configure pin, or internal CRC error in memory occurs. If multiple protections are triggered, the output code includes multiple 1s (logic high) corresponding to the protections triggered.

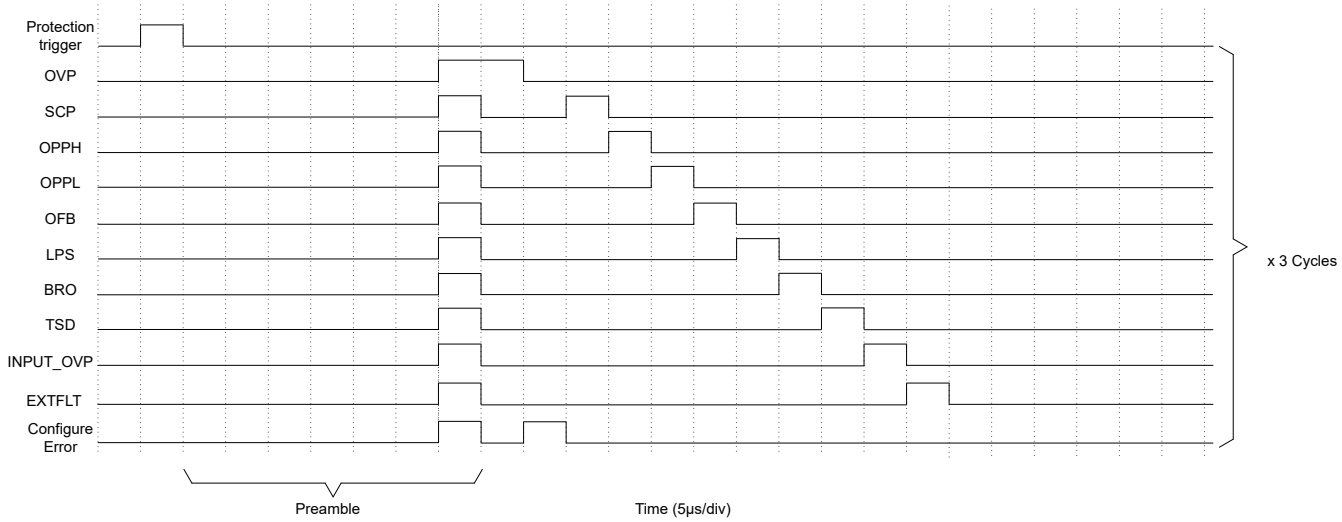


Figure 7-15. Error Codes on CFX Pin for Various Protections

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCG2883x/4x is a 65W AC/DC flyback converter with integrated 750V GaN HEMT and secondary side output voltage regulation using optocoupler. The device offers self-bias and auxless sensing to eliminate the need for transformer auxiliary winding to give a simpler and lower cost design. The UCG2883x/4x with the integrated GaN HEMT is capable of switching up to 500kHz switching frequency to realize a small form factor and high power density flyback design.

8.2 Typical Application

The UCG2883x/4x supports 65W AC/DC flyback designs which is useful for cellphone and notebook chargers, USB wall outlets, industrial power rails and server aux power supplies, amongst other applications. The integrated GaN HEMT and auxless sensing simplify the flyback design to connect only key power stage components and the programming resistors to configure the design for the target application. Table 8-1 lists the design requirements for a typical 65W notebook charger.

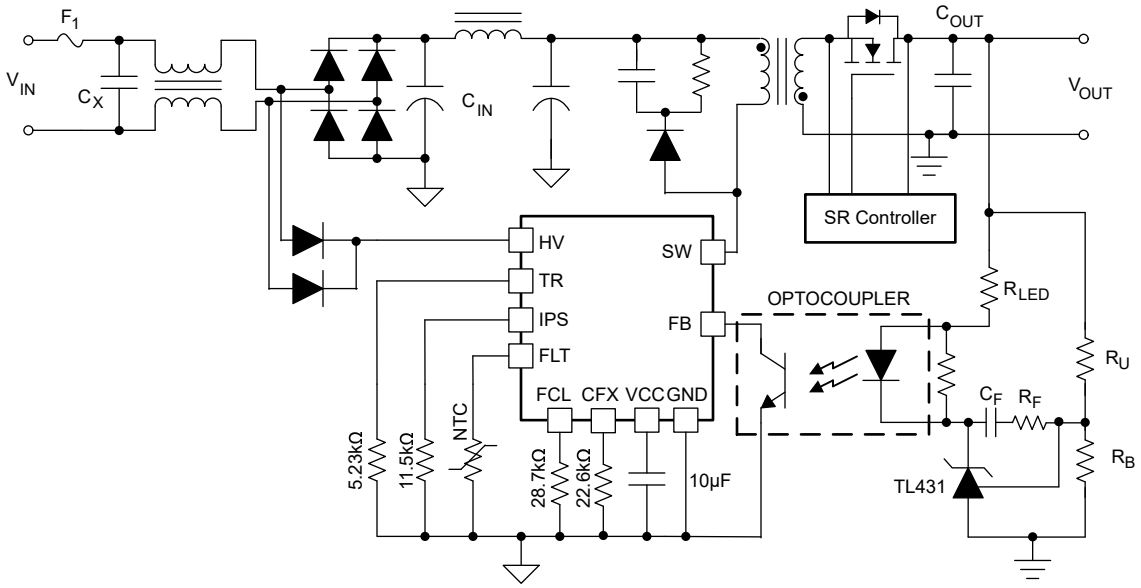


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1. Design Parameters

DESIGN PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line input voltage		90	115/230	264	VAC
Input bulk capacitor voltage		80			V
Line frequency		45	50/60	66	Hz
Output voltage/current	USB-PD output	5V/3A, 9V/3A, 15V/3A, 20V/3.25A			
Output power				65	W
Output ripple				200	mV

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Table 8-1. Design Parameters (continued)

DESIGN PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency			>93% at full load		
No-load input power				30	mW
Tiny load input power	P_{OUT} = 180mW			300	mW
Switching frequency				140	kHz

8.2.2 Detailed Design Procedure

This section describes the method for calculating the power stage component values.

8.2.2.1 Input Bulk Capacitor

The bulk capacitor includes one or more high voltage electrolytic capacitors in parallel at the output of the bridge rectifier. Capacitors are required for storing energy for the duration when instantaneous line input voltage reduces below the peak value while delivering rated output power. Input EMI filter design is outside the scope of this datasheet and not discussed.

Maintain a certain minimum input bulk capacitor voltage ($V_{BULKmin}$) to prevent from triggering brown-out and providing sufficient power delivery capability. $V_{BULKmin}$ is assumed as 75V for this design. The minimum required input bulk capacitance (C_{IN}) is estimated using Equation 5. The value depends on the rated input power, $V_{BULKmin}$, min. AC line input voltage and the time duration for which this capacitor must support the output load, without reducing below $V_{BULKmin}$.

$$C_{IN} = \frac{2P_{IN} \times \left(\frac{1}{4f_{AC}} + \frac{1}{2\pi f_{AC}} \arcsin\left[\frac{V_{BULKmin}}{\sqrt{2}V_{ACmin}} \right] \right)}{(\sqrt{2}V_{ACmin})^2 - (V_{BULKmin})^2} \quad (5)$$

Using above equation, min C_{IN} value comes to 100µF for P_{OUT} of 65W, 93% efficiency at V_{ACmin} of 85VAC. Multiple capacitors can be used in parallel to realize this value to reduce total ESR and size of these capacitors.

8.2.2.2 Transformer Primary Inductance and Turns Ratio

The transformer turns ratio is limited by the primary GaN HEMT maximum drain-source voltage (V_{DS}) rating and determines the secondary SR FET voltage rating and switching losses. The turns ratio is chosen as 6 for this design to reduce the snubber losses and improve efficiency. The UCG2883x/4x supports turns ratio in the range from 6 to 7.875 for 20V output.

The transformer primary inductance determines the switching frequency through the range of flyback converter operation using UCG2883x/4x. For this design, the switching frequency is assumed at half of the maximum limit of 140kHz, which is 70kHz at low line input 90VAC. At this input voltage and full load 65W, the converter operates in 1st valley QR mode and the demagnetization ringing duration is ignored to give duty cycle:

$$D_{max} = \frac{NV_{OUT}}{V_{IN} + NV_{OUT}} \quad (6)$$

where turns ratio N is given by the following:

$$N = \frac{N_P}{N_S} \quad (7)$$

From Equation 6 and Equation 7, the primary inductance is given by the following:

$$L_M = \frac{V_{BULKmin}^2 \times D_{max}^2 \times T_{SW} \times \eta}{2P_{OUTmax}} \quad (8)$$

Based on turns ratio equal to 6, the secondary SR FET voltage is calculated using Equation 9 and current rating is calculated using Equation 10. With 25% margin, use an SR FET of at least 100V and 24A rating.

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$$V_{SRFET} = \frac{\sqrt{2}V_{ACmax}}{N} + V_{OUT} \quad (9)$$

$$I_{SEC,\,PK} = N \times I_{PRI,\,PK} \quad (10)$$

8.2.2.3 Output Capacitor

The output capacitor value is determined based on two specifications: output voltage ripple and output transient voltage response (overshoot and undershoot). The minimum capacitor value for a load step from no-load to full load is given by:

$$C_{OUT} = \frac{I_{step} \times t_{response}}{\Delta V_{OUT}} \quad (11)$$

Where

- I_{step} is the largest output current step
- $t_{response}$ is the loop response time
- ΔV_{OUT} is the allowable output voltage change

$$t_{response} = \frac{0.33}{f_C} + T_{SW} \quad (12)$$

Where

- f_C is the approximate loop crossover frequency, set to 5kHz here
- T_{SW} is the switching time period at the initial load condition before the load step

For crossover frequency of 3kHz, 250kHz switching frequency in burst mode, output current step of 3.25A and voltage undershoot and overshoot of 0.5V, the minimum required output capacitor value is 740µF. To account for the capacitor ESR and ESL, an 820µF capacitor is chosen.

8.2.2.4 Selection Resistors

The UCG2883x/4x offers programming options with resistors on IPS, TR, CFX and FCL pins for user to configure the device for the required configuration. Refer to Table 7-1, Table 7-2, Table 7-3 and Table 7-4 for resistor values to set a turns ratio of 6, 3.1A maximum peak current, 1.03A minimum peak current, CCM enabled, X-cap discharge enabled and 140kHz frequency clamp required for notebook charger applications.

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8.2.3 Application Curves

The figures below are measured on the 65W, universal input evaluation module for UCG2883x/4x. The waveforms show switching at different valleys for different output powers, frequency foldback and burst mode operation and no-load to full load transients with 20V and 5V output.

Yellow: SW node, Green: Input bulk capacitor voltage, Pink: FB pin voltage

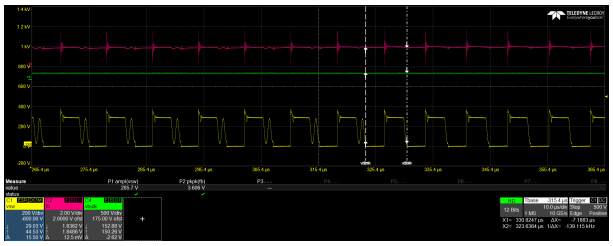


Figure 8-2. 1st and 2nd Valley Operation at 115VAC

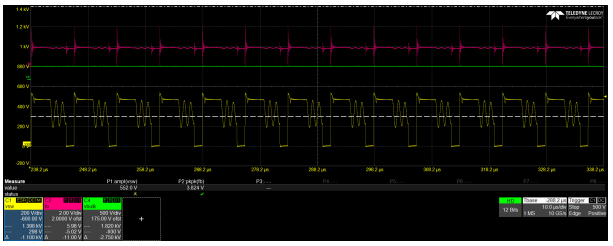


Figure 8-3. 3rd Valley Operation at 230VAC

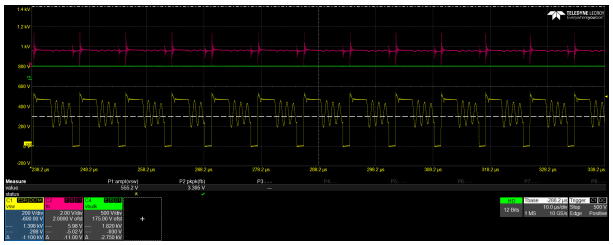


Figure 8-4. 4th Valley Operation at 230VAC

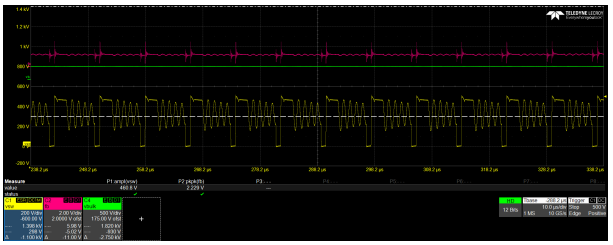


Figure 8-5. 5th Valley Operation at 230VAC

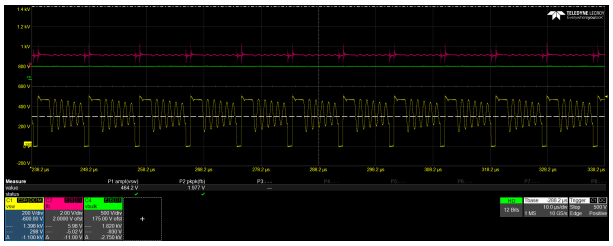


Figure 8-6. 6th Valley Operation at 230VAC

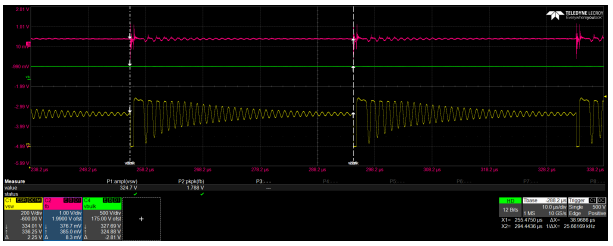


Figure 8-7. Frequency Foldback Mode at 230VAC

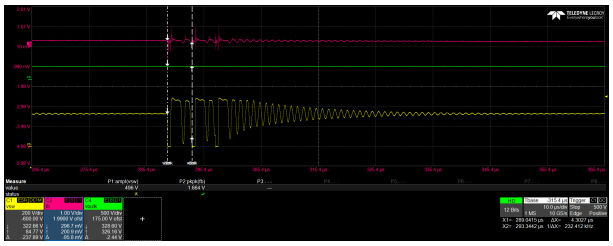
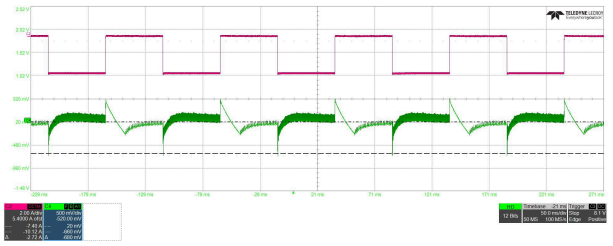


Figure 8-8. Burst Mode at 230VAC

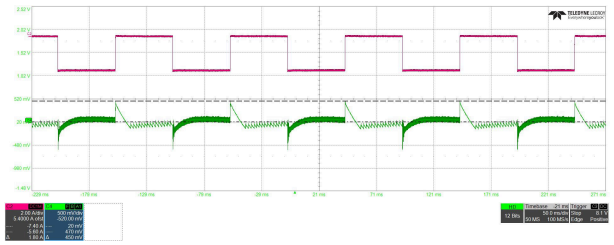


Note

Green: V_{OUT}, Pink: Output current

Figure 8-9. Load Transient at 230VAC and 20V Output

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Note

Green: V_{OUT}, Pink: Output current

Figure 8-10. Load Transient at 230VAC and 5V Output

8.3 Power Supply Recommendations

The UCG2883x/4x is intended for use in AC/DC adapters with universal AC input in the range from 85VAC to 264VAC, 45Hz to 66Hz, using flyback topology for up to 65W output. While the UCG2883x/4x is useful for USB-PD charger applications, this converter is also used in industrial applications with fixed output voltages at 12V, 24V, 36V, and so on. Change the TR pin resistor to accommodate output voltages that are different from the default 20V maximum output voltage setting. On the secondary side feedback, achieve output regulation with a USB-PD controller or TL431 for fixed output designs.

UCG2883x/4x uses self-biasing technology, eliminates the need for Flyback auxiliary winding, reduces BoM cost, improves the efficiency, and simplifies the EMI design. The VCC voltage is self-regulated up to $V_{VCC(REG)}$ level. To provide proper function of the self-biasing mechanism place a high-frequency, low-ESL 0.1µF ceramic capacitor within 1mm of the VCC and GND pins.

Additionally, the overall VCC capacitance is selected based on the line frequency and line drop out test requirement. To minimize the converter standby power, the VCC capacitor must hold enough energy to provide the UCG2883x/4x supply current in burst mode ($I_{VCCSLEEP}$) through out half a line cycle. If the power supply must pass a line drop out test, VCC capacitor must hold enough energy to provide the supply current in burst mode ($I_{VCCSLEEP}$), and through out the line drop-out period. The VCC capacitance is determined by the larger holdup time required for burst mode operation or line drop-out test. Follow Equation 13 to select the corresponding capacitor value. Because the capacitance reduces with voltage applied, perform capacitance derating.

$$C_{VCC} > \left(T_{holdup} \times I_{VCCSLEEP}\right) \div 0.3V \quad (13)$$

8.4 Layout

8.4.1 Layout Guidelines

To increase the reliability and feasibility of the design, recommendations are to adhere to the following guidelines for PCB layout. The guidelines are general recommendations which can be followed for any power supply design and are generally not topology-specific. The main theme in power supply layouts is to keep high current loops as small as possible to avoid coupling and any additional losses or false switching due to inaccurate sensing caused by board parasitics.

1. Minimize the high current loops to reduce parasitic capacitances and inductances. For UCG2883x/4x, high current loops are the primary side power loop, secondary side power loop and the leakage snubber loop.
2. Separate the device signal ground from the high current ground to isolate the switching noise away from the low voltage signals. For UCG2883x/4x, the components on pins 4-11 are referenced to GND pins 3 and 10 which then connect to the device thermal pad and GND power plane and follows this recommendation.
3. Place the bypass capacitor on VCC pin as close as possible to the VCC and GND pins of the device.
4. Route the trace from HV pin through the two diodes to X-capacitor orthogonal and away from the SW pin or trace to minimize switching noise coupling to the flyback converter input and avoid bypassing the EMI filter components.

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Use the *UCG28826 Evaluation Module* User's Guide as a reference when designing the circuit board.

8.4.2 Layout Example

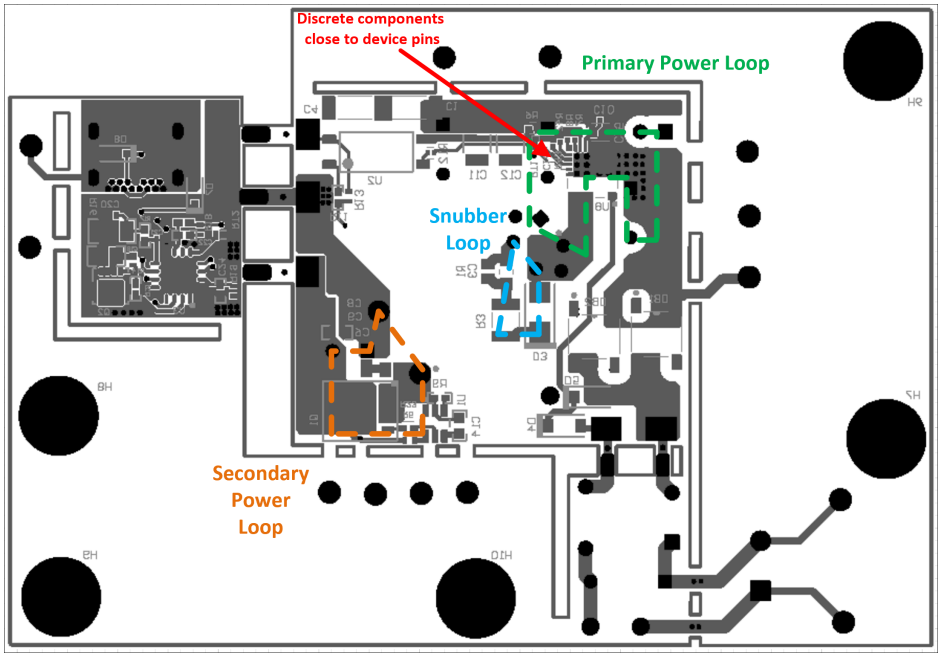


Figure 8-11. Bottom Layer Layout of UCG28826EVM-093 Evaluation Board

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *Design a Fixed Output Voltage Flyback with the UCG2882x Family of Devices*, application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics*, application note
- Texas Instruments, *UCG28826EVM-093 Using the UCG28826EVM-093 65W USB-C PD High Density GaN Integrated Quasi-Resonant Flyback Converter*, EVM user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2026) to Revision C (October 2026)	Page
• Added UCG28838 to datasheet	1
• Added UCG28844 to datasheet	1
• Changed the document status from *Production Data* to *Production Mixed*	1

Changes from Revision A (March 2026) to Revision B (April 2026)	Page
• Changed the document status from *Production Mix* to *Production Data*	1

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Changes from Revision * (March 2026) to Revision A (March 2026)	Page
• Changed the document status from *Advance Information* to *Production Mix*	1
• Added UCG28846 to datasheet	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCG28836-1REZR	Active	Production	VQFN (REZ) | 12	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	U288361 NNNNC
UCG28838-2REZR	Active	Production	VQFN (REZ) | 12	2000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 105	U288382 NNNNC
UCG28846-1DR	Active	Production	SOIC (D) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	U288461

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

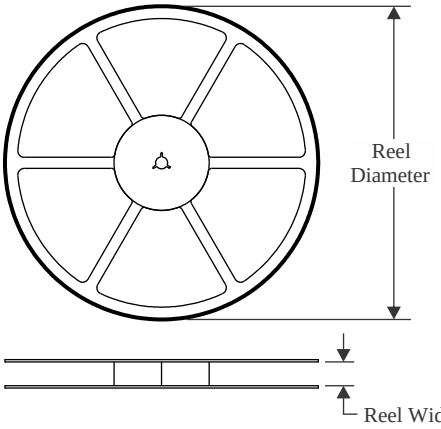
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

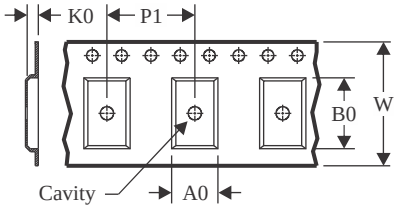
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

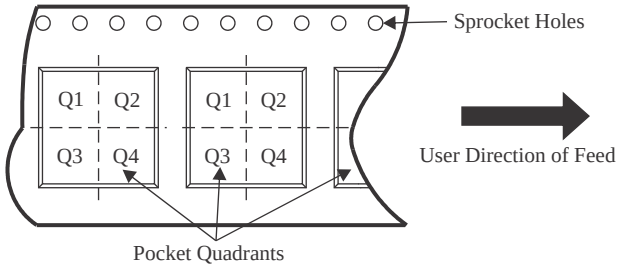


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

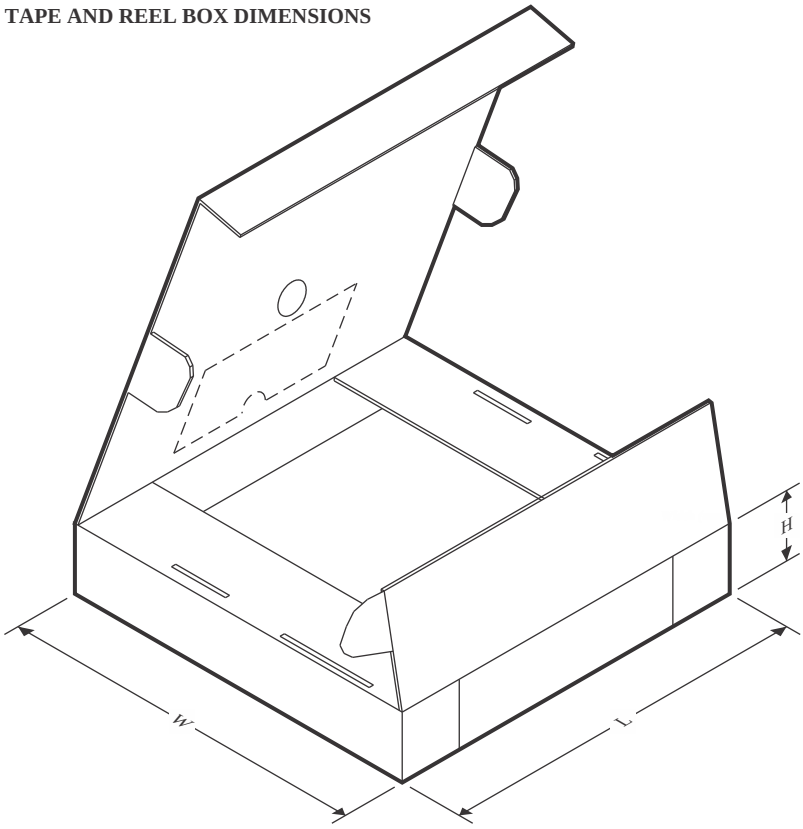
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCG28836-1REZR	VQFN	REZ	12	2000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
UCG28838-2REZR	VQFN	REZ	12	2000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
UCG28846-1DR	SOIC	D	16	2000	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

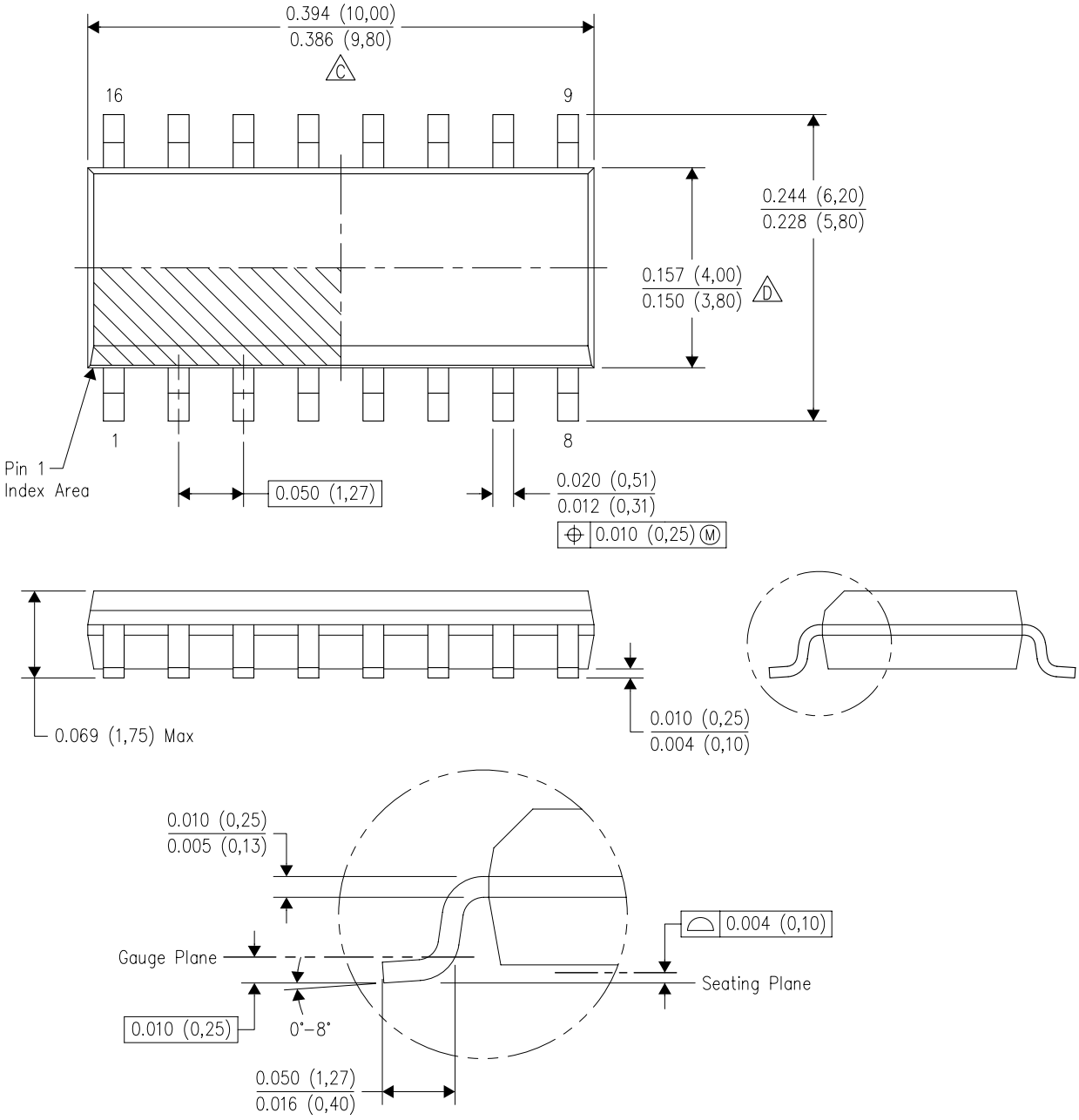
TAPE AND REEL BOX DIMENSIONS



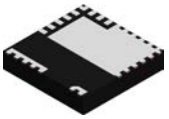
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCG28836-1REZR	VQFN	REZ	12	2000	346.0	346.0	33.0
UCG28838-2REZR	VQFN	REZ	12	2000	346.0	346.0	33.0
UCG28846-1DR	SOIC	D	16	2000	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

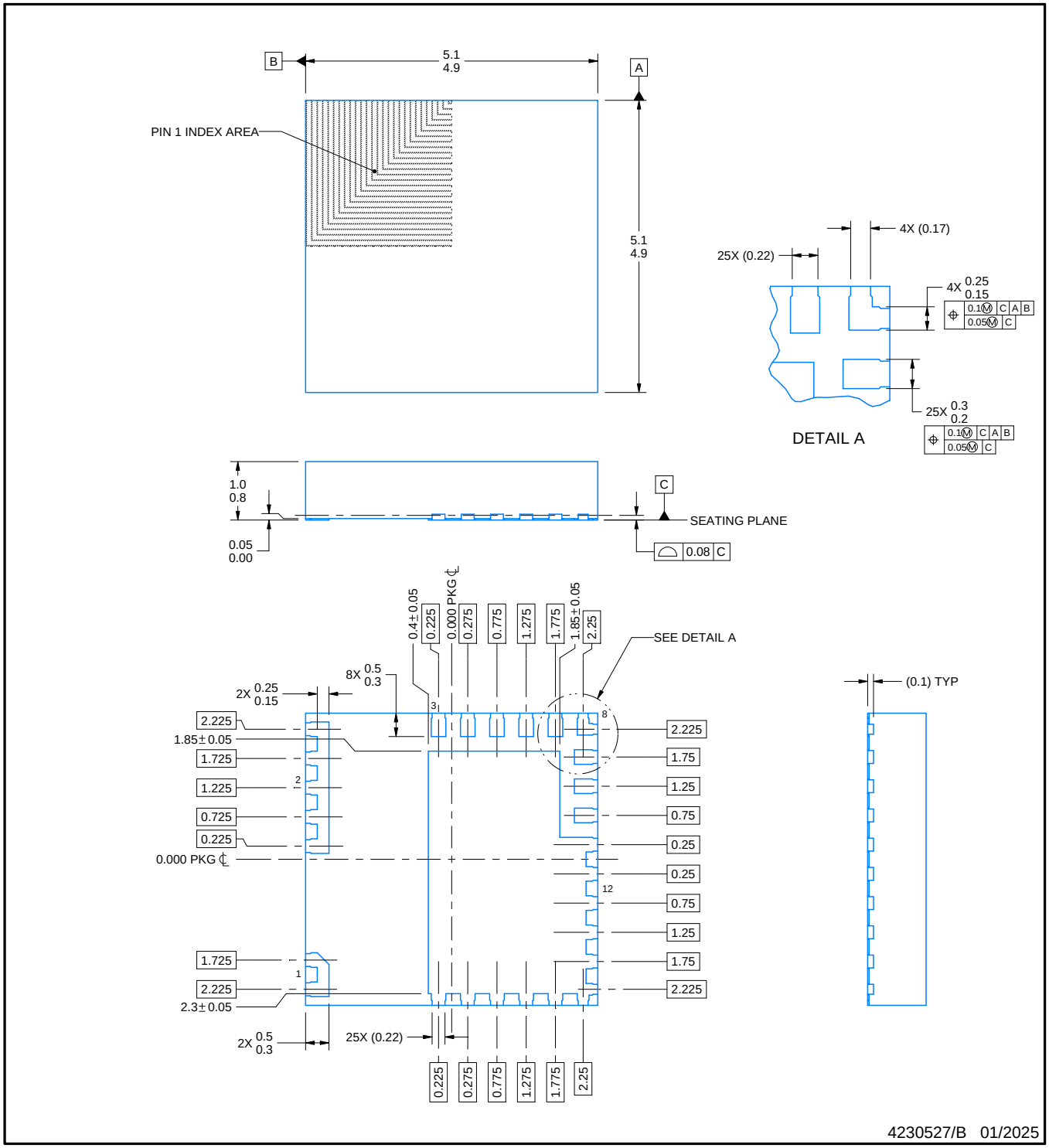


PACKAGE OUTLINE

REZ0012A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

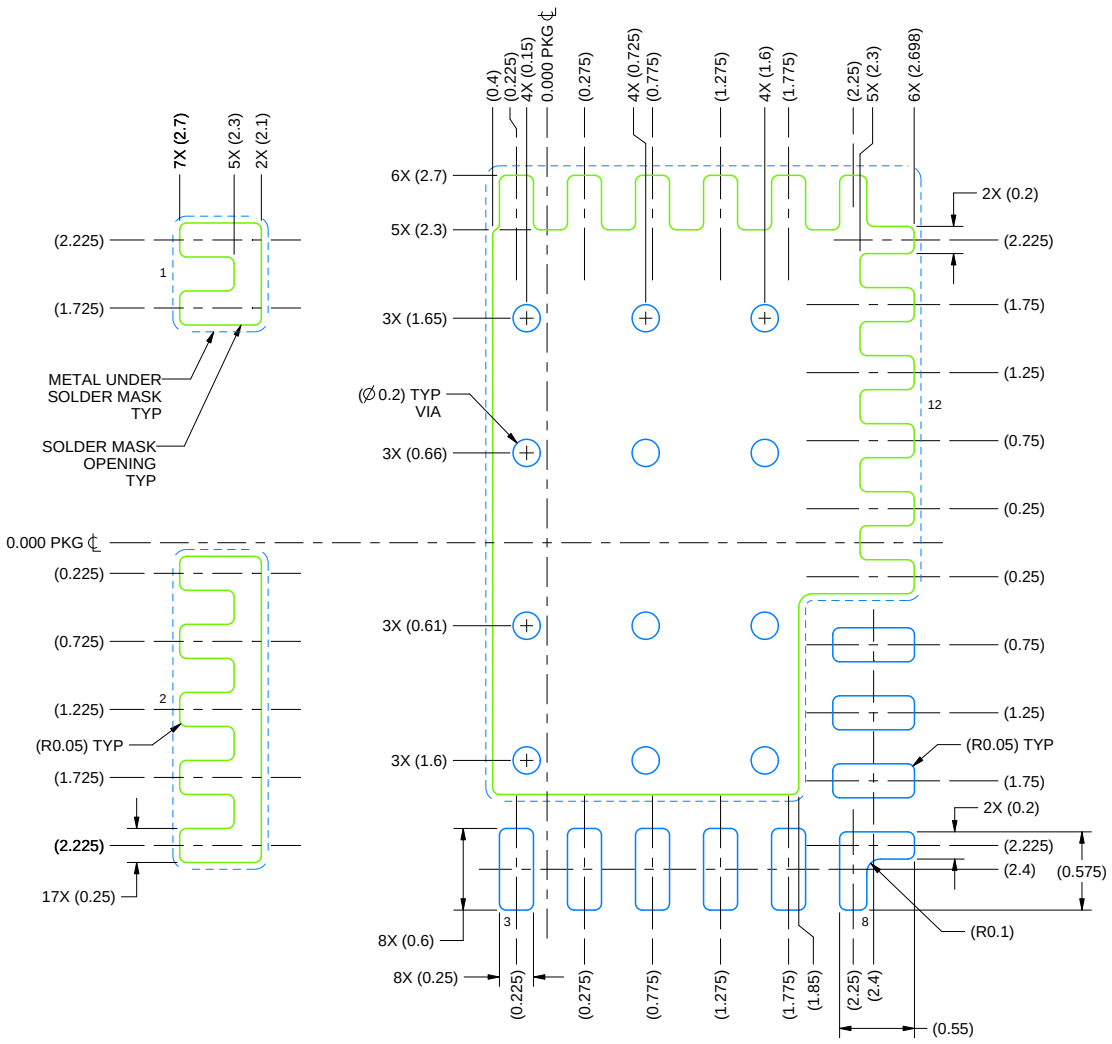
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

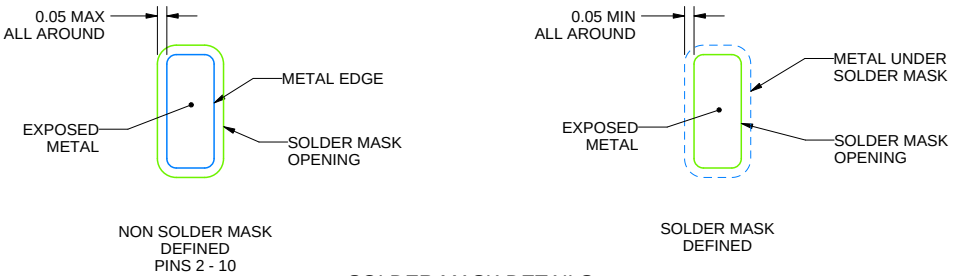
REZ0012A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 18X



NON SOLDER MASK DEFINED PINS 2 - 10

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

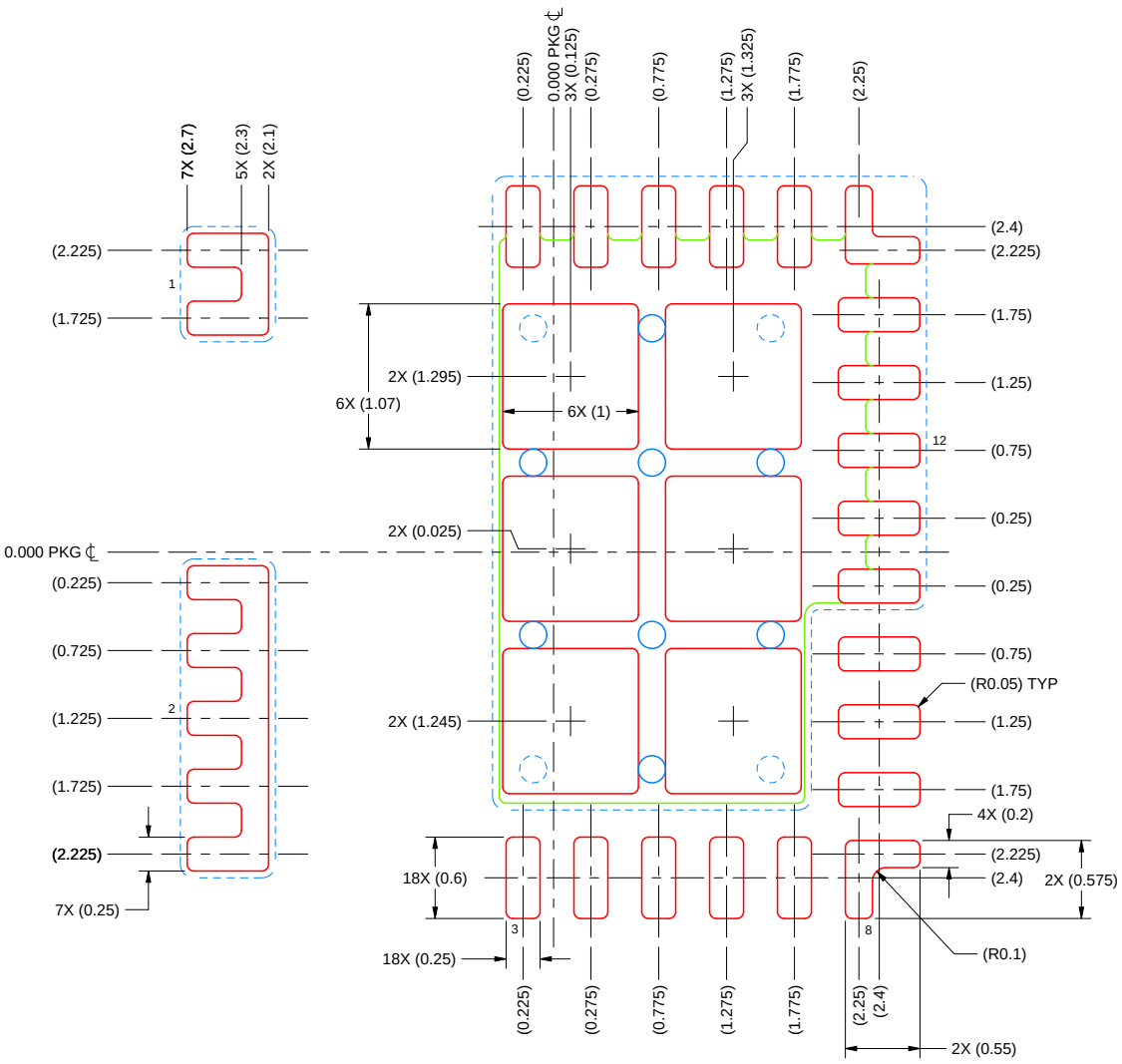
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

REZ0012A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 18X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 12: 71%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025