TPLD2001-Q1 Automotive Programmable Logic Device with 18-GPIO and Selectable I²C/SPI

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: -40°C to 125°C ambient temperature range
- Operating characteristics
  - Extended temperature range: -40°C to 125°C
  - Wide supply voltage range: 1.71V to 5.5V
- Configurable macro-cells
  - 2-, 3-, and 4-bit lookup tables (LUT)
  - D-type flip-flops and latches with and without reset/set option
  - 8-bit shift register
  - 16-bit pattern generator
  - 8-state state machine
  - Counters and delay generators
  - PWM generators
  - Watchdog timer
  - Programmable deglitch filter or edge detector
  - Discrete analog comparators
  - Multi-channel sampling analog comparator with multi-voltage reference select
  - Voltage reference and Analog temperature sensor
  - Analog multiplexers
  - Oscillators
- Flexible digital I/O features
  - All digital signals can be routed to any GPIO
  - Digital input modes: digital in with and without Schmitt-trigger, low-voltage digital in
  - Digital output modes: push-pull, open-drain NMOS, tri-state
- Development tools
  - TPLD2001-Q1 evaluation module
  - TPLD programmer
  - InterConnect Studio
- In-line programming capable

2 Applications

- Wearables
- PC and notebooks
- Personal electronics
- Factory automation and control
- Gaming applications
- Communications equipment
- Automotive

3 Description

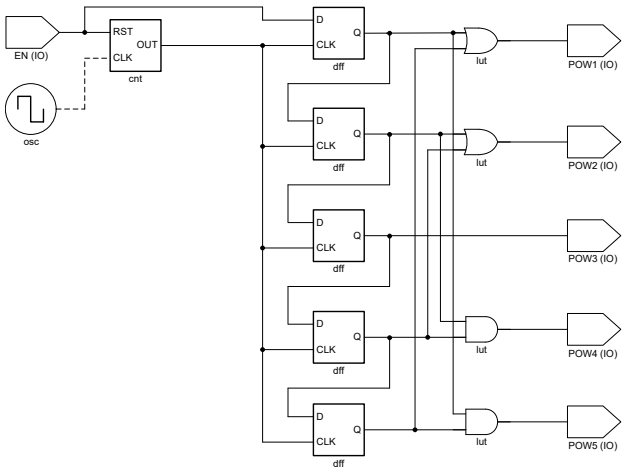
The TPLD2001-Q1 is part of the TI Programmable Logic Device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks. TPLD provides an integrated, compact, low power design to implement common system functions, such as timing delays, voltage monitors, system resets, power sequencers, I/O expanders, and more. This cost-optimized device offers a rich set of functionality in a small form factor, supports an extended temperature range from -40°C to 125°C, and operates with supply voltages ranging from 1.71V to 5.5V.

System designers can create circuits and configure the macro-cells, I/O pins, and interconnections by temporarily emulating the non-volatile memory or by permanently programming the one-time programmable (OTP) via InterConnect Studio. The TPLD2001-Q1 is supported by an extensive hardware and software ecosystem with application notes, reference designs and design examples. Visit ti.com for more information and access to design tools.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPLD2001-Q1	DGS (VSSOP, 20)	5.10mm × 3.00mm

(1) For more information, see Mechanical, Packaging and Orderable Information
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

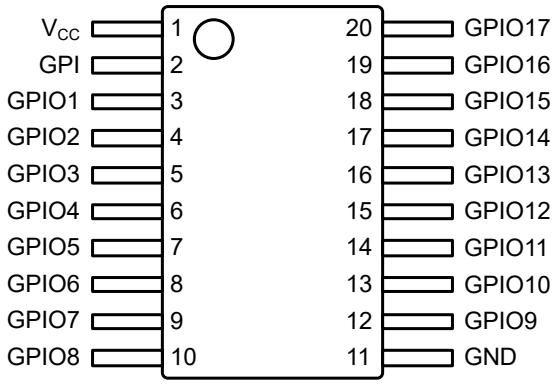

Figure 4-1. DGS Package, 20-Pin VSSOP (top view)

Table 4-1. Pin Functions

PIN			DESCRIPTION			
NAME	VSSOP (DGS)	TYPE[1]	Primary function	Secondary analog function (if any)	Secondary digital function (if any)	Secondary serial communications function (if any)
GPI	2	I	General-purpose input[2]			VPP
GPIO1	3	I/O	General-purpose I/O with OE[3]	AMUX0A / ACMP IN2		Interface select
GPIO2	4	I/O	General-purpose I/O with OE[3]	AMUX0B / ACMP IN3		I^2C address 6
GPIO3	5	I/O	General-purpose I/O with OE[3]	AMUX0Y		I^2C address 5
GPIO4	6	I/O	General-purpose I/O	ACMP IN0		I^2C address 4
GPIO5	7	I/O	General-purpose I/O			SPI nCS / I^2C address 3
GPIO6	8	I/O	General-purpose I/O			SPI SCLK / I^2C SCL
GPIO7	9	I/O	General-purpose I/O			SPI SDI / I^2C SDA
GPIO8	10	I/O	General-purpose I/O			SPI SDO
GND	11	P	Ground			
GPIO9	12	I/O	General-purpose I/O	Ext. VREF IN		
GPIO10	13	I/O	General-purpose I/O with OE[3]	McACMP IN0		
GPIO11	14	I/O	General-purpose I/O with OE[3]	McACMP IN1		
GPIO12	15	I/O	General-purpose I/O with OE[3]	McACMP IN2		
GPIO13	16	I/O	General-purpose I/O with OE[3]	McACMP IN3		
GPIO14	17	I/O	General-purpose I/O	AMUX1A	OSC0 Ext. CLK	
GPIO15	18	I/O	General-purpose I/O with OE[3]	AMUX1B	OSC1 Ext. CLK	
GPIO16	19	I/O	General-purpose I/O with OE[3]	ACMP IN1		
GPIO17	20	I/O	General-purpose I/O with OE[3]	AMUX1Y	OSC2 Ext. CLK	

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Table 4-1. Pin Functions (continued)

PIN			DESCRIPTION			
NAME	VSSOP (DGS)	TYPE(1)	Primary function	Secondary analog function (if any)	Secondary digital function (if any)	Secondary serial communications function (if any)
V_{CC}	1	P	Supply voltage			

(1) P = power, I/O = input/output, I = input
(2) The general-purpose input (GPI) pin will sustain a high-voltage (VPP) during programming. Take special precaution with peripherals connected to this pin if performing in-system programming.
(3) The output enable (OE) connection is available through the connection mux and can be configured in InterConnect Studio.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage on V_{CC} relative to GND		-0.5	7	V
V_I	Input voltage range[2]		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range[2]		-0.5	V_{CC} + 0.5	V
I_{IOK}	Input-output clamp current	V_{IO} < 0 or V_{IO} > V_{CC}	-50	50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	-50	50	mA
I_{DC}	Maximum average or DC current (through each pin)	Push-pull 1X		12	mA
		Push-pull 2X		17	
		Open-drain NMOS 1X		18	
		Open-drain NMOS 2X		28	
		Open-drain NMOS 4X		45	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			1.71	5.5	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
V_{IH}	High-level input voltage	Logic input	1.71V to 5.5V	(0.7 × V_{CC})		V
		Low-voltage logic input	1.8V ± 0.09V	0.90		
			3.3V ± 0.3V	1.08		
			5V ± 0.5V	1.22		
V_{IH}	High-level input voltage	I^2C SCL, SDA pins SPI SDI, SCLK, nCS	1.71V to 5.5V	(0.7 × V_{CC})		V
V_{IL}	Low-level input voltage	Logic input	1.71V to 5.5V		(0.3 × V_{CC})	V
		Low-voltage logic input	1.8V ± 0.09V		0.47	
			3.3V ± 0.3V		0.52	
			5V ± 0.5V		0.56	
V_{IL}	Low-level input voltage	I^2C SCL, SDA pins SPI SDI, SCLK, nCS	1.71V to 5.5V		(0.3 × V_{CC})	V

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over operating free-air temperature range (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
F_{IN_MAX}	Maximum input frequency	IN0 only	1.71V to 5.5V		250	kHz
$F_{(EXT_OSC)}$	External Oscillator Frequency	Logic input	1.71V to 5.5V		25	MHz
T_A	Ambient temperature			–40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC[1]						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DGS (VSSOP)	20	92.9	35.7	49.7	1.3	49.3	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Supply and Power-on Reset								
V_{PORR}	Power-on reset voltage, V_{CC} rising		$V_I = V_{CC}$ or GND, $I_O = 0$		1.20		1.45	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		$V_I = V_{CC}$ or GND, $I_O = 0$		1.14		1.36	V
t_{SU}	Startup time		from V_{CC} rising past V_{PORR} to GPO becoming active			0.76		ms
V_{PP}	Programming voltage				7.5		8	V
t_{PP}	Programming time					50		ms
Digital IO								
V_{T+}	Positive-going input threshold voltage	Logic Input with Schmitt Trigger		1.8V ± 0.09V	0.94		1.27	V
				3.3V ± 0.3V	1.55		2.17	
				5V ± 0.5V	2.21		3.19	
V_{T-}	Negative-going input threshold voltage	Logic Input with Schmitt Trigger		1.8V ± 0.09V	0.58		0.94	V
				3.3V ± 0.3V	1.10		1.79	
				5V ± 0.5V	1.63		2.7	
V_{HYS}	Schmitt-Trigger hysteresis (V_{T+} - V_{T-})	Logic Input with Schmitt Trigger		1.8V ± 0.09V	0.24	0.36		V
				3.3V ± 0.3V	0.33	0.42		
				5V ± 0.5V	0.40	0.49		
V_{HYS}	IN0 hysteresis			1.71V to 5.5V			0.2	V
V_{OH}	High-level output voltage	Push-pull 1X	I_{OH} = -100µA	1.8V ± 0.09V	1.68			V
		Push-pull 2X			1.69			
		Push-pull 1X	I_{OH} = -3mA	3.3V ± 0.3V	2.47			
		Push-pull 2X			2.63			
		Push-pull 1X	I_{OH} = -5mA	5V ± 0.5V	3.84			
		Push-pull 2X			4.02			
V_{OH}	High-level output voltage	SPI SDO	I_{OH} = -2mA	1.71V to 5.5V	(0.7 × V_{CC})			V

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	Push-pull 1X	I_{OL} = 100µA	1.8V ± 0.09V			0.01	V
		Push-pull 2X					0.01	
		Open-drain NMOS 1X					0.01	
		Open-drain NMOS 2X					0.01	
		Push-pull 1X	I_{OL} = 3mA	3.3V ± 0.3V			0.1	
		Push-pull 2X					0.1	
		Open-drain NMOS 1X					0.1	
		Open-drain NMOS 2X					0.1	
		Push-pull 1X	I_{OL} = 5mA	5V ± 0.5V			0.12	
		Push-pull 2X					0.12	
		Open-drain NMOS 1X					0.12	
		Open-drain NMOS 2X					0.12	
V_{OL}	Low-level output voltage	I^2C SCL, SDA pins (Open-drain NMOS 4X)	I_{OL} = 3mA	V_{CC} > 2V			0.4	V
		I^2C SCL, SDA pins (Open-drain NMOS 4X)	I_{OL} = 2mA	V_{CC} ≤ 2V			(0.2 × V_{CC})	
		SPI SDO pin	I_{OL} = 2mA	1.71V to 5.5V			(0.3 × V_{CC})	
I_{OL}	Low-level output current	I^2C SCL, SDA pins (Standard mode, Fast mode)	V_{OL} = 0.4V	1.71V to 5.5V	3			mA
		I^2C SCL, SDA pins (Fast mode Plus)			20			
I_I	Input leakage current	All pins	V_I = V_{CC}	1.71V to 5.5V			±1	µA
			V_I = GND				±1	
I_{OZ}	Off-state (high-Z state) output current		V_O = 0 to 5.5V	1.71V to 5.5V			±1	µA
F_{OUT}	Max output frequency (1)	All IOs Push-pull 1X or Push-pull 2X	C_L = 15pF	1.8V ± 0.09V			8	MHz
				3.3V ± 0.3V			8	MHz
				5V ± 0.5V			8	MHz
F_{OUT}	Max output frequency (1)	IO14, IO15, IO17 only Push-pull 1X or Push-pull 2X	C_L = 15pF	1.8V ± 0.09V			10	MHz
				3.3V ± 0.3V			12	MHz
				5V ± 0.5V			12	MHz
$R_{pu(int)}$	Internal pull-up resistance					1		MΩ
						100		kΩ
						10		kΩ
$R_{pd(int)}$	Internal pull-down resistance					1		MΩ
						100		kΩ
						10		kΩ
C_I	Input pin capacitance	Each input pin	V_I = V_{CC} or GND	1.71V to 5.5V		4	10	pF
C_I	Input pin capacitance	I^2C SCL pin SPI SDI, SCK, nCS pins	V_I = V_{CC} or GND	1.71V to 5.5V		4	10	pF
C_{IO}	Input-output pin capacitance	Each I/O pin	V_{IO} = V_{CC} or GND	1.71V to 5.5V		4	10	pF
C_{IO}	Input-output pin capacitance	I^2C SDA pin	V_{IO} = V_{CC} or GND	1.71V to 5.5V		4	10	pF
Analog Comparator - Discrete Analog Comparator								

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{start}	Start time	ACMP power on delay	Bandgap force on, Oscillator force on	1.71V to 5.5V		120		µs
			Bandgap force on, Oscillator auto on			120		
			Bandgap auto on, Oscillator force on			120		
			Bandgap auto on, Oscillator auto on			180		
V_{AI}	Input voltage	Positive input		1.71V to 5.5V	0		V_{CC}	V
		Negative input			0		2.016	
V_{offset}	Input offset voltage	T_A = 25°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 1504mV	1.71V to 5.5V	-12		12	mV
		–40°C < T_A ≤ 125°C			-15		15	
		T_A = 25°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 2016mV	2.3V to 5.5V	-12		12	
		–40°C < T_A ≤ 125°C			-15		15	
dV_{IO}/dT	Input offset voltage drift	–40°C < T_A ≤ 125°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 1504mV	1.71V to 5.5V	-20	0.1	35	µV/ºC
			V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 2016mV	2.3V to 5.5V	-20	0.1	34	
I_B	Input bias current						1	µA
C_{ID}	Input capacitance, differential					3		pF
C_{IM}	Input capacitance, common mode					3		pF
PROP	Propagation delay, response time	Low to High, Low bandwidth enabled	Gain = 1, Vref = 32mV to 1504mV, Overdrive = 32mV	1.71V to 5.5V			11	µs
		High to Low, Low bandwidth enabled					10	
		Low to High, Low bandwidth disabled					2	
		High to Low, Low bandwidth disabled					2	
		Low to High, Low bandwidth enabled	Gain = 1, Vref = 32mV to 2016mV, Overdrive = 32mV	2.3V to 5.5V			16	
		High to Low, Low bandwidth enabled					9	
		Low to High, Low bandwidth disabled					3	
		High to Low, Low bandwidth disabled					2	
Analog Comparator - Multi-channel Analog Comparator								

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{start}	Start time	ACMP power on delay	Bandgap force on OSC force on 1-channel, 1-VREF	1.71V to 5.5V		135		µs
			Bandgap force on OSC0 force on Multi-channel mode			2.9		ms
			Bandgap force on OSC1 force on Multi-channel mode			150		µs
V_{AI}	Input voltage	Positive input		1.71V to 5.5V	0		V_{CC}	V
		Negative input			0		2.016	
V_{offset}	Input offset voltage	T_A = 25°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 1504mV	1.71V to 5.5V	-12		12	mV
		–40°C < T_A ≤ 125°C			-15		15	
		T_A = 25°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 2016mV	2.3V to 5.5V	-12		12	
		–40°C < T_A ≤ 125°C			-15		15	
dV_{IO}/dT	Input offset voltage drift	–40°C < T_A ≤ 125°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 1504mV	1.71V to 5.5V	-20	0.1	35	µV/ºC
			V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 2016mV	2.3V to 5.5V	-20	0.1	31	
I_B	Input bias current						1	µA
C_{ID}	Input capacitance, differential					3		pF
C_{IM}	Input capacitance, common mode					3		pF

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
PROP	Propagation delay, response time	Low to High, Low bandwidth enabled	1 channel, Gain = 1, Vref = 32mV to 1504mV, Overdrive = 32mV	1.71V to 5.5V			11	µs
		High to Low, Low bandwidth enabled					10	
		Low to High, Low bandwidth disabled	1 channel, Gain = 1, Vref = 32mV to 1504mV, Overdrive = 32mV	1.71V to 5.5V			2	
		High to Low, Low bandwidth disabled					2	
		Low to High, Low bandwidth enabled	1 channel, Gain = 1, Vref = 32mV to 2016mV, Overdrive = 32mV	2.3V to 5.5V			11	µs
		High to Low, Low bandwidth enabled					8	µs
		Low to High, Low bandwidth disabled	1 channel, Gain = 1, Vref = 32mV to 2016mV, Overdrive = 32mV	2.3V to 5.5V			2	µs
		High to Low, Low bandwidth disabled					2	µs
		Low to High	Multi-channel, Gain = 1, Vref = 32mV to 1504mV, Overdrive = 32mV	1.71V to 5.5V			(t_{SMP_CLK} × CH)	µs
		High to Low					(t_{SMP_CLK} × CH)	µs
		Low to High	Multi-channel, Gain = 1, Vref = 32mV to 2016mV, Overdrive = 32mV	2.3V to 5.5V			(t_{SMP_CLK} × CH)	µs
		High to Low					(t_{SMP_CLK} × CH)	µs
Analog Comparator - Hysteresis								
V_{HYS}	Built-in hysteresis	–40°C < T_A ≤ 125°C	V_{HYS} = 64mV	1.71V to 5.5V	54.4	62.8	71.0	mV
			V_{HYS} = 128mV		109.0	126.5	136.1	
			V_{HYS} = 192mV		176.7	189.3	204.3	
Analog Comparator - Input Gain								
R_{sin}	Series input resistance		Gain = 0.5	1.71V to 5.5V		1		MΩ
			Gain = 0.33			0.75		
			Gain = 0.25			1		
G_{err}	Gain error		Gain = 0.5	1.71V to 5.5V	-2.3	1.3	5.8	%
			Gain = 0.33		-1.6	1.6	5.0	
			Gain = 0.25		-1.5	1.8	4.7	
Voltage Reference								

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VREF	Internal VREF error	T_A = 25°C	VREF = 32mV to 512mV	1.71V to 5.5V	-4.98	0.67	5.96	%
		–40°C < T_A ≤ 125°C			-6.61		6.73	
		T_A = 25°C	VREF = 544mV to 1024mV		-6.12	0.05	6.55	
		–40°C < T_A ≤ 125°C			-6.65		6.80	
		T_A = 25°C	VREF = 1056mV to 1504mV		-5.99	0.01	6.40	
		–40°C < T_A ≤ 125°C			-6.59		6.84	
		T_A = 25°C	VREF = 1536mV to 2016mV	2.3 V to 5.5 V	-4.76	0.32	5.59	
		–40°C < T_A ≤ 125°C			-6.31		6.37	
Analog Temperature Sensor								
T_{ERR}	Temperature sensor accuracy		10°C to 45°C	1.71V to 5.5V	-3.8		4.1	ºC
			-40°C to 85°C		-6.5		6.8	
			-40°C to 105°C		-6.5		6.8	
			-40°C to 125°C		-7.4		7.7	
T_{OUT}	Temperature sensor output		-40°C	1.71V to 5.5V	1.212	1.242	1.270	V
			-30°C		1.170	1.197	1.223	
			-20°C		1.128	1.152	1.174	
			-10°C		1.086	1.107	1.127	
			0°C		1.042	1.061	1.079	
			10°C		0.998	1.016	1.033	
			20°C		0.956	0.972	0.986	
			25°C		0.934	0.949	0.963	
			30°C		0.916	0.927	0.937	
			40°C		0.868	0.883	0.897	
			50°C		0.823	0.840	0.854	
			60°C		0.778	0.796	0.813	
			70°C		0.733	0.753	0.771	
			80°C		0.687	0.709	0.730	
			85°C		0.663	0.687	0.709	
			90°C		0.640	0.665	0.688	
			100°C		0.594	0.621	0.647	
			110°C		0.547	0.578	0.608	
			120°C		0.501	0.534	0.567	
			125°C		0.478	0.512	0.545	
t_{DELAY}	Temperature sensor start-up delay			1.71V to 5.5V		70	100	µs
Analog Multiplexer								

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
r_{on}	ON-state switch resistance	–40°C < T_A ≤ 125°C	V_I = 0V, I_O = 4mA	1.8V ± 0.09V			35	Ω
			V_I = 1.71V, I_O = -4mA				35	
			V_I = 0V, I_O = 8mA	2.5V ± 0.2V			32.5	
			V_I = 2.3V, I_O = -8mA				32.5	
			V_I = 0V, I_O = 24mA	3.3V ± 0.3V			30	
			V_I = 3V, I_O = -24mA				35	
			V_I = 0V, I_O = 30mA	5V ± 0.5V			30	
			V_I = 2.4V, I_O = -30mA				30	
			V_I = 4.5V, I_O = -30mA				30	
r_{range}	ON-state switch resistance over signal range	0 ≤ V_A, V_B ≤ V_{CC} –40°C < T_A ≤ 125°C	I_O = -4mA	1.8V ± 0.09V			205	Ω
			I_O = -8mA	2.5V ± 0.2V			75	
			I_O = -24mA	3.3V ± 0.3V			35	
			I_O = -30mA	5V ± 0.5V			25	
Δr_{on}	Difference of ON-state resistance between switches	V_A, V_B = 1.15V –40°C < T_A ≤ 125°C	I_O = -4mA	1.8V ± 0.09V		14.7		Ω
		V_A, V_B = 1.6V –40°C < T_A ≤ 125°C	I_O = -8mA	2.5V ± 0.2V		5.3		
		V_A, V_B = 2.1V –40°C < T_A ≤ 125°C	I_O = -24mA	3.3V ± 0.3V		3.5		
		V_A, V_B = 3.15V –40°C < T_A ≤ 125°C	I_O = -30mA	5V ± 0.5V		3.8		
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_A, V_B ≤ V_{CC} –40°C < T_A ≤ 125°C	I_O = -4mA	1.8V ± 0.09V		110		Ω
			I_O = -8mA	2.5V ± 0.2V		40		
			I_O = -24mA	3.3V ± 0.3V		10		
			I_O = -30mA	5V ± 0.5V		2		
I_{off}	OFF-state switch leakage current		0 ≤ V_I, V_O ≤ V_{CC}	1.71V to 5.5V			±7.5	μA
$I_{S(on)}$	ON-state switch leakage current		V_I = V_{CC} or GND, V_O = Open	5.5V		±0.1	±2.5	μA
Cio(off)	Switch input/output capacitance	A, B		5V		9.5		pF
Cio(on)	Switch input/output capacitance	A, B		5V		20		pF
		Y				20		

(1) Open drain switching performance will be limited by pull-up resistors used

5.6 Supply Current Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Standby											

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T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Standby	Inputs = static, Outputs = open, I_O = 0, OSC powered off, ACMP powered off		1.38			1.41			1.43		µA
I_{CC}	Standby, Bandgap enabled	Bandgap force on		3.46			3.49			3.52		µA
Oscillator												
I_{CC}	OSC0 enabled: 2kHz	Predivide = 1		0.62			0.71			1.11		µA
		Predivide = 2		0.62			0.71			1.07		
		Predivide = 4		0.62			0.71			1.04		
		Predivide = 8		0.62			0.71			1.08		
I_{CC}	OSC1 enabled: 2MHz	Predivide = 1		31.4			34.4			42.7		µA
		Predivide = 2		28.4			31.5			39.8		
		Predivide = 4		26.5			29.5			37.9		
		Predivide = 8		25.4			28.5			36.9		
I_{CC}	OSC2 enabled: 25MHz	Predivide = 1		317.5			319.1			319.8		µA
		Predivide = 2		260.2			261.4			261.9		
		Predivide = 4		227.3			228.3			228.7		
		Predivide = 8		210.7			211.6			212		
I_{CC}	OSC2 enabled: 25MHz	Normal startup, OSC output idle		15.0			15.7			18.2		µA
I_{CC}	OSC2 enabled: 25MHz	Fast startup enabled, OSC output idle		21.0			21.8			23.6		µA
Analog Comparator - Discrete Analog Comparator												
I_{CC}	Discrete analog comparator (ACMP)	External VREF (32mV), IN+ = 0V, Low bandwidth mode disabled		3.57			3.67			3.75		µA
		External VREF (32mV), IN+ = VCC, Low bandwidth mode disabled		4.22			4.33			4.44		
		External VREF (32mV), IN+ = 0V, Low bandwidth mode enabled		0.86			0.86			0.86		
		External VREF (32mV), IN+ = VCC, Low bandwidth mode enabled		0.86			0.87			0.87		
Analog Comparator - Multi-channel Analog Comparator												

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T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Multi-channel sampling analog comparator (McACMP)	1 channel, External VREF (32mV), IN+ = 0V, Low bandwidth mode disabled		3.56			3.66			3.83		µA
		1 channel, External VREF (32mV), IN+ = VCC, Low bandwidth mode disabled		4.2			4.32			4.45		
		1 channel, External VREF (32mV), IN+ = 0V, Low bandwidth mode enabled		0.9			0.91			0.94		
		1 channel, External VREF (32mV), IN+ = VCC, Low bandwidth mode enabled		0.91			0.92			0.94		
		4 channel continuous sampling, External VREF (32mV), IN+ = 0V, OSC = 2kHz		0.94			0.98			1.06		
		4 channel continuous sampling, External VREF (32mV), IN+ = 0V, OSC = 100kHz		4.05			4.17			4.28		
Voltage Reference												
I_{CC}	Voltage reference (VREF)	Internal VREF (32mV to 2016mV)		4.83			4.89			4.93		µA
Analog Temperature Sensor												
I_{CC}	Analog temperature sensor (TS)	Temperature sensor enabled		3.46			3.46			3.55		µA
Analog Multiplexer												
I_{CC}	Analog multiplexer (AMUX)	Analog mux enabled		2.29			3.14			4.01		µA

5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Digital IO									
t_{pd}	Delay	Logic input	Push-pull output	Rising	1.8V ± 0.09V		32.4		ns
				Falling			29.6		
				Rising	3.3V ± 0.3V		19.2		
				Falling			17.0		
				Rising	5V ± 0.5V		15.2		
				Falling			14.4		

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Delay		Logic input with Schmitt trigger	Push-pull output	Rising	1.8V ± 0.09V		38.2		ns
					Falling			36.5		
					Rising	3.3V ± 0.3V		23.4		
					Falling			22.5		
					Rising	5V ± 0.5V		19.2		
					Falling			19.8		
t_{pd}	Delay		Low-voltage logic input	Push-pull output	Rising	1.8V ± 0.09V		32.3		ns
					Falling			32.7		
					Rising	3.3V ± 0.3V		21.3		
					Falling			21.8		
					Rising	5V ± 0.5V		18.5		
					Falling			18.1		
t_{pd}	Delay		Logic input	Open-drain NMOS output	Rising	1.8V ± 0.09V		—		ns
					Falling			26.3		
					Rising	3.3V ± 0.3V		—		
					Falling			17.6		
					Rising	5V ± 0.5V		—		
					Falling			15.4		
t_{pd}	Delay	Output enable from pin	OE	Push-pull output	Hi-Z to 1	1.8V ± 0.09V		45.4		ns
						3.3V ± 0.3V		28.8		
						5V ± 0.5V		24.5		
					Hi-Z to 0	1.8V ± 0.09V		39.3		ns
						3.3V ± 0.3V		24.5		
						5V ± 0.5V		21.1		
Configurable Use Logic										
t_{pd}	Delay	2-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		1.0		ns
					Falling			0.9		
					Rising	3.3V ± 0.3V		1.0		
					Falling			0.9		
					Rising	5V ± 0.5V		1.0		
					Falling			0.9		
t_{pd}	Delay	3-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		0.9		ns
					Falling			0.7		
					Rising	3.3V ± 0.3V		0.9		
					Falling			0.7		
					Rising	5V ± 0.5V		0.9		
					Falling			0.7		
t_{pd}	Delay	4-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		1.1		ns
					Falling			1.0		
					Rising	3.3V ± 0.3V		1.1		
					Falling			1.0		
					Rising	5V ± 0.5V		1.1		
					Falling			1.0		

over operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Delay	DFF/Latch	CLK	Q	Rising	1.8V ± 0.09V		1.5		ns
					Falling			1.6		
					Rising	3.3V ± 0.3V		1.5		
					Falling			1.6		
					Rising	5V ± 0.5V		1.6		
					Falling			1.7		
t_{pd}	Delay	DFF/Latch	nRST/nSET	Q	Rising	1.8V ± 0.09V		4.6		ns
					Falling			4.6		
					Rising	3.3V ± 0.3V		4.7		
					Falling			4.6		
					Rising	5V ± 0.5V		4.7		
					Falling			4.6		
t_{pd}	Delay	Shift register	CLK	OUT	Rising	1.8V ± 0.09V		1.5		ns
					Falling			1.6		
					Rising	3.3V ± 0.3V		1.5		
					Falling			1.6		
					Rising	5V ± 0.5V		1.5		
					Falling			1.6		
t_{pd}	Delay	Shift register	nRST	OUT	Rising	1.8V ± 0.09V		—		ns
					Falling			2.2		
					Rising	3.3V ± 0.3V		—		
					Falling			2.2		
					Rising	5V ± 0.5V		—		
					Falling			2.2		
t_{pd}	Delay	Pattern generator	CLK	OUT	Rising	1.8V ± 0.09V		1.7		ns
					Falling			1.7		
					Rising	3.3V ± 0.3V		1.5		
					Falling			1.6		
					Rising	5V ± 0.5V		1.7		
					Falling			1.7		
Counter/Delay										
t_{pd}	Delay	Counter - Delay mode	Rising edge of IN	Rising edge of OUT	Falling edge triggered	1.8V ± 0.09V		3.7		ns
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			2.9		
			Rising edge of IN	Rising edge of OUT	Falling edge triggered	3.3V ± 0.3V		3.7		
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			2.9		
			Rising edge of IN	Rising edge of OUT	Falling edge triggered	5V ± 0.5V		3.7		
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			2.9		

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pw}	Pulse width	Counter - Edge detect mode	Rising edge of OUT	Falling edge of OUT	Rising edge detect	1.8V ± 0.09V		19.7		ns
						3.3V ± 0.3V		19.8		
						5V ± 0.5V		19.8		
					Falling edge detect	1.8V ± 0.09V		19.9		
						3.3V ± 0.3V		19.9		
						5V ± 0.5V		19.9		
					Both edge detect	1.8V ± 0.09V		19.9		
						3.3V ± 0.3V		20.0		
						5V ± 0.5V		20.0		
State Machine										
t_{st_pw}	State transition pulse width					1.8V ± 0.09V		22.0		ns
						3.3V ± 0.3V		22.0		
						5V ± 0.5V		22.0		
t_{st_dly}	State transition delay					1.8V ± 0.09V		61.5		ns
						3.3V ± 0.3V		51.3		
						5V ± 0.5V		48.6		
Oscillator										
f_{err}	Oscillator frequency error				OSC0 2kHz	1.8V ± 0.09V	-5.0		7.0	%
						3.3V ± 0.3V	-5.5		6.0	
						5V ± 0.5V	-5.5		6.0	
					OSC1 2MHz	1.8V ± 0.09V	-8.4		11.3	%
						3.3V ± 0.3V	-9.5		11.0	
						5V ± 0.5V	-10.4		7.5	
					OSC2 25MHz	1.8V ± 0.09V	-5.8		3.6	%
						3.3V ± 0.3V	-4.4		4.6	
						5V ± 0.5V	-5.3		4.6	
t_{d_osc}	Oscillator startup delay				OSC0 2kHz	1.8V ± 0.09V		364.2		µs
						3.3V ± 0.3V		315.8		
						5V ± 0.5V		319.9		
t_{d_osc}	Oscillator startup delay				OSC1 2MHz, Bandgap force on	1.8V ± 0.09V		0.52		µs
						3.3V ± 0.3V		0.49		
						5V ± 0.5V		0.53		
t_{d_osc}	Oscillator startup delay				OSC2 25MHz, Bandgap force on	1.8V ± 0.09V		2.80		µs
						3.3V ± 0.3V		2.69		
						5V ± 0.5V		2.58		
t_{d_osc}	Oscillator startup delay				OSC2 25MHz, Fast startup enabled	1.8V ± 0.09V		0.38		µs
						3.3V ± 0.3V		0.37		
						5V ± 0.5V		0.34		
t_{d_bg}	Bandgap startup delay				Bandgap auto on	1.8V ± 0.09V		42.0		µs
						3.3V ± 0.3V		42.0		
						5V ± 0.5V		42.0		

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{set_osc}	Oscillator startup settling time				OSC0 2kHz	1.8V ± 0.09V		164.0		µs
						3.3V ± 0.3V		165.2		
						5V ± 0.5V		166.1		
					OSC1 2MHz	1.8V ± 0.09V		0.8		µs
						3.3V ± 0.3V		0.7		
						5V ± 0.5V		0.7		
					OSC2 25MHz	1.8V ± 0.09V		0.1		µs
						3.3V ± 0.3V		0.1		
						5V ± 0.5V		0.1		
t_{d_err}	Delay error				OSC (Forced power on)	1.71V to 5.5V	0		1	CLK cycle
Programmable Filter										
t_{pflt_pw}	Pulse width	Programmable filter - Edge detect mode	Rising edge of OUT	Falling edge of OUT	1 cell	1.8V ± 0.09V		138.2		ns
						3.3V ± 0.3V		138.1		
						5V ± 0.5V		138.3		
					2 cells	1.8V ± 0.09V		238.4		ns
						3.3V ± 0.3V		238.2		
						5V ± 0.5V		238.0		
					3 cells	1.8V ± 0.09V		336.9		ns
						3.3V ± 0.3V		336.4		
						5V ± 0.5V		336.6		
					4 cells	1.8V ± 0.09V		434.3		ns
						3.3V ± 0.3V		434.2		
						5V ± 0.5V		434.5		
t_{pflt_pd}	Delay	Programmable filter - Edge detect mode			Any cells	1.8V ± 0.09V		63.4		ns
						3.3V ± 0.3V		63.4		
						5V ± 0.5V		63.4		
t_{pflt_d}	Delay	Programmable filter - Both edge delay mode	Rising/Falling edge of IN	Rising/Falling edge of OUT	1 cell	1.8V ± 0.09V		153.4		ns
						3.3V ± 0.3V		153.5		
						5V ± 0.5V		153.6		
					2 cells	1.8V ± 0.09V		253.7		ns
						3.3V ± 0.3V		253.9		
						5V ± 0.5V		253.6		
					3 cells	1.8V ± 0.09V		352.4		ns
						3.3V ± 0.3V		352.2		
						5V ± 0.5V		352.7		
					4 cells	1.8V ± 0.09V		450.2		ns
						3.3V ± 0.3V		449.9		
						5V ± 0.5V		450.3		
Analog Multiplexer										
Frequency response (switch on)			Y or A, B	A, B or Y	R_L = 50Ω, f_{in} = sine wave	1.8V ± 0.09V		204		MHz
						2.5V ± 0.2V		205		
						3.3V ± 0.3V		207		
						5V ± 0.5V		211		

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Crosstalk (between switches)		A or B	B or A	R_L = 50Ω, f_{in} = 10MHz (sine wave)	1.8V ± 0.09V		-48.6		dB
					2.5V ± 0.2V		-48.3		
					3.3V ± 0.3V		-48.2		
					5V ± 0.5V		-48.0		
Feedthrough attentuation (switch off)		Y or A, B	A, B or Y	C_L = 5pF, R_L = 50Ω, f_{in} = 10MHz (sine wave)	1.8V ± 0.09V		-47.6		dB
					2.5V ± 0.2V		-47.7		
					3.3V ± 0.3V		-47.7		
					5V ± 0.5V		-47.7		
Charge injection		IN	Y	C_L = 0.1nF, R_L = 1MΩ	3.3V		1.2		pC
					5V		1.5		
Total harmonic distortion		Y or A, B	A, B or Y	V_I = 0.5 × V_{pp}, R_L = 600Ω, f_{in} = 600Hz to 20kHz (sine wave)	1.8V ± 0.09V		0.06		%
					2.5V ± 0.2V		0.03		
					3.3V ± 0.3V		0.015		
					5V ± 0.5V		0.45		
t_{pd}(2)	Delay	Y or A, B	A, B or Y		1.8V ± 0.09V			2.6	ns
					2.5V ± 0.2V			1.6	
					3.3V ± 0.3V			1.2	
					5V ± 0.5V			1.0	
t_{en}(3)	Enable time	IN	A or B		1.8V ± 0.09V	5.9		45.0	ns
					2.5V ± 0.2V	3.8		36.2	
					3.3V ± 0.3V	3.4		33.8	
					5V ± 0.5V	2.6		30.8	
t_{dis}(4)	Disable time				1.8V ± 0.09V	6.0		45.7	
					2.5V ± 0.2V	4.7		36.4	
					3.3V ± 0.3V	3.7		33.3	
					5V ± 0.5V	3.2		30.8	
t_{B-M}	Break-before-make time	IN	Y	IN = LOW to HIGH step A, B = V_{CC}/2, R_L = 50Ω, C_L = 35pF	1.8V ± 0.09V	2.8	4.1		ns
					2.5V ± 0.2V	2.1	2.6		
					3.3V ± 0.3V	1.5	2.1		
					5V ± 0.5V	1.0	1.5		

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.

5.8 I²C Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			STANDARD MODE (Sm)		FAST MODE (Fm)		FAST MODE PLUS (Fm+)		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	0	1000	kHz
t_{sch}	I²C clock high time		4		0.6		0.26		µs
t_{scl}	I²C clock low time		4.7		1.3		0.5		µs
t_{sp}	I²C spike time			50		50		50	ns
t_{sds}	I²C serial-data setup time		250		100		50		ns

over operating free-air temperature range (unless otherwise noted)

PARAMETER			STANDARD MODE (Sm)		FAST MODE (Fm)		FAST MODE PLUS (Fm+)		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{sdh}	I^2C serial-data hold time		0		0		0		ns
t_{icr}	I^2C input rise time			1000	20	300		120	ns
t_{icf}	I^2C input fall time			300	20 × (V_{CC} / 5.5V)	300	20 × (V_{CC} / 5.5V)	120	ns
t_{ocf}	I^2C output fall time	10-pF to 400-pF bus (Sm/Fm) 10-pF to 550-pF bus (Fm+)		300		300		120	ns
t_{buf}	I^2C bus free time between stop and start		4.7		1.3		0.5		µs
t_{sts}	I^2C start or repeated start condition setup		4.7		0.6		0.26		µs
t_{sth}	I^2C start or repeated start condition hold		4		0.6		0.26		µs
t_{sps}	I^2C stop condition setup		4		0.6		0.26		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45		0.9		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45		0.9		0.45	µs
C_b	I^2C bus capacitive load			400		400		550	pF

5.9 SPI Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK, SPI clock frequency				4	MHz
t_{SCLK}	SCLK, SPI clock period		250			ns
t_R	SDI, nCS, and SCLK signals rise time				40	ns
t_F	SDI, nCS, and SCLK signals fall time				40	ns
t_{SCLKH}	SCLK High time		125			ns
t_{SCLKL}	SCLK Low time		125			ns
t_{NCS_SU}	nCS setup time before rising edge of SCLK		100			ns
t_{NCS_HOLD}	nCS hold time after falling edge of SCLK		100			ns
t_{NCS_DIS}	nCS disable time		50			ns
t_{SDI_SU}	SDI setup time before rising edge of SCLK		50			ns
t_{SDI_HOLD}	SDI hold time after rising edge of SCLK		50			ns
t_{SDO_VALID}	Time from falling edge of SCLK to next SDO data				80	ns
t_{SDOR}	SDO rise time				40	ns
t_{SDOF}	SDO fall time				40	ns

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6 Typical Characteristics

T_A = 25°C

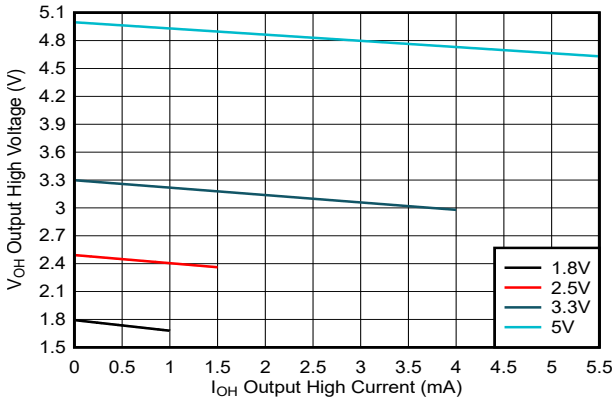


Figure 6-1. Typical 1X Push-Push Output Voltage in the High State (V_{OH})

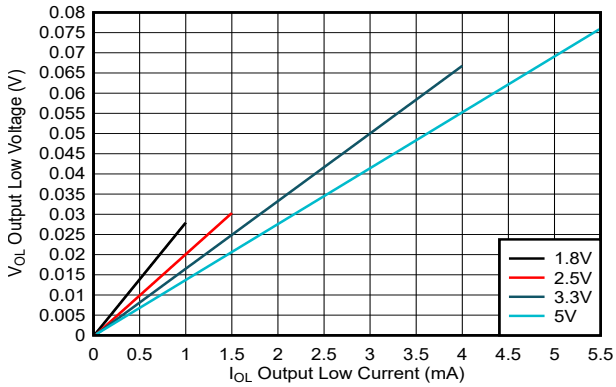


Figure 6-2. Typical 1X Push-Push Output Voltage in the Low State (V_{OL})

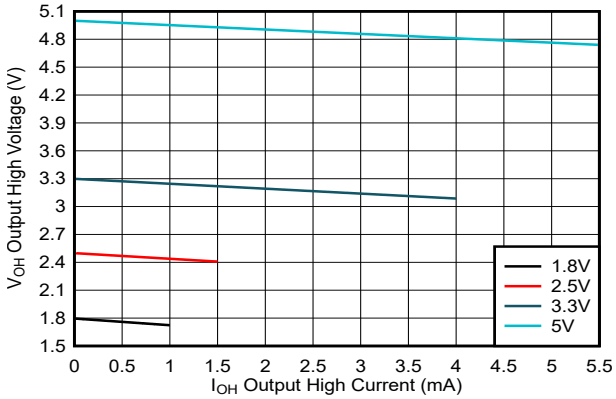


Figure 6-3. Typical 2X Push-Push Output Voltage in the High State (V_{OH})

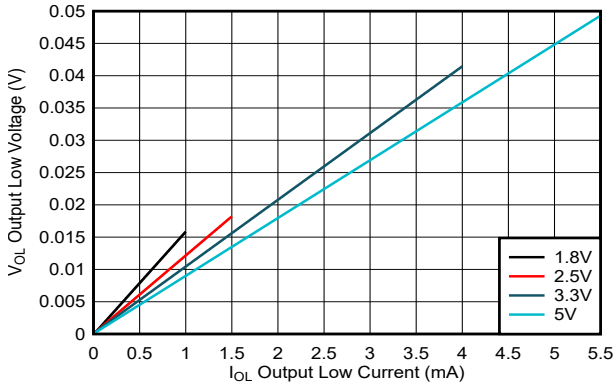


Figure 6-4. Typical 2X Push-Push Output Voltage in the Low State (V_{OL})

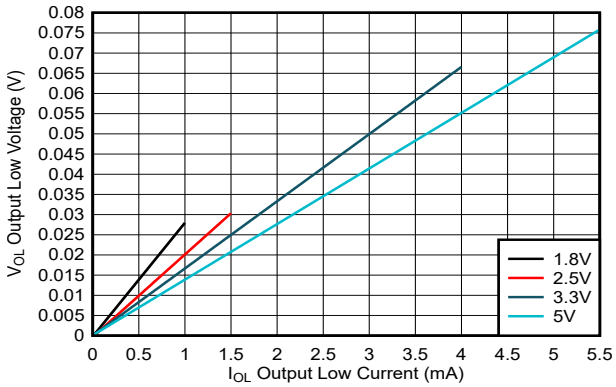


Figure 6-5. Typical 1X Open-Drain NMOS Output Voltage in the Low State (V_{OL})

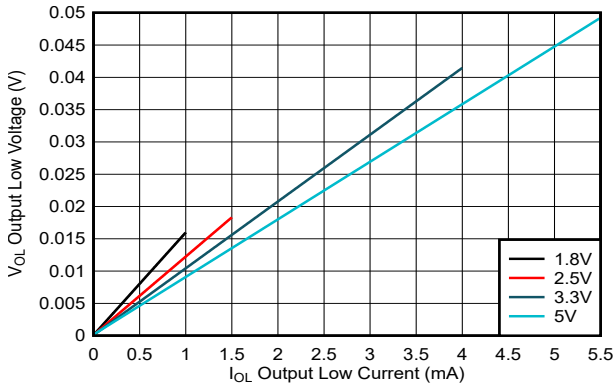


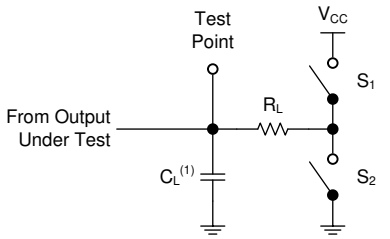
Figure 6-6. Typical 2X Open-Drain NMOS Output Voltage in the Low State (V_{OL})

7 Parameter Measurement Information

Phase relationships between waveforms are selected arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 5ns.

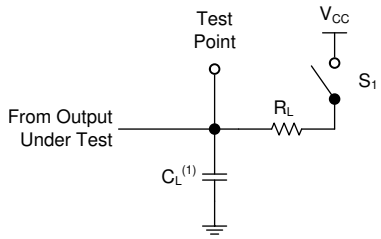
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



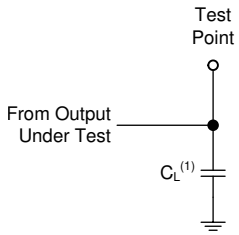
(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 7-2. Load Circuit for Open-Drain Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 7-3. Load Circuit for Push-Pull Outputs

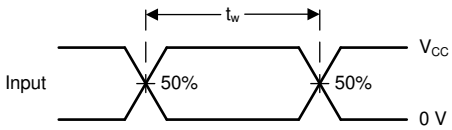


Figure 7-4. Voltage Waveforms, Pulse Duration

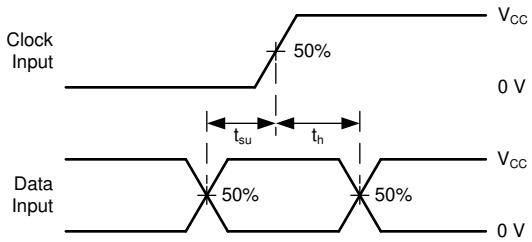


Figure 7-5. Voltage Waveforms, Setup and Hold Times

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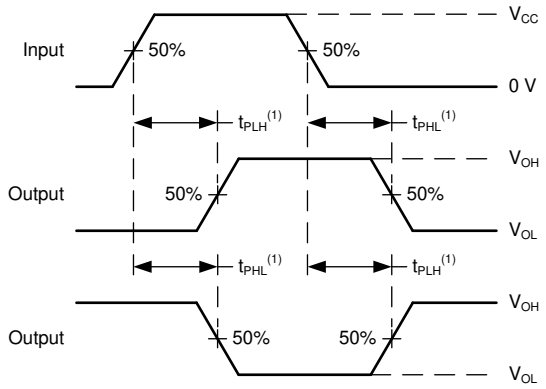
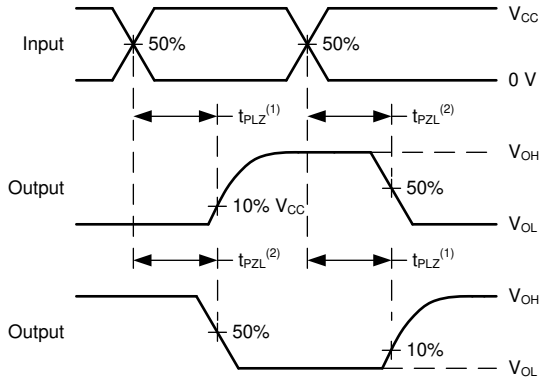


(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 7-6. Voltage Waveforms Propagation Delays



(1) The greater between t_{PLZ} and t_{PZL} is the same as t_{pd}.

Figure 7-8. Voltage Waveforms Propagation Delays

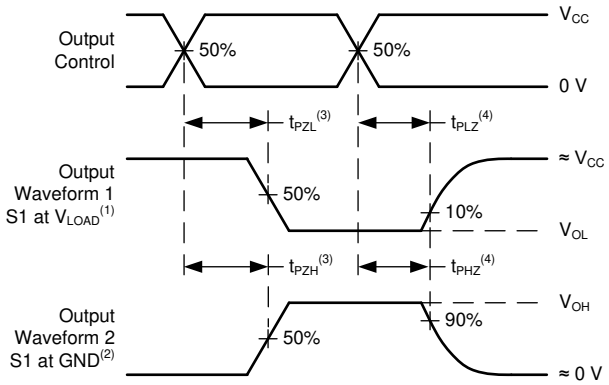
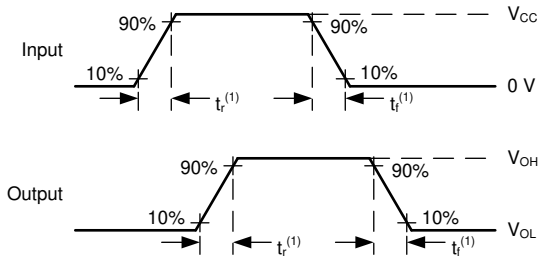
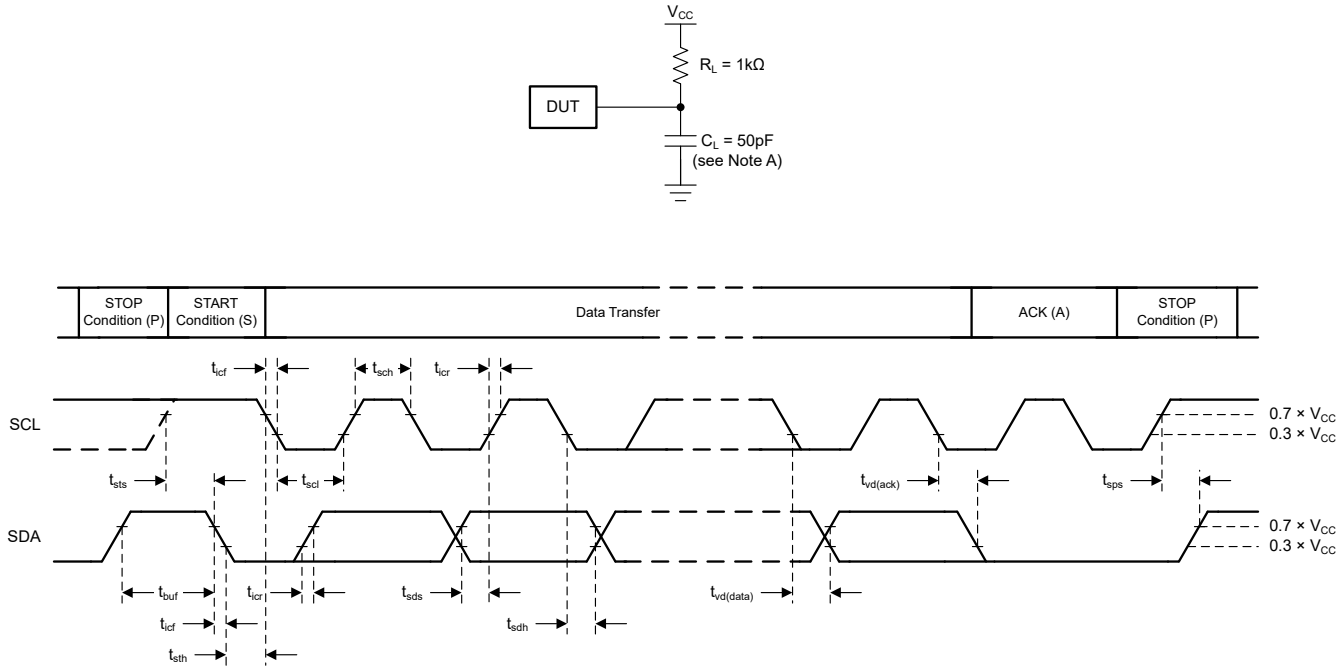


Figure 7-7. Voltage Waveforms Propagation Delays



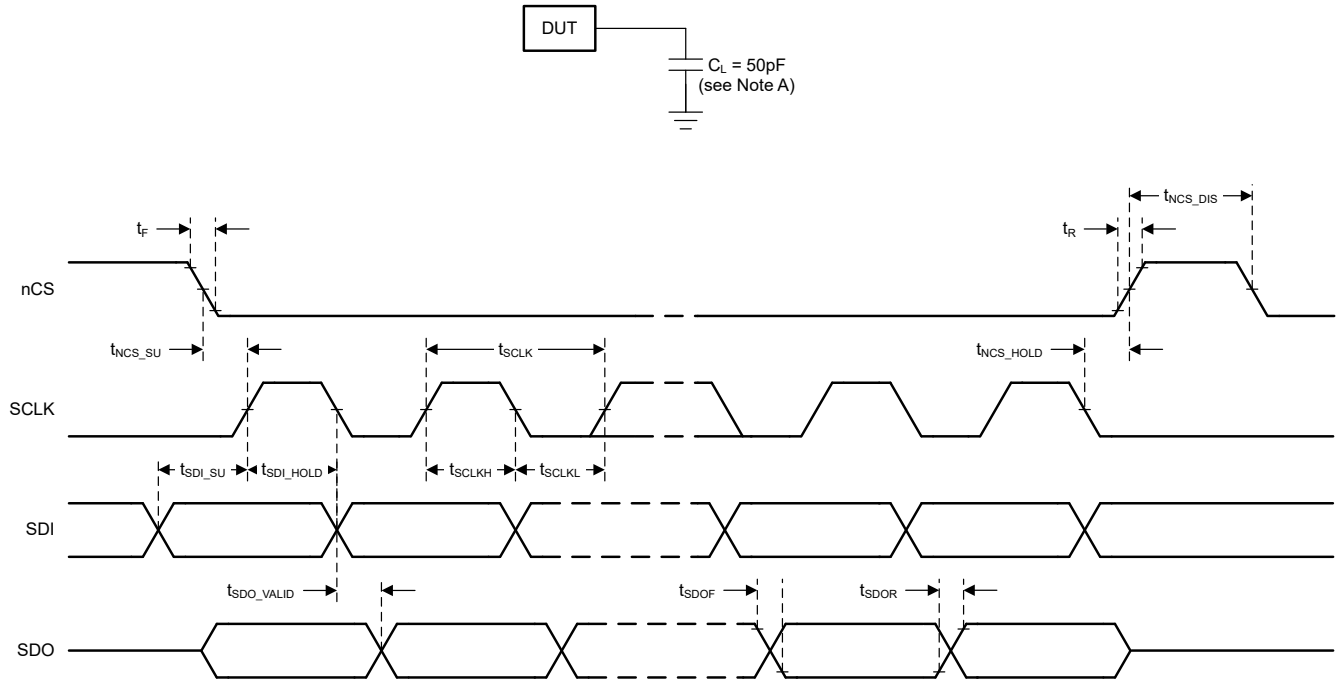
(1) The greater between t_r and t_f is the same as t_t.

Figure 7-9. Voltage Waveforms, Input and Output Transition Times



A. C_L include probe and jig capacitance.

Figure 7-10. I²C Interface Load Circuit and Voltage Waveforms



A. C_L include probe and jig capacitance.

Figure 7-11. SPI Interface Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

The TPLD2001-Q1 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks to provide an integrated, compact, low power solution to implement common system functions.

The TPLD2001-Q1 has seventeen GPIOs and one GPI that can be configured as digital inputs, digital outputs, digital input/outputs, or analog input/outputs.

The TPLD2001-Q1 has a system of interconnects, further referred to as the connection mux, to configure the routing of internal macro-cells and I/O pins. Each connection mux input is hardwired to a specific digital macro-cell output, such as digital I/O, lookup tables, and analog comparator outputs. The connection mux allows each of the digital inputs to only connect to one output so that bus contention does not occur.

The TPLD2001-Q1 features the following macro-cells:

- Fourteen configurable use logic blocks to implement combinational or sequential logic
  - Three selectable 2-bit LUT or D flip-flop/latch
  - One selectable 2-bit LUT or Pattern generator
  - Two selectable 3-bit LUT or D flip-flop/latch
  - Four selectable 3-bit LUT or D flip-flop/latch or shift register
  - Four selectable 4-bit LUT or D flip-flop/latch
- Six configurable logic and timing blocks
  - Four 3-bit LUT or D flip-flop/latch and/or 8-bit counter
  - Two 3-bit LUT or D flip-flop/latch and/or 16-bit counter
- Two programmable deglitch filter or edge detector
- One deglitch filter or edge detector
- One 8-state state machine, asynchronous or synchronous mode
- Four 8-bit counter/finite state machine
- Four PWM generators
- One watchdog timer
- Four discrete analog comparators
- One multi-channel analog comparator with integrated sampling engine and multi-voltage reference selection
- Internal voltage reference
- Analog temperature sensor
- Two break-before-make analog multiplexers
- Three oscillators: 2kHz, 2MHz, and 25MHz
- One serial communication: selectable between I^2C or SPI

InterConnect Studio enables a simple drag-and-drop interface to build custom circuit designs and configure the macro-cells, I/O pins, and interconnections by writing the configuration registers (volatile memory) or loading from the one-time programmable (OTP) non-volatile memory. In addition to circuit creation, InterConnect Studio has the ability to simulate digital and analog functionality to verify designs and provide a typical power consumption estimate. Once circuit designs are finalized, the OTP can be written to and locked to prevent readback of its contents.

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8.2 Functional Block Diagram

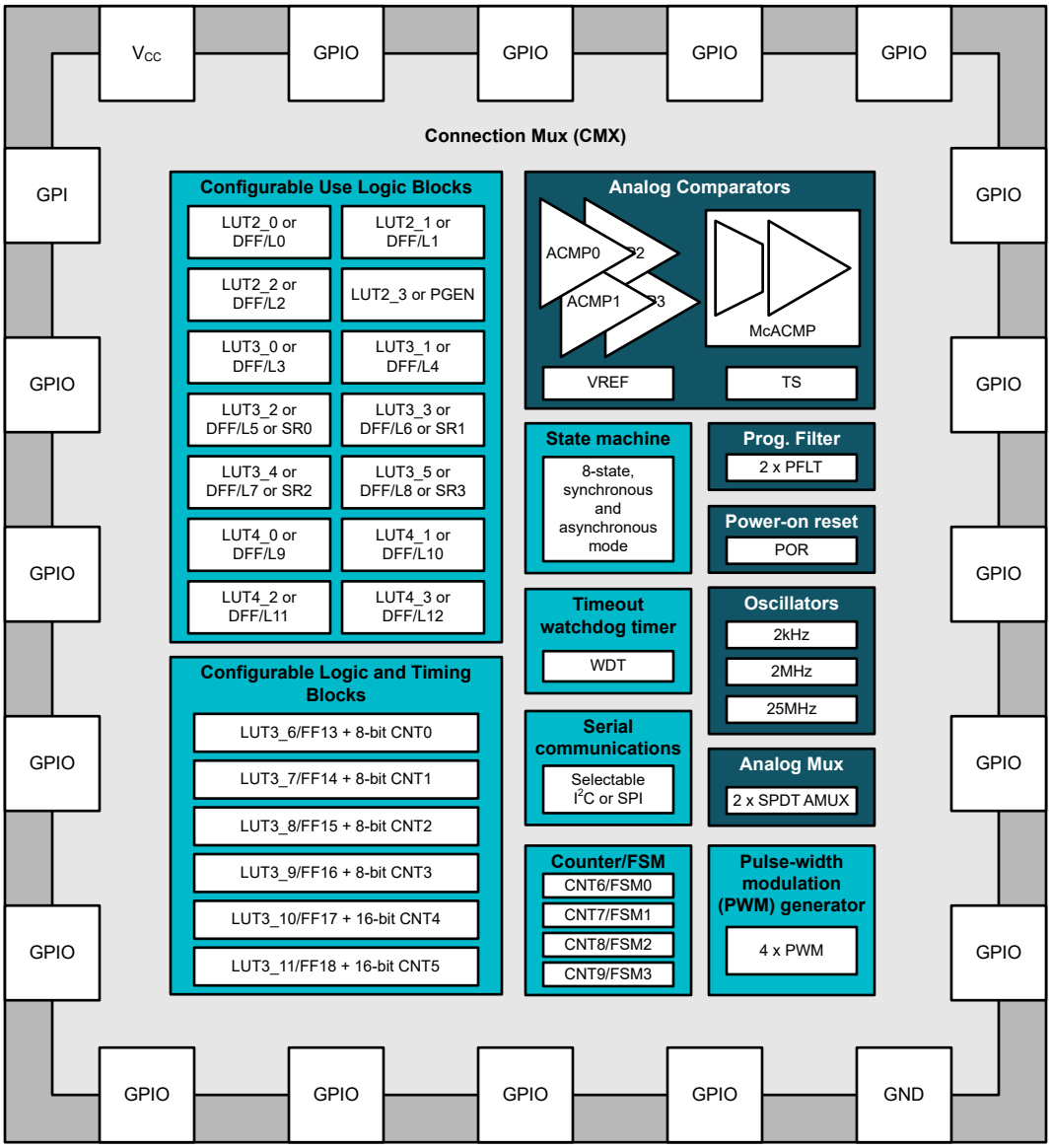

Figure 8-1. TPLD2001-Q1 Functional Block Diagram

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8.3 Feature Description

8.3.1 I/O Pins

TPLD2001-Q1 has one input and seventeen multifunction I/O pins. GPIO pins can function as either a user defined input, output, or a special function.

8.3.1.1 Input Modes

The following options are available when configuring pins as an input:

- Digital input without Schmitt-trigger
- Digital input with Schmitt-trigger
- Low-voltage digital input

The low-voltage digital input has lower V_{IH}/V_{IL} specifications than the digital input without Schmitt trigger. This allows for up-translation from any voltage domain lower than V_{CC} that meets the low-voltage digital input V_{IH} and V_{IL} specifications.

In addition to digital input options, several IOs can serve a special function. Three IOs can be used as an external oscillator input.

- IO14: OSC0 external clock
- IO15: OSC1 external clock
- IO17: OSC2 external clock

Several IOs can also be configured to serve as analog inputs to the internal analog comparators.

- IO4: ACMP IN0
- IO16: ACMP IN1
- IO1: ACMP IN2
- IO2: ACMP IN3
- IO9: External VREF IN
- IO10: McACMP IN0
- IO11: McACMP IN1
- IO12: McACMP IN2
- IO13: McACMP IN3

Three IOs can also be configured as bidirectional analog pins for the internal break-before-make analog multiplexer.

- IO1: AMUX0A
- IO2: AMUX0B
- IO3: AMUX0Y
- IO14: AMUX1A
- IO15: AMUX1B
- IO17: AMUX1Y

8.3.1.2 Output Modes

The following options are available with programmable drive strengths when configuring pins as an output:

- Push-pull output
- Open-drain NMOS output

8.3.1.3 Pull-Up or Pull-Down Resistors

All I/O pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10kΩ, 100kΩ and 1MΩ. The internal resistors can be configured as either pull-up or pull-down. When designing in InterConnect Studio, any pin left unused in a design are configured with a 1MΩ pull-down by default. Furthermore, following a power-on event, all ports are in a Hi-Z state until the power-on reset sequence has completed.

Table 8-1. Pin Configuration Options

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IN0	Pin not used	—	—	Pull Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low voltage digital input	Floating	—
				Pull Down Pull Up	10k 100k 1M
IO6, IO7	Pin not used	—	—	Pull Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low voltage digital input	Floating	—
				Pull Down Pull Up	10k 100k 1M
	Digital output	1	Push pull (1X, 2X) Open drain NMOS (1X, 4X)	Floating	—
				Pull Down Pull Up	10k 100k 1M
IO1, IO2, IO3, IO10, IO11, IO12, IO13, IO15, IO16, IO17	Pin not used	—	—	Pull Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low voltage digital input	Floating	—
				Pull Down Pull Up	10k 100k 1M
	Digital output	1	Push pull (1X, 2X)	Floating	—
			Open drain NMOS (1X, 2X) 3-state output (1X, 2X)	Pull Down Pull Up	10k 100k 1M
	Digital input/output	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low voltage digital input	Floating	—
				Pull Down Pull Up	10k 100k 1M
		1	Push pull (1X, 2X) Open drain NMOS (1X, 2X)		
	Analog input/output	—	Analog input/output	Floating	—
				Pull Down Pull Up	10k 100k 1M

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Table 8-1. Pin Configuration Options (continued)

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IO5, IO8	Pin not used	—	—	Pull Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low voltage digital input	Floating	—
				Pull Down Pull Up	10k 100k 1M
	Digital output	1	Push pull (1X, 2X)	Floating	—
			Open drain NMOS (1X, 2X)	Pull Down Pull Up	10k 100k 1M
IO4, IO9, IO14	Pin not used	—	—	Pull Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low voltage digital input	Floating	—
				Pull Down Pull Up	10k 100k 1M
	Digital output	1	Push pull (1X, 2X)	Floating	—
			Open drain NMOS (1X, 2X)	Pull Down Pull Up	10k 100k 1M
	Analog input/output	—	Analog input/output	Floating	—
				Pull Down Pull Up	10k 100k 1M

Note

When using an IO with output-enable (OE) controlled from the CMX, configured as a Digital output with 3-state output, it is recommended to configure the input mode to Analog input/output.

8.3.2 Connection Mux

The connection mux is used to create the internal routing for internal functions of the device once the device is programmed. The registers are programmed from the one-time programmable memory (OTP).

The output of each functional macro-cell within the TPLD2001-Q1 has a specific digital bit code assigned to the output that is either set to active “High” or inactive “Low” based on the design that is created. Once the 2048 register bits within the TPLD2001-Q1 are programmed a fully custom circuit is created.

The connection mux has 83 inputs and 157 outputs. Each of the 83 inputs to the connection mux is hard-wired to a particular source macro-cell, including I/O pins, LUTs, analog comparators, other digital resources and V_{CC} and GND. The input to a digital macro-cell uses a 7-bit register to select one of these 83 input lines.

Table 8-2. Connection Mux Input Table

Connection Mux Input	Connection Mux Input Signal	Mux Decode						
		6	5	4	3	2	1	0
0	GND	0	0	0	0	0	0	0
1	IN0 DIN	0	0	0	0	0	0	1
2	IO1 DIN / VIRTUAL IN0	0	0	0	0	0	1	0

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Table 8-2. Connection Mux Input Table (continued)

Connection Mux Input	Connection Mux Input Signal	Mux Decode						
		6	5	4	3	2	1	0
3	IO2 DIN / VIRTUAL IN1	0	0	0	0	0	1	1
4	IO3 DIN / VIRTUAL IN2	0	0	0	0	1	0	0
5	IO4 DIN / VIRTUAL IN3	0	0	0	0	1	0	1
6	IO5 DIN / VIRTUAL IN4	0	0	0	0	1	1	0
7	IO6 DIN / VIRTUAL IN5	0	0	0	0	1	1	1
8	IO7 DIN / VIRTUAL IN6	0	0	0	1	0	0	0
9	IO8 DIN	0	0	0	1	0	0	1
10	IO9 DIN / VIRTUAL IN7	0	0	0	1	0	1	0
11	IO10 DIN	0	0	0	1	0	1	1
12	IO11 DIN	0	0	0	1	1	0	0
13	IO12 DIN	0	0	0	1	1	0	1
14	IO13 DIN	0	0	0	1	1	1	0
15	IO14 DIN	0	0	0	1	1	1	1
16	IO15 DIN	0	0	1	0	0	0	0
17	IO16 DIN	0	0	1	0	0	0	1
18	IO17 DIN	0	0	1	0	0	1	0
19	LUT2_0 / DFF OUT	0	0	1	0	0	1	1
20	LUT2_1 / DFF OUT	0	0	1	0	1	0	0
21	LUT2_2 / DFF OUT	0	0	1	0	1	0	1
22	LUT2_3 / PGEN OUT	0	0	1	0	1	1	0
23	LUT3_0 / DFF OUT	0	0	1	0	1	1	1
24	LUT3_1 / DFF OUT	0	0	1	1	0	0	0
25	LUT3_2 / DFF / SR OUT	0	0	1	1	0	0	1
26	LUT3_3 / DFF / SR OUT	0	0	1	1	0	1	0
27	LUT3_4 / DFF / SR OUT	0	0	1	1	0	1	1
28	LUT3_5 / DFF / SR OUT	0	0	1	1	1	0	0
29	LUT3_6 / LDC OUT	0	0	1	1	1	0	1
30	LUT3_7 / LDC OUT	0	0	1	1	1	1	0
31	LUT3_8 / LDC OUT	0	0	1	1	1	1	1
32	LUT3_9 / LDC OUT	0	1	0	0	0	0	0
33	LUT3_10 / LDC OUT	0	1	0	0	0	0	1
34	LUT3_11 / LDC OUT	0	1	0	0	0	1	0
35	LUT4_0 / DFF OUT	0	1	0	0	0	1	1
36	LUT4_1 / DFF OUT	0	1	0	0	1	0	0
37	LUT4_2 / DFF OUT	0	1	0	0	1	0	1
38	LUT4_3 / DFF OUT	0	1	0	0	1	1	0
39	PFLT0 OUT	0	1	0	0	1	1	1

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Table 8-2. Connection Mux Input Table (continued)

Connection Mux Input	Connection Mux Input Signal	Mux Decode						
		6	5	4	3	2	1	0
40	PFLT1 OUT	0	1	0	1	0	0	0
41	FLT / EDET OUT	0	1	0	1	0	0	1
42	SM OUT0	0	1	0	1	0	1	0
43	SM OUT1	0	1	0	1	0	1	1
44	SM OUT2	0	1	0	1	1	0	0
45	SM OUT3	0	1	0	1	1	0	1
46	SM OUT4	0	1	0	1	1	1	0
47	SM OUT5	0	1	0	1	1	1	1
48	SM OUT6	0	1	1	0	0	0	0
49	SM OUT7	0	1	1	0	0	0	1
50	ACMP0 OUT	0	1	1	0	0	1	0
51	ACMP1 OUT	0	1	1	0	0	1	1
52	ACMP2 OUT	0	1	1	0	1	0	0
53	ACMP3 OUT	0	1	1	0	1	0	1
54	McACMP CH0_0 OUT	0	1	1	0	1	1	0
55	McACMP CH0_1 OUT	0	1	1	0	1	1	1
56	McACMP CH1_0 OUT	0	1	1	1	0	0	0
57	McACMP CH1_1 OUT	0	1	1	1	0	0	1
58	McACMP CH2_0 OUT	0	1	1	1	0	1	0
59	McACMP CH2_1 OUT	0	1	1	1	0	1	1
60	McACMP CH3_0 OUT	0	1	1	1	1	0	0
61	McACMP CH3_1 OUT	0	1	1	1	1	0	1
62	McACMP DATA RDY	0	1	1	1	1	1	0
63	OSC0 OUT0	0	1	1	1	1	1	1
64	OSC0 OUT1	1	0	0	0	0	0	0
65	OSC1 OUT0	1	0	0	0	0	0	1
66	OSC1 OUT1	1	0	0	0	0	1	0
67	OSC2 OUT	1	0	0	0	0	1	1
68	CNT8 OUT	1	0	0	0	1	0	0
69	CNT9 OUT	1	0	0	0	1	0	1
70	CNT10 OUT	1	0	0	0	1	1	0
71	CNT11 OUT	1	0	0	0	1	1	1
72	PWM GEN0 OUTN	1	0	0	1	0	0	0
73	PWM GEN0 OUTP	1	0	0	1	0	0	1
74	PWM GEN1 OUTN	1	0	0	1	0	1	0
75	PWM GEN1 OUTP	1	0	0	1	0	1	1
76	PWM GEN2 OUTN	1	0	0	1	1	0	0

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Table 8-2. Connection Mux Input Table (continued)

Connection Mux Input	Connection Mux Input Signal	Mux Decode						
		6	5	4	3	2	1	0
77	PWM GEN2 OUTP	1	0	0	1	1	0	1
78	PWM GEN3 OUTN	1	0	0	1	1	1	0
79	PWM GEN3 OUTP	1	0	0	1	1	1	1
80	WDT OUT	1	0	1	0	0	0	0
81	POR OUT	1	0	1	0	0	0	1
82	Reserved[1]	1	0	1	0	0	1	0
...	...	...	...	...	...	...	...	...
126	Reserved[1]	1	1	1	1	1	1	0
127	VCC	1	1	1	1	1	1	1

1. Reserved options are internally connected to VCC.

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Table 8-3. Connection mux output table

Connection mux output	Connection mux output signal
0	IO1 DOUT
1	IO1 OE
2	IO2 DOUT
3	IO2 OE
4	IO3 DOUT
5	IO3 OE
6	IO4 DOUT
7	IO5 DOUT
8	IO6 DOUT
9	IO7 DOUT
10	IO8 DOUT
11	IO9 DOUT
12	IO10 DOUT
13	IO10 OE
14	IO11 DOUT
15	IO11 OE
16	IO12 DOUT
17	IO12 OE
18	IO13 DOUT
19	IO13 OE
20	IO14 DOUT
21	IO15 DOUT
22	IO15 OE
23	IO16 DOUT
24	IO16 OE
25	IO17 DOUT
26	IO17 OE
27	LUT2_0 IN0 / DFF CLK IN
28	LUT2_0 IN1 / DFF D IN
29	LUT2_1 IN0 / DFF CLK IN
30	LUT2_1 IN1 / DFF D IN
31	LUT2_2 IN0 / DFF CLK IN
32	LUT2_2 IN1 / DFF D IN
33	LUT2_3 IN0 / PGEN CLK IN
34	LUT2_3 IN1 / PGEN RST IN
35	LUT3_0 IN0 / DFF CLK IN
36	LUT3_0 IN1 / DFF D IN
37	LUT3_0 IN2 / DFF RST IN
38	LUT3_1 IN0 / DFF CLK IN
39	LUT3_1 IN1 / DFF D IN
40	LUT3_1 IN2 / DFF RST IN
41	LUT3_2 IN0 / DFF / SR CLK IN
42	LUT3_2 IN1 / DFF / SR D IN
43	LUT3_2 IN2 / DFF / SR RST IN
44	LUT3_3 IN0 / DFF / SR CLK IN

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Table 8-3. Connection mux output table (continued)

Connection mux output	Connection mux output signal
45	LUT3_3 IN1 / DFF / SR D IN
46	LUT3_3 IN2 / DFF / SR RST IN
47	LUT3_4 IN0 / DFF / SR CLK IN
48	LUT3_4 IN1 / DFF / SR D IN
49	LUT3_4 IN2 / DFF / SR RST IN
50	LUT3_5 IN0 / DFF / SR CLK IN
51	LUT3_5 IN1 / DFF / SR D IN
52	LUT3_5 IN2 / DFF / SR RST IN
53	LUT3_6 IN0 / DFF CLK IN OR LDC IN0
54	LUT3_6 IN1 / DFF D IN OR LDC IN1
55	LUT3_6 IN2 / DFF RST IN OR LDC IN2
56	LUT3_7 IN0 / DFF CLK IN OR LDC IN0
57	LUT3_7 IN1 / DFF D IN OR LDC IN1
58	LUT3_7 IN2 / DFF RST IN OR LDC IN2
59	LUT3_8 IN0 / DFF CLK IN OR LDC IN0
60	LUT3_8 IN1 / DFF D IN OR LDC IN1
61	LUT3_8 IN2 / DFF RST IN OR LDC IN2
62	LUT3_9 IN0 / DFF CLK IN OR LDC IN0
63	LUT3_9 IN1 / DFF D IN OR LDC IN1
64	LUT3_9 IN2 / DFF RST IN OR LDC IN2
65	LUT3_10 IN0 / DFF CLK IN OR LDC IN0
66	LUT3_10 IN1 / DFF D IN OR LDC IN1
67	LUT3_10 IN2 / DFF RST IN OR LDC IN2
68	LUT3_11 IN0 / DFF CLK IN OR LDC IN0
69	LUT3_11 IN1 / DFF D IN OR LDC IN1
70	LUT3_11 IN2 / DFF RST IN OR LDC IN2
71	LUT4_0 IN0 / DFF CLK IN
72	LUT4_0 IN1 / DFF D IN
73	LUT4_0 IN2 / DFF RST IN
74	LUT4_0 IN3
75	LUT4_1 IN0 / DFF CLK IN
76	LUT4_1 IN1 / DFF D IN
77	LUT4_1 IN2 / DFF RST IN
78	LUT4_1 IN3
79	LUT4_2 IN0 / DFF CLK IN
80	LUT4_2 IN1 / DFF D IN
81	LUT4_2 IN2 / DFF RST IN
82	LUT4_2 IN3
83	LUT4_3 IN0 / DFF CLK IN
84	LUT4_3 IN1 / DFF D IN
85	LUT4_3 IN2 / DFF RST IN
86	LUT4_3 IN3
87	PFLT0 IN
88	PFLT1 IN
89	FLT / EDET IN

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Table 8-3. Connection mux output table (continued)

Connection mux output	Connection mux output signal
90	SM ST0 EN0
91	SM ST0 EN1
92	SM ST0 EN2
93	SM ST1 EN0
94	SM ST1 EN1
95	SM ST1 EN2
96	SM ST2 EN0
97	SM ST2 EN1
98	SM ST2 EN2
99	SM ST3 EN0
100	SM ST3 EN1
101	SM ST3 EN2
102	SM ST4 EN0
103	SM ST4 EN1
104	SM ST4 EN2
105	SM ST5 EN0
106	SM ST5 EN1
107	SM ST5 EN2
108	SM ST6 EN0
109	SM ST6 EN1
110	SM ST6 EN2
111	SM ST7 EN0
112	SM ST7 EN1
113	SM ST7 EN2
114	SM CLK IN
115	SM RST IN
116	ACMP0 PWR UP
117	ACMP1 PWR UP
118	ACMP2 PWR UP
119	ACMP3 PWR UP
120	McACMP ENABLE
121	McACMP RST
122	OSC0 PWR DOWN
123	OSC1 PWR DOWN
124	OSC2 PWR DOWN
125	CNT6 / FSM IN
126	CNT6 / FSM UP
127	CNT6 / FSM KEEP
128	CNT6 / FSM CLK IN
129	CNT7 / FSM IN
130	CNT7 / FSM UP
131	CNT7 / FSM KEEP
132	CNT7 / FSM CLK IN
133	CNT8 / FSM IN
134	CNT8 / FSM UP

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Table 8-3. Connection mux output table (continued)

Connection mux output	Connection mux output signal
135	CNT8 / FSM KEEP
136	CNT8 / FSM CLK IN
137	CNT9 / FSM IN
138	CNT9 / FSM UP
139	CNT9 / FSM KEEP
140	CNT9 / FSM CLK IN
141	PWM GEN0 PWR UP
142	PWM GEN1 PWR UP
143	PWM GEN2 PWR UP
144	PWM GEN3 PWR UP
145	WDT EN
146	WDT IN
147	VIRTUAL OUT0
148	VIRTUAL OUT1
149	VIRTUAL OUT2
150	VIRTUAL OUT3
151	VIRTUAL OUT4
152	VIRTUAL OUT5
153	VIRTUAL OUT6
154	VIRTUAL OUT7
155	AMUX0_SEL
156	AMUX1_SEL

8.3.3 Configurable Use Logic Blocks

Combinational logic is supported via Look-up Tables (LUTs) within the TPLD2001-Q1. Inputs and outputs for the combination function macro-cells are configured from the connection mux with specific logic functions being defined by the state of OTP bits.

The TPLD2001-Q1 has fourteen configurable use logic blocks (macro-cells) that can serve as a combinational or sequential logic function. In each case, the macro-cells can serve as a Look-up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these logic blocks:

- Three selectable 2-input LUT or D flip-flop or latch (DFF/L)
- One selectable 2-input LUT or pattern generator (PGEN)
- Two selectable 3-input LUT or DFF/L with reset/set
- Four selectable 3-input LUT or DFF/L or Shift register (SR)
- Four selectable 4-input LUT or DFF/L with reset/set

8.3.3.1 2-Bit LUT or D Flip-Flop/Latch macro-cell

This configurable use logic block serves as either a 2-bit LUT or as a D flip-flop or latch.

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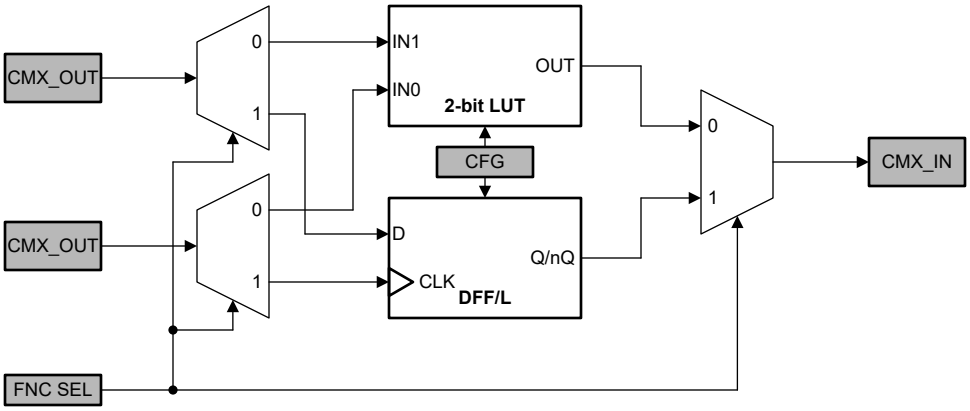

Figure 8-2. 2-bit LUT or DFF/Latch Block Diagram

8.3.3.1.1 2-Bit LUT

When used to implement LUT functions, the 2-bit LUT take in two input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 2-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses a 4-bit register to define the output function.

Table 8-4 shows the truth tables for the 2-bit LUT.

Table 8-4. 2-bit LUT Truth Table

IN1	IN0	OUT
0	0	
0	1	
1	0	
1	1	

8.3.3.1.2 D Flip-Flop/Latch

When used to implement a sequential logic element, the two input signals from the connection mux go to the data (D) and clock (CLK) inputs of the flip-flop or latch, with the output going back to the connection mux. This macro-cell has initial state parameters as well as clock and output polarity parameters that can be configured.

The operation of the D flip-flop/latch follows the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLK) or inverted (nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q does not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q does not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is Low).
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 8-5 and Table 8-6 show the truth tables for the D flip-flop and D latch, respectively.

Table 8-5. D Flip-Flop Truth Table

CLKPOL	CLK	D	Q	nQ
0	↓	0	Q_0	nQ_0
	↑	0	0	1
	↓	1	Q_0	nQ_0
	↑	1	1	0
1	↓	0	0	1
	↑	0	Q_0	nQ_0
	↓	1	1	0
	↑	1	Q_0	nQ_0

Table 8-6. D Latch Truth Table

CLKPOL	CLK	D	Q	nQ
0	0	0	0	1
	1	0	Q_0	nQ_0
	0	1	1	0
	1	1	Q_0	nQ_0
1	0	0	Q_0	nQ_0
	1	0	0	1
	0	1	Q_0	nQ_0
	1	1	1	0

8.3.3.2 2-Bit LUT or Pattern Generator macro-cell

This configurable use logic block serves as either a 2-bit LUT or as a Pattern generator.

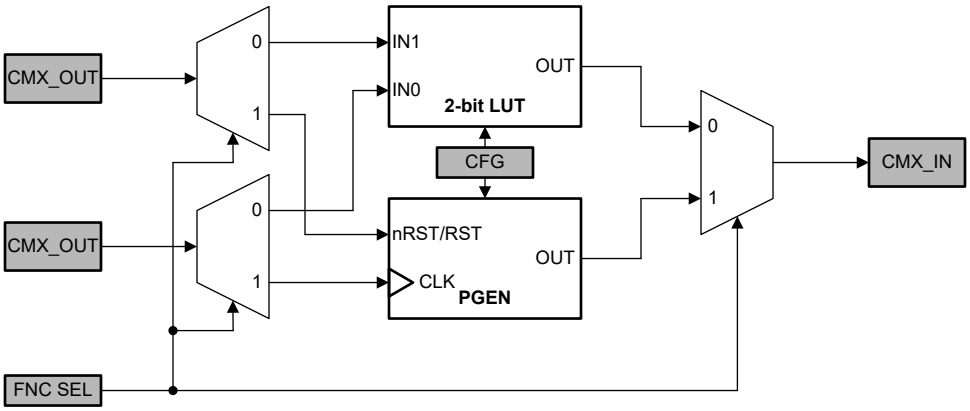

Figure 8-3. 2-bit LUT or Pattern Generator Block Diagram

8.3.3.2.1 2-Bit LUT

When used to implement LUT functions, the 2-bit LUT take in two input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 2-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses a 4-bit register to define the output function.

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Table 8-7 shows the truth tables for the 2-bit LUT.

Table 8-7. 2-bit LUT Truth Table

IN1	IN0	OUT
0	0	
0	1	
1	0	
1	1	

8.3.3.2.2 Pattern Generator

When configured as a Pattern generator, the two input signals from the connect mux go to the reset (nRST/RST) and clock (CLK) inputs of the pattern generator, with the output going back to the connection mux. This macro-cell has pattern size, bit pattern, and reset signal polarity parameters that can be configured to generate up to a 16-bit pattern that is clocked out continually on the rising edge of the CLK input as long as the macro-cell is not in reset. While in reset, the macro-cell continually outputs the first bit of the programmed bit pattern.

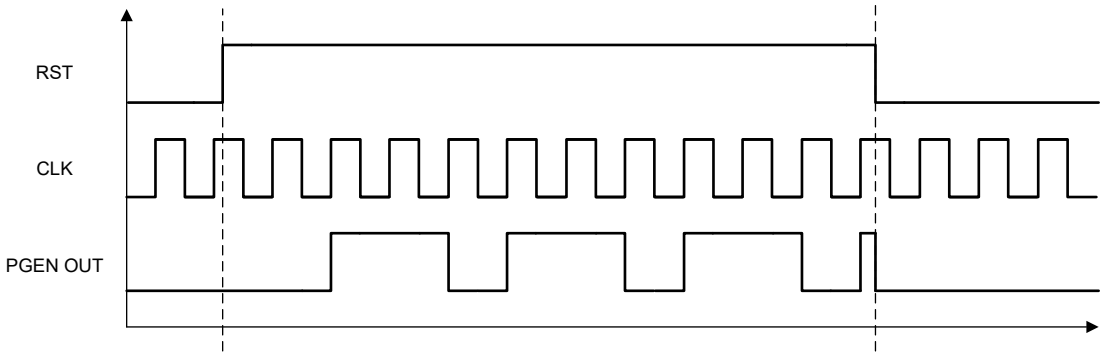

Figure 8-4. Pattern Generator Output Timing Diagram Example (SIZE = 3, PATTERN = 011, Low level RST)

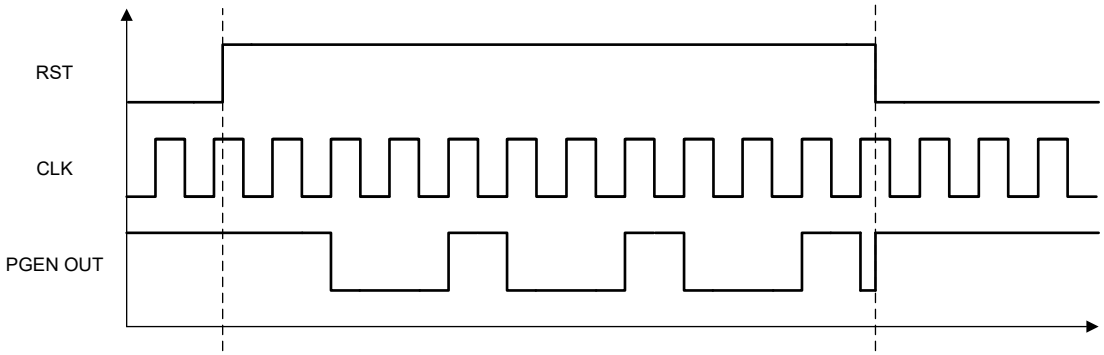

Figure 8-5. Pattern Generator Output Timing Diagram Example (SIZE = 3, PATTERN = 100, Low level RST)

The output pattern can be updated in-system using the User Registers. It is recommended to put the pattern generator in a reset state when updating the pattern registers to verify glitch-free loading of the data.

8.3.3.3 3-Bit LUT or D Flip-Flop/Latch With Reset/Set Macro-Cell

This configurable use logic block serves as either a 3-bit LUT or as a D flip-flop or latch with a reset or set.

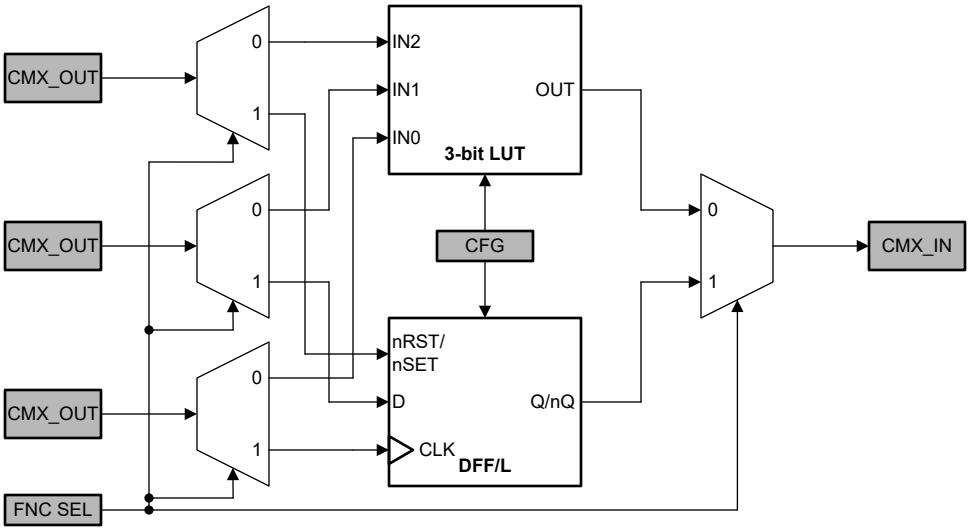

Figure 8-6. 3-bit LUT or DFF/Latch with nRST/nSET Block Diagram

8.3.3.3.1 3-bit LUT

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses an 8-bit register to define the output function.

Table 8-8 shows truth tables for the 3-bit LUT.

Table 8-8. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

8.3.3.3.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has user-configurable initial state, clock polarity, reset/set polarity, output stage select, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLK) or inverted (nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q does not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q does not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is Low).

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- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- These DFF/Latches have the option to further isolate the output from the input with the use of a second DFF/Latch sampling on the falling edge of CLK, or rising edge of nCLK, by enabling the "Dual Stage DFF" option.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 8-9 and Table 8-10 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

Table 8-9. D Flip-Flop with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	Q_0	nQ_0
			↑	0	0	1
			↓	1	Q_0	nQ_0
			↑	1	1	0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	0	1
			↑	0	Q_0	nQ_0
			↓	1	1	0
			↑	1	Q_0	nQ_0

Table 8-10. D Latch with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		0	0	0	1
			1	0	Q_0	nQ_0
			0	1	1	0
			1	1	Q_0	nQ_0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		0	0	Q_0	nQ_0
			1	0	0	1
			0	1	Q_0	nQ_0
			1	1	1	0

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8.3.3.4 3-Bit LUT or D Flip-Flop/Latch or Shift Register macro-cell

This configurable use logic block can serve as either a 3-bit LUT or as a D flip-flop or latch with a reset or set or an 8-bit Shift register.

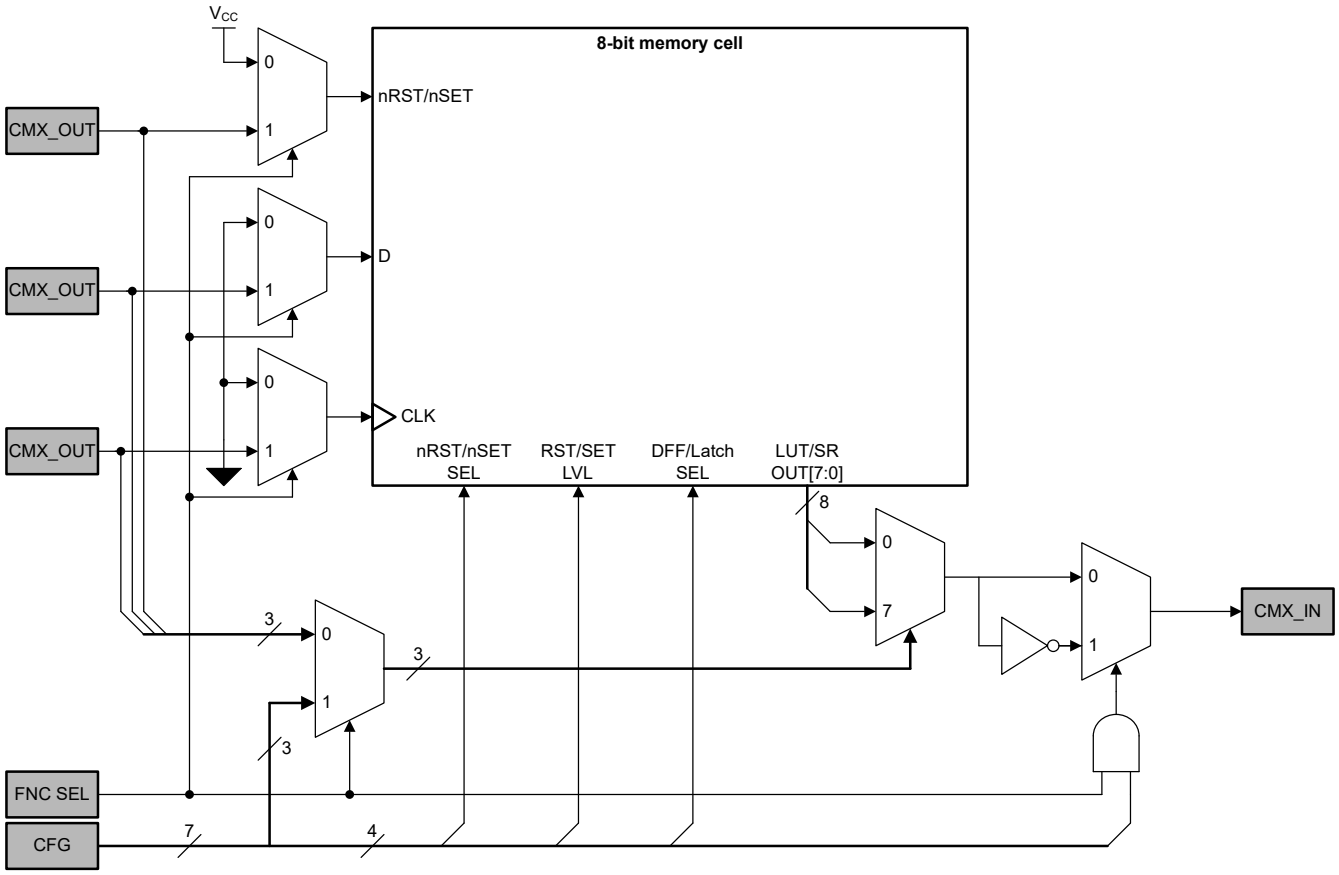

Figure 8-7. 3-bit LUT or DFF/Latch with nRST/nSET or 8-bit SISO Shift Register Block Diagram

8.3.3.4.1 3-bit LUT

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses an 8-bit register to define the output function.

Table 8-11 shows truth tables for the 3-bit LUT.

Table 8-11. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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8.3.3.4.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has user-configurable initial state, reset/set polarity, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 8-12 and Table 8-13 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

Table 8-12. D Flip-Flop with nRST/nSET truth table

nRST	nSET	CLK	D	Q	nQ
0	—	X	X	0	1
—	0	X	X	1	0
1	1	↓	0	Q_0	nQ_0
		↑	0	0	1
		↓	1	Q_0	nQ_0
		↑	1	1	0

Table 8-13. D Latch with nRST/nSET truth table

nRST	nSET	CLK	D	Q	nQ
0	—	X	X	0	1
—	0	X	X	1	0
1	1	0	0	0	1
		1	0	Q_0	nQ_0
		0	1	1	0
		1	1	Q_0	nQ_0

8.3.3.4.3 8-bit Shift Register

When used to implement a shift register, users can configure the initial state, reset/set polarity, output polarity, and register length. The register length can be set to a minimum of 2 and a maximum of 8.

Figure 8-8 shows an example of how the Shift register macro-cell operates.

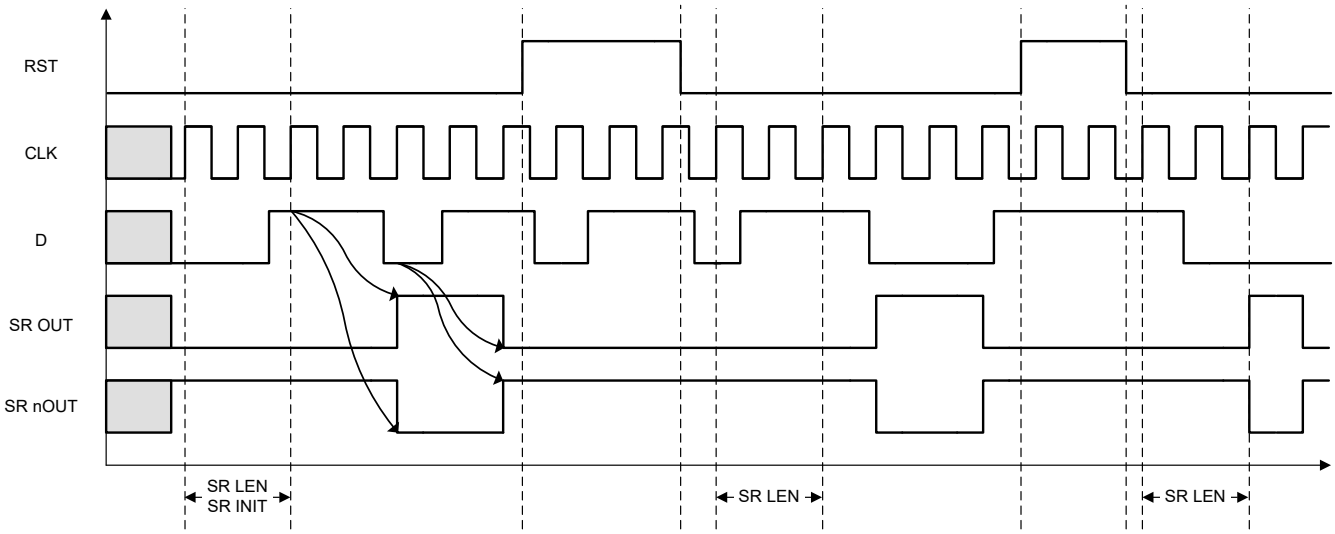

Figure 8-8. Shift Register Output Timing Diagram Example (INIT STATE = 00, REG LENGTH = 2, High level RST)

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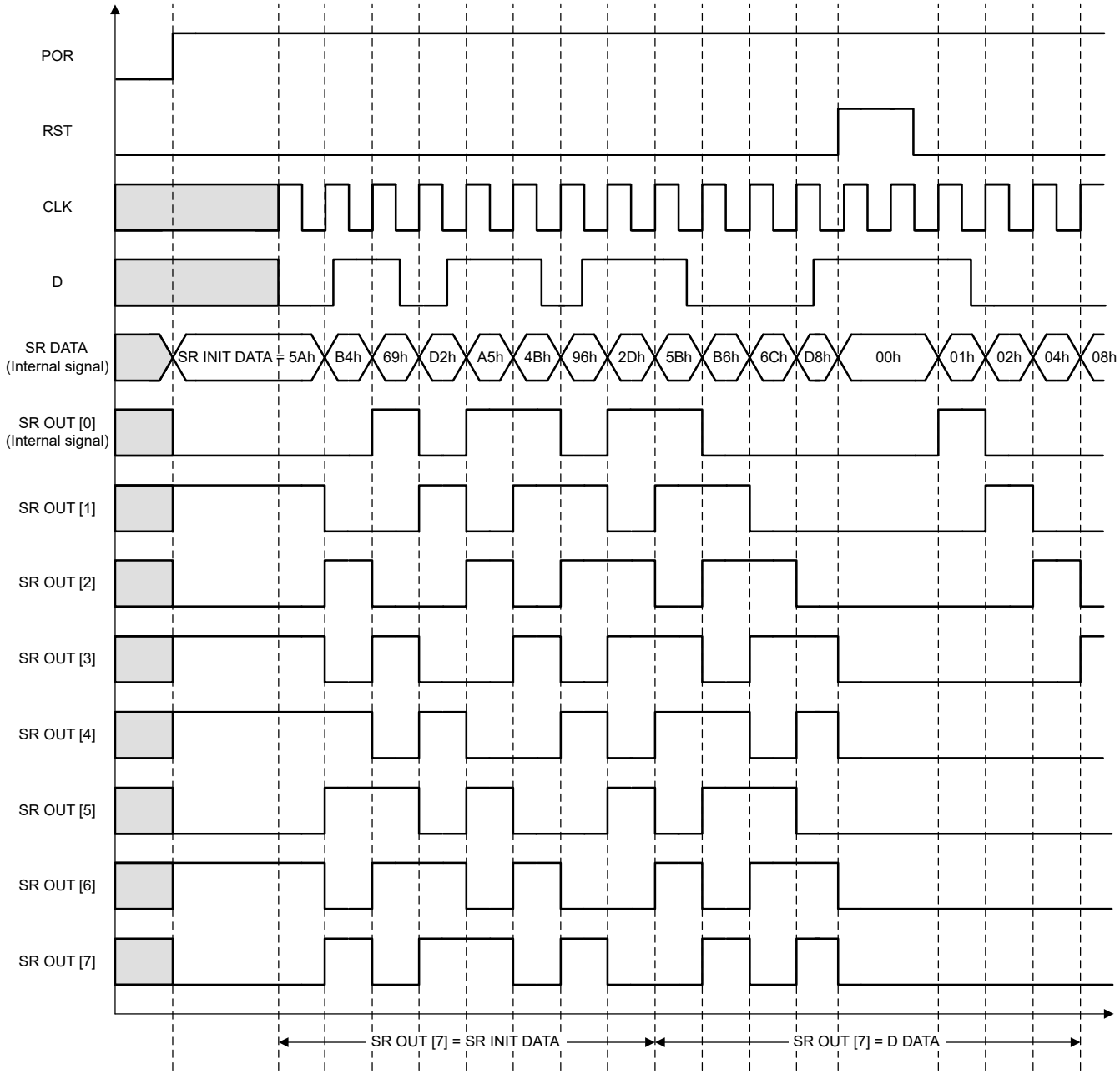

Figure 8-9. Shift Register Output Timing Diagram Example (INIT STATE = 5Ah, High level RST)

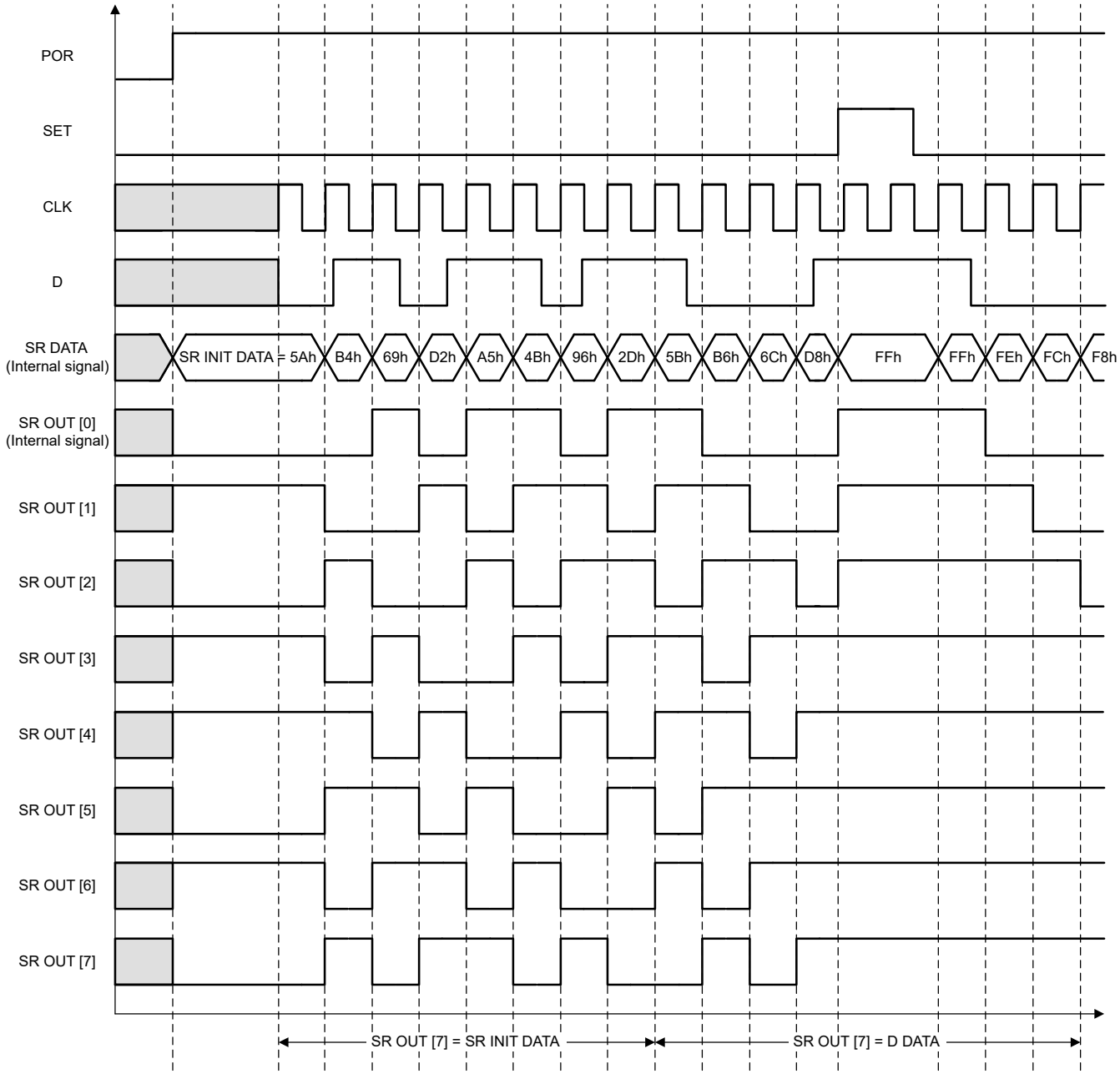

Figure 8-10. Shift Register Output Timing Diagram Example (INIT STATE = 5Ah, High level SET)

8.3.3.5 4-Bit LUT or D Flip-Flop/Latch with Reset/Set Macro-Cell

This configurable use logic block can serve as either a 4-bit LUT or as a D flip-flop or latch with a reset or set.

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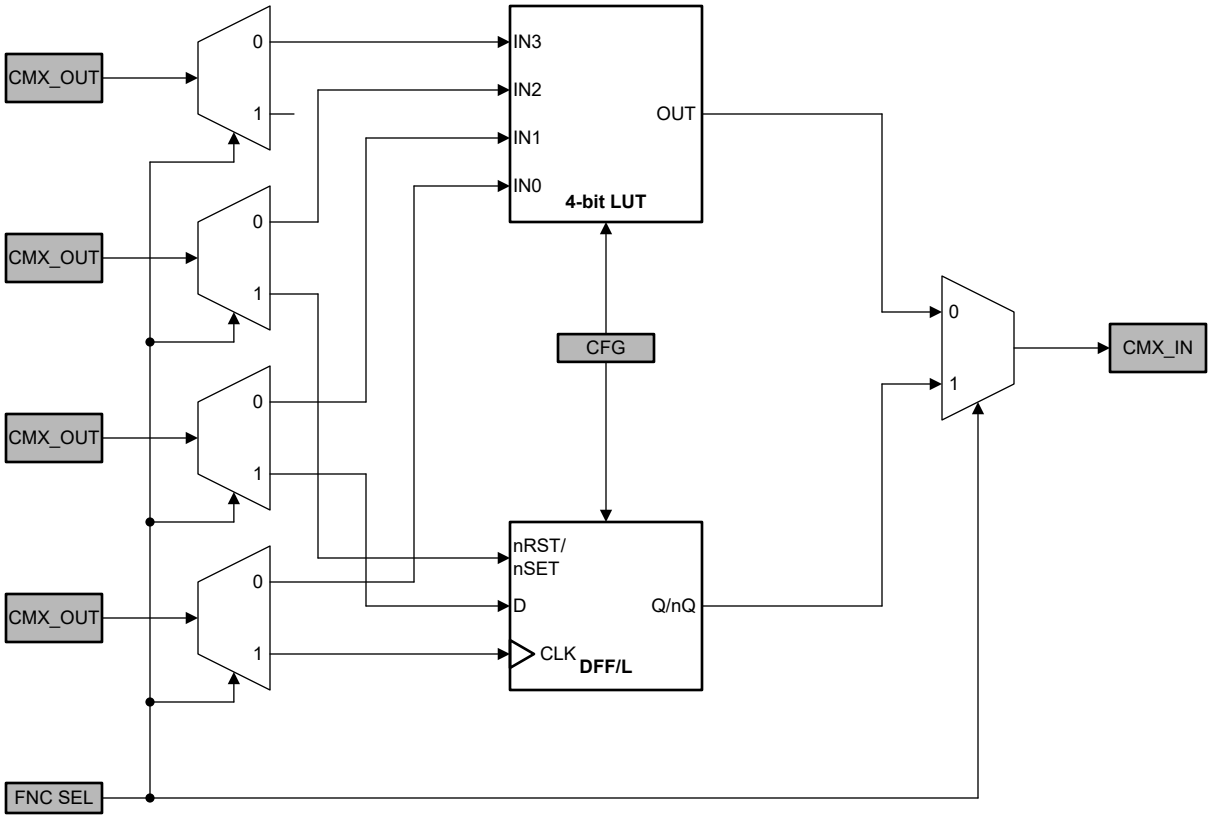

Figure 8-11. 4-bit LUT or DFF/Latch Block Diagram

8.3.3.5.1 4-bit LUT

When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection mux and produces a single output, which goes back into the connection mux. This LUT can be configured to any 4-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, this macro-cell uses a 16-bit register to define the output function.

Table 8-14 shows truth tables for the 4-bit LUT.

Table 8-14. 4-bit LUT Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

8.3.3.5.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has user-configurable initial state, clock polarity, reset/set polarity, output stage select, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLK) or inverted (nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q does not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q does not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is Low).
- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- These DFF/Latches have the option to further isolate the output from the input with the use of a second DFF/Latch sampling on the falling edge of CLK, or rising edge of nCLK, by enabling the "Dual Stage DFF" option.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 8-15 and Table 8-16 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

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Table 8-15. D Flip-Flop with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	Q_0	nQ_0
			↑	0	0	1
			↓	1	Q_0	nQ_0
			↑	1	1	0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	0	1
			↑	0	Q_0	nQ_0
			↓	1	1	0
			↑	1	Q_0	nQ_0

Table 8-16. D Latch with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		0	0	0	1
			1	0	Q_0	nQ_0
			0	1	1	0
			1	1	Q_0	nQ_0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		0	0	Q_0	nQ_0
			1	0	0	1
			0	1	Q_0	nQ_0
			1	1	1	0

8.3.4 Configurable Logic and Timing Blocks

The TPLD2001-Q1 has eight configurable logic and timing blocks (macro-cells) that can serve as a combinational or sequential logic function. The configurable logic and timing blocks can serve as a 3-bit LUT, D flip-flop with nRST/nSET, an 8-bit Counter/Delay generator, or a 16-bit Counter/Delay generator. These macro-cells also have the option to combine the previous functions, with a LUT/DFF output connected to the CNT/DLY input or a CNT/DLY output connected to any LUT/DFF input.

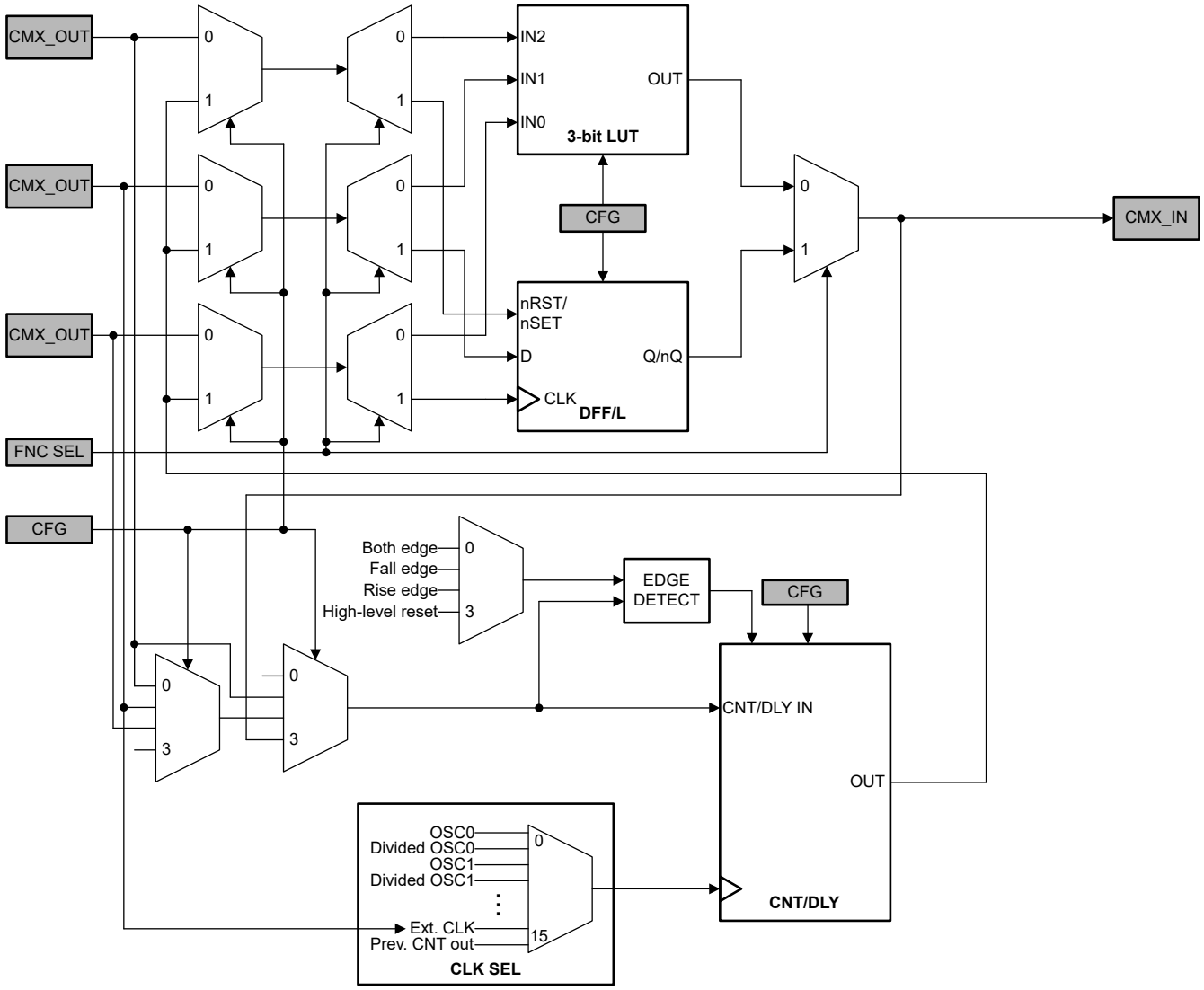

Figure 8-12. LUT/DFF + CNT/DLY Block Diagram

Table 8-17. LUT/DFF + CNT/DLY Connection Options

LDC_FS (1 bit)	LDC_CMX_IN_SEL (2 bits)	LDC_CMX_MODE (2 bits)	LDC IN0	LDC IN1	LDC IN2	LDC OUT
0	XX	00	LUT A	LUT B	LUT C	LUT OUT
1	XX	00	DFF CLK	DFF D	DFF RST	DFF OUT
X	XX	01	Unused	CNT Ext. CLK	CNT IN	CNT OUT
0	00	10	LUT A	LUT B	CNT IN	LUT OUT
0	01	10	LUT A	CNT IN	LUT C	LUT OUT
0	10	10	CNT IN	LUT B	LUT C	LUT OUT
1	00	10	DFF CLK	DFF D	CNT IN	DFF OUT
1	01	10	DFF CLK	CNT IN	DFF RST	DFF OUT
1	10	10	CNT IN	DFF D	DFF RST	DFF OUT
0	XX	11	LUT A	LUT B	LUT C	CNT OUT

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Table 8-17. LUT/DFF + CNT/DLY Connection Options (continued)

LDC_FS (1 bit)	LDC_CMX_IN_SEL (2 bits)	LDC_CMX_MODE (2 bits)	LDC IN0	LDC IN1	LDC IN2	LDC OUT
1	XX	11	DFF CLK	DFF D	DFF RST	CNT OUT

8.3.4.1 3-bit LUT

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses an 8-bit register to define the output function.

Table 8-18 shows truth tables for the 3-bit LUT.

Table 8-18. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

8.3.4.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has user-configurable initial state, reset/set polarity, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 8-19 and Table 8-20 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

Table 8-19. D Flip-Flop with nRST/nSET truth table

nRST	nSET	CLK	D	Q	nQ
0	—	X	X	0	1
—	0	X	X	1	0

Table 8-19. D Flip-Flop with nRST/nSET truth table (continued)

nRST	nSET	CLK	D	Q	nQ
1	1	↓	0	Q_0	nQ_0
		↑	0	0	1
		↓	1	Q_0	nQ_0
		↑	1	1	0

Table 8-20. D Latch with nRST/nSET truth table

nRST	nSET	CLK	D	Q	nQ
0	—	X	X	0	1
—	0	X	X	1	0
1	1	0	0	0	1
		1	0	Q_0	nQ_0
		0	1	1	0
		1	1	Q_0	nQ_0

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8.3.4.3 Counters/Delay Generators (CNT/DLY)

The TPLD2001-Q1 has four 8-bit and two 16-bit counters/delay generators, supporting a maximum DATA value of 255 and 65535, respectively. The counter count can be read and the data can be updated in-system using the User Registers. When reading the current count, two consecutive read transactions are required for accurate data read. TI recommends to put the counter in a reset state when updating the counter data registers to prevent glitches during loading of the data. Two clock pulses are required to release the counter from reset after writing new counter data.

For further flexibility, the clock source for each of these macro-cells can be configured as the internal oscillator (OSC0, OSC1, or OSC2), a divided clock derived from an oscillator (OSC0/8, /64, /512, /4096, /32768, /262144, or OSC1/8, /64, /512, or OSC2/4), or an external clock source coming from the connection mux. Note that the counter/delay macro-cell is rising edge triggered, that is the counter decrements on the rising edge of the CLK input.

Note

For unused counter macro-cells, TI recommends to set the clock selection (CLK_SEL) to External CLK from CMX.

Users can use the counter/delay generator macro-cell in the following modes: delay, one-shot, frequency comparator, counter, edge detector, delayed edge detector.

8.3.4.3.1 Delay Mode

When configured as a Delay generator (DLY), this macro-cell delays the input based on counter DATA and CLK input frequency and postpones rising and/or falling edges. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which to delay is selected by the Edge select parameter and can be configured as:

- Rising: only delay on rising edges of IN.
- Falling: only delay on falling edges of IN.
- Both: delay on both rising and falling edges of IN.

For delay applications, TI recommends to use larger counter data values for less error. If an input pulse width is shorter than the specified delay time, the pulse is filtered out. This feature can be useful for deglitching.

If the on-chip oscillator is used, a delay error or offset is introduced depending on whether the OSC is set to "forced power on" or "auto power on". An additional 2 clock cycles are included in the delay calculation for clock synchronization.

The delay time is calculated by:

$$\mathrm{DELAY} = \left[\mathrm{DATA} + \left(t_{d_er} \text{ or } t_{d_os}\right) + 2\right] \div f_{CLK} \tag{1}$$

When the OSC is set to "auto power on" and DLY macro-cells are triggered subsequently before the previous output is present, the OSC continues to clock and the DLY begins on the next rising edge. Thus, the subsequent delays can be calculated as if the OSC are set to "forced power on".

Figure 8-13 shows an example of the Delay macro-cell operation set to both edge delay and data = 1.

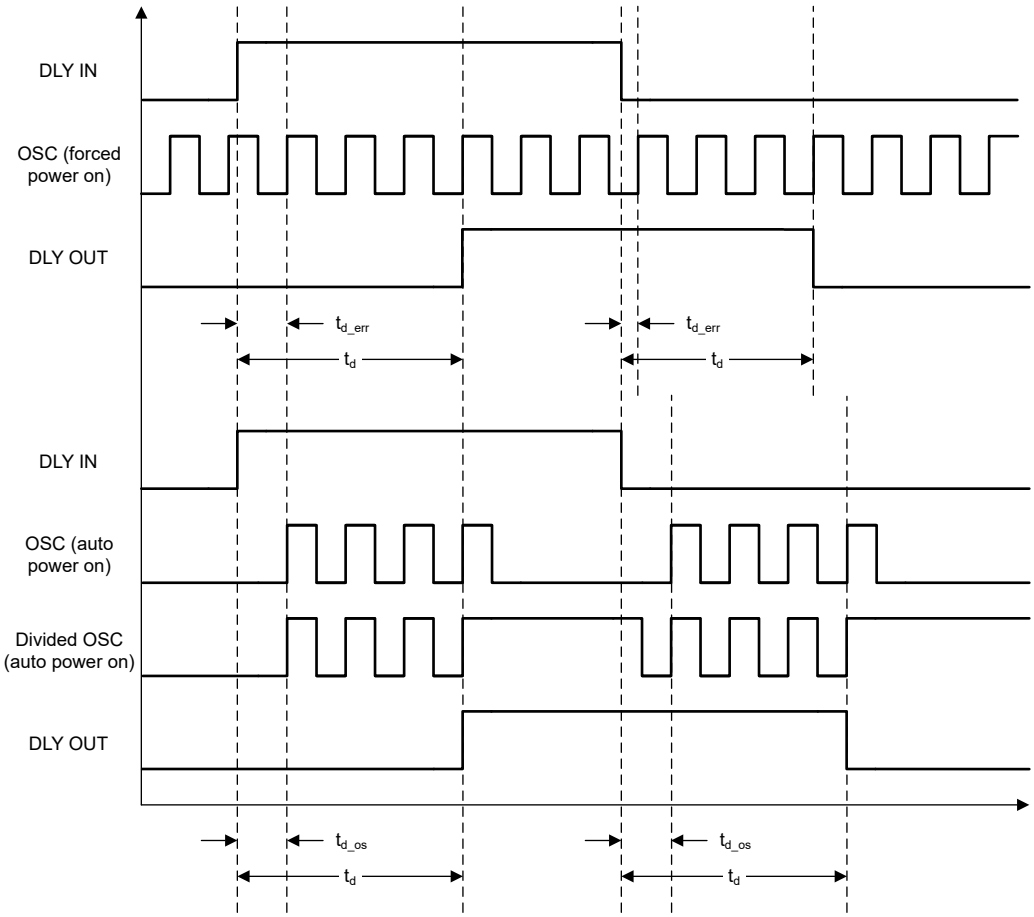

Figure 8-13. Delay Output Timing Example (Both Edge Delay and DATA = 1)

Figure 8-14 shows an example timing of Delay macro-cells with respect to the edge selected and data = 3.

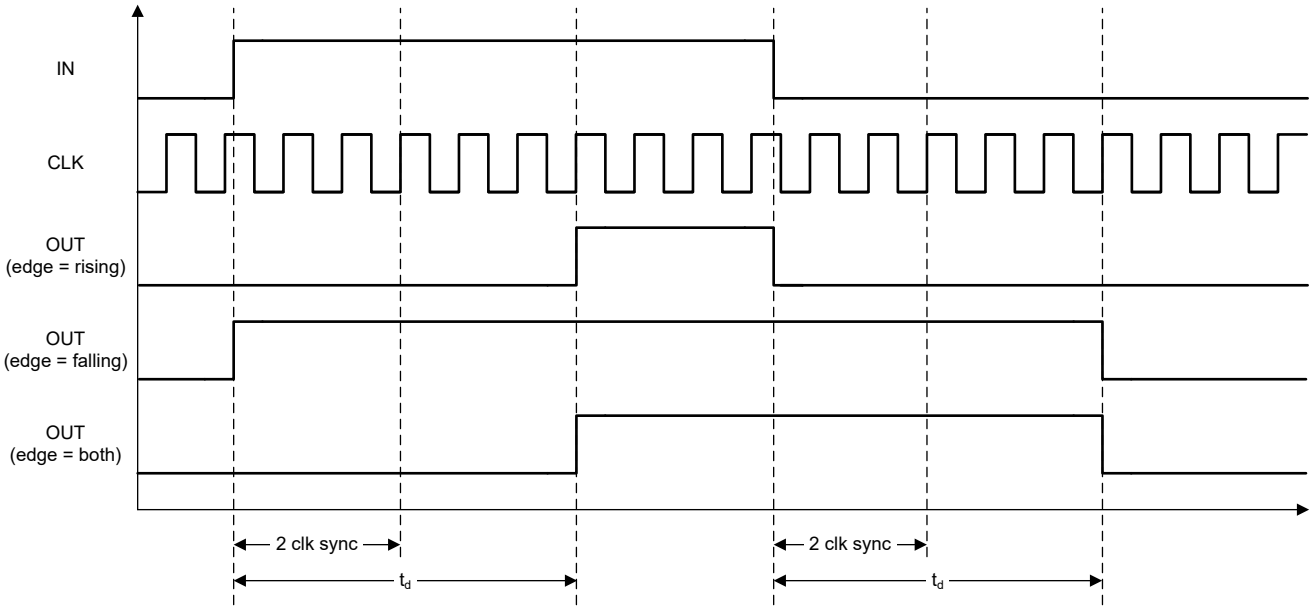

Figure 8-14. Delay Output Timing Example (DATA = 3)

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8.3.4.3.2 Reset Counter Mode

When configured as a Counter (CNT) and a valid edge appears on the IN input, this macro-cells resets the internal counter to 0 and begins counting down from DATA on the next rising clock edge. Then, the macro-cell outputs a pulse for the duration of one CLK period when the count reaches 0 and wrap around to the value in DATA. The counter continually operates until another reset is received. The edge on which the Counter is reset is determined by the Edge select parameter and can be configured as:

- Rising: only rising edges of IN reset the counter.
- Falling: only falling edges of IN reset the counter.
- Both: both rising and falling edges of IN reset the counter.
- High Level Reset: the counter is reset to 0 whenever IN is High; after reset, the counter output stays Low until the next rising CLK edge, then operates normally.

The counter time is calculated by:

$$\mathrm{COUNT} = [\mathrm{DATA} + 1] \div f_{\mathrm{CLK}} \tag{2}$$

After a reset, an additional 2 clock cycles is added for clock synchronization with an option to bypass. Note, bypassing the clock synchronization can result in the counter resetting to an unknown value.

Note

Counters are initialized with DATA = 0 after POR.

Figure 8-15 and Figure 8-16 show examples of Counter output timing diagrams with respect to the Edge select parameter with DATA = 1 and DATA = 3, respectively.

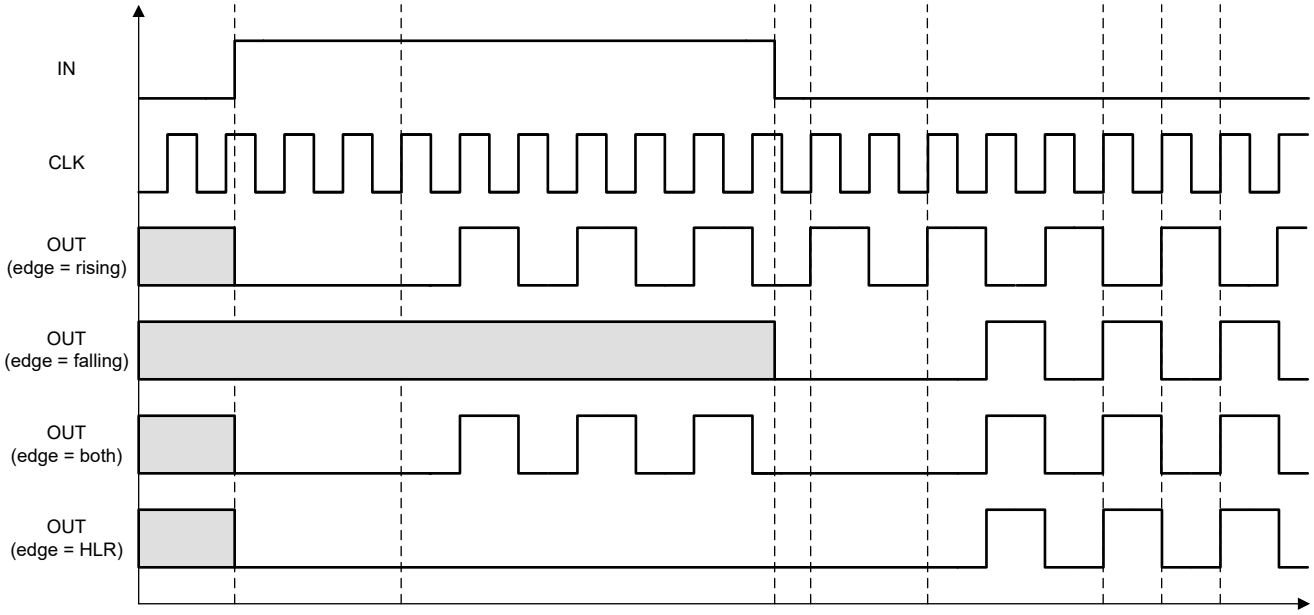

Figure 8-15. Counter Output Timing Example (DATA = 1)

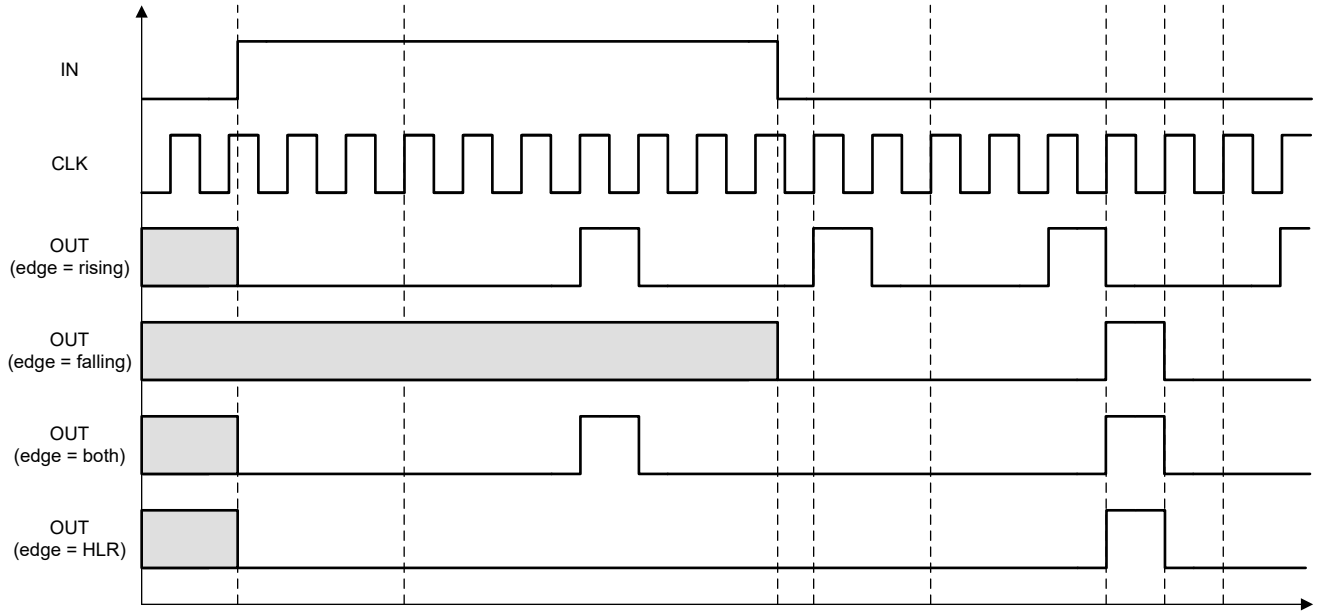

Figure 8-16. Counter Output Timing Example (DATA = 3)

Figure 8-17 shows an example of how the Counter macro-cell operates when the IN signal is shorter than the counter length (shown when edge select parameter is set to "both").

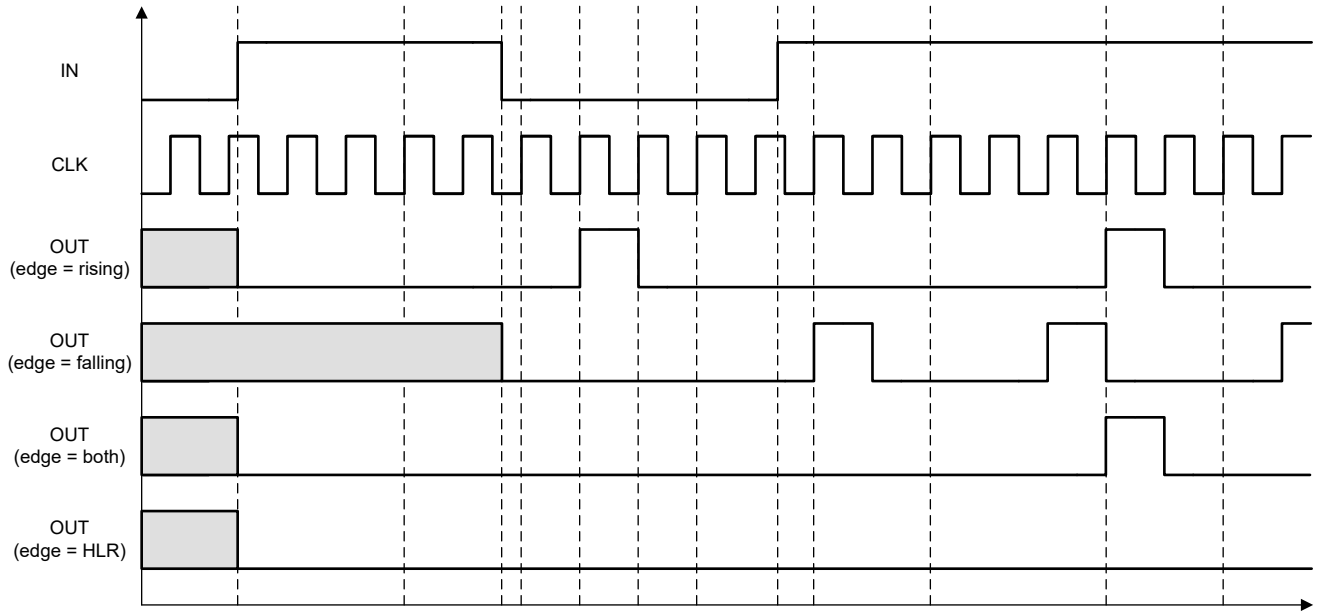

Figure 8-17. Counter Output Timing Example with RST < DATA (DATA = 3)

8.3.4.3.3 One-Shot Mode

When configured as a One-shot, this macro-cell generates a pulse that begins when a valid edge appears on the IN input, which triggers the counter to begin counting down from DATA following two CLK cycles, and the pulse ends once the counter reaches 0 and DATA is subsequently reloaded into the counter and waiting for the next trigger. Triggers received while the counter is decrementing are ignored. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which the One-shot is reset is determined by the Edge select parameter and can be configured as:

- **Rising**: only rising edges of IN reset the one-shot.

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- **Falling**: only falling edges of IN reset the one-shot.
- **Both**: both rising and falling edges of IN reset the one-shot.

An additional 2 clock cycles are included in the one-shot pulse width calculation for clock synchronization.

$$\text{ONESHOT} = \left[\text{DATA} + \left(t_{d_er} \text{ or } t_{d_os}\right) + 1\right] \div f_{CLK} \quad (3)$$

Figure 8-18 shows an example of how the One-shot macro-cell operates with respect to the Edge select parameter.

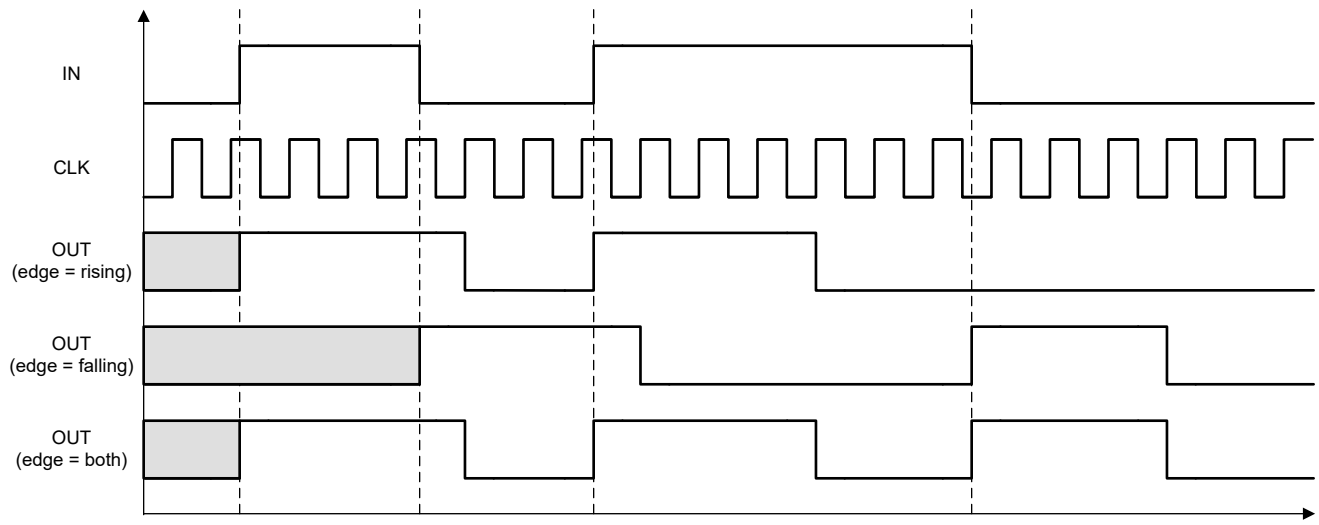

Figure 8-18. One-shot output timing example (DATA = 2)

8.3.4.3.4 Frequency Detector Mode

When configured as a Frequency detector (FDET), this macro-cell indicates whether the input signal is faster or slower than the period specified by DATA. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which the Frequency detector is reset is determined by the Edge select parameter and can be configured as:

- **Rising**: rising edges of IN trigger and reset the frequency detector.
- **Falling**: falling edges of IN trigger and reset the frequency detector.
- **Both**: rising edges of IN triggers the frequency detector to begin counting and falling edges of IN reset the frequency detector.

Upon receiving a trigger, an additional 2 clock cycles is used to synchronize IN and the counter with CLK, then the counter begins decrementing from DATA on the following rising edge of CLK. For proper operation of the FDET macro-cell, TI recommends using a minimum DATA of 3.

If the internal counter reaches 0, the FDET macro-cell outputs a Low signal, indicating the input frequency is slower than DATA. Otherwise, if the counter is interrupted with a reset before reaching 0, the FDET macro-cell outputs a High signal, indicating a faster signal on IN.

Figure 8-19 shows an example of how the FDET macro-cell operates with respect to the Edge select parameter.

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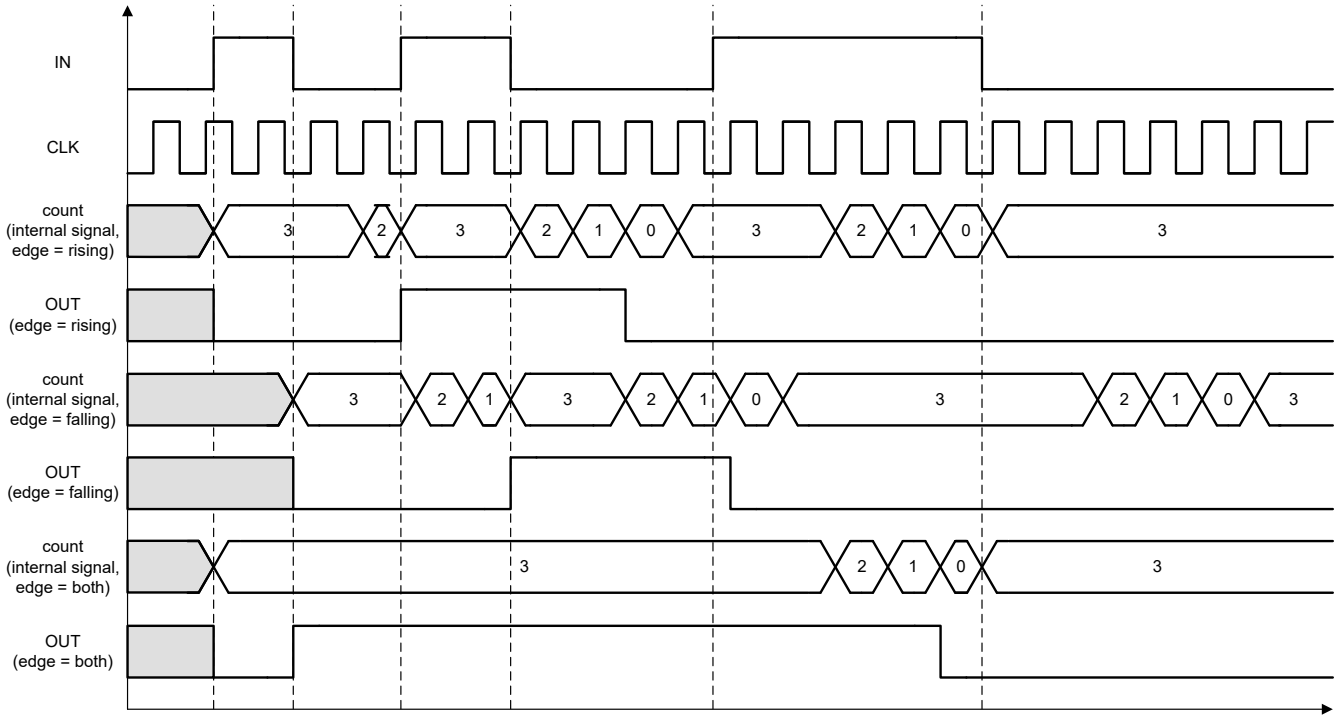

Figure 8-19. Frequency detector output timing example (DATA = 4)

8.3.4.3.5 Edge Detector Mode

When configured as an Edge detector (EDET), this macro-cell generates a pulse of approximately 20ns width when a valid edge is detected. The edge on which the Edge detector generates a pulse is determined by the Edge select parameter and can be configured as:

- **Rising**: only rising edges of IN generate a pulse.
- **Falling**: only falling edges of IN generate a pulse.
- **Both**: both rising and falling edges of IN generate a pulse.

Figure 8-20 shows an example of how the EDET macro-cell operates with respect to the Edge select parameter.

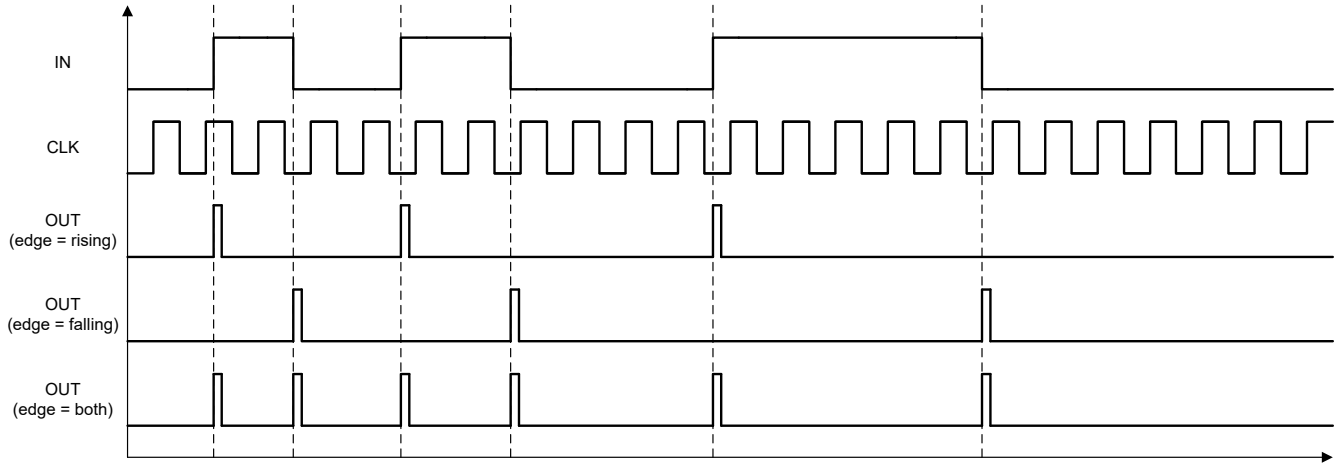

Figure 8-20. Edge Detector Output Timing Example

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8.3.4.3.6 Delayed Edge Detector Mode

When configured as a Delayed edge detector (Delayed EDET), this macro-cell delays the input by the value in DATA and then generate a pulse of approximately 20ns width when the selected edge is detected on the delayed input. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which to delay and then output an edge detect pulse is selected by the Edge select parameter and can be configured as:

- **Rising**: only delay on rising edges of IN.
- **Falling**: only delay on falling edges of IN.
- **Both**: delay on both rising and falling edges of IN.

Upon receiving a trigger, an additional 2 clock cycles is used to synchronize IN and the counter with CLK, then the counter begins decrementing from DATA on the following rising edge of CLK. If the counter is allowed to reach 0 and wrap around back to DATA, the Delayed EDET macro-cell outputs a pulse. Otherwise, if the counter is interrupted with a reset before reaching 0, the Delayed EDET macro-cell "filter out" the previous edge.

Figure 8-21 shows an example of how the Delayed EDET macro-cell operates with respect to the Edge select parameter.

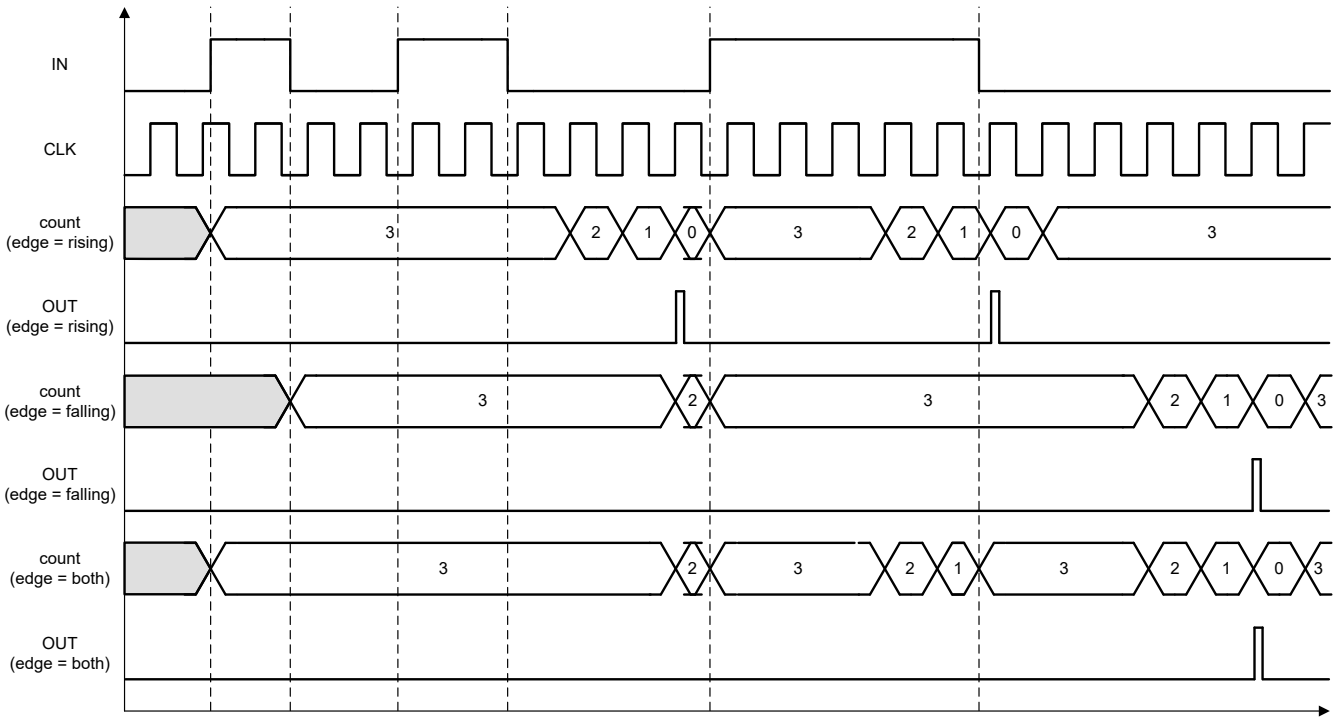

Figure 8-21. Delayed Edge Detector Output Timing Example (DATA = 3)

8.3.4.4 LUT/DFF + CNT modes

In addition to the discrete LUT, DFF/latch, or counters described previously, the configurable logic and timing blocks can be configured in two other modes:

- Mode 1: LUT/DFF into counter. The three inputs from the connection mux go into the LUT/DFF/LAT and the output of the first stage feed into the input of the counter. The output of the counter goes back into the connection mux.
- Mode 2: Counter into LUT/DFF. One input from the connection mux goes to the counter input and the output feeds into any one input of the LUT or the DFF/LAT. The output of the second stage goes back into the connection mux.

This feature enables more LUTs, DFFs/latches, and counters to be used in a design. However, within a single block, only the LUT or only the DFF/latch may be used. Further, in these modes, the external clock source from the connection mux for the counter is disabled, thus, only a frequency derived from the internal oscillator can be used.

8.3.5 Programmable Deglitch Filter or Edge Detector

The TPLD2001-Q1 has two macro-cells that can be configured as a Programmable filter (PFLT) or Edge detector (EDET). The PFLT macro-cell can be used to generate a delay (t_{pflt_d}) characterized by t_{pflt_pw} and t_{pflt_pd}. t_{pflt_pw} can be set to 125ns, 250ns, 375ns, or 500ns and t_{pflt_pd} is a fixed value. Furthermore, the output of the macro-cell can be configured to one of four options: rising edge detection, falling edge detection, both edge detection, or both edge delay. Lastly, the filter operates as a short low-pass filter and its output can be set as non-inverted or inverted.

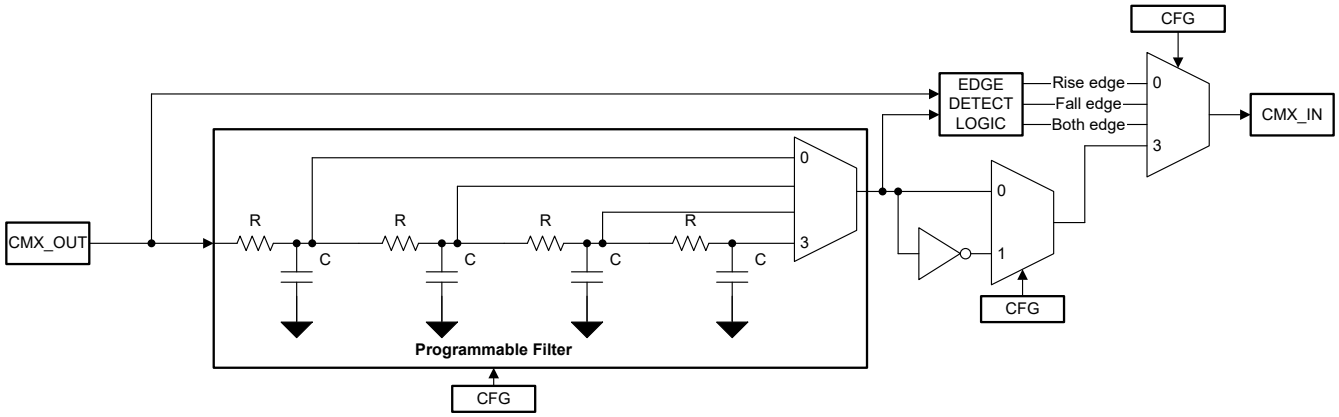

Figure 8-22. Programmable Filter/Edge Detector Block Diagram

Note

The input signal must be longer than the t_{pflt_d}, otherwise it filters out.

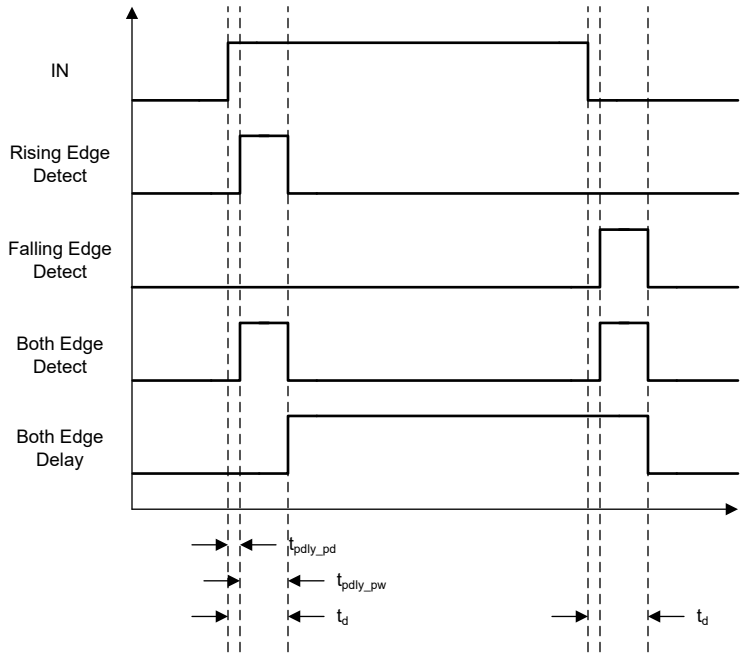

Figure 8-23. Delayed edge detector output timing diagram

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8.3.6 Deglitch Filter or Edge Detector

The TPLD2001-Q1 has one macro-cell that can be configured as a Deglitch filter or an Edge detector.

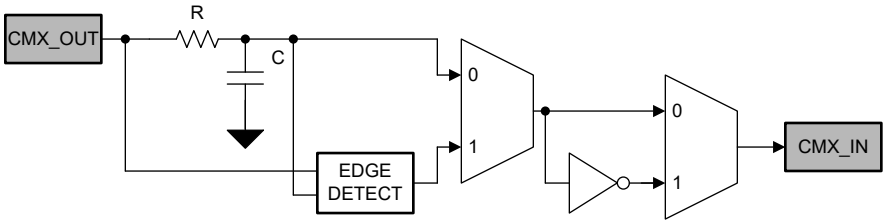

Figure 8-24. Deglitch Filter or Edge Detector Block Diagram

The Deglitch filter operates as short low-pass filter and the filter output can be set as non-inverted or inverted.

As an Edge detector, this macro-cell can be configured to output a short pulse that is triggered on the rising edge, the falling edge, both edges, or act as a filter and delay both edges. The edge detector output can be set as non-inverted or inverted.

8.3.7 State Machine (SM)

The TPLD2001-Q1 features a state machine macro-cell that can be operated synchronously or asynchronously with 24 state transition inputs, 1 clock input, 1 state machine reset input, and 8 outputs. This macro-cell can be configured to create a 2- to 8-state state machine, where the states, state transition conditions, state transition inputs, and state outputs are user-defined. Each state has a maximum of 3 transition conditions that can trigger a transition into that particular state, limited by the state transition inputs that are hardwired in the connection mux.

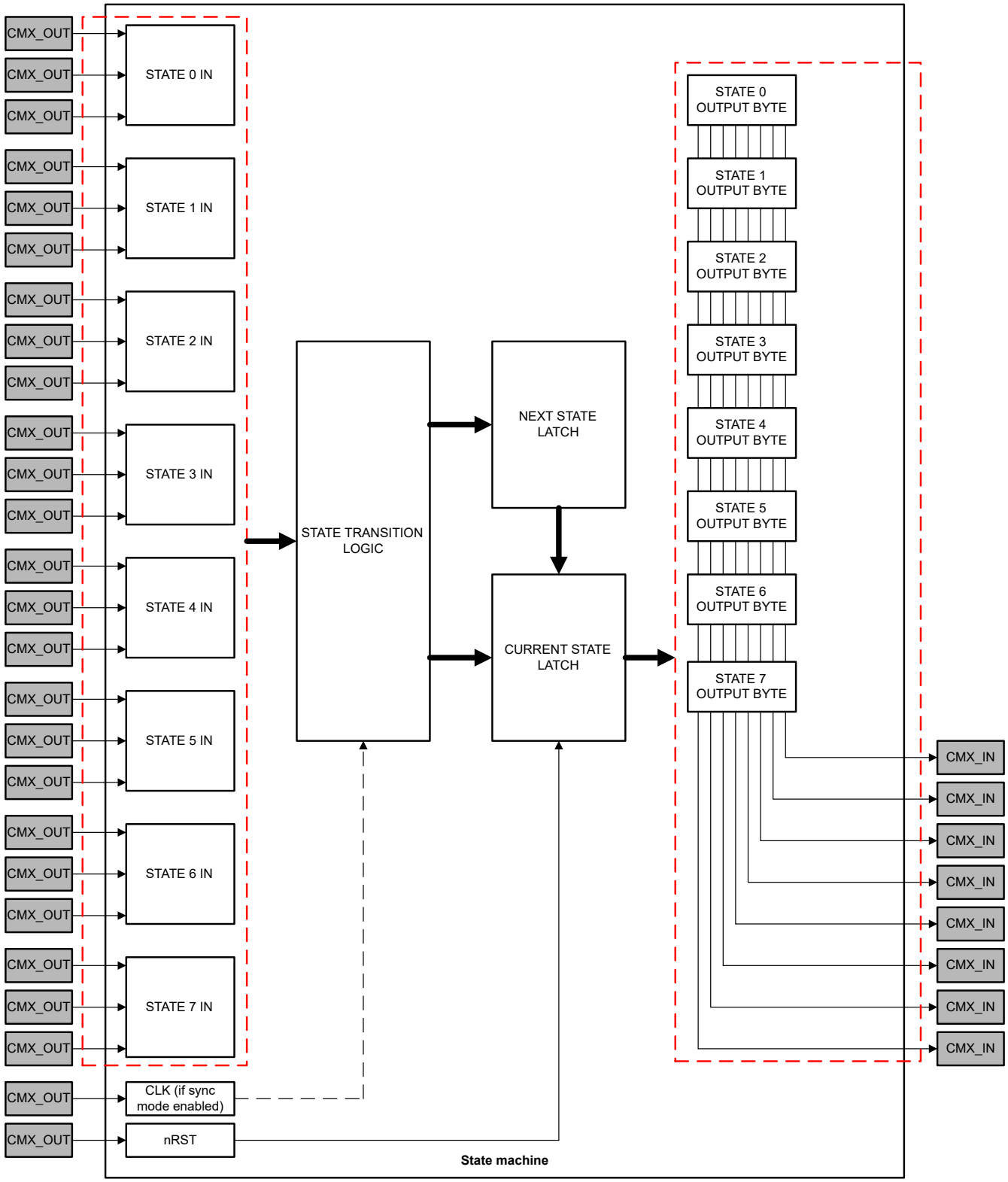

Figure 8-25. State Machine Block Diagram

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8.3.7.1 State Machine Inputs

The state machine macro-cell has 26 inputs from the connection mux: 24 state transition inputs, 1 clock input, and 1 reset input.

Each of the 24 state transition inputs are active-high inputs, meaning a high-level input would trigger a state transition given the timing considerations are met. Further, these 24 inputs are grouped such that each set of 3 inputs drives a transition into a particular state. For example, there are 3 inputs that drives a transition from any state into State 2. Thus, this limits the maximum number of transitions into a particular state to 3.

When operating the state machine in synchronous mode and a state transition condition is met, the state transition will occur on the next rising edge of the clock input. In asynchronous mode, when a state transition condition is met, the state transition occurs asynchronously and the clock input is unavailable/ignored.

There is also an active-low, asynchronous reset input which, when asserted, puts the state machine into a reset state and, when released, will place the state machine in the user-selected initial state.

8.3.7.2 State Machine Outputs

The state machine macro-cell has 8 outputs into the connection mux. With an 8-byte RAM, users are able to set the behavior of the 8 outputs for each defined state, which could be seen as 8 parallel outputs that can be configured depending on the current state. Each of the 8 outputs are connection mux inputs that could be elsewhere in the design, such as an input into a LUT, D flip-flop, counter, or out to a GPO pin.

The state machine outputs can be updated in-system using the User Registers. For glitch-free operation, it is recommended to put the state machine in a reset while the state machine output bits are being modified.

8.3.7.3 Configuring the State Machine

The following can be configured for an operating state machine: states, initial state, state transitions, mode, clock polarity.

- **States:** Up to 8 states can be used.
- **Initial state:** One of the states used can be selected as the initial state in which the state machine macro-cell resets to following an asynchronous reset.
- **State transitions:** Users can set the transition from one state into another to enable a state transition condition input, with a maximum of 3 transitions into a particular state. The state transition conditions are inputs from the connection mux and can be configured to come from any GPI or other macro-cell outputs.
- **Mode:** The state machine can be selected to operate in synchronous mode, in which state transition conditions are synchronously latched in with respect to the clock input, or asynchronous mode.
- **Clock synchronization:** When operating in synchronous mode, there is an option to synchronize the state machine clock to the system clock to further reduce glitches.

The serial communication interface, if enabled, can be used to read the current state of an active state machine and reconfigure the state outputs. Any changes made to the state machine configuration through the serial communication interface are only reflected after the next state transition or a reset event. Thus, to maintain the desired behavior, best practice is to keep the state machine in reset while reconfiguring the macro-cell.

8.3.7.4 State Machine Timing Considerations

When the state machine macro-cell is in operation, especially when operating asynchronously, the state transition inputs timing requirement, delays in the I/O, other macro-cells used in the state transition input path, and the connection mux need to be taken into consideration to verify inputs are properly processed and state transitions are deterministic.

In synchronous mode, state transition trigger input needs to be asserted for at least 2 clock cycles, otherwise the input is ignored. In asynchronous mode, the state transition trigger input needs to be asserted for at least the state transition pulse width, t_{st_pw}. If a state transition condition is met, the transition occurs after the state transition delay, t_{st_dly}.

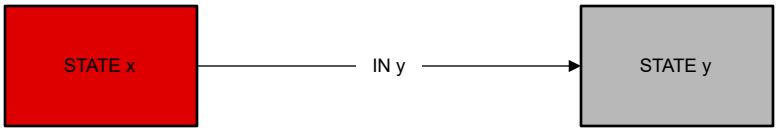

Figure 8-26. State Transitions

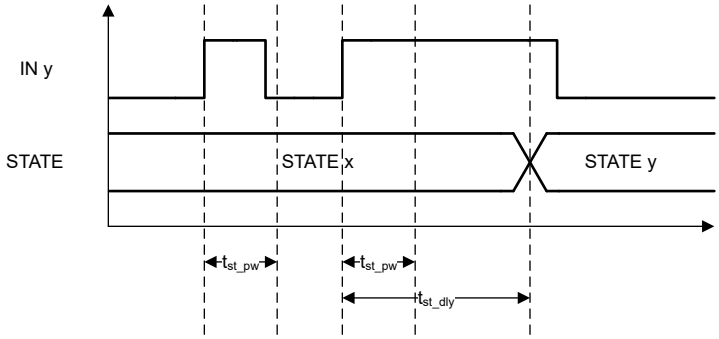

Figure 8-27. State Transition Trigger Requirements Timing Example

When two or more state transition input triggers exist within the state transition pulse width, t_{st_pw}, the next state is indeterminate. To avoid such cases, careful consideration must be taken in the timing of the state transition inputs.

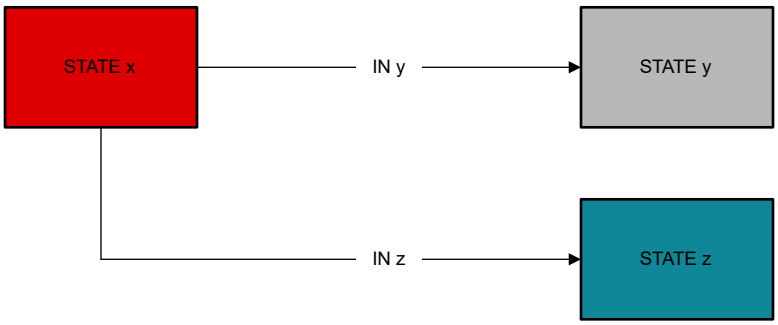

Figure 8-28. State Transitions With Competing Triggers

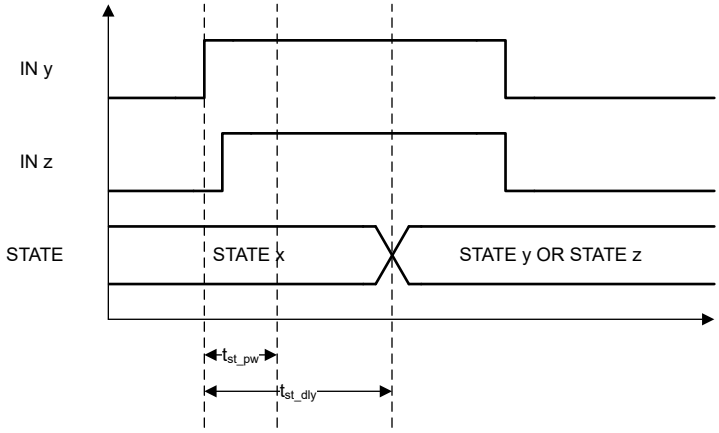

Figure 8-29. State Transition With Competing Triggers Considerations Timing Example

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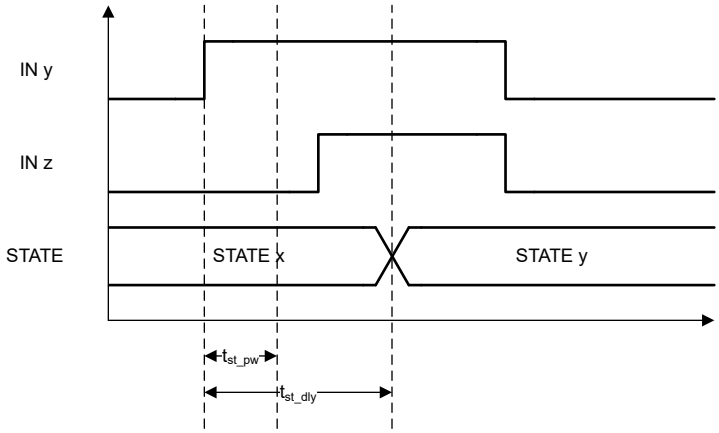

Figure 8-30. State Transition Considerations for Deterministic Transition Timing Example

For sequential state transitions or closed-loop state transitions, where state transition input triggers are asserted that prompt the state machine to go into a next state, transitions into consecutive states occurs after the state transition delay, t_{st_dly}. Thus, the state machine remains in the current state for at least t_{st_dly}.

Figure 8-31. Sequential state transition

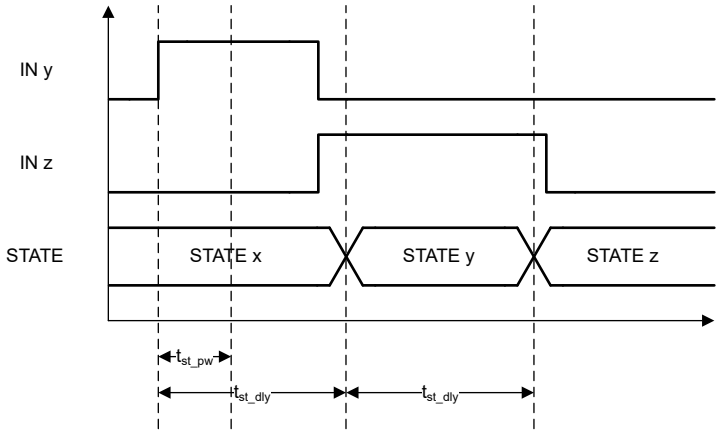

Figure 8-32. Sequential State Transition Timing Example

The closed-loop state transition example shown only considers two states. However, the closed-loop can be made with any number of states from two to the maximum of eight.

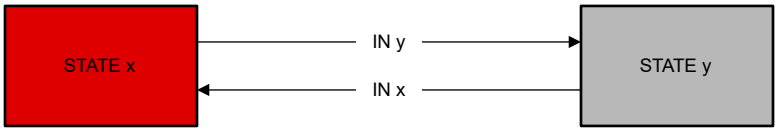

Figure 8-33. Closed Loop State Transition

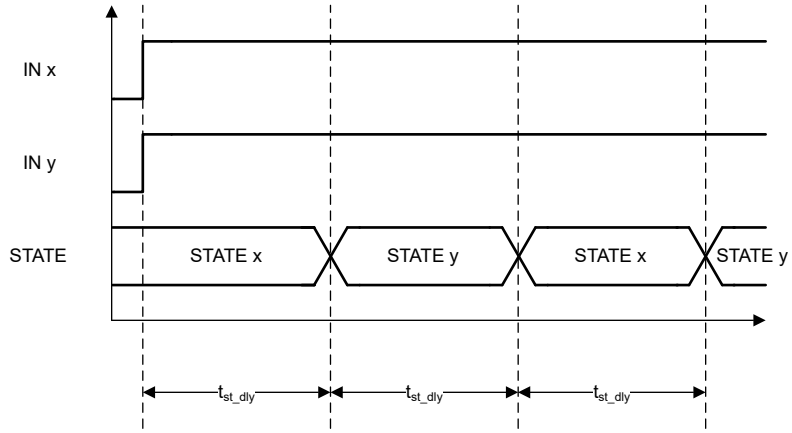

Figure 8-34. Closed Loop State Transition Timing Example

8.3.8 8-Bit Counters/Delay Generators/Finite State Machines

The TPLD2001-Q1 has four 8-bit counters that can operate as a finite state machine (FSM) while in Reset counter mode in addition to the modes outlined in Section 8.3.4.3. These 8-bit counter macro-cells have 4 inputs from the connection mux: counter input, FSM up/down, FSM keep, and external clock input; and 1 output into the connection mux: counter out. There is also an 8-bit parallel output of the current count value from this macro-cell that routes directly into the pulse-width modulation (PWM) generator macro-cells.

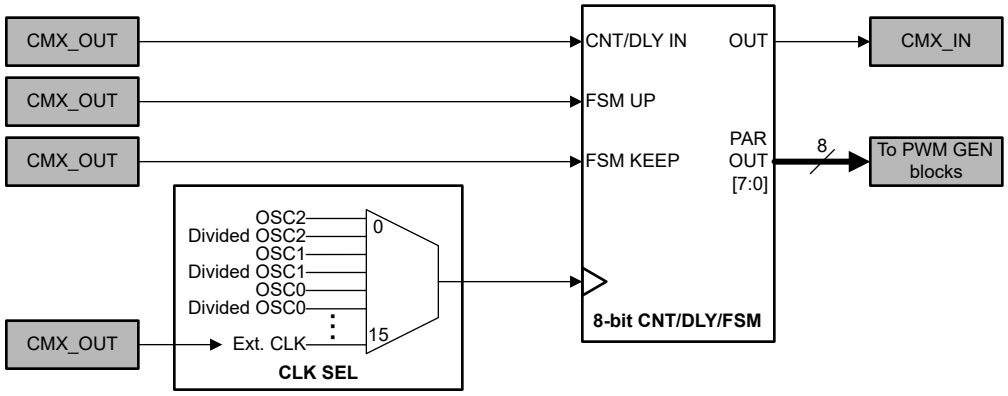

Figure 8-35. CNT/DLY/FSM block diagram

The following can be configured for an operating FSM: counter reset data and clock.

- Counter reset data: The value which the counter loads when a reset condition is met and can be set to any value from 1 to 255. The counter data can be updated in-system using the User Registers. TI recommends to put the counter in a reset state when updating the counter data registers to maintain glitch-free loading of the data.
- Edge select, the edge in which to asynchronously reset the counter to the initial counter data: Both, Rise, Fall, or High-level reset.
- Clock input: OSC0, a divided clock derived from OSC0 (/8, /64, /512, /4096, /32768, /262144), OSC1, a divided clock derived from OSC1 (/8, /64, /512), OSC2, a divided clock derived from OSC2 (/4), or an external clock.

Note

For unused counter macro-cells, set the clock selection (CLK_SEL) to External CLK from CMX to reduce excess current draw.

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The FSM UP input determines the direction of the counter/FSM, whether the count decrements or increments with respect to the rising edge of the clock input. While FSM UP = Low, the counter decrements (count downward) and reset to the initial counter data once 0 is reached; and while FSM UP = High, the counter increments (count upward) and reset to the initial counter data once 255 is reached.

The FSM KEEP input pauses, or latch, the current count and ignore any FSM UP or clock input. The count reset input still resets the counter, but neither decrements nor increments. While FSM KEEP = Low, the counter counts as configured; and while FSM KEEP = High, the counter pauses. If a constant FSM counter value is needed, set FSM KEEP to High and FSM UP to Low to maintain proper functionality.

After a trigger of UP or KEEP, an additional 2 clock cycles is added for clock synchronization with an option to bypass. Note, bypassing the clock synchronization can result in the counter resetting to an unknown value.

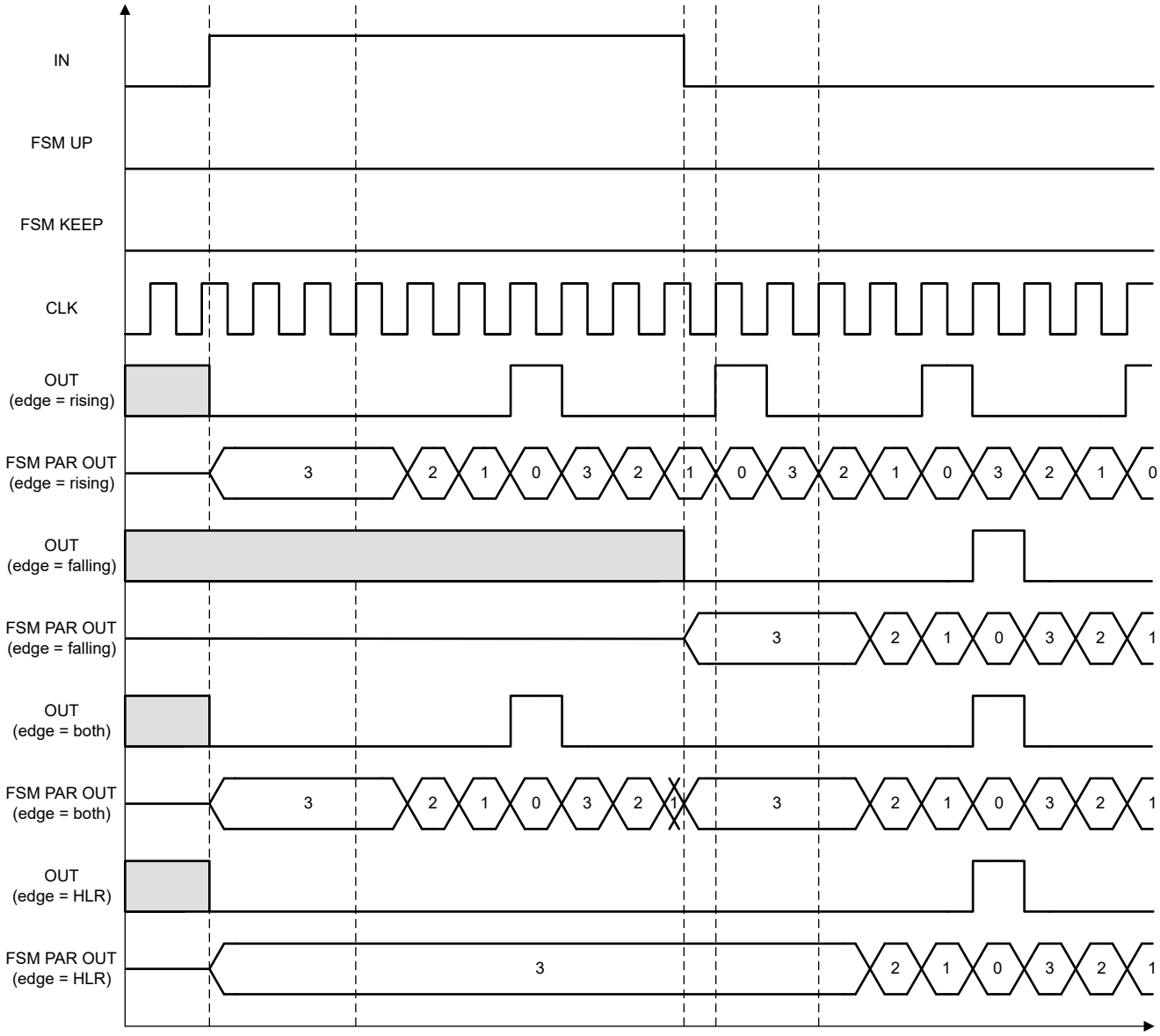

Figure 8-36. CNT/FSM timing example (DATA = 3)

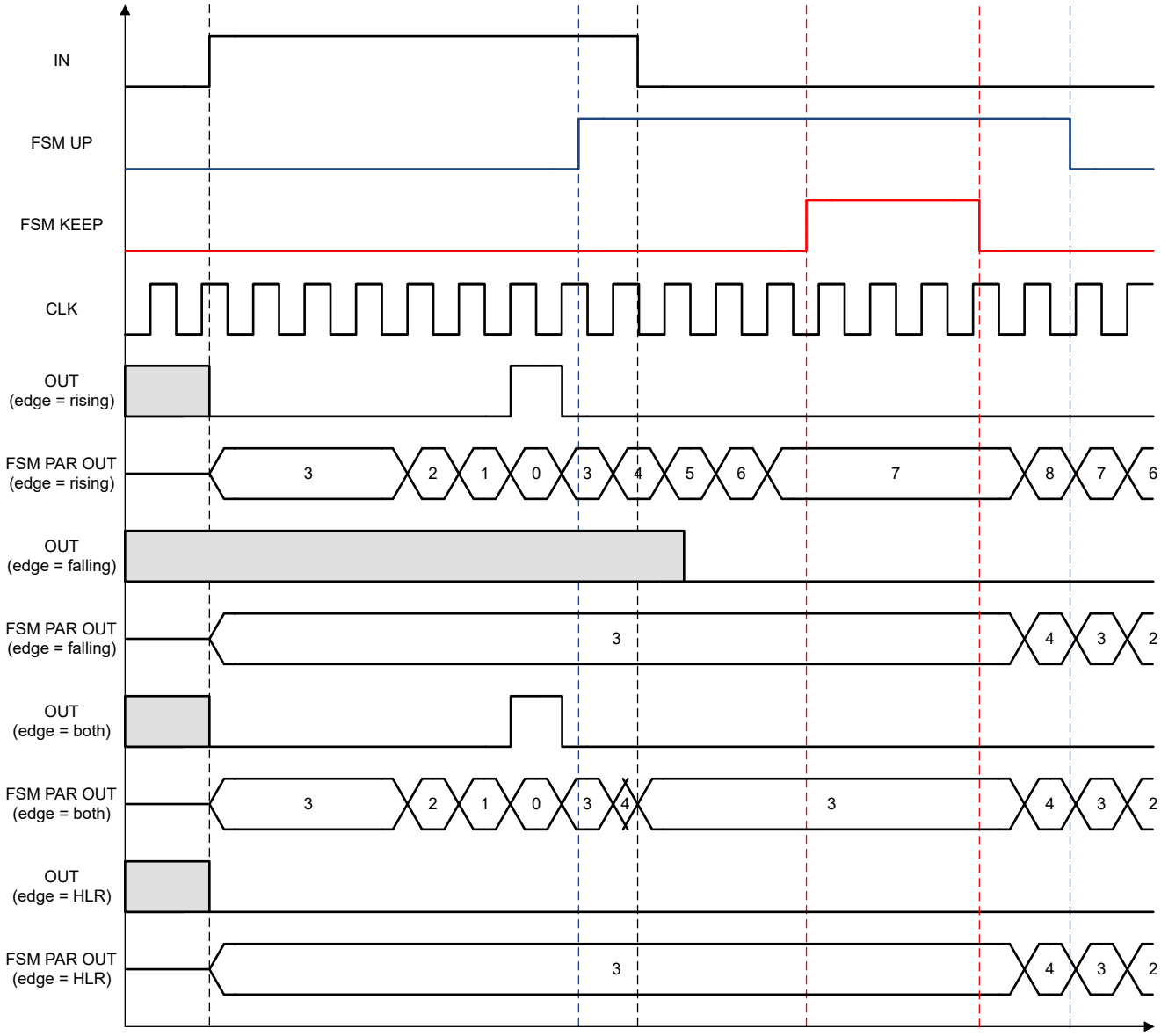

Figure 8-37. CNT/FSM with UP/KEEP timing example (DATA = 3)

8.3.9 PWM Generators

The TPLD2001-Q1 has four pulse-width modulation (PWM) generators that outputs a square wave with a duty cycle proportional to the counter value from the selected FSM. These PWM generator macro-cells have 1input from the connection mux to control the macro-cell power up; 1 input directly from FSM blocks; and 2 outputs into the connection mux.

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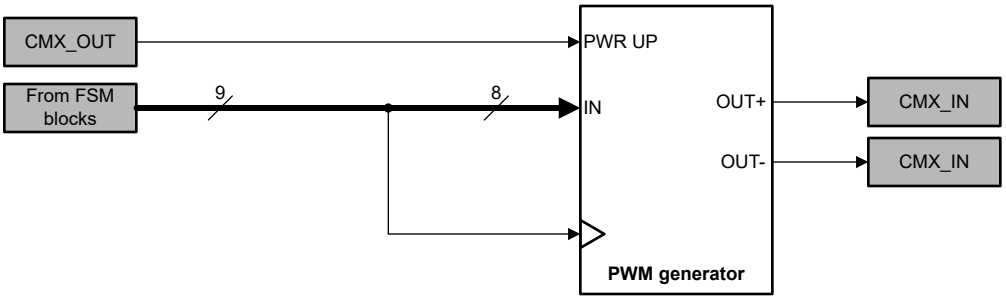

Figure 8-38. PWM Generator Block Diagram

The following can be configured for an operating PWM generator: input source, deadband time, output polarity, clock.

- **Data input source (IN):** Any of the four FSMs can be selected to provide the counter value.
- **Deadband time (t_{db}):** 0 CLKs (no deadband), 1 CLK, 2 CLKs, or 5 CLKs. The deadband time will be applied to the OUT- output of the PWM generator.
- **Output polarity:** the polarity of each output (OUT+ and OUT-) can be configured to non-inverted or inverted (nOUT+ and/or nOUT-).
- **Clock:** OSC0, a divided clock derived from OSC0 (/8, /64, /512, /4096, /32768, /262144), OSC1, a divided clock derived from OSC1 (/8, /64, /512), OSC2, or a divided clock derived from OSC2 (/4).

The PWM generator macro-cell reads the count value of the selected FSM once every 256 clock cycles. Thus, the PWM generator output frequency is determined by $f_{CLK}/256$. Further, the duty cycle of the PWM signal calculated by: Duty cycle (%) = (IN / 256) * 100, with a minimum duty cycle of 0% (or 0/256) and a maximum of 99.61% (or 255/256).

Note, upon startup of the PWM generator, the macro-cell requires 2 clock cycles for clock synchronization. If the selected deadband time is greater than the FSM counter data input, a constant low will appear on the non-inverted OUT- output. Additionally, the PWM generator macro-cell can be powered down by sending a LOW signal to the PWM PWR UP input to prevent outputing in an idle state.

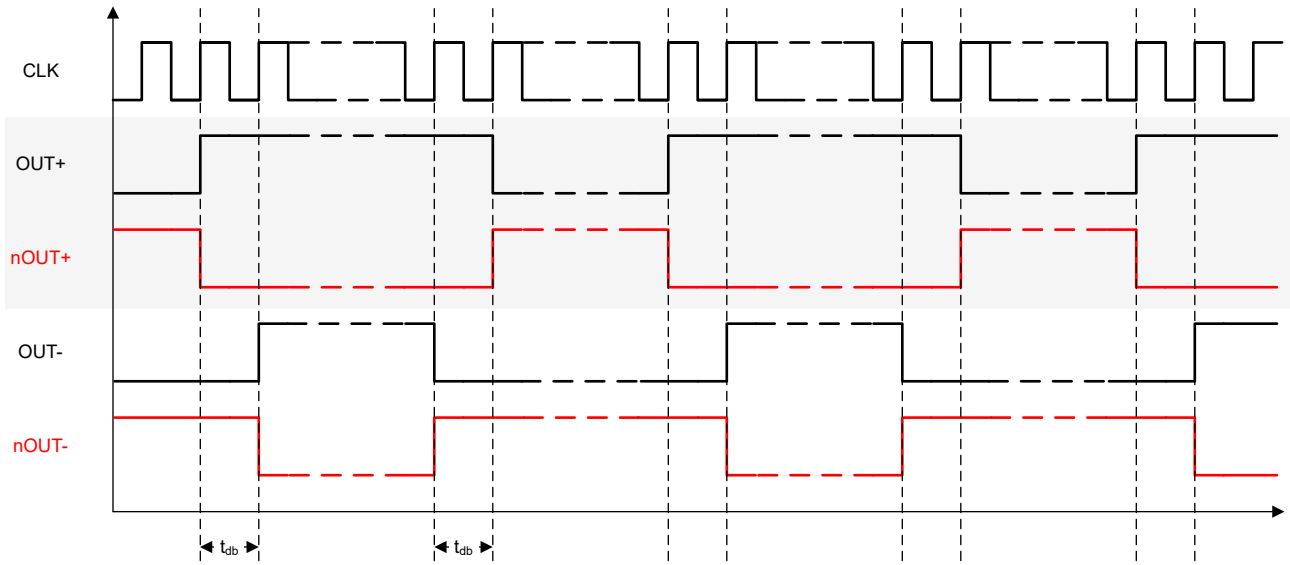

Figure 8-39. PWM Generator Timing Example

8.3.10 Watchdog Timer

The watchdog timer (WDT) macro-cell monitors the input into the macro-cell for any edge (rising or falling) in the time frame defined by the t_{WD} time period. The WDT macro-cell has 2 inputs from the connection mux: 1 active-high enable and 1 watchdog input. There is also 1 clock input directly from the internal oscillators.

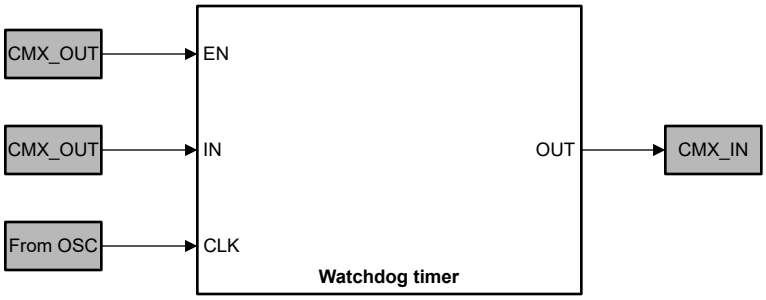

Figure 8-40. Watchdog Timer Block Diagram

The following can be configured for an operating WDT: the timeout period (t_{WD}), the output assert time (t_{WDO}), the clock source, an additional clock divider option, behavior of WDT while disabled.

- Timeout period (t_{WD}): The WDT operates on an 8-bit counter and supports count data values of 5 to 255.
- Output assert time (t_{WDO}): A separate 8-bit counter controls the output assertion time period, supporting count data values of 1 to 255.
- Clock source: OSC0, a divided clock derived from OSC0 (/8, /64, /512, /4096, /32768, /262144), OSC1, a divided clock derived from OSC1 (/8, /64, /512), OSC2, or a divided clock derived from OSC2 (/4).
- Additional clock division: An additional clock divide by 100 can be toggled to further extend the timeout period.
- Behavior while disabled: Users can set the counter to reset to the specified count data when the WDT is disabled or to pause the counter and resume once the WDT is re-enabled. Regardless of selection, the counter will reset if any edges appear on the WDT input while the WDT macro-cell is disabled.

When a timeout condition is reached, the WDT macro-cell outputs a Low pulse for the specified amount of time.

Note

For unused watchdog timer macro-cell, set the clock selection (CLK_SEL) to External CLK from CMX to reduce excess current draw.

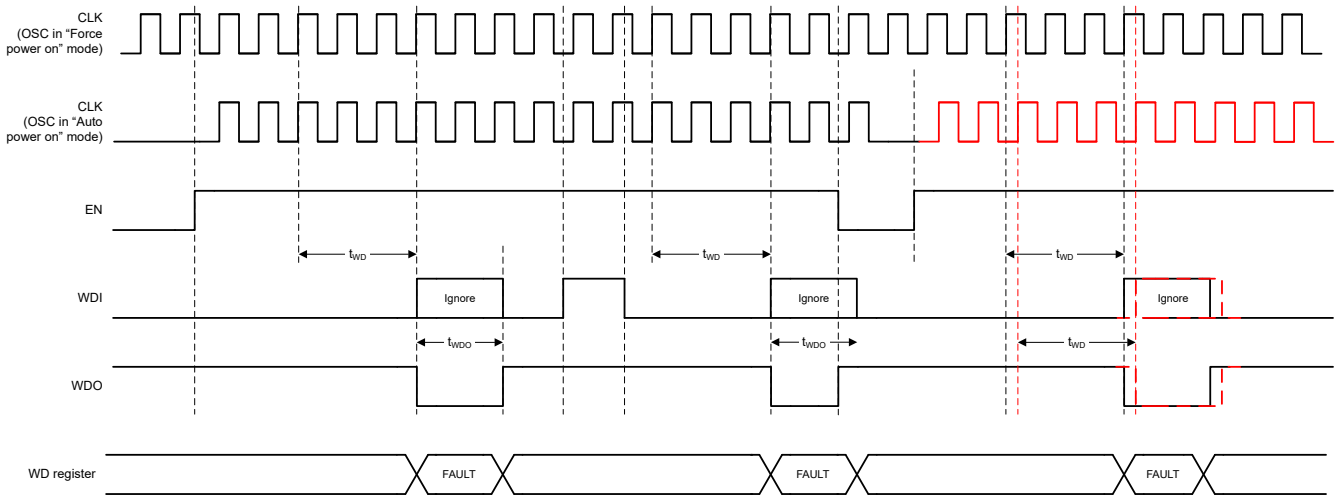

Figure 8-41. Watchdog timer output timing example (reset count when disabled)

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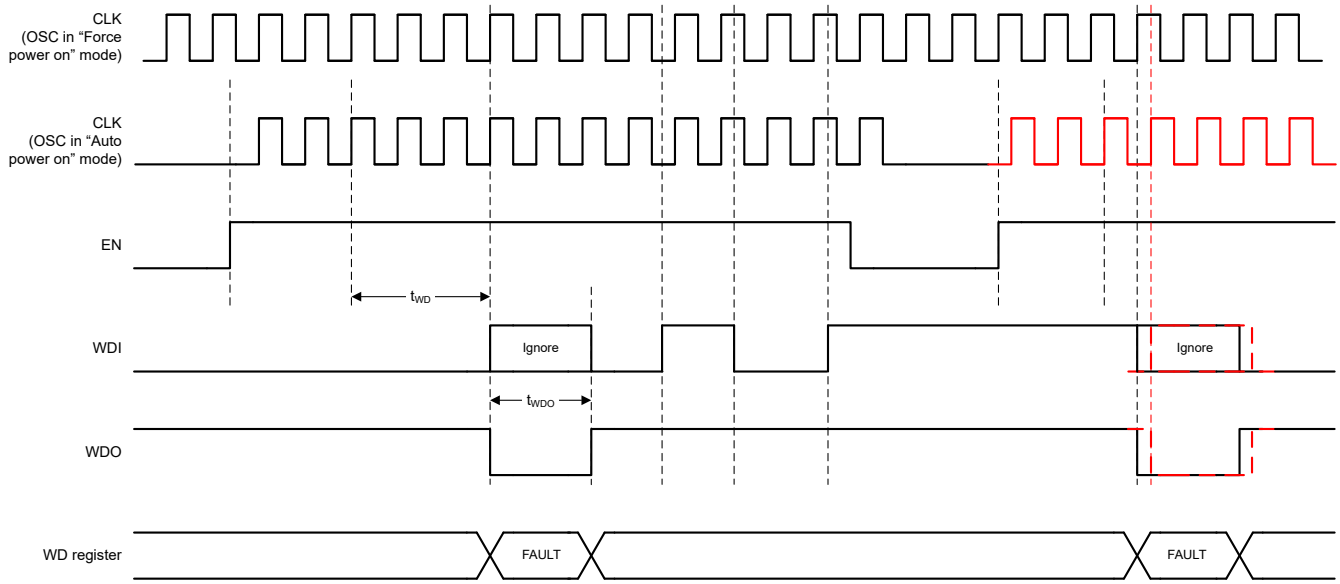

Figure 8-42. Watchdog timer output timing example (pause count when disabled)

8.3.11 Analog Comparators

The TPLD2001-Q1 has four discrete analog comparators (ACMP) and one multi-channel sampling comparator (McACMP). The ACMP and McACMP compares two voltages (IN+ and IN-) and outputs a digital signal (OUT) indicating which is larger, a High signal for IN+ and a Low for IN-.

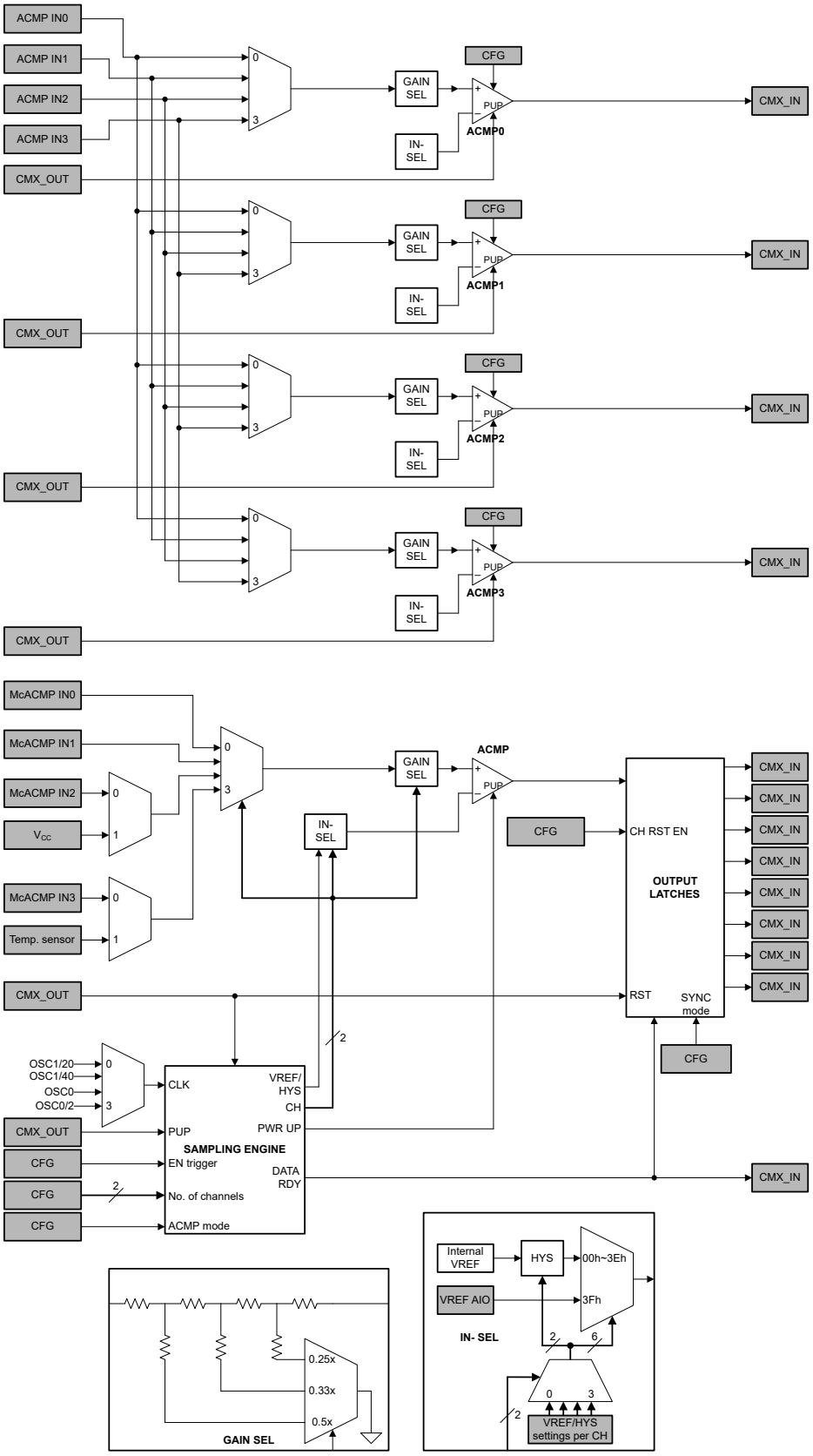

Figure 8-43. Analog Comparators Block Diagram

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8.3.11.1 Discrete Analog Comparator (ACMP)

For the ACMP macro-cell to be used in a TPLD design, the power up (PWR UP) port needs to be connected to a logic High signal. By connecting to signals coming from the connection mux, having the ACMP always on, always off, or switched on dynamically based on a digital signal coming from the connection mux is possible.

- PWR UP = 1 => ACMP is powered up.
- PWR UP = 0 => ACMP is powered down.

When powered down, the output of the ACMP is a static logic Low. Upon power up, the output remains Low, and then become valid 110µs (max) after the PWR UP signal goes high, during which time, maintain that OSC1 is not powered down.

The ACMP macro-cell has a positive input signal that can be provided by a variety of external sources with a selectable gain stage before going into the analog comparator. The negative input signal can either come from the internal VREF or an external source, which is shared between all comparator channels.

Table 8-21. ACMP Input Sources

Parameters	Source
IN+ source	ACMP IN0
	ACMP IN1
	ACMP IN2
	ACMP IN3

IN+ gain: The McACMP positive input can be provided by a variety of external sources, and can also have a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connecting to the analog comparator.

IN- voltage range: 32mV to 2.016V through the internal VREF or up to 2.016V external source.

The VREF selection per discrete analog comparator can be updated in-system using the User Registers. For glitch-free measurements, TI recommends to disable/power down all analog comparators when changing the VREF. If the analog comparator is not disabled while the VREF selection is being updated, up to 10µs for valid data can be needed to output from the analog comparators.

Hysteresis: If the internal VREF is used, corresponding ACMP channels have four selectable hysteresis options 0mV, 32mV, 64mV and 192mV. If the IN+ input signal is slow or noisy, TI recommends to use hysteresis.

- **0mV**: will disable the input signal hysteresis.
- **64mV**: is a +32mV and -32mV hysteresis. For VREF = 1.024V, the trigger points is 1.056V and 0.992V.
- **128mV**: is a +64mV and -64mV hysteresis. For VREF = 1.024V, the trigger points is 1.088V and 0.960V.
- **192mV**: is a +96mV and -96mV hysteresis. For VREF = 1.024V, the trigger points is 1.120V and 0.928V.

If hysteresis is desired, the internal VREF must be used. Further, hysteresis values that otherwise extends beyond the range of the VREF are limited to the minimum and maximum values available in the device. For example, if IN- = 1.984V and VHYS = ±64mV, the lower trigger point is 1.920V and the upper trigger point is 2.016V.

Low bandwidth: The ACMP cell has a selection for the bandwidth of the input signal, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared.

8.3.11.2 Multi-channel Analog Comparator (McACMP)

For the McACMP macro-cell to be used in a TPLD design, the power up (PUP) port needs to be connected to a logic High signal. By connecting to signals coming from the connection mux, it is possible to have the McACMP always on, always off, or switched on dynamically based on a digital signal coming from the connection mux.

- PUP = 1 => McACMP is powered up.
- PUP = 0 => McACMP is powered down.

Upon power up, the output remains static and then become valid t_{start} after the PUP signal goes high, during which time, verify OSC1 is not powered down.

The McACMP macro-cell has a positive input signal that can be provided by a variety of external sources with a selectable gain stage before going into the analog comparator. The negative input signal can either come from the internal VREF or an external source, which is shared between all comparator channels. Each channel has the option to select up to four negative input points to compare against.

Table 8-22. McACMP Input Sources

Parameters	Primary source	Secondary source
IN+ source	McACMP IN0	
	McACMP IN1	
	McACMP IN2	V_{CC}
	McACMP IN3	Temp. sensor

IN+ gain: The McACMP positive input can be provided by a variety of external sources, and can also have a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connecting to the analog comparator.

IN- voltage range: 32mV to 2.016V through the internal VREF or up to 2.016V external source.

The VREF selection per channel of the multi-channel sampling analog comparator can be updated in-system using the User Registers. For glitch-free measurements, it is recommended to disable/power down all analog comparators when changing the VREF. If the analog comparator is not disabled while the VREF selection is being updated, it can take up to 10µs for valid data to be output from the analog comparators.

Hysteresis: If the internal VREF is used, corresponding McACMP channels have four selectable hysteresis options 0mV, 32mV, 64mV and 192mV. If the IN+ input signal is slow or noisy, it is recommended to use hysteresis.

- **0mV**: disables the input signal hysteresis.
- **64mV**: is a +32mV and -32mV hysteresis. For VREF = 1.024V, the trigger points are 1.056V and 0.992V.
- **128mV**: is a +64mV and -64mV hysteresis. For VREF = 1.024V, the trigger points are 1.088V and 0.960V.
- **192mV**: is a +96mV and -96mV hysteresis. For VREF = 1.024V, the trigger points are 1.120V and 0.928V.

If hysteresis is desired, the internal VREF must be used. Further, hysteresis values that would otherwise extend beyond the range of the VREF is limited to the minimum and maximum values available in the device. For example, if IN- = 1.984V and VHYS = ±64mV, the lower trigger point is 1.920V and the upper trigger point is 2.016V.

When only one channel and one VREF is selected, the McACMP disables the sampling engine and operate as a discrete analog comparator.

In multi-channel sampling mode, the TPLD2001-Q1 can be configured to sample up to 4 channels, each with its own selectable gain, voltage reference, and hysteresis (if the internal VREF is used). The sampling clock can be selected from the output of OSC0 or OSC1 with a given pre-divider and an additional divider at the McACMP. Other configurations that can be set are the output synchronicity, the trigger to begin a sample sequence, a sequence restart and output latch reset/clear input, and the option to select up to 2 VREFs per channel.

When sampling in multi-channel mode, the McACMP samples the set channels in sequential order (channel 0 through channel n) and the edge of the clock on which samples are captured can be selected.

Clock: The McACMP sampling clock can be selected to be OSC1 / 20, OSC1 / 40, OSC0, or OSC0 / 2.

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Table 8-23. McACMP Clock Options

Base Frequency	Pre-dividers	Dividers
2kHz	1	1
	2	2
	4	
	8	
2MHz	1	20
	2	40
	4	
	8	

Enable trigger: Note that the Enable signal is a synchronous signal for the McACMP, thus the trigger pulse width needs to be at least one clock cycle wide.

- **Edge sensitive PUP mode:** The McACMP begins one sampling sequence when a rising edge is detected at the PUP input and then enter an idle state.
- **Level sensitive PUP mode:** The McACMP begins the sampling sequence when a high signal is detected at the PUP input and continuously sample as long as PUP is high, and once PUP goes low, the McACMP finishes the sampling sequence before entering an idle state.

Output synchronicity:

- **Simultaneous:** Sampled outputs are latched and then appear at the respective channel output after the last channel is sampled.
- **Staggered:** Sampled outputs appears at the respective channel output as they are sampled.

Sampling edge select:

- **Negative edge:** samples are captured on the negative or falling edge of the clock.
- **Positive edge:** samples are captured on the positive or rising edge of the clock.

Sequence restart/output latch reset: while the McACMP is running, a restart/reset signal can be asserted to restart the sampling sequence from channel 0. Channels can also independently be selected to have the output latch data cleared when this signal is asserted. If the reset input is held low, the McACMP will continuously sample channel 0 regardless of Enable trigger mode, until the reset is released.

There is also a data ready output that asserts a high signal for one clock of the base clock frequency once all channels configured have been sampled. For example, if the 1kHz (2kHz/2) sampling clock is selected, the data ready pulse width is 500µs.

Figure 8-44 shows and example of a McACMP configured to sample channel 0 and channel 1 with 2 VREFs each and only channel 0 with the output latch reset enabled.

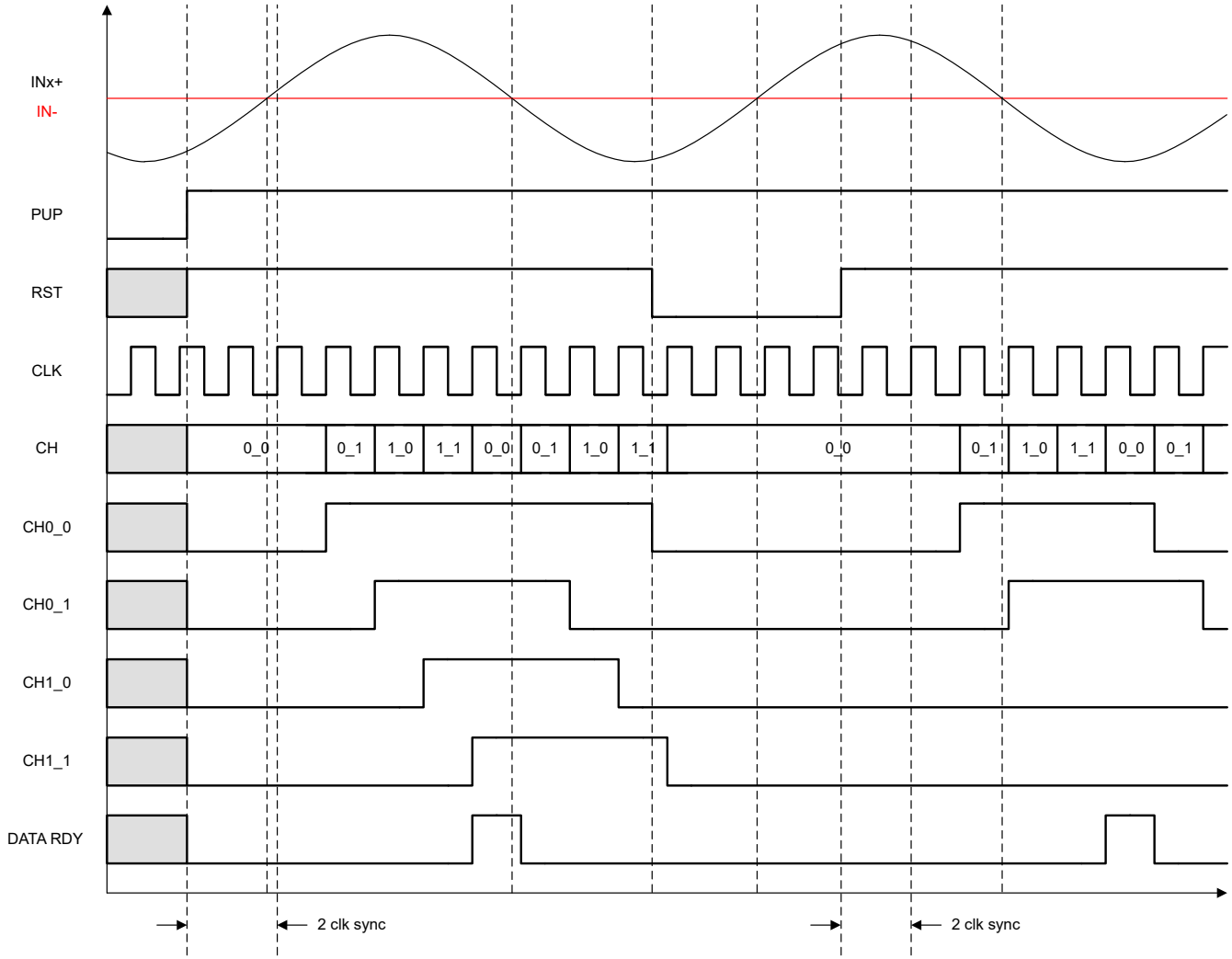

Figure 8-44. Multi-channel Sampling Comparator Timing Example

8.3.12 Voltage Reference (VREF)

The TPLD2001-Q1 has a voltage reference macro-cell to provide references to the analog comparators. This macro-cell provides a user selection of fixed voltage references from 32mV to 2.016V in 32mV increments or an externally supplied voltage reference from the External VREF AIO can be provided. The External VREF option is shared between all comparators and all channels of the McACMP.

When operating on a V_{CC} less than 2.3V, the maximum VREF option is reduced to V_{CC} - 0.3V; thus, the maximum VREF when operating at 1.8V supply is 1.504V.

The VREF selection per discrete analog comparator or per channel of the multi-channel sampling analog comparator can be updated in-system using the User Registers. For glitch-free measurements, it is recommended to disable/power down all analog comparators when changing the VREF. If the analog comparator is not disabled while the VREF selection is being updated, it can take up to the Analog Comparator t_{start} for valid data to be output from the analog comparators.

Table 8-24. VREF Selection Table

Bit Enumeration	VREF output
000000	32mV
000001	64mV
000010	96mV

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Table 8-24. VREF Selection Table (continued)

Bit Enumeration	VREF output
000011	128mV
000100	160mV
000101	192mV
000110	224mV
000111	256mV
001000	288mV
001001	320mV
001010	352mV
001011	384mV
001100	416mV
001101	448mV
001110	480mV
001111	512mV
010000	544mV
010001	576mV
010010	608mV
010011	640mV
010100	672mV
010101	704mV
010110	736mV
010111	768mV
011000	800mV
011001	832mV
011010	864mV
011011	896mV
011100	928mV
011101	960mV
011110	992mV
011111	1024mV
100000	1056mV
100001	1088mV
100010	1120mV
100011	1152mV
100100	1184mV
100101	1216mV
100110	1248mV
100111	1280mV
101000	1312mV
101001	1344mV
101010	1376mV
101011	1408mV
101100	1440mV
101101	1472mV
101110	1504mV
101111	1536mV

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Table 8-24. VREF Selection Table (continued)

Bit Enumeration	VREF output
110000	1568mV
110001	1600mV
110010	1632mV
110011	1664mV
110100	1696mV
110101	1728mV
110110	1760mV
110111	1792mV
111000	1824mV
111001	1856mV
111010	1888mV
111011	1920mV
111100	1952mV
111101	1984mV
111110	2016mV
111111	Ext. VREF AIO

Table 8-25. VREF Range

V_{CC}	VREF Range
1.71V - 2.3V	32mV - 1.504V
2.3V - 5.5V	32mV - 2.016V

8.3.13 Analog Temperature Sensor (TS)

The TPLD2001-Q1 has an Analog temperature sensor (TS) macro-cell that operates from -40°C to +125°C. The linear transfer function has a slope of -0.0044V/°C (typical) and an output voltage of 1.061V (typical) at 0°C.

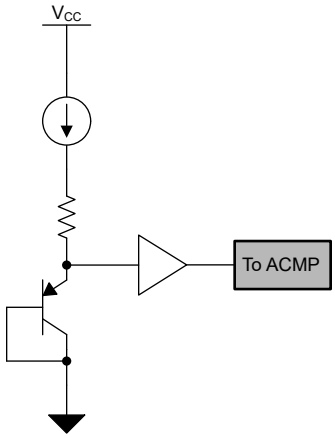

Figure 8-45. Analog temperature sensor block diagram

The formula to convert from temperature (T, in Celsius) to sensor output (V_{out}, in volts) is:

$$V_{out} = [-0.0044 \times T] + 1.061 \quad (4)$$

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8.3.14 Analog Multiplexer (AMUX)

The TPLD2001-Q1 has two Analog multiplexer (AMUX) macro-cells that operate as break-before-make, single-pole double-throw (SPDT) analog switches. This AMUX can handle both analog and digital signals and permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

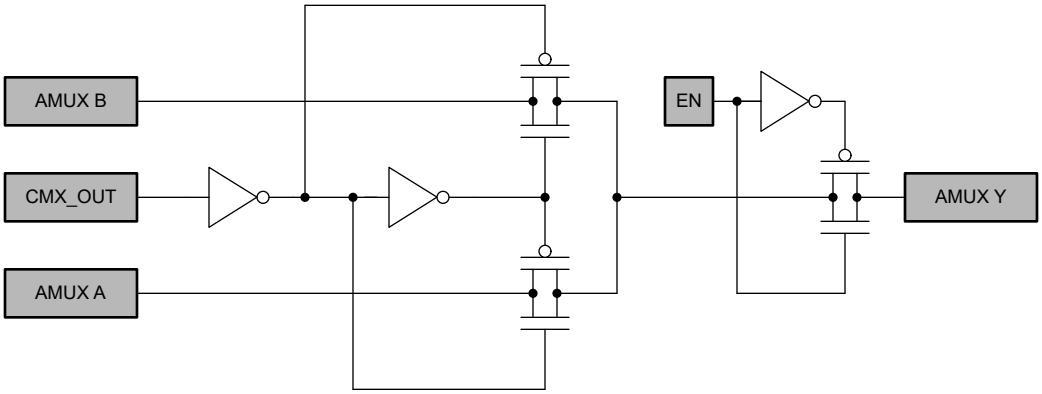

Figure 8-46. Analog multiplexer block diagram

Either the A channel or the B channel is activated depending upon the control input from the connection mux. If the control input is Low, A channel is selected. If the control input is High, B channel is selected.

Table 8-26. AMUX Function Table

Control input (CMX_OUT)	On channel
Low	AMUX Y = AMUX A
High	AMUX Y = AMUX B

8.3.15 Oscillators

The TPLD2001-Q1 has three internal oscillators, OSC0 is fixed to 2kHz, OSC1 is fixed to 2MHz, and OSC2 is fixed to 25MHz. The user can also bypass in the internal oscillators and the operating frequency can come from an external clock input coming from an IO.

8.3.15.1 2kHz Fixed Frequency Oscillator

The TPLD2001-Q1 has one internal oscillator operating at 2kHz. The user can use the oscillator at this operating frequency for the OSC macro-cell, or the internal oscillator can be bypassed and the operating frequency can come from an external clock.

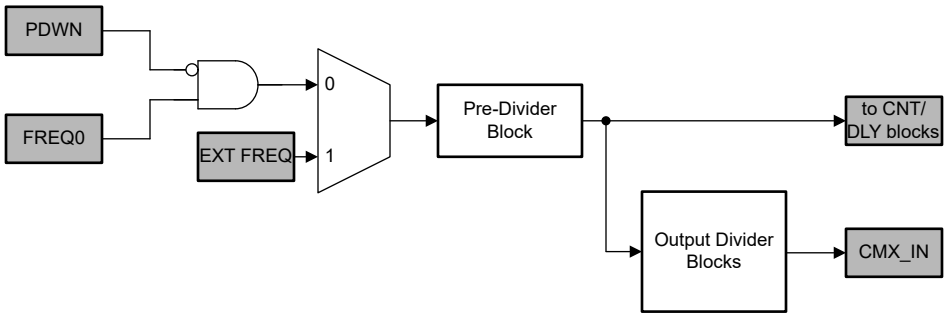

Figure 8-47. Fixed frequency oscillator block diagram

Following the operating clock input, there are two divider stages that allow users the flexibility of various clock frequencies for use throughout the device.

The first stage divider allows the selection of up to four options from the operating oscillator frequency as listed in Table 8-28. The output of the first divider stage is routed directly to the counter/delay generator macro-cell CLK inputs, where a separate second divider stage is available.

The output of the first divider stage is also routed into a second divider stage within the oscillator macro-cell. The oscillator macro-cell has a separate second stage divider, with an output (OUT0) into the connection mux, see Table 8-29.

Table 8-27. Frequency Options and Limits

Frequency Option	MIN	TYP	MAX
FREQ0	1.9kHz	2kHz	2.1kHz
EXT	-	-	25MHz

Table 8-28. Oscillator Pre-dividers

Pre-Divider Option	Magnitude
P0	1
P1	2
P2	4
P3	8

Table 8-29. Oscillator Output Dividers

Output Divider Options	Magnitude
OD0	1
OD1	2
OD2	3
OD3	4
OD4	8
OD5	12

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Table 8-29. Oscillator Output Dividers (continued)

Output Divider Options	Magnitude
OD6	24
OD7	64

8.3.15.2 2MHz Fixed Frequency Oscillator

The TPLD2001-Q1 has one internal oscillator operating at 2MHz. The user can use the oscillator at this operating frequency for the OSC macro-cell, or the internal oscillator can be bypassed and the operating frequency can come from an external clock.

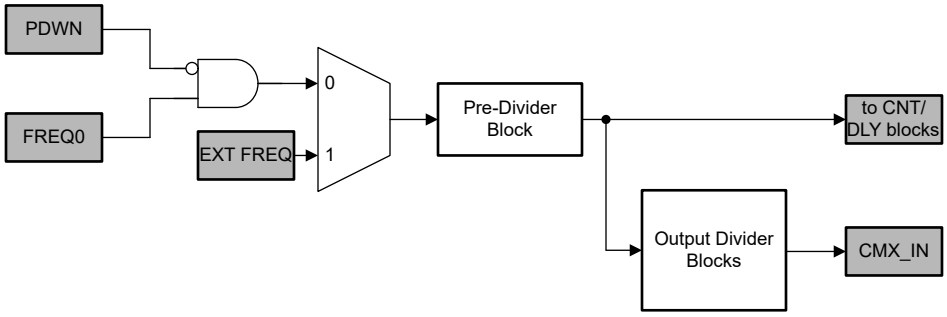

Figure 8-48. Fixed frequency oscillator block diagram

Following the operating clock input, there are two divider stages that allow users the flexibility of various clock frequencies for use throughout the device.

The first stage divider allows the selection of up to four options from the operating oscillator frequency as listed in Table 8-31. The output of the first divider stage is routed directly to the counter/delay generator macro-cell CLK inputs, where a separate second divider stage is available.

The output of the first divider stage is also routed into a second divider stage within the oscillator macro-cell. The oscillator macro-cell has a separate second stage divider, with an output (OUT0) into the connection mux, see Table 8-32.

Table 8-30. Frequency Options and Limits

Frequency Option	MIN	TYP	MAX
FREQ0	1.9MHz	2MHz	2.1MHz
EXT	-	-	25MHz

Table 8-31. Oscillator Pre-dividers

Pre-Divider Option	Magnitude
P0	1
P1	2
P2	4
P3	8

Table 8-32. Oscillator Output Dividers

Output Divider Options	Magnitude
OD0	1
OD1	2
OD2	3
OD3	4
OD4	8

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Table 8-32. Oscillator Output Dividers (continued)

Output Divider Options	Magnitude
OD5	12
OD6	24
OD7	64

8.3.15.3 25MHz Fixed Frequency Oscillator

The TPLD2001-Q1 has one internal oscillator operating at 25MHz. The user can use the oscillator at this operating frequency for the OSC macro-cell, or the internal oscillator can be bypassed and the operating frequency can come from an external clock.

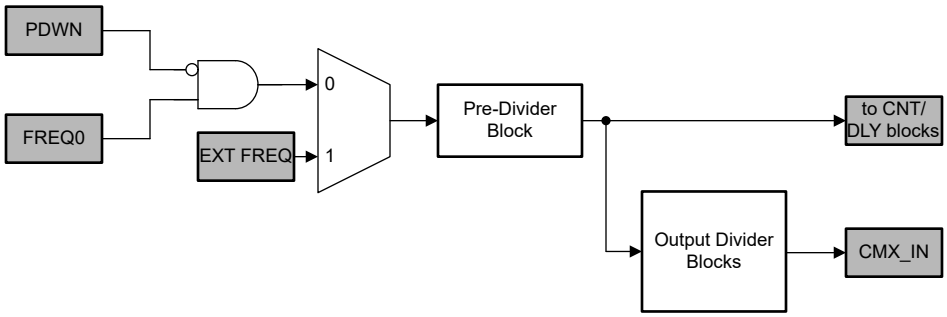

Figure 8-49. Fixed frequency oscillator block diagram

Following the operating clock input, there are two divider stages that allow users the flexibility of various clock frequencies for use throughout the device.

The first stage divider allows the selection of up to four options from the operating oscillator frequency as listed in Table 8-34. The output of the first divider stage is routed directly to the counter/delay generator macro-cell CLK inputs, where a separate second divider stage is available.

The output of the first divider stage is also routed into a second divider stage within the oscillator macro-cell. The oscillator macro-cell has a separate second stage divider, with an output (OUT0) into the connection mux, see Table 8-35.

Table 8-33. Frequency Options and Limits

Frequency Option	MIN	TYP	MAX
FREQ0	23.75MHz	25MHz	26.25MHz
EXT	-	-	25MHz

Table 8-34. Oscillator Pre-dividers

Pre-Divider Option	Magnitude
P0	1
P1	2
P2	4
P3	8

Table 8-35. Oscillator Output Dividers

Output Divider Options	Magnitude
OD0	1
OD1	2
OD2	3
OD3	4

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Table 8-35. Oscillator Output Dividers (continued)

Output Divider Options	Magnitude
OD4	8
OD5	12
OD6	24
OD7	64

8.3.15.4 Oscillator Power Modes

When using any of the device's internal oscillator, there are three power modes available for each oscillator:

- **Auto power on (CTRL_SRC = 0 and PWR_MODE = 0):** the internal oscillator is triggered when any macro-cell that requires the oscillator is running and then power off once the task is complete.
- **Force power on (CTRL_SRC = 0 and PWR_MODE = 1)**: the internal oscillator continuously runs as long as the device is powered on.
- **External power on/off (CTRL_SRC = 1, CTRL_SEL = 0, and PWR_MODE = 1)**: a High input into the PDWN input powers down the oscillator and a Low powers on the oscillator.

These power modes are only applicable when the internal oscillator is selected and is bypassed when an external clock (SRC_SEL = 1) is used. While the internal oscillator is powered off, all pre-dividers and secondary state dividers are in a paused state.

8.3.16 Serial Communications

The TPLD2001-Q1 has a serial communications macro-cell for in-system updates to configuration registers via the user registers.

The user registers allow for reading of the Device ID, Program ID, current Counter COUNT, current Counter DATA, Watchdog Timer DATA, Watchdog Timer Status, Pattern Generator DATA, State Machine Status and Output DATA, Voltage Reference Selections for the Analog Comparators, Virtual Inputs, and Virtual Outputs. See the User Registers register map for associated addresses.

By writing to the respective registers, the current Counter DATA, Watchdog Timer DATA, Pattern Generator DATA, State Machine Output DATA, Voltage Reference Selections, and Virtual Inputs can be updated in-system.

This macro-cell can configure the TPLD2001-Q1 as an I^{2}C or SPI device.

8.3.16.1 I^{2}C Mode

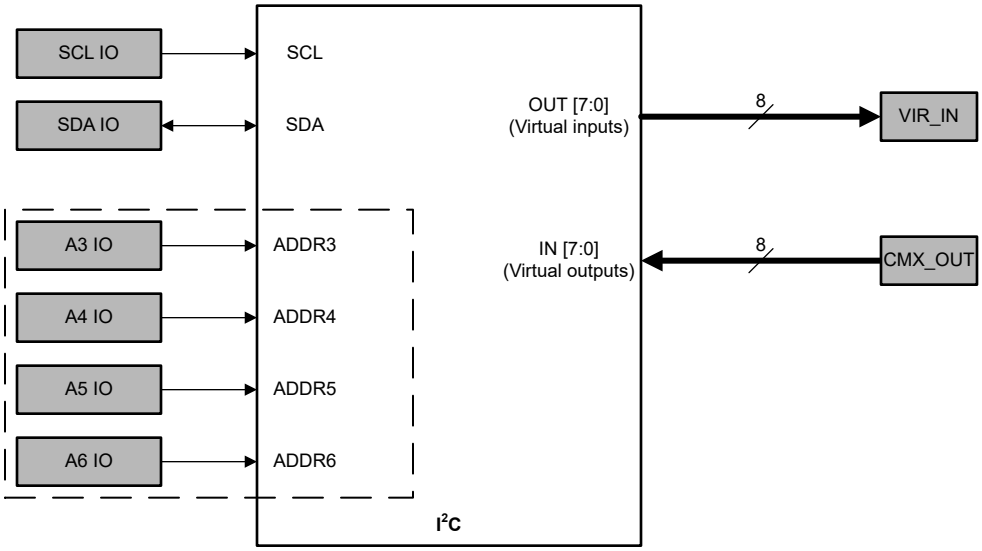

Figure 8-50. I^{2}C Serial Communications GPIO Allocation

When configured to I²C, the following IOs are used by the macro-cell:

- IO6: SCL
- IO7: SDA
- IO5: HW defined ADDR 3, A3 (optional)
- IO4: HW defined ADDR 4, A4 (optional)
- IO3: HW defined ADDR 5, A5 (optional)
- IO2: HW defined ADDR 6, A6 (optional)

The TPLD2001-Q1 supports:

- Peripheral/Target mode only
- Standard mode, Fast mode, and Fast mode plus
- Configurable 4-bit hardware address by IO or by OTP memory

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer only initiates when the bus is not busy.

The target device address of the TPLD is derived from the OTP and the most significant byte have an option to come from IOs, which the TPLD samples the IOs only at power up of the TPLD device, which allows use of the respective GPIO as a digital input within a circuit design. There is also an option to enable IO latching to continuously sample while powered on by setting the I2C_IO_LAT bit to logic 1.

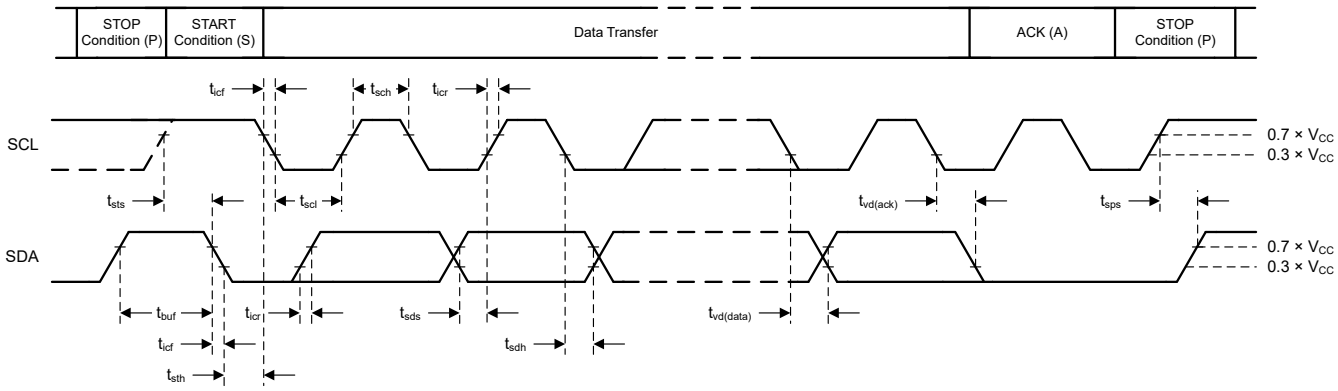

Figure 8-51. I²C Read/Write Timing Diagram

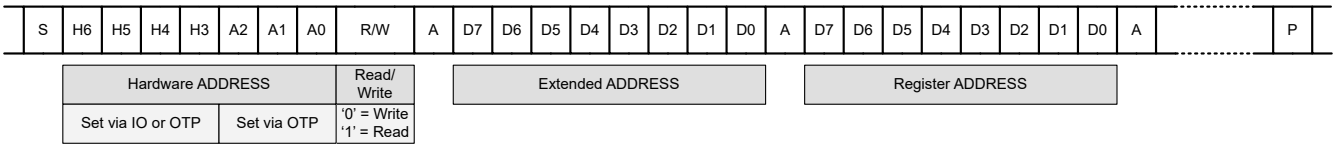

Figure 8-52. TPLD I²C Frame and Formatting

I²C communication with this device is initiated by a controller sending a START condition, a high-to-low transition on the SDA input/output, while the SCL input is high. After the START condition, the device hardware address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address input of the responder device must not be changed between the START and the STOP conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP).

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A STOP condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller.

Any number of data bytes can be transferred from the transmitter to receiver between the START and the STOP conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a responder receiver is addressed, the responder receiver must generate an ACK after each byte is received. Similarly, the controller must generate a NACK after each byte that the controller receives from the responder transmitter. Setup and hold times must be met for proper operation.

A controller receiver signals an end of data to the responder transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the responder. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a STOP condition.

When writing or reading from the TPLD2001-Q1, there is an option to enable automatic address incrementing by writing a logic 0 to bit 0 of address 0x0FD. This can be disabled by writing a logic 1. Note, for I^{2}C, the address auto-increment only works within a specific extended, or page, address. Thus, if burst read or write is used, keep in mind 0x0FF rolls over to 0x000.

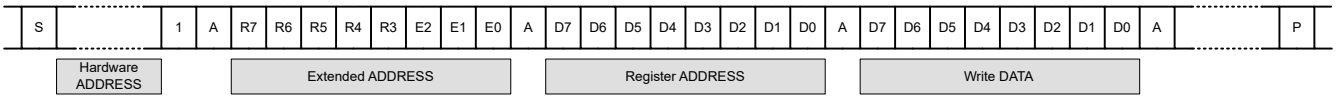

Figure 8-53. TPLD I^{2}C Write Command Formatting

To transmit data or write to the TPLD2001-Q1, the bus controller must send the device hardware address and set the least significant bit (LSB) to a logic 0. The next two bytes set the register address and then the write data follows. There is no limitation on the number of data bytes sent in one write frame.

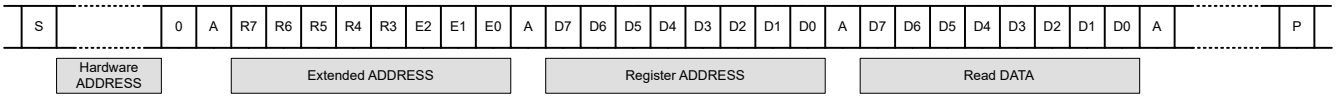

Figure 8-54. TPLD I^{2}C Read Command Formatting

To read from the TPLD2001-Q1, the bus controller first must send the TPLD2001-Q1 hardware address with the LSB set to a logic 1. The byte that follows contains the data in the address previously written to, or the next address if address auto-increment is enabled.

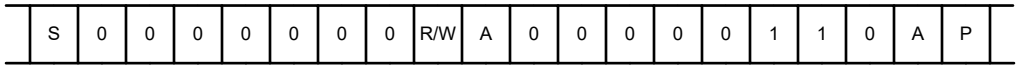

Figure 8-55. TPLD I^{2}C Software Reset Command

The Software Reset call is a command sent from the controller on the I2C bus that instructs all devices that support the command to be reset to the power-up default state and listening for the Software Reset call can be enabled by setting the I2C_RST_EN bit to logic 1. For the Software Reset to function as expected, the I^{2}C bus must be functional and no devices can be hanging the bus.

The software Reset call is defined as the following steps:

1. A START condition is sent by the I^{2}C bus controller.
2. The address used is the reserved General Call I^{2}C bus address '0000 000' with the R/W bit set to 0. The byte sent is 0x00.
3. Any devices supporting the General Call functionality ACK. If the R/W bit is set to 1 (read), the device NACK.
4. Once the General Call address is acknowledged, the controller sends only 1 byte of data equal to 0x06. If the data byte is any other value, the device does not acknowledge nor reset. If more than 1 byte is sent, no more bytes are acknowledged and the device ignores the I^{2}C message considering it invalid.

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5. After the 1 byte of data (0x06) is sent, the controller sends a STOP condition to end the Software Reset call sequence. A repeated START condition is ignored by the device and no reset can be performed.

Once the above steps are completed successfully, the device performs a reset, clearing all register values back to power-on defaults.

8.3.16.2 SPI Mode

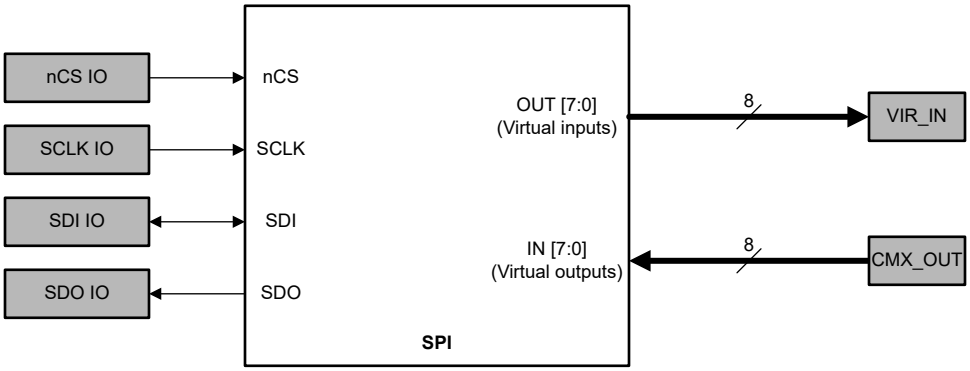

Figure 8-56. SPI Serial Communications GPIO Allocation

When configured to SPI, the following IOs are used by the macro-cell:

- IO5: nCS
- IO6: SCLK
- IO7: SDI
- IO8: SDO

The TPLD2001-Q1 supports:

- Peripheral/Target mode only
- SPI mode 0, that is, SCLK is idle Low and SDI/SDO is valid on the rising edge of SCLK
- Up to 4MHz SCLK
- 8-bit data frame size

The SPI communication uses a standard SPI. Physically, the digital interface pins are nCS (Chip select not), SDI (Serial Data In), SDO (Serial Data Out), and SCLK (SPI Clock).

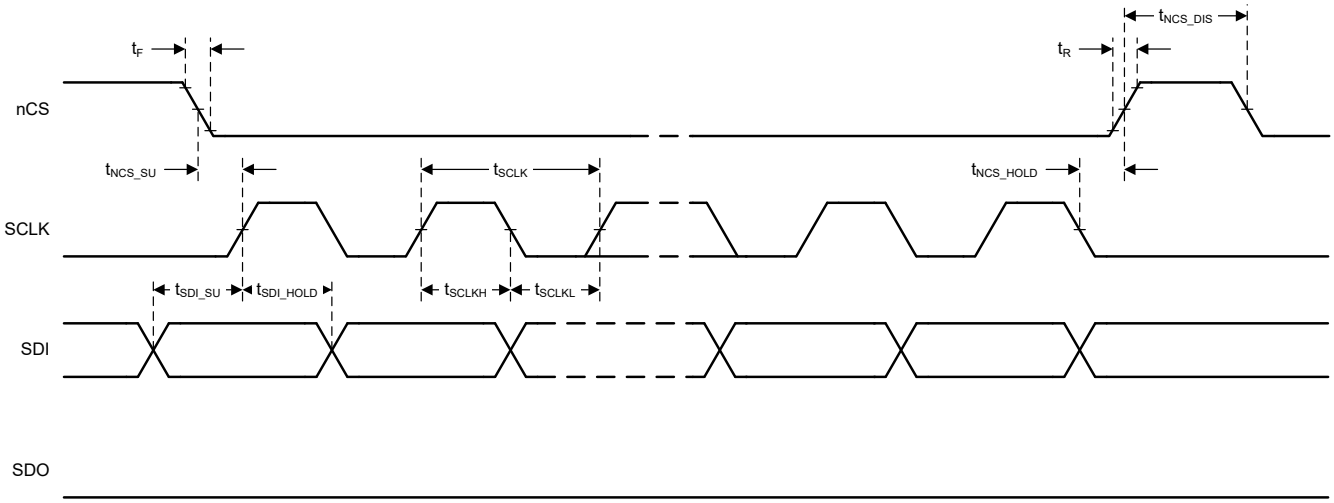

Figure 8-57. SPI Write Timing Diagram

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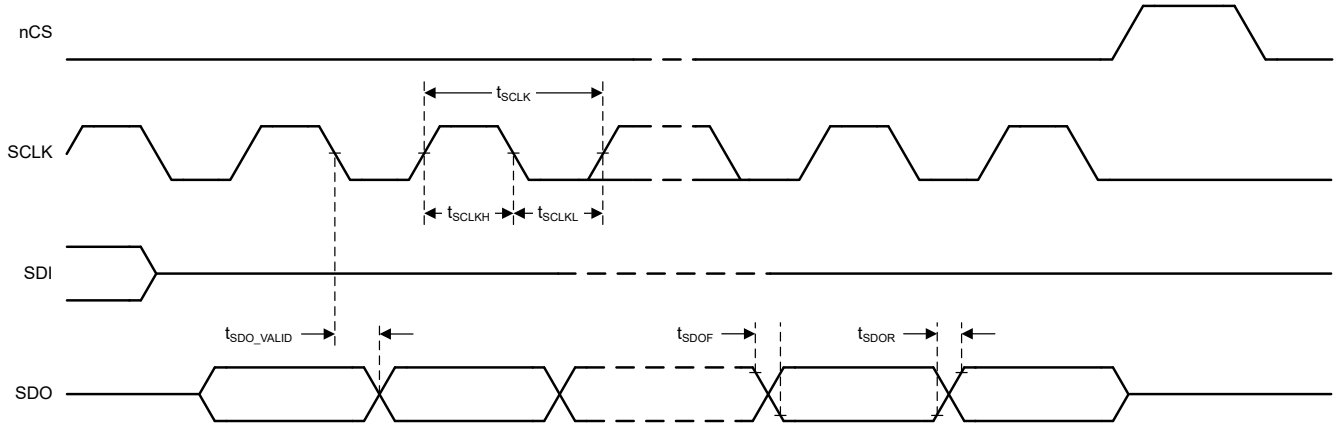

Figure 8-58. SPI Read Timing Diagram

The SPI module in TPLD2001-Q1 supports mode 0, thus input data on the SDI line is sampled on the rising edge of SCLK. The SPI output data on the SDO line is changed on the falling edge of SCLK.

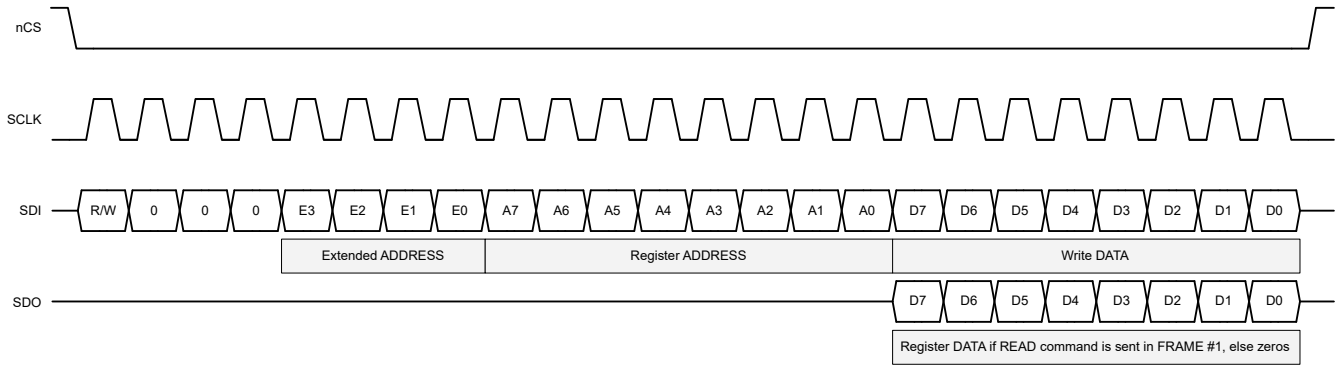

Figure 8-59. TPLD SPI Frame and Formatting

Each SPI transaction is consists of a 1-bit command, a 7-bit extended address, an 8-bit target register address, and an 8-bit data field. The data shifted out on the SDO line contains the data that is stored in the set address with the READ command (R/W = 0). Data bytes shifted out during a WRITE command (R/W = 1) is content of the registers prior to the new data being written.

8.3.16.3 Virtual I/Os

Within the TPLD, this macro-cell has 8 inputs and 8 outputs to allow for reading of up to 8 digital macro-cell outputs and provide up to 8 virtual inputs to be used within the device.

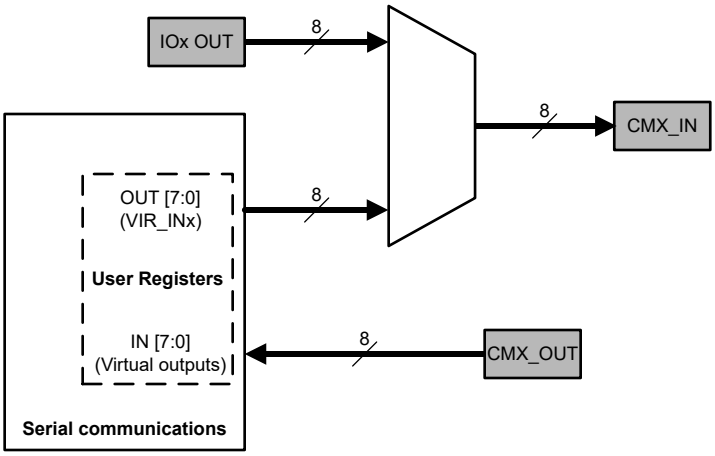

Figure 8-60. Serial Communications Block Diagram

The outputs of this macro-cell act as virtual inputs into the device. The routing of the signal into the Connection Mux is shared with the physical digital input pins, so if a virtual input is used, the digital input pin resource is no longer available and the Connection Mux input is sourced from the Virtual Input register. Table 8-36 shows the shared resource between the digital input pin and the virtual input.

Table 8-36. Digital IO and Virtual In Shared Resources

Virtual input	VIR_IN0	VIR_IN1	VIR_IN2	VIR_IN3	VIR_IN4	VIR_IN5	VIR_IN6	VIR_IN7
Digital input pin	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8

Using the virtual inputs and virtual outputs, the TPLD can be configured for 8-bit serial-to-parallel GPIO expansion or parallel-to-serial buffering.

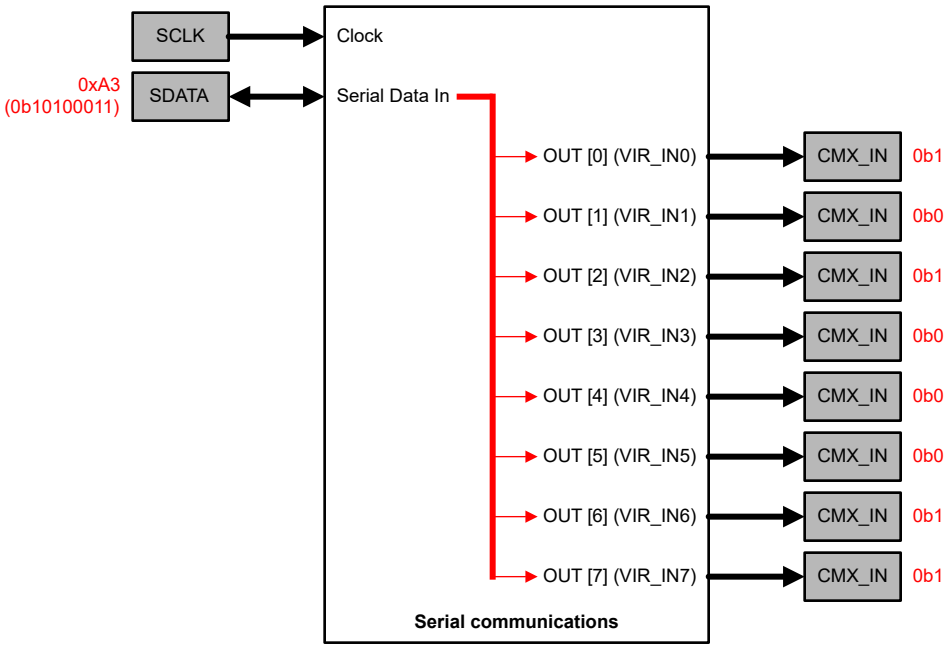

Figure 8-61. Serial Communications for Serial-to-Parallel I/O Expander Block Diagram

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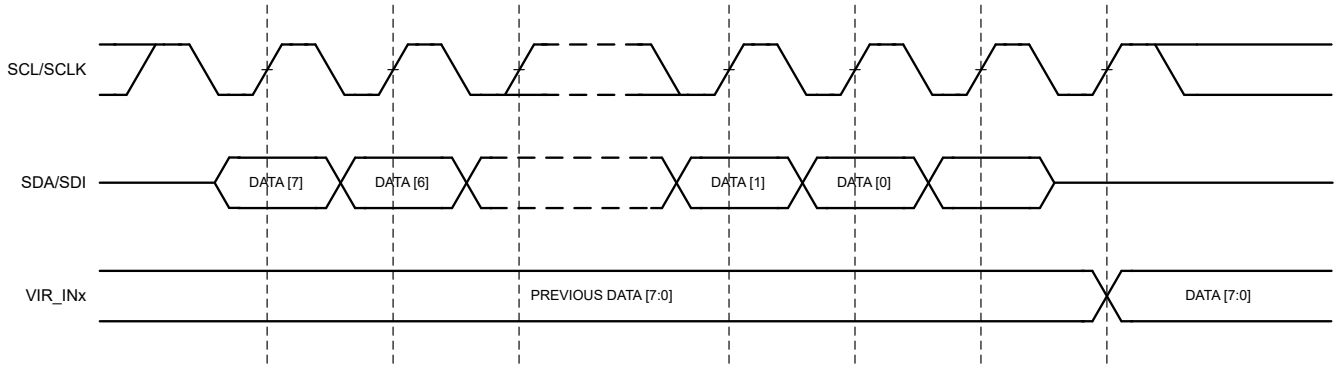

Figure 8-62. Serial Communications for Serial-to-Parallel I/O Expander Timing Example

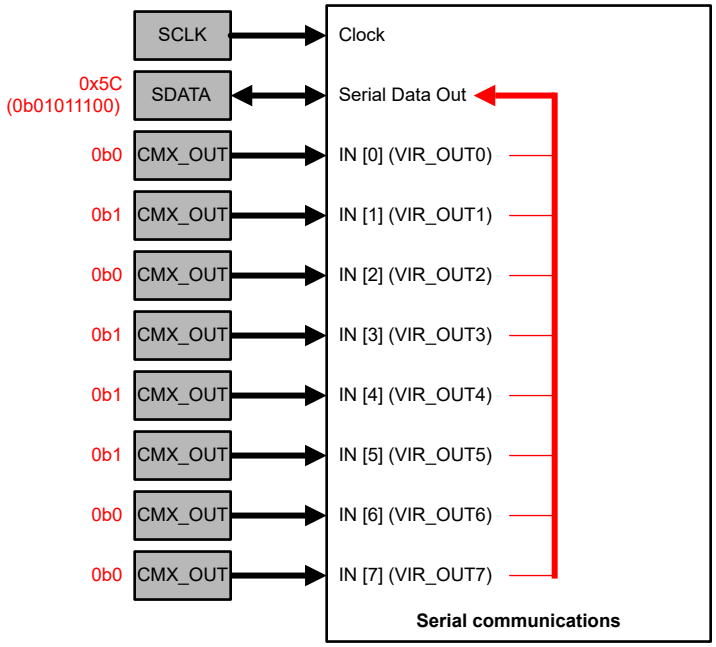

Figure 8-63. Serial Communications for Parallel-to-Serial Block Diagram

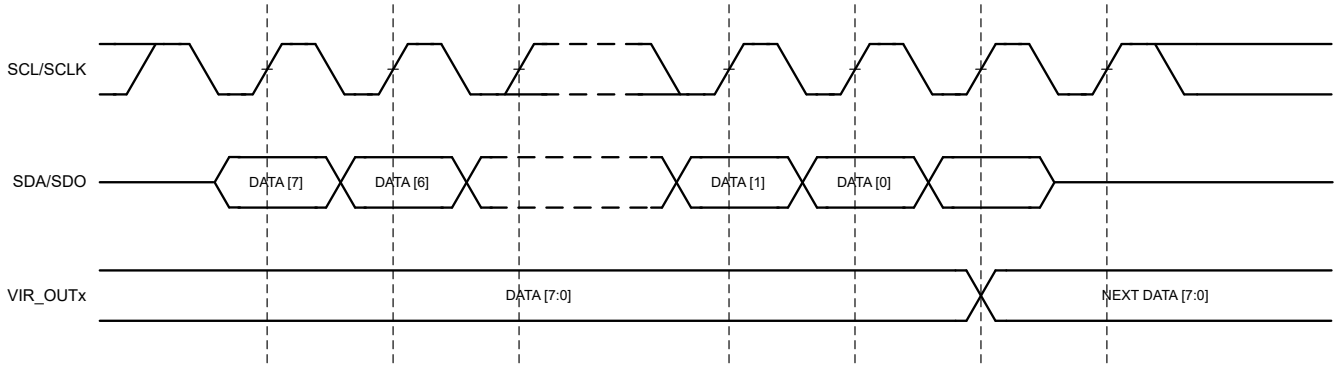

Figure 8-64. Serial Communications for Parallel-to-Serial Timing Example

8.4 Device Functional Modes

8.4.1 Power-On Reset

The TPLD2001-Q1 has a power-on reset (POR) macro-cell to ensure correct device initialization and operation of all macro-cells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{CC} power is first ramping to the device, and also while the V_{CC} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macro-cells inside the device, and finally to the state of the I/O pins.

The power-on Reset (POR) macro-cell produces a logic HIGH signal as an output when the device power supply (V_{CC}) rises to approximately V_{PORR} and device completely starts up. All outputs are in high impedance state and chip starts loading data from OTP. The reset signal is released for internal macro-cells and all the registers are initialized to the default states. Figure 8-65 shows POR system generates a sequence of signals that enable certain macro-cells.

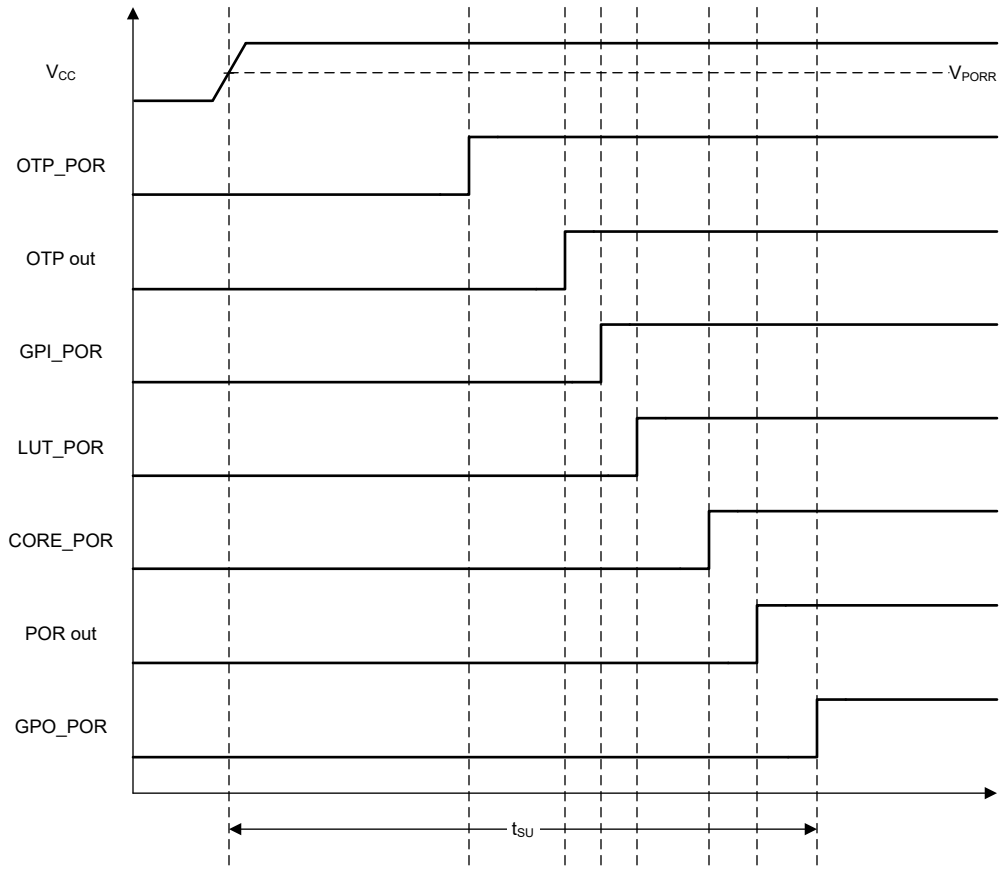

Figure 8-65. POR Sequence

As can be seen from Figure 8-65 after the V_{CC} has start ramping up and crosses the V_{PORR} threshold,

- First, the on-chip RAM is reset.
- Next the chip (TPLD2001-Q1) reads the data from OTP, and transfers this information to RAM (registers) that serve to configure each macro-cell, and the connection mux which routes signals between macro-cells.
- The third stage causes the reset of the input pins (GPIOs that are configured as Inputs), and then to enable them.
- After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches, and Pipe Delay are initialized.
- After all macro-cells are initialized internal POR signal (POR macro-cell output) goes from LOW to HIGH.
- The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

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GPIO quick charge: If enabled, during the POR sequence, a 2kΩ resistor is connected between the GPIO and GND to precondition the GPIO.

Initialization: All internal macro-cells by default have initial low level. Starting from when $V_{CC} > V_{PORR}$, macro-cells in the TPLD2001-Q1 are powered on and forced into a reset state. All outputs are in Hi-Z and the chip starts loading data from OTP. Then the reset signal is released for internal macro-cells and they begin to initialize according to the following sequence:

- Input pins, analog comparators, pull up/pull down resistors
- LUTs
- DFFs, Delays/Counters, pipe delay
- POR output to matrix
- Output pin corresponds to the internal logic

The POR signal going high indicates the mentioned power-up sequence is complete.

8.4.2 Power Supply Control Modes

The TPLD2001-Q1 has the option to control the power mode of the Bandgap Voltage and the Prebias Voltage. It is recommended to keep these bits to 000 (Auto on/off); however, if analog macro-cells (for example, oscillators, analog comparators) are not used, these settings can be used to power off the Bandgap and Prebias Voltages to further reduce the power consumption of the device.

Table 8-37. Bandgap Voltage Power Control Modes

Control code	Bit description
000	Auto ON for: • Oscillators • Analog Comparators • Voltage Reference • Temperature Sensor • PWM Generator/Watchdog Timer/State Machine not using "External CLK from CMX" Except Force ON if any Counter is used
001	Auto ON for: • Oscillators • Analog Comparators • Voltage Reference • Temperature Sensor • Any Counter/PWM Generator/Watchdog Timer/State Machine not using "External CLK from CMX"
01X	Force ON
1XX	Force OFF

Table 8-38. Prebias Voltage Power Control Modes

Control code	Bit description
000	Auto ON for: • Oscillators • Analog Comparators • Voltage Reference • Temperature Sensor • Any Counter/PWM Generator/Watchdog Timer/State Machine not using "External CLK from CMX" Except Force ON if any DFF or any Counter/PWM Generator/ Watchdog Timer/State Machine configured with "External CLK from CMX" is used in the design
001	Auto ON for: • Oscillators • Analog Comparators • Voltage Reference • Temperature Sensor • Any Counter/PWM Generator/Watchdog Timer/State Machine not using "External CLK from CMX" • Any active Serial Communications transaction
01X	Force ON
1XX	Force OFF

8.4.3 Protection Features

The TPLD2001-Q1 has some protection features including read/write protection for device configuration bits and CRC error detection on the internal OTP.

8.4.3.1 Device Read/Write Lock

The TPLD2001-Q1 implements lock features that enables device read-back protection for secure applications and prevents an accidental or unintended write to the TPLD2001-Q1 registers. There are three bits in the OTP that allows the user to define rules for reading and writing through the serial communications interface:

- **Configuration register (CFG) read (RD) lock**: the CFG RD lock, if set, blocks all read commands of the configuration registers through the serial communications interface and respond with 0's.
- **Configuration register (CFG) write (WR) lock**: the CFG WR lock, if set, blocks all write commands to the configuration registers through the serial communications interface.
- **User register (USER) lock**: the USER lock consists of two bits and, depending on bit setting, blocks write commands to the user register space through the serial communications interface to specific register addresses and any changes requested is denied (no changes are made to the configuration registers).

Table 8-39. User Register Lock Access Type Enumeration

Register	Lock bits						
	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b00	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b01	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b10	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b11	CFG RD lock = 0b1 CFG WR lock = 0b0 USER lock = 0bXX	CFG RD lock = 0b0 CFG WR lock = 0b1 USER lock = 0bXX	CFG RD lock = 0b1 CFG WR lock = 0b1 USER lock = 0bXX
Device ID (0x000 - 0x003)	R	R	R	R	R	R	R

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Table 8-39. User Register Lock Access Type Enumeration (continued)

Register	Lock bits						
Program ID (0x004 - 0x007)	R	R	R	R	R	R	R
Counter COUNT (0x010 - 0x01F)	R	R	R	R	—	R	—
Counter DATA (0x020 - 0x02F)	R/W	R/W	R	R	—	R/W	—
Watchdog Timer DATA (0x030 - 0x031)	R/W	R/W	R	R	—	R/W	—
Watchdog Timer Status (0x032)	R	R	R	R	—	R	—
Pattern Generator (0x040 - 0x041)	R/W	R/W	R	R	—	R/W	—
State Machine (0x050 - 0x05F)	R/W	R	R/W	R	—	R/W	—
Voltage Reference select for Analog Comparator (0x070 - 0x07F)	R/W	R	R	R/W	—	R/W	—
Virtual Input (0x0E0)	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Virtual Output (0x0E1)	R	R	R	R	R	R	R
CRC Status (0x0FE)	R	R	R	R	R	R	R
Configuration Registers (0x200 - 0x3FF)	R/W	R/W	R/W	R/W	W	R	—

Any write commands that come to the device via the serial communications interface that are not blocked, based on the protection bits, changes the contents of the configuration register that mirror the OTP bits. These write commands do not change the OTP bits themselves, and a POR event restores the register bits to original programmed contents of the OTP.

8.4.3.2 OTP Cyclic Redundancy Check (CRC)

Cyclic Redundancy Checks (CRCs) is a common method of performing error checking on areas of OTP and verifying data integrity of this memory. OTP is used to configure the macro-cells and connection mux routing of the TPLD2001-Q1. The OTP is one-time programmable and holds the device configuration data. OTP memory is loaded during device power up and transferred to TPLD2001-Q1 connection mux.

To verify the bit integrity of the OTP memory before the stored configuration is loaded from OTP to device registers, as a safety measure, TPLD2001-Q1 implements a cyclic redundancy check (CRC) feature for the OTP to make sure that the data stored in the OTP is uncorrupted. At start-up, the OTP is read internally and checks for a valid CRC. If the CRC is not valid, this process is performed for a total of 7 more times. If still not valid after the 8th attempt, the device proceeds with loading the contents from OTP but sets the following status bits:

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CRC_ERR_CNT bits:

The CRC_ERR_CNT bits in register 0x0FEh [7:5] indicate the number of failed CRC attempts before loading the OTP contents into the configuration of the device.

CRC_ERR_FLAG bit:

The CRC_ERR_FLAG bit in register 0x0FEh [0] indicates there are more than 8 CRC calculation failures in the loading of the OTP contents into the configuration of the device.

8.4.4 Programming

The TPLD2001-Q1 is programmed through a I^2C or SPI.

In the programmed case for the TPLD2001-Q1 device, the configuration choices made by the user are stored as bit settings in the OTP, and this information is transferred at startup time to connection mux registers that enable the configuration of the macro-cells and for setting the connections in the connection mux to route signals in the manner most appropriate for the user's application.

8.4.4.1 Selectable I^2C/SPI

In an unprogrammed TPLD2001-Q1 device, the Interface Select pin (IO1) is sampled at device power up to determine the interface the TPLD boots up with after t_{SU} (max).

When the pin is tied to GND (logic low) or left floating, the TPLD2001-Q1 is configured with a I^2C interface with the first four bits of the target address determined by the respective HW Addr IO and the next three bits default to 001b, or ADDR = [A6][A5][A4][A3][0][0][1].

When the pin is tied to VCC (logic high), the TPLD2001-Q1 is configured with a SPI.

In a programmed device (one in which the OTP has been burned), this setting is overwritten by the selection stored in the OTP memory.

I2C_EN	SPI_EN	Interface enabled
0	0	Device is unprogrammed (blank)
0	1	SPI
1	0	I^2C
1	1	Neither I2C nor SPI, pins are GPIOs

8.4.4.2 Configuration Memory and One-Time Programmable Memory Programming

The TPLD2001-Q1 contains one-time programmable (OTP) memory bits. These memory bits retain the set values in the absence of a power supply, are used to configure the TPLD device, and can be programmed a maximum of one time. The default values for all the configuration registers in the TPLD2001-Q1 are loaded from OTP after a POR event is issued.

Procedure to temporarily set up configuration registers:

1. After starting up the device with the desired serial communications protocol, read the DEVICE_ID from registers 0x000 and 0x001 to verify communication with the device is established
2. Then:
   a. For SPI, send the following four frames with at least 200µs between frames: 0x9000B9, 0x90003E, 0x9000AF, 0x900058
   b. For I^2C, in four write transactions, send the following with at least 500µs between transactions:
      i. Transaction 1: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0xB9
      ii. Transaction 2: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0x3E
      iii. Transaction 3: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0xAF
      iv. Transaction 4: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0x58
3. After the final frame is sent, wait 1ms.

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4. Verify the correct configuration mode is entered correctly by reading 0x10 from register 0x400.
5. Write 0x02 to register 0x400.
6. Send configuration bits to 0x200 - 0x3FF.
7. Optionally, after sending configuration bits, read commands can be used to verify the correct data is written to the device.
8. Then:
   a. For SPI, send the following frame: 0x90004B
   b. For I^2C, send the following write transaction: BYTE0 = ADDR, BYTE1 = 01, BYTE2 = 0x4B
9. Lastly, write 0x00 to register 0x400 for the configuration to take effect.
10. Device is now temporarily configured.

Note

When temporarily configuring the TPLD with the I^2C macro-cell enabled, the first four bits of the target address is set to 0000b and the next three bits comes from the configuration bits, or ADDR = [0][0][0][0][A2][A1][A0]. An OTP burn is necessary to change the first four bits, or MSB, of the target address.

To change the temporary configuration, TI recommends to power cycle the device and repeating the procedure to temporarily set up the configuration registers.

If the device is already temporarily configured with the I^2C macro-cell enabled, writes to the I2C_ADDR register (SER_COMM_CFG1) takes immediate effect. Thus, subsequent I^2C transactions need to be addressed to the updated target address.

Procedure to burn the OTP:

1. If the device has been temporarily configured, power cycle the device to clear configuration registers before continuing.
2. Follow steps 1 - 7 from the procedure to temporarily set up configuration registers.
3. Apply V_{PP} to the GPI pin.
4. Write 0x01 to register 0x401 to start the OTP programming.
5. Wait t_{PP} for the programming to be complete.
6. Remove V_{PP} from the GPI pin.
7. Device OTP is now burned.

8.4.4.3 Intel HEX File Format

InterConnect Studio generates the configuration bits in Intel HEX format. The .hex file can be parsed to extract the datastream to configure the TPLD device. The Intel HEX record, or line of text, structure is shown below.

Table 8-40. Record structure example

:	10	0200	00	000102030405060708090A0B0C0D0E0F	76
Start code	Byte count	Address	Record type	Data	Checksum

- **Start code:** one character, an ASCII colon (:).
- **Byte count:** two hex digits to indicate the number of bytes in the Data field.
- **Address:** four hex digits to represent the starting address offset of the first Data byte.
- **Record type:** two hex digits defining the meaning of the Data field. While Intel HEX has six standard record types, only two are used in the .hex file generation.
  - **Hex code 00:** indicates Data record type; the example record structure above results in a Byte count of 0x10 (16 bytes), starting Address of 0x0200, and Data (0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, and 0x0F).
  - **Hex code 01:** indicates an End of File record type; the Byte count is 0x00, the Address is typically 0x0000, and the Data field is omitted.

- **Data:** contains the sequence of *Byte count* bytes of data.
- **Checksum:** two hex digits computed by taking the summation of each byte preceding the Checksum and computing the two's complement of the sum's least significant byte. This value can be used to verify the record has no errors.

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9 TPLD2001-Q1 Registers

The following section provides the registers accessible in the TPLD2001-Q1.

Note

Reads from and writes to the device are asynchronous; thus current counter count value may change by the time the read occurs depending on the speed of the clock used for the counter and of the serial communications interface.

Note

When updating counter data, it is recommended to put the counter in reset. If counters are not kept in a reset state, updates to CNT0 to CNT5 will not take affect until the next reset; whereas updates to CNT6 to CNT9 will take immediate affect.

After updating the counter data, two clocks are required to re-initialize the counter. If an External Clock option is used, provide the two clocks for proper operation of the counter.

9.1 TPLD2001_User Registers

Table 9-1 lists the memory-mapped registers for the TPLD2001_User registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. TPLD2001_USER Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	DEVICE_ID0	DEVICE_ID_MSB							
1h	DEVICE_ID1	DEVICE_ID_LSB							
2h	DEVICE_ID2	DEVICE_ID_RSVD							
3h	DEVICE_ID3	DEVICE_ID_REV							
4h	DEVICE_ID4	DEVICE_ID4							
5h	DEVICE_ID5	DEVICE_ID5							
6h	DEVICE_ID6	DEVICE_ID6							
7h	DEVICE_ID7	DEVICE_ID7							
10h	CNT0_COUNT	CNT0_COUNT							
11h	CNT1_COUNT	CNT1_COUNT							
12h	CNT2_COUNT	CNT2_COUNT							
13h	CNT3_COUNT	CNT3_COUNT							
14h	CNT4_COUNT_LSB	CNT4_COUNT_LSB							
15h	CNT4_COUNT_MSB	CNT4_COUNT_MSB							
16h	CNT5_COUNT_LSB	CNT5_COUNT_LSB							
17h	CNT5_COUNT_MSB	CNT5_COUNT_MSB							
18h	CNT6_COUNT	CNT6_COUNT							
19h	CNT7_COUNT	CNT7_COUNT							
1Ah	CNT8_COUNT	CNT8_COUNT							
1Bh	CNT9_COUNT	CNT9_COUNT							
20h	CNT0_DATA	CNT0_DATA							
21h	CNT1_DATA	CNT1_DATA							
22h	CNT2_DATA	CNT2_DATA							
23h	CNT3_DATA	CNT3_DATA							
24h	CNT4_DATA_LSB	CNT4_DATA_LSB							
25h	CNT4_DATA_MSB	CNT4_DATA_MSB							
26h	CNT5_DATA_LSB	CNT5_DATA_LSB							
27h	CNT5_DATA_MSB	CNT5_DATA_MSB							
28h	CNT6_DATA	CNT6_DATA							
29h	CNT7_DATA	CNT7_DATA							
2Ah	CNT8_DATA	CNT8_DATA							
2Bh	CNT9_DATA	CNT9_DATA							
30h	WDT_TIMEOUT_DATA	WATCHDOG_TIMEOUT_DATA							
31h	WDT_OUTPUT_DATA	WATCHDOG_OUTPUT_DATA							
32h	WDT_STATUS	RESERVED							WDT_STATUS
40h	PGEN_DATA_LSB	PGEN_DATA_LSB							
41h	PGEN_DATA_MSB	PGEN_DATA_MSB							
50h	STATE_MACHINE	RESERVED					CURRENT_STATE		
51h	STATE0_OUT	STATE0_OUT							
52h	STATE1_OUT	STATE1_OUT							
53h	STATE2_OUT	STATE2_OUT							
54h	STATE3_OUT	STATE3_OUT							
55h	STATE4_OUT	STATE4_OUT							
56h	STATE5_OUT	STATE5_OUT							
57h	STATE6_OUT	STATE6_OUT							
58h	STATE7_OUT	STATE7_OUT							
70h	VREF_ACMP0	RESERVED		VREF_ACMP0					
71h	VREF_ACMP1	RESERVED		VREF_ACMP1					
72h	VREF_ACMP2	RESERVED		VREF_ACMP2					
73h	VREF_ACMP3	RESERVED		VREF_ACMP3					

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Table 9-1. TPLD2001_USER Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
74h	VREF_McACMP0_0	RESERVED		VREF_McACMP0_0					
75h	VREF_McACMP0_1	RESERVED		VREF_McACMP0_1					
76h	VREF_McACMP1_0	RESERVED		VREF_McACMP1_0					
77h	VREF_McACMP1_1	RESERVED		VREF_McACMP1_1					
78h	VREF_McACMP2_0	RESERVED		VREF_McACMP2_0					
79h	VREF_McACMP2_1	RESERVED		VREF_McACMP2_1					
7Ah	VREF_McACMP3_0	RESERVED		VREF_McACMP3_0					
7Bh	VREF_McACMP3_1	RESERVED		VREF_McACMP3_1					
E0h	VIRTUAL_INPUT	VIRTUAL_IN							
E1h	VIRTUAL_OUTPUT	VIRTUAL_OUT							
FDh	SER_COMM_CFG	RESERVED							ADDR_INC
FEh	CRC_STATUS	ERR_CNT			RESERVED				ERR_FLAG
FFh	SER_COMM_WR_MASK	SER_COMM_WR_MASK							

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. TPLD2001_User Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.1.1 DEVICE_ID0 Register (Offset = 0h) [Reset = 20h]

DEVICE_ID0 is shown in Table 9-3.

Return to the Summary Table.

Table 9-3. DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_MSB	R	20h	

9.1.2 DEVICE_ID1 Register (Offset = 1h) [Reset = 01h]

DEVICE_ID1 is shown in Table 9-4.

Return to the Summary Table.

Table 9-4. DEVICE_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_LSB	R	1h	

9.1.3 DEVICE_ID2 Register (Offset = 2h) [Reset = 00h]

DEVICE_ID2 is shown in Table 9-5.

Return to the Summary Table.

Table 9-5. DEVICE_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_RSVD	R	0h	

9.1.4 DEVICE_ID3 Register (Offset = 3h) [Reset = 00h]

DEVICE_ID3 is shown in Table 9-6.

Return to the Summary Table.

Table 9-6. DEVICE_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_REV	R	0h	

9.1.5 DEVICE_ID4 Register (Offset = 4h) [Reset = X0h]

DEVICE_ID4 is shown in Table 9-7.

Return to the Summary Table.

Table 9-7. DEVICE_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID4	R	Xh	

9.1.6 DEVICE_ID5 Register (Offset = 5h) [Reset = X0h]

DEVICE_ID5 is shown in Table 9-8.

Return to the Summary Table.

Table 9-8. DEVICE_ID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID5	R	Xh	

9.1.7 DEVICE_ID6 Register (Offset = 6h) [Reset = X0h]

DEVICE_ID6 is shown in Table 9-9.

Return to the Summary Table.

Table 9-9. DEVICE_ID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID6	R	Xh	

9.1.8 DEVICE_ID7 Register (Offset = 7h) [Reset = X0h]

DEVICE_ID7 is shown in Table 9-10.

Return to the Summary Table.

Table 9-10. DEVICE_ID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID7	R	Xh	

9.1.9 CNT0_COUNT Register (Offset = 10h) [Reset = X0h]

CNT0_COUNT is shown in Table 9-11.

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Return to the Summary Table.

Table 9-11. CNT0_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT0_COUNT	R	Xh	

9.1.10 CNT1_COUNT Register (Offset = 11h) [Reset = X0h]

CNT1_COUNT is shown in Table 9-12.

Return to the Summary Table.

Table 9-12. CNT1_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT1_COUNT	R	Xh	

9.1.11 CNT2_COUNT Register (Offset = 12h) [Reset = X0h]

CNT2_COUNT is shown in Table 9-13.

Return to the Summary Table.

Table 9-13. CNT2_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT2_COUNT	R	Xh	

9.1.12 CNT3_COUNT Register (Offset = 13h) [Reset = X0h]

CNT3_COUNT is shown in Table 9-14.

Return to the Summary Table.

Table 9-14. CNT3_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT3_COUNT	R	Xh	

9.1.13 CNT4_COUNT_LSB Register (Offset = 14h) [Reset = X0h]

CNT4_COUNT_LSB is shown in Table 9-15.

Return to the Summary Table.

Table 9-15. CNT4_COUNT_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT4_COUNT_LSB	R	Xh	

9.1.14 CNT4_COUNT_MSB Register (Offset = 15h) [Reset = X0h]

CNT4_COUNT_MSB is shown in Table 9-16.

Return to the Summary Table.

Table 9-16. CNT4_COUNT_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT4_COUNT_MSB	R	Xh	

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9.1.15 CNT5_COUNT_LSB Register (Offset = 16h) [Reset = X0h]

CNT5_COUNT_LSB is shown in Table 9-17.

Return to the Summary Table.

Table 9-17. CNT5_COUNT_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT5_COUNT_LSB	R	Xh	

9.1.16 CNT5_COUNT_MSB Register (Offset = 17h) [Reset = X0h]

CNT5_COUNT_MSB is shown in Table 9-18.

Return to the Summary Table.

Table 9-18. CNT5_COUNT_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT5_COUNT_MSB	R	Xh	

9.1.17 CNT6_COUNT Register (Offset = 18h) [Reset = X0h]

CNT6_COUNT is shown in Table 9-19.

Return to the Summary Table.

Table 9-19. CNT6_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT6_COUNT	R	Xh	

9.1.18 CNT7_COUNT Register (Offset = 19h) [Reset = X0h]

CNT7_COUNT is shown in Table 9-20.

Return to the Summary Table.

Table 9-20. CNT7_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT7_COUNT	R	Xh	

9.1.19 CNT8_COUNT Register (Offset = 1Ah) [Reset = X0h]

CNT8_COUNT is shown in Table 9-21.

Return to the Summary Table.

Table 9-21. CNT8_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT8_COUNT	R	Xh	

9.1.20 CNT9_COUNT Register (Offset = 1Bh) [Reset = X0h]

CNT9_COUNT is shown in Table 9-22.

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Table 9-22. CNT9_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT9_COUNT	R	Xh	

9.1.21 CNT0_DATA Register (Offset = 20h) [Reset = X0h]

CNT0_DATA is shown in Table 9-23.

Return to the Summary Table.

Table 9-23. CNT0_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT0_DATA	R/W	Xh	

9.1.22 CNT1_DATA Register (Offset = 21h) [Reset = X0h]

CNT1_DATA is shown in Table 9-24.

Return to the Summary Table.

Table 9-24. CNT1_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT1_DATA	R/W	Xh	

9.1.23 CNT2_DATA Register (Offset = 22h) [Reset = X0h]

CNT2_DATA is shown in Table 9-25.

Return to the Summary Table.

Table 9-25. CNT2_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT2_DATA	R/W	Xh	

9.1.24 CNT3_DATA Register (Offset = 23h) [Reset = X0h]

CNT3_DATA is shown in Table 9-26.

Return to the Summary Table.

Table 9-26. CNT3_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT3_DATA	R/W	Xh	

9.1.25 CNT4_DATA_LSB Register (Offset = 24h) [Reset = X0h]

CNT4_DATA_LSB is shown in Table 9-27.

Return to the Summary Table.

Table 9-27. CNT4_DATA_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT4_DATA_LSB	R/W	Xh	

9.1.26 CNT4_DATA_MSB Register (Offset = 25h) [Reset = X0h]

CNT4_DATA_MSB is shown in Table 9-28.

Return to the Summary Table.

Table 9-28. CNT4_DATA_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT4_DATA_MSB	R/W	Xh	

9.1.27 CNT5_DATA_LSB Register (Offset = 26h) [Reset = X0h]

CNT5_DATA_LSB is shown in Table 9-29.

Return to the Summary Table.

Table 9-29. CNT5_DATA_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT5_DATA_LSB	R/W	Xh	

9.1.28 CNT5_DATA_MSB Register (Offset = 27h) [Reset = X0h]

CNT5_DATA_MSB is shown in Table 9-30.

Return to the Summary Table.

Table 9-30. CNT5_DATA_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT5_DATA_MSB	R/W	Xh	

9.1.29 CNT6_DATA Register (Offset = 28h) [Reset = X0h]

CNT6_DATA is shown in Table 9-31.

Return to the Summary Table.

Table 9-31. CNT6_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT6_DATA	R/W	Xh	

9.1.30 CNT7_DATA Register (Offset = 29h) [Reset = X0h]

CNT7_DATA is shown in Table 9-32.

Return to the Summary Table.

Table 9-32. CNT7_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT7_DATA	R/W	Xh	

9.1.31 CNT8_DATA Register (Offset = 2Ah) [Reset = X0h]

CNT8_DATA is shown in Table 9-33.

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Table 9-33. CNT8_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT8_DATA	R/W	Xh	

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9.1.32 CNT9_DATA Register (Offset = 2Bh) [Reset = X0h]

CNT9_DATA is shown in Table 9-34.

Return to the Summary Table.

Table 9-34. CNT9_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT9_DATA	R/W	Xh	

9.1.33 WDT_TIMEOUT_DATA Register (Offset = 30h) [Reset = X0h]

WDT_TIMEOUT_DATA is shown in Table 9-35.

Return to the Summary Table.

Table 9-35. WDT_TIMEOUT_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WATCHDOG_TIMEOUT_DATA	R/W	Xh	

9.1.34 WDT_OUTPUT_DATA Register (Offset = 31h) [Reset = X0h]

WDT_OUTPUT_DATA is shown in Table 9-36.

Return to the Summary Table.

Table 9-36. WDT_OUTPUT_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WATCHDOG_OUTPUT_DATA	R/W	Xh	

9.1.35 WDT_STATUS Register (Offset = 32h) [Reset = X0h]

WDT_STATUS is shown in Table 9-37.

Return to the Summary Table.

Table 9-37. WDT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	WDT_STATUS	R	Xh	Watchdog fault/timeout output

9.1.36 PGEN_DATA_LSB Register (Offset = 40h) [Reset = X0h]

PGEN_DATA_LSB is shown in Table 9-38.

Return to the Summary Table.

Table 9-38. PGEN_DATA_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_LSB	R/W	Xh	

9.1.37 PGEN_DATA_MSB Register (Offset = 41h) [Reset = X0h]

PGEN_DATA_MSB is shown in Table 9-39.

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Table 9-39. PGEN_DATA_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_MSB	R/W	Xh	

9.1.38 STATE_MACHINE Register (Offset = 50h) [Reset = X0h]

STATE_MACHINE is shown in Table 9-40.

Return to the Summary Table.

Table 9-40. STATE_MACHINE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0h	Reserved
2:0	CURRENT_STATE	R	Xh	

9.1.39 STATE0_OUT Register (Offset = 51h) [Reset = X0h]

STATE0_OUT is shown in Table 9-41.

Return to the Summary Table.

Table 9-41. STATE0_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE0_OUT	R/W	Xh	

9.1.40 STATE1_OUT Register (Offset = 52h) [Reset = X0h]

STATE1_OUT is shown in Table 9-42.

Return to the Summary Table.

Table 9-42. STATE1_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE1_OUT	R/W	Xh	

9.1.41 STATE2_OUT Register (Offset = 53h) [Reset = X0h]

STATE2_OUT is shown in Table 9-43.

Return to the Summary Table.

Table 9-43. STATE2_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE2_OUT	R/W	Xh	

9.1.42 STATE3_OUT Register (Offset = 54h) [Reset = X0h]

STATE3_OUT is shown in Table 9-44.

Return to the Summary Table.

Table 9-44. STATE3_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE3_OUT	R/W	Xh	

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9.1.43 STATE4_OUT Register (Offset = 55h) [Reset = X0h]

STATE4_OUT is shown in Table 9-45.

Return to the Summary Table.

Table 9-45. STATE4_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE4_OUT	R/W	Xh	

9.1.44 STATE5_OUT Register (Offset = 56h) [Reset = X0h]

STATE5_OUT is shown in Table 9-46.

Return to the Summary Table.

Table 9-46. STATE5_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE5_OUT	R/W	Xh	

9.1.45 STATE6_OUT Register (Offset = 57h) [Reset = X0h]

STATE6_OUT is shown in Table 9-47.

Return to the Summary Table.

Table 9-47. STATE6_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE6_OUT	R/W	Xh	

9.1.46 STATE7_OUT Register (Offset = 58h) [Reset = X0h]

STATE7_OUT is shown in Table 9-48.

Return to the Summary Table.

Table 9-48. STATE7_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE7_OUT	R/W	Xh	

9.1.47 VREF_ACMP0 Register (Offset = 70h) [Reset = X0h]

VREF_ACMP0 is shown in Table 9-49.

Return to the Summary Table.

Table 9-49. VREF_ACMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_ACMP0	R/W	Xh	

9.1.48 VREF_ACMP1 Register (Offset = 71h) [Reset = X0h]

VREF_ACMP1 is shown in Table 9-50.

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Table 9-50. VREF_ACMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_ACMP1	R/W	Xh	

9.1.49 VREF_ACMP2 Register (Offset = 72h) [Reset = X0h]

VREF_ACMP2 is shown in Table 9-51.

Return to the Summary Table.

Table 9-51. VREF_ACMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_ACMP2	R/W	Xh	

9.1.50 VREF_ACMP3 Register (Offset = 73h) [Reset = X0h]

VREF_ACMP3 is shown in Table 9-52.

Return to the Summary Table.

Table 9-52. VREF_ACMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_ACMP3	R/W	Xh	

9.1.51 VREF_McACMP0_0 Register (Offset = 74h) [Reset = X0h]

VREF_McACMP0_0 is shown in Table 9-53.

Return to the Summary Table.

Table 9-53. VREF_McACMP0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP0_0	R/W	Xh	

9.1.52 VREF_McACMP0_1 Register (Offset = 75h) [Reset = X0h]

VREF_McACMP0_1 is shown in Table 9-54.

Return to the Summary Table.

Table 9-54. VREF_McACMP0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP0_1	R/W	Xh	

9.1.53 VREF_McACMP1_0 Register (Offset = 76h) [Reset = X0h]

VREF_McACMP1_0 is shown in Table 9-55.

Return to the Summary Table.

Table 9-55. VREF_McACMP1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

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Table 9-55. VREF_McACMP1_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VREF_McACMP1_0	R/W	Xh	

9.1.54 VREF_McACMP1_1 Register (Offset = 77h) [Reset = X0h]

VREF_McACMP1_1 is shown in Table 9-56.

Return to the Summary Table.

Table 9-56. VREF_McACMP1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP1_1	R/W	Xh	

9.1.55 VREF_McACMP2_0 Register (Offset = 78h) [Reset = X0h]

VREF_McACMP2_0 is shown in Table 9-57.

Return to the Summary Table.

Table 9-57. VREF_McACMP2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP2_0	R/W	Xh	

9.1.56 VREF_McACMP2_1 Register (Offset = 79h) [Reset = X0h]

VREF_McACMP2_1 is shown in Table 9-58.

Return to the Summary Table.

Table 9-58. VREF_McACMP2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP2_1	R/W	Xh	

9.1.57 VREF_McACMP3_0 Register (Offset = 7Ah) [Reset = X0h]

VREF_McACMP3_0 is shown in Table 9-59.

Return to the Summary Table.

Table 9-59. VREF_McACMP3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP3_0	R/W	Xh	

9.1.58 VREF_McACMP3_1 Register (Offset = 7Bh) [Reset = X0h]

VREF_McACMP3_1 is shown in Table 9-60.

Return to the Summary Table.

Table 9-60. VREF_McACMP3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

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Table 9-60. VREF_McACMP3_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VREF_McACMP3_1	R/W	Xh	

9.1.59 VIRTUAL_INPUT Register (Offset = E0h) [Reset = X0h]

VIRTUAL_INPUT is shown in Table 9-61.

Return to the Summary Table.

Table 9-61. VIRTUAL_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VIRTUAL_IN	R/W	Xh	

9.1.60 VIRTUAL_OUTPUT Register (Offset = E1h) [Reset = X0h]

VIRTUAL_OUTPUT is shown in Table 9-62.

Return to the Summary Table.

Table 9-62. VIRTUAL_OUTPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VIRTUAL_OUT	R	Xh	

9.1.61 SER_COMM_CFG Register (Offset = FDh) [Reset = X0h]

SER_COMM_CFG is shown in Table 9-63.

Return to the Summary Table.

Table 9-63. SER_COMM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	ADDR_INC	R/W	Xh	Address auto-incrementing disable 0h = Enabled 1h = Disabled

9.1.62 CRC_STATUS Register (Offset = FEh) [Reset = X0h]

CRC_STATUS is shown in Table 9-64.

Return to the Summary Table.

Table 9-64. CRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	ERR_CNT	R	0h	
4:1	RESERVED	R	0h	Reserved
0	ERR_FLAG	R	Xh	

9.1.63 SER_COMM_WR_MASK Register (Offset = FFh) [Reset = X0h]

SER_COMM_WR_MASK is shown in Table 9-65.

Return to the Summary Table.

Table 9-65. SER_COMM_WR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SER_COMM_WR_MASK	R/W	Xh	

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9.2 TPLD2001_Cfg_0 Registers

Table 9-66 lists the memory-mapped registers for the TPLD2001_Cfg_0 registers. All register offset addresses not listed in Table 9-66 should be considered as reserved locations and the register contents should not be modified.

Table 9-66. TPLD2001_CFG_0 Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
200h	CMX_0	RESERVED	IO1_DOUT_CMX						
201h	CMX_1	RESERVED	IO1_OE_CMX						
202h	CMX_2	RESERVED	IO2_DOUT_CMX						
203h	CMX_3	RESERVED	IO2_OE_CMX						
204h	CMX_4	RESERVED	IO3_DOUT_CMX						
205h	CMX_5	RESERVED	IO3_OE_CMX						
206h	CMX_6	RESERVED	IO4_DOUT_CMX						
207h	CMX_7	RESERVED	IO5_DOUT_CMX						
208h	CMX_8	RESERVED	IO6_DOUT_CMX						
209h	CMX_9	RESERVED	IO7_DOUT_CMX						
20Ah	CMX_10	RESERVED	IO8_DOUT_CMX						
20Bh	CMX_11	RESERVED	IO9_DOUT_CMX						
20Ch	CMX_12	RESERVED	IO10_DOUT_CMX						
20Dh	CMX_13	RESERVED	IO10_OE_CMX						
20Eh	CMX_14	RESERVED	IO11_DOUT_CMX						
20Fh	CMX_15	RESERVED	IO11_OE_CMX						
210h	CMX_16	RESERVED	IO12_DOUT_CMX						
211h	CMX_17	RESERVED	IO12_OE_CMX						
212h	CMX_18	RESERVED	IO13_DOUT_CMX						
213h	CMX_19	RESERVED	IO13_OE_CMX						
214h	CMX_20	RESERVED	IO14_DOUT_CMX						
215h	CMX_21	RESERVED	IO15_DOUT_CMX						
216h	CMX_22	RESERVED	IO15_OE_CMX						
217h	CMX_23	RESERVED	IO16_DOUT_CMX						
218h	CMX_24	RESERVED	IO16_OE_CMX						
219h	CMX_25	RESERVED	IO17_DOUT_CMX						
21Ah	CMX_26	RESERVED	IO17_OE_CMX						
21Bh	CMX_27	RESERVED	LUT2_0_IN0_/_DFF_CLK_IN_CMX						
21Ch	CMX_28	RESERVED	LUT2_0_IN1_/_DFF_D_IN_CMX						
21Dh	CMX_29	RESERVED	LUT2_1_IN0_/_DFF_CLK_IN_CMX						
21Eh	CMX_30	RESERVED	LUT2_1_IN1_/_DFF_D_IN_CMX						
21Fh	CMX_31	RESERVED	LUT2_2_IN0_/_DFF_CLK_IN_CMX						
220h	CMX_32	RESERVED	LUT2_2_IN1_/_DFF_D_IN_CMX						
221h	CMX_33	RESERVED	LUT2_3_IN0_/_PGEN_CLK_IN_CMX						
222h	CMX_34	RESERVED	LUT2_3_IN1_/_PGEN_RST_IN_CMX						
223h	CMX_35	RESERVED	LUT3_0_IN0_/_DFF_CLK_IN_CMX						
224h	CMX_36	RESERVED	LUT3_0_IN1_/_DFF_D_IN_CMX						
225h	CMX_37	RESERVED	LUT3_0_IN2_/_DFF_RST_IN_CMX						
226h	CMX_38	RESERVED	LUT3_1_IN0_/_DFF_CLK_IN_CMX						
227h	CMX_39	RESERVED	LUT3_1_IN1_/_DFF_D_IN_CMX						
228h	CMX_40	RESERVED	LUT3_1_IN2_/_DFF_RST_IN_CMX						
229h	CMX_41	RESERVED	LUT3_2_IN0_/_DFF/SR_CLK_IN_CMX						
22Ah	CMX_42	RESERVED	LUT3_2_IN1_/_DFF/SR_D_IN_CMX						
22Bh	CMX_43	RESERVED	LUT3_2_IN2_/_DFF/SR_RST_IN_CMX						
22Ch	CMX_44	RESERVED	LUT3_3_IN0_/_DFF/SR_CLK_IN_CMX						
22Dh	CMX_45	RESERVED	LUT3_3_IN1_/_DFF/SR_D_IN_CMX						
22Eh	CMX_46	RESERVED	LUT3_3_IN2_/_DFF/SR_RST_IN_CMX						
22Fh	CMX_47	RESERVED	LUT3_4_IN0_/_DFF/SR_CLK_IN_CMX						
230h	CMX_48	RESERVED	LUT3_4_IN1_/_DFF/SR_D_IN_CMX						

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Table 9-66. TPLD2001_CFG_0 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
231h	CMX_49	RESERVED	LUT3_4_IN2_/_DFF/SR_RST_IN_CMX						
232h	CMX_50	RESERVED	LUT3_5_IN0_/_DFF/SR_CLK_IN_CMX						
233h	CMX_51	RESERVED	LUT3_5_IN1_/_DFF/SR_D_IN_CMX						
234h	CMX_52	RESERVED	LUT3_5_IN2_/_DFF/SR_RST_IN_CMX						
235h	CMX_53	RESERVED	LUT3_6_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX						
236h	CMX_54	RESERVED	LUT3_6_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX						
237h	CMX_55	RESERVED	LUT3_6_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX						
238h	CMX_56	RESERVED	LUT3_7_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX						
239h	CMX_57	RESERVED	LUT3_7_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX						
23Ah	CMX_58	RESERVED	LUT3_7_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX						
23Bh	CMX_59	RESERVED	LUT3_8_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX						
23Ch	CMX_60	RESERVED	LUT3_8_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX						
23Dh	CMX_61	RESERVED	LUT3_8_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX						
23Eh	CMX_62	RESERVED	LUT3_9_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX						
23Fh	CMX_63	RESERVED	LUT3_9_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX						
240h	CMX_64	RESERVED	LUT3_9_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX						
241h	CMX_65	RESERVED	LUT3_10_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX						
242h	CMX_66	RESERVED	LUT3_10_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX						
243h	CMX_67	RESERVED	LUT3_10_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX						
244h	CMX_68	RESERVED	LUT3_11_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX						
245h	CMX_69	RESERVED	LUT3_11_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX						
246h	CMX_70	RESERVED	LUT3_11_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX						
247h	CMX_71	RESERVED	LUT4_0_IN0_/_DFF_CLK_IN_CMX						
248h	CMX_72	RESERVED	LUT4_0_IN1_/_DFF_D_IN_CMX						
249h	CMX_73	RESERVED	LUT4_0_IN2_/_DFF_RST_IN_CMX						
24Ah	CMX_74	RESERVED	LUT4_0_IN3__CMX						
24Bh	CMX_75	RESERVED	LUT4_1_IN0_/_DFF_CLK_IN_CMX						
24Ch	CMX_76	RESERVED	LUT4_1_IN1_/_DFF_D_IN_CMX						
24Dh	CMX_77	RESERVED	LUT4_1_IN2_/_DFF_RST_IN_CMX						
24Eh	CMX_78	RESERVED	LUT4_1_IN3__CMX						
24Fh	CMX_79	RESERVED	LUT4_2_IN0_/_DFF_CLK_IN__CMX						
250h	CMX_80	RESERVED	LUT4_2_IN1_/_DFF_D_IN_CMX						
251h	CMX_81	RESERVED	LUT4_2_IN2_/_DFF_RST_IN_CMX						
252h	CMX_82	RESERVED	LUT4_2_IN3__CMX						
253h	CMX_83	RESERVED	LUT4_3_IN0_/_DFF_CLK_IN__CMX						
254h	CMX_84	RESERVED	LUT4_3_IN1_/_DFF_D_IN_CMX						
255h	CMX_85	RESERVED	LUT4_3_IN2_/_DFF_RST_IN_CMX						
256h	CMX_86	RESERVED	LUT4_3_IN3__CMX						
257h	CMX_87	RESERVED	PFLT0_IN_CMX						
258h	CMX_88	RESERVED	PFLT1_IN_CMX						
259h	CMX_89	RESERVED	FILT_IN_CMX						
25Ah	CMX_90	RESERVED	SM_ST0_EN0_CMX						
25Bh	CMX_91	RESERVED	SM_ST0_EN1_CMX						
25Ch	CMX_92	RESERVED	SM_ST0_EN2_CMX						
25Dh	CMX_93	RESERVED	SM_ST1_EN0_CMX						
25Eh	CMX_94	RESERVED	SM_ST1_EN1_CMX						
25Fh	CMX_95	RESERVED	SM_ST1_EN2_CMX						
260h	CMX_96	RESERVED	SM_ST2_EN0_CMX						
261h	CMX_97	RESERVED	SM_ST2_EN1_CMX						
262h	CMX_98	RESERVED	SM_ST2_EN2_CMX						
263h	CMX_99	RESERVED	SM_ST3_EN0_CMX						
264h	CMX_100	RESERVED	SM_ST3_EN1_CMX						
265h	CMX_101	RESERVED	SM_ST3_EN2_CMX						
266h	CMX_102	RESERVED	SM_ST4_EN0_CMX						
267h	CMX_103	RESERVED	SM_ST4_EN1_CMX						

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Table 9-66. TPLD2001_CFG_0 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
268h	CMX_104	RESERVED	SM_ST4_EN2_CMX						
269h	CMX_105	RESERVED	SM_ST5_EN0_CMX						
26Ah	CMX_106	RESERVED	SM_ST5_EN1_CMX						
26Bh	CMX_107	RESERVED	SM_ST5_EN2_CMX						
26Ch	CMX_108	RESERVED	SM_ST6_EN0_CMX						
26Dh	CMX_109	RESERVED	SM_ST6_EN1_CMX						
26Eh	CMX_110	RESERVED	SM_ST6_EN2_CMX						
26Fh	CMX_111	RESERVED	SM_ST7_EN0_CMX						
270h	CMX_112	RESERVED	SM_ST7_EN1_CMX						
271h	CMX_113	RESERVED	SM_ST7_EN2_CMX						
272h	CMX_114	RESERVED	SM_CLK_IN_CMX						
273h	CMX_115	RESERVED	SM_RST_IN_CMX						
274h	CMX_116	RESERVED	ACMP0_PWR_UP_CMX						
275h	CMX_117	RESERVED	ACMP1_PWR_UP_CMX						
276h	CMX_118	RESERVED	ACMP2_PWR_UP_CMX						
277h	CMX_119	RESERVED	ACMP3_PWR_UP_CMX						
278h	CMX_120	RESERVED	McACMP_ENABLE_CMX						
279h	CMX_121	RESERVED	McACMP_RST_CMX						
27Ah	CMX_122	RESERVED	OSC0_PWR_DOWN_CMX						
27Bh	CMX_123	RESERVED	OSC1_PWR_DOWN_CMX						
27Ch	CMX_124	RESERVED	OSC2_PWR_DOWN_CMX						
27Dh	CMX_125	RESERVED	CNT6_FSM0_IN_CMX						
27Eh	CMX_126	RESERVED	CNT6_FSM0_UP_CMX						
27Fh	CMX_127	RESERVED	CNT6_FSM0_KEEP_CMX						
280h	CMX_128	RESERVED	CNT6_FSM0_CLK_IN_CMX						
281h	CMX_129	RESERVED	CNT7_FSM1_IN_CMX						
282h	CMX_130	RESERVED	CNT7_FSM1_UP_CMX						
283h	CMX_131	RESERVED	CNT7_FSM1_KEEP_CMX						
284h	CMX_132	RESERVED	CNT7_FSM1_CLK_IN_CMX						
285h	CMX_133	RESERVED	CNT8_FSM2_IN_CMX						
286h	CMX_134	RESERVED	CNT8_FSM2_UP_CMX						
287h	CMX_135	RESERVED	CNT8_FSM2_KEEP_CMX						
288h	CMX_136	RESERVED	CNT8_FSM2_CLK_IN_CMX						
289h	CMX_137	RESERVED	CNT9_FSM3_IN_CMX						
28Ah	CMX_138	RESERVED	CNT9_FSM3_UP_CMX						
28Bh	CMX_139	RESERVED	CNT9_FSM3_KEEP_CMX						
28Ch	CMX_140	RESERVED	CNT9_FSM3_CLK_IN_CMX						
28Dh	CMX_141	RESERVED	PWM_GEN0_PWR_UP_CMX						
28Eh	CMX_142	RESERVED	PWM_GEN1_PWR_UP_CMX						
28Fh	CMX_143	RESERVED	PWM_GEN2_PWR_UP_CMX						
290h	CMX_144	RESERVED	PWM_GEN3_PWR_UP_CMX						
291h	CMX_145	RESERVED	WDT_EN_CMX						
292h	CMX_146	RESERVED	WDT_IN_CMX						
293h	CMX_147	RESERVED	VIRTUAL_OUT0_CMX						
294h	CMX_148	RESERVED	VIRTUAL_OUT1_CMX						
295h	CMX_149	RESERVED	VIRTUAL_OUT2_CMX						
296h	CMX_150	RESERVED	VIRTUAL_OUT3_CMX						
297h	CMX_151	RESERVED	VIRTUAL_OUT4_CMX						
298h	CMX_152	RESERVED	VIRTUAL_OUT5_CMX						
299h	CMX_153	RESERVED	VIRTUAL_OUT6_CMX						
29Ah	CMX_154	RESERVED	VIRTUAL_OUT7_CMX						
29Bh	CMX_155	RESERVED	AMUX0_SEL_CMX						
29Ch	CMX_156	RESERVED	AMUX1_SEL_CMX						

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Complex bit access types are encoded to fit into small table cells. Table 9-67 shows the codes that are used for access types in this section.

Table 9-67. TPLD2001_Cfg_0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.2.1 CMX_0 Register (Offset = 200h) [Reset = X0h]

CMX_0 is shown in Table 9-68.

Return to the Summary Table.

IO1 DOUT connection mux routing select

Table 9-68. CMX_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

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Table 9-68. CMX_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	IO1_DOUT_CMX	R/W	Xh	0h = GND 1h = IN0 DIN 2h = IO1 / VIO_0 DIN 3h = IO2 / VIO_1 DIN 4h = IO3 / VIO_2 DIN 5h = IO4 / VIO_3 DIN 6h = IO5 / VIO_4 DIN 7h = IO6 / VIO_5 DIN 8h = IO7 / VIO_6 DIN 9h = IO8 Ah = IO9 DIN / VIO_7 DIN Bh = IO10 DIN Ch = IO11 DIN Dh = IO12 DIN Eh = IO13 DIN Fh = IO14 DIN 10h = IO15 DIN 11h = IO16 DIN 12h = IO17 DIN 13h = LUT2_0 OUT 14h = LUT2_1 OUT 15h = LUT2_2 OUT 16h = LUT2_3 OUT 17h = LUT3_0 OUT 18h = LUT3_1 OUT 19h = LUT3_2 OUT 1Ah = LUT3_3 OUT 1Bh = LUT3_4 OUT 1Ch = LUT3_5 OUT 1Dh = LUT3_6 / LDC OUT 1Eh = LUT3_7 / LDC OUT 1Fh = LUT3_8 / LDC OUT 20h = LUT3_9 / LDC OUT 21h = LUT3_10 / LDC OUT 22h = LUT3_11 / LDC OUT 23h = LUT4_0 OUT 24h = LUT4_1 OUT 25h = LUT4_2 OUT 26h = LUT4_3 OUT 27h = PFLT0 OUT 28h = PFLT1 OUT 29h = FLT / EDET OUT 2Ah = SM OUT0 2Bh = SM OUT1 2Ch = SM OUT2 2Dh = SM OUT3 2Eh = SM OUT4 2Fh = SM OUT5 30h = SM OUT6 31h = SM OUT7 32h = ACMP0 OUT 33h = ACMP1 OUT 34h = ACMP2 OUT 35h = ACMP3 OUT 36h = McACMP CH0_0 OUT 37h = McACMP CH0_1 OUT 38h = McACMP CH1_0 OUT 39h = McACMP CH1_1 OUT 3Ah = McACMP CH2_0 OUT 3Bh = McACMP CH2_1 OUT 3Ch = McACMP CH3_0 OUT 3Dh = McACMP CH3_1 OUT 3Eh = McACMP DATA RDY 3Fh = OSC0 OUT0 40h = OSC0 OUT1 41h = OSC1 OUT0 42h = OSC1 OUT1 43h = OSC2 OUT 44h = CNT6 OUT 45h = CNT7 OUT 46h = CNT8 OUT 47h = CNT9 OUT 48h = PWM GEN0 OUTN 49h = PWM GEN0 OUTP 4Ah = PWM GEN1 OUTN 4Bh = PWM GEN1 OUTP 4Ch = PWM GEN2 OUTN 4Dh = PWM GEN2 OUTP 4Eh = PWM GEN3 OUTN 4Fh = PWM GEN3 OUTP 50h = WDT OUT 51h = POR OUT 52h = Reserved 53h = Reserved 54h = Reserved 55h = Reserved 56h = Reserved 57h = Reserved

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Table 9-68. CMX_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				58h = Reserved 59h = Reserved 5Ah = Reserved 5Bh = Reserved 5Ch = Reserved 5Dh = Reserved 5Eh = Reserved 5Fh = Reserved 60h = Reserved 61h = Reserved 62h = Reserved 63h = Reserved 64h = Reserved 65h = Reserved 66h = Reserved 67h = Reserved 68h = Reserved 69h = Reserved 6Ah = Reserved 6Bh = Reserved 6Ch = Reserved 6Dh = Reserved 6Eh = Reserved 6Fh = Reserved 70h = Reserved 71h = Reserved 72h = Reserved 73h = Reserved 74h = Reserved 75h = Reserved 76h = Reserved 77h = Reserved 78h = Reserved 79h = Reserved 7Ah = Reserved 7Bh = Reserved 7Ch = Reserved 7Dh = Reserved 7Eh = Reserved 7Fh = VCC

9.2.2 CMX_1 Register (Offset = 201h) [Reset = X0h]

CMX_1 is shown in Table 9-69.

Return to the Summary Table.

IO1 OE connection mux routing select

Table 9-69. CMX_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO1_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.3 CMX_2 Register (Offset = 202h) [Reset = X0h]

CMX_2 is shown in Table 9-70.

Return to the Summary Table.

IO2 DOUT connection mux routing select

Table 9-70. CMX_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO2_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.4 CMX_3 Register (Offset = 203h) [Reset = X0h]

CMX_3 is shown in Table 9-71.

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Return to the Summary Table.

IO2 OE connection mux routing select

Table 9-71. CMX_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO2_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.5 CMX_4 Register (Offset = 204h) [Reset = X0h]

CMX_4 is shown in Table 9-72.

Return to the Summary Table.

IO3 DOUT connection mux routing select

Table 9-72. CMX_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO3_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.6 CMX_5 Register (Offset = 205h) [Reset = X0h]

CMX_5 is shown in Table 9-73.

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IO3 OE connection mux routing select

Table 9-73. CMX_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO3_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.7 CMX_6 Register (Offset = 206h) [Reset = X0h]

CMX_6 is shown in Table 9-74.

Return to the Summary Table.

IO4 DOUT connection mux routing select

Table 9-74. CMX_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO4_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.8 CMX_7 Register (Offset = 207h) [Reset = X0h]

CMX_7 is shown in Table 9-75.

Return to the Summary Table.

IO5 DOUT connection mux routing select

Table 9-75. CMX_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

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Table 9-75. CMX_7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	IO5_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.9 CMX_8 Register (Offset = 208h) [Reset = X0h]

CMX_8 is shown in Table 9-76.

Return to the Summary Table.

IO6 DOUT connection mux routing select

Table 9-76. CMX_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO6_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.10 CMX_9 Register (Offset = 209h) [Reset = X0h]

CMX_9 is shown in Table 9-77.

Return to the Summary Table.

IO7 DOUT connection mux routing select

Table 9-77. CMX_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO7_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.11 CMX_10 Register (Offset = 20Ah) [Reset = X0h]

CMX_10 is shown in Table 9-78.

Return to the Summary Table.

IO8 DOUT connection mux routing select

Table 9-78. CMX_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO8_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.12 CMX_11 Register (Offset = 20Bh) [Reset = X0h]

CMX_11 is shown in Table 9-79.

Return to the Summary Table.

IO9 DOUT connection mux routing select

Table 9-79. CMX_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO9_DOUT_CMX	R/W	Xh	Same options as CMX_0

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9.2.13 CMX_12 Register (Offset = 20Ch) [Reset = X0h]

CMX_12 is shown in Table 9-80.

Return to the Summary Table.

IO10 DOUT connection mux routing select

Table 9-80. CMX_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO10_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.14 CMX_13 Register (Offset = 20Dh) [Reset = X0h]

CMX_13 is shown in Table 9-81.

Return to the Summary Table.

IO10 OE connection mux routing select

Table 9-81. CMX_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO10_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.15 CMX_14 Register (Offset = 20Eh) [Reset = X0h]

CMX_14 is shown in Table 9-82.

Return to the Summary Table.

IO11 DOUT connection mux routing select

Table 9-82. CMX_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO11_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.16 CMX_15 Register (Offset = 20Fh) [Reset = X0h]

CMX_15 is shown in Table 9-83.

Return to the Summary Table.

IO11 OE connection mux routing select

Table 9-83. CMX_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO11_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.17 CMX_16 Register (Offset = 210h) [Reset = X0h]

CMX_16 is shown in Table 9-84.

Return to the Summary Table.

IO12 DOUT connection mux routing select

Table 9-84. CMX_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO12_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.18 CMX_17 Register (Offset = 211h) [Reset = X0h]

CMX_17 is shown in Table 9-85.

Return to the Summary Table.

IO12 OE connection mux routing select

Table 9-85. CMX_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO12_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.19 CMX_18 Register (Offset = 212h) [Reset = X0h]

CMX_18 is shown in Table 9-86.

Return to the Summary Table.

IO13 DOUT connection mux routing select

Table 9-86. CMX_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO13_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.20 CMX_19 Register (Offset = 213h) [Reset = X0h]

CMX_19 is shown in Table 9-87.

Return to the Summary Table.

IO13 OE connection mux routing select

Table 9-87. CMX_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO13_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.21 CMX_20 Register (Offset = 214h) [Reset = X0h]

CMX_20 is shown in Table 9-88.

Return to the Summary Table.

IO14 DOUT connection mux routing select

Table 9-88. CMX_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO14_DOUT_CMX	R/W	Xh	Same options as CMX_0

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9.2.22 CMX_21 Register (Offset = 215h) [Reset = X0h]

CMX_21 is shown in Table 9-89.

Return to the Summary Table.

IO15 DOUT connection mux routing select

Table 9-89. CMX_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO15_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.23 CMX_22 Register (Offset = 216h) [Reset = X0h]

CMX_22 is shown in Table 9-90.

Return to the Summary Table.

IO15 OE connection mux routing select

Table 9-90. CMX_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO15_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.24 CMX_23 Register (Offset = 217h) [Reset = X0h]

CMX_23 is shown in Table 9-91.

Return to the Summary Table.

IO16 DOUT connection mux routing select

Table 9-91. CMX_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO16_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.25 CMX_24 Register (Offset = 218h) [Reset = X0h]

CMX_24 is shown in Table 9-92.

Return to the Summary Table.

IO16 OE connection mux routing select

Table 9-92. CMX_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO16_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.26 CMX_25 Register (Offset = 219h) [Reset = X0h]

CMX_25 is shown in Table 9-93.

Return to the Summary Table.

IO17 DOUT connection mux routing select

Table 9-93. CMX_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO17_DOUT_CMX	R/W	Xh	Same options as CMX_0

9.2.27 CMX_26 Register (Offset = 21Ah) [Reset = X0h]

CMX_26 is shown in Table 9-94.

Return to the Summary Table.

IO17 OE connection mux routing select

Table 9-94. CMX_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	IO17_OE_CMX	R/W	Xh	Same options as CMX_0

9.2.28 CMX_27 Register (Offset = 21Bh) [Reset = X0h]

CMX_27 is shown in Table 9-95.

Return to the Summary Table.

LUT2_0 IN0 / DFF CLK IN connection mux routing select

Table 9-95. CMX_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_0_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.29 CMX_28 Register (Offset = 21Ch) [Reset = X0h]

CMX_28 is shown in Table 9-96.

Return to the Summary Table.

LUT2_0 IN1 / DFF D IN connection mux routing select

Table 9-96. CMX_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_0_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.30 CMX_29 Register (Offset = 21Dh) [Reset = X0h]

CMX_29 is shown in Table 9-97.

Return to the Summary Table.

LUT2_1 IN0 / DFF CLK IN connection mux routing select

Table 9-97. CMX_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_1_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

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9.2.31 CMX_30 Register (Offset = 21Eh) [Reset = X0h]

CMX_30 is shown in Table 9-98.

Return to the Summary Table.

LUT2_1 IN1 / DFF D IN connection mux routing select

Table 9-98. CMX_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_1_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.32 CMX_31 Register (Offset = 21Fh) [Reset = X0h]

CMX_31 is shown in Table 9-99.

Return to the Summary Table.

LUT2_2 IN0 / DFF CLK IN connection mux routing select

Table 9-99. CMX_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_2_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.33 CMX_32 Register (Offset = 220h) [Reset = X0h]

CMX_32 is shown in Table 9-100.

Return to the Summary Table.

LUT2_2 IN1 / DFF D IN connection mux routing select

Table 9-100. CMX_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_2_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.34 CMX_33 Register (Offset = 221h) [Reset = X0h]

CMX_33 is shown in Table 9-101.

Return to the Summary Table.

LUT2_3 IN0 / PGEN CLK IN connection mux routing select

Table 9-101. CMX_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_3_IN0_/ _PGEN_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.35 CMX_34 Register (Offset = 222h) [Reset = X0h]

CMX_34 is shown in Table 9-102.

Return to the Summary Table.

LUT2_3 IN1 / PGEN RST IN connection mux routing select

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Table 9-102. CMX_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT2_3_IN1_/ _PGEN_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.36 CMX_35 Register (Offset = 223h) [Reset = X0h]

CMX_35 is shown in Table 9-103.

Return to the Summary Table.

LUT3_0 IN0 / DFF CLK IN connection mux routing select

Table 9-103. CMX_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_0_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.37 CMX_36 Register (Offset = 224h) [Reset = X0h]

CMX_36 is shown in Table 9-104.

Return to the Summary Table.

LUT3_0 IN1 / DFF D IN connection mux routing select

Table 9-104. CMX_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_0_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.38 CMX_37 Register (Offset = 225h) [Reset = X0h]

CMX_37 is shown in Table 9-105.

Return to the Summary Table.

LUT3_0 IN2 / DFF RST IN connection mux routing select

Table 9-105. CMX_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_0_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.39 CMX_38 Register (Offset = 226h) [Reset = X0h]

CMX_38 is shown in Table 9-106.

Return to the Summary Table.

LUT3_1 IN0 / DFF CLK IN connection mux routing select

Table 9-106. CMX_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_1_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

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9.2.40 CMX_39 Register (Offset = 227h) [Reset = X0h]

CMX_39 is shown in Table 9-107.

Return to the Summary Table.

LUT3_1 IN1 / DFF D IN connection mux routing select

Table 9-107. CMX_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_1_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.41 CMX_40 Register (Offset = 228h) [Reset = X0h]

CMX_40 is shown in Table 9-108.

Return to the Summary Table.

LUT3_1 IN2 / DFF RST IN connection mux routing select

Table 9-108. CMX_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_1_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.42 CMX_41 Register (Offset = 229h) [Reset = X0h]

CMX_41 is shown in Table 9-109.

Return to the Summary Table.

LUT3_2 IN0 / DFF/SR CLK IN connection mux routing select

Table 9-109. CMX_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_2_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.43 CMX_42 Register (Offset = 22Ah) [Reset = X0h]

CMX_42 is shown in Table 9-110.

Return to the Summary Table.

LUT3_2 IN1 / DFF/SR D IN connection mux routing select

Table 9-110. CMX_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_2_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.44 CMX_43 Register (Offset = 22Bh) [Reset = X0h]

CMX_43 is shown in Table 9-111.

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LUT3_2 IN2 / DFF/SR RST IN connection mux routing select

Table 9-111. CMX_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_2_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.45 CMX_44 Register (Offset = 22Ch) [Reset = X0h]

CMX_44 is shown in Table 9-112.

Return to the Summary Table.

LUT3_3 IN0 / DFF/SR CLK IN connection mux routing select

Table 9-112. CMX_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_3_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.46 CMX_45 Register (Offset = 22Dh) [Reset = X0h]

CMX_45 is shown in Table 9-113.

Return to the Summary Table.

LUT3_3 IN1 / DFF/SR D IN connection mux routing select

Table 9-113. CMX_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_3_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.47 CMX_46 Register (Offset = 22Eh) [Reset = X0h]

CMX_46 is shown in Table 9-114.

Return to the Summary Table.

LUT3_3 IN2 / DFF/SR RST IN connection mux routing select

Table 9-114. CMX_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_3_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.48 CMX_47 Register (Offset = 22Fh) [Reset = X0h]

CMX_47 is shown in Table 9-115.

Return to the Summary Table.

LUT3_4 IN0 / DFF/SR CLK IN connection mux routing select

Table 9-115. CMX_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_4_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

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9.2.49 CMX_48 Register (Offset = 230h) [Reset = X0h]

CMX_48 is shown in Table 9-116.

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LUT3_4 IN1 / DFF/SR D IN connection mux routing select

Table 9-116. CMX_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_4_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.50 CMX_49 Register (Offset = 231h) [Reset = X0h]

CMX_49 is shown in Table 9-117.

Return to the Summary Table.

LUT3_4 IN2 / DFF/SR RST IN connection mux routing select

Table 9-117. CMX_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_4_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.51 CMX_50 Register (Offset = 232h) [Reset = X0h]

CMX_50 is shown in Table 9-118.

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LUT3_5 IN0 / DFF/SR CLK IN connection mux routing select

Table 9-118. CMX_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_5_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.52 CMX_51 Register (Offset = 233h) [Reset = X0h]

CMX_51 is shown in Table 9-119.

Return to the Summary Table.

LUT3_5 IN1 / DFF/SR D IN connection mux routing select

Table 9-119. CMX_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_5_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.53 CMX_52 Register (Offset = 234h) [Reset = X0h]

CMX_52 is shown in Table 9-120.

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LUT3_5 IN2 / DFF/SR RST IN connection mux routing select

Table 9-120. CMX_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_5_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.54 CMX_53 Register (Offset = 235h) [Reset = X0h]

CMX_53 is shown in Table 9-121.

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LUT3_6 IN0 / DFF CLK IN OR LDC IN0 connection mux routing select

Table 9-121. CMX_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_6_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

9.2.55 CMX_54 Register (Offset = 236h) [Reset = X0h]

CMX_54 is shown in Table 9-122.

Return to the Summary Table.

LUT3_6 IN1 / DFF D IN OR LDC IN1 connection mux routing select

Table 9-122. CMX_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_6_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

9.2.56 CMX_55 Register (Offset = 237h) [Reset = X0h]

CMX_55 is shown in Table 9-123.

Return to the Summary Table.

LUT3_6 IN2 / DFF RST IN OR LDC IN2 connection mux routing select

Table 9-123. CMX_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_6_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

9.2.57 CMX_56 Register (Offset = 238h) [Reset = X0h]

CMX_56 is shown in Table 9-124.

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LUT3_7 IN0 / DFF CLK IN OR LDC IN0 connection mux routing select

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Table 9-124. CMX_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_7_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

9.2.58 CMX_57 Register (Offset = 239h) [Reset = X0h]

CMX_57 is shown in Table 9-125.

Return to the Summary Table.

LUT3_7 IN1 / DFF D IN OR LDC IN1 connection mux routing select

Table 9-125. CMX_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_7_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

9.2.59 CMX_58 Register (Offset = 23Ah) [Reset = X0h]

CMX_58 is shown in Table 9-126.

Return to the Summary Table.

LUT3_7 IN2 / DFF RST IN OR LDC IN2 connection mux routing select

Table 9-126. CMX_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_7_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

9.2.60 CMX_59 Register (Offset = 23Bh) [Reset = X0h]

CMX_59 is shown in Table 9-127.

Return to the Summary Table.

LUT3_8 IN0 / DFF CLK IN OR LDC IN0 connection mux routing select

Table 9-127. CMX_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_8_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

9.2.61 CMX_60 Register (Offset = 23Ch) [Reset = X0h]

CMX_60 is shown in Table 9-128.

Return to the Summary Table.

LUT3_8 IN1 / DFF D IN OR LDC IN1 connection mux routing select

Table 9-128. CMX_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

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Table 9-128. CMX_60 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	LUT3_8_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

9.2.62 CMX_61 Register (Offset = 23Dh) [Reset = X0h]

CMX_61 is shown in Table 9-129.

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LUT3_8 IN2 / DFF RST IN OR LDC IN2 connection mux routing select

Table 9-129. CMX_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_8_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

9.2.63 CMX_62 Register (Offset = 23Eh) [Reset = X0h]

CMX_62 is shown in Table 9-130.

Return to the Summary Table.

LUT3_9 IN0 / DFF CLK IN OR LDC IN0 connection mux routing select

Table 9-130. CMX_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_9_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

9.2.64 CMX_63 Register (Offset = 23Fh) [Reset = X0h]

CMX_63 is shown in Table 9-131.

Return to the Summary Table.

LUT3_9 IN1 / DFF D IN OR LDC IN1 connection mux routing select

Table 9-131. CMX_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_9_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

9.2.65 CMX_64 Register (Offset = 240h) [Reset = X0h]

CMX_64 is shown in Table 9-132.

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LUT3_9 IN2 / DFF RST IN OR LDC IN2 connection mux routing select

Table 9-132. CMX_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

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Table 9-132. CMX_64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	LUT3_9_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

9.2.66 CMX_65 Register (Offset = 241h) [Reset = X0h]

CMX_65 is shown in Table 9-133.

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LUT3_10 IN0 / DFF CLK IN OR LDC IN0 connection mux routing select

Table 9-133. CMX_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_10_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

9.2.67 CMX_66 Register (Offset = 242h) [Reset = X0h]

CMX_66 is shown in Table 9-134.

Return to the Summary Table.

LUT3_10 IN1 / DFF D IN OR LDC IN1 connection mux routing select

Table 9-134. CMX_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_10_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

9.2.68 CMX_67 Register (Offset = 243h) [Reset = X0h]

CMX_67 is shown in Table 9-135.

Return to the Summary Table.

LUT3_10 IN2 / DFF RST IN OR LDC IN2 connection mux routing select

Table 9-135. CMX_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_10_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

9.2.69 CMX_68 Register (Offset = 244h) [Reset = X0h]

CMX_68 is shown in Table 9-136.

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LUT3_11 IN0 / DFF CLK IN OR LDC IN0 connection mux routing select

Table 9-136. CMX_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

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Table 9-136. CMX_68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	LUT3_11_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

9.2.70 CMX_69 Register (Offset = 245h) [Reset = X0h]

CMX_69 is shown in Table 9-137.

Return to the Summary Table.

LUT3_11 IN1 / DFF D IN OR LDC IN1 connection mux routing select

Table 9-137. CMX_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_11_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

9.2.71 CMX_70 Register (Offset = 246h) [Reset = X0h]

CMX_70 is shown in Table 9-138.

Return to the Summary Table.

LUT3_11 IN2 / DFF RST IN OR LDC IN2 connection mux routing select

Table 9-138. CMX_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT3_11_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

9.2.72 CMX_71 Register (Offset = 247h) [Reset = X0h]

CMX_71 is shown in Table 9-139.

Return to the Summary Table.

LUT4_0 IN0 / DFF CLK IN connection mux routing select

Table 9-139. CMX_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_0_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.73 CMX_72 Register (Offset = 248h) [Reset = X0h]

CMX_72 is shown in Table 9-140.

Return to the Summary Table.

LUT4_0 IN1 / DFF D IN connection mux routing select

Table 9-140. CMX_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_0_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

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9.2.74 CMX_73 Register (Offset = 249h) [Reset = X0h]

CMX_73 is shown in Table 9-141.

Return to the Summary Table.

LUT4_0 IN2 / DFF RST IN connection mux routing select

Table 9-141. CMX_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_0_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.75 CMX_74 Register (Offset = 24Ah) [Reset = X0h]

CMX_74 is shown in Table 9-142.

Return to the Summary Table.

LUT4_0 IN3 connection mux routing select

Table 9-142. CMX_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_0_IN3__CMX	R/W	Xh	Same options as CMX_0

9.2.76 CMX_75 Register (Offset = 24Bh) [Reset = X0h]

CMX_75 is shown in Table 9-143.

Return to the Summary Table.

LUT4_1 IN0 / DFF CLK IN connection mux routing select

Table 9-143. CMX_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_1_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.77 CMX_76 Register (Offset = 24Ch) [Reset = X0h]

CMX_76 is shown in Table 9-144.

Return to the Summary Table.

LUT4_1 IN1 / DFF D IN connection mux routing select

Table 9-144. CMX_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_1_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.78 CMX_77 Register (Offset = 24Dh) [Reset = X0h]

CMX_77 is shown in Table 9-145.

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LUT4_1 IN2 / DFF RST IN connection mux routing select

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Table 9-145. CMX_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_1_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.79 CMX_78 Register (Offset = 24Eh) [Reset = X0h]

CMX_78 is shown in Table 9-146.

Return to the Summary Table.

LUT4_1 IN3 connection mux routing select

Table 9-146. CMX_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_1_IN3__CMX	R/W	Xh	Same options as CMX_0

9.2.80 CMX_79 Register (Offset = 24Fh) [Reset = X0h]

CMX_79 is shown in Table 9-147.

Return to the Summary Table.

LUT4_2 IN0 / DFF CLK IN connection mux routing select

Table 9-147. CMX_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_2_IN0_/ _DFF_CLK_IN__CMX	R/W	Xh	Same options as CMX_0

9.2.81 CMX_80 Register (Offset = 250h) [Reset = X0h]

CMX_80 is shown in Table 9-148.

Return to the Summary Table.

LUT4_2 IN1 / DFF D IN connection mux routing select

Table 9-148. CMX_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_2_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.82 CMX_81 Register (Offset = 251h) [Reset = X0h]

CMX_81 is shown in Table 9-149.

Return to the Summary Table.

LUT4_2 IN2 / DFF RST IN connection mux routing select

Table 9-149. CMX_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_2_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

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9.2.83 CMX_82 Register (Offset = 252h) [Reset = X0h]

CMX_82 is shown in Table 9-150.

Return to the Summary Table.

LUT4_2 IN3 connection mux routing select

Table 9-150. CMX_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_2_IN3__CMX	R/W	Xh	Same options as CMX_0

9.2.84 CMX_83 Register (Offset = 253h) [Reset = X0h]

CMX_83 is shown in Table 9-151.

Return to the Summary Table.

LUT4_3 IN0 / DFF CLK IN connection mux routing select

Table 9-151. CMX_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_3_IN0_/ _DFF_CLK_IN__CMX	R/W	Xh	Same options as CMX_0

9.2.85 CMX_84 Register (Offset = 254h) [Reset = X0h]

CMX_84 is shown in Table 9-152.

Return to the Summary Table.

LUT4_3 IN1 / DFF D IN connection mux routing select

Table 9-152. CMX_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_3_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.86 CMX_85 Register (Offset = 255h) [Reset = X0h]

CMX_85 is shown in Table 9-153.

Return to the Summary Table.

LUT4_3 IN2 / DFF RST IN connection mux routing select

Table 9-153. CMX_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_3_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.87 CMX_86 Register (Offset = 256h) [Reset = X0h]

CMX_86 is shown in Table 9-154.

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LUT4_3 IN3 connection mux routing select

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Table 9-154. CMX_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LUT4_3_IN3__CMX	R/W	Xh	Same options as CMX_0

9.2.88 CMX_87 Register (Offset = 257h) [Reset = X0h]

CMX_87 is shown in Table 9-155.

Return to the Summary Table.

PFLT0 IN connection mux routing select

Table 9-155. CMX_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	PFLT0_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.89 CMX_88 Register (Offset = 258h) [Reset = X0h]

CMX_88 is shown in Table 9-156.

Return to the Summary Table.

PFLT1 IN connection mux routing select

Table 9-156. CMX_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	PFLT1_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.90 CMX_89 Register (Offset = 259h) [Reset = X0h]

CMX_89 is shown in Table 9-157.

Return to the Summary Table.

FLT/EDET IN connection mux routing select

Table 9-157. CMX_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	FILT_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.91 CMX_90 Register (Offset = 25Ah) [Reset = X0h]

CMX_90 is shown in Table 9-158.

Return to the Summary Table.

SM ST0 EN0 connection mux routing select

Table 9-158. CMX_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST0_EN0_CMX	R/W	Xh	Same options as CMX_0

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9.2.92 CMX_91 Register (Offset = 25Bh) [Reset = X0h]

CMX_91 is shown in Table 9-159.

Return to the Summary Table.

SM ST0 EN1 connection mux routing select

Table 9-159. CMX_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST0_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.93 CMX_92 Register (Offset = 25Ch) [Reset = X0h]

CMX_92 is shown in Table 9-160.

Return to the Summary Table.

SM ST0 EN2 connection mux routing select

Table 9-160. CMX_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST0_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.94 CMX_93 Register (Offset = 25Dh) [Reset = X0h]

CMX_93 is shown in Table 9-161.

Return to the Summary Table.

SM ST1 EN0 connection mux routing select

Table 9-161. CMX_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST1_EN0_CMX	R/W	Xh	Same options as CMX_0

9.2.95 CMX_94 Register (Offset = 25Eh) [Reset = X0h]

CMX_94 is shown in Table 9-162.

Return to the Summary Table.

SM ST1 EN1 connection mux routing select

Table 9-162. CMX_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST1_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.96 CMX_95 Register (Offset = 25Fh) [Reset = X0h]

CMX_95 is shown in Table 9-163.

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SM ST1 EN2 connection mux routing select

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Table 9-163. CMX_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST1_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.97 CMX_96 Register (Offset = 260h) [Reset = X0h]

CMX_96 is shown in Table 9-164.

Return to the Summary Table.

SM ST2 EN0 connection mux routing select

Table 9-164. CMX_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST2_EN0_CMX	R/W	Xh	Same options as CMX_0

9.2.98 CMX_97 Register (Offset = 261h) [Reset = X0h]

CMX_97 is shown in Table 9-165.

Return to the Summary Table.

SM ST2 EN1 connection mux routing select

Table 9-165. CMX_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST2_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.99 CMX_98 Register (Offset = 262h) [Reset = X0h]

CMX_98 is shown in Table 9-166.

Return to the Summary Table.

SM ST2 EN2 connection mux routing select

Table 9-166. CMX_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST2_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.100 CMX_99 Register (Offset = 263h) [Reset = X0h]

CMX_99 is shown in Table 9-167.

Return to the Summary Table.

SM ST3 EN0 connection mux routing select

Table 9-167. CMX_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST3_EN0_CMX	R/W	Xh	Same options as CMX_0

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9.2.101 CMX_100 Register (Offset = 264h) [Reset = X0h]

CMX_100 is shown in Table 9-168.

Return to the Summary Table.

SM ST3 EN1 connection mux routing select

Table 9-168. CMX_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST3_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.102 CMX_101 Register (Offset = 265h) [Reset = X0h]

CMX_101 is shown in Table 9-169.

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SM ST3 EN2 connection mux routing select

Table 9-169. CMX_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST3_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.103 CMX_102 Register (Offset = 266h) [Reset = X0h]

CMX_102 is shown in Table 9-170.

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SM ST4 EN0 connection mux routing select

Table 9-170. CMX_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST4_EN0_CMX	R/W	Xh	Same options as CMX_0

9.2.104 CMX_103 Register (Offset = 267h) [Reset = X0h]

CMX_103 is shown in Table 9-171.

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SM ST4 EN1 connection mux routing select

Table 9-171. CMX_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST4_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.105 CMX_104 Register (Offset = 268h) [Reset = X0h]

CMX_104 is shown in Table 9-172.

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SM ST4 EN2 connection mux routing select

Table 9-172. CMX_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST4_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.106 CMX_105 Register (Offset = 269h) [Reset = X0h]

CMX_105 is shown in Table 9-173.

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SM ST5 EN0 connection mux routing select

Table 9-173. CMX_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST5_EN0_CMX	R/W	Xh	Same options as CMX_0

9.2.107 CMX_106 Register (Offset = 26Ah) [Reset = X0h]

CMX_106 is shown in Table 9-174.

Return to the Summary Table.

SM ST5 EN1 connection mux routing select

Table 9-174. CMX_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST5_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.108 CMX_107 Register (Offset = 26Bh) [Reset = X0h]

CMX_107 is shown in Table 9-175.

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SM ST5 EN2 connection mux routing select

Table 9-175. CMX_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST5_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.109 CMX_108 Register (Offset = 26Ch) [Reset = X0h]

CMX_108 is shown in Table 9-176.

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SM ST6 EN0 connection mux routing select

Table 9-176. CMX_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST6_EN0_CMX	R/W	Xh	Same options as CMX_0

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9.2.110 CMX_109 Register (Offset = 26Dh) [Reset = X0h]

CMX_109 is shown in Table 9-177.

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SM ST6 EN1 connection mux routing select

Table 9-177. CMX_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST6_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.111 CMX_110 Register (Offset = 26Eh) [Reset = X0h]

CMX_110 is shown in Table 9-178.

Return to the Summary Table.

SM ST6 EN2 connection mux routing select

Table 9-178. CMX_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST6_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.112 CMX_111 Register (Offset = 26Fh) [Reset = X0h]

CMX_111 is shown in Table 9-179.

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SM ST7 EN0 connection mux routing select

Table 9-179. CMX_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST7_EN0_CMX	R/W	Xh	Same options as CMX_0

9.2.113 CMX_112 Register (Offset = 270h) [Reset = X0h]

CMX_112 is shown in Table 9-180.

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SM ST7 EN1 connection mux routing select

Table 9-180. CMX_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST7_EN1_CMX	R/W	Xh	Same options as CMX_0

9.2.114 CMX_113 Register (Offset = 271h) [Reset = X0h]

CMX_113 is shown in Table 9-181.

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SM ST7 EN2 connection mux routing select

Table 9-181. CMX_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_ST7_EN2_CMX	R/W	Xh	Same options as CMX_0

9.2.115 CMX_114 Register (Offset = 272h) [Reset = X0h]

CMX_114 is shown in Table 9-182.

Return to the Summary Table.

SM CLK IN connection mux routing select

Table 9-182. CMX_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.116 CMX_115 Register (Offset = 273h) [Reset = X0h]

CMX_115 is shown in Table 9-183.

Return to the Summary Table.

SM RST IN connection mux routing select

Table 9-183. CMX_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	SM_RST_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.117 CMX_116 Register (Offset = 274h) [Reset = X0h]

CMX_116 is shown in Table 9-184.

Return to the Summary Table.

ACMP0 PWR UP connection mux routing select

Table 9-184. CMX_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	ACMP0_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.118 CMX_117 Register (Offset = 275h) [Reset = X0h]

CMX_117 is shown in Table 9-185.

Return to the Summary Table.

ACMP1 PWR UP connection mux routing select

Table 9-185. CMX_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	ACMP1_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

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9.2.119 CMX_118 Register (Offset = 276h) [Reset = X0h]

CMX_118 is shown in Table 9-186.

Return to the Summary Table.

ACMP2 PWR UP connection mux routing select

Table 9-186. CMX_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	ACMP2_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.120 CMX_119 Register (Offset = 277h) [Reset = X0h]

CMX_119 is shown in Table 9-187.

Return to the Summary Table.

ACMP3 PWR UP connection mux routing select

Table 9-187. CMX_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	ACMP3_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.121 CMX_120 Register (Offset = 278h) [Reset = X0h]

CMX_120 is shown in Table 9-188.

Return to the Summary Table.

McACMP ENABLE connection mux routing select

Table 9-188. CMX_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	McACMP_ENABLE_CMX	R/W	Xh	Same options as CMX_0

9.2.122 CMX_121 Register (Offset = 279h) [Reset = X0h]

CMX_121 is shown in Table 9-189.

Return to the Summary Table.

McACMP RST connection mux routing select

Table 9-189. CMX_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	McACMP_RST_CMX	R/W	Xh	Same options as CMX_0

9.2.123 CMX_122 Register (Offset = 27Ah) [Reset = X0h]

CMX_122 is shown in Table 9-190.

Return to the Summary Table.

OSC0 PWR DOWN connection mux routing select

Table 9-190. CMX_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	OSC0_PWR_DOWN_CMX	R/W	Xh	Same options as CMX_0

9.2.124 CMX_123 Register (Offset = 27Bh) [Reset = X0h]

CMX_123 is shown in Table 9-191.

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OSC1 PWR DOWN connection mux routing select

Table 9-191. CMX_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	OSC1_PWR_DOWN_CMX	R/W	Xh	Same options as CMX_0

9.2.125 CMX_124 Register (Offset = 27Ch) [Reset = X0h]

CMX_124 is shown in Table 9-192.

Return to the Summary Table.

OSC2 PWR DOWN connection mux routing select

Table 9-192. CMX_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	OSC2_PWR_DOWN_CMX	R/W	Xh	Same options as CMX_0

9.2.126 CMX_125 Register (Offset = 27Dh) [Reset = X0h]

CMX_125 is shown in Table 9-193.

Return to the Summary Table.

CNT6/FSM IN connection mux routing select

Table 9-193. CMX_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT6_FSM0_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.127 CMX_126 Register (Offset = 27Eh) [Reset = X0h]

CMX_126 is shown in Table 9-194.

Return to the Summary Table.

CNT6/FSM UP connection mux routing select

Table 9-194. CMX_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT6_FSM0_UP_CMX	R/W	Xh	Same options as CMX_0

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9.2.128 CMX_127 Register (Offset = 27Fh) [Reset = X0h]

CMX_127 is shown in Table 9-195.

Return to the Summary Table.

CNT6/FSM KEEP connection mux routing select

Table 9-195. CMX_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT6_FSM0_KEEP_CMX	R/W	Xh	Same options as CMX_0

9.2.129 CMX_128 Register (Offset = 280h) [Reset = X0h]

CMX_128 is shown in Table 9-196.

Return to the Summary Table.

CNT6/FSM CLK IN connection mux routing select

Table 9-196. CMX_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT6_FSM0_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.130 CMX_129 Register (Offset = 281h) [Reset = X0h]

CMX_129 is shown in Table 9-197.

Return to the Summary Table.

CNT7/FSM IN connection mux routing select

Table 9-197. CMX_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT7_FSM1_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.131 CMX_130 Register (Offset = 282h) [Reset = X0h]

CMX_130 is shown in Table 9-198.

Return to the Summary Table.

CNT7/FSM UP connection mux routing select

Table 9-198. CMX_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT7_FSM1_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.132 CMX_131 Register (Offset = 283h) [Reset = X0h]

CMX_131 is shown in Table 9-199.

Return to the Summary Table.

CNT7/FSM KEEP connection mux routing select

Table 9-199. CMX_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT7_FSM1_KEEP_CMX	R/W	Xh	Same options as CMX_0

9.2.133 CMX_132 Register (Offset = 284h) [Reset = X0h]

CMX_132 is shown in Table 9-200.

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CNT7/FSM CLK IN connection mux routing select

Table 9-200. CMX_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT7_FSM1_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.134 CMX_133 Register (Offset = 285h) [Reset = X0h]

CMX_133 is shown in Table 9-201.

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CNT8/FSM IN connection mux routing select

Table 9-201. CMX_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT8_FSM2_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.135 CMX_134 Register (Offset = 286h) [Reset = X0h]

CMX_134 is shown in Table 9-202.

Return to the Summary Table.

CNT8/FSM UP connection mux routing select

Table 9-202. CMX_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT8_FSM2_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.136 CMX_135 Register (Offset = 287h) [Reset = X0h]

CMX_135 is shown in Table 9-203.

Return to the Summary Table.

CNT8/FSM KEEP connection mux routing select

Table 9-203. CMX_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT8_FSM2_KEEP_CMX	R/W	Xh	Same options as CMX_0

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9.2.137 CMX_136 Register (Offset = 288h) [Reset = X0h]

CMX_136 is shown in Table 9-204.

Return to the Summary Table.

CNT8/FSM CLK IN connection mux routing select

Table 9-204. CMX_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT8_FSM2_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.138 CMX_137 Register (Offset = 289h) [Reset = X0h]

CMX_137 is shown in Table 9-205.

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CNT9/FSM IN connection mux routing select

Table 9-205. CMX_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT9_FSM3_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.139 CMX_138 Register (Offset = 28Ah) [Reset = X0h]

CMX_138 is shown in Table 9-206.

Return to the Summary Table.

CNT9/FSM UP connection mux routing select

Table 9-206. CMX_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT9_FSM3_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.140 CMX_139 Register (Offset = 28Bh) [Reset = X0h]

CMX_139 is shown in Table 9-207.

Return to the Summary Table.

CNT9/FSM KEEP connection mux routing select

Table 9-207. CMX_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT9_FSM3_KEEP_CMX	R/W	Xh	Same options as CMX_0

9.2.141 CMX_140 Register (Offset = 28Ch) [Reset = X0h]

CMX_140 is shown in Table 9-208.

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CNT9/FSM CLK IN connection mux routing select

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Table 9-208. CMX_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	CNT9_FSM3_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.142 CMX_141 Register (Offset = 28Dh) [Reset = X0h]

CMX_141 is shown in Table 9-209.

Return to the Summary Table.

PWM GEN0 PWR UP connection mux routing select

Table 9-209. CMX_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	PWM_GEN0_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.143 CMX_142 Register (Offset = 28Eh) [Reset = X0h]

CMX_142 is shown in Table 9-210.

Return to the Summary Table.

PWM GEN1 PWR UP connection mux routing select

Table 9-210. CMX_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	PWM_GEN1_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.144 CMX_143 Register (Offset = 28Fh) [Reset = X0h]

CMX_143 is shown in Table 9-211.

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PWM GEN2 PWR UP connection mux routing select

Table 9-211. CMX_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	PWM_GEN2_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

9.2.145 CMX_144 Register (Offset = 290h) [Reset = X0h]

CMX_144 is shown in Table 9-212.

Return to the Summary Table.

PWM GEN3 PWR UP connection mux routing select

Table 9-212. CMX_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	PWM_GEN3_PWR_UP_CMX	R/W	Xh	Same options as CMX_0

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9.2.146 CMX_145 Register (Offset = 291h) [Reset = X0h]

CMX_145 is shown in Table 9-213.

Return to the Summary Table.

WDT EN connection mux routing select

Table 9-213. CMX_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	WDT_EN_CMX	R/W	Xh	Same options as CMX_0

9.2.147 CMX_146 Register (Offset = 292h) [Reset = X0h]

CMX_146 is shown in Table 9-214.

Return to the Summary Table.

WDT IN connection mux routing select

Table 9-214. CMX_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	WDT_IN_CMX	R/W	Xh	Same options as CMX_0

9.2.148 CMX_147 Register (Offset = 293h) [Reset = X0h]

CMX_147 is shown in Table 9-215.

Return to the Summary Table.

VIRTUAL OUT0 connection mux routing select

Table 9-215. CMX_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT0_CMX	R/W	Xh	Same options as CMX_0

9.2.149 CMX_148 Register (Offset = 294h) [Reset = X0h]

CMX_148 is shown in Table 9-216.

Return to the Summary Table.

VIRTUAL OUT1 connection mux routing select

Table 9-216. CMX_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT1_CMX	R/W	Xh	Same options as CMX_0

9.2.150 CMX_149 Register (Offset = 295h) [Reset = X0h]

CMX_149 is shown in Table 9-217.

Return to the Summary Table.

VIRTUAL OUT2 connection mux routing select

Table 9-217. CMX_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT2_CMX	R/W	Xh	Same options as CMX_0

9.2.151 CMX_150 Register (Offset = 296h) [Reset = X0h]

CMX_150 is shown in Table 9-218.

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VIRTUAL OUT3 connection mux routing select

Table 9-218. CMX_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT3_CMX	R/W	Xh	Same options as CMX_0

9.2.152 CMX_151 Register (Offset = 297h) [Reset = X0h]

CMX_151 is shown in Table 9-219.

Return to the Summary Table.

VIRTUAL OUT4 connection mux routing select

Table 9-219. CMX_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT4_CMX	R/W	Xh	Same options as CMX_0

9.2.153 CMX_152 Register (Offset = 298h) [Reset = X0h]

CMX_152 is shown in Table 9-220.

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VIRTUAL OUT5 connection mux routing select

Table 9-220. CMX_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT5_CMX	R/W	Xh	Same options as CMX_0

9.2.154 CMX_153 Register (Offset = 299h) [Reset = X0h]

CMX_153 is shown in Table 9-221.

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VIRTUAL OUT6 connection mux routing select

Table 9-221. CMX_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT6_CMX	R/W	Xh	Same options as CMX_0

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9.2.155 CMX_154 Register (Offset = 29Ah) [Reset = X0h]

CMX_154 is shown in Table 9-222.

Return to the Summary Table.

VIRTUAL OUT7 connection mux routing select

Table 9-222. CMX_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	VIRTUAL_OUT7_CMX	R/W	Xh	Same options as CMX_0

9.2.156 CMX_155 Register (Offset = 29Bh) [Reset = X0h]

CMX_155 is shown in Table 9-223.

Return to the Summary Table.

AMUX0_SEL connection mux routing select

Table 9-223. CMX_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	AMUX0_SEL_CMX	R/W	Xh	Same options as CMX_0

9.2.157 CMX_156 Register (Offset = 29Ch) [Reset = X0h]

CMX_156 is shown in Table 9-224.

Return to the Summary Table.

AMUX1_SEL connection mux routing select

Table 9-224. CMX_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	AMUX1_SEL_CMX	R/W	Xh	Same options as CMX_0

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9.3 TPLD2001_Cfg_1 Registers

Table 9-225 lists the memory-mapped registers for the TPLD2001_Cfg_1 registers. All register offset addresses not listed in Table 9-225 should be considered as reserved locations and the register contents should not be modified.

Table 9-225. TPLD2001_CFG_1 Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
300h	IN0_CFG	RESERVED	PULL_UP_EN	RES_SEL		RESERVED		IN_CTRL	
301h	IO1_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
302h	IO2_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
303h	IO3_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
304h	IO4_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
305h	IO5_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
306h	IO6_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
307h	IO7_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
308h	IO8_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
309h	IO9_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
30Ah	IO10_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
30Bh	IO11_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
30Ch	IO12_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
30Dh	IO13_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
30Eh	IO14_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
30Fh	IO15_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
310h	IO16_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
311h	IO17_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
320h	VIO_SEL_0	V_IN7	V_IN6	V_IN5	V_IN4	V_IN3	V_IN2	V_IN1	V_IN0
324h	LUT_FS_0	RESERVED				LUT2_3_FS	LUT2_2_FS	LUT2_1_FS	LUT2_0_FS
325h	LUT_FS_1	RESERVED		LUT3_5_FS	LUT3_4_FS	LUT3_3_FS	LUT3_2_FS	LUT3_1_FS	LUT3_0_FS
327h	LUT_FS_3	RESERVED				LUT4_3_FS	LUT4_2_FS	LUT4_1_FS	LUT4_0_FS
328h	LUT2_0_CFG	RESERVED				BIT3	BIT2	BIT1	BIT0
329h	LUT2_1_CFG	RESERVED				BIT3	BIT2	BIT1	BIT0
32Ah	LUT2_2_CFG	RESERVED				BIT3	BIT2	BIT1	BIT0
32Eh	LUT2_3_CFG0	RESERVED		PGEN_RST	RESERVED	BITS3_0			
32Fh	LUT2_3_CFG1	PGEN_DATA_LSB							
330h	LUT2_3_CFG2	PGEN_DATA_MSB							
334h	LUT3_0_CFG	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
335h	LUT3_1_CFG	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
336h	LUT3_2_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
337h	LUT3_2_CFG1	BITS15_8							
338h	LUT3_3_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
339h	LUT3_3_CFG1	BITS15_8							
33Ah	LUT3_4_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
33Bh	LUT3_4_CFG1	BITS15_8							
33Ch	LUT3_5_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
33Dh	LUT3_5_CFG1	BITS15_8							
344h	LUT4_0_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
345h	LUT4_0_CFG1	BITS15_8							
346h	LUT4_1_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
347h	LUT4_1_CFG1	BITS15_8							
348h	LUT4_2_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
349h	LUT4_2_CFG1	BITS15_8							
34Ah	LUT4_3_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
34Bh	LUT4_3_CFG1	BITS15_8							
354h	LUT3_6_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
355h	LUT3_6_CFG1	CNT_DATA							
356h	LUT3_6_CFG2	CLK_SEL				MODE_SEL			

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Table 9-225. TPLD2001_CFG_1 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
357h	LUT3_6_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
358h	LUT3_6_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
359h	LUT3_7_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
35Ah	LUT3_7_CFG1	CNT_DATA							
35Bh	LUT3_7_CFG2	CLK_SEL				MODE_SEL			
35Ch	LUT3_7_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
35Dh	LUT3_7_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
35Eh	LUT3_8_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
35Fh	LUT3_8_CFG1	CNT_DATA							
360h	LUT3_8_CFG2	CLK_SEL				MODE_SEL			
361h	LUT3_8_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
362h	LUT3_8_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
363h	LUT3_9_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
364h	LUT3_9_CFG1	CNT_DATA							
365h	LUT3_9_CFG2	CLK_SEL				MODE_SEL			
366h	LUT3_9_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
367h	LUT3_9_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
372h	LUT3_10_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
373h	LUT3_10_CFG1	CNT_DATA_7:0							
374h	LUT3_10_CFG2	CNT_DATA_15:8							
375h	LUT3_10_CFG3	CLK_SEL				MODE_SEL			
376h	LUT3_10_CFG4	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
377h	LUT3_10_CFG5	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
378h	LUT3_11_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
379h	LUT3_11_CFG1	CNT_DATA_7:0							
37Ah	LUT3_11_CFG2	CNT_DATA_15:8							
37Bh	LUT3_11_CFG3	CLK_SEL				MODE_SEL			
37Ch	LUT3_11_CFG4	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
37Dh	LUT3_11_CFG5	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
37Eh	CNT6_FSM0_CFG0	CNT_DATA							
37Fh	CNT6_FSM0_CFG1	CLK_SEL				MODE_SEL			
380h	CNT6_FSM0_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
381h	CNT7_FSM1_CFG0	CNT_DATA							
382h	CNT7_FSM1_CFG1	CLK_SEL				MODE_SEL			
383h	CNT7_FSM1_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
384h	CNT8_FSM2_CFG0	CNT_DATA							
385h	CNT8_FSM2_CFG1	CLK_SEL				MODE_SEL			
386h	CNT8_FSM2_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
387h	CNT9_FSM3_CFG0	CNT_DATA							
388h	CNT9_FSM3_CFG1	CLK_SEL				MODE_SEL			
389h	CNT9_FSM3_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
38Ah	PWM_GEN0_CFG	RESERVED				TDB_SEL		OUTP_POL	OUTN_POL
38Bh	PWM_GEN1_CFG	RESERVED				TDB_SEL		OUTP_POL	OUTN_POL
38Ch	PWM_GEN2_CFG	RESERVED				TDB_SEL		OUTP_POL	OUTN_POL
38Dh	PWM_GEN3_CFG	RESERVED				TDB_SEL		OUTP_POL	OUTN_POL
38Eh	PWM_SRC_CFG	PWM_GEN3_DATA_SEL		PWM_GEN2_DATA_SEL		PWM_GEN1_DATA_SEL		PWM_GEN0_DATA_SEL	
38Fh	SM_CFG0	RESERVED	SM_S1_IN0			RESERVED	SM_S0_IN0		
390h	SM_CFG1	RESERVED	SM_S1_IN1			RESERVED	SM_S0_IN1		
391h	SM_CFG2	RESERVED	SM_S1_IN2			RESERVED	SM_S0_IN2		
392h	SM_CFG3	RESERVED	SM_S3_IN0			RESERVED	SM_S2_IN0		
393h	SM_CFG4	RESERVED	SM_S3_IN1			RESERVED	SM_S2_IN1		
394h	SM_CFG5	RESERVED	SM_S3_IN2			RESERVED	SM_S2_IN2		
395h	SM_CFG6	RESERVED	SM_S5_IN0			RESERVED	SM_S4_IN0		
396h	SM_CFG7	RESERVED	SM_S5_IN1			RESERVED	SM_S4_IN1		
397h	SM_CFG8	RESERVED	SM_S5_IN2			RESERVED	SM_S4_IN2		

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Table 9-225. TPLD2001_CFG_1 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
398h	SM_CFG9	RESERVED	SM_S7_IN0			RESERVED	SM_S6_IN0		
399h	SM_CFG10	RESERVED	SM_S7_IN1			RESERVED	SM_S6_IN1		
39Ah	SM_CFG11	SM_SYNC_EN	SM_S7_IN2			RESERVED	SM_S6_IN2		
3A7h	SM_CFG12	SM_CLK_SEL				SM_MODE	SM_INIT_STATE		
3A8h	SM_CFG13	S0_OUT_CFG							
3A9h	SM_CFG14	S1_OUT_CFG							
3AAh	SM_CFG15	S2_OUT_CFG							
3ABh	SM_CFG16	S3_OUT_CFG							
3ACh	SM_CFG17	S4_OUT_CFG							
3ADh	SM_CFG18	S5_OUT_CFG							
3AEh	SM_CFG19	S6_OUT_CFG							
3AFh	SM_CFG20	S7_OUT_CFG							
3B8h	WDT_CFG0	WDT_TIMEOUT_DATA							
3B9h	WDT_CFG1	WDT_OUT_DATA							
3BAh	WDT_CFG2	WDT_CLK_SEL				RESERVED		WDT_100X_EN	WDT_EN_SEL
3BBh	PFLT0_CFG	RESERVED		PFLT_DLY_SEL		PFLT_POL	RESERVED	PFLT_EDGE_SEL	
3BCh	PFLT1_CFG	RESERVED		PFLT_DLY_SEL		PFLT_POL	RESERVED	PFLT_EDGE_SEL	
3BDh	FILT_CFG	RESERVED				FLT_POL	OTP_SPARE	FLT_EDGE_SEL	
3BEh	OSC0_CFG0	RESERVED	CTRL_SRC	CTRL_SEL	SRC_SEL	PDIV		RESERVED	PWR_MODE
3BFh	OSC0_CFG1	OUT1_EN	OUT1_DIV			OUT0_EN	OUT0_DIV		
3C0h	OSC1_CFG0	RESERVED	CTRL_SRC	CTRL_SEL	SRC_SEL	PDIV		RESERVED	PWR_MODE
3C1h	OSC1_CFG1	OUT1_EN	OUT1_DIV			OUT0_EN	OUT0_DIV		
3C2h	OSC2_CFG0	SU_DLY	CTRL_SRC	CTRL_SEL	SRC_SEL	PDIV		RESERVED	PWR_MODE
3C3h	OSC2_CFG1	RESERVED				OUT_EN	OUT_DIV		
3C6h	ACMP0_CFG0	BW_SEL		INP_SEL		GAIN_SEL		HYS_SEL	
3C7h	ACMP0_CFG1	RESERVED		VREF_SEL					
3C8h	ACMP1_CFG0	BW_SEL		INP_SEL		GAIN_SEL		HYS_SEL	
3C9h	ACMP1_CFG1	RESERVED		VREF_SEL					
3CAh	ACMP2_CFG0	BW_SEL		INP_SEL		GAIN_SEL		HYS_SEL	
3CBh	ACMP2_CFG1	RESERVED		VREF_SEL					
3CCh	ACMP3_CFG0	BW_SEL		INP_SEL		GAIN_SEL		HYS_SEL	
3CDh	ACMP3_CFG1	RESERVED		VREF_SEL					
3CFh	MCACMP_CFG0	TS_INP_EN	VCC_INP_EN	SYNC_EN	MCS_MODE	CH_EN		RESERVED	MCS_EN
3D0h	MCACMP_CFG1	BW_SEL		RESERVED			EDGE_SEL	MCS_CLK_SEL	
3D1h	MCACMP_CH0_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3D2h	MCACMP_CH0_CFG1	CH_VREF_SEL		VREF_SEL					
3D3h	MCACMP_CH0_CFG2	RESERVED		VREF_SEL1					
3D6h	MCACMP_CH1_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3D7h	MCACMP_CH1_CFG1	CH_VREF_SEL		VREF_SEL					
3D8h	MCACMP_CH1_CFG2	RESERVED		VREF_SEL1					
3DBh	MCACMP_CH2_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3DCh	MCACMP_CH2_CFG1	CH_VREF_SEL		VREF_SEL					
3DDh	MCACMP_CH2_CFG2	RESERVED		VREF_SEL1					
3E0h	MCACMP_CH3_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3E1h	MCACMP_CH3_CFG1	CH_VREF_SEL		VREF_SEL					
3E2h	MCACMP_CH3_CFG2	RESERVED		VREF_SEL1					
3E5h	AMUX0_CFG	RESERVED							AMUX_EN
3E6h	AMUX1_CFG	RESERVED							AMUX_EN
3F2h	SER_COMM_CFG0	I2C_ADDR_SRC_SEL				I2C_IO_LAT	I2C_RST_EN	I2C_EN	SPI_EN
3F3h	SER_COMM_CFG1	I2C_ADDR_MSB				I2C_ADDR_LSB			RESERVED
3F7h	MISC_CFG0	GPIO_QC	CFG_RD_LCK	CFG_WR_LCK	OTP_WR_LCK	USER_LCK		RESERVED	
3FAh	DEVICE_ID4	DEVICE_ID4							
3FBh	DEVICE_ID5	DEVICE_ID5							
3FCh	DEVICE_ID6	DEVICE_ID6							
3FDh	DEVICE_ID7	DEVICE_ID7							

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Table 9-225. TPLD2001_CFG_1 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FEh	CRC_LSB	CRC_LSB							
3FFh	CRC_MSB	CRC_MSB							

Complex bit access types are encoded to fit into small table cells. Table 9-226 shows the codes that are used for access types in this section.

Table 9-226. TPLD2001_Cfg_1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.3.1 IN0_CFG Register (Offset = 300h) [Reset = XXh]

IN0_CFG is shown in Table 9-227.

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GPI configuration

Table 9-227. IN0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	RESERVED	R	0h	Reserved
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

9.3.2 IO1_CFG Register (Offset = 301h) [Reset = XXh]

IO1_CFG is shown in Table 9-228.

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GPIO1 configuration

Table 9-228. IO1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X

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Table 9-228. IO1_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.3 IO2_CFG Register (Offset = 302h) [Reset = XXh]

IO2_CFG is shown in Table 9-229.

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GPIO2 configuration

Table 9-229. IO2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.4 IO3_CFG Register (Offset = 303h) [Reset = XXh]

IO3_CFG is shown in Table 9-230.

Return to the Summary Table.

GPIO3 configuration

Table 9-230. IO3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.5 IO4_CFG Register (Offset = 304h) [Reset = X0h]

IO4_CFG is shown in Table 9-231.

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GPIO4 configuration

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Table 9-231. IO4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.6 IO5_CFG Register (Offset = 305h) [Reset = X0h]

IO5_CFG is shown in Table 9-232.

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GPIO5 configuration

Table 9-232. IO5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

9.3.7 IO6_CFG Register (Offset = 306h) [Reset = X0h]

IO6_CFG is shown in Table 9-233.

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GPIO6 configuration

Table 9-233. IO6_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 4X

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Table 9-233. IO6_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

9.3.8 IO7_CFG Register (Offset = 307h) [Reset = X0h]

IO7_CFG is shown in Table 9-234.

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GPIO7 configuration

Table 9-234. IO7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 4X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

9.3.9 IO8_CFG Register (Offset = 308h) [Reset = X0h]

IO8_CFG is shown in Table 9-235.

Return to the Summary Table.

GPIO8 configuration

Table 9-235. IO8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

9.3.10 IO9_CFG Register (Offset = 309h) [Reset = X0h]

IO9_CFG is shown in Table 9-236.

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GPIO9 configuration

Table 9-236. IO9_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.11 IO10_CFG Register (Offset = 30Ah) [Reset = XXh]

IO10_CFG is shown in Table 9-237.

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GPIO10 Configuration

Table 9-237. IO10_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.12 IO11_CFG Register (Offset = 30Bh) [Reset = XXh]

IO11_CFG is shown in Table 9-238.

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GPIO11 Configuration

Table 9-238. IO11_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X

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Table 9-238. IO11_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.13 IO12_CFG Register (Offset = 30Ch) [Reset = XXh]

IO12_CFG is shown in Table 9-239.

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GPIO12 Configuration

Table 9-239. IO12_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.14 IO13_CFG Register (Offset = 30Dh) [Reset = XXh]

IO13_CFG is shown in Table 9-240.

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GPIO13 Configuration

Table 9-240. IO13_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.15 IO14_CFG Register (Offset = 30Eh) [Reset = X0h]

IO14_CFG is shown in Table 9-241.

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GPIO14 Configuration

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Table 9-241. IO14_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.16 IO15_CFG Register (Offset = 30Fh) [Reset = XXh]

IO15_CFG is shown in Table 9-242.

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GPIO15 Configuration

Table 9-242. IO15_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.17 IO16_CFG Register (Offset = 310h) [Reset = XXh]

IO16_CFG is shown in Table 9-243.

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GPIO16 Configuration

Table 9-243. IO16_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X

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Table 9-243. IO16_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.18 IO17_CFG Register (Offset = 311h) [Reset = XXh]

IO17_CFG is shown in Table 9-244.

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GPIO17 Configuration

Table 9-244. IO17_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

9.3.19 VIO_SEL_0 Register (Offset = 320h) [Reset = X0h]

VIO_SEL_0 is shown in Table 9-245.

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IO8 to IO1 virtual IO select

Table 9-245. VIO_SEL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V_IN7	R/W	0h	0h = IO9 1h = V_IN7
6	V_IN6	R/W	0h	0h = IO7 1h = V_IN6
5	V_IN5	R/W	0h	0h = IO6 1h = V_IN5
4	V_IN4	R/W	0h	0h = IO5 1h = V_IN4
3	V_IN3	R/W	Xh	0h = IO4 1h = V_IN3
2	V_IN2	R/W	Xh	0h = IO3 1h = V_IN2
1	V_IN1	R/W	Xh	0h = IO2 1h = V_IN1
0	V_IN0	R/W	Xh	0h = IO1 1h = V_IN0

9.3.20 LUT_FS_0 Register (Offset = 324h) [Reset = 0Xh]

LUT_FS_0 is shown in Table 9-246.

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LUT2_3 to LUT2_0 function select

Table 9-246. LUT_FS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	LUT2_3_FS	R/W	Xh	0h = LUT 1h = PGEN
2	LUT2_2_FS	R/W	Xh	0h = LUT 1h = DFF
1	LUT2_1_FS	R/W	Xh	0h = LUT 1h = DFF
0	LUT2_0_FS	R/W	Xh	0h = LUT 1h = DFF

9.3.21 LUT_FS_1 Register (Offset = 325h) [Reset = XXh]

LUT_FS_1 is shown in Table 9-247.

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LUT3_5 to LUT3_0 function select

Table 9-247. LUT_FS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	LUT3_5_FS	R/W	Xh	0h = LUT 1h = DFF/SR
4	LUT3_4_FS	R/W	Xh	0h = LUT 1h = DFF/SR
3	LUT3_3_FS	R/W	Xh	0h = LUT 1h = DFF/SR
2	LUT3_2_FS	R/W	Xh	0h = LUT 1h = DFF/SR
1	LUT3_1_FS	R/W	Xh	0h = LUT 1h = DFF
0	LUT3_0_FS	R/W	Xh	0h = LUT 1h = DFF

9.3.22 LUT_FS_3 Register (Offset = 327h) [Reset = 0Xh]

LUT_FS_3 is shown in Table 9-248.

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LUT4_3 to LUT4_0 function select

Table 9-248. LUT_FS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	LUT4_3_FS	R/W	Xh	0h = LUT 1h = DFF
2	LUT4_2_FS	R/W	Xh	0h = LUT 1h = DFF
1	LUT4_1_FS	R/W	Xh	0h = LUT 1h = DFF
0	LUT4_0_FS	R/W	Xh	0h = LUT 1h = DFF

9.3.23 LUT2_0_CFG Register (Offset = 328h) [Reset = X0h]

LUT2_0_CFG is shown in Table 9-249.

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LUT2_0 / DFF0 configuration

Table 9-249. LUT2_0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	BIT3	R/W	Xh	LUT2[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT2[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT2[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT2[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.24 LUT2_1_CFG Register (Offset = 329h) [Reset = X0h]

LUT2_1_CFG is shown in Table 9-250.

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LUT2_1 / DFF1 configuration

Table 9-250. LUT2_1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	BIT3	R/W	Xh	LUT2[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT2[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT2[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT2[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.25 LUT2_2_CFG Register (Offset = 32Ah) [Reset = X0h]

LUT2_2_CFG is shown in Table 9-251.

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LUT2_2 / DFF2 configuration

Table 9-251. LUT2_2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	BIT3	R/W	Xh	LUT2[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT2[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT2[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT2[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

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9.3.26 LUT2_3_CFG0 Register (Offset = 32Eh) [Reset = XXh]

LUT2_3_CFG0 is shown in Table 9-252.

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LUT2_3 / PGEN configuration 0

Table 9-252. LUT2_3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	PGEN_RST	R/W	Xh	OTP_SPARE or PGEN RST LVL 0h = Low 1h = High
4	RESERVED	R	0h	Reserved
3:0	BITS3_0	R/W	Xh	LUT2[3:0] or PGEN SIZE 0h = 1 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8 8h = 9 9h = 10 Ah = 11 Bh = 12 Ch = 13 Dh = 14 Eh = 15 Fh = 16

9.3.27 LUT2_3_CFG1 Register (Offset = 32Fh) [Reset = X0h]

LUT2_3_CFG1 is shown in Table 9-253.

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PGEN configuration 1

Table 9-253. LUT2_3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_LSB	R/W	Xh	PGEN_DATA[7:0]

9.3.28 LUT2_3_CFG2 Register (Offset = 330h) [Reset = X0h]

LUT2_3_CFG2 is shown in Table 9-254.

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PGEN configuration 2

Table 9-254. LUT2_3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_MSB	R/W	Xh	PGEN_DATA[15:8]

9.3.29 LUT3_0_CFG Register (Offset = 334h) [Reset = X0h]

LUT3_0_CFG is shown in Table 9-255.

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LUT3_0 / DFF3 configuration

Table 9-255. LUT3_0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.30 LUT3_1_CFG Register (Offset = 335h) [Reset = X0h]

LUT3_1_CFG is shown in Table 9-256.

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LUT3_1 / DFF4 configuration

Table 9-256. LUT3_1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.31 LUT3_2_CFG0 Register (Offset = 336h) [Reset = X0h]

LUT3_2_CFG0 is shown in Table 9-257.

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LUT3_2 / DFF5 / SR0 configuration 0

Table 9-257. LUT3_2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]

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Table 9-257. LUT3_2_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.32 LUT3_2_CFG1 Register (Offset = 337h) [Reset = X0h]

LUT3_2_CFG1 is shown in Table 9-258.

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LUT3_2 / DFF5 / SR0 configuration 1

Table 9-258. LUT3_2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	DFF / SR INIT VAL

9.3.33 LUT3_3_CFG0 Register (Offset = 338h) [Reset = X0h]

LUT3_3_CFG0 is shown in Table 9-259.

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LUT3_3 / DFF6 / SR1 configuration 0

Table 9-259. LUT3_3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

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9.3.34 LUT3_3_CFG1 Register (Offset = 339h) [Reset = X0h]

LUT3_3_CFG1 is shown in Table 9-260.

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LUT3_3 / DFF6 / SR1 configuration 1

Table 9-260. LUT3_3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	DFF / SR INIT VAL

9.3.35 LUT3_4_CFG0 Register (Offset = 33Ah) [Reset = X0h]

LUT3_4_CFG0 is shown in Table 9-261.

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LUT3_4 / DFF7 / SR2 configuration 0

Table 9-261. LUT3_4_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.36 LUT3_4_CFG1 Register (Offset = 33Bh) [Reset = X0h]

LUT3_4_CFG1 is shown in Table 9-262.

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LUT3_4 / DFF7 / SR2 configuration 1

Table 9-262. LUT3_4_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	DFF / SR INIT VAL

9.3.37 LUT3_5_CFG0 Register (Offset = 33Ch) [Reset = X0h]

LUT3_5_CFG0 is shown in Table 9-263.

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LUT3_5 / DFF8 / SR3 configuration 0

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Table 9-263. LUT3_5_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.38 LUT3_5_CFG1 Register (Offset = 33Dh) [Reset = X0h]

LUT3_5_CFG1 is shown in Table 9-264.

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LUT3_5 / DFF8 / SR3 configuration 1

Table 9-264. LUT3_5_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	DFF / SR INIT VAL

9.3.39 LUT4_0_CFG0 Register (Offset = 344h) [Reset = X0h]

LUT4_0_CFG0 is shown in Table 9-265.

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LUT4_0 / DFF15 configuration 0

Table 9-265. LUT4_0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT4[7]
6	BIT6	R/W	0h	LUT4[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT4[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT4[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT4[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT4[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT4[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT4[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

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9.3.40 LUT4_0_CFG1 Register (Offset = 345h) [Reset = X0h]

LUT4_0_CFG1 is shown in Table 9-266.

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LUT4_0 / DFF15 configuration 1

Table 9-266. LUT4_0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	LUT4[15:8]

9.3.41 LUT4_1_CFG0 Register (Offset = 346h) [Reset = X0h]

LUT4_1_CFG0 is shown in Table 9-267.

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LUT4_1 / DFF16 configuration 0

Table 9-267. LUT4_1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT4[7]
6	BIT6	R/W	0h	LUT4[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT4[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT4[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT4[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT4[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT4[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT4[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.42 LUT4_1_CFG1 Register (Offset = 347h) [Reset = X0h]

LUT4_1_CFG1 is shown in Table 9-268.

Return to the Summary Table.

LUT4_1 / DFF16 configuration 1

Table 9-268. LUT4_1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	LUT4[15:8]

9.3.43 LUT4_2_CFG0 Register (Offset = 348h) [Reset = X0h]

LUT4_2_CFG0 is shown in Table 9-269.

Return to the Summary Table.

LUT4_2 / DFF17 configuration 0

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Table 9-269. LUT4_2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT4[7]
6	BIT6	R/W	0h	LUT4[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT4[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT4[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT4[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT4[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT4[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT4[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.44 LUT4_2_CFG1 Register (Offset = 349h) [Reset = X0h]

LUT4_2_CFG1 is shown in Table 9-270.

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LUT4_2 / DFF17 configuration 1

Table 9-270. LUT4_2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	LUT4[15:8]

9.3.45 LUT4_3_CFG0 Register (Offset = 34Ah) [Reset = X0h]

LUT4_3_CFG0 is shown in Table 9-271.

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LUT4_3 / DFF18 configuration 0

Table 9-271. LUT4_3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT4[7]
6	BIT6	R/W	0h	LUT4[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT4[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT4[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT4[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT4[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT4[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output

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Table 9-271. LUT4_3_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BIT0	R/W	Xh	LUT4[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.46 LUT4_3_CFG1 Register (Offset = 34Bh) [Reset = X0h]

LUT4_3_CFG1 is shown in Table 9-272.

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LUT4_3 / DFF18 configuration 1

Table 9-272. LUT4_3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BITS15_8	R/W	Xh	LUT4[15:8]

9.3.47 LUT3_6_CFG0 Register (Offset = 354h) [Reset = X0h]

LUT3_6_CFG0 is shown in Table 9-273.

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LDC0 configuration 0

Table 9-273. LUT3_6_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.48 LUT3_6_CFG1 Register (Offset = 355h) [Reset = X0h]

LUT3_6_CFG1 is shown in Table 9-274.

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LDC0 configuration 1

Table 9-274. LUT3_6_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

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9.3.49 LUT3_6_CFG2 Register (Offset = 356h) [Reset = X0h]

LUT3_6_CFG2 is shown in Table 9-275.

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LDC0 configuration 2

Table 9-275. LUT3_6_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.50 LUT3_6_CFG3 Register (Offset = 357h) [Reset = X0h]

LUT3_6_CFG3 is shown in Table 9-276.

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LDC0 configuration 3

Table 9-276. LUT3_6_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

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9.3.51 LUT3_6_CFG4 Register (Offset = 358h) [Reset = XXh]

LUT3_6_CFG4 is shown in Table 9-277.

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LDC0 configuration 4

Table 9-277. LUT3_6_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

9.3.52 LUT3_7_CFG0 Register (Offset = 359h) [Reset = X0h]

LUT3_7_CFG0 is shown in Table 9-278.

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LDC1 configuration 0

Table 9-278. LUT3_7_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.53 LUT3_7_CFG1 Register (Offset = 35Ah) [Reset = X0h]

LUT3_7_CFG1 is shown in Table 9-279.

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LDC1 configuration 1

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Table 9-279. LUT3_7_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

9.3.54 LUT3_7_CFG2 Register (Offset = 35Bh) [Reset = X0h]

LUT3_7_CFG2 is shown in Table 9-280.

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LDC1 configuration 2

Table 9-280. LUT3_7_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.55 LUT3_7_CFG3 Register (Offset = 35Ch) [Reset = X0h]

LUT3_7_CFG3 is shown in Table 9-281.

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LDC1 configuration 3

Table 9-281. LUT3_7_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted

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Table 9-281. LUT3_7_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.56 LUT3_7_CFG4 Register (Offset = 35Dh) [Reset = XXh]

LUT3_7_CFG4 is shown in Table 9-282.

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LDC1 configuration 4

Table 9-282. LUT3_7_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

9.3.57 LUT3_8_CFG0 Register (Offset = 35Eh) [Reset = X0h]

LUT3_8_CFG0 is shown in Table 9-283.

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LDC2 configuration 0

Table 9-283. LUT3_8_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.58 LUT3_8_CFG1 Register (Offset = 35Fh) [Reset = X0h]

LUT3_8_CFG1 is shown in Table 9-284.

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LDC2 configuration 1

Table 9-284. LUT3_8_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

9.3.59 LUT3_8_CFG2 Register (Offset = 360h) [Reset = X0h]

LUT3_8_CFG2 is shown in Table 9-285.

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LDC2 configuration 2

Table 9-285. LUT3_8_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.60 LUT3_8_CFG3 Register (Offset = 361h) [Reset = X0h]

LUT3_8_CFG3 is shown in Table 9-286.

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LDC2 configuration 3

Table 9-286. LUT3_8_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)

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Table 9-286. LUT3_8_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.61 LUT3_8_CFG4 Register (Offset = 362h) [Reset = XXh]

LUT3_8_CFG4 is shown in Table 9-287.

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LDC2 configuration 4

Table 9-287. LUT3_8_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

9.3.62 LUT3_9_CFG0 Register (Offset = 363h) [Reset = X0h]

LUT3_9_CFG0 is shown in Table 9-288.

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LDC3 configuration 0

Table 9-288. LUT3_9_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

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9.3.63 LUT3_9_CFG1 Register (Offset = 364h) [Reset = X0h]

LUT3_9_CFG1 is shown in Table 9-289.

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LDC3 configuration 1

Table 9-289. LUT3_9_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

9.3.64 LUT3_9_CFG2 Register (Offset = 365h) [Reset = X0h]

LUT3_9_CFG2 is shown in Table 9-290.

Return to the Summary Table.

LDC3 configuration 2

Table 9-290. LUT3_9_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.65 LUT3_9_CFG3 Register (Offset = 366h) [Reset = X0h]

LUT3_9_CFG3 is shown in Table 9-291.

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LDC3 configuration 3

Table 9-291. LUT3_9_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved

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Table 9-291. LUT3_9_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.66 LUT3_9_CFG4 Register (Offset = 367h) [Reset = XXh]

LUT3_9_CFG4 is shown in Table 9-292.

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LDC3 configuration 4

Table 9-292. LUT3_9_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

9.3.67 LUT3_10_CFG0 Register (Offset = 372h) [Reset = X0h]

LUT3_10_CFG0 is shown in Table 9-293.

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LDC4 configuration 0

Table 9-293. LUT3_10_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output

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Table 9-293. LUT3_10_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.68 LUT3_10_CFG1 Register (Offset = 373h) [Reset = X0h]

LUT3_10_CFG1 is shown in Table 9-294.

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LDC4 configuration 1

Table 9-294. LUT3_10_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA_7:0	R/W	Xh	CNT DATA[7:0]

9.3.69 LUT3_10_CFG2 Register (Offset = 374h) [Reset = X0h]

LUT3_10_CFG2 is shown in Table 9-295.

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LDC4 configuration 2

Table 9-295. LUT3_10_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA_15:8	R/W	Xh	CNT_DATA[15:8]

9.3.70 LUT3_10_CFG3 Register (Offset = 375h) [Reset = X0h]

LUT3_10_CFG3 is shown in Table 9-296.

Return to the Summary Table.

LDC4 configuration 3

Table 9-296. LUT3_10_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX

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Table 9-296. LUT3_10_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.71 LUT3_10_CFG4 Register (Offset = 376h) [Reset = X0h]

LUT3_10_CFG4 is shown in Table 9-297.

Return to the Summary Table.

LDC4 configuration 4

Table 9-297. LUT3_10_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.72 LUT3_10_CFG5 Register (Offset = 377h) [Reset = XXh]

LUT3_10_CFG5 is shown in Table 9-298.

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LDC4 configuration 5

Table 9-298. LUT3_10_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

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9.3.73 LUT3_11_CFG0 Register (Offset = 378h) [Reset = X0h]

LUT3_11_CFG0 is shown in Table 9-299.

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LDC5 configuration 0

Table 9-299. LUT3_11_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

9.3.74 LUT3_11_CFG1 Register (Offset = 379h) [Reset = X0h]

LUT3_11_CFG1 is shown in Table 9-300.

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LDC5 configuration 1

Table 9-300. LUT3_11_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA_7:0	R/W	Xh	CNT DATA[7:0]

9.3.75 LUT3_11_CFG2 Register (Offset = 37Ah) [Reset = X0h]

LUT3_11_CFG2 is shown in Table 9-301.

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LDC5 configuration 2

Table 9-301. LUT3_11_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA_15:8	R/W	Xh	CNT_DATA[15:8]

9.3.76 LUT3_11_CFG3 Register (Offset = 37Bh) [Reset = X0h]

LUT3_11_CFG3 is shown in Table 9-302.

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LDC5 configuration 3

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Table 9-302. LUT3_11_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.77 LUT3_11_CFG4 Register (Offset = 37Ch) [Reset = X0h]

LUT3_11_CFG4 is shown in Table 9-303.

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LDC5 configuration 4

Table 9-303. LUT3_11_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.78 LUT3_11_CFG5 Register (Offset = 37Dh) [Reset = XXh]

LUT3_11_CFG5 is shown in Table 9-304.

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LDC5 configuration 5

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Table 9-304. LUT3_11_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

9.3.79 CNT6_FSM0_CFG0 Register (Offset = 37Eh) [Reset = X0h]

CNT6_FSM0_CFG0 is shown in Table 9-305.

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Table 9-305. CNT6_FSM0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

9.3.80 CNT6_FSM0_CFG1 Register (Offset = 37Fh) [Reset = X0h]

CNT6_FSM0_CFG1 is shown in Table 9-306.

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Table 9-306. CNT6_FSM0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

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9.3.81 CNT6_FSM0_CFG2 Register (Offset = 380h) [Reset = 0Xh]

CNT6_FSM0_CFG2 is shown in Table 9-307.

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Table 9-307. CNT6_FSM0_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.82 CNT7_FSM1_CFG0 Register (Offset = 381h) [Reset = X0h]

CNT7_FSM1_CFG0 is shown in Table 9-308.

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Table 9-308. CNT7_FSM1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

9.3.83 CNT7_FSM1_CFG1 Register (Offset = 382h) [Reset = X0h]

CNT7_FSM1_CFG1 is shown in Table 9-309.

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Table 9-309. CNT7_FSM1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX

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Table 9-309. CNT7_FSM1_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.84 CNT7_FSM1_CFG2 Register (Offset = 383h) [Reset = 0Xh]

CNT7_FSM1_CFG2 is shown in Table 9-310.

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Table 9-310. CNT7_FSM1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.85 CNT8_FSM2_CFG0 Register (Offset = 384h) [Reset = X0h]

CNT8_FSM2_CFG0 is shown in Table 9-311.

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Table 9-311. CNT8_FSM2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

9.3.86 CNT8_FSM2_CFG1 Register (Offset = 385h) [Reset = X0h]

CNT8_FSM2_CFG1 is shown in Table 9-312.

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Table 9-312. CNT8_FSM2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.87 CNT8_FSM2_CFG2 Register (Offset = 386h) [Reset = 0Xh]

CNT8_FSM2_CFG2 is shown in Table 9-313.

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Table 9-313. CNT8_FSM2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.88 CNT9_FSM3_CFG0 Register (Offset = 387h) [Reset = X0h]

CNT9_FSM3_CFG0 is shown in Table 9-314.

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Table 9-314. CNT9_FSM3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

9.3.89 CNT9_FSM3_CFG1 Register (Offset = 388h) [Reset = X0h]

CNT9_FSM3_CFG1 is shown in Table 9-315.

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Table 9-315. CNT9_FSM3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

9.3.90 CNT9_FSM3_CFG2 Register (Offset = 389h) [Reset = 0Xh]

CNT9_FSM3_CFG2 is shown in Table 9-316.

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Table 9-316. CNT9_FSM3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted

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Table 9-316. CNT9_FSM3_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

9.3.91 PWM_GEN0_CFG Register (Offset = 38Ah) [Reset = X0h]

PWM_GEN0_CFG is shown in Table 9-317.

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Table 9-317. PWM_GEN0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

9.3.92 PWM_GEN1_CFG Register (Offset = 38Bh) [Reset = X0h]

PWM_GEN1_CFG is shown in Table 9-318.

Return to the Summary Table.

Table 9-318. PWM_GEN1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

9.3.93 PWM_GEN2_CFG Register (Offset = 38Ch) [Reset = X0h]

PWM_GEN2_CFG is shown in Table 9-319.

Return to the Summary Table.

Table 9-319. PWM_GEN2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output

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Table 9-319. PWM_GEN2_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

9.3.94 PWM_GEN3_CFG Register (Offset = 38Dh) [Reset = X0h]

PWM_GEN3_CFG is shown in Table 9-320.

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Table 9-320. PWM_GEN3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

9.3.95 PWM_SRC_CFG Register (Offset = 38Eh) [Reset = X0h]

PWM_SRC_CFG is shown in Table 9-321.

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Table 9-321. PWM_SRC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PWM_GEN3_DATA_SEL	R/W	0h	PWM3 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3
5:4	PWM_GEN2_DATA_SEL	R/W	0h	PWM2 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3
3:2	PWM_GEN1_DATA_SEL	R/W	Xh	PWM1 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3
1:0	PWM_GEN0_DATA_SEL	R/W	Xh	PWM0 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3

9.3.96 SM_CFG0 Register (Offset = 38Fh) [Reset = XXh]

SM_CFG0 is shown in Table 9-322.

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Table 9-322. SM_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

Table 9-322. SM_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	SM_S1_IN0	R/W	Xh	STATE1 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S0_IN0	R/W	Xh	STATE0 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.97 SM_CFG1 Register (Offset = 390h) [Reset = XXh]

SM_CFG1 is shown in Table 9-323.

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Table 9-323. SM_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S1_IN1	R/W	Xh	STATE1 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S0_IN1	R/W	Xh	STATE0 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.98 SM_CFG2 Register (Offset = 391h) [Reset = XXh]

SM_CFG2 is shown in Table 9-324.

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Table 9-324. SM_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S1_IN2	R/W	Xh	STATE1 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved

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Table 9-324. SM_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	SM_S0_IN2	R/W	Xh	STATE0 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.99 SM_CFG3 Register (Offset = 392h) [Reset = XXh]

SM_CFG3 is shown in Table 9-325.

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Table 9-325. SM_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S3_IN0	R/W	Xh	STATE3 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S2_IN0	R/W	Xh	STATE2 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.100 SM_CFG4 Register (Offset = 393h) [Reset = XXh]

SM_CFG4 is shown in Table 9-326.

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Table 9-326. SM_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S3_IN1	R/W	Xh	STATE3 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S2_IN1	R/W	Xh	STATE2 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

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9.3.101 SM_CFG5 Register (Offset = 394h) [Reset = XXh]

SM_CFG5 is shown in Table 9-327.

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Table 9-327. SM_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S3_IN2	R/W	Xh	STATE3 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S2_IN2	R/W	Xh	STATE2 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.102 SM_CFG6 Register (Offset = 395h) [Reset = XXh]

SM_CFG6 is shown in Table 9-328.

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Table 9-328. SM_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S5_IN0	R/W	Xh	STATE5 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S4_IN0	R/W	Xh	STATE4 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.103 SM_CFG7 Register (Offset = 396h) [Reset = XXh]

SM_CFG7 is shown in Table 9-329.

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Table 9-329. SM_CFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

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Table 9-329. SM_CFG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	SM_S5_IN1	R/W	Xh	STATE5 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S4_IN1	R/W	Xh	STATE4 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.104 SM_CFG8 Register (Offset = 397h) [Reset = XXh]

SM_CFG8 is shown in Table 9-330.

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Table 9-330. SM_CFG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S5_IN2	R/W	Xh	STATE5 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S4_IN2	R/W	Xh	STATE4 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.105 SM_CFG9 Register (Offset = 398h) [Reset = XXh]

SM_CFG9 is shown in Table 9-331.

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Table 9-331. SM_CFG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S7_IN0	R/W	Xh	STATE7 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved

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Table 9-331. SM_CFG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	SM_S6_IN0	R/W	Xh	STATE6 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.106 SM_CFG10 Register (Offset = 399h) [Reset = XXh]

SM_CFG10 is shown in Table 9-332.

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Table 9-332. SM_CFG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S7_IN1	R/W	Xh	STATE7 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S6_IN1	R/W	Xh	STATE6 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.107 SM_CFG11 Register (Offset = 39Ah) [Reset = 0Xh]

SM_CFG11 is shown in Table 9-333.

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Table 9-333. SM_CFG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SM_SYNC_EN	R/W	0h	State machine synchronous mode clock sync enable 0h = Disabled 1h = Enabled
6:4	SM_S7_IN2	R/W	0h	STATE7 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S6_IN2	R/W	Xh	STATE6 IN2 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

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9.3.108 SM_CFG12 Register (Offset = 3A7h) [Reset = X0h]

SM_CFG12 is shown in Table 9-334.

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Table 9-334. SM_CFG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SM_CLK_SEL	R/W	0h	State machine CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3	SM_MODE	R/W	Xh	State machine synchronous mode select 0h = Asynchronous 1h = Synchronous
2:0	SM_INIT_STATE	R/W	Xh	State machine initial state select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

9.3.109 SM_CFG13 Register (Offset = 3A8h) [Reset = X0h]

SM_CFG13 is shown in Table 9-335.

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Table 9-335. SM_CFG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S0_OUT_CFG	R/W	Xh	

9.3.110 SM_CFG14 Register (Offset = 3A9h) [Reset = X0h]

SM_CFG14 is shown in Table 9-336.

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Table 9-336. SM_CFG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S1_OUT_CFG	R/W	Xh	

9.3.111 SM_CFG15 Register (Offset = 3AAh) [Reset = X0h]

SM_CFG15 is shown in Table 9-337.

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Table 9-337. SM_CFG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S2_OUT_CFG	R/W	Xh	

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9.3.112 SM_CFG16 Register (Offset = 3ABh) [Reset = X0h]

SM_CFG16 is shown in Table 9-338.

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Table 9-338. SM_CFG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S3_OUT_CFG	R/W	Xh	

9.3.113 SM_CFG17 Register (Offset = 3ACh) [Reset = X0h]

SM_CFG17 is shown in Table 9-339.

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Table 9-339. SM_CFG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S4_OUT_CFG	R/W	Xh	

9.3.114 SM_CFG18 Register (Offset = 3ADh) [Reset = X0h]

SM_CFG18 is shown in Table 9-340.

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Table 9-340. SM_CFG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S5_OUT_CFG	R/W	Xh	

9.3.115 SM_CFG19 Register (Offset = 3AEh) [Reset = X0h]

SM_CFG19 is shown in Table 9-341.

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Table 9-341. SM_CFG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S6_OUT_CFG	R/W	Xh	

9.3.116 SM_CFG20 Register (Offset = 3AFh) [Reset = X0h]

SM_CFG20 is shown in Table 9-342.

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Table 9-342. SM_CFG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S7_OUT_CFG	R/W	Xh	

9.3.117 WDT_CFG0 Register (Offset = 3B8h) [Reset = X0h]

WDT_CFG0 is shown in Table 9-343.

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Table 9-343. WDT_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WDT_TIMEOUT_DATA	R/W	Xh	WDT Timeout Period Counter DATA

9.3.118 WDT_CFG1 Register (Offset = 3B9h) [Reset = X0h]

WDT_CFG1 is shown in Table 9-344.

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Table 9-344. WDT_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WDT_OUT_DATA	R/W	Xh	WDT Output Period Counter DATA

9.3.119 WDT_CFG2 Register (Offset = 3BAh) [Reset = 0Xh]

WDT_CFG2 is shown in Table 9-345.

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Table 9-345. WDT_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	WDT_CLK_SEL	R/W	0h	WDT CLK SEL 0h = OSC2 (25MHz) 1h = OSC2 / 4 2h = OSC1 (2MHz) 3h = OSC1 / 8 4h = OSC1 / 64 5h = OSC1 / 512 6h = OSC0 (2kHz) 7h = OSC0 / 8 8h = OSC0 / 64 9h = OSC0 / 512 Ah = OSC0 / 4096 Bh = OSC0 / 32768 Ch = OSC0 / 262144 Dh = Reserved Eh = Reserved Fh = External CLK from CMX
3:2	RESERVED	R	0h	Reserved
1	WDT_100X_EN	R/W	Xh	WDT 100X CLK multiplier EN 0h = Disabled 1h = Enabled
0	WDT_EN_SEL	R/W	Xh	WDT EN function select 0h = Reset CNT 1h = Pause CNT

9.3.120 PFLT0_CFG Register (Offset = 3BBh) [Reset = XXh]

PFLT0_CFG is shown in Table 9-346.

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Table 9-346. PFLT0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:4	PFLT_DLY_SEL	R/W	Xh	Programmable filter delay value select 0h = 125ns 1h = 250ns 2h = 375ns 3h = 500ns
3	PFLT_POL	R/W	Xh	Programmable filter output polarity select 0h = Non-inverted 1h = Inverted
2	RESERVED	R	0h	Reserved

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Table 9-346. PFLT0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PFLT_EDGE_SEL	R/W	Xh	Programmable filter edge select 0h = Rising edge 1h = Falling edge 2h = Both edge 3h = Filter

9.3.121 PFLT1_CFG Register (Offset = 3BCh) [Reset = XXh]

PFLT1_CFG is shown in Table 9-347.

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Table 9-347. PFLT1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:4	PFLT_DLY_SEL	R/W	Xh	Programmable filter delay value select 0h = 125ns 1h = 250ns 2h = 375ns 3h = 500ns
3	PFLT_POL	R/W	Xh	Programmable filter output polarity select 0h = Non-inverted 1h = Inverted
2	RESERVED	R	0h	Reserved
1:0	PFLT_EDGE_SEL	R/W	Xh	Programmable filter edge select 0h = Rising edge 1h = Falling edge 2h = Both edge 3h = Filter

9.3.122 FILT_CFG Register (Offset = 3BDh) [Reset = 0Xh]

FILT_CFG is shown in Table 9-348.

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Table 9-348. FILT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	FLT_POL	R/W	Xh	Filter output polarity select 0h = Non-inverted 1h = Inverted
2	OTP_SPARE	R	0h	SPARE
1:0	FLT_EDGE_SEL	R/W	Xh	Filter / Edge detect edge select 0h = Rising edge 1h = Falling edge 2h = Both edge 3h = Filter

9.3.123 OSC0_CFG0 Register (Offset = 3BEh) [Reset = XXh]

OSC0_CFG0 is shown in Table 9-349.

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Table 9-349. OSC0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	CTRL_SRC	R/W	Xh	OSC power control source select 0h = From register 1h = From CMX
5	CTRL_SEL	R/W	Xh	OSC power control polarity select 0h = Power down (Low enables OSC, High disables OSC) 1h = Reserved

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Table 9-349. OSC0_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SRC_SEL	R/W	Xh	OSC frequency source select 0h = Internal OSC 1h = External clock
3:2	PDIV	R/W	Xh	OSC pre-divider select 0h = / 1 1h = / 2 2h = / 4 3h = / 8
1	RESERVED	R	0h	Reserved
0	PWR_MODE	R/W	Xh	OSC power mode select 0h = Auto power on 1h = Force power on

9.3.124 OSC0_CFG1 Register (Offset = 3BFh) [Reset = X0h]

OSC0_CFG1 is shown in Table 9-350.

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Table 9-350. OSC0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT1_EN	R/W	0h	OSC OUT1 enable 0h = Disabled 1h = Enabled
6:4	OUT1_DIV	R/W	0h	OSC OUT1 secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64
3	OUT0_EN	R/W	Xh	OSC OUT0 enable 0h = Disabled 1h = Enabled
2:0	OUT0_DIV	R/W	Xh	OSC OUT0 secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64

9.3.125 OSC1_CFG0 Register (Offset = 3C0h) [Reset = XXh]

OSC1_CFG0 is shown in Table 9-351.

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Table 9-351. OSC1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	CTRL_SRC	R/W	Xh	OSC power control source select 0h = From register 1h = From CMX
5	CTRL_SEL	R/W	Xh	OSC power control polarity select 0h = Power down (Low enables OSC, High disables OSC) 1h = Reserved
4	SRC_SEL	R/W	Xh	OSC frequency source select 0h = Internal OSC 1h = External clock
3:2	PDIV	R/W	Xh	OSC pre-divider select 0h = / 1 1h = / 2 2h = / 4 3h = / 8
1	RESERVED	R	0h	Reserved

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Table 9-351. OSC1_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PWR_MODE	R/W	Xh	OSC power mode select 0h = Auto power on 1h = Force power on

9.3.126 OSC1_CFG1 Register (Offset = 3C1h) [Reset = X0h]

OSC1_CFG1 is shown in Table 9-352.

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Table 9-352. OSC1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT1_EN	R/W	0h	OSC OUT1 enable 0h = Disabled 1h = Enabled
6:4	OUT1_DIV	R/W	0h	OSC OUT1 secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64
3	OUT0_EN	R/W	Xh	OSC OUT0 enable 0h = Disabled 1h = Enabled
2:0	OUT0_DIV	R/W	Xh	OSC OUT0 secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64

9.3.127 OSC2_CFG0 Register (Offset = 3C2h) [Reset = 0Xh]

OSC2_CFG0 is shown in Table 9-353.

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Table 9-353. OSC2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SU_DLY	R/W	0h	OSC startup delay control 0h = Enabled 1h = Disabled
6	CTRL_SRC	R/W	0h	OSC power control source select 0h = From register 1h = From CMX
5	CTRL_SEL	R/W	0h	OSC power control polarity select 0h = Power down (Low enables OSC, High disables OSC) 1h = Reserved
4	SRC_SEL	R/W	0h	OSC frequency source select 0h = Internal OSC 1h = External clock
3:2	PDIV	R/W	0h	OSC pre-divider select 0h = / 1 1h = / 2 2h = / 4 3h = / 8
1	RESERVED	R	0h	Reserved
0	PWR_MODE	R/W	Xh	OSC power mode select 0h = Auto power on 1h = Force power on

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9.3.128 OSC2_CFG1 Register (Offset = 3C3h) [Reset = 0Xh]

OSC2_CFG1 is shown in Table 9-354.

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Table 9-354. OSC2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	OUT_EN	R/W	Xh	OSC OUT enable 0h = Disabled 1h = Enabled
2:0	OUT_DIV	R/W	Xh	OSC OUT secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64

9.3.129 ACMP0_CFG0 Register (Offset = 3C6h) [Reset = X0h]

ACMP0_CFG0 is shown in Table 9-355.

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Table 9-355. ACMP0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BW_SEL	R/W	0h	ACMP bandwidth select 0h = High bandwidth 1h = Low bandwidth 2h = Reserved 3h = Reserved
5:4	INP_SEL	R/W	0h	ACMP input source select 0h = ACMP IN0 1h = ACMP IN1 2h = ACMP IN2 3h = ACMP IN3
3:2	GAIN_SEL	R/W	Xh	ACMP gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	ACMP hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

9.3.130 ACMP0_CFG1 Register (Offset = 3C7h) [Reset = XXh]

ACMP0_CFG1 is shown in Table 9-356.

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Table 9-356. ACMP0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 9-356. ACMP0_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VREF_SEL	R/W	Xh	ACMP VREF select 0h = 32mV 1h = 64mV 2h = 96mV 3h = 128mV 4h = 160mV 5h = 192mV 6h = 224mV 7h = 256mV 8h = 288mV 9h = 320mV Ah = 352mV Bh = 384mV Ch = 416mV Dh = 448mV Eh = 480mV Fh = 512mV 10h = 544mV 11h = 576mV 12h = 608mV 13h = 640mV 14h = 672mV 15h = 704mV 16h = 736mV 17h = 768mV 18h = 800mV 19h = 832mV 1Ah = 864mV 1Bh = 896mV 1Ch = 928mV 1Dh = 960mV 1Eh = 992mV 1Fh = 1.024V 20h = 1.056V 21h = 1.088V 22h = 1.120V 23h = 1.152V 24h = 1.184V 25h = 1.216V 26h = 1.248V 27h = 1.280V 28h = 1.312V 29h = 1.344V 2Ah = 1.376V 2Bh = 1.408V 2Ch = 1.440V 2Dh = 1.472V 2Eh = 1.504V 2Fh = 1.536V 30h = 1.568V 31h = 1.600V 32h = 1.632V 33h = 1.664V 34h = 1.696V 35h = 1.728V 36h = 1.760V 37h = 1.792V 38h = 1.824V 39h = 1.856V 3Ah = 1.888V 3Bh = 1.920V 3Ch = 1.952V 3Dh = 1.984V 3Eh = 2.016V 3Fh = External VREF

9.3.131 ACMP1_CFG0 Register (Offset = 3C8h) [Reset = X0h]

ACMP1_CFG0 is shown in Table 9-357.

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Table 9-357. ACMP1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BW_SEL	R/W	0h	ACMP bandwidth select 0h = High bandwidth 1h = Low bandwidth 2h = Reserved 3h = Reserved

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Table 9-357. ACMP1_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	INP_SEL	R/W	0h	ACMP input source select 0h = ACMP IN0 1h = ACMP IN1 2h = ACMP IN2 3h = ACMP IN3
3:2	GAIN_SEL	R/W	Xh	ACMP gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	ACMP hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

9.3.132 ACMP1_CFG1 Register (Offset = 3C9h) [Reset = XXh]

ACMP1_CFG1 is shown in Table 9-358.

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Table 9-358. ACMP1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 9-358. ACMP1_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VREF_SEL	R/W	Xh	ACMP VREF select 0h = 32mV 1h = 64mV 2h = 96mV 3h = 128mV 4h = 160mV 5h = 192mV 6h = 224mV 7h = 256mV 8h = 288mV 9h = 320mV Ah = 352mV Bh = 384mV Ch = 416mV Dh = 448mV Eh = 480mV Fh = 512mV 10h = 544mV 11h = 576mV 12h = 608mV 13h = 640mV 14h = 672mV 15h = 704mV 16h = 736mV 17h = 768mV 18h = 800mV 19h = 832mV 1Ah = 864mV 1Bh = 896mV 1Ch = 928mV 1Dh = 960mV 1Eh = 992mV 1Fh = 1.024V 20h = 1.056V 21h = 1.088V 22h = 1.120V 23h = 1.152V 24h = 1.184V 25h = 1.216V 26h = 1.248V 27h = 1.280V 28h = 1.312V 29h = 1.344V 2Ah = 1.376V 2Bh = 1.408V 2Ch = 1.440V 2Dh = 1.472V 2Eh = 1.504V 2Fh = 1.536V 30h = 1.568V 31h = 1.600V 32h = 1.632V 33h = 1.664V 34h = 1.696V 35h = 1.728V 36h = 1.760V 37h = 1.792V 38h = 1.824V 39h = 1.856V 3Ah = 1.888V 3Bh = 1.920V 3Ch = 1.952V 3Dh = 1.984V 3Eh = 2.016V 3Fh = External VREF

9.3.133 ACMP2_CFG0 Register (Offset = 3CAh) [Reset = X0h]

ACMP2_CFG0 is shown in Table 9-359.

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Table 9-359. ACMP2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BW_SEL	R/W	0h	ACMP bandwidth select 0h = High bandwidth 1h = Low bandwidth 2h = Reserved 3h = Reserved

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Table 9-359. ACMP2_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	INP_SEL	R/W	0h	ACMP input source select 0h = ACMP IN0 1h = ACMP IN1 2h = ACMP IN2 3h = ACMP IN3
3:2	GAIN_SEL	R/W	Xh	ACMP gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	ACMP hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

9.3.134 ACMP2_CFG1 Register (Offset = 3CBh) [Reset = XXh]

ACMP2_CFG1 is shown in Table 9-360.

Return to the Summary Table.

Table 9-360. ACMP2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 9-360. ACMP2_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VREF_SEL	R/W	Xh	ACMP VREF select 0h = 32mV 1h = 64mV 2h = 96mV 3h = 128mV 4h = 160mV 5h = 192mV 6h = 224mV 7h = 256mV 8h = 288mV 9h = 320mV Ah = 352mV Bh = 384mV Ch = 416mV Dh = 448mV Eh = 480mV Fh = 512mV 10h = 544mV 11h = 576mV 12h = 608mV 13h = 640mV 14h = 672mV 15h = 704mV 16h = 736mV 17h = 768mV 18h = 800mV 19h = 832mV 1Ah = 864mV 1Bh = 896mV 1Ch = 928mV 1Dh = 960mV 1Eh = 992mV 1Fh = 1.024V 20h = 1.056V 21h = 1.088V 22h = 1.120V 23h = 1.152V 24h = 1.184V 25h = 1.216V 26h = 1.248V 27h = 1.280V 28h = 1.312V 29h = 1.344V 2Ah = 1.376V 2Bh = 1.408V 2Ch = 1.440V 2Dh = 1.472V 2Eh = 1.504V 2Fh = 1.536V 30h = 1.568V 31h = 1.600V 32h = 1.632V 33h = 1.664V 34h = 1.696V 35h = 1.728V 36h = 1.760V 37h = 1.792V 38h = 1.824V 39h = 1.856V 3Ah = 1.888V 3Bh = 1.920V 3Ch = 1.952V 3Dh = 1.984V 3Eh = 2.016V 3Fh = External VREF

9.3.135 ACMP3_CFG0 Register (Offset = 3CCh) [Reset = X0h]

ACMP3_CFG0 is shown in Table 9-361.

Return to the Summary Table.

Table 9-361. ACMP3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BW_SEL	R/W	0h	ACMP bandwidth select 0h = High bandwidth 1h = Low bandwidth 2h = Reserved 3h = Reserved

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Table 9-361. ACMP3_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	INP_SEL	R/W	0h	ACMP input source select 0h = ACMP IN0 1h = ACMP IN1 2h = ACMP IN2 3h = ACMP IN3
3:2	GAIN_SEL	R/W	Xh	ACMP gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	ACMP hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

9.3.136 ACMP3_CFG1 Register (Offset = 3CDh) [Reset = XXh]

ACMP3_CFG1 is shown in Table 9-362.

Return to the Summary Table.

Table 9-362. ACMP3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 9-362. ACMP3_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VREF_SEL	R/W	Xh	ACMP VREF select 0h = 32mV 1h = 64mV 2h = 96mV 3h = 128mV 4h = 160mV 5h = 192mV 6h = 224mV 7h = 256mV 8h = 288mV 9h = 320mV Ah = 352mV Bh = 384mV Ch = 416mV Dh = 448mV Eh = 480mV Fh = 512mV 10h = 544mV 11h = 576mV 12h = 608mV 13h = 640mV 14h = 672mV 15h = 704mV 16h = 736mV 17h = 768mV 18h = 800mV 19h = 832mV 1Ah = 864mV 1Bh = 896mV 1Ch = 928mV 1Dh = 960mV 1Eh = 992mV 1Fh = 1.024V 20h = 1.056V 21h = 1.088V 22h = 1.120V 23h = 1.152V 24h = 1.184V 25h = 1.216V 26h = 1.248V 27h = 1.280V 28h = 1.312V 29h = 1.344V 2Ah = 1.376V 2Bh = 1.408V 2Ch = 1.440V 2Dh = 1.472V 2Eh = 1.504V 2Fh = 1.536V 30h = 1.568V 31h = 1.600V 32h = 1.632V 33h = 1.664V 34h = 1.696V 35h = 1.728V 36h = 1.760V 37h = 1.792V 38h = 1.824V 39h = 1.856V 3Ah = 1.888V 3Bh = 1.920V 3Ch = 1.952V 3Dh = 1.984V 3Eh = 2.016V 3Fh = External VREF

9.3.137 MCACMP_CFG0 Register (Offset = 3CFh) [Reset = 0Xh]

MCACMP_CFG0 is shown in Table 9-363.

Return to the Summary Table.

Table 9-363. MCACMP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TS_INP_EN	R/W	0h	Temperature sensor input to McACMP enable 0h = Disabled 1h = Enabled
6	VCC_INP_EN	R/W	0h	VCC input to McACMP enable 0h = Disabled 1h = Enabled

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Table 9-363. MCACMP_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SYNC_EN	R/W	0h	McACMP output synchronicity select 0h = Asychronous 1h = Synchronous
4	MCS_MODE	R/W	0h	McACMP trigger mode select 0h = Level sensitive EN mode 1h = Edge sensitive EN mode
3:2	CH_EN	R/W	0h	Number of channels sampled select 0h = 1 channel 1h = 2 channels 2h = 3 channels 3h = 4 channels
1	RESERVED	R	0h	Reserved
0	MCS_EN	R/W	Xh	Sampling mode select 0h = Regular mode (single channel) 1h = Multi-channel mode

9.3.138 MCACMP_CFG1 Register (Offset = 3D0h) [Reset = 0Xh]

MCACMP_CFG1 is shown in Table 9-364.

Return to the Summary Table.

Table 9-364. MCACMP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BW_SEL	R/W	0h	McACMP bandwidth select 0h = High bandwidth 1h = Low bandwidth 2h = Reserved 3h = Reserved
5:3	RESERVED	R	0h	Reserved
2	EDGE_SEL	R/W	Xh	McACMP sampling edge select 0h = Sample on negative edge of CLK 1h = Sample on positive edge of CLK
1:0	MCS_CLK_SEL	R/W	Xh	McACMP CLK select 0h = OSC1 (2MHz) / 20 1h = OSC1 / 40 2h = OSC0 (2kHz) 3h = OSC0 / 2

9.3.139 MCACMP_CH0_CFG0 Register (Offset = 3D1h) [Reset = XXh]

MCACMP_CH0_CFG0 is shown in Table 9-365.

Return to the Summary Table.

Table 9-365. MCACMP_CH0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH0 RST EN select 0h = Disabled 1h = Enabled
5:4	INP_SEL	R/W	Xh	McACMP CH0 input source select 0h = McACMP IN0 1h = McACMP IN1 2h = McACMP IN2 (or VCC) 3h = McACMP IN3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH0 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH0 hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

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9.3.140 MCACMP_CH0_CFG1 Register (Offset = 3D2h) [Reset = X0h]

MCACMP_CH0_CFG1 is shown in Table 9-366.

Return to the Summary Table.

Table 9-366. MCACMP_CH0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH_VREF_SEL	R/W	0h	No. of VREF select 0h = 1 VREF 1h = 2 VREF 2h = Reserved 3h = Reserved
5:0	VREF_SEL	R/W	Xh	McACMP CH0_0 VREF select 0h = 32mV 1h = 64mV 2h = 96mV 3h = 128mV 4h = 160mV 5h = 192mV 6h = 224mV 7h = 256mV 8h = 288mV 9h = 320mV Ah = 352mV Bh = 384mV Ch = 416mV Dh = 448mV Eh = 480mV Fh = 512mV 10h = 544mV 11h = 576mV 12h = 608mV 13h = 640mV 14h = 672mV 15h = 704mV 16h = 736mV 17h = 768mV 18h = 800mV 19h = 832mV 1Ah = 864mV 1Bh = 896mV 1Ch = 928mV 1Dh = 960mV 1Eh = 992mV 1Fh = 1.024V 20h = 1.056V 21h = 1.088V 22h = 1.120V 23h = 1.152V 24h = 1.184V 25h = 1.216V 26h = 1.248V 27h = 1.280V 28h = 1.312V 29h = 1.344V 2Ah = 1.376V 2Bh = 1.408V 2Ch = 1.440V 2Dh = 1.472V 2Eh = 1.504V 2Fh = 1.536V 30h = 1.568V 31h = 1.600V 32h = 1.632V 33h = 1.664V 34h = 1.696V 35h = 1.728V 36h = 1.760V 37h = 1.792V 38h = 1.824V 39h = 1.856V 3Ah = 1.888V 3Bh = 1.920V 3Ch = 1.952V 3Dh = 1.984V 3Eh = 2.016V 3Fh = External VREF

9.3.141 MCACMP_CH0_CFG2 Register (Offset = 3D3h) [Reset = XXh]

MCACMP_CH0_CFG2 is shown in Table 9-367.

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Table 9-367. MCACMP_CH0_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_SEL1	R/W	Xh	McACMP CH0_1 VREF select (same options as CH0_0)

9.3.142 MCACMP_CH1_CFG0 Register (Offset = 3D6h) [Reset = XXh]

MCACMP_CH1_CFG0 is shown in Table 9-368.

Return to the Summary Table.

Table 9-368. MCACMP_CH1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH1 RST EN select 0h = Disabled 1h = Enabled
5:4	INP_SEL	R/W	Xh	McACMP CH1 input source select 0h = McACMP IN0 1h = McACMP IN1 2h = McACMP IN2 (or VCC) 3h = McACMP IN3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH1 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH1 hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

9.3.143 MCACMP_CH1_CFG1 Register (Offset = 3D7h) [Reset = X0h]

MCACMP_CH1_CFG1 is shown in Table 9-369.

Return to the Summary Table.

Table 9-369. MCACMP_CH1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH_VREF_SEL	R/W	0h	No. of VREF select 0h = 1 VREF 1h = 2 VREF 2h = Reserved 3h = Reserved
5:0	VREF_SEL	R/W	Xh	McACMP CH1_0 VREF select (same options as CH0_0)

9.3.144 MCACMP_CH1_CFG2 Register (Offset = 3D8h) [Reset = XXh]

MCACMP_CH1_CFG2 is shown in Table 9-370.

Return to the Summary Table.

Table 9-370. MCACMP_CH1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_SEL1	R/W	Xh	McACMP CH1_1 VREF select (same options as CH0_0)

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9.3.145 MCACMP_CH2_CFG0 Register (Offset = 3DBh) [Reset = XXh]

MCACMP_CH2_CFG0 is shown in Table 9-371.

Return to the Summary Table.

Table 9-371. MCACMP_CH2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH2 RST EN select 0h = Disabled 1h = Enabled
5:4	INP_SEL	R/W	Xh	McACMP CH2 input source select 0h = McACMP IN0 1h = McACMP IN1 2h = McACMP IN2 (or VCC) 3h = McACMP IN3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH2 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH2 hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

9.3.146 MCACMP_CH2_CFG1 Register (Offset = 3DCh) [Reset = X0h]

MCACMP_CH2_CFG1 is shown in Table 9-372.

Return to the Summary Table.

Table 9-372. MCACMP_CH2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH_VREF_SEL	R/W	0h	No. of VREF select 0h = 1 VREF 1h = 2 VREF 2h = Reserved 3h = Reserved
5:0	VREF_SEL	R/W	Xh	McACMP CH2_0 VREF select (same options as CH0_0)

9.3.147 MCACMP_CH2_CFG2 Register (Offset = 3DDh) [Reset = XXh]

MCACMP_CH2_CFG2 is shown in Table 9-373.

Return to the Summary Table.

Table 9-373. MCACMP_CH2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_SEL1	R/W	Xh	McACMP CH2_1 VREF select (same options as CH0_0)

9.3.148 MCACMP_CH3_CFG0 Register (Offset = 3E0h) [Reset = XXh]

MCACMP_CH3_CFG0 is shown in Table 9-374.

Return to the Summary Table.

Table 9-374. MCACMP_CH3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH3 RST EN select 0h = Disabled 1h = Enabled

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Table 9-374. MCACMP_CH3_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	INP_SEL	R/W	Xh	McACMP CH3 input source seelct 0h = McACMP IN0 1h = McACMP IN1 2h = McACMP IN2 (or VCC) 3h = McACMP IN3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH3 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH3 hysteresis select 0h = 0mV 1h = 64mV 2h = 128mV 3h = 192mV

9.3.149 MCACMP_CH3_CFG1 Register (Offset = 3E1h) [Reset = X0h]

MCACMP_CH3_CFG1 is shown in Table 9-375.

Return to the Summary Table.

Table 9-375. MCACMP_CH3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH_VREF_SEL	R/W	0h	No. of VREF select 0h = 1 VREF 1h = 2 VREF 2h = Reserved 3h = Reserved
5:0	VREF_SEL	R/W	Xh	McACMP CH3_0 VREF select (same options as CH0_0)

9.3.150 MCACMP_CH3_CFG2 Register (Offset = 3E2h) [Reset = XXh]

MCACMP_CH3_CFG2 is shown in Table 9-376.

Return to the Summary Table.

Table 9-376. MCACMP_CH3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_SEL1	R/W	Xh	McACMP CH3_1 VREF select (same options as CH0_0)

9.3.151 AMUX0_CFG Register (Offset = 3E5h) [Reset = 0Xh]

AMUX0_CFG is shown in Table 9-377.

Return to the Summary Table.

Table 9-377. AMUX0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	AMUX_EN	R/W	Xh	AMUX EN 0h = Disabled 1h = Enabled

9.3.152 AMUX1_CFG Register (Offset = 3E6h) [Reset = 0Xh]

AMUX1_CFG is shown in Table 9-378.

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Table 9-378. AMUX1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	AMUX_EN	R/W	Xh	AMUX EN 0h = Disabled 1h = Enabled

9.3.153 SER_COMM_CFG0 Register (Offset = 3F2h) [Reset = X0h]

SER_COMM_CFG0 is shown in Table 9-379.

Return to the Summary Table.

Table 9-379. SER_COMM_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I2C_ADDR_SRC_SEL	R/W	0h	I2C HW address source select (bitwise) 0h = OTP 1h = IO
3	I2C_IO_LAT	R/W	Xh	I2C HW addressing IO latching select 0h = Enabled 1h = Disabled
2	I2C_RST_EN	R/W	Xh	I2C Global Reset listening select 0h = Disabled 1h = Enabled
1	I2C_EN	R/W	Xh	I2C serial communications enable select 0h = Disabled 1h = Enabled
0	SPI_EN	R/W	Xh	SPI serial communications enable select 0h = Disabled 1h = Enabled

9.3.154 SER_COMM_CFG1 Register (Offset = 3F3h) [Reset = 00h]

SER_COMM_CFG1 is shown in Table 9-380.

Return to the Summary Table.

Table 9-380. SER_COMM_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I2C_ADDR_MSB	R/W	0h	I2C HW address
3:1	I2C_ADDR_LSB	R/W	0h	I2C HW address
0	RESERVED	R	0h	Reserved

9.3.155 MISC_CFG0 Register (Offset = 3F7h) [Reset = 00h]

MISC_CFG0 is shown in Table 9-381.

Return to the Summary Table.

Table 9-381. MISC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_QC	R/W	0h	GPIO quick charge control 0h = Disabled 1h = Enabled
6	CFG_RD_LCK	R/W	0h	CFG read lock control 0h = Disabled 1h = Enabled
5	CFG_WR_LCK	R/W	0h	CFG write lock control 0h = Disabled 1h = Enabled
4	OTP_WR_LCK	R/W	0h	OTP write lock control 0h = Disabled 1h = Enabled

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Table 9-381. MISC_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	USER_LCK	R/W	0h	USER read/write lock control 0h = R/W to all non-reserved, non-read-only registers 1h = R/W to only Counter DATA, Watchdog Timer DATA, and Pattern Generator registers 2h = R/W to only State Machine registers 3h = R/W to only Voltage Reference select registers
1:0	RESERVED	R	0h	Reserved

9.3.156 DEVICE_ID4 Register (Offset = 3FAh) [Reset = X0h]

DEVICE_ID4 is shown in Table 9-382.

Return to the Summary Table.

Table 9-382. DEVICE_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID4	R	Xh	Device ID

9.3.157 DEVICE_ID5 Register (Offset = 3FBh) [Reset = X0h]

DEVICE_ID5 is shown in Table 9-383.

Return to the Summary Table.

Table 9-383. DEVICE_ID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID5	R	Xh	Device ID

9.3.158 DEVICE_ID6 Register (Offset = 3FCh) [Reset = X0h]

DEVICE_ID6 is shown in Table 9-384.

Return to the Summary Table.

Table 9-384. DEVICE_ID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID6	R	Xh	Device ID

9.3.159 DEVICE_ID7 Register (Offset = 3FDh) [Reset = X0h]

DEVICE_ID7 is shown in Table 9-385.

Return to the Summary Table.

Table 9-385. DEVICE_ID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID7	R	Xh	Device ID

9.3.160 CRC_LSB Register (Offset = 3FEh) [Reset = X0h]

CRC_LSB is shown in Table 9-386.

Return to the Summary Table.

Table 9-386. CRC_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC_LSB	R/W	Xh	CRC LSB for 2kb OTP

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9.3.161 CRC_MSB Register (Offset = 3FFh) [Reset = X0h]

CRC_MSB is shown in Table 9-387.

Return to the Summary Table.

Table 9-387. CRC_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC_MSB	R/W	Xh	CRC MSB for 2kb OTP

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The configurable logic and timing blocks of TPLD2001-Q1 allow for the device to provide symmetric power-up and power-down signals for numerous components. In this application the device is configured to output the maximum amount of power- up and power-down sequencing signals based on a counter/delay macro-cell.

10.2 Typical Application

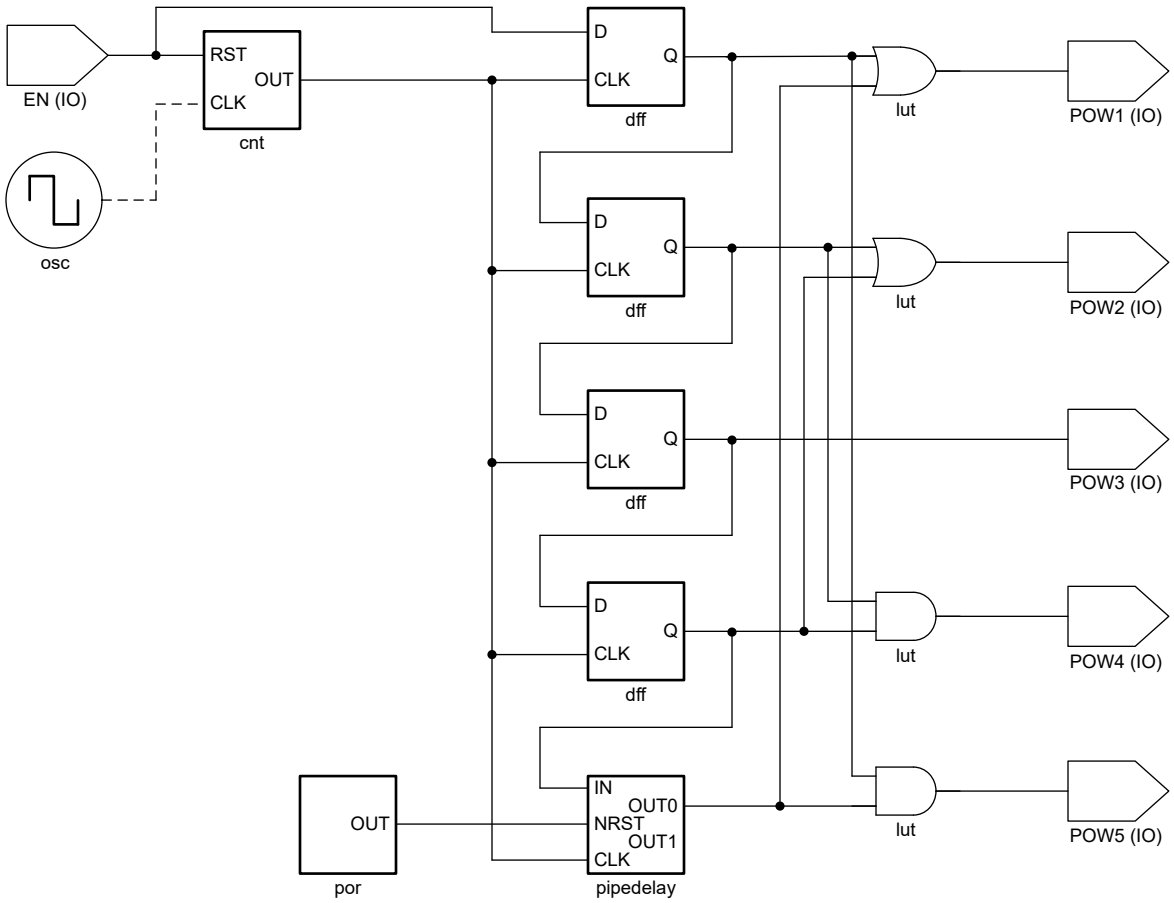

Figure 10-1. Typical Application Block Diagram

10.2.1 Design Requirements

10.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the TPLD2001-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the TPLD2001-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The TPLD2001-Q1 can drive a load with a total capacitance less than or equal to 15pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 15pF.

The TPLD2001-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} andV_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

10.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$or $V_{t-(min)}$ to be considered a logic LOW, and $V_{IH(min)}$or $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the unused inputs can be connected with a pull-up or pull-down resistor if the input is used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the TPLD2001-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The TPLD2001-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

The TPLD2001-Q1 can be used with no signal transition rate requirements because the device has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value provides the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

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10.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*.The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

10.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the TPLD2001-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation application note*.

10.2.3 Application Curves

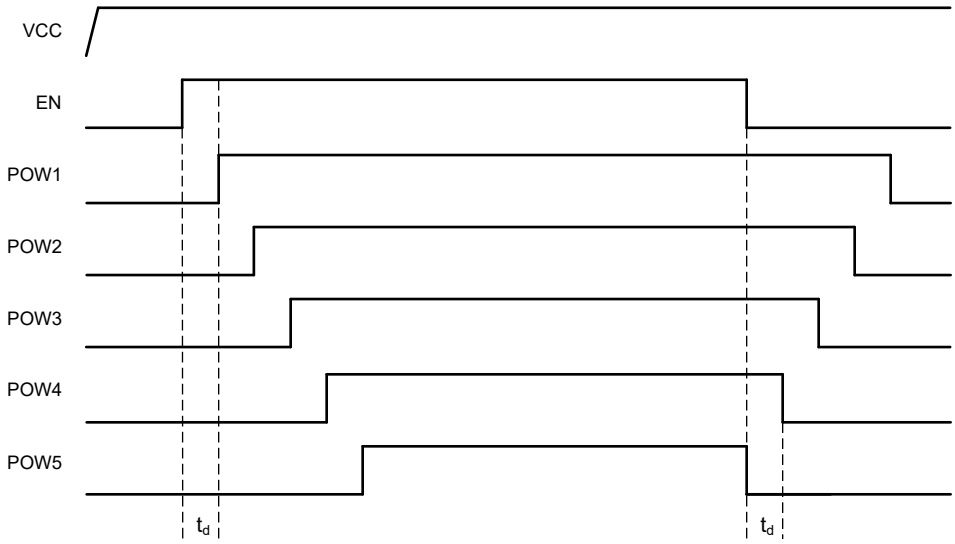

Figure 10-2. Application Timing Diagram

10.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. A design can use multiple bypass capacitors in parallel to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

10.4 Layout

10.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10.4.2 Layout Example

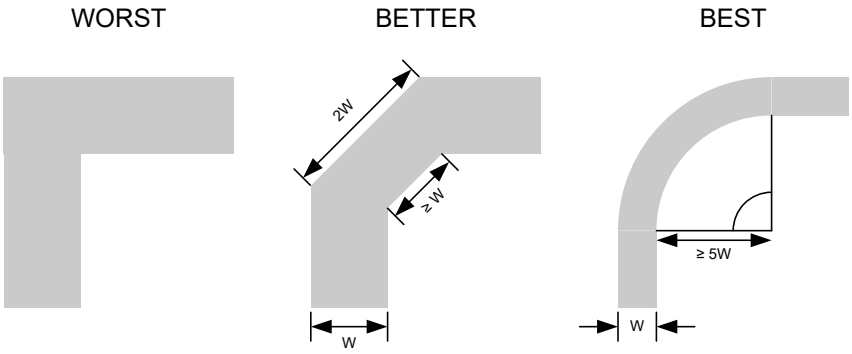

Figure 10-3. Example Trace Corners for Improved Signal Integrity

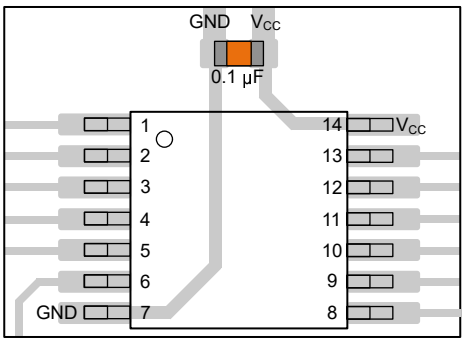

Figure 10-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

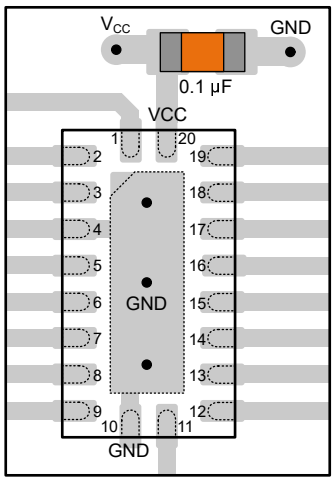

Figure 10-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

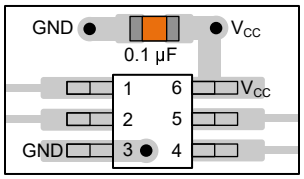

Figure 10-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

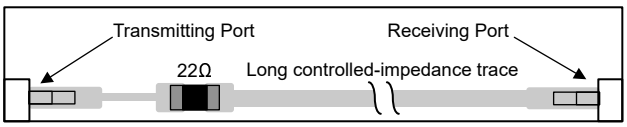

Figure 10-7. Example Damping Resistor Placement for Improved Signal Integrity

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2026) to Revision B (October 2026)	Page
• Added F_{IN_MAX} for IN0 to Recommended Operating Conditions	5

Changes from Revision * (July 2025) to Revision A (July 2026)	Page
• Updated device status from Advanced Information to Production Data	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPLD2001DGSRQ1	Active	Preproduction	VSSOP (DGS) | 20	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPLD2001DGSRQ1	Active	Production	VSSOP (DGS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TQ2001

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPLD2001-Q1 :

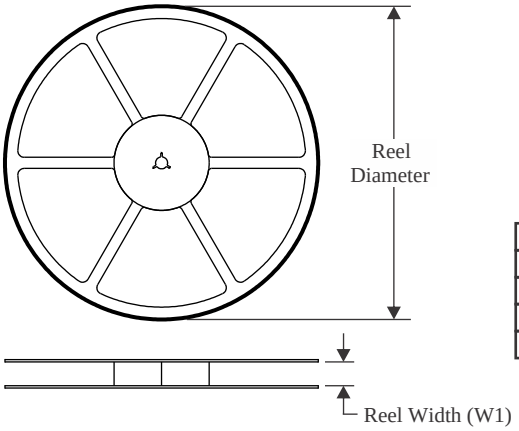
- Catalog : TPLD2001

NOTE: Qualified Version Definitions:

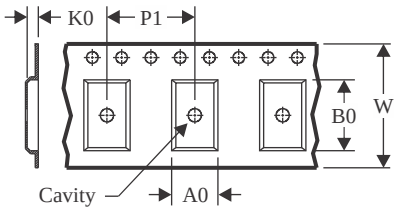
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

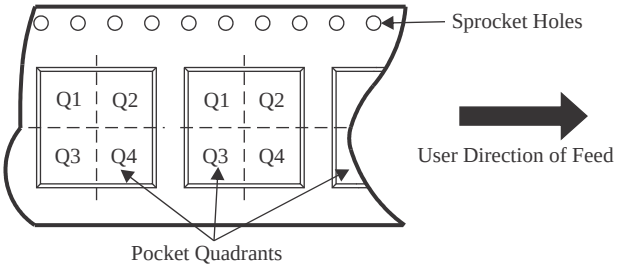


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

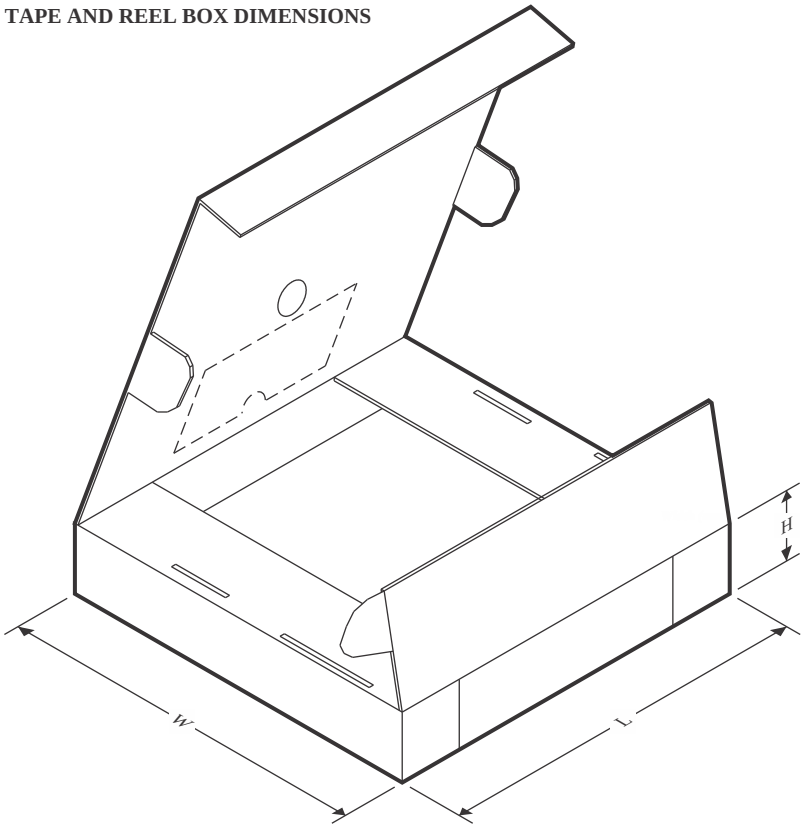
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

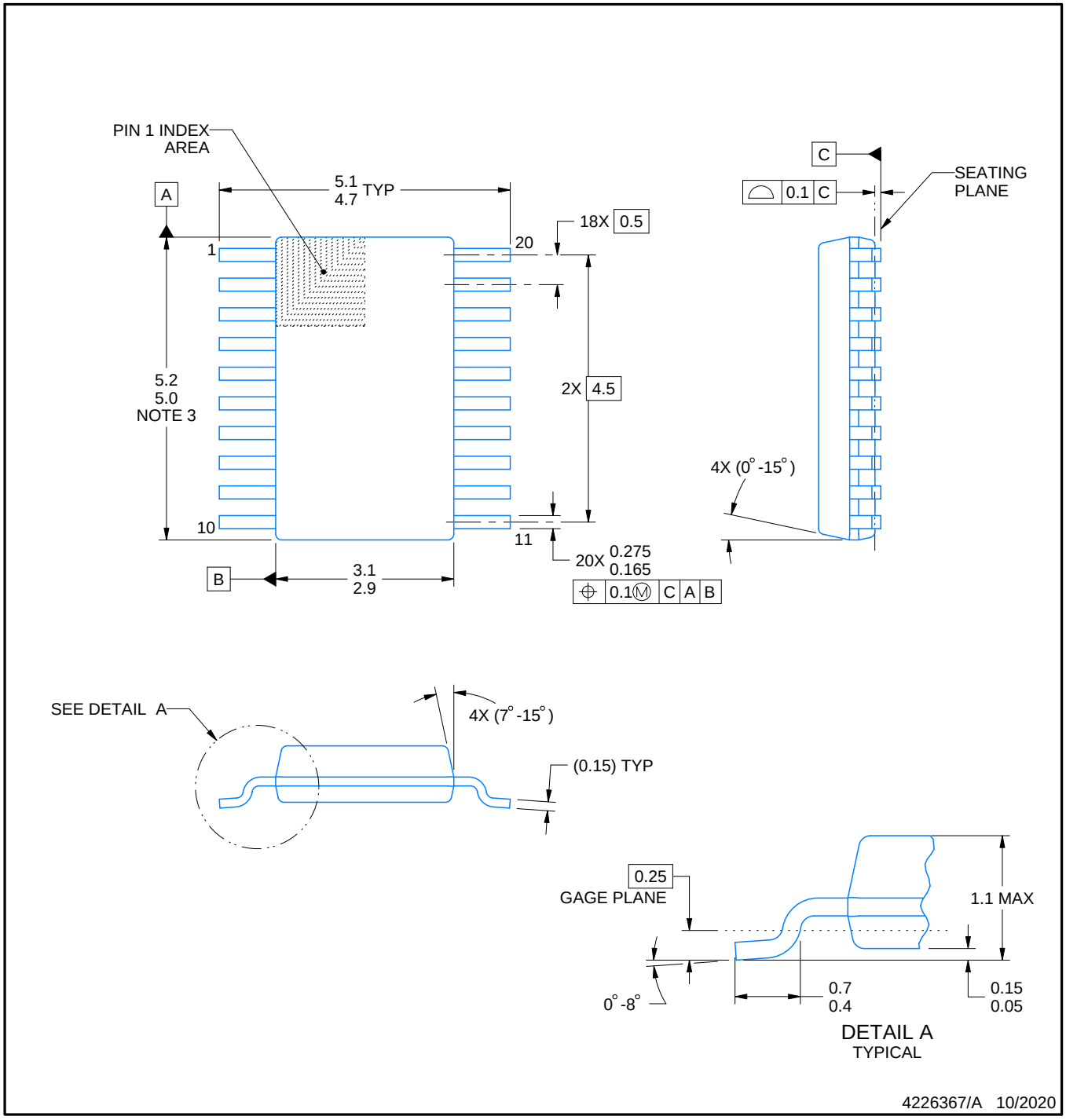
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPLD2001DGSRQ1	VSSOP	DGS	20	3000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

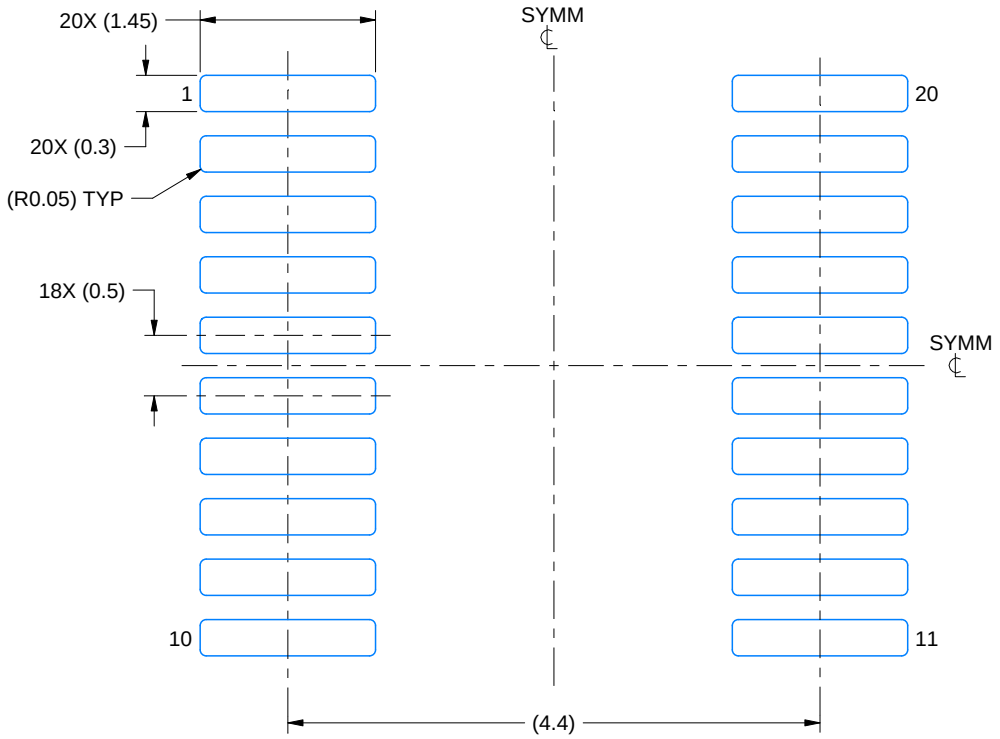
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPLD2001DGSRQ1	VSSOP	DGS	20	3000	353.0	353.0	32.0



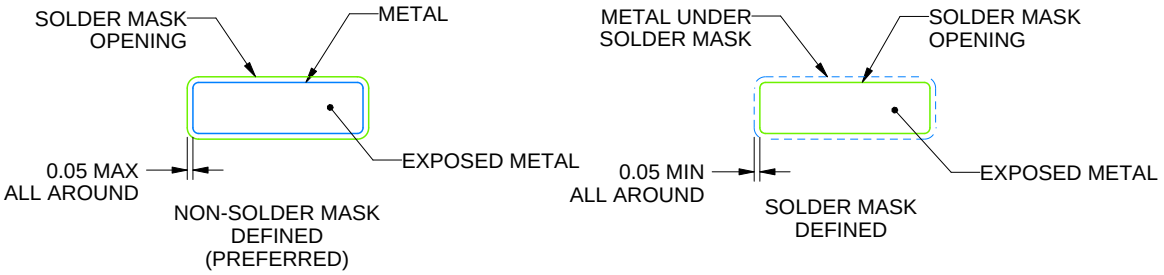
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X



SOLDER MASK DETAILS

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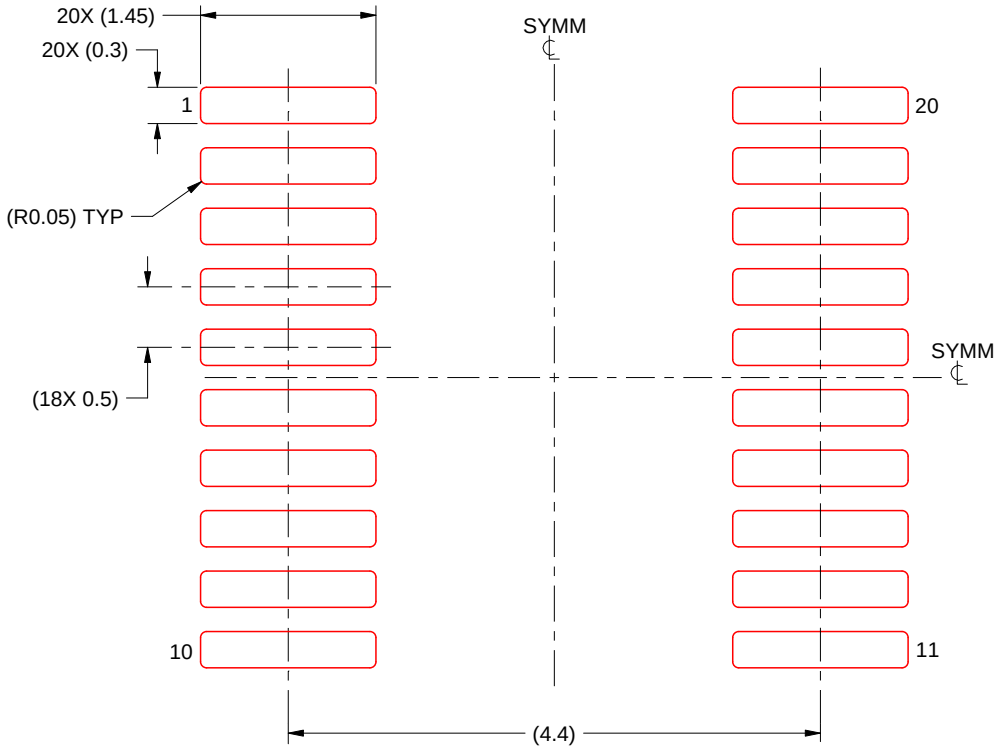
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025